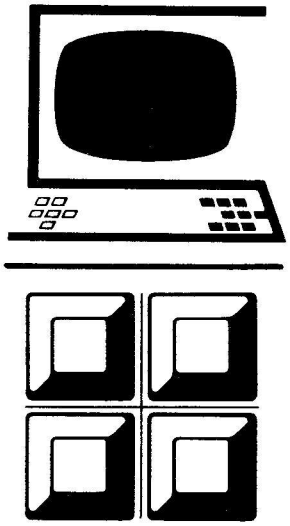
System 6300
Diagnostics Manual

SOFTWARE RELEASE ZF01



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Specifications subject to change.

This manual provides maintenance information for the Four-Phase System 6300 Processor and is intended for Four-Phase Customer Engineers trained on the System 6300 and TM6000 Workstation.

The introductory section of this manual provides a physical description and specifications of the System 6300.

Troubleshooting and corrective maintenance procedures for the System 6300 are provided to board and module level. Principles of operation of the System 6300 and assembly illustrations with part numbers are also included in this manual.

The Customer Engineer should have available the following Four-Phase hardware publications when responding to a system customer service call:

- System 6300 Diagnostic Manual (87601202)
- System 6300 Technical Manual (87601203)
- System 6300 Installation and User's Guide (87601199)
- TM6000 Workstation Service Manual (87601193)
- TM6000 Workstation Technical Manual (87601172)

These manuals should be referenced when more specific technical information is required.

Warning

This equipment generates, uses, and can radiate radio frequency energy and if not installed and used as described in the applicable installation manuals, may interfere with radio communications. It has been tested and found to comply with the limits for a Class A computing device pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference when operated in a commercial environment. Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

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The System 6300 Processor is a minicomputer using the CTIX operating system. With the maximum available storage, the computer includes 2M byte memory, a 40M byte fixed disc drive, and a 655K byte floppy disc drive. As a system host, the System 6300 can support a cluster of eight TM6000 workstations through the RS-422 port; one lineprinter through the lineprinter interface; and a letter quality printer and modem through the RS-232-C A and B ports. The Customer Engineer should be familiar with the features of the System 6300; however, an overview is provided in this section.

SYSTEM 6300 FEATURES

The System 6300 consists of the following features:

- Singleboard computer: the main processor houses the Motorola 68010 CPU, 1/2M byte memory, and disc and communications input/output.
- MC68010 CPU operating at 10 MHz with no wait states.
- Virtual address space of 4M bytes.
- Base memory of 1/2M bytes, expandable to 2M byte by adding one to three 1/2M byte memory expansion boards.
- Mass storage provided by a fixed disc of user selected capacity (10M byte to 40M byte) and a floppy disc drive.
- Two RS-232-C ports (A and B) and one RS-422 port.
- Multiuser demand-paged virtual memory CTIX operating system.
- Parallel printer port.

PHYSICAL DESCRIPTION

The System 6300 consists of a single enlosure having the following requirements:

- One main processor and zero to three memory expansion boards.
- Metal structure to support the main processor and memory expansion boards (when applicable) in the enclosure.
- One fixed disc drive and one floppy disc drive.
- Power supply module.
- Cabling between the power supply module and the boards and drives. Cabling between the drives and the main processor.
- Expansion boards connected through zero insertion force (ZIF) connectors.

The main processor is 15 inches by 18 inches. The expansion boards are 6 inches by 15 inches. All logic boards are four layers deep with complete uninterrupted ground planes.

Figure 1-1 shows the rear of the System 6300 Processor enclosure. The five status indicator lights are at the rear of the cabinet in the upper right-hand corner. The on/off switch and power plug is below and to the left of the indicator lights. The RESET switch is farther down and to the right, and the port input/ output connectors are above the RESET switch.

The main processor mounts on the swing-down side of the enclosure. The memory expansion boards attach to the main processor by the metal structure and zero insertion force (ZIF) connectors.

The fixed disc drive mounts vertically at the lower front of the system cabinet. If the system uses the floppy disc drive, the drive mounts vertically at the top front of the cabinet. (That is, the floppy disc drive opening is aligned vertically at the front of the cabinet.) If the system uses the removable-cartridge disc drive, the drive also mounts at the front of the cabinet, but horizontally.

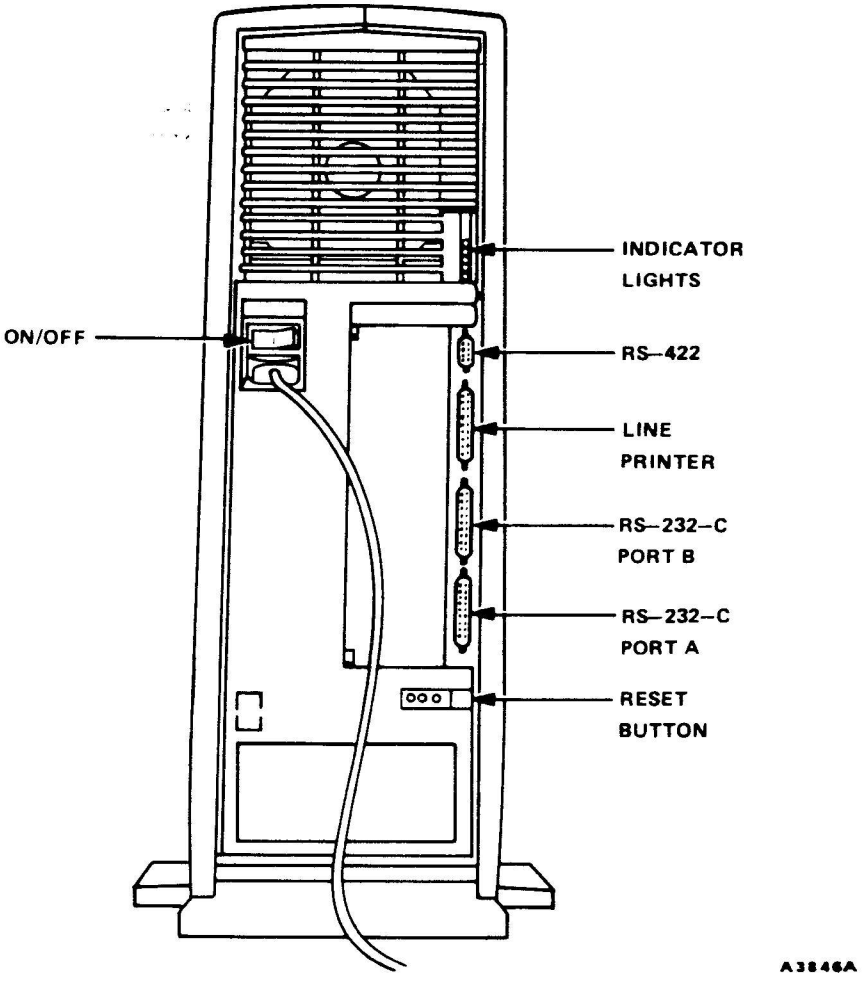

Figure 1-1. System 6300 Rear Panel

Figure 1-2 shows the interior of the System 6300 enclosure. This illustration shows the System 6300 with a floppy disc drive.

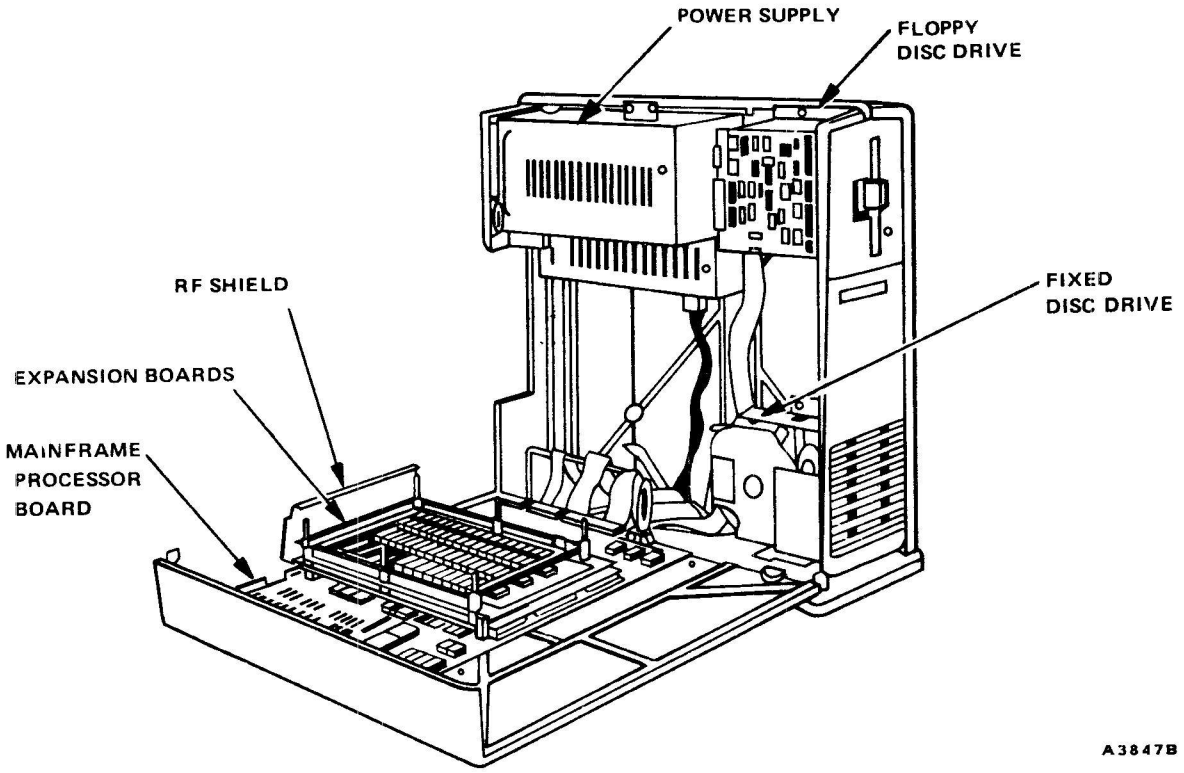

Figure 1-2. Interior of System 6300

SYSTEM 6300 SPECIFICATIONS

Table 1-1 lists the specifications for the System 6300:

Table 1-1. System 6300 Specifications

Physical Characteristics

Height: 22.5 inches (57.15 cm)
Width: 7.0 inches (17.78 cm), 10.0 inches (25.40 cm) including base
Depth: 23.0 inches (58.42 cm), (excluding 2 inch rear standoff)
Weight: 60 pounds (27.22 kilograms)

Electrical Characteristics

The input power requirements are:

Nominal	Voltage Range	Frequency Range
115V	85-130V RMS, 2.6 Amps	47 to 440 Hertz
230V	180-260V RMS, 1.3 Amps	47 to 440 Hertz

The ac loads specified above represent the loads presented to the line by a fully configured system.

Environmental Characteristics

Ambient Temperature

Operating: 50 degrees F (10 degrees C) to 104 degrees F (40 degrees C)

Non-operating: -40 degrees F (-40 degrees C) to 140 degrees F (60 dgrees C)

Relative Humidity

Operating: 5% to 95% RH, noncondensing
Non-operating: 5% to 95% RH, noncondensing

Altitude Limitations

Operating: Sea Level to 10,000 feet
Non-operating: Sea Level to 30,000 feet

Shock

Operating: 5g
Non-operating: 15g

SAFETY SPECIFICATIONS

The System 6300 meets or exceeds the following requirements:

UL 478 (EDP) and 114 (Office Equipment)
CSA 154 (EDP) and 143 (Office Equipment)
FCC Part 15, Subpart J, Class A
VDE 0730 Parts I and II
BSI BS 3861 Parts I, II, and III
ESD: 5,000 volts - no observable effect
15,000 volts - no operator perceived errors
25,000 volts - no permanent damage

This section provides information to help in locating System 6300 problems. The System 6300 troubleshooting flowchart shows the steps required for locating a defective processor or expansion board, disc drive, power supply module, or cable assembly. Refer to Section 3 for procedures on replacing these devices.

The status indicator lights (light emitting diodes) on the rear of the system are also described. The status indicator lights display boot program progress codes and failure codes.

SYSTEM 6300 TROUBLESHOOTING FLOWCHART

The System 6300 troubleshooting flowchart, Figure 2-1, shows steps required for troubleshooting the system and includes suggested corrective action. Follow this flowchart when troubleshooting the System 6300. As mentioned, procedures for replacing defective devices are provided in Section 3 of this manual.

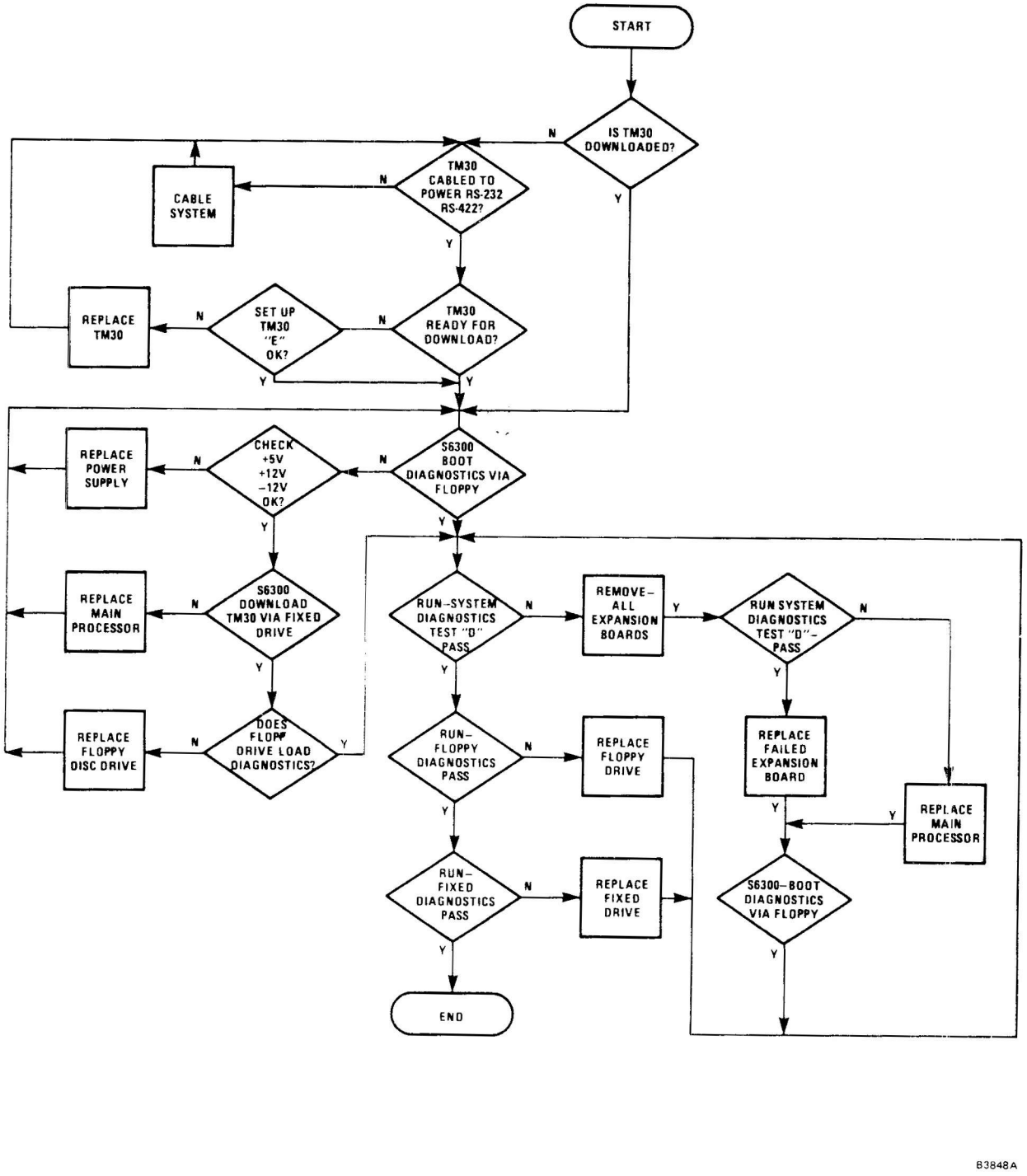

Figure 2-1. System 6300 Troubleshooting Flowchart

PROGRAM INDICATOR CODES

The boot program progress and failure codes are displayed through indicator lights (light emitting diodes) at the rear of the System 6300 enclosure. See Figure 2-2.

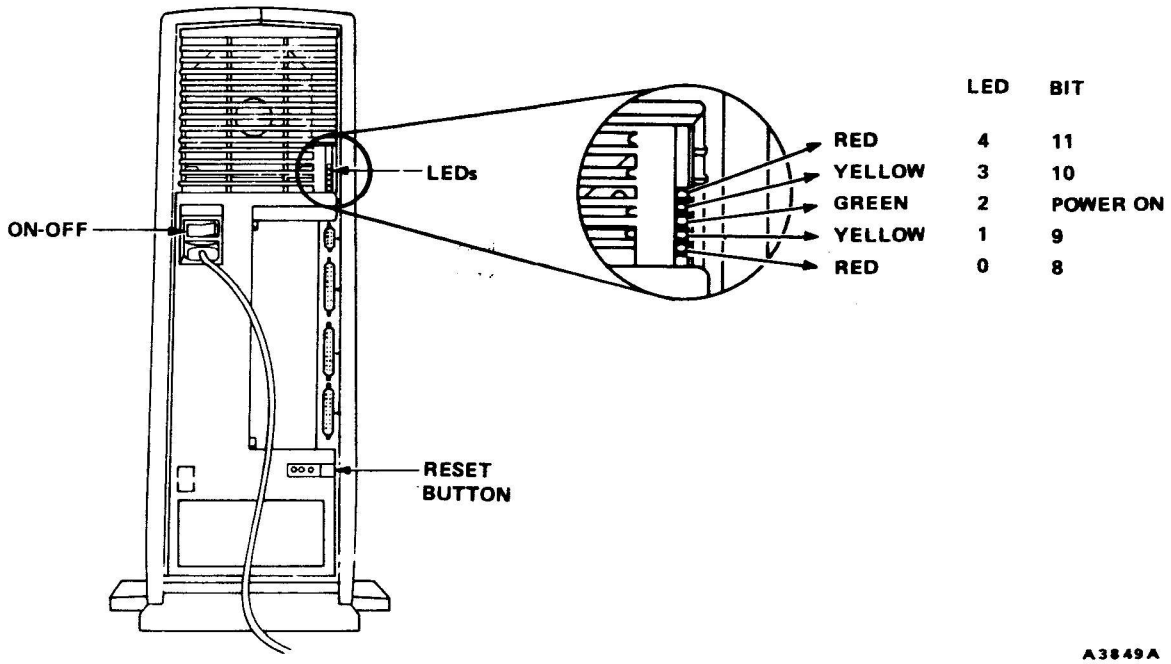

Figure 2-2. System 6300 Indicator Lights

There are five indicator lights mounted vertically and numbered from 0 to 4 (4 is at the top of the row of indicator lights).

- Red 4
- Yellow 3
- Green 2
- Yellow 1
- Red 0

Table 2-1 lists the various combinations of the indicator lights and their meanings for the boot program progress codes. The green indicator (2) in the center remains on when the System 6300 is powered up. Table 2-2 lists the failure program codes.

Table 2-1. Indicator Progress Codes

Indicator Light				Meaning
4	3	1	0	
on	off	off	off	Recalibrating discs.
on	off	off	on	Searching for loader. Loader searching for CTIX.
on	on	off	off	Loading loader. Loader loading CTIX.
on	off	on	on	Entering loader.
on	off	on	off	Searching for a dump area.
on	on	off	on	(1) Dumping to floppy. (2) Entering loaded program. (3) Booting from floppy.
on	on	on	off	(1) Dumping to cartridge. (2) Booting from cartridge. (3) Write memory test.
on	on	on	on	(1) Dumping to fixed disc. (2) Booting from fixed disc. (3) Address test occurring. (4) Initial reset before executing Boot routine.
off	off	off	off	Initialize timers and save status.
off	on	off	off	Debugger waiting for connection during down load.
on	off	off	off	Debugger doing download.

Table 2-2. Indicator Failure Codes

Indicator Light				
4	3	1	0	Meaning and Corrective Action
off	off	off	off	No problem.
off	off	off	on	FAIL1. Can't recall any disc. a. Replace the main processor. b. Replace the power supply module.
off	on	off	on	FAIL3. Can't find loader. (The Boot continues to search for a loader when FAIL3 is active.) Replace the software operating system of the floppy and fixed disc drives.
off	on	on	off	FAIL6. Write memory test fail. Replace the main processor.
off	on	on	on	FAIL7. Address memory test fail. Replace the main processor and memory expansion boards. See the System 6300 troubleshooting flowchart (Figure 2-1).

This section describes the procedures for replacing the System 6300 processor and expansion boards, disc drives, and power supply module. Before opening the System 6300 cabinet for maintenance, be sure the ac power cord is unplugged from the ac power source.

OPENING THE SYSTEM 6300 CABINET

Open the System 6300 cabinet by performing the following procedure:

1. Facing the front of the cabinet, allow about three feet on the left side for the cabinet side panel to open.

2. Place a small rod shaped tool such as a screwdriver into one of the two small openings on the top of the cabinet. Insert the tool about 1/2 inch into the opening and push down approximately 1/4 inch after contacting the lever lock. (This unlocks one of the two lever locks.)

3. While maintaining the downward pressure on the tool, force apart the unlocked half of the cabinet enough to unlock the lever (about 1/2 inch).

4. Repeat steps 2 and 3 to unlock the other lever.

5. Slowly lower the cabinet side panel until it is perpendicular to the system. See Figure 3-1.

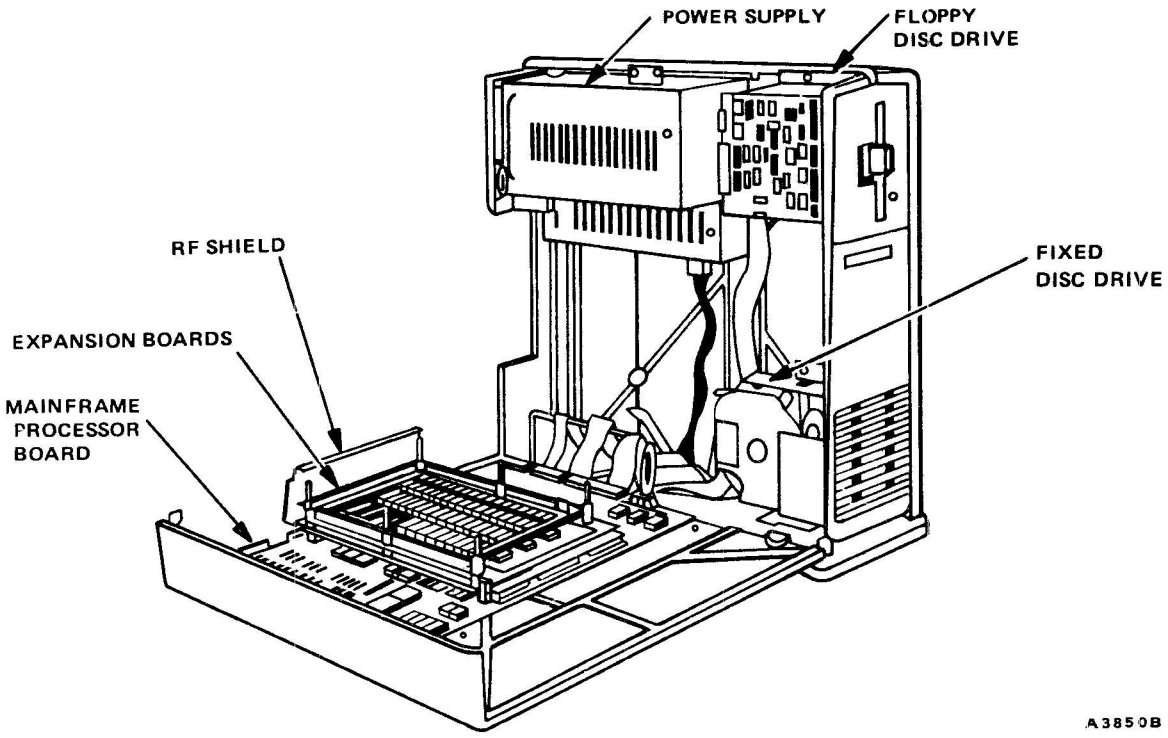

Figure 3-1. System 6300 Cabinet Opened

CLOSING THE SYSTEM 6300 CABINET

To close the System 6300 cabinet, perform the following procedure:

1. Swing the horizontal cabinet side panel (with processor and expansion boards attached) up until the lock levers on the horizontal portion are touching the locks on the vertical portion.

2. Slowly force the cabinet together, applying force at both lever lock points. When the levers snap into the locks, the cabinet is closed.

REPLACING THE MAIN PROCESSOR BOARD

To replace the System 6300 main processor, perform the following procedures:

1. Open the System 6300 cabinet. (See "Opening the System 6300 Cabinet" above.)

2. Remove the expansion boards. See "Replacing Memory Expansion Boards" in this section.

3. Disconnect the power supply cable, connector A1A1 P2, from the main processor at board location J21. See Figure 3-2.

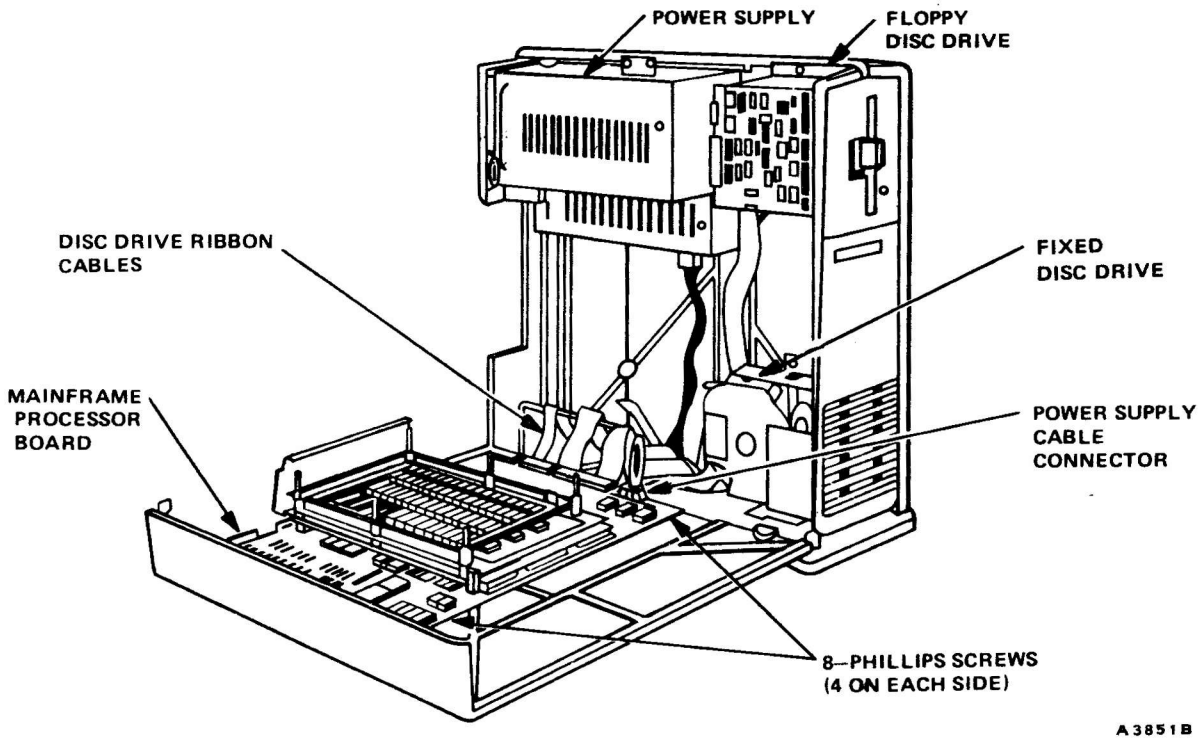

Figure 3-2. Main Processor Board

4. Disconnect the three disc drive ribbon cables from the main processor (Figure 3-2).

5. Remove the eight Phillips screws that secure the main processor to the System 6300 cabinet panel (Figure 3-2).

6. Remove the main processor.

7. Install the new main processor, replace the eight Phillips head mounting screws, and connect the cables.

8. Replace the expansion boards, if any. If a communications expansion board is included in the system configuration, replace it first. The communications expansion board should always be adjacent to the main processor.

REPLACING THE FLOPPY DISC DRIVE

To replace the System 6300 floppy disc drive, perform the following procedures:

1. Open the System 6300 cabinet. (See "Opening the System 6300 Cabinet" above.)

2. Disconnect the ribbon cable marked A1A2 P2P3 from the floppy disc drive printed circuit board. See Figure 3-3.

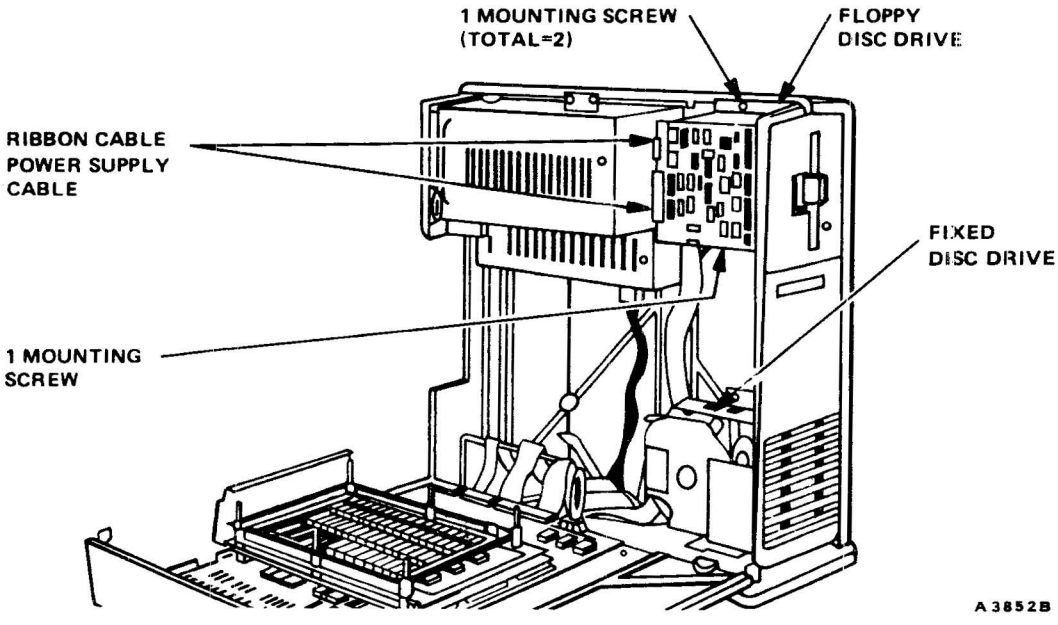

Figure 3-3. System 6300 Floppy Disc Drive

3. Disconnect the power supply cable marked A1A3 P3 from the floppy disc drive printed circuit board (Figure 3-3).

4. Remove the two Phillips screws that secure the floppy disc drive to the cabinet (Figure 3-3). Hold the floppy disc drive with one hand while removing the last screw.

5. Slide the floppy disc drive towards the power supply approximately 3/4 inches to clear the cabinet molding and remove the drive.

6. Install the new floppy drive, replace the two Phillips mounting screws, and connect the cables.

REPLACING THE FIXED DISC DRIVE

To replace the System 6300 fixed disc drive, perform the following procedures:

1. Open the System 6300 cabinet. (See "Opening the System 6300 Cabinet" above.)

2. Carefully disconnect the two ribbon cables marked A1A3 P1 and A1A3 P2 from the fixed drive printed circuit board. See Figure 3-4.

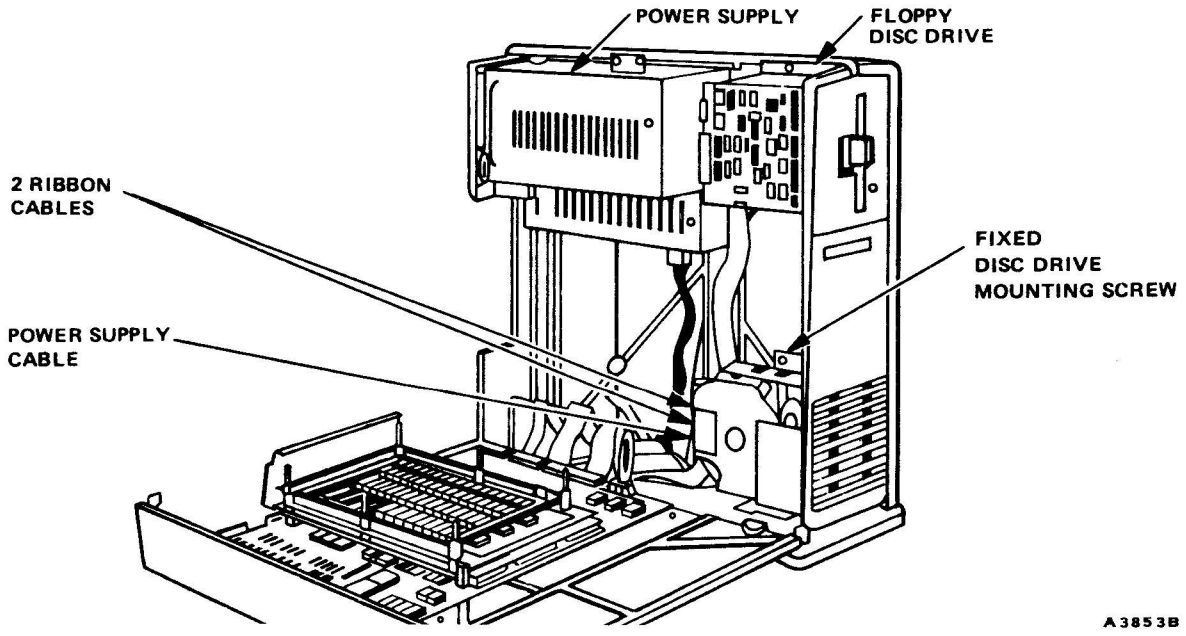

Figure 3-4. System 6300 Fixed Disc Drive

3. Disconnect the power supply cable, A1A3 P3, from the printed circuit board (Figure 3-4).

4. Remove the Phillips mounting screw located on top of the fixed disc drive (Figure 3-4).

5. Remove the fixed disc drive.

6. Install the new fixed disc drive, replace the Phillips mounting screw, and connect the cables.

REPLACING THE POWER SUPPLY MODULE

To replace the System 6300 power supply, perform the following procedures:

1. Open the System 6300 cabinet. (See "Opening the System 6300 Cabinet" above.)

2. Disconnect the power supply cable for the main processor, A1A4 P28, and disc drives, A1A1 P3, located underneath the power supply enclosure. See Figure 3-5.

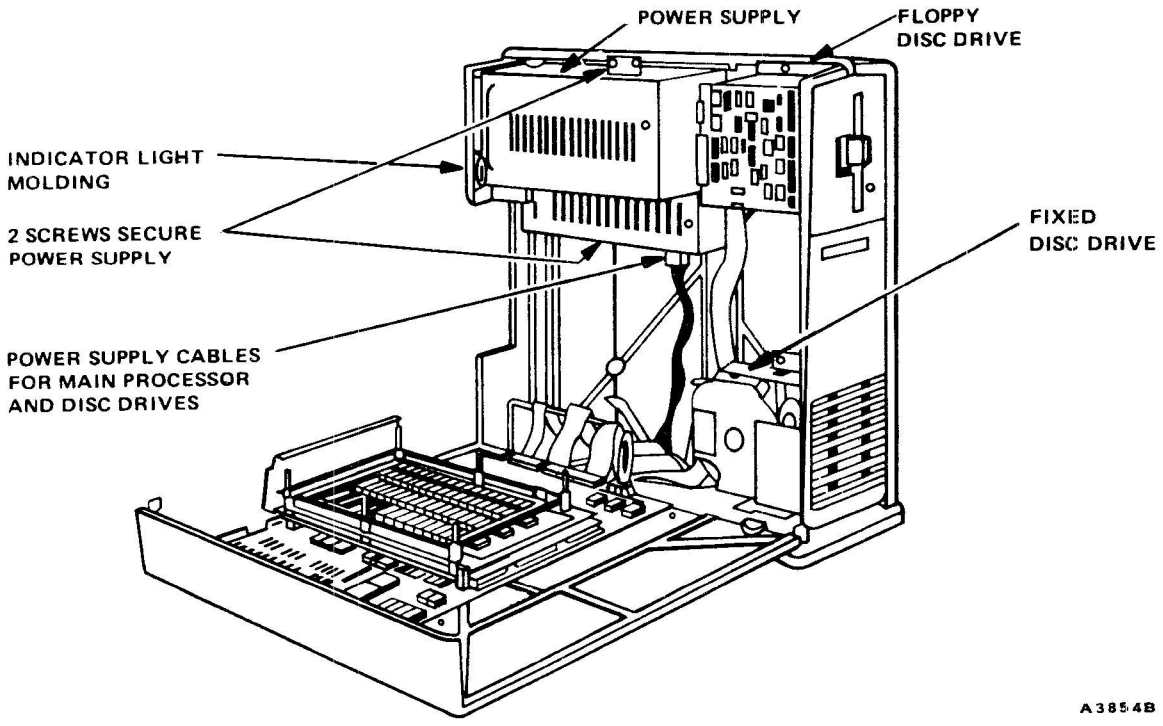

Figure 3-5. System 6300 Power Supply Module

3. Remove the two Phillips mounting screws securing the power supply module to the System 6300 cabinet (Figure 3-5). Hold the power supply module with one hand while removing the last screw.

4. Slide the power supply approximately 1/4 inch towards the floppy disc drive in order to clear the cabinet molding for the main processor indicator lights (Figure 3-5). Also, molded hooks on the rear panel must be fully engaged in mating holes on the power supply.

5. Remove the power supply module from the cabinet.

6. Install the new power supply module, replace the two Phillips mounting screws, and connect the cables marked A1A4 P28 and A1A1 P3.

REMOVING THE POWER SUPPLY MODULE COVER

To remove the power supply module cover, perform the following procedure:

1. Loosen the two power supply cover screws located on the right of the power supply module. See Figure 3-6.

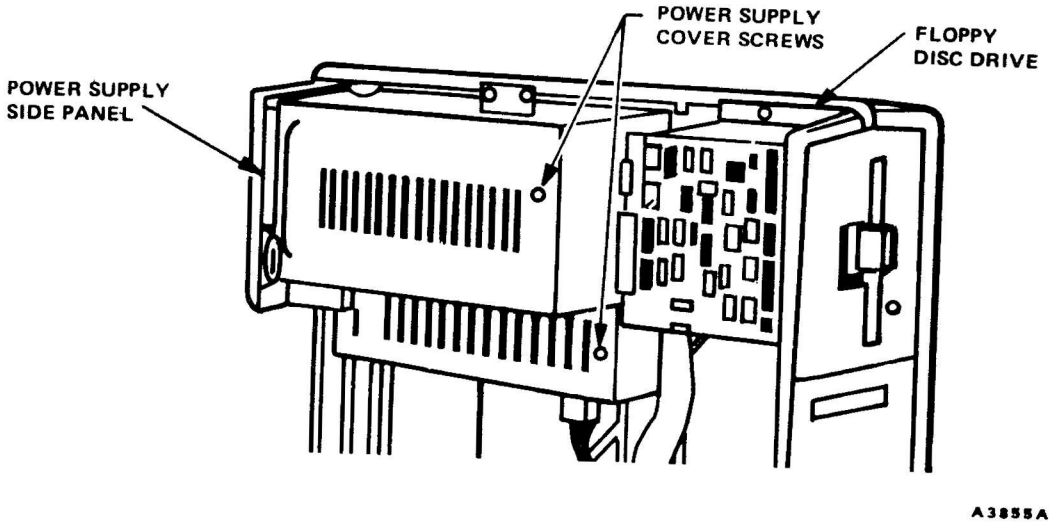

Figure 3-6. Power Supply Module Cover

2. Slide the cover out of the power supply module side panel to the right approximately 1/2 inch and remove (Figure 3-6).

3. Install the power supply module cover by sliding it back into the power supply side panel and tighten the cover screws.

REPLACING MEMORY EXPANSION BOARDS

The System 6300 supports from one to three memory expansion (ME) boards and one communications expansion board. When installing or removing expansion boards, be aware of the following:

- Expansion boards require no cabling; zero insertion force (ZIF) connectors on each board connect the boards to each other and to the main processor. The ZIF connector pins must be clean and straight.
- Expansion boards stack on top of the main processor and are supported by a threaded-stud metal structure that contains six rods. Nuts are screwed down onto the studs securing the boards.
- If the optional communications expansion board is installed, it must be installed closest to the main processor, underneath any memory expansion boards.

Memory Expansion Requirements

Table 3-1 lists the number of memory expansion (ME) boards needed for each system memory configuration.

Table 3-1. Memory Expansion Requirements

System Memory	Additional Boards
.5M byte	No ME boards
1.0M byte	One ME board
1.5M byte	Two ME boards
2.0M byte	Three ME boards

Expansion Board Jumpers

The 1/2M byte base memory of the System 6300 is expandable to 2M byte by adding one to three 1/2M byte memory expansion boards. Two jumpers are used on each memory expansion board to configure the memory address range for that board. The location of the two jumpers on the expansion boards is MA19 and MA20. See Figure 3-7. (On certain vendor expansion boards MA19 is identified as E1 and MA20 is identified as E2.)

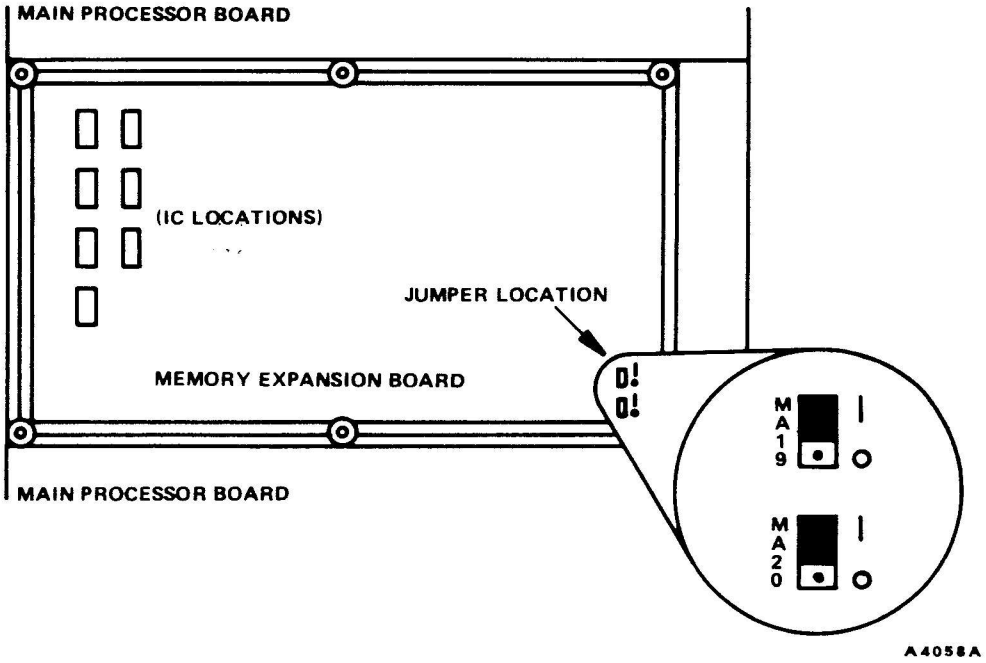

Figure 3-7. Memory Expansion Board Jumper Location

Table 3-2 lists the jumper settings for the address range for each physical memory board location. All boards must be strapped leaving no "holes" or "gaps" in memory. Note the jumper positions in Figure 3-7.

Table 3-2. Address Range Jumpers

Physical Location	Addressing Range	MA19 (E-1)	MA20 (E-2)
Main Processor Board	$000000 - 07FFFE	off	off
First expansion board	$080000 - 0FFFFE	on	off
Second expansion board	$100000 - 17FFFE	off	on
Third expansion board	$180000 - 1FFFFE	on	on

Adding an Expansion Board

To add a memory expansion board, perform the following procedures:

1. Open the ZIF connector on the expansion board by pulling the plastic ZIF actuator lever away from the board as far as the lever will go (approximately 1/2 inch). See Figure 3-8.

2. Center the expansion board over the threaded-stud metal structure and slide the board down until it lies flush with the board underneath it; make sure the ZIF connectors line up.

NOTE

Use care when securing the delicate ZIF connectors. Force can cause damage.

3. Install and finger-tighten the six nuts that secure the board.

4. To close the ZIF contacts, slowly push the plastic ZIF lever towards the expansion board, keeping the lever exactly perpendicular to the side of the board (Figure 3-8).

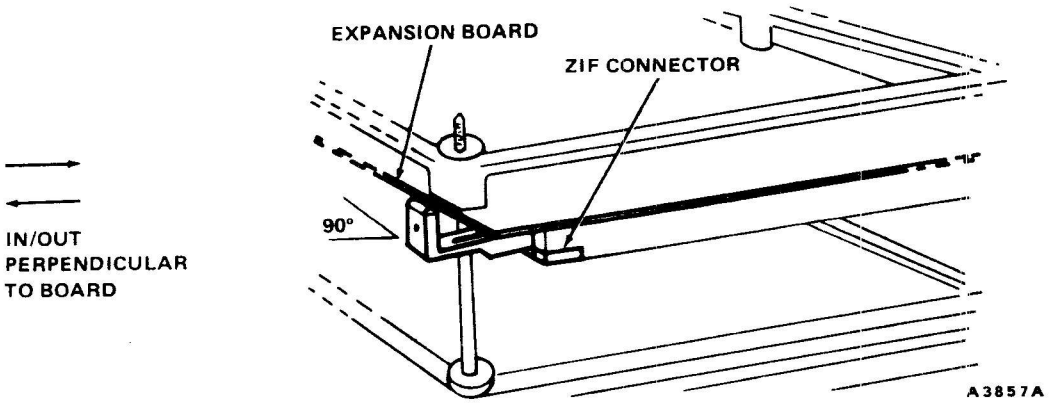

Figure 3-8. Expansion Board ZIF Connector

NOTE

Do not force the lever at an angle; this will cause irreparable damage to the board and connector.

5. When the end of the ZIF lever is flush with the board, the ZIF contacts are then closed, and the board is installed.

Removing an Expansion Board

The System 6300 expansion boards can be removed one at a time or as one stack from the main processor. To remove an expansion board, perform the following procedure:

1. Pull the expansion board ZIF actuator lever out from the board (Figure 3-8) until the lever will not pull further (approximately 1/2 inch).

2. Loosen and remove the six nuts that secure the board to the threaded-stud metal structure.

3. Slowly remove the board by lifting it away from the metal structure.

4. Replace and hand tighten the six nuts.

5. Close the System 6300 cabinet. (See "Closing the System 6300 Cabinet" above.)

REPLACING FLOPPY AND FIXED DISC DRIVE RIBBON CABLES

To replace the floppy and fixed disc drive ribbon cables, perform the following procedures:

1. Open the System 6300 cabinet. (See "Opening the System 6300 Cabinet" above.)

2. Remove the power supply. See "Replacing the Power Supply Module" in this section.

3. Disconnect the ribbon cables at both floppy (A1A2 P1) and fixed (A1A3 P1 and A1A3 P2) drives.

4. Disconnect the power supply cable, A1A3 P3, from the fixed disc drive printed circuit board.

5. Remove the ribbon cable trough cover that secures the ribbon cable to the cabinet wall. Figure 3-9 shows the location of the cable trough cover in the System 6300 cabinet.

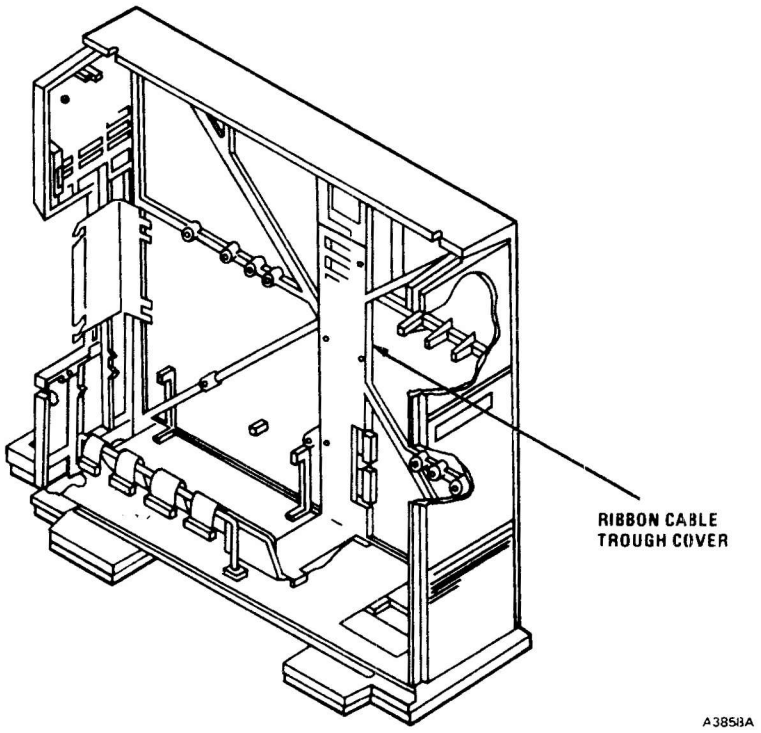

Figure 3-9. Ribbon Cable Trough Cover

6. Disconnect the ribbon cables from the main processor connector locking tabs on the main processor connectors and slide the ribbon cable out. See Figure 3-10.

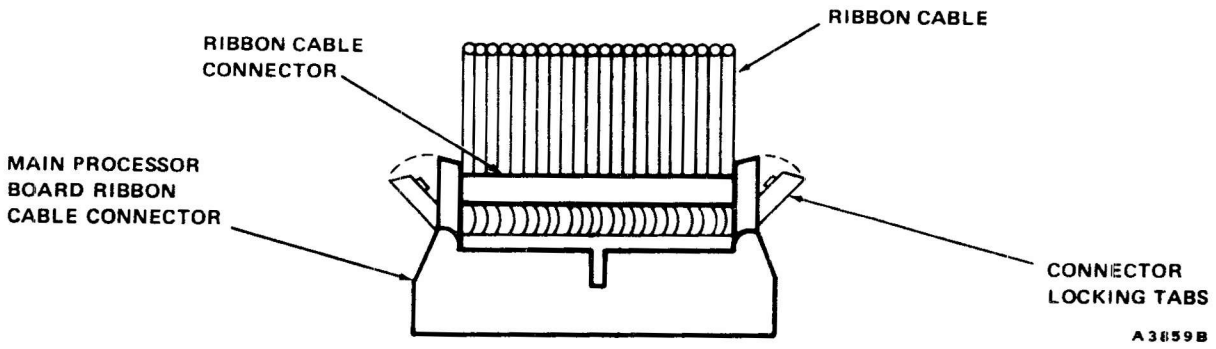

Figure 3-10. Main Processor Board Ribbon Cable Connector

7. Remove the ribbon cables from the System 6300 cabinet.

8. Replace the ribbon cable trough cover, power supply, and connect cables for the power supply.

POWER SUPPLY VOLTAGE ADJUSTMENT

The power supply voltages are checked at the power cable connector on the main processor. See Figure 3-11.

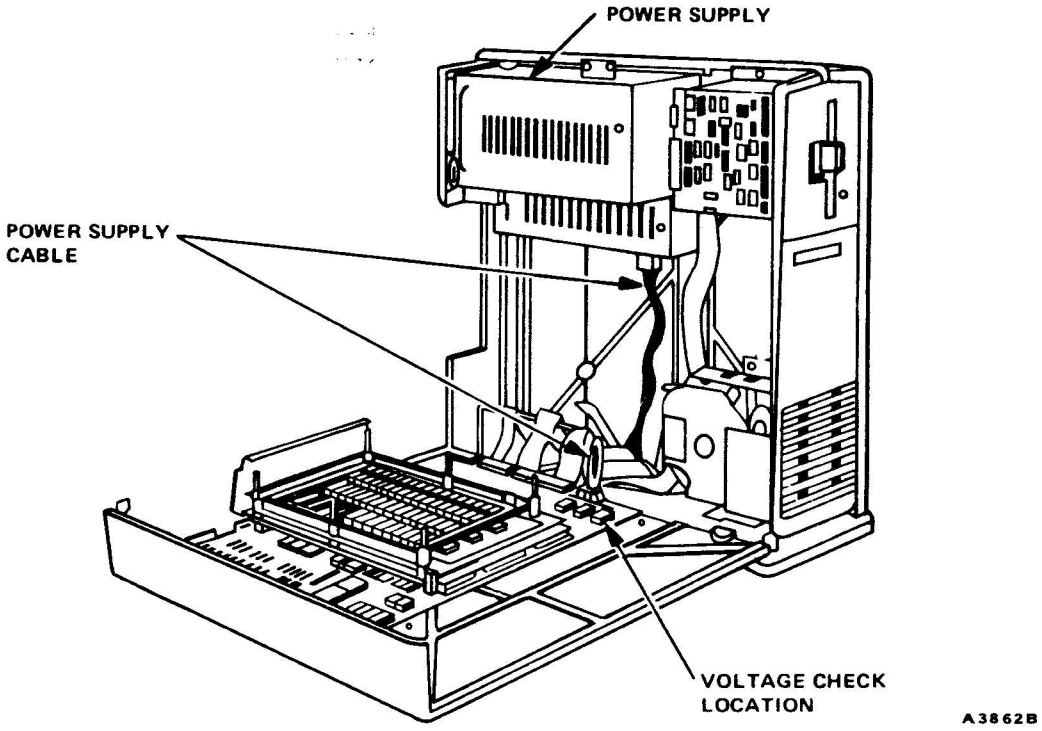

Figure 3-11. Power Voltage Check Location

Checking Voltages

To check the voltages, perform the following procedures:

1. Place the ground lead of the voltmeter to the ground position on the main processor's power connector, J21, pin 9. See Figure 3-12.

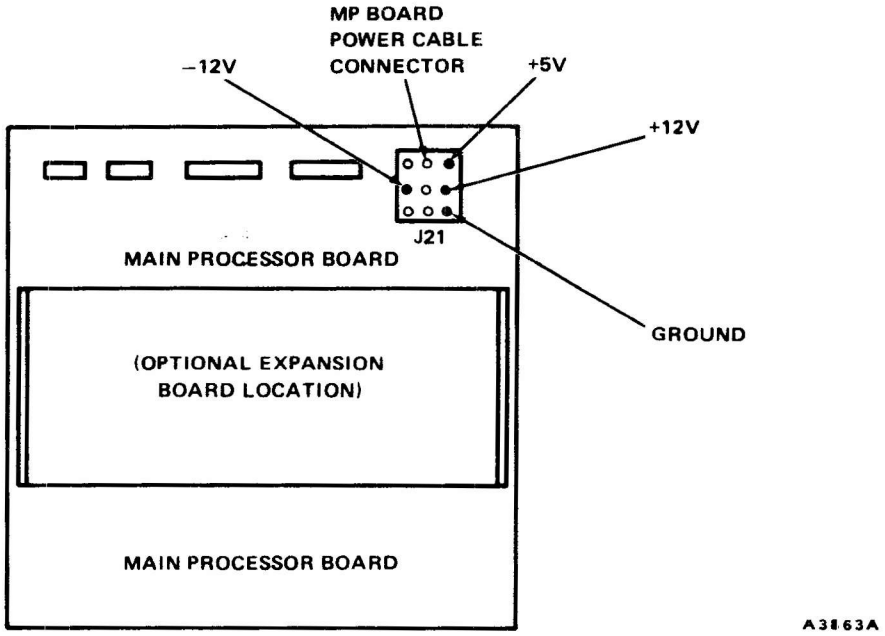

Figure 3-12. Power Connector Voltage Check Points

2. With the ground lead connected to ground, pin 9, place the positive lead from the voltmeter to check +5V, pin 7, on the power connector (Figure 3-12).

3. To check +12V, place the positive lead from the voltmeter to +12V, pin 8, on the power connector (Figure 3-12).

4. Repeat step 3 for -12V, pin 2 (Figure 3-12).

Adjusting +5 Volts

The only adjustable power supply voltage is the +5V potentiometer. To adjust the +5V, perform the following procedure:

1. Remove the power supply module cover. See "Replacing the Power Supply Module Cover" in this section.

2. Locate the +5V adjustable potentiometer. See Figure 3-13.

NOTE

Be careful not to touch the power wire harness that connects the ac source to the power supply module since power is applied to check voltages. See Figure 3-13.

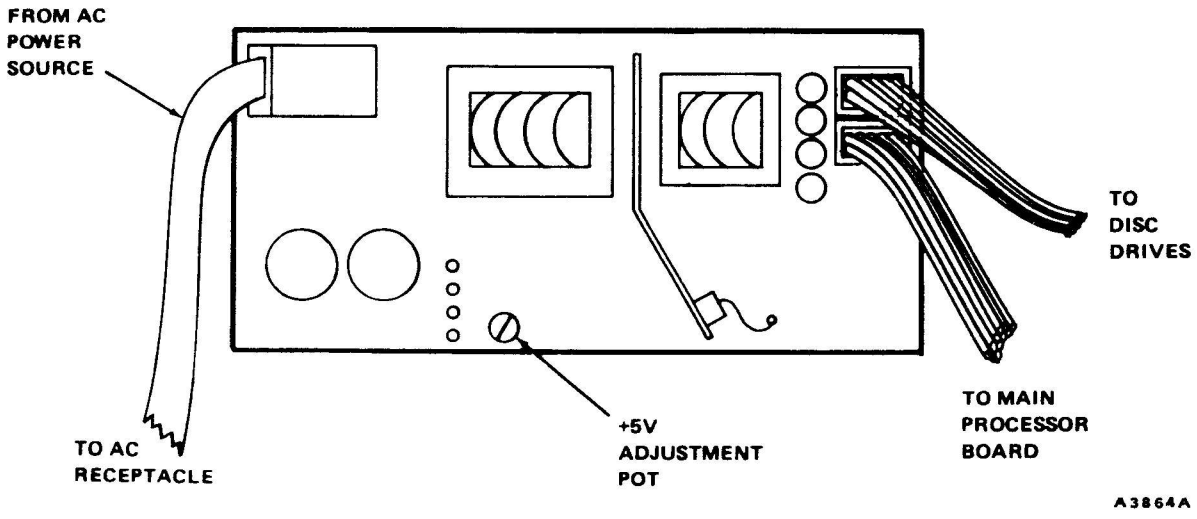

Figure 3-13. Adjustment for +5V

3. Adjust the +5V pot until the voltmeter reading is within the tolerance of 4.9 to 5.1 volts.

4. Replace the power supply module if the +5V reading is out of the specification tolerance.

This section describes the basic functions of the microprocessor operations within the System 6300. See Table 4-1. A detailed functional description is discussed in the System 6300 Technical Manual. The System 6300 is made up of five basic functions:

- System Control
- Processor Control
- Memory Control
- Input/output
- Interrupt Control

Table 4-1. System 6300 Functions

System Function	Function Elements
System Control	System clocks Bus control System reset Status indicator lights
Processor Control	CPU CPU State Machine Bootstrap ROM Processor buffers Address decode logic System 6300 processor registers
Memory Control	Map logic Memory access control Onboard and expansion RAM memory Parity logic Refresh logic Memory error control
Input/output	Disc Control Fast Communications (RS-422) Port Slow Communications (RS-232-C) Port Printer port External port (optional Ethernet expansion)
Interrupt Control	Interrupt Controller Interrupt Control PAL Interrupt Acknowledge PAL

Figure 4-1 shows the functional block diagram of the System 6300.

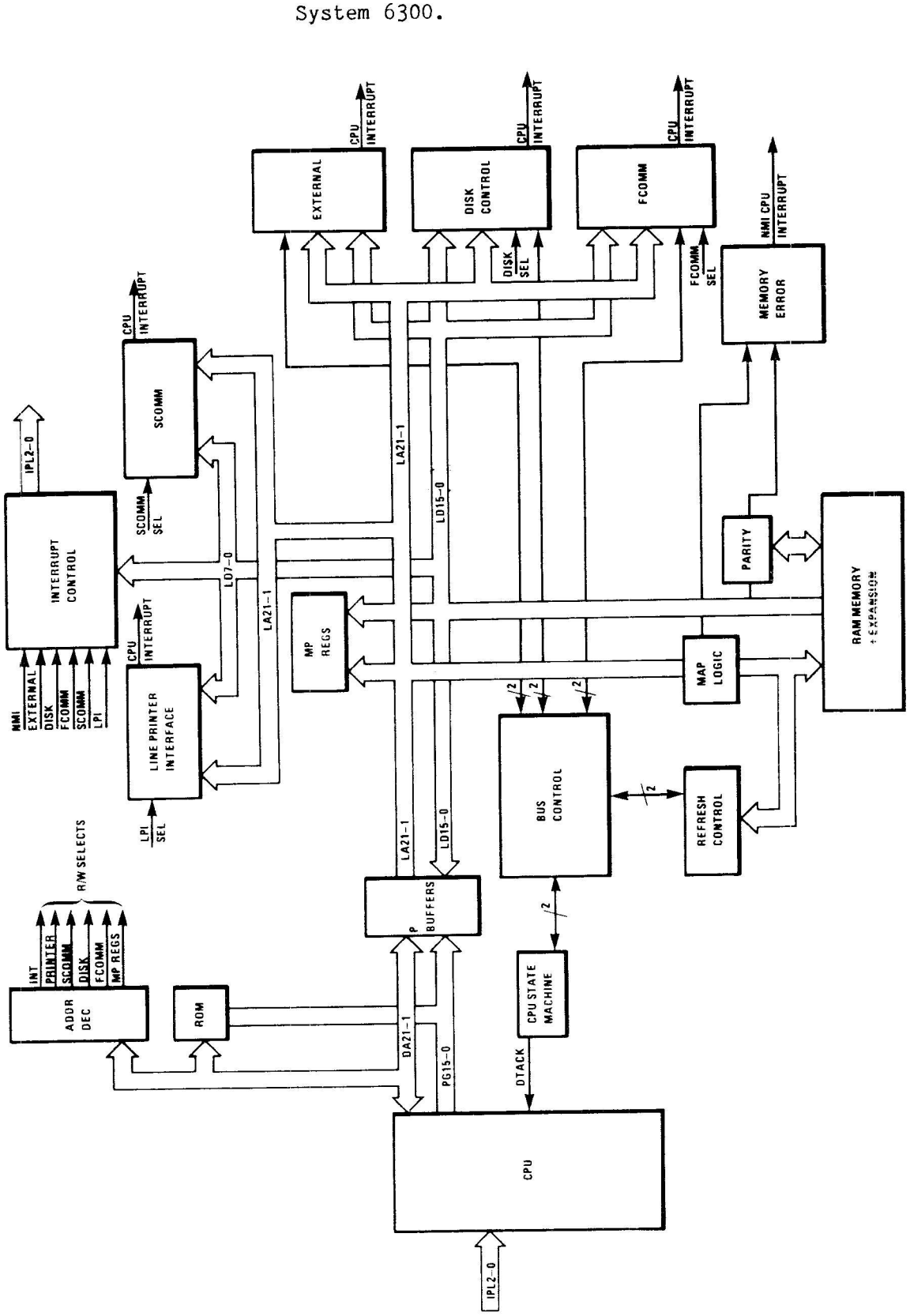

Figure 4-1. System 6300 Functional Block Diagram

SYSTEM CONTROL

The system control directs and monitors overall system activity. It generates the system clocks, controls bus arbitration, performs system reset, and, under the operating system, sets or resets the system status indicators.

When under the operating system mode, the CPU controls system activity including DMA set up, processor register read/writes, map register accessing, and memory page allocation.

System Clocks

The System 6300 has two system clocks, PCLK and PCLK inverted, and two local clocks, 20 MHz and 20 MHz inverted. The clocks trigger all synchronous local activities. The clock circuitry contains several additional clocks, for specific hardware, generated by the 20 MHz clock.

Bus Control

The bus control contains two elements:

- Bus arbiter
- Miscellaneous control programmable array logic (PAL)

The bus arbiter directs local system activity by receiving bus requests from the CPU and input/output elements. The local system consists of elements on the main processor and memory expansion boards. The bus arbiter also grants bus control according to the following priority scheme:

1. External port (optional)
2. Disc control
3. RS-422 fast communications port
4. Refresh control
5. CPU

The CPU requests bus control to perform memory accesses or register read/writes. The refresh control requests bus control to refresh the dynamic memory. All the other elements request bus control for DMA transfers.

The bus arbiter allows continuous local transfers to occur with no wait time between transfers; if, at the end of a local transfer, another request is pending, the arbiter immediately sends a new bus grant and the next transfer begins. No input/output device performs two successive transfers, however, because of recovery time built into the request/grant protocol.

The miscellaneous control PAL directs certain parts of memory accesses such as parity and byte select.

System Reset

There are three ways to reset the System 6300 hardware, including CPU: by software (through the reset command), by hardware (through the RESET switch), or by a power-on.

PROCESSOR CONTROL

The processor control centers around the 32-bit Motorola MC68010 CPU and includes the processor registers, CPU state machine, processor buffers, process address decode, and status indicator lights.

CPU

The MC68010 performs seven basic system cycles:

- CPU fast cycle and slow cycle read
- CPU fast cycle and slow cycle write
- CPU read-modify-write (test and set)
- CPU space (slow cycle interrupt acknowledge)
- Bus error
- Halt
- Reset

Fast cycle transfers are CPU accesses to either memory, the processor registers, or the map registers. Fast cycle transfers last 400 nanoseconds. (Fast cycle transfers also include DMA transfers, between either the disc control or fast communications port and memory, and the refresh cycle.)

Slow cycle transfers are CPU accesses to either the timers, the input/output device registers, or ROM. Slow cycle transfers, lasting 1000 nanoseconds, take longer because of the slower response time of the addressed device. The CPU interrupt-acknowledge cycle is a special type slow cycle transfer.

From the CPU's viewpoint, fast and slow cycle transfers are identical, except that the CPU enters wait states during slow cycle transfers while it waits for an acknowledge signal. When doing the read-modify-write cycle, after the read portion, the CPU performs wait states to allow any pending DMA requests to proceed. The CPU does the write portion when the system is idle.

CPU State Machine

The CPU state machine is a state sequencer consisting of a single PAL. During CPU read/writes, the machine synchronizes the CPU to the bus arbiter, memory control, and interrupt control.

Processor Buffers

Two sets of buffers, the P-address buffers and P-data buffers, route the processor address and processor data buses to the logical address and logical data buses (the local system buses).

Bootstrap ROM

Upon a system power-up or reset, the CPU automatically addresses ROM (through the ROM enable bit in the general control register). A bootstrap routine directs the CPU to initialize the System 6300 and read in the operating system from the disc.

Processor Registers

The MC68010 processor has five control and status registers:

- General control register
- General status register
- Clear status register
- Bus status register
- System reset register

These registers are described in the System 6300 Technical Manual.

Processor Address Decode

The processor address decode include four programmable array logics (PAL):

- Device select PAL
- Processor register-address decode PAL
- Two input/output device register-address decode PALs

During CPU read/write transfers, the device select PAL decodes the processor address. The PAL outputs a select signal to the element the CPU is addressing and, if necessary, enables the processor buffers. If the CPU accesses a processor or input/output device register, the device select PAL enables the applicable address decode PAL, and the PAL asserts the register read/write signal(s).

Status Indicator Lights

There are five status indicator lights, visible from the back of the System 6300 cabinet. Four lights are associated with bits in the general control register. The operating system turns these on and off. The other light (green indicator in the center of the five lights) indicates that the System 6300 is powered-up.

MEMORY CONTROL

Memory control contains six main elements:

- Map logic
- Memory access control
- Base (onboard) and expansion RAM memory
- Parity logic
- Refresh logic
- Memory error control

Map Logic

The system virtual address space is 24 bits long. The virtual memory space (4M byte) comprises one quarter to the total system space. All register or memory accesses must be even byte aligned. The hardware sees only bits 23 through 1; bit 0 is dropped because it is always 0.

After the system control determines that memory is being addressed (virtual address bits 23 through 22 equal 00), the memory control receives the lower 21 virtual address bits through the logical address bus. The upper ten bits (bits 21 through 12) address the map logic to select a page. The maps output a 9-bit logical mapped address, LMA 20 through 12, and, with the lower 11 bits of the virtual address (bits 11 through-1), forms the complete physical memory address.

Each user can address the maps using the full 4M byte of virtual memory address space. When a user loads a process into the computer, the supervisor sets up the map registers for that process, assigning the process an unused place in memory. As users input more and more information, the supervisor sends information back to the disc, remembering where (disc, track, and sector) it has sent the information and to where it belongs.

During each memory access, the map logic updates a table, called the page map table, to indicate the result of the access. The table records the status for each page, as follows:

- Not present (no memory available at that address).
- Present but not accessed (memory available, but it has not been accessed yet).
- Accessed but not written to (memory available that has been read, but not written).
- Written (memory available that has been written to and must be sent back to the disc before being overwritten).

Memory Access Control

The memory access control, triggered by the bus control, outputs timing and control signals to the rest of the memory control. This element includes a delay timer (also used in CPU/register accesses) and address decoders and multiplexers.

Main Memory

Main memory is sectioned off into pages 4096 bytes long. The lower ten bits of the logical address (bit 0 is dropped) select the word on the page. The main processor (and each memory expansion board) contains 128 pages, or 512K bytes. The page address is the 9-bit latched map address, from the map logic. The upper two bits of the latched map address select the board to be accessed; the lower seven select the page on the board.

Parity Circuit

During memory writes, the parity circuit generates parity on the write data, and the memory access control writes the parity into the parity RAM when it writes the data into the memory RAM. During memory reads, the parity circuit checks the parity of the data and generates a parity error signal if it is incorrect. If the operating system has not masked out the error, the error generates a nonmaskable CPU interrupt.

Refresh Control

The refresh control contains the refresh request and refresh memory address generators. The control refreshes a row of memory every 13 microseconds; therefore refreshing all of memory (including expansion) every 1.65 milliseconds (for RAMs that refresh 256 rows) or 3.3 milliseconds (for RAMs that refresh 128 rows).

The memory error control responds to invalid memory accesses (user attempts to write to a write-protected or operating system location) or errors during an access (parity or nonexistent memory address) by sending a bus error signal to the CPU or generating a nonmaskable interrupt request to the interrupt control. (Nonmaskable interrupts occur without bus errors, and bus errors occur without nonmaskable interrupts.)

INPUT/OUTPUT DEVICES

The input/output devices include disc control, fast and slow communications ports, and lineprinter interface.

Disc Control

The disc control contains three elements:

- Disc DMA controller
- Disc Bus interface unit
- Fixed disc and floppy disc contollers

Figure 4-2 shows a block diagram of the disc control in connection with the CPU, the bus arbiter, and memory control.

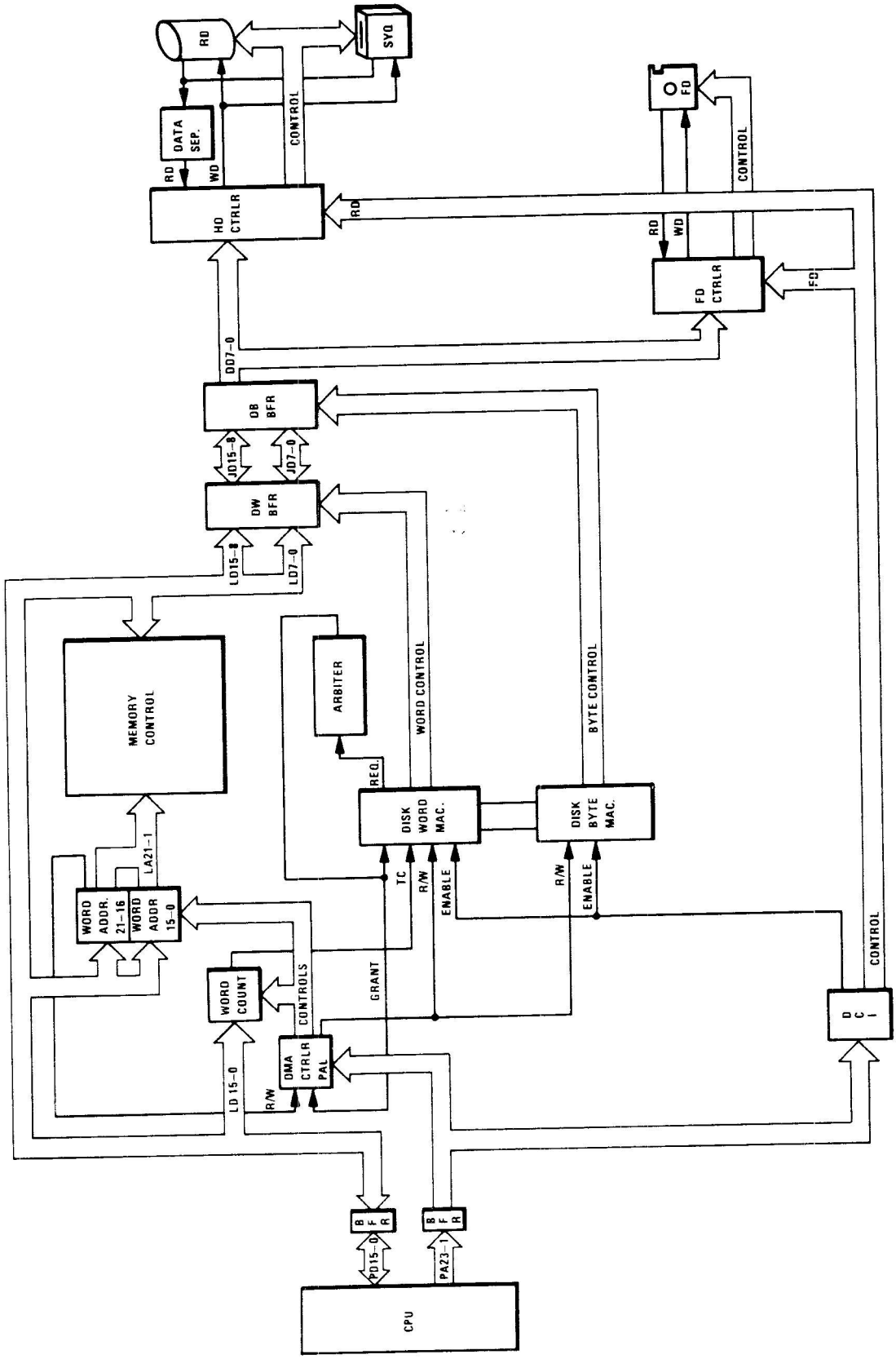

Figure 4-2. Disc Control Functional Block Diagram

DISC DMA CONTROLLER

The disc DMA controller stores and updates the memory address and word count during each disc DMA transfer and tells the disc bus interface unit when the DMA operation is finished. The controller consists of the wisc DMA control programmable array logic (PAL), the disc DMA word count and word address registers, and disc terminal count flip/flop.

The DMA control PAL controls CPU accesses to the word count and word address registers and updates the registers after each disc/memory transfer. After the disc control transfers the last word to or from memory, the word count register generates a terminal count signal setting the terminal count flip/flop. The flip/flop alerts the interface unit to the end of operation status.

DISC BUS INTERFACE UNIT

The disc bus interface unit is the interface between the disc controllers and the CPU and memory control. It has four primary functions:

- To provide an input/output data path between the controllers' I/O registers and the CPU.
- To provide a DMA data path between the controllers' data registers and memory.
- To service DMA requests by the controllers during DMA operations.
- To mask out pending interrupts from a disabled controller.

The disc bus interface unit includes the following:

- Disc control register
- Disc controller interface PAL
- Disc word/byte control

Refer to the System 6300 Technical Manual for details on the disc bus interface unit.

DISC CONTROLLERS

The disc controllers control the interface to the disc drives, including drive and command select, addressing, serial input/output, timing, and other drive related functions. The controllers also generate CPU interrupts and interface to the disc bus interface unit for byte transfers. There is a fixed disc controller and a floppy disc controller.

Only one major difference exists between the disc controllers (concerning the local system): the fixed disc controller is a bus master device and the floppy disc controller is a bus slave device.

Fixed Disc Controller

After the disc bus interface unit enables the fixed disc controller for a disc read/write operation, the controller sends data requests to the interface unit shortly before it either sends a byte of data (DMA disc read) or latches the disc data bus contents (DMA disc read). Without waiting for an acknowledge, after roughly 400 nanoseconds the controller either assumes the interface unit has latched the read byte or itself latches the write byte.

In both cases, the fixed disc controller removes the data request without prompting. The disc bus interface unit is therefore, in effect, the bus slave and the fixed disc controller the bus master. If the disc bus interface unit is not ready for the transfer when the fixed disc controller requests it, an overflow or underrun error occurs.

Floppy Disc Controller

After the disc bus interface unit enables the floppy disc controller for a disc read/write operation, the controller does nothing in the local system until it receives a chip-select from the interface unit. Then, when it is ready to read/write data, the controller returns a data request. The disc bus interface unit then returns a read enable or write enable, that causes the floppy disc controller to output the read byte (DMA disc read) or open its input latches (DMA disc write).

The disc bus interface unit removes the enable, then removes the chip select. The negated enable causes the floppy disc controller to either disable its disc data bus drivers or latch the write data.

In both cases the floppy disc controller waits for a prompt from the disc bus interface unit, returns an acknowledge (data request), prepares to read/write the data, then does the read/write when the disc bus interface unit tells it to. The disc bus interface unit is therefore, in effect, the bus master and the floppy disc controller the bus slave.

Fast Communications RS-422 Port

The fast communications port operates as a secondary station transceiver, because other devices interfacing to the RS-422 bus (for example, another computer) can act as bus masters. The fast communications port therefore acts as either a bus master or bus slave, depending on whether it is sending or receiving information.

Whenever a device performs a transmission, that device begins the transfer by sending a secondary station address that identifies the intended receiver. The receiver must already be receiver enabled to decode the address, determine that the information is intended for it, and to receive the information.

The port contains the following:

- Fast communications DMA controller
- Fast communications bus interface unit
- RS-422 port controller

FAST COMMUNICATIONS DMA CONTROLLER

The fast communications DMA controller, identical to the disc DMA controller, stores and updates the memory address and word count during each disc DMA transfer and tells the fast communications bus interface unit when the DMA operation is finished.

The controller consists of the fast communications DMA control PAL, the fast communications DMA word count and word address registers, and the fast communications terminal count flip/flop. The DMA control PAL controls CPU accesses to the word count and word address registers and updates the registers after each disc/memory transfer.

When the bus interface unit has transferred the last word to or from memory, the word count register generates a terminal count signal, setting the terminal count flip/flop. The flip/flop alerts the interface unit to the end of operation status.

FAST COMMUNICATIONS BUS INTERFACE UNIT

The fast communications bus interface unit is the control and data interface between the disc controllers and both the CPU and memory control. It has three primary functions:

- To provide an input/output data path between the RS-422 port controller and the CPU.
- To provide a DMA data path between the RS-422 port controller and memory.
- To service DMA requests by the RS-422 port controller during DMA operations.

The fast communications bus interface unit contains the following:

- Fast communications control register
- Word/byte control

Refer to the System 6300 Technical Manual for details on the fast communications bus interface unit.

RS-422 PORT CONTROLLER

The RS-422 multi-protocol communications controller interfaces with the fast communications bus interface unit as a slave device, the same way that the floppy disc controller interfaces to the disc bus interface unit. After it alerts the bus interface unit that it is ready to do a transfer, the controller is passive and waits for the unit to assert and negate the read/write control signals.

Slow Communications Port

The slow communications port controls the RS-232-C serial data ports A and B. The main control, including serializing incoming and outgoing data, comes from the 8274 multi-protocol serial controller. (A 7201 chip can substitute for the 8274.) Other elements include the programmable baud rate generator, external interface, and miscellaneous registers.

Unlike the fast communications port, performing DMA, the slow communications port operates in the local system only as a CPU interrupt device. When the port is ready to transfer data to or from memory, or when it wishes to alert the CPU to some error, command or status conditon, it interrupts the CPU. The CPU vectors to an interrupt routine, where it reads registers in the port controller to determine the reason for the interrupt.

On the basis of the information it reads, the CPU responds to the error/command/status condition or acts as the intermediary for a data transfer between memory and the port controller (by performing CPU/memory and CPU/port controller data register accesses).

The CPU may receive information telling it to set up a slow communications input/output operation (to or from a peripheral); the CPU does several slow cycle writes to load the slow communications registers, then triggers the port by a final write, to commence the operation.

Slow communications address decode determines when the CPU is accessing a slow communications port register. (This circuitry also determines if the CPU is writing the interrupt controller, in the interrrupt control.) There are three sets of slow communications registers:

- Programmable baud rate generator
- Slow communications clock/external data
- 8274 (or 7201) internal registers

The CPU loads the baud rate generator with a divisor to obtain the baud rate transmit/receive clocks. The CPU can also choose to use external clocks by setting up the slow communications miscellaneous PAL to do so. This PAL also contains registers that output secondary transmit data. Refer to the 8274 (or 7201) manufacturers specification for a description of the port controller registers.

Lineprinter Interface

The lineprinter interface routes data to the printer. Like the slow communications port, the lineprinter interface interrupts the CPU when it is ready to transfer data. The CPU then does a memory read and printer write. The port has an output latch. The CPU also reads status from the lineprinter interface, through an input buffer that connects incoming information to the logical data bus.

INTERRUPT CONTROL

The multi-level interrupt MC68010 consists of seven priority levels of interrupts. An interrupt control field, input to the CPU, alerts the CPU to the interrupt condition and also defines the priority level of the interrupt. Interrupts of a higher level pre-empt interrupts of a lower level, even if the CPU is servicing a lower level interrupt at the time of the higher level interrupt. This prevents random interrupt nesting.

The CPU contains a programmable priority level, or interrupt mask, of its own and, with one exception, ignores interrupts of a lower or equal level. The exception is when a device sends a level seven interrupt: in this case the CPU responds even if the CPU itself is set at level seven. The level seven interrupt is therefore a nonmaskable interupt. The operating system changes the CPU's priority level frequently, by executing a single instruction.

The CPU responds to interrupts by executing an interrupt acknowledge cycle, where it outputs the priority level it is acknowledging on the address bus and indicates the interrupt acknowledge, through the function code.

The interrupt control has the three following principle elements:

- Interrupt controller A (ICA on schematics)
- Interrupt control encoder
- Interrupt acknowledge programmable array logic (PAL)

Interrupt Controller

The interrupt controller, controlling normal vector interrupts, receives interrupt requests from various System 6300 elements and generates a single interrupt request to the interrupt control encoder. Before sending the interrupt request, the interrupt controller compares the active inputs with its own interrupt mask, loaded by the operating system. This allows the operating system to block unwanted interrupts.

Interrupt Control PAL

The interrupt control PAL receives CPU interrupt requests from the interrupt controller, the memory error PAL, and the other System 6300 devices. The interrupt control PAL determines the highest priority device requesting an interrupt and sends a 3-bit interrupt control field to the CPU, with the value of the field indicating the priority level of the interrupt.

If the CPU does not mask out the interrupt, the CPU responds through an interrupt acknowledge cycle, where the CPU indicates the selected interrupt level through the address field. The interrupt acknowledge PAL decodes the CPU response.

Interrupt Acknowledge PAL

The interrupt acknowledge PAL decodes the interrupt acknowledge cycle address field to determine the device that the CPU is acknowledging, then alerts the device by sending it an interrupt acknowledge signal. There are two types of CPU interrupts: auto-vector and normal vector.

If it is a normal vector interrupt, the interrupting device supplies the CPU with a vector address and (normal vector) acknowledge. The CPU uses the address to determine the location of the interrupt routine for that device.

If it is an auto-vector interrupt, after the device requests an interrupt and receives an interrupt acknowledge, it returns only an (auto-vector) acknowledge. The CPU supplies its own vector address, based on the interrupt level of the device.

The interrupt controller is a normal vector device. When it receives an interrupt acknowledge from the interrupt acknowledge PAL, the interrupt controller prioritizes the interrupt requests that it has currently active and outputs the interrupt vector (previously loaded by the CPU) associated with its highest priority active input. The CPU vectors to the interrupt service routine so indicated.

The fast communications interrupts and (optional) expansion board interrupts are also normal vector. All other interrupts are auto-vector. When the CPU acknowledges an auto-vector interrupt, the interrupt control encoder returns the auto-vector acknowledge, and the CPU supplies its own interrupt vector.

During the interrupt routine the CPU should erase the condition causing the interrupt and, effectively, remove the interrupt. Upon completing the interrupt, the CPU resumes normal processing, unless a different unmasked interrupt is pending. In this case the CPU responds to that interrupt. As the interrupt controller receives more than one interrupt request input, it may continue to assert its CPU interrupt even after the CPU has already serviced it.

This section shows the assemblies that make up the System 6300 in an exploded view. Table 5-1 follows the illustration and lists the parts for the System 6300.

SYSTEM 6300 PARTS ILLUSTRATION

The System 6300, Figure 5-1, is shown in an exploded view. All the parts shown are numbered and listed with Four-Phase part numbers in Table 5-1.

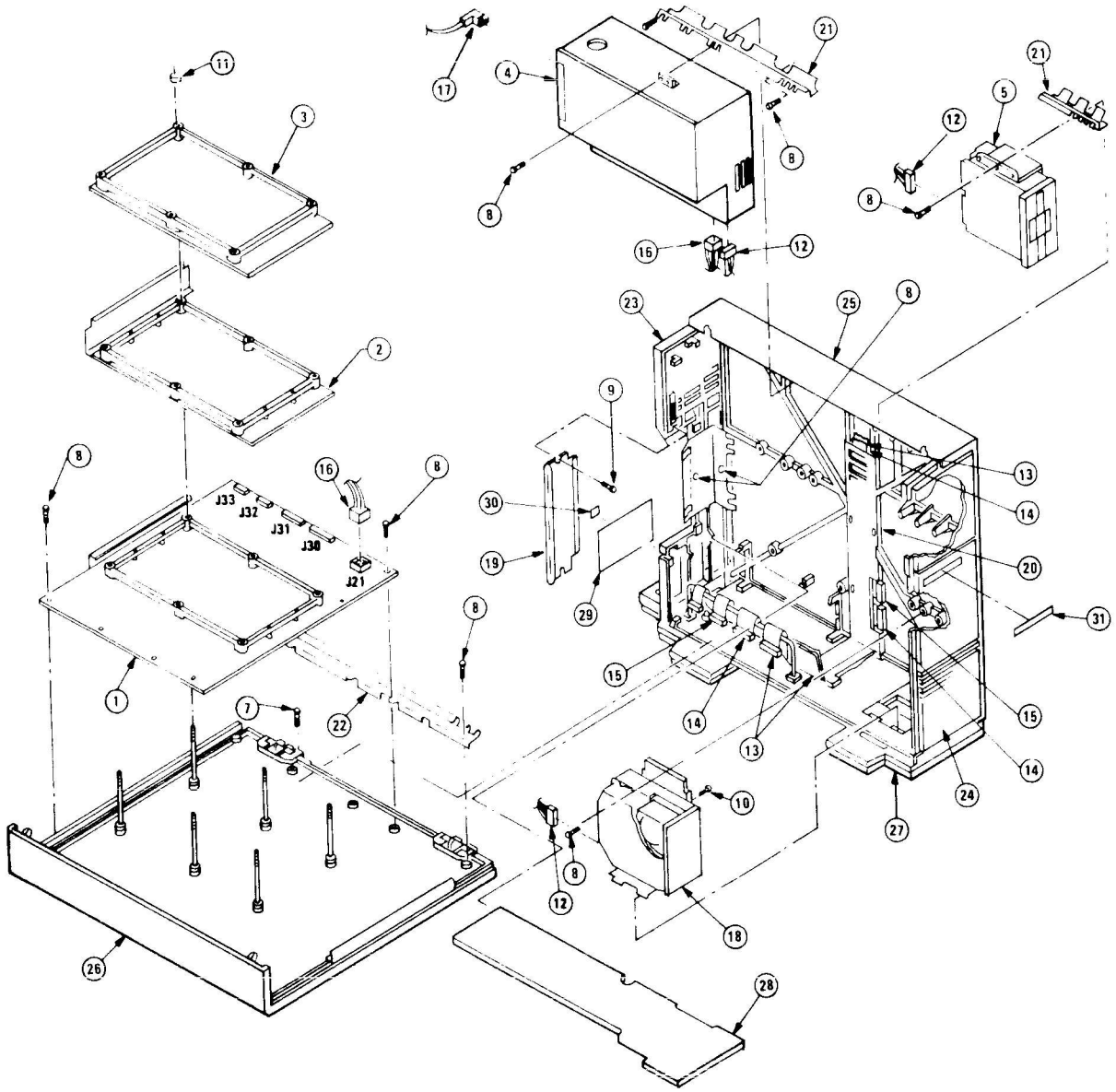

Figure 5-1. System 6300 Parts Illustration

PARTS LISTING

Table 5-1 lists the System 6300 parts with Four-Phase part numbers. The item number references the parts illustration drawing.

Table 5-1. System 6300 Parts Listing

Item Number	Part Description	Four-Phase Part Number
1	Main Processor PCA	76442011
2	Ethernet/Communications Expansion PCA	76442012
3	Memory Expansion PCA	76442013
4	Universal Power Supply Module	76442015
5	Floppy Disc Drive Module	76442000
6	Fixed Disc Drive Module-10M Byte	76442009
	Fixed Disc Drive Module-20M Byte	76442010
	Fixed Disc Drive Module-40M Byte	76442014
7	THD Forming 8 X 3/4 Screw	76442039
8	Selftap #10-16 X 3/8 Phillips Screw	76442038
9	Selftap #6-3/8 Phillips Screw	76442036
10	Sem #6-3 X 3/8 Phillips Pan Head Screw	76442037
11	Main Processor PCA Retaining Nut	76442040
12	Disc Drive DC Power Cable	76442023
13	Floppy Disc Control Cable	76442024
14	Fixed Disc Control Cable	76442025
15	Fixed Disc Data Cable	76442026
16	Power Supply/Main Processor PCA Power Cable	76442027
17	AC Power Cord	76442029
18	Fixed Disc Module Mounting Bracket	76442041
19	Blank Connector Panel	76442042
20	Cable Trough Cover	76442043
21	Fixed (Top) Side Contact Strip	76442044
22	Hinged (Bottom) Side Contact Strip	76442045
23	Rear Panel	76442030
24	Front Panel	76442031
25	Left Side Panel	76442032
26	Right Side Panel	76442033
27	Base Panel	76442034
28	Enclosure Cooling Shelf	76442046
29	Serial Label	
30	UL Listing Label	
31	Logo	

TM6000 parts listing and illustrations are located in the TM6000 Workstation Service Manual. However, Table 5-2 lists the TM6000 Workstation major assemblies for reference.

Table 5-2. TM6000 Workstation Part Numbers

Major Assembly	Four-Phase Part Number
TM30 Video Monitor Assembly	76441000
Base Logic Assembly	76441001
Keyboard Assembly	76441002
Power Supply Module	76441003
TM6000 Workstation 110V	76441004
TM6000 Workstation 220V	76441005
TM6000 Workstation Flat Power Supply Cable	76441009

USER'S COMMENTS

System 6300 Service Manual

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