FIELD MAINTENANCE PRINT SET

TABLE OF CONTENTS

UNIT VARIATIONS COVERED BY THIS PRINT SET
DZV11-A
DZV11-B
DZV11-C

DZV11

Field Maintenance Print Set

Digital Equipment Corporation

Print Set Part Number MP- Ø0462

REV A

NUMBER DZV11-Ø-1

CODE TC

SIZE B

REVISION HISTORY	REV.	ECO NUMBER	DATE
MR	A	DZV11-MKØØ1	12-81

DRN. G. DRAYTON	DATE 18 AUG 77	TITLE digital
CHK'D. S. ROBERTS	DATE 23 NOV 77	DZV11
DES. ENG. WILLIS R. SMITH	DATE 23 NOV 77	
RESP. ENG. WILLIS R. SMITH	DATE 14-Jan-82 23 NOV 77	
FIELD SERVICE HENRY S. YANG	DATE 23 NOV 77	
NEXT HIGHER DOC.		

DOCUMENT NUMBER

SIZE	CODE	NUMBER	REV.
B	TC	DZV11-Ø-1	A

SHEET 1 OF 1

DRB 124A

MK

DRAWING DIRECTORY

FOR FIELD MAINTENANCE PRINT SET REFER TO: B-TC-DZV11-Ø-1

UNIT VARIATIONS

VAR	TITLE
DZV11-A	ASYN MUX
DZV11-B	ASYN MUX (WITH TEST CONN. & CABLE)
DZV11-C	ASYN MUX (WITH TEST CONN. & DIST. CABLE)

REVISIONS		
REV.	CHANGE NO.	CHK
A	DZV11-MKØØ1	

USED ON OPTION/MODEL: DZV11

SHEET 1 OF 2

DRN. G. DRAYTON	DATE 21NOV77	TITLE: DZV11 DRAWING DIRECTORY
CHK'D. S. ROBERTS	DATE 21NOV77	digital
PROJ. ENG. W. R. SMITH	DATE 14-JAN-82 23NOV77	SIZE B / CODE DD / NUMBER DZV11-Ø / REV A
PROD. K. MERCADO	DATE 23NOV77	DIST.

DRB 106A

MK

3

FIND NO.	DRAWING NO.	DESCRIPTION	TYPE
1	MP00462	DZV11 FIELD MAINTENANCE PRINT SET (MP)	-
	B-TC-DZV11-0-1	DZV11 FIELD MAINTENANCE PRINT SET (TC)	-
	D-UA-DZV11-0-0	UNIT ASSEMBLY (DZV11)	E/M
	A-SP-DZV11-0-2	ENGINEERING SPEC.	-
	A-SP-DZV11-0-3	ACCEPTANCE PROCEDURE	-
	E-UA-BC11U-0-0	CABLE ASSY (BC11U)	E/M
	C-UA-H329-0-0	DZV11 TEST CONNECTOR	E/M
	K-PL-7018253-0-0	SHIPPING LIST DZV11	-
	D-AR-DZV11-0-4	DZV11-C INSTALLATION	E/M
2	B-DD-M7957-0	ASYN MUX	E/M
3	D-CS-H325-0-1	H325 TEST CONNECTOR	E/M
	K-CO-H325-0-4	X-Y COORDINATE HOLE LOCATION	-
	D-AH-H325-0-5	ASSY/DRILLING HOLE LAYOUT	-
	B-MH-H325-0-6	MODULE ECO HISTORY	-
4	A-SP-370029?-42-0	PACKAGING INSTRUCTIONS	-
5	A-SP-3700297-44-0	PACKAGING INSTRUCTIONS	-
6	D-AD-7018219-0-0	DZV11 DISTRIBUTION ASSY	E/M
	K-PL-7018219-0-0	DZV11 DISTRIBUTION ASSY	E/M
	D-IA-7018203-0-0	DZV11 DIST. CABLE ASSY	E/M
	C-MD-7423236-0-0	PANEL MTG DZV11	M

FIND NO.	DRAWING NO.	DESCRIPTION	TYPE

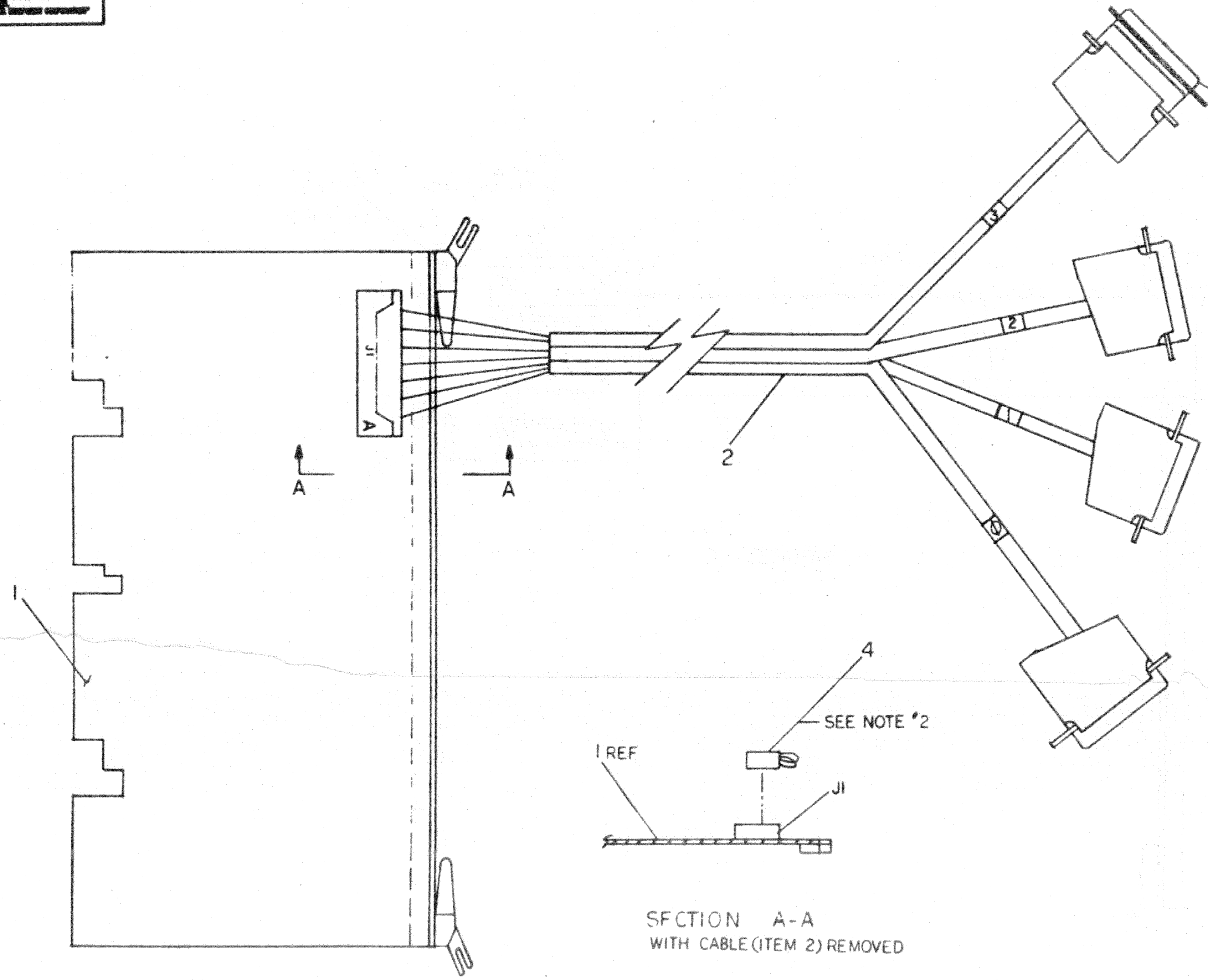
TYPE: E ELECTRICAL, M MECHANICAL, E/M ELECTRO/MECHANICAL

digital

TITLE	SHEET	SIZE	CODE	NUMBER	REV.
UNIT ASSY (DZV11)	2 OF 2	B	DD	DZV11-0	A

DRB 108A

MK



NOTE:

1. TEST CONNECTOR ITEM #3 TO BE INSERTED AS SHOWN INTO THE INDIVIDUAL CONNECTORS OF THE CABLE WITH THE MARKINGS Ø, 1, 2 & 3; FOR TESTING CABLE ASSEMBLY.
2. TEST CONNECTOR (ITEM #4) TO BE PLACED AS SHOWN INTO CONNECTOR (J1) FOR TESTING BOARD (ITEM #1)
3. SEMS SCREW (ITEM #9) USED TO MOUNT DISTRIBUTION PANEL.

CAUTION: OFF SHEET PARTS LIST EXISTS. REFER TO K-PL-DZV11-Ø-Ø.

DZV11-B	DZV11-A	DESCRIPTION	DWG./PART NO.	ITEM NO.
1	–	PACKAGING INSTRUCTIONS	A-SP-370C297-44-0	7
–	1	PACKAGING INSTRUCTIONS	A-SP-370C297-42-0	6
1	1	DZV11 SHIPPING LIST	A-PL-DZV11-Ø	5
1	–	DZV11 TEST CONNECTOR	C-UA-H329-Ø-Ø	4
1	–	H325 TEST CONNECTOR	D-CS-H325-Ø-1	3
1	–	CABLE ASSY BC11U	E-UA-BC11U-25-Ø	2
1	1	ASYN MUX	D-UA-M7957-Ø-Ø	1

QUANTITY & VARIATION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

THIRD ANGLE PROJECTION

REMOVE BURRS AND BREAK SHARP CORNERS

DO NOT SCALE DWG

MATERIAL: SEE PARTS LIST

FINISH: —

NEXT HIGHER ASSY.: B-DD-DZV11-Ø

SCALE: —

SHEET OF 2

FIRST USED ON: DZV11

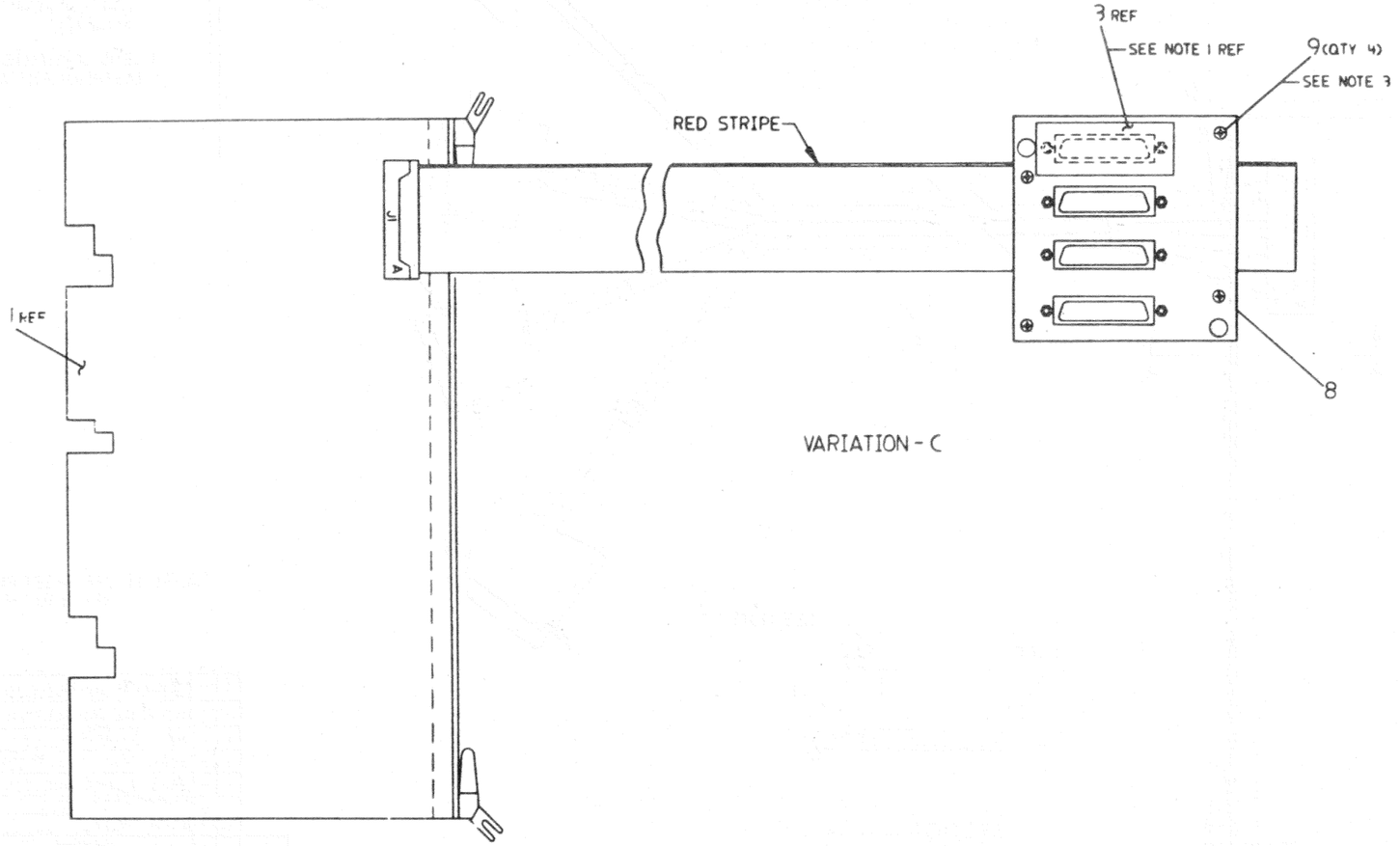
TITLE: UNIT ASSEMBLY (DZV11)

SIZE	CODE	NUMBER	REV.
D	UA	DZV11-Ø-Ø	A

REVISIONS: A — DZV11-MK301 — W. SMITH

MK

5



VARIATION - C

REVISION HISTORY		
DATE	ECO NUMBER	REV.

TITLE	UNIT ASSEMBLY (DZV11)
DOCUMENT NUMBER	D UA DZV11-Ø-Ø
REV	A
SCALE	NONE
SHEET	2 OF 2
MK	

D UA DZV11-Ø-Ø A

AUTOMATED BY PRTLST.3P(44) P A R T S L I S T SHEET A1 OF A1

LINE	ITEM	DOCUMENT NUMBER	PART NUMBER	DESCRIPTION	QUANTITY PER VARIATION A	B	C
1	1	B-TC-DZV11-0-1	MP00462-00	DZV11 CUSTOMER PRINT SET	1	1	1
2	2		ZJ251-RB	DZV11 DOC/PT KIT#	1	1	1
3	3		EKDZV11-UG	DZV-11 ASYNCHRONOUS MULTIPLEXER	1	1	1
4	4	SEE NOTE 1	EKDZV11-TM	DZV-11 ASYNCHRONOUS MULTIPLEXER	REF	REF	REF
5	5	SEE NOTE 1	ZJ251-PB	DZV11 PT ONLY KIT#	REF	REF	REF
6	6	SEE NOTE 1	ZJ251-FR	DZV11 DIAG MCRF ONLYU KIT#	REF	REF	REF

7 NOTE: 1. OPTIONAL SOFTWARE ITEMS 4,5&6 AVAILABLE UPON REQUEST.

REVISION HISTORY			BASIC PART NO: 7018253										
ENG	ECO NUMBER	REV	SECTION A OF A	DRN: G DRAYTON	DATE: 21-NOV-77		D	I	G	I	T	A	L
WS	DZV11-MK001	A	SECTION. VARIATION INDEX [A] A ,B ,C	CHK'D: S ROBERTS 9 JAN 82	DATE: 23-NOV-77	TITLE	PARTS LIST						
			[B]	DES.ENG.: W SMITH	DATE: 23-NOV-77		SHIPPING LIST, DZV11						
			[C]	RESP.ENG.: W SMITH D. Backes	DATE: 23-NOV-77	DOCUMENT NUMBER							
			[D]			SIZE	CODE	NUMBER				REV	
			[E]	MFG.ENG.: K MERCADO	14-JAN-82 DATE: 23-NOV-77	K	PL	7018253-0-0				A	
			[F]	ASSEMBLY NUMBER: D-UA-DZV11-0-0	TOP DOCUMENT NUMBER: #R-DD-DZV11-0			FILE NAME: MK0SSO.PLS				EDIT # 3	

MK

SIZE	CODE	NUMBER	REV.
B	DD	M7957-Ø	C

DRAWING NO.	NO. OF SHTS.	PART NO.	DESCRIPTION	REVISIONS
		M7957-ØØ	ASYN MUX MODULE	B
~~B-MH-M7957-Ø-0~~	~~1~~		~~MODULE ECO HISTORY~~	~~B~~
D-UA-M7957-Ø-Ø	1		ASYN MUX	B C
~~D-PL-M7957-Ø-Ø~~	~~4~~		~~ASYN MUX~~	~~B~~
D-CS-M7957-Ø-1	14		ASYN MUX	B C
D-MD-5012754-0-0	5		DRILL & ETCH DRAWING	B C
		5012754	ETCH BOARD	C D
M7957-Ø-L			P.C. DESIGN DATA BASE	REF D
~~M7957-Ø-PL~~			~~INSERTION P/L DATA BASE~~	~~REF~~
K-PL-M7957-Ø-Ø	2		ASYN MUX (DBP)	C
D-EC-5Ø12754-Ø-Ø	2		ETCH CUT DRAWING	- C

NOTES:

REVISIONS		
DATE	CHG NO.	REV.
8-81	MKØØ1	C

digital

USED ON OPTION/MODEL	
DZV11	

DRN.	RITA BUREAU	4-1-77
CHK'D		8/10/77
ENG.		8/10/77
PROD.		8/10/77

TITLE: ASYN MUX

SIZE	CODE	NUMBER	REV.
B	DD	M7957-Ø	C

SHEET 1 OF 1

DRB 128

9

MV

AUTOMATED BY PRTLST.3P(44) — P A R T S L I S T — SHEET A1 OF A2

LINE	ITEM	DOCUMENT NUMBER	PART NUMBER	DESCRIPTION	QTY PER VARIATION 00	REFERENCE DESIGNATOR
1	1	D-MD-5012754-0-0	5012754-00	M7957	1	
2	2		1010279-00	.47 MFD 25V 20% CER	6	C29-C34
3	3		1000009-00	33.0 MMF 100V 5%200PPM MICA	1	C1
4	4		1000012-00	56.0 MMF 100V 5%200PPM MICA	1	C2
5	5		1000016-00	100.0 MMF 100V 5%200PPM MICA	2	C3,C4
6	6		1000021-00	220.0 MMF 100V 5%200PPM MICA	1	C5
7	7		1000022-00	270.0 MMF 100V 5%200PPM MICA	1	C7
8	8		1000024-00	470.0 MMF 100V 5%200PPM MICA	12	C9-C20
9	9		1000026-00	680.0 MMF 100V 5%200PPM MICA	3	C6,C27,C28
10	10		1001610-01	.01 MFD50/100V +80-20% DISC	48	C35-C82
11	11		1005306-00	6.8MFD 35V 10% S.TANT	6	C21-C26
12	12		1100114-00	D 664 QS\75PCB PIV= 25V SP	6	D4-D9
13	13		1109990-00	1N 757A VZ= 9.1 5% .40W P	1	D3
14	14		1110836-00	1N 759A VZ= 12.0 5% .40W	2	D1,D2
15	15		1209941-02	HEADER 100 40POS RT ANGLE	1	J1
16	16		1211164-04	SW,DIP 1P 1A 8POS	1	E2
17	17		1211164-06	SW,DIP 1P 1A 10POS	1	E30
18	18		1300229-00	100.0 .25 W 5.0 % CC	2	R1,R2
19	19		1300243-00	120.0 .50 W 5.0 % CC	1	R28
20	20		1300295-00	330.0 .25 W 5.0 % CC	7	R4-R10
21	21		1300365-00	1.0 K .25 W 5.0 % CC	8	R14-R19,R3,R29
22	22		1300391-00	1.50 K .25 W 5.0 % CC	1	R27
23	23		1301401-00	750.0 .25 W 5.0 % CC	1	R13
24	24		1301424-00	680.0 .25 W 5.0 % CC	2	R11,R12
25	25		1301874-00	5.60 K .25 W 5.0 % CC	6	R21-R26
26	26		1309413-00	3.83 K .25 W 1.0 % RN55D-F10	1	R20
27	27		1609428-00	DELAY= 50NS,0TAPS D0150	2	E79,E76
28	28		1811660-02	OSCILLATOR, XTAL 5.0688 MHZ	1	E78
29	29		1909705-00	DEC 8881 NAND GATE-QUAD 2IN O	1	E40
30	30		1910322-00	DEC 1488L DRIVER,LINE,QUAD,EI	3	E57,E73,E80

REVISION HISTORY			BASIC PART NO: M7957
ENG	ECO NUMBER	REV	SECTION A OF A
RH	M7957-MK001	C	SECTION.VARIATION INDEX [A] 00 [B] [C] [D] [E] [F] [H] [J] [K] [L] [M] [N]

DRN: RITA BUREAU	DATE: 06-APR-77	DBP D I G I T A L
CHK'D: K.GLEEZEN	DATE: 10-AUG-77	TITLE PARTS LIST ASYN MUX
DES.ENG: W SMITH	DATE: 10-AUG-77	
RESP.ENG.: R.HARRINGTON	DATE: 26-OCT-81	DOCUMENT NUMBER
MFG.ENG.: B.WOODARD	DATE: 26-OCT-81	SIZE: K / CODE: PL / NUMBER: M7957-0-0 / REV: C
ASSEMBLY NUMBER: D-UA-M7957-0-0	TOP DOCUMENT NUMBER: $B-DD-M7957-0	FILE NAME: MK0522.PLS / EDIT #: 3

MK

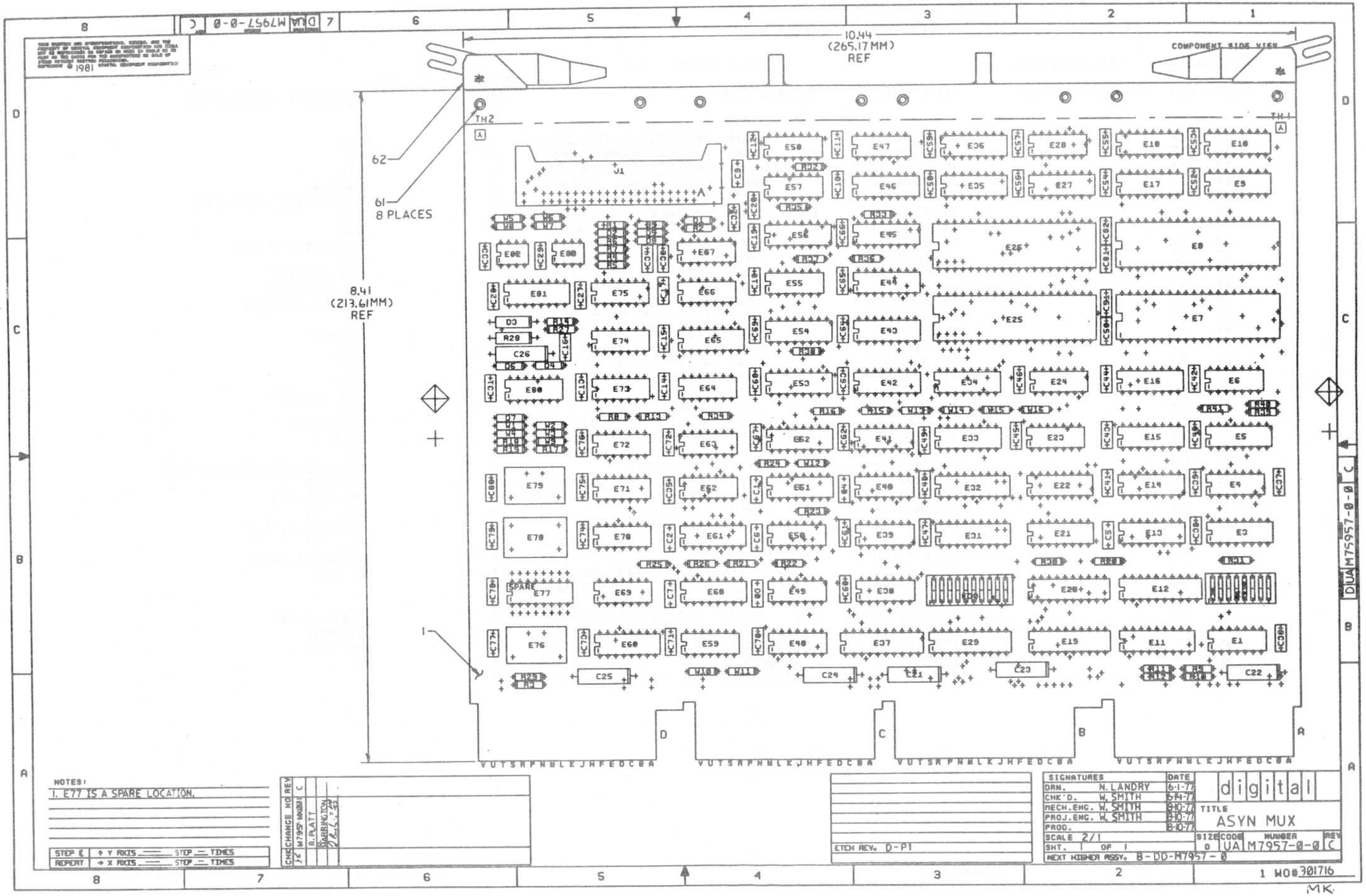
AUTOMATED BY PRTLST.3P(44)

P A R T S L I S T

LINE	ITEM	DOCUMENT NUMBER	PART NUMBER	DESCRIPTION	QTY PER VARIATION 00	REFERENCE DESIGNATOR
31	31		1910534-00	74S04 INVERTER GATE-HEX 1I	1	E75
32	32		1911469-00	DEC 8640 RECEIVER,BUS,QUAD,U	1	E1
33	33		1911911-00	DEC 74S124 OSCILLATOR,DUAL VOLT	1	E81
34	34		1912098-00	0026 DRIVER,MOS CLOCK,2	2	E82,E83
35	35		1912646-00	LS253 MUX 1 OF 4 (DUAL)	8	E13,E14,E21,E42-E46
36	36		1912729-00	DC 004 PROTOCOL,REG. SELECT	1	E12
37	37		1912730-00	DC 003 INTERRUPT,2 CIRCUIT	1	E11
38	38		1913040-00	DC 005 TRANSCEIVER 4BIT	4	E19,E20,E29,E37
39	39		1912799-00	LS00 NAND-GATE-QUAD 2IN,P	1	E23
40	40		1912801-00	LS02 NOR-GATE-QUAD 2IN	3	E38,E39,E69
41	41		1912803-00	74LS04 INVERTER GATE,HEX	3	E47,E48,E72
42	42		1912805-00	LS08 AND GATE-QUAD 2IN,PO	4	E4,E24,E55,E71
43	43		1912808-00	LS11 AND GATE-TRIPLE 3IN	1	E64
44	44		1912811-00	LS21 AND GATE-DUAL 4IN,PO	2	E28,E41
45	45		1912813-00	LS27 NOR GATE-TRIPLE 3IN	1	E49
46	46		1912816-00	LS32 OR GATE-QUAD 2IN,POS	1	E59
47	47		1912817-00	LS37 NAND GATE-QUAD 2IN,P	1	E63
48	48		1912824-00	LS74 FF-D DUAL,EDGE TRIGG	3	E50,E62,E70
49	49		1912830-00	LS90 COUNTER,ASYNCH UP,DE	1	E66
50	50		1912845-00	LS153 MUX 1 OF 4 (DUAL)	3	E3,E9,E10
51	51		1912846-00	LS155 DECODER,2 OF 4(DUAL)	2	E5,E16
52	52		1912847-00	LS157 MUX 1 OF 2(QUAD)	1	E56
53	53		1912853-00	LS175 FF-D QUAD	6	E15,E22,E52,E53,E54,E65
54	54		1912854-00	LS193 COUNTER,SYNCHR,4BIT,	2	E36,E68
55	55		1912858-00	LS221 ONE SHOT-DUAL,SCHMIT	3	E51,E60,E61
56	56		1912860-00	LS259 LATCH 8BIT	2	E33,E34
57	57		2111188-00	3341 64X4 FIFO MEMORY	4	E17,E18,E27,E35
58	58		2112623-00	DUAL BAUD RATE GEN/PROG DIVIDER,	2	E31,E32
59	59		2113937-00	UART 125K BUAD	4	E7,E8,E25,E26
60	60		9009185-00	JUMPER, WIRE, INSULATED, BLACK B	16	W1-W16
61	61		9000024-01	EYELET,ROLL FLANGE .1210DX .192	8	
62	62		1213113-01	HANDLE,MODULE,	1	
63	63		1913130-00	DEC 1489A RECEIVER,LINE,QUAD,	3	E58,E67,E74
64	64		1300316-00	470.0 .25 W 5.0 % CC	2	R30,R31
65	65		1300479-00	10.0 K .25 W 5.0 % CC	10	R32-R41
66	66		1300005-03	R NETWORK 13-10K 5.0 % 14PIN	1	E6
67	67		9107256-11	TUBING,THIN WALL: .027ID UL	A/R	

D	I	G	I	T	A	L	TITLE	SECTION A OF A
							ASYN MUX	

SIZE	CODE	DOCUMENT NUMBER	REV
K	PL	M7957-0-0	C



NOTES:
1. E77 IS A SPARE LOCATION.

STEP	↑ Y AXIS ____ STEP ____ TIMES
REPEAT	→ X AXIS ____ STEP ____ TIMES

CHG	CHANGE NO	REV
1X	M7957 MODS	C
	R. PLATT	
	ROBBINGTON	
	22-Jul-77	

ETCH REV. 0-P1

SIGNATURES		DATE
DRN.	N. LANDRY	6-1-77
CHK'D.	W. SMITH	6-14-77
MECH. ENG.	W. SMITH	8-10-77
PROJ. ENG.	W. SMITH	8-10-77
PROD.		8-10-77

SCALE 2/1
SHT. 1 OF 1
NEXT HIGHER ASSY. 8-DD-M7957-0

digital

TITLE: ASYN MUX

SIZE	CODE	NUMBER	REV
D	UA	M7957-0-0	C

1 WO# 301716

MK

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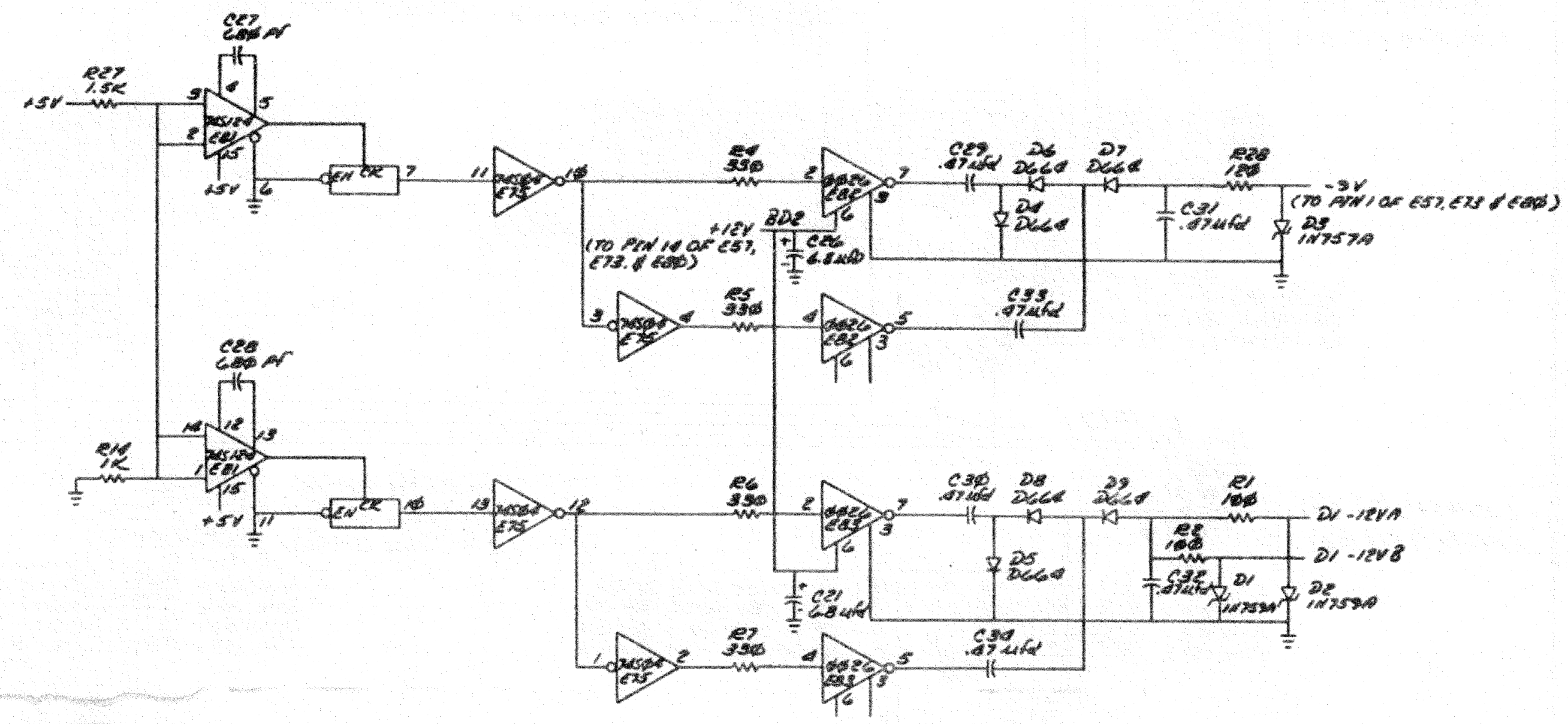
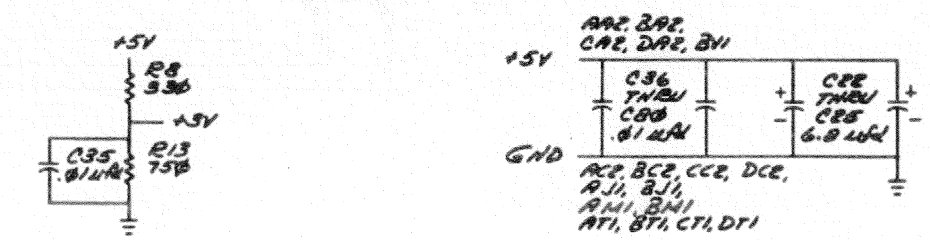
BERG PINNING CHART

A	GROUND
B	EIA XMIT DATA Ø0
C	EIA RECEIVED DATA Ø0
D	EIA DATA TERM RDY Ø0
E	EIA RING Ø0
F	EIA FORCED BUSY Ø0
H	EIA REQ TO SEND Ø0
J	
K	GROUND
L	EIA CARRIER Ø0
M	GROUND
N	EIA XMIT DATA Ø1
P	EIA RECEIVED DATA Ø1
R	EIA DATA TERM RDY Ø1
S	EIA RING Ø1
T	EIA FORCED BUSY Ø1
U	EIA REQ TO SEND Ø1
V	
W	GROUND
X	EIA CARRIER Ø1
Y	EIA CARRIER Ø2
Z	GROUND
AA	
BB	EIA REQ TO SEND Ø2
CC	EIA FORCED BUSY Ø2
DD	EIA RING Ø2
EE	EIA DATA TERM RDY Ø2
FF	EIA RECEIVED DATA Ø2
HH	EIA XMIT DATA Ø2
JJ	GROUND
KK	EIA CARRIER Ø3
LL	GROUND
MM	
NN	EIA REQ TO SEND Ø3
PP	EIA FORCED BUSY Ø3
RR	EIA RING Ø3
SS	EIA DATA TERM RDY Ø3
TT	EIA RECEIVED DATA Ø3
UU	EIA XMIT DATA Ø3
VV	GROUND



CLOCK ADDRESS				BAUD RATE	PERIOD (USEC)
D	C	B	A		
Ø	Ø	Ø	Ø	5Ø	125Ø.ØØ
Ø	Ø	Ø	1	75	833.33
Ø	Ø	1	Ø	11Ø	568.18
Ø	Ø	1	1	134.5	464.68
Ø	1	Ø	Ø	15Ø	416.67
Ø	1	Ø	1	3ØØ	2Ø8.33
Ø	1	1	Ø	6ØØ	1Ø4.17
Ø	1	1	1	12ØØ	52.Ø8
1	Ø	Ø	Ø	18ØØ	34.72
1	Ø	Ø	1	2ØØØ	31.25
1	Ø	1	Ø	24ØØ	26.ØØ
1	Ø	1	1	36ØØ	17.36
1	1	Ø	Ø	48ØØ	13.Ø2
1	1	Ø	1	72ØØ	8.68
1	1	1	Ø	96ØØ	6.51
1	1	1	1	INVALID	



REVISIONS: CHANGE NO. M7957-MKP01 — REV. C — R. HARRINGTON

(CHARTS)

FIRST USED ON	DZV11
TITLE	ASYN MUX (DI)
NEXT HIGHER ASSY.	D-UA-M7957-Ø-Ø
SIZE	D
CODE	CS
NUMBER	M7957-Ø-1
REV.	C
SHEET	1 OF 14

digital

NOTE:
DEVICE ADDRESS IS DETERMINED BY SWITCH PACK E30. SWITCH CLOSED (ON) FOR A BUS LOGICAL ONE (LOW).

(ADDRESS BIT 07)
(ADDRESS BIT 06)
(ADDRESS BIT 05)
E30 E30-6 E30-7 E30-8

(ADDRESS BIT 12)
(ADDRESS BIT 11)
E30 E30-1 E30-2

(ADDRESS BIT 04)
(ADDRESS BIT 03)
E30 E30-9 E30-10

(ADDRESS BIT 00)
(ADDRESS BIT 09)
(ADDRESS BIT 08)
E30 E30-3 E30-4 E30-5

M1502 E47 — D2 ODD PARITY L
M1502 E47 — D2 PARITY ENABLE L

DC005 E19
BDAL 00 L — AV2 — BUS 0 DAT 0 — D2 DEVICE DATA BUS 00
BDAL 07 L — AL2 — BUS 1 DAT 1 — D2 DEVICE DATA BUS 07
BDAL 06 L — BK2 — BUS 2 DAT 2 — D2 DEVICE DATA BUS 06
BDAL 05 L — BJ2 — BUS 3 DAT 3 — D2 DEVICE DATA BUS 05
JA 1, JA 2, JA 3 MATCH
BBS7 L — MEM B
D5 VECTOR BIT 07 N — JAV 1
D5 VECTOR BIT 06 N — JAV 2
D5 VECTOR BIT 05 N — JAV 3
XMIT REC

DC005 E37
BDAL 15 L — BV2 — BUS 0 DAT 0 — D2 DEVICE DATA BUS 15
BDAL 14 L — BU2 — BUS 1 DAT 1 — D2 DEVICE DATA BUS 14
BDAL 12 L — BS2 — BUS 2 DAT 2 — D2 DEVICE DATA BUS 12
BDAL 11 L — BR2 — BUS 3 DAT 3 — D2 DEVICE DATA BUS 11
+5V — JA 1, JA 2, JA 3 MATCH — D2 DEVICE SELECT H
MEM B
JAV 1, JAV 2, JAV 3
XMIT REC

D4 READ L
D4 READ DEVICE H

DC005 E22
BDAL 01 L — AV2 — BUS 0 DAT 0 — D2 DEVICE DATA BUS 01
BDAL 04 L — BN2 — BUS 1 DAT 1 — D2 DEVICE DATA BUS 04
BDAL 03 L — BF2 — BUS 2 DAT 2 — D2 DEVICE DATA BUS 03
BDAL 02 L — BE2 — BUS 3 DAT 3 — D2 DEVICE DATA BUS 02
JA 1, JA 2, JA 3 MATCH
+5V
MEM B
JAV 1, JAV 2, JAV 3
D5 VECTOR BIT 04 N
D5 VECTOR BIT 03 N
D5 VECTOR BIT 02 N
XMIT REC

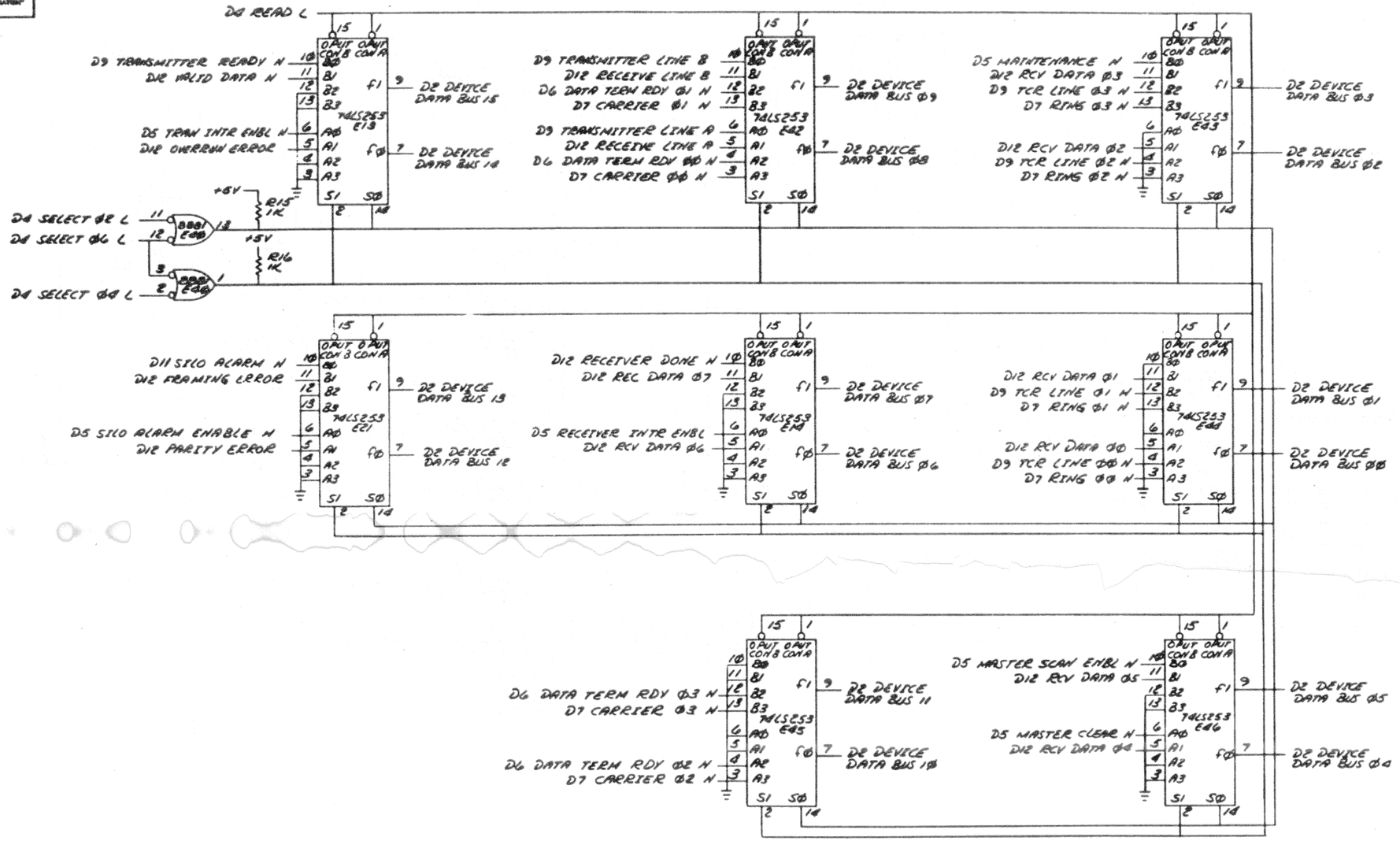
DC005 E29
BDAL 13 L — BT2 — BUS 0 DAT 0 — D2 DEVICE DATA BUS 13
BDAL 10 L — BP2 — BUS 1 DAT 1 — D2 DEVICE DATA BUS 10
BDAL 09 L — BM2 — BUS 2 DAT 2 — D2 DEVICE DATA BUS 09
BDAL 08 L — BH2 — BUS 3 DAT 3 — D2 DEVICE DATA BUS 08
JA 1, JA 2, JA 3 MATCH
MEM B
JAV 1, JAV 2, JAV 3
D5 VECTOR BIT 08 N
XMIT REC

(TRANSCEIVERS)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
ASYN MUX (D2)	D	CS	M7957-0-1	C
SCALE —	SHEET 2 OF 14	DIST.		

AJK



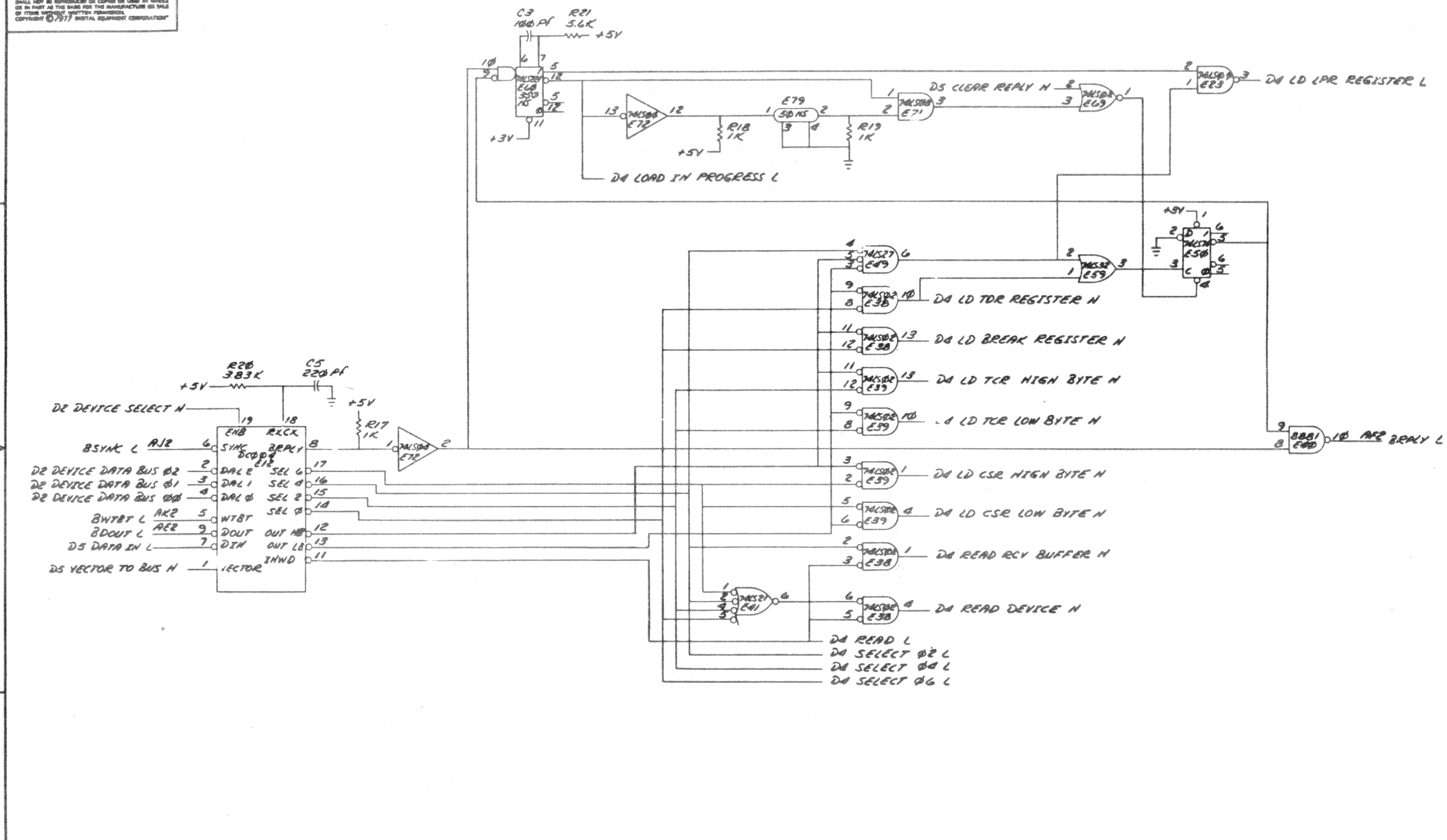
(OUTPUT DATA MULTIPLEXERS)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
ASYN MUX (D3)	D	CS	M7957 - Ø - 1	C
SCALE —	SHEET 3 OF 14	DIST.		

DCS M7957-Ø-1

15



(ADDRESS SELECT & DECODE)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
ASYN MUX (D4)	D	CS	M7957-0-1	C
SCALE — SHEET 4 OF 14	DIST.			

MK

NOTE:
VECTOR ADDRESS IS DETERMINED BY SWITCH PACK E2. SWITCH CLOSED (ON) FOR QBUS LOGICAL ONE (LOW).

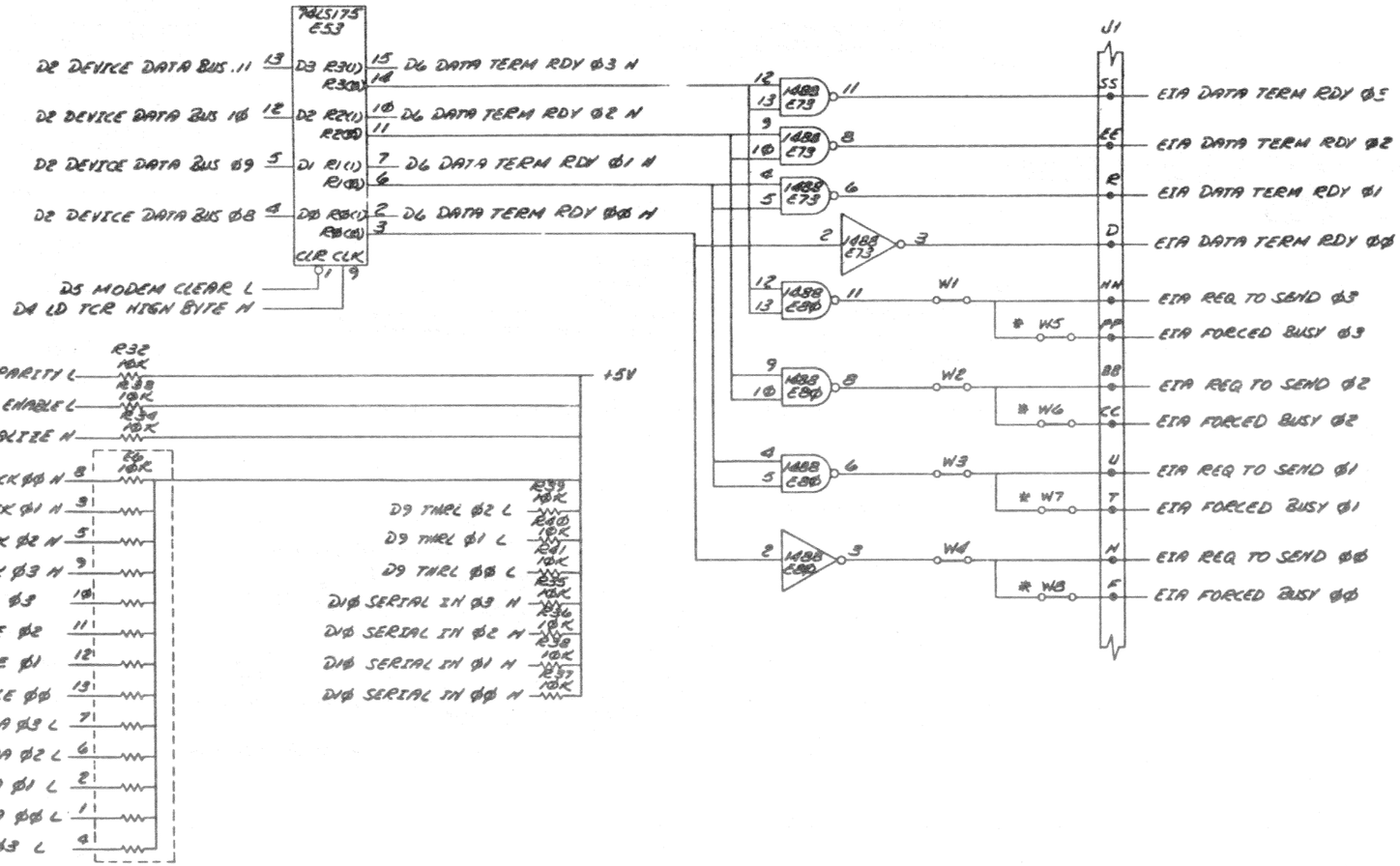
+5V
BIAK I L
D12 RECEIVER DONE N
D11 SILO ALARM N
BDIN L
D5 DATA IN L
D9 TRANSMITTER READY N
D6 DEVICE DATA BUS Ø6
D7 DEVICE DATA BUS Ø7
D4 LD CSR LOW BYTE N
D4 LD CSR HIGH BYTE N
+5V
BIAK O L
D5 RECEIVER INTR ENBL
AL2 BIRQ L
+5V
D5 VECTOR TO BUS N
D5 VECTOR BIT Ø8 N
D5 VECTOR BIT Ø7 N
D5 VECTOR BIT Ø6 N
D5 VECTOR BIT Ø5 N
D5 VECTOR BIT Ø4 N
D5 VECTOR BIT Ø3 N
D5 VECTOR BIT Ø2 N
+3V
D2 DEVICE DATA BUS 12
D4 LD CSR HIGH BYTE N
D5 SILO ALARM ENABLE N
D5 SILO ALARM ENABLE L
D2 DEVICE DATA BUS Ø5
D2 DEVICE DATA BUS Ø4
D2 DEVICE DATA BUS Ø3
D4 LD CSR LOW BYTE N
D3 R3(1)
R3(0)
D2 R2(1)
R2(0)
D1 R1(1)
R1(0)
D0 R0(1)
R0(0)
CLR CLK
D0 MASTER SCAN ENBL N
D5 MASTER SCAN ENBL L
D5 MAINTENANCE N
AR2
AS2
CR2
W10
CS2
JUMPER INSTALLED ONLY IN M9270 BACKPLANE.
CM2
W11
CM2
JUMPER INSTALLED ONLY IN M9270 BACKPLANE.
C6 680pf
R22 5.6K
+5V
D5 MASTER CLEAR N
D5 INITIALIZE N
D5 INITIALIZE L
+3V
BINIT L
D5 MODEM CLEAR L
D5 CLEAR REPLY N

(CSR, INTR, INITIALIZE)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE: ASYN MUX (D5)
SIZE: D | CODE: CS | NUMBER: M7957-Ø-1 | REV: C
SCALE | SHEET 5 OF 14 | DIST.

NOTE:
* FOR M38E AND M38 MODEMS WITH THE FORCED BUSY OPTION, THIS JUMPER MUST BE INSTALLED TO ALLOW REQUEST TO SEND TO CONTROL FORCED BUSY.
(CH = BUSY) IF OPTION IS NOT INSTALLED, REMOVE THIS JUMPER.

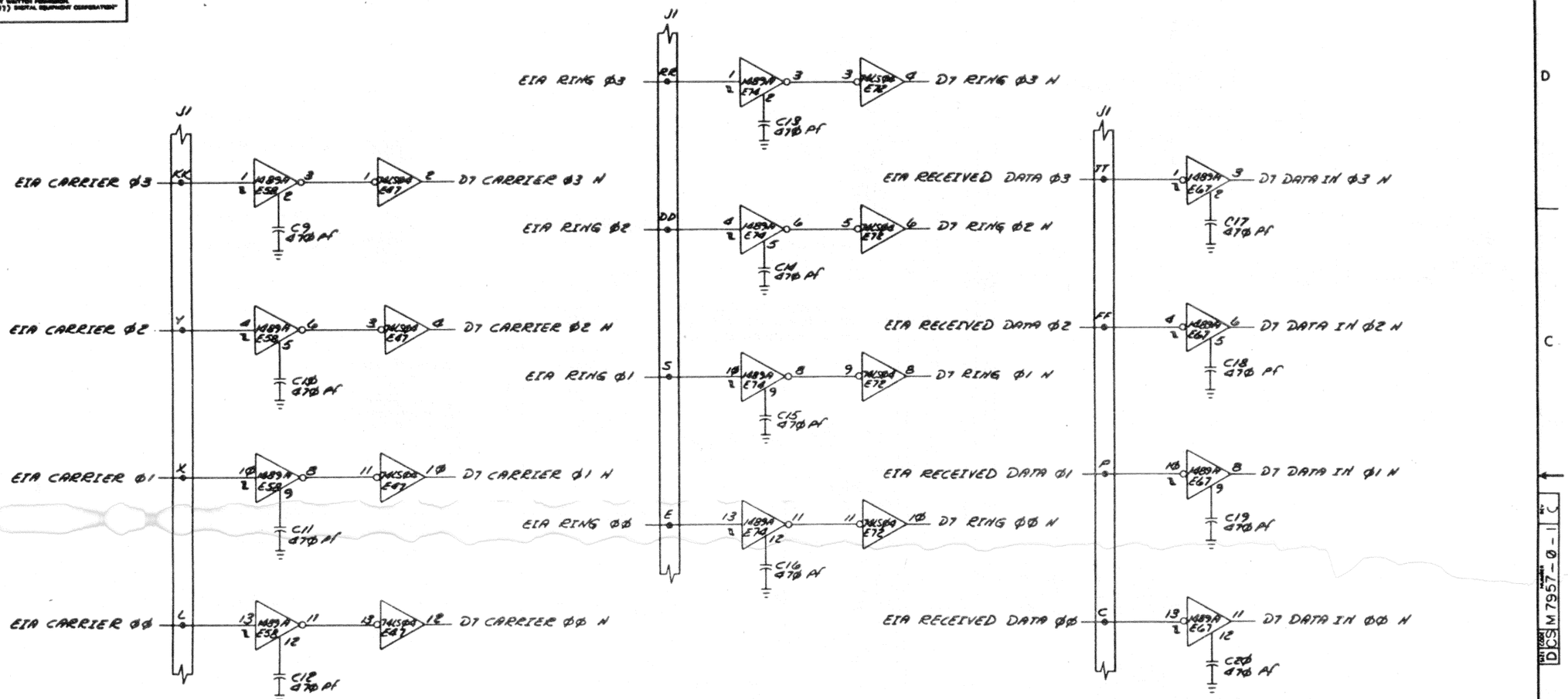


(EIA Driver & Receivers)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
ASYN MUX (D6)	D	CS	M7957-0-1	C
SCALE 1=1	SHEET 6 OF 14	DIST.		

81

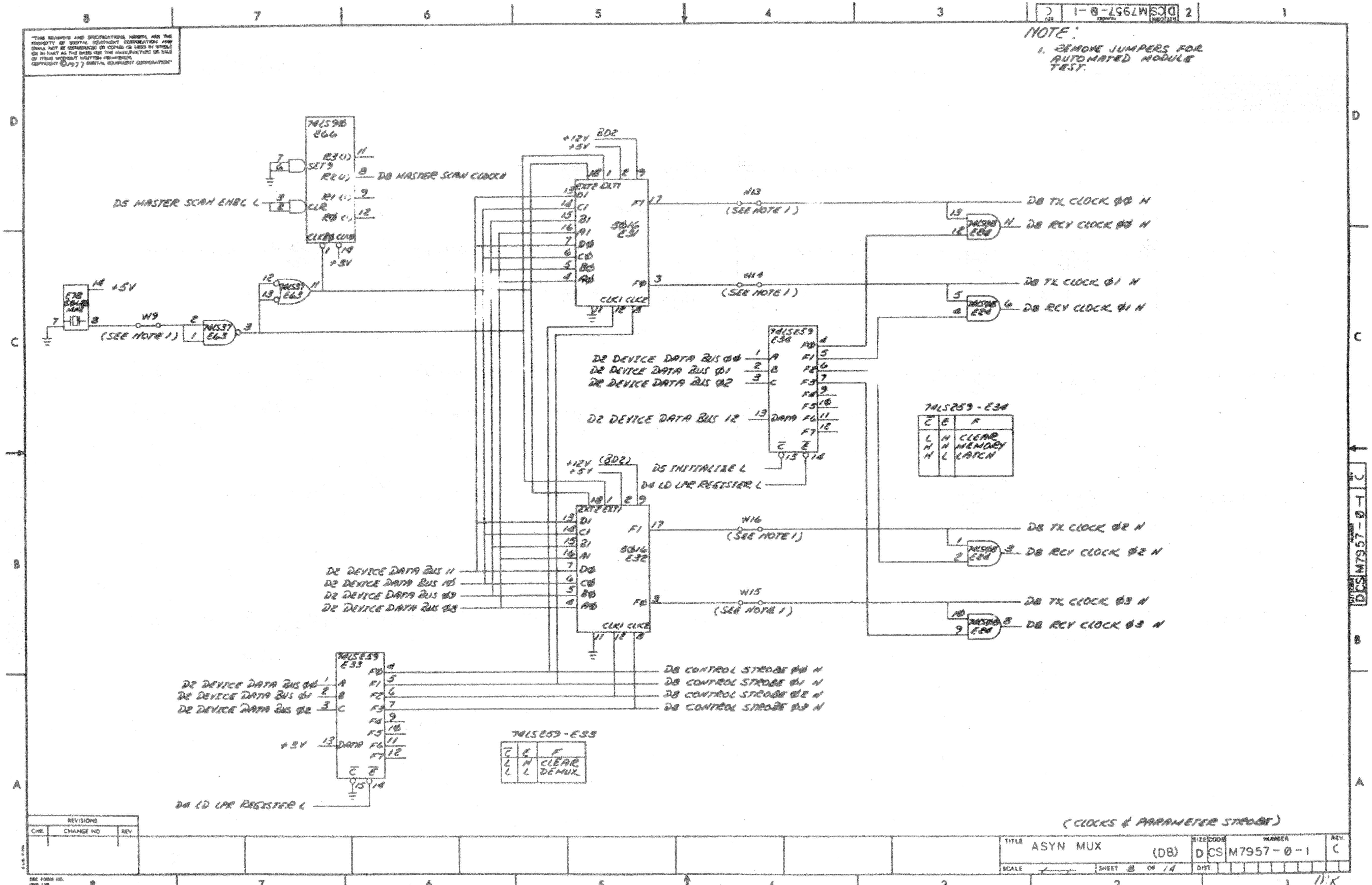


(EIA RECEIVERS)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
ASYN MUX (D7)	D	DCS	M7957 - Ø - 1	C
SCALE —	SHEET 7 OF 18	DIST		

MK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NOTE:
1. REMOVE JUMPERS FOR AUTOMATED MODULE TEST.
74LS90 E66
D8 MASTER SCAN CLOCK H
D5 MASTER SCAN ENBL L
E78 5.068 MHZ
+5V
W9
(SEE NOTE 1)
74LS37 E63
+12V
+5V
BD2
5016 E31
W13
(SEE NOTE 1)
W14
(SEE NOTE 1)
D8 TX CLOCK Ø0 H
D8 RCV CLOCK Ø0 H
D8 TX CLOCK Ø1 H
D8 RCV CLOCK Ø1 H
74LS08 E24
74LS259 E34
D2 DEVICE DATA BUS Ø0
D2 DEVICE DATA BUS Ø1
D2 DEVICE DATA BUS Ø2
D2 DEVICE DATA BUS 12
74LS259 - E34
C̄ Ē F
L H CLEAR
H H MEMORY
H L LATCH
D5 INITIALIZE L
D4 LD LPR REGISTER L
5016 E32
W16
(SEE NOTE 1)
W15
(SEE NOTE 1)
D8 TX CLOCK Ø2 H
D8 RCV CLOCK Ø2 H
D8 TX CLOCK Ø3 H
D8 RCV CLOCK Ø3 H
D2 DEVICE DATA BUS 11
D2 DEVICE DATA BUS 10
D2 DEVICE DATA BUS Ø9
D2 DEVICE DATA BUS Ø8
74LS259 E33
D8 CONTROL STROBE Ø0 H
D8 CONTROL STROBE Ø1 H
D8 CONTROL STROBE Ø2 H
D8 CONTROL STROBE Ø3 H
74LS259 - E33
C̄ Ē F
L H CLEAR
L L DEMUX
+5V
D4 LD LPR REGISTER L
(CLOCKS & PARAMETER STROBE)
TITLE ASYN MUX (D8)
SIZE D CODE CS NUMBER M7957-Ø-1 REV. C
SHEET 8 OF 14
REVISIONS CHK CHANGE NO REV

NOTE:
1. REMOVE JUMPER FOR AUTOMATED MODULE TEST.

D9 TRANSMITTER LINE B
D9 TRANSMITTER LINE A
D9 TRANSMITTER READY N

D13 TBMT Ø0
D13 TBMT Ø1
D14 TBMT Ø2
D14 TBMT Ø3

D8 DEVICE DATA BUS Ø0
D8 DEVICE DATA BUS Ø1
D8 DEVICE DATA BUS Ø2
D8 DEVICE DATA BUS Ø3

D5 INITIALIZE L
D4 LD TCR LOW BYTE N

D5 MASTER SCAN ENBL N

D9 TCR LINE Ø0 N
D9 TCR LINE Ø1 N
D9 TCR LINE Ø2 N
D9 TCR LINE Ø3 N

D4 LOAD IN PROGRESS L

D4 LD TDR REGISTER N

D9 TMRL Ø3 L
D9 TMRL Ø2 L
D9 TMRL Ø1 L
D9 TMRL Ø0 L

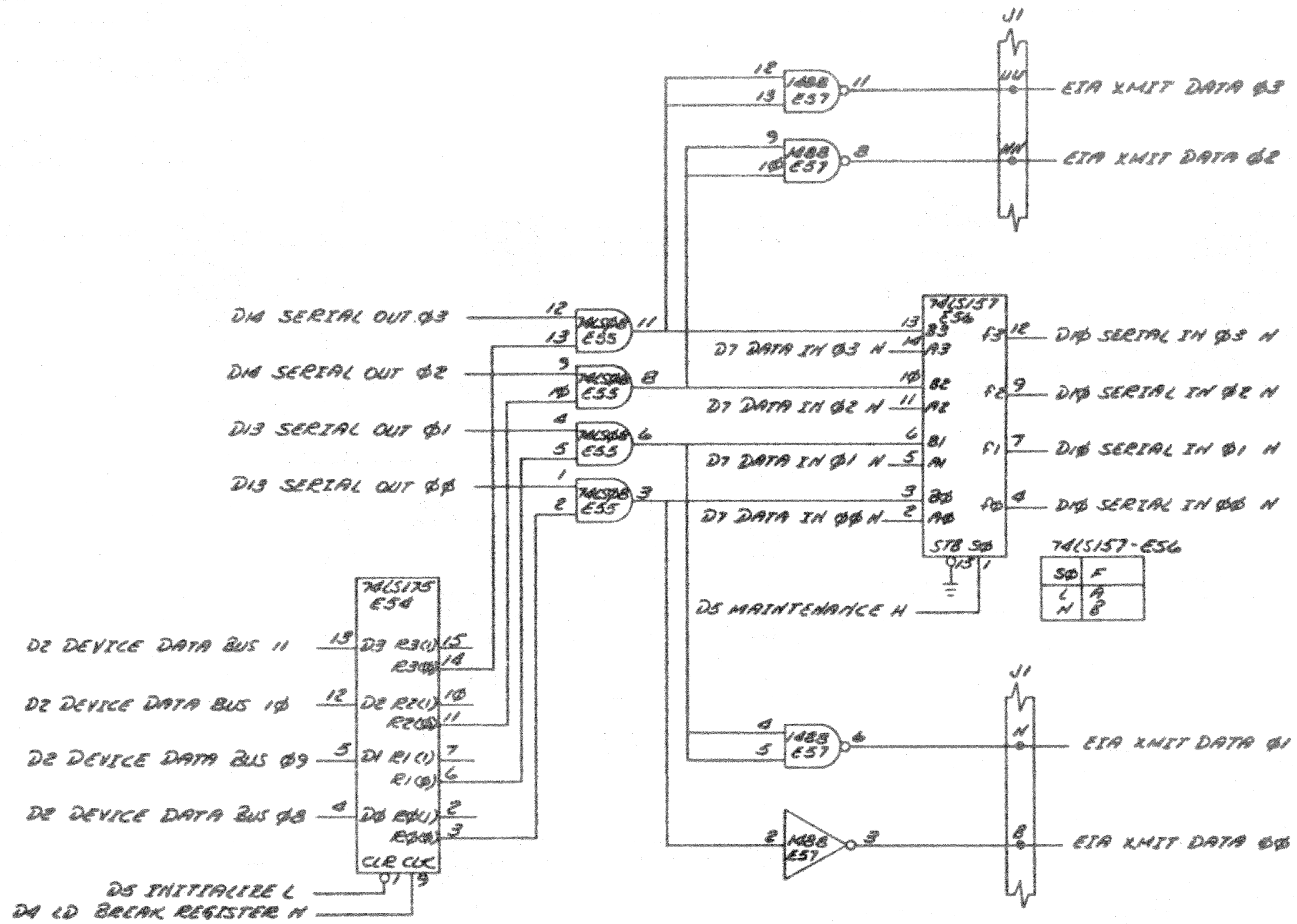
(SEE NOTE 1)

(TRANSMITTER CONTROL)

REVISIONS		
CHK	CHANGE NO	REV

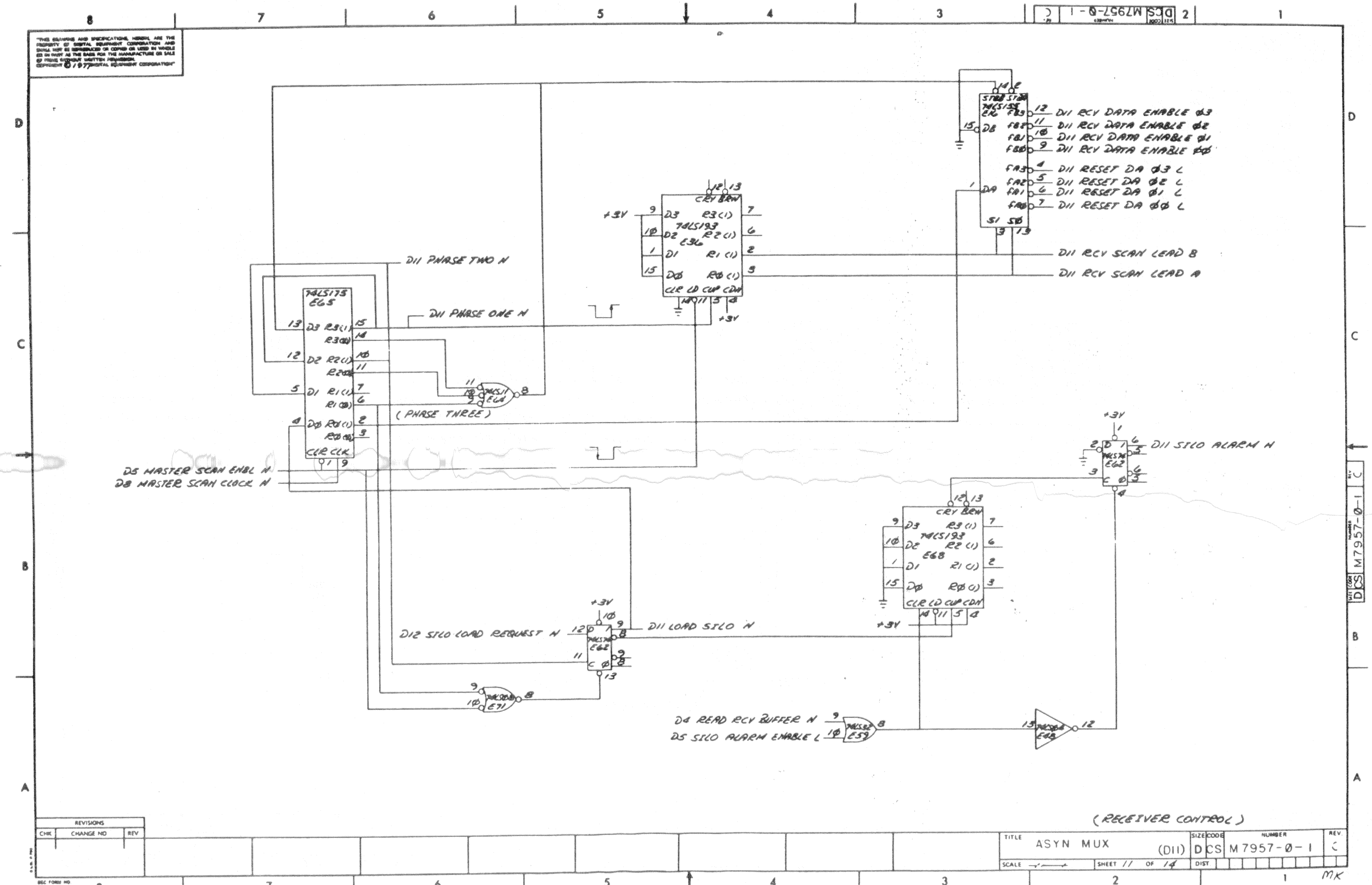
TITLE		SIZE	CODE	NUMBER	REV.
ASYN MUX	(D9)	D	CS	M7957-0-1	C
SCALE	SHEET 9 OF 14	DIST.			

21



(BREAK, TRANSMIT DATA, MAINTENANCE)

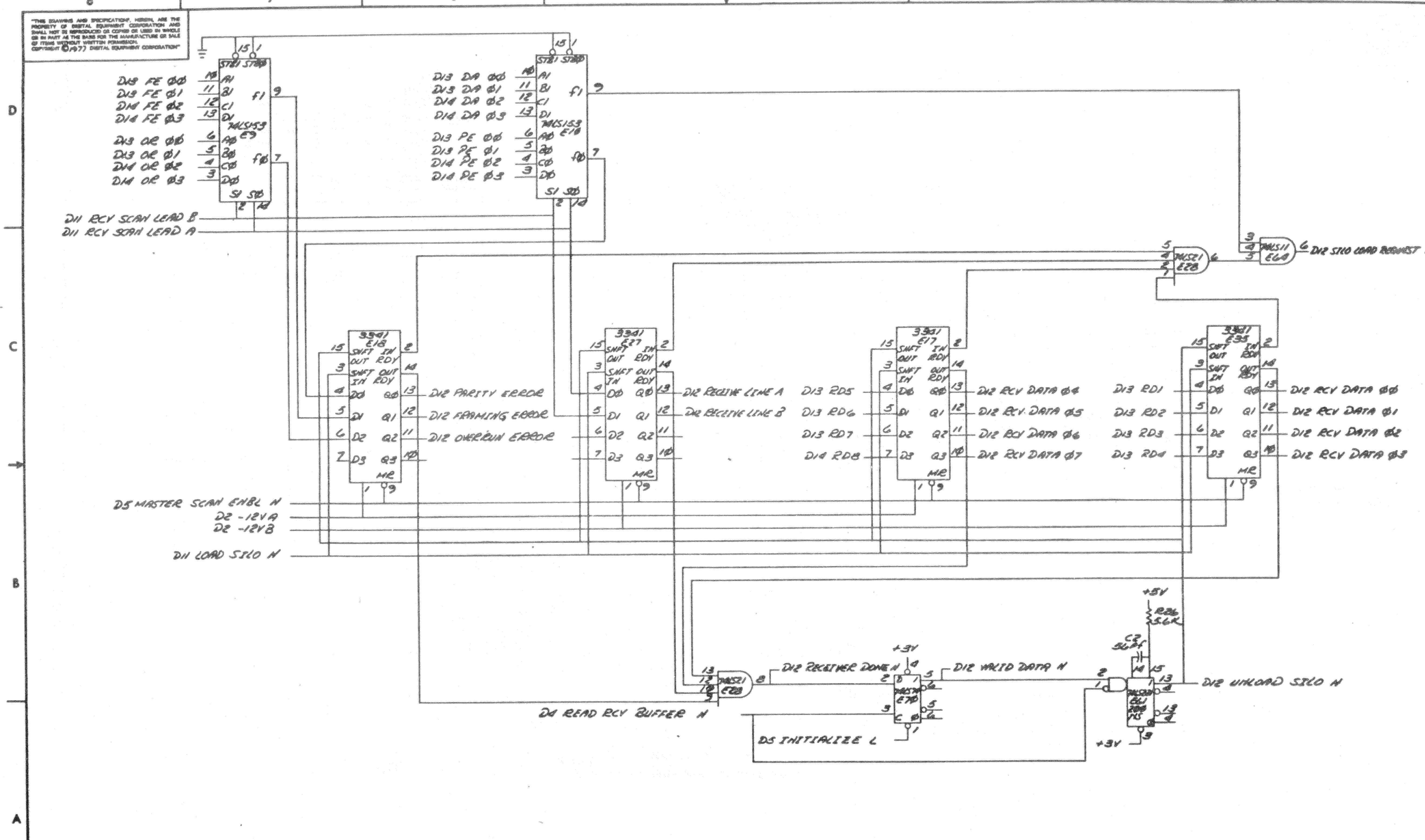
TITLE ASYN MUX (DIØ)	SIZE D	CODE CS	NUMBER M7957-Ø-1	REV. C
SCALE	SHEET 10 OF 14			



(RECEIVER CONTROL)

TITLE	SIZE	CODE	NUMBER	REV.
ASYN MUX (D11)	D	CS	M7957-Ø-1	C

SCALE — SHEET 11 OF 14



(SILO BUFFERS AND UNLOAD CONTROL)

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TITLE	ASYN MUX (DI2)	SIZE D	CODE CS	NUMBER M7957-Ø-1	REV. C
SCALE		SHEET 12 OF 16	DIST.		

D CS M7957-Ø-1 C

MK

UART Ø0 E26

DI0 SERIAL IN Ø0 N — 20 SERIAL IN
DI1 RESET DA Ø0 L — 18 CLR R DONE
DI1 RCV DATA ENABLE Ø0 — 4 STB RD
16 STB STATUS
DB RCV CLOCK Ø0 N — 17 R CLK
DB TK CLOCK Ø0 N — 9Ø X CLK
D9 TMRL Ø0 L — 23 LD XD
33 XD7
32 XD6
31 XD5
3Ø XD4
29 XD3
28 XD2
27 XD1
26 XD0

R DONE — 19 — DI3 DA Ø0
OR ERR — 15 — DI3 OR Ø0
FR ERR — 14 — DI3 FE Ø0
P ERR — 13 — DI3 PE Ø0
RD7 — 5 — DI3 RD8
RD6 — 6 — DI3 RD7
RD5 — 7 — DI3 RD6
RD4 — 8 — DI3 RD5
RD3 — 9 — DI3 RD4
RD2 — 1Ø — DI3 RD3
RD1 — 11 — DI3 RD2
RD0 — 12 — DI3 RD1
XRDY — 22 — DI3 TBMT Ø0
SERIAL OUT — 25 — DI3 SERIAL OUT Ø0
EOC — 24

21 36 37 38 35 39 34

DI3 DA Ø1
DI3 OR Ø1
DI3 FE Ø1
DI3 PE Ø1
DI3 RD8
DI3 RD7
DI3 RD6
DI3 RD5
DI3 RD4
DI3 RD3
DI3 RD2
DI3 RD1

UART Ø1 E25

DI0 SERIAL IN Ø1 N — 20 SERIAL IN
DI1 RESET DA Ø1 L — 18 CLR R DONE
DI1 RCV DATA ENABLE Ø1 — 4 STB RD
16 STB STATUS
DB RCV CLOCK Ø1 N — 17 R CLK
DB TK CLOCK Ø1 N — 9Ø X CLK
D9 TMRL Ø1 L — 23 LD XD
33 XD7
32 XD6
31 XD5
3Ø XD4
29 XD3
28 XD2
27 XD1
26 XD0

R DONE — 19
OR ERR — 15
FR ERR — 14
P ERR — 13
RD7 — 5
RD6 — 6
RD5 — 7
RD4 — 8
RD3 — 9
RD2 — 1Ø
RD1 — 11
RD0 — 12
XRDY — 22 — DI3 TBMT Ø1
SERIAL OUT — 25 — DI3 SERIAL OUT Ø1
EOC — 24

CLR EOB MRE MRI MP ØP LDC
21 36 37 38 35 39 34

D8 DEVICE DATA BUS Ø7
D8 DEVICE DATA BUS Ø6
D8 DEVICE DATA BUS Ø5
D8 DEVICE DATA BUS Ø4
D8 DEVICE DATA BUS Ø3
D8 DEVICE DATA BUS Ø2
D8 DEVICE DATA BUS Ø1
D8 DEVICE DATA BUS Ø0

D5 INITIALIZE N

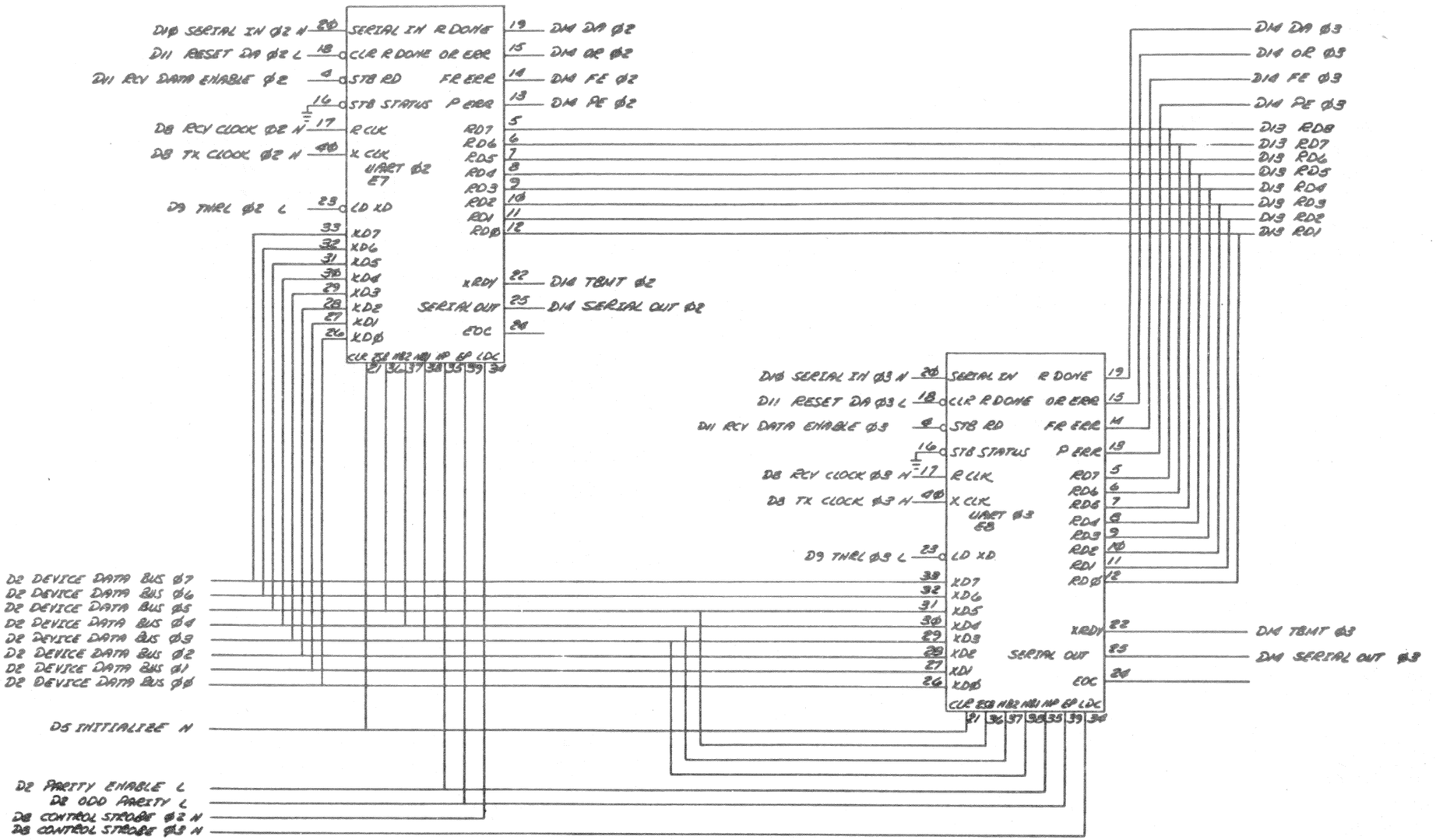
D8 PARITY ENABLE L
D8 ODD PARITY L
D8 CONTROL STROBE Ø0 N
D8 CONTROL STROBE Ø1 N

(UARTS Ø0 & Ø1)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	ASYN MUX (DI3)	SIZE	CODE	NUMBER / REV.
SCALE	SHEET 13 OF 14	D	CS	M7957-Ø-1 / C
		DIST.		

MK



(UARTS Ø2 & Ø3)

REVISIONS

CHK	CHANGE NO.	REV.

TITLE	ASYN MUX (D14)	
SIZE/CODE	NUMBER	REV.
	DCSM7957-0-1	C
SCALE	SHEET 14 OF 14	DIST.

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

ENGINEERING SPECIFICATION DATE 4/25/77

TITLE DZV11 ASYNCHRONOUS MULTIPLEXOR

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE

ENG	APPD	SIZE	CODE	NUMBER	REV
Willis Smith		A	SP	DZV11-0-2	

SHEET 1 OF 18

TABLE OF CONTENTS

1.0 General Description

The DZV11 is a multiplexor interface between four asynchronous serial data communications channels and the LSI-11 bus. The DZV11 provides an EIA level interface and enough data-set control to permit dial up (auto answer) operation with modems capable of full duplex operation such as the Bell models 103, 113, 212 or equivalent. The DZV11 does not support half duplex operations or the secondary transmit and receive operations available with some modems such as the Bell model 202. Program compatibility is maintained with the Unibus option, DZ11-A. The only compatibility exception being the number of serial channels supported. The DZV11 has applications in data concentration and collection systems in front-end systems interfacing to a host computer, and for use in a cluster controller for terminal applications.

The following is a summary of the programmable features offered for each line:

Character length:	5,6,7 or 8 level code
Number of stop bits:	1 or 2 for 6,7,8 level code 1 or 1.5 for 5 level code
Parity generation and detection:	Odd, even or none
Operating speed:	50, 75, 110, 134.5, 150, 300 600, 1200, 1800, 2000, 2400, 3600, 4800, 7200 and 9600.
Breaks:	Generation and detection

1.1 Available Options:

The DZV11 can be supplied in two different configurations, each designated by a suffix letter (A or B). Each multiplexor configuration utilizes a quad height module designated as the M7957. All input and output leads of the M7957 conform to EIA Standard RS232C and are available on a Berg header.

The required hardware for the DZV11-A option is just the M7957 module. Cabling assemblies to terminals and modem channels are not supplied with this option, but are available in the DZV11-B configuration. Each DZV11-B configuration consists of an M7957 module, BC11U-25 cable assembly, and two accessory test connectors, H329 and H325.

2.0 Performance Specifications

2.1 Bus Loading:

The DZV11 represents one unit load to the LSI-11 bus.

2.2 Power Consumption

1.15 Amps @ +5 Volts
0.39 Amps @ +12 Volts

2.3 Environmental:

The DZV11 operates in an environment from 5 to 50 degrees centigrade with a relative humidity of 10% or less to 95%.

2.4 Maximum Configurations:

The DZV11 multiplexor is assigned a device address in the floating address space. The floating address space starts at 760010 and extends to 764000. A maximum configuration of DZV11's would not be limited by floating address space, but would be limited by the rules governing an intermediate size system configuration. Therefore, a maximum of seven DZV11 multiplexors may reside in a nine by four backplane. Refer to Section 3.5 for throughput limitations.

2.5 Available Interrupts:

A. Receiver Done Interrupt - occurs every time a character appears at the output of the Receiver Buffer Register and the Silo Alarm is disabled. Can be enabled or disabled from the bus.

B. Silo Alarm Interrupt - occurs after sixteen entries have been made into the Receive Buffer Register by the scanner. This interrupt disables Receiver Done Interrupt and is rearmed when the Receive Buffer Register has been read.

C. Transmit Interrupt - occurs everytime the scanner finds a Uart buffer empty condition, and the Transmitter Control Register bit is set for that line. Can be enabled or disabled from the bus.

2.5 Receivers:

The receivers provide serial to parallel conversion of 5,6,7, 8 level code with one start space and at least one stop mark. The character length, number of stops bits,

parity generation and operating speed are programmable parameters for each line. A Receiver and Transmitter of a corresponding line share the same operating speed with provisions for enabling/disabling of that receive line.

Each receiver is double-buffered and has an allowable input distortion of 43.75% on any bit. Also, the accumulated character distortion must not exceed 43.75%. This limits the speed distortion to 4.8% for an eight bit character. Break detection is provided on each receiver.

2.7 Transmitters:

The transmitters provide parallel to serial conversion of 5,6,7,8 level code with or without parity. The parity sense when selected can be either odd or even. The stop code can be either 1 or 2 units except when 5 level code is selected. When 5 level code is selected, the stop code can be set to 1 or 1.5 units. The character length, number of stop units, parity generation and sense, and operating speed are programmable parameters for each line. The operating speed for the transmitter is common with the receiver. Breaks are capable of being transmitted on any line. The gross start-stop distortion for a transmitter's TTL output will be less then 2.5% for an eight bit character.

2.8 Baud Rate Generator:

The baud rate generator is a MOS/LSI device, which provides the DZV11 multiplexor with full programmable capability for operating speed selection. Each line has an independent generator capable of producing one of fifteen selectable baud rates. Speed tolerance for all rates is less 0.3% with a clock duty of 50% $\pm$ 5%.

3.0 Hardware Description

3.1 Receiver Control:

The receiver control section utilizes a forty pin MOS/LSI device for each line to provide serial to parallel assembly of received characters. These devices are designated as a Universal Asynchronous Receiver/Transmitters (UART). In addition to receive character assembly, the UART provides parity checking, break detection and overrun detection. The UART is double buffered, allowing a full character time to remove the received character to a hardware buffer. The UARTS are serviced by a four phase scanner, which runs at a nominal one megahertz rate. Each cycle of the scanner sequentially checks for a new UART Data Available

flag. When a flag is found, the scanner deposits the character into a sixteen by sixty-four First In/First Out buffer. This buffer has the following characteristics: If space is available in the FI/FO buffer, the character will be written into the buffer. It will then automatically propagate down to the first available open slot. It will be stored there until a character is removed from the output side, remaining characters propagate toward the output. The character is stored with the following format. The data bits are stored in the low byte or first eight bits, the channel number is stored in two bits, and the status information is stored in three bits (parity, overrun and framing error). Bit 15 indicates a valid entry when it is present. Once any character reaches the output of the buffer, a Receiver Done occurs, thus indicating the service routine must read the buffer to obtain the character. As the character is read, the FI/FO buffer output is incremented, causing the contents to propagate down, now providing the next character stored in the buffer.

The software services the Receiver Done flag on either an interrupt or flag checking basis. In either case, characters are serviced out of the FI/FO buffer. As each character is read from the buffer, the next character is presented at the output (assuming that one was in the buffer). The service routine should process all characters in the FI/FO to avoid overhead involved in entering and leaving the service routine. The service routine deals with only the output of the FI/FO buffer and cannot alter or affect the scanner phases.

3.2 Transmitter Control:

The transmitter control section utilized UARTS for parallel to serial conversion of transmit characters for each line. The transmitter uses four bits of the low byte of the Transmitter Control Register (TCR) for the enabling of each transmitter of a per-line basis. Setting the bit for a particular line will cause the "pseudo-scanner" to stop at this line if Transmit Buffer Empty (TBMT) is set and thus set the Transmitter Ready bit. If the Transmitter Interrupt Enable bit is set, an interrupt will be generated. Note, that if all TCR bits are clear, the Transmitter Ready bit will be clear, this is a departure from conventional signle line unit ready flags.

If the TCR bit is set for a particular line, the "pseudo-scanner" will stop when it detects the AND condition of TCR and TBMT for this particular line. Transmitter Ready will then set. An interrupt will be generated if Transmitter Interrupt Enable is set. The service routine should read the TRANSMITTER LINE bits located in the high byte

of the Control and Status Register. The routine then loads the appropriate character into the low byte of the Transmit Data Register, and the "pseudo scanner" automatically clears Transmitter Ready and begins searching for another AND condition of TBMT and TCR. The "pseudo-scan" is a four level priority encoder. A sampling clock records the respective states of the AND conditions of TBMT and TCR for the lines. The states are then presented to a priority encoder which produces the Transmitter Line bits and Ready Flag. The clock then stops, waiting for the character to be loaded. Once loading of the Transmit Data Register has occurred, the clock is restarted and a new sample is produced for the priority encoder. Transmitter Line Number three has the highest priority, while line number zero has the lowest.

When operating in interrupt mode, the service routine should check to assure no other lines require servicing before exiting. This would reduce the number of times that the service routine would have to be entered, thus reducing the overhead per character.

Breaks may be transmitted on any line by asserting the corresponding bit in the high byte of the Transmit Data Register. This pulls the output line to a space and holds it there until the bit is cleared. Timing of the breaks must be done by the software.

3.3 Maintenance Provisions:

Three methods of maintenance testing are provided with the DZV11. For systems testing, the multiplexor has a maintenance bit (CSR03) which will internally loopback all the data leads. In this mode, only the data leads are disconnected from the EIA drivers and receivers.

For complete line testing of the EIA logic, an H329 module test connector can be installed on the socket housing of the M7957. This provides staggered loopback in the following manner:

Transmitted Data Line 00 to Received Data Line 01
Transmitted Data Line 01 to Received Data Line 00
Transmitted Data Line 02 to Received Data Line 03
Transmitted Data Line 03 to Received Data Line 02

Data Term Rdy Line 00 to Ring & Carrier Line 01
Data Term Rdy Line 01 to Ring & Carrier Line 00
Data Term Rdy Line 02 to Ring & Carrier Line 03
Data Term Rdy Line 03 to Ring & Carrier Line 02

The third level of maintenance testing is offered at the option acceptance level. An H325 cable test connector can be used with the BC11U cable assembly to provide single line loopback capabilities. The H329 and H325 test connectors are supplied as a basic item of the DZV11-B option only.

3.4 BC11U, Interface Cable:

The interfacing cable for modem and terminal connections to the DZV11-B is provided by the BC11U cable assembly. It consists of four separate cables. Each cable is terminated by a separate DB25-P type connector and a common Berg housing. The housing connects the EIA input/output leads of the module to the appropriate pinning of a DB25-P connector. The following list of connector pins are typical for each line on the assembly.

PIN NUMBER	DESCRIPTION	
1	Protective Ground	*
2	Transmitted Data	
3	Received Data	
4	Request to Send	
7	Signal Ground	*
8	Carrier	
20	Data Terminal Ready	
22	Ring Indicator	
25	Forced Busy	**

* Common Connection
** Optionally Controlled by Request to Send

Request to Send is connected to Data Terminal Ready through a jumper on the module. This allows Request to Send control for full duplex 202 Modem applications. Additional per line jumpers are also provided to allow Request to Send to control Forced Busy.

3.5 Throughput:

Each DZV11 is capable of a throughput rate of 10,970 characters per second. This rate is calculated as follows:

(Bits/Seconds x No. Lines X Direction) divided by Bits/ Character. (9600 x 4 x 2) 1/7 equals 10,970 Character/ Second.

For a character service routine of 100 µsec or less, the device throughput rate can be sustained.

4.0 Programming

The DZV11 contains six addressable registers. They are listed as follows:

A. Control & Status Register
B. Receiver Buffer Register
C. Line Parameter Register
D. Transmitter Control Register
E. Modem Status Register
F. Transmit Data Register

4.1 Address Allocation:

The device address assigned to the DZV11 resides in the floating address space of the LSI-11. This address space ranges from 160010_8 to 163776_8. Each DZV11 requires increments of 10_8 address locations. Since program compatibility is maintained with the Unibus counterpart DZ11, the DZV11 multiplexor must use the space allocated for the DZ11. This imposes that address gaps occur for those Unibus counterpart devices that may or may not be designed for the LSI bus. With this restriction, the DZV11 is arranged as the eighth device in the floating address space. Other LSI bus devices that have counterpart Unibus devices and which occupy the floating address space are the DUV11 and DPV11. These are arranged as the fourth and fifth devices respectively.

4.2 Interrupt Allocation:

The DZV11 device vector address is selected from the floating vector space. This space ranges from address 300_8 to address 776_8. Vector address compatability with the DZ11 must also be adhered to by the DZV11. The multiplexor is thus assigned as the twenty-sixth device in the floating vector space. The DUV11 and DPV11 are assigned as the twentieth and twenty-first device respectively.

Each DZV11 requires two interrupt vectors, one for the transmitter section and one for the receiver section. If simultaneous interrupt requests were generated from each section, the receiver section would have priority in placing its vector onto the LSI bus. A receiver interrupt to address XX0 will be generated from having either a Receiver Done (CSR 07) or Silo Alarm (CSR13) occurrance. A transmitter interrupt to address XX4 will be generated by Transmitter Ready (CSR15). Additional prerequisites for generating interrupts are that the individual interrupt enable bits (CSR 06 and CSR 14) be set. The recommended method of clearing interrupt enable bits is to first raise the Processor Status Word to level four, next clear these interrupt

enable bits and then lower the Processor Status Word to zero. Using this method prevents false interrupts from being generated.

4.3 Control & Status Register: (CSR) 76XXX0

The Control and Status Register is a byte and word addressable register. All bits in the CSR are cleared by an occurrance of BINIT or by setting device Master Clear (CSR 04). The bit assignment is as follows:

Bit	Description
00-02	Unused. Read as zero
03	Maintenance This bit, when set, loops all the transmitter's serial output leads to the corresponding receiver's serial input leads on a TTL basis. While operating in maintenance mode, the EIA received data leads are disabled. Normal operating mode is assumed when this bit is cleared. This bit is Read/Write.
04	Master Clear When written to a one, generates "Initialize" within the DZV11. A read back of the CSR with this bit set, indicates initialize in progress within the device. This bit is self-clearing. All register, silos and UARTS are cleared with the following exceptions: A. Only bit 15 of the Receiver Buffer Register (VALID DATA), the remaining bits 00 through 14 are not. B. The high byte of the Transmitter Control Register is not cleared by Master Clear. C. The Modem Status Register is not cleared by Master Clear.
05	Master Scan Enable This Read/Write bit must be set to permit the receiver and transmitter control sections to begin scanning. When cleared, Transmitter Ready

(CSR 15) will be inhibited from setting and the received character buffers (Silos) will be cleared.

06 Receiver Interrupt Enable

This bit, when set, permits the setting of CSR 07 or CSR 13 to generate a receiver interrupt request. This bit is Read/Write.

07 Receiver Done

This is a read only bit that will set when a character appears at the output of the FI/FO buffer. To operate in interrupt per character mode, CSR 06 must be set and CSR 12 must be cleared. With both CSR 06 and CSR 12 cleared, character flag mode would be indicated. Receiver Done will clear when the Receiver Buffer Register (RBUF) is read or when Master Scan Enable (CSR 05) is cleared. If the FI/FO buffer contains an additional character, the Receiver Done flag will stay cleared a minimum of one microsecond before presenting that character.

08-09 Transmitter Line Number

These read only bits indicate the line number whose transmit buffer requires servicing. These bits are valid only when Transmitter Ready (CSR 15) is set and will be cleared when Master Scan Enable is cleared. Bit 08 is the least significant bit.

10-11 Unused. Read as zero.

12 Silo Alarm Enable

This is a Read/Write bit, when set, enables the silo alarm counter to keep count of the number of characters stored in the FI/FO buffer. The counter will be

cleared when the Silo Alarm Enable bit is cleared. Conditioning of this bit must occur prior to any character reception.

13 Silo Alarm

This is a read only bit set by the hardware after 16 characters have been entered into the FI/FO buffer. Silo Alarm will be held cleared when Silo Alarm Enable (CSR 12) is cleared. This bit will be reset by a read to the Receiver Buffer Register and will not set until 16 additional characters are entered into the buffer. If Receiver Interrupt Enable (CSR 06) is set, the occurrance of Silo Alarm will generate a receiver interrupt request. Reception with CSR 06 cleared, permits flag mode operation of the Silo Alarm bit.

14 Transmitter Interrupt Enable

This bit must be set for Transmitter Ready to generate an interrupt. It is Read/Write.

15 Transmitter Ready

This bit is read only and is set by the hardware. This bit will set when the transmitter clock stops on a line whose transmit buffer may be loaded with another character and whose associated TCR bit is set. The Transmitter Line Number, specified in CSR 08 and CSR 09, is only valid when Transmitter Ready is set. Transmitter Ready will be cleared by any of the following conditions:

1. Master Scan Enable cleared.
2. When the associated TCR bit is cleared for the line number pointed to in CSR 08 and CSR 09.

3. At the conclusion of the load instruction of the Transmit Data Register (low byte only).

If additional transmit lines require service, Transmitter Ready will reappear within a min. of 1.4 usec from the completion of the Transmit Data Register load instruction. The occurrance of Transmitter Ready with Transmitter Interrupt Enable set, will generate a transmitter interrupt request.

4.4 Receiver Buffer Register: (RBUF) 76XXX2 READ ONLY

This is a 16 bit read only register which contains the received character at the output of the FI/FO buffer. A read of the register causes the character entry to be extracted from the buffer and all other entries to bubble down to the lowest unoccupied location. Only the Valid Data bit (RBUF 15) is cleared by BINIT or by setting device Master Clear (CSR 04). Bits 00-14 are not affected. The format of the RBUF register is defined as follows:

Bit	Description
00-07	Received Character These bits contain the received character, right justified. The least significant bit is bit 00. Unused bits are 0. The parity bit is not shown.
08-09	Received Character Line Number These bits contain the line number upon which the aforementioned character was received. Bit 08 is the least significant bit.
10-11	Unused. Read as zero.
12	Parity Error This bit is set if the sense of the parity of the received character does not agree with that designated for that line.

13	Framing Error This bit is set if the received character did not have a stop bit present at the proper time. This bit is usually interpreted as indicating the reception of a break.
14	Overrun Error This bit is set if the received character was preceded by a character that was lost due to the inability of the receiver scanner to service the UART receiver holding buffer on that line.
15	Valid Data This bit, when set, indicates that the data presented in bits 00-14 is valid. This bit permits the use of a character handling program that takes characters from the FI/FO buffer until there are no more available. This is done by reading this register and checking bit 15 until the program obtains a word for which bit 15 is zero.

4.5 Line Parameter Register: (LPR) 76XXX2 WRITE ONLY

This register controls the operating parameters associated with each line in the DZV11. The LPR register is a word addressable, write only register. The line parameters for all lines must be reloaded following an occurrance of either BINIT or device Master Clear.

Bit	Description
00-01	Parameter Line Number These bits specify the line number for which the parameter information (bits 3 through 12) is to apply. Bit 00 is the least significant bit.

02 — Unused. Must always be written as a zero when specifying the Parameter Line Number. Writing this bit as a one will extend the Parameter Line Number field into non-existant lines. Parameters for lines 00 through 03 will not be affected.

03-04 — Character Length
These bits are set to receive and transmit characters of the length (excluding parity) as shown below.

04	03	
0	0	5 bit
0	1	6 bit
1	0	7 bit
1	1	8 bit

05 — Two Stop Bits
This bit, when set, conditions a line transmitting with 6,7 or 8 bit code to transmit characters having two stop marks. If the line is transmitting 5 bit code, assertion of this bit causes the characters to be transmitted with 1.5 stop marks. If this bit is not asserted, 1 stop mark is sent.

06 — Parity Enable

If this bit is set, characters transmitted on the line have an appropriate parity bit affixed; and characters received on the line have their parity checked.

07 — Odd Parity
If this bit is set and bit 06 is set, characters of odd parity are generated on the line and incoming characters are expected to have odd parity. If this bit is not set, but bit 06 is set, characters of even parity are generated on the line and incoming characters are expected to have even parity. If bit 06 is not set, the setting of this bit is immaterial.

08-11 — Speed Code

The state of these bits determine the operating speed for the transmitter and receiver of the selected line.

11	10	09	08	Baud Rate
0	0	0	0	50
0	0	0	1	75
0	0	1	0	110
0	0	1	1	134.5
0	1	0	0	150
0	1	0	1	300
0	1	1	0	600
0	1	1	1	1200
1	0	0	0	1800
1	0	0	1	2000
1	0	1	0	2400
1	0	1	1	3600
1	1	0	0	4800
1	1	0	1	7200
1	1	1	0	9600
1	1	1	1	Invalid

12 — Receiver Enable
This bit must be set before the UART receiver logic can assemble characters from the serial input line. This bit will be cleared following a BINIT or device Master Clear.

13-15 — Unused

4.6 Transmitter Control Register: (TCR) 76XXX4

The TCR register is a byte and word addressable register. The low byte of the TCR register contains the transmitter control bits which must be set to initiate transmission on a line. Each TCR bit position corresponds to a line number. For example, TCR bit 00 corresponds to line 00, bit 01 to line 01, etc. Setting of a TCR bit causes the transmitter scanner clock to stop if the UART for this line has a transmit buffer empty comdition. An interrupt will then be generated if Transmitter Interrupt Enable is set. The scanner clock will restart when either the Transmit Data Register is loaded with a character or the TCR bit is cleared for the line on which the clock has stopped. TCR bits must only be cleared when the scanner is not running, i.e., Transmitter Ready is set or Master Scan Enable is cleared.

The TCR bits are represented in bits 00 through 03. These bits are Read/Write and cleared by BINIT or device Master Clear. Bits 04 through 07 are unused and read as zero.

The high byte of the TCR register contains the writeable modem control lead, Data Terminal Ready (DTR). Bit designations are as follows:

Bit	Name
08	DTR Line 00
09	DTR Line 01
10	DTR Line 02
11	DTR Line 03
12-15	Unused. Read as zero

Assertion of a Data Terminal Ready bit puts an ON condition on the appropriate modem circuit for that line. Data Terminal Ready bits are Read/Write and cleared only by BINIT. Jumpers have been provided to allow the Request to Send circuits to be asserted with Data Terminal Ready assertions.

4.7 Modem Status Register: (MSR) 76XXX6 READ ONLY

This is a sixteen bit read only register. A read to this register results in the status of the readable modem control leads, Ring and Carrier. The ON condition of a modem control lead is interpreted as a logical one. Bits 04 through 07 and 12 through 15 are unused and read as a zero. Remaining bit designations are as follows:

Bit	Name
00	Ring Line 00
01	Ring Line 01
02	Ring Line 02
03	Ring Line 03
04-07	Unused. Read as zero.
08	Carrier Line 00
09	Carrier Line 01
10	Carrier Line 02
11	Carrier Line 03
12-15	Unused. Read as zero.

4.8 Transmit Data Register: (TDR) 76XXX6 WRITE ONLY

The TDR Register is a byte and word addressable, write only register. Characters for transmission are loaded into the low byte. TDR bit 00 is the least significant bit. Loading of a character should occur only when Transmitter Ready (CSR 15) is set. That character which is loaded into this register is directed to the line defined in CSR bits 08 and 09. The high byte of the Transmit Data Register is designated as the Break Control Register.

Each of the four multiplexor lines has a corresponding break bit for that line. TDR bit 08 represents the break bit for line 00, TDR bit 09 for line 01, etc. TDR bits 12 through 15 are unused. Setting a break bit will force that lines output to space. This condition will remain until cleared by the program. This register is cleared by BINIT or device Master Clear. The Break Control Register can be utilized regardless of the state of the device Maintenance bit (CSR 03).

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TITLE DZV11 Test and Acceptance Procedure

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REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE

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TITLE DZV11 Test and Acceptance Procedure

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	A	SP	DZV11-Ø-3	

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95

The following paragraphs provide testing procedures for the DZV11 option in all its variations. It is assumed that the user has a good working knowledge of the LSI11 QBUS and the DZV11. If not, the following references are required reading:

1. DZV11 User's Guide (ED-DZV11-UG-xxx)
2. Microcomputer Handbook
3. LSI11, PDP11/03 User's Manual (ED-LSI11-TM-xxx)

The DZV11 is a four line asynchronous interface that is used with the LSI11 processor. It provides an EIA interface and enough data set control to permit dial-up operation with full duplex modems such as the Bell series 103, 113 and equivalent.

The DZV11 can be supplied in two different configurations, each designated by a suffix letter (A or B). Each multiplexor configuration utilizes a quad height module designated the M7957. All input and output leads of the M7957 conform to EIA standard RS232C and are available on a Berg header.

The required hardware for the DZV11-A option is just the M7957 module. Cabling assemblies to terminals and modem channels are not supplied with this option, but are available in the DZV11-B configuration. Each DZV11-B configuration consists of an M7957 module, BC11U-25 cable assembly, and two accessory test connectors, H329 and H325.

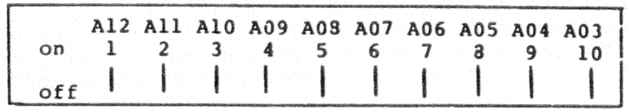
1. DZV11 Device Address

The device address assigned to the DZV11 resides in the floating address space of the LSI11. This address space ranges from 160010 (8) to 163776 (8). Each DZV11 requires increments of 10 (8) address locations and the first option should be configured with an address of 160010. The initial configured address assumes that the system consists of only DZV11's in the floating address field. If the DUV11 option is also configured in the floating address field, assign the DZV11 an address which establishes a gap of 10 (8) address locations between the last DUV11 and the first DZV11. For example: If the system consisted of one DUV11 located at 160010 (8), then the DZV11 should be configured with an address of 160030.

1.1 Setting the Device Address

Once the position of the DZV11 has been established in the floating address scheme, the QBUS address is selected by a switch pack on the M7957 module. The IC designator for the ten position dip pack is E30. For a logical one (1) on a QBUS address line, set the rocker switch that corresponds to the particular address bit to the ON (closed) position. The ON position is when the rocker is depressed at the ON side of the switch. Rocker #1 corresponds to the most significant address bit, bit 12, rocker #10 is the least significant address bit selector. The following figures represent the address selector, E30, and the switch settings for some example device addresses.

Address Selector E30



ADDRESS	A12	A11	A10	A09	A08	A07	A06	A05	A04	A03
160000	-	-	-	-	-	-	-	-	-	-
160010	-	-	-	-	-	-	-	-	-	X
160020	-	-	-	-	-	-	-	-	X	-
160030	-	-	-	-	-	-	-	-	X	X
160040	-	-	-	-	-	-	-	X	-	-
etc										
.										
.										
163760	-	-	X	X	X	X	X	X	X	-
163770	-	-	X	X	X	X	X	X	X	X

Note: X=ON
-=OFF

2. DZV11 Interrupt Vector

Similiar to the device address, the vector address of the DZV11 resides in the floating vector space of the LSI11. The vector space ranges from address 300 (8) to address 776 (8). Each DZV11 requires increments of 10 (8) address locations for its two contiguous interrupt vectors. If the DZV11 is the only option in the floating vector area, configure it for a vector of 300 (8). If there are options other than the DZV11 residing in the floating vector area, other configuration rules must be applied. When configuring the device vector, only the first vector address musr be considered. The first vector, or base vector, must start on a zero boundary.

A zero boundary is one which has the three least significant bits equal to zero. The second vector is controlled by the first vector and data bit 02. Data bit 02 is generated by the M7957 hardware.

2.1 Setting the Interrupt Vector

Once the position of the DZV11 has been established in the floating vector scheme, the QBUS vector is selected by a switch pack on the M7957 module. The IC designator for the eight position dip pack is E2. To generate a logical one (1) for the QBUS vector bit, set the rocker switch that corresponds to that particular bit to the ON (closed) position. The ON position is when the rocker is depressed at the ON side of the switch. Rocker #1 corresponds to the most significant vector bit, bit 08, rocker #6 is the least significant vector bit selector. The following figures represent the vector selector, E2, and the switch settings for some example vector addresses.

Vector Selector E2

	V08	V07	V06	V05	V04	V03	NOT USED	
on	1	2	3	4	5	6	7	8
off	|	|	|	|	|	|	|	|

VECTOR	V08	V07	V06	V05	V04	V03
300	-	X	X	-	-	-
310	-	X	X	-	-	X
320	-	X	X	-	X	-
330	-	X	X	-	X	X
etc						
.						
.						
760	X	X	X	X	X	-
770	X	X	X	X	X	X

Note: X=ON
-=OFF

3. Jumper Configuration

There are sixteen jumpers located on the M7957 module. Insertion or removal of a jumper is dependent on its function. Jumper locations can be found on the Unit Assembly drawing of the M7957 module. Jumpers are catagorized as those required for:

3.1 Module Test

There are six (6) jumpers specified to be removed only during module test time at the General Radio test level. At all other levels of testing and for device operation these jumpers must be installed. These jumpers are designated as W9, W12, W13, W14, W15, and W16.

3.2 Device Operation

Two (2) jumpers, W10 and W11, are specified as those which are required for device operation. These jumpers must be installed only when the module is used in an H9270 backplane, or a backplane that applies the QBUS signals to the C and D sections of the module. When installed or tested in a C/D Bus type LSI11 backplane, these jumpers are required to be removed.

3.3 Modem Control Support

There are eight (8) jumpers which are used for modem control support. These jumpers, W1 thru W8, are required to be installed at module test, opcion test and acceptance time. Jumpers W1 thru W4, when installed, allow assertion of the Request to Send lead to the modem by the setting of Data Terminal Ready in a DZV11 device register. Each line is provided with a jumper option. W1 represents the jumper option for line 3, W2 for line 2, W3 for line 1 and W4 for line 0. The remaining four jumpers, W5 thru W8, allow the Request to Send lead to control the Forced Busy lead to the modem. The assertion of a Request to Send lead applies an ON or Busy condition to the Forced Busy lead. Each line is provided with a jumper option, W5 represents line 3, W6 represents line 2, etc. The Forced Busy option is available with 103E and 113B modems.

4. Power Requirements

1.15 Amps @+5 Volts
0.39 Amps @+12 Volts

5. Enviornmental Specifications

The DZV11 operates in an environment from 5 to 50 degrees Centigrade (41 to 122 degrees F) with a relative humidity of 10% or less to 95% without condensation.

6. Maintenance Philosophy

Maintenance of the DZV11 is accomplished by following this test procedure while using the device diagnostics. The testing can be divided into five areas.

6.1 Visual Inspection

This is a visual check for solder shorts and damaged or missing components. A visual inspection can often save needless checkout time.

6.2 Internal Loopback

This is the simplest maintenance mode provided and it is the first logical mode used in this procedure. With bit 03 of the DZV11's Control and Status Register set, the output serial data from the Uarts are looped back into their respective serial data inputs. All lines are looped around simultaneously.

6.3 Staggered Loopback

In this mode of operation, the output signals from line 0 connect back to the inputs of line 1 and the output signals of line 1 connect back to the inputs of line 0. Lines 2 and 3 are looped back in the same manner. To operate in this mode, the H329 test connector is required and the device maintenance bit (CSR 03) is kept cleared.

6.4 External Test

This maintenance mode tests the lines to the point where the customer attaches the modem or terminal. Testing in this mode requires that the H325 test connector be attacned to one individual line of the BC11U cable assembly. In external mode, each line of the DZV11 can be tested by changing the H325 to a new line required for each test.

6.5 On Line Test with Terminal

In this mode of operation, an EIA terminal is connected to a single line of the BC11U cable assembly. All lines are individually checked out with the aid of a device diagnostic.

7. Diagnostics

Four device diagnostics have been created for checkout of the DZV11. These are available as libkit #ZJ251. In addition to the diagnostics, a DEC/X11 exercisor module, Maindec-11-DXDZB, is available. The following is a short description of each program.

7.1 Maindec Introduction

A) Maindec-11-DVDZA. This is the first diagnostic of a two part series which is used for basic option checkout. This program exercises the read/write bits of the registers, performs simple transmission and reception exercises for each line and verfies the interrupt capabilities of the option.

B) Maindec-11-DVDZB. This diagnostic continues the series of basic option diagnostics. Exercises of the transmitters and receivers in all possible operating modes and at all possible data rates are performed. Error conditions are induced on the line and the option is then checked for its ability to recognize these errors.

C) Maindec-11-DVDZC. Maindec DVDZC verifies the cable interface connection between the module and the EIA connector. The diagnostic provides the operator a choice of testing the cable interface assembly or testing the actual connection of a line to an EIA supported terminal.

D) Maindec-11-DVDZD. This program is designed as a verification aid for the field service personnel in establishing a communication link from the DZV11 to another LSI11 or to a communications test center. It is used with the Interprocessor Test Program (Maindec-11-DZITP) as an overlay to the monitor.

E) Maindec-11-DXDZB. DXDZB is a systems exercisor module used with DEC/X11. It can operate up to eight consecutively addressed DZV11 multiplexors. Internal maintenance mode is implemented for transmission and reception of character bursts of data. All lines of each selected multiplexor are enabled for running.

7.2 Operation of Diagnostics

The basic checkout programs, Maindecs DVDZA, DVDZB, and DVDZC, each require 4K of memory for operation. All programs are in absolute format and can be loaded using the absolute loader. Other media, such as disks, may also be used.

Once a diagnostic has been loaded into memory, it is started at location 200 (8). The diagnostics will either autosize the system or request operating parameters before execution of the tests. The value contained in the software switch register determines the startup mode of the program. Address 176 (8) is reserved as the software switch register. The writeups for each diagnostic provide a more detailed explanation of their operation.

7.2.1 Autosizing

When a diagnostic is initially started and the software switch register location is cleared, autosizing will be performed. The autosizer routine is designed to detect all DZV11 device and vector addresses within the floating address and vector area. Other parameters required for device testing are given defaulted values. These values include testing of all four lines, with internal maintenance mode selected and at a baud rate of 19.2K baud.

The autosized values used during testing will be displayed on the console in the form of a DZV11 status table. The status table values must be verified for their correctness by the operator. Maindec's DZDVA and DZDVB are the only diagnostics to have autosizing capabilities. The remaining diagnostics require either a monitor or manual intervention for execution and do not autosize.

7.2.2 Parameter Input

An operator may also supply specific parameters for testing if it is desired. This feature is provided by having the software switch register bit 00 set when Maindec DVDZA or Maindec DVDZB is started. The operator must then input a response to the following dialogue on the console terminal:

lst CSR ADDRESS (160000:163770):
(You must type in the first DZV11 CSR in the system you wish testing to begin at. Range: 160000:163770.)

lst VECTOR ADDRESS (300:770):
(You must type in the vector of the first DZV11 in the system under test. Range: 300:770.)

MAINTENANCE MODE
(EXTERNAL (H325) (E))
(INTERNAL (DZCSR03=1 (I))
(STAGGERED (H329) (S))
(Type "E" or "I" or "S" depending on which mode you wish to run in. If running "EXTERNAL", all selected lines must be terminated by H325 test connectors.)

OF DZV11's (IN OCTAL) (1:20):
(Type the total number of DZV11 to be tested in the system. Range is 1 thru 20 in octal.)

All responses are terminated by typing a carriage return. It is important to note that all the DZV11's must be contiguous for both address and vector. Also all the extra parameters such as the default baud rate and the number of active lines for each device are given to the existing DZV11's in the system.

Operation of Maindec DVDZC always requires an opening dialogue. Special software switch register settings are not required when this diagnostic is started. Since this program provides both a cable interface test and a terminal echo test, the response depends on the specific test required by the operator. The following is printed on the console terminal when the cable test is selected:

VECTOR ADDRESS-
(You type a vector followed by a carriage return.)

CONTROL REGISTER ADDRESS-
(You type in the DZV11 CSR address under test followed by a carriage return.)

WHICH TEST? ECHO OR CABLE (E OR C)
(Type C and a carriage return.)

BAUD RATE-
(Type either 50, 110, 135, 150, 300, 600, 1200, 1800, 2000, 2400, 3600, 4800, 7200, 9600 followed by a carriage return.)

LINE-
(You type the line which has the H325 test connector. Type either 0, 1, 2, 3). Program will then print:)

CABLE TEST-
(The diagnostic is now exercising the selected line.)

Selection of the terminal echo test will repeat the vector and control register address questions and print out the following:

```
WHICH TEST? ECHO OR CABLE (E OR C)
                        (Type E and a carriage return.)
BAUD RATE-
                        (Type a baud rate value followed
                        by a carriage return.)
LINE-
                        (Type a line number followed by
                        a carriage return. The program
                        will print:)
TERMINAL ECHO TEST
TYPE A CHARACTER ON THE DZV11 TERMINAL
                        (The program has now transmitted
                        an output message to the DZV11
                        terminal and is waiting for a
                        printable character to be typed
                        on the terminal. The program will
                        then echo all printable characters
                        that are received.)
```

By typing any printing key on the cinsole terminal, a request for a new line number will be asked. At this time the operator should attach either the H325 test connector or the output terminal to a new line and continue operating the program until all lines are checked.

7.2.3 Status Table

This is the description given to a reserved area of memory, addresses 1500 thru 1740, that DZDVA and DZDVB use for storing the operating parameters of the tests. Each DZV11 on the system requires five consecutive address locations for storage and a total status table support of sixteen DZV11s. The methods described previously, autosizing or console input, are used to configure this input table. The following represents a typical status table printout:

```
MAP OF DZV11 STATUS
1500      160100
1502      000300
1504      000017
1506      017470
1510      100000
```


The previous information will be repeated for each of up to 16 DZV11's in the system. Explanation.

1500	160100	This is the system control register for the first DZV11 in the system.
1502	000300	This is the receiver interrupt vector for the first DZV11 in the system.
1504	000017	This is the bit representation of the active lines to be tested.
1506	017470	This is the parameter location used in most of the tests. It signifies the following: Receiver Enabled, 19.2K Baud, Eight bits per character, and Two stop bits. This value is loaded into the Line Parameter Register of the device.
1510	000000	This location contains the type of maintenance selected for testing. 000000=Internal Maintenance Mode 000200=External Maintenance Mode H325 100000=Staggered Mode (H329)

8. Test Procedure

8.1 Module Checkout

All DZV11 modules are General Radio tested and require no further testing at this level. Jumpers W9, W12, W13, W14, W15, and W16 must be removed for this level of testing. When module checkout is complete, all jumpers must be installed for the level of checkout.

8.2 Option Checkout

This procedure checks both variations of the DZV11 (DZV11-A & B) Any differences in the checkout procedure due to the different optios are noted where applicable.

8.2.1 Preliminary Setup:

a) Visually inspect the module for broken or damaged components and make any necessary replacements.
b) Verify that all current ECO's, if any, are installed.
c) Set the address dipswitch to 160010 and the vector dipswitch to 300. Refer to the DZV11 Address and Interrupt Vector sections for assistance. Note also that all jumpers

should be installed before testing. Jumpers W10 and W11 are exceptions as they apply to the type of QBUS backplane to be used.
d) Check for power shorts to ground and for shorts between different voltages. The power distribution on the module pins is as follows:
+5v pins BV1 or A2 of all sections
+12v pin BD2
gnd pins C2 or T1 of all sections

8.2.2 DZV11-A Testing

a) Install the DZV11-A option in the QBUS backplane. When inserting the module, make sure that the power is off and be careful to avoid snagging the components on the card guides and adjacent module.
b) Turn on power and load Maindec-11-DVDZA into memory.
c) Open location 176 (8) and enter the value 000001. This location is the software switch register and the value entered represents a request to input parameters from the console. Refer to section, Operation of Diagnostic, for assistance. Close the location with a carriage return.
d) Type 200G on the console. The introductory title for DVDZA will be printed and the parameter input dialogue will be entered. Respond appropriately to all questions, making sure that I is typed when selecting maintenance mode. Note that all DZV11-A options can only be tested with internal maintenance mode selected. Step C may be omitted if autosizing is desired. Internal maintenance mode operation is then defaulted to.
e) The program will then print RUNNING on the console and procede to execute the various tests. First pass execution time is approximately 20 seconds. Subsequent passes require approximately 90 seconds. Three error free end of pass printouts are required for each selected DZV11-A
f) At the completion of step E, load Maindec-11-DVDZB into memory.
g) The status table for the selected devices has not been modified by the loading of DVDZB. Open location 176 (8) and enter the value 000200. This indicates that the existing table can be used, as built, without the need for console input. Internal maintenance mode operation is then defaulted to.
h) Type 200G on the console. The introductory title for DVDZB will be printed, followed by RUNNING. Program execution will now begin. First pass run time is approximately 1½ minutes. Subsequent passes require 2½ minutes. Three error free end of pass printouts are required for each selected DZV11-A. DZV11-A option checkout is now complete.

8.2.3 DZV11-B Testing

a) Insert the H329 module test connector in the 40 pin housing of the module. It should be connected with the letter side facing up. Next install the option in the QBUS backplane. When inserting the module, make sure the power is off. Be careful to avoid snagging the components on the card guide edges and on adjacent modules.
b) Turn on power and load Maindec-11-DVDZA into memory.
c) Open location 176 (8) and enter the value 000001. This represents a request to input parameters from the console. Close the location by typing a carriage return.
d) Type 200G on the console. The introductory title for DVDZA will be printed and the parameter input dialogue will be entered. Respond appropriately to all questions, making sure that S is typed when selecting maintenance mode. All DZV11-B options are to be tested with staggered maintenance mode selected.
e) The program will print RUNNING on the console and procede to execute the various tests. First pass execution time is approximately 20 seconds. Subsequent passes require approximately 90 seconds. Three error free end of pass printouts are required for each selected DZV11-B.
f) At the completion of step E, load Maindec-11-DVDZB into memory.
g) The status table for the selected device has not been modified by the loading of DVDZB. Open location 176 (8) and enter the value 000200. This indicates that the existing table can be used as built, without the need for a console input. Close the location by typing a carriage return.
h) Type 200G on the console. The introductory title for DVDZB will be printed, followed by RUNNING. Program execution will now begin. First pass run time is approximately 1½ minutes. Subsequent passes require 2½ minutes. Again, three error free end of pass printouts are required for each selected DZV11-B.
i) At the completion of step H, stop the program and power down. Remove the module from its backplane slot. Replace the H329 test connector with the Berg end of the BC11U acble assembly. Terminate line 0 of the cable with an H325 connector. Install the module in the backplane and apply power.
j) Load Maindec-11-DVDZC into memory. Type 200G on the console terminal. Select the cable test, at 9600 baud for line 0.

k) The program will execute the cable test and printout the end of pass message within 15 seconds. Three error free end of pass printouts are required for each line. Longer execution times can be expected at lower baud rates.
l) Complete the checkout of the remaining lines by typing any printing key on the console terminal. This requests that a new line number be entered and that the H325 terminate the new line. Continue testing until all lines are successfully checked. DZV11-B option checkout is now complete.

8.3 System Test and Acceptance

The first level of system checkout for the DZV11(s) shall include a successful completion of that particular option using its option level testing procedure. The final level of system test will be to run the DEC/X11 systems exercisor module. Other options on the system should be exercised in addition to the DZV11 option(s) under test. Run the exercisor for three completions without error. If the DZV11 is an add-on and does not ship as part of a system, the exercisor is not required as part of the system acceptance. Check the shipping list (A-PL-DZV11-0-4) and verify nothing is missing. Acceptance is complete.

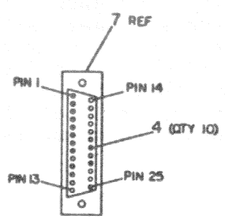
WIRE TABLE

ITEM NO.	DESCRIPTION AWG	DESCRIPTION COLOR	FROM POINT	FROM CONNECTION	FROM TERM	TO POINT	TO CONNECTION	TO TERM	REMARKS
	22	BLK		P1-1			P5-A	3	
		BRN		P1-2			P5-B		
		GRY		P1-3			P5-C		
		BLU		P1-4			P5-M		
1		ORN		P1-5	4		P5-J		
		RED		P1-8			P5-L		
		YEL		P1-25			P5-F		
		VIO		P1-7			P5-K		
		WHT		P1-20			P5-D		
		GRN		P1-22			P5-E		
		BLK		P2-1			P5-M		
		BRN		P2-2			P5-N		
		GRY		P2-3			P5-P		
		BLU		P2-4			P5-U		
1		ORN		P2-5	4		P5-V		
		RED		P2-8			P5-X		
		YEL		P2-25			P5-Y		
		VIO		P2-7			P5-W		
		WHT		P2-20			P5-R		
		GRN		P2-22			P5-S		
		BLK		P3-1			P5-JJ		
		BRN		P3-2			P5-HH		
		GRY		P3-3			P5-FF		
		BLU		P3-4			P5-BB		
1		ORN		P3-5	4		P5-AA		
		RED		P3-8			P5-Y		
		YEL		P3-25			P5-CC		
		VIO		P3-7			P5-Z		
		WHT		P3-20			P5-EE		
		GRN		P3-22			P5-DD		
		BLK		P4-1			P5-VV		
		BRN		P4-2			P5-UU		
		GRY		P4-3			P5-TT		
1		BLU		P4-4	4		P5-NN		
		ORN		P4-5			P5-MM		
		RED		P4-8			P5-KK		
		YEL		P4-25			P5-PP		
		VIO		P4-7			P5-LL		
		WHT		P4-20			P5-SS		
	22	GRN		P4-22			P5-RR	3	

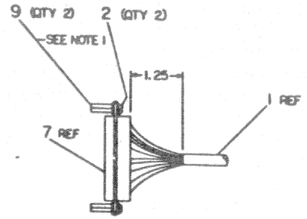
LEGEND		
NUMBER	DIM "X" VARIATION	DIM "Y" (PRECUT) REF
BC11U-25	25 FT. ±3 INCHES	25 FT. 2 INCHES ±3 INCHES

NOTES:

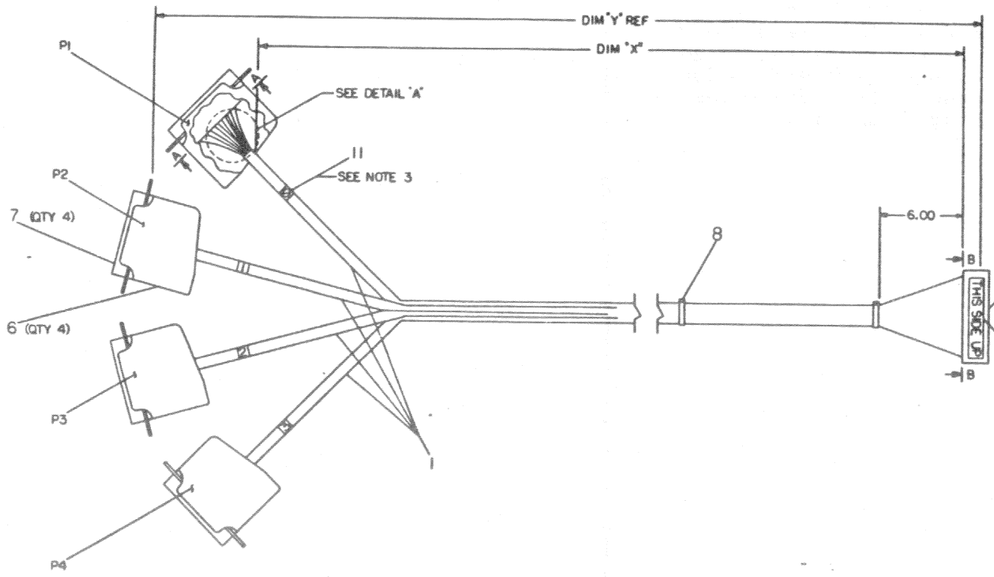
1. SPACER (ITEM 9) TO BE DISCARDED IF NOT REQUIRED FOR CABLE CONNECTION.
2. CABLE TIES (ITEM 8) TO BE USED APPROXIMATELY EVERY 3 INCHES FOR 4 FEET STARTING AT P5 (ITEM 5).
3. MARKERS (ITEM 11) TO BE USED TO IDENTIFY CABLES (ITEM 1).
4. LABEL (ITEM 10) TO BE PLACED ON LETTERED SIDE OF TERMINATOR (ITEM 3).

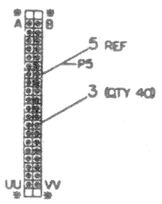


VIEW A-A
SCALE: NONE
(P1, P2, P3, P4)



DETAIL "A"
(P1, P2, P3, P4)





VIEW B-B
SCALE: 2/1
* INDICATES CAVITIES NOT USED

4	MARKERS, TERMINAL	9008384-01	11
1	LABEL, (THIS SIDE UP)	3611567-00	10
8	SPACER, HEX, 4-40 X .25	9008436-00	9
17	TIE, CABLE	9007880-00	8
4	CONN., SHELL MALE	1210493-51	7
4	CONN., HOOD W/STRAIN RELIEF	1210433-50	6
1	TERMINATOR, 44 POS HOUSING	1210918-15	5
40	CONN., PIN, 20-24 AWG	1210499-33	4
80	SOCKET, CRIMP	1210089-03	3
8	SCREW, CAP, 8851-9-40 X .25	1210-993-51	2
AR	CABLE, 10 CONDUCTOR	31076.21-00	1
	DESCRIPTION	ENGINEER NO.	ITEM NO.

DZV11

CABLE ASSY BC11U

B-00-DEV11-0

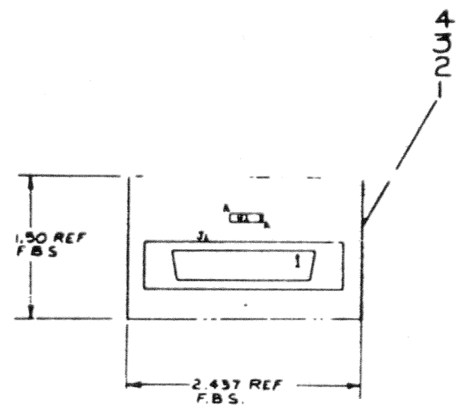
BC11U-0-0

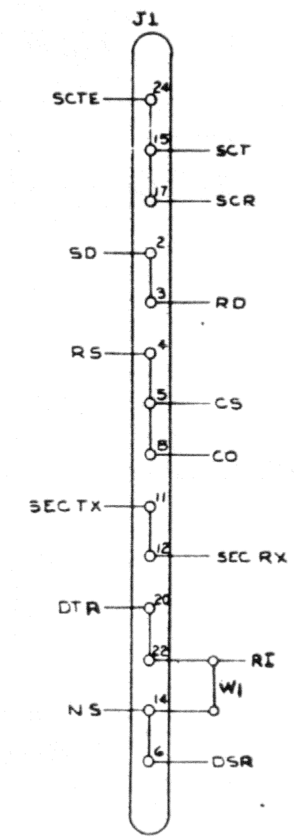
A

SCALE 1

44

NOTES:





PARTS LIST

QTY	REF. DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.
REF		X-Y COORDINATE HOLE LOC	K-CO-H325-0-4	1
REF		ASSY/DRILLING HOLE LAYOUT	D-AH-H325-0-8	2
REF		MODULE ECO HISTORY	B-MH-H325-0-6	3
1		ETCHED CIRCUIT BOARD	5011698	4
1	J1	CONNECTOR	1210247	5
1	W1	INSULATED JUMPER WIRE	9009135	6

• IC TYPE	GND	+5V

GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE

IC PIN LOCATIONS

FIRST USED ON OPTION MODEL: DV11

ETCH BOARD REV. C

REVISIONS: REV. A — CHANGE NO. ORIGINATED — H325-00UC1; REV. B — F. ZERESKI

SEMICONDUCTOR CONVERSION CHART

DEC NO.	EIA NO.	DEC NO.	EIA NO.

NEXT HIGHER ASSY: D-UA-DV11-0-0

SCALE —/— SHEET 1 OF 1

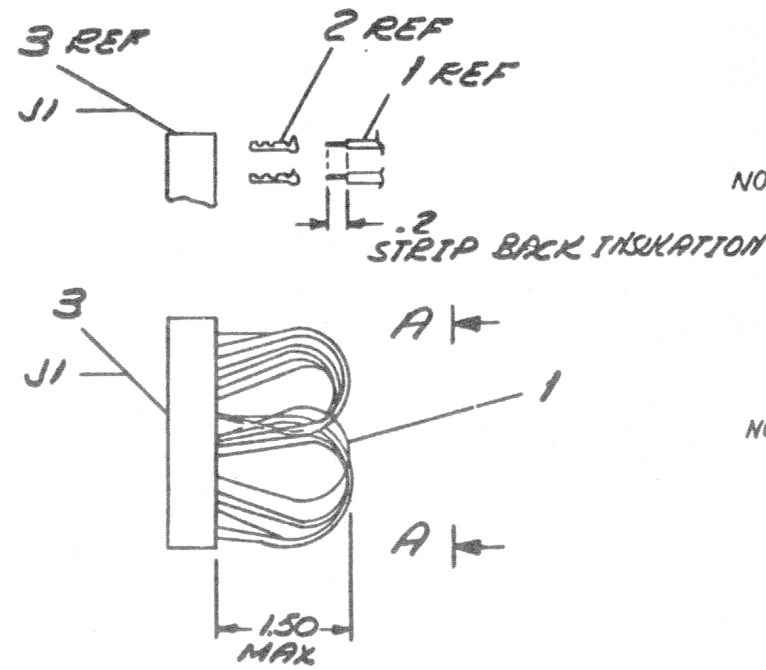
digital

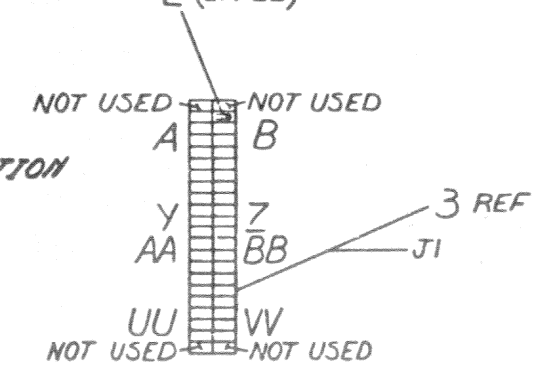
TITLE: H325 TEST CONNECTOR

SIZE D CODE CS NUMBER H325-0-1 REV. B

WIRE TABLE

ITEM NO.	DESCRIPTION AWG	DESCRIPTION COLOR	FROM CONN	FROM WITH	TO CONN	TO WITH
1	26.	BLK	J1-A	2	J1-VV	2
			J1-B		J1-P	
			J1-C		J1-N	
			J1-S		J1-D	
					J1-K	
			J1-L		J1-E	
					J1-R	
			J1-HH		J1-TT	
			J1-FF		J1-UU	
			J1-DD		J1-Y	
					J1-SS	
			J1-KK		J1-EE	
1	26	BLK		2	J1-RR	2





VIEW A-A
(REAR VIEW)

QTY.	DESCRIPTION	PART NO.	ITEM NO.
1	HOUSING, SOCKET	1210928-15	3
22	SOCKET, CRIMP	1210089-05	2
A/R	WIRE #26 AWG, (BLK)	9107636-00	1

PARTS LIST

DRN	DATE
CHK'D S. Roberts	DATE 3 Aug 77
ENG Willis P Smith	DATE 3 Aug 77
PROJ. ENG. Willis P Smith	DATE 3 Aug 77
PROD.	DATE 10 Aug 77

NEXT HIGHER ASSY. B-DD-H329-Ø

SCALE NONE

SHEET 1 OF 1

digital

TITLE DZV11 TEST CONNECTOR

SIZE	CODE	NUMBER	REV.
C	UA	H329-Ø-Ø	A

DIST.

FIRST USED ON OPTION/MODEL: M7957

REVISIONS

CHK	CHANGE NO.	REV.
	H329-00001	A

13 Oct. 77

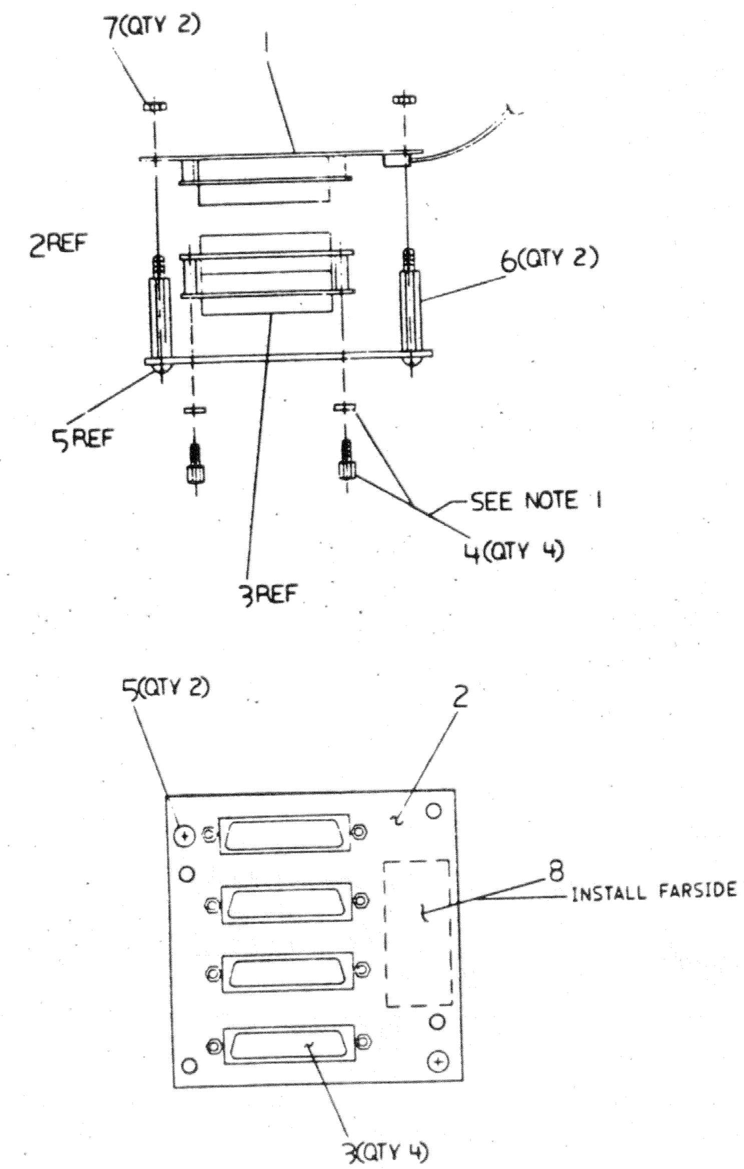
W SMITH

DEC FORM NO. DEC 111-A

97

NOTES:

1. ITEM 4: DISCARD "NUTS" AND "FLAT WASHERS" THAT ARE SUPPLIED WITH THE PACKAGE.



CAUTION: OFF SHEET PARTS LIST
REFER TO K-PL-7018219-0-0

DESCRIPTION	DWG./PART NO.	ITEM NO.
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES		

ANGLES ±0° 30'	CLASS OF ACCURACY (CHECK ONE)	OVER 0 TO 0.2	OVER 0.2 TO 1.2	OVER 1.2 TO 4.8	OVER 4.8 TO 12.0	OVER 12.0 TO 40.0	OVER 40.0 TO 83.0
SURFACE QUALITY IN MICROINCHES	MEDIUM	±.004	±.008	±.012	±.016	±.024	±.04
	PREFERRED	±.012	±.016	±.025	±.04	±.063	±0.1

QUANTITY & VARIATION

THIRD ANGLE PROJECTION

REMOVE BURRS AND BREAK SHARP CORNERS

DO NOT SCALE DWG

MATERIAL: SEE PARTS LIST

FINISH: —

DRN [illegible] FEB 81
CHK [illegible]
ENG. [illegible]
PROJ. ENG. [illegible]
PROD. [illegible]

NEXT HIGHER ASSY.

SCALE: NONE

SHEET OF

FIRST USED ON: DZV11

digital

TITLE: DZV11 DISTRIBUTION ASSY

SIZE	CODE	NUMBER	REV.
D	AD	7018219-0-0	A

DIST

MK

REVISIONS			
CHR.	CHANGE NO.	ORIGINATED	REV. A

AUTOMATED BY PRTLST.3P(44)

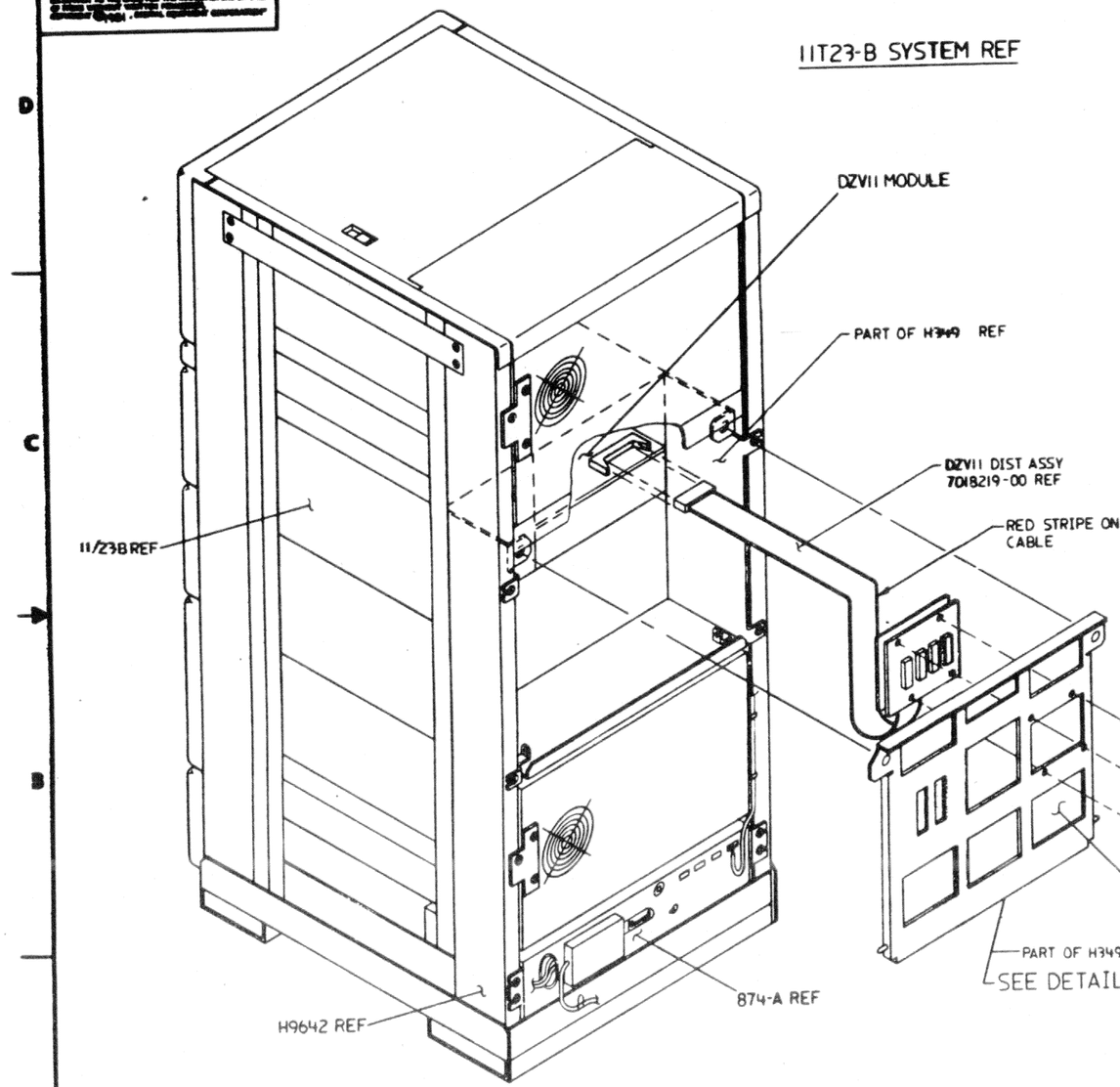
P A R T S L I S T

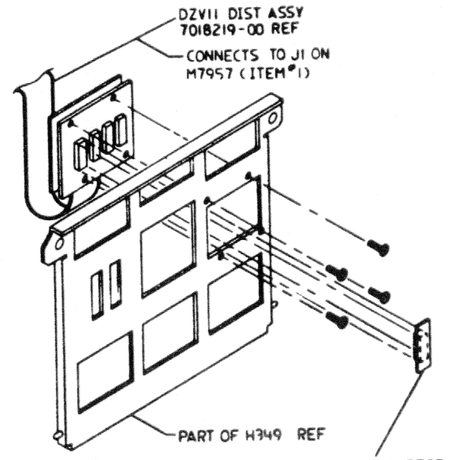
LINE	ITEM	DOCUMENT NUMBER	PART NUMBER	DESCRIPTION	QUANTITY PER VARIATION 00
1	1	D-IA-7018203-0-0	7018203-00	DZV11 DIST CABLE ASSY	1
2	2	C-MD-7423235-0-0	7423235-00	PLATE,MTG DISTB.PANEL	1
3	3		1217431-01	CONN,D SUB 25PIN ASSY STRAIGHT W	4
4	4		9008451-00	SCREW LOCK,ASSY	4
5	5		9009701-00	SCREW,FAN,PHIL,SEMS 6-32X .312L	2
6	6		9000001-05	STANDOFF,HEX,M/F 6-32X 1	2
7	7		9008185-00	NUT,KEP 6-32X 1/4 AF	2
8	8		9009255-00	LABEL, POWER SUPPLY, 2-15/16 " L	1

REVISION HISTORY			BASIC PART NO: 7018219												
ENG	ECO NUMBER	REV	SECTION A OF A	DRN: M.DUGGAN	DATE: 13-MAY-81	DBP	D	I	G	I	T	A	L		
	INITIAL	A	SECTION. VARIATION INDEX [A] 00	CHK'D: J FALKOWSKI	DATE: 24-AUG-81	TITLE: PARTS LIST DZV11 DISTRIBUTION ASSY									
			[B]	DES.ENG.: J STANLEY	DATE: 24-AUG-81										
			[C]	RESP.ENG.: J STANLEY	DATE: 24-AUG-81	DOCUMENT NUMBER									
			[D]			SIZE: K	CODE: PL	NUMBER: 7018219-0-0						REV: A	
			[E]	MFG.ENG.: J DOUGHERTY	DATE: 24-AUG-81										
			[F]	ASSEMBLY NUMBER: D-AD-7018219-0-0	TOP DOCUMENT NUMBER:	FILE NAME: MK0429.PLS								EDIT #: 6	

MK

11T23-B SYSTEM REF





DETAIL "A"
(VARIATION-C)

DRN	
CHK'D	
ENGR	
PROJ. ENGR	
PROD.	
NEXT HIGHER ASSY.	B-DD-DZV11-0
SCALE	NONE
SHEET	OF
FIRST USED ON	DZV11
TITLE	DZV11-C INSTALLATION ARRANGEMENT
SIZE	D
CODE	AR
NUMBER	DZV11-0-4
REV.	A