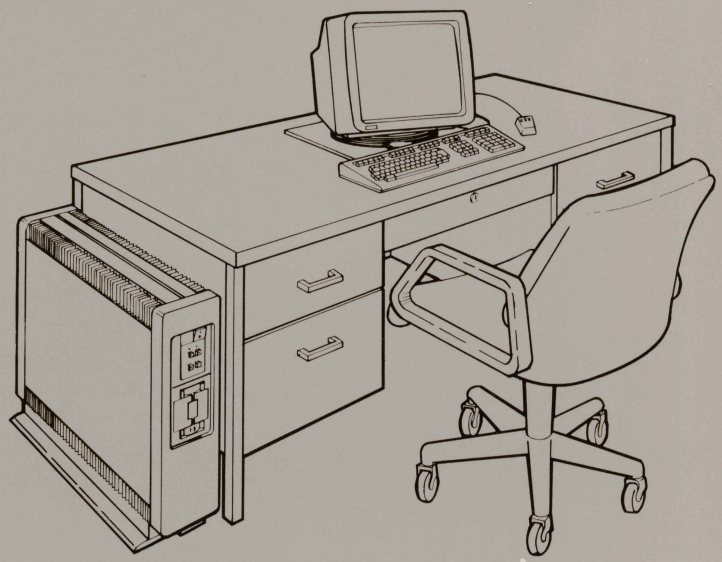
AZ-GLFAB-MN

# VAXstation II

## Technical Manual, BA23 Enclosure



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Technical Manual

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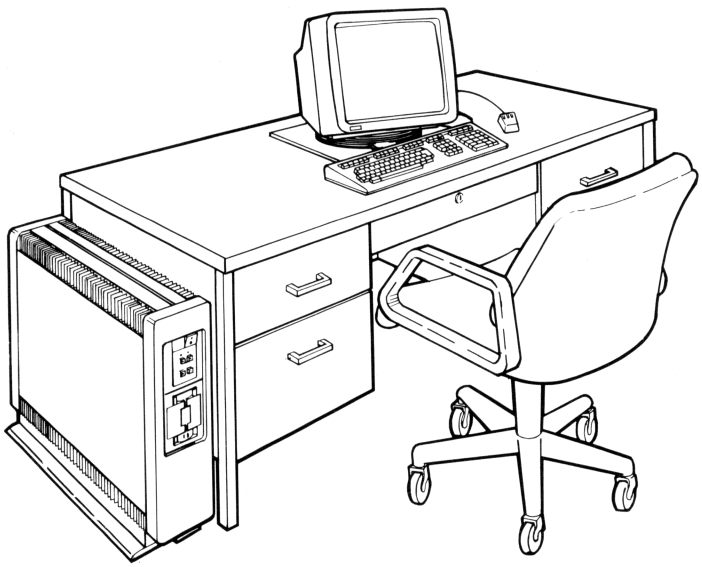

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VAXELN
VAXstation
VMS
VT
Work Processor

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# Preface

## INTRODUCTION

The VAXstation II is a single-user workstation based on the MicroVAX II processor. It contains the VCB01 single-plane bit-mapped video subsystem, an RQDX2 mass storage subsystem, and the MicroVMS operating system. A technical/graphics workstation is formed with the addition of the VR260 monitor, an LK201-AA keyboard, and a VS10X-EA mouse. The workstation can be used as a stand-alone system, or, using the optional DEQNA Ethernet controller, in a clustered environment of print servers, disk servers, and other workstations.

This manual describes the VAXstation II base system, its service procedures, and configuration of options. The manual is meant as a reference tool for Digital's Field Service engineers trained to maintain the VAXstation II system.

- Chapter 1, System Introduction – Describes and lists the general and physical characteristics of the base system.
- Chapter 2, System Description – Describes the major functional components of the base system, and includes information about addresses, switches, and indicators.
- Chapter 3, Options – Describes the optional modules that can be installed to extend the base system's capabilities, and includes information about the addresses, switches, and indicators of the options.
- Chapter 4, Configuration – Describes configuration rules, and switch and jumper settings.
- Chapter 5, Diagnostics – Describes the MicroVAX Maintenance System (MMS) and error reporting, and includes basic troubleshooting guidelines.
- Chapter 6, FRU Removal and Replacement – Describes FRU removal and replacement procedures.
- Appendix A, Console Commands – Describes the command line processor, and lists and describes the available commands, giving their proper syntax.

- Appendix B, Console Error Messages and Explanations – Lists and describes the error messages generated by the command line processor.
- Appendix C, VCB01 Video Controller Module – Describes the module's architecture and provides register and programming information.

## CONVENTIONS USED IN THIS MANUAL

| | |
|---|---|
| NOTE | Contains general information. |
| CAUTION | Contains information to prevent damage to equipment. |
| WARNING | Contains information to prevent personal injury. |
| <mm:nn> | Read as "mm through nn." This use of angle brackets and the colon indicates a bit field or a set of lines or signals. For example, A<17:00> is the mnemonic for Unibus address lines "A17 through A00." |
| <RETURN> | A label enclosed by angle brackets represents a control or special character key on the keyboard (in this case, the Return key). |
| <CTRL>C | Control sequence. Press the special function key <CTRL> and the standard key C at the same time. |

# System Introduction 1

## 1.1 INTRODUCTION

This chapter describes the general and physical characteristics of the VAXstation II. The major physical units are:

1. System enclosure
2. Graphics subsystem I/O devices.

Mounted in the BA23 system enclosure, the VAXstation II has two basic configurations which differ only in mass storage devices. (Table 1-1)

**Table 1-1 VAXstation II Configurations**

| Configuration | Component | Description |
|---|---|---|
| 1 and 2 | KA630-AA | MicroVAX II CPU with 1-Mbyte local (on-board) memory, boot/diagnostic ROM, floating point processor, console SLU (serial line unit), interval timer, and Q22-Bus map. |
| 1 and 2 | MS630-AA | 1-Mbyte memory expansion module, dual-height, with 256 K chips. |
| 1 and 2 | VCB01-KP | VCB01 bit-map video controller with interface for:<br>• LK201 keyboard<br>• VS10X-EA mouse<br>• VS10X-XX tablet. |
| 1 and 2<br><br>1<br>1<br>2 | RQDX2 | Disk controller, supporting MSCP (mass storage control protocol) for:<br>• RD52 31-Mbyte fixed disk drive<br>• RX50 818-Kbyte dual diskette drive<br>• RD53 71-Mbyte fixed disk drive. |

**Table 1-1 VAXstation II Configurations (Cont.)**

| Configuration | Component | Description |
|---|---|---|
| 2 | TQK50 | 95-Mbyte streaming tape subsystem, including tape drive and controller supporting TMSCP (tape mass storage control protocol). |
| 1 and 2 | BA23-A | System enclosure. |

## 1.2 SYSTEM COMPONENTS

Several major components make up the VAXstation II. (Figure 1-1) These are the BA23 enclosure, which houses either an RD52 fixed disk drive and RX50 diskette drive, or an RD53 fixed disk drive and TK50 tape drive, depending on the particular system configuration. Also included within the BA23 enclosure are the system controls and indicators, backplane, power supply, and I/O distribution panel.

The VAXstation II graphics subsystem consists of a VR260 monochrome monitor, LK201 keyboard, VCB01 video controller, and the VS10X mouse. An optional graphics tablet that uses either a hand-held puck or stylus may be used in place of the mouse.

The VCB01 video controller is a quad-height module (part number M7602-YA) that provides a mouse interface, keyboard interface, and cursor controls for creating displays on the VR260 monitor.

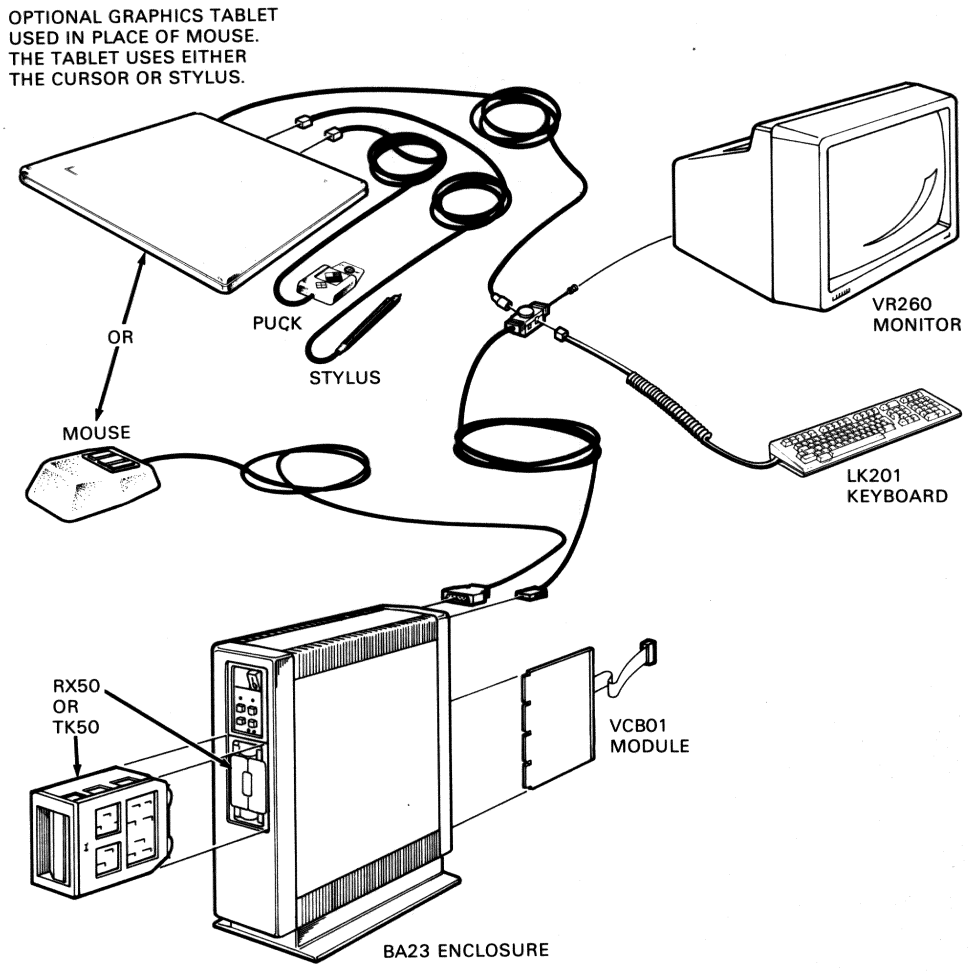



Figure 1-1 VAXstation II System Components

## 1.3 SYSTEM ENCLOSURE

The BA23 enclosure (Figure 1-2) contains the MicroVAX II CPU, the VCB01 video controller, mass storage devices, and options. The air-cooled enclosure operates in an open office environment and includes the following major subassemblies.

- Frame
- Control panel
- Mass storage area
- Backplane assembly
- Power supply and fans
- I/O (input/output) distribution panel

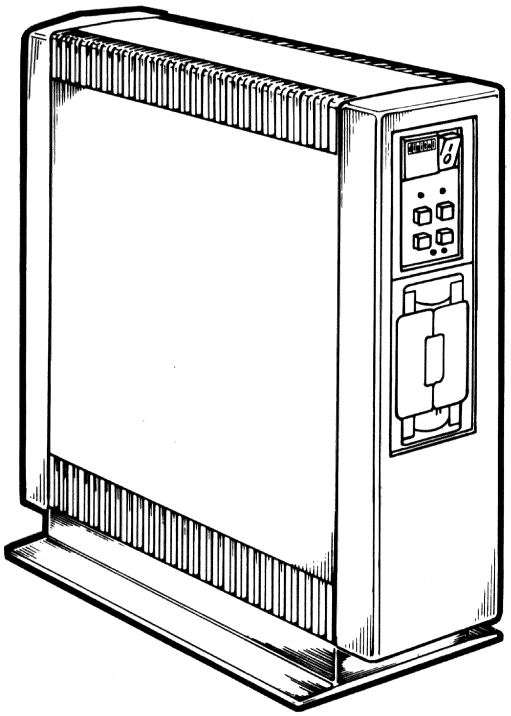


Figure 1-2 BA23 Enclosure

### 1.3.1 BA23-A Frame

The BA23-A frame mounts in either a rack or floorstand. The floorstand converts to tabletop use. Table 1-2 lists the dimensions and weights of the various configurations.

**Table 1-2 BA23-A Dimensions and Weights**

| | Floorstand | Tabletop | Rackmount |
|---|---|---|---|
| Height | 64.2 cm (24.5 in) | 17.7 cm (7.0 in) | 13.3 cm (5.2 in) |
| Width | 25.4 cm (10.0 in) | 56.2 cm (22.13 in) | 48.25 cm (19.0 in) |
| Depth | 72.6 cm (28.6 in) | 72.6 cm (28.6 in) | 64.3 cm (25.3 in) |
| Weight | 31.75 kg (70.0 lb) | 29.5 kg (65.0 lb) | 24.0 kg (53.0 lb) |

The BA23-A frame contains the power supply and the backplane assembly, and includes space for two 13.3 cm (5.25 in) mass storage devices. (Figure 1-3)

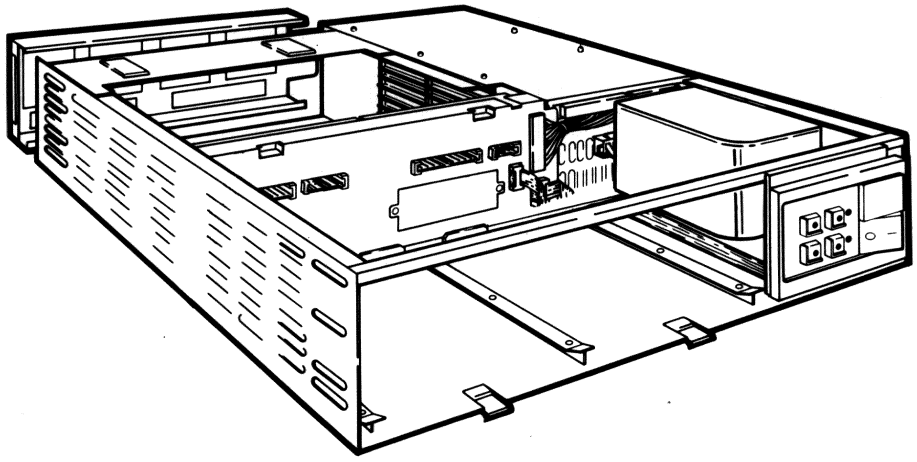


Figure 1-3 BA23-A Frame

A removable bezel covers the front of the BA23-A frame. The floorstand and tabletop models also have a removable rear bezel. (Figure 1-4)

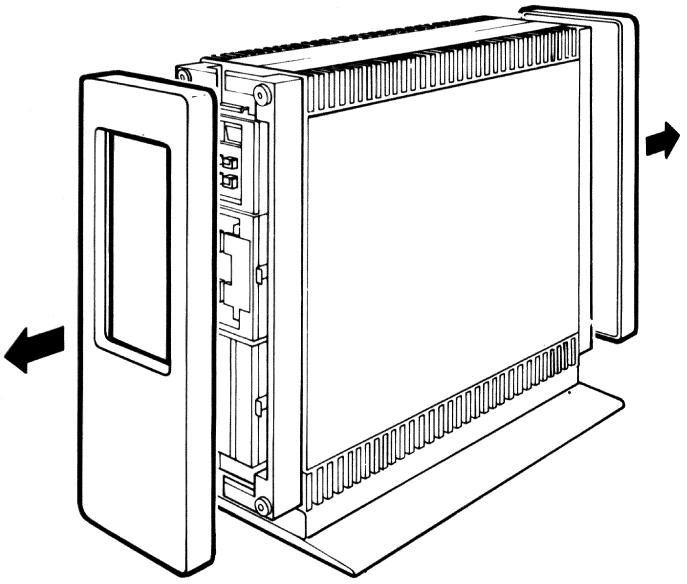


Figure 1-4 BA23 Removable Bezels

**1.3.1.1 Air Circulation –** Two fans in the BA23-A frame draw air from the bottom of the enclosure. (Figure 1-5) One fan is above the control panel, the other above the power supply.

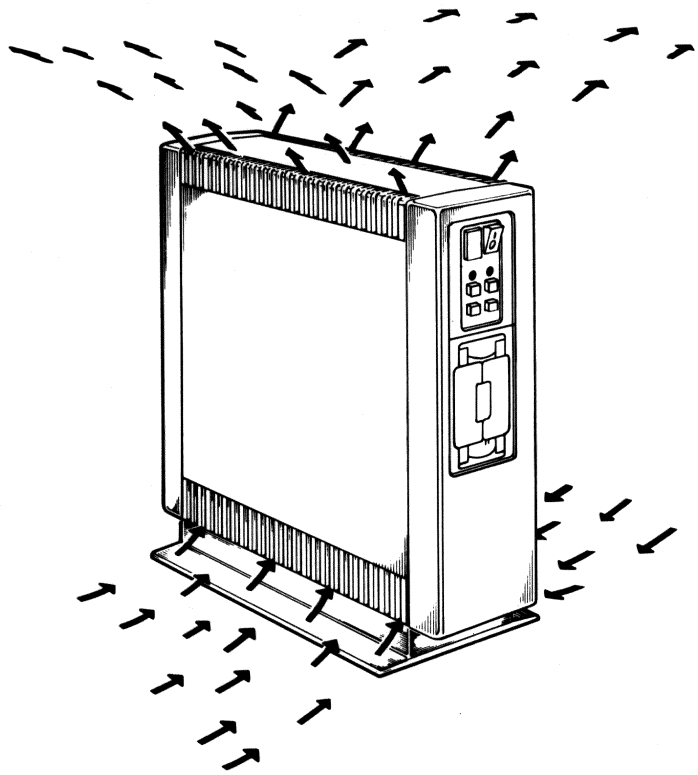


Figure 1-5 Airflow

### 1.3.2 Front Control Panel

The front control panel of the enclosure contains the system controls and indicators (Figure 1-6); Table 1-3 describes their functions.

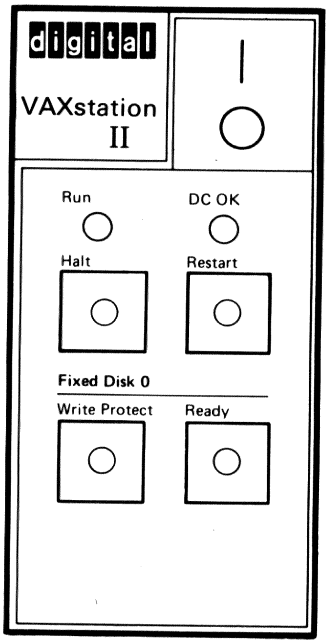



Figure 1-6 BA23 Front Control Panel

**Table 1-3 Front Panel Controls and Indicators**

| Control/ Indicator | Position/ Indication | Description |
|---|---|---|
| 1/0 (Power) | 1 (one) ON | Rocker switch with integral red indicator – Lights when system ac power is ON. |
| | 0 (zero) OFF | System ac power is OFF. |
| DC OK | ON | Green LED – Lights when all dc voltages are present and within tolerance. |
| | OFF | The Q22-Bus BDCOK (bus dc power is OK) signal is negated. |
| Run | ON | Green LED – Lights when the CPU is executing in run mode. |
| | OFF | The CPU is executing in console mode. |

**Table 1-3 Front Panel Controls and Indicators (Cont.)**

| Control/ Indicator | Position/ Indication | Description |
|---|---|---|
| Halt | OUT<br>LED OFF | Push-on/push-off switch with integral red LED – Normal position for running user software. |
| | IN<br>LED ON | Stops normal software operation – Puts the CPU in console mode; the system accepts only console commands. (See Appendix A.) |
| | | NOTE: When it is in the disable position, the Halt Enable switch overrides the Halt switch. |
| Restart | | Momentary-contact switch – When enabled and pressed, causes a simulated power down/up sequence to restart CPU operation. |
| | | NOTE: When it is in the disable position, the Restart Enable switch overrides the Restart switch. |
| Fixed Disk 0 Write-Protect | OUT<br>LED OFF | Normal operation – Push-on/push-off switch with integral yellow LED; enables disk read and write operations. |
| | IN<br>LED ON | Data can be read from, but not written to the disk. |
| Fixed Disk 0 Ready | OUT<br>LED ON | Normal operation – Enables disk reads and writes. |
| | IN<br>LED OFF | Push-on/push-off switch with integral green LED – Prevents fixed disk read and write operations. |

**1.3.2.1 Control Panel Printed Circuit Board –** The control panel PC (printed circuit) board lies behind the molded plastic front control panel. An LTC (line-time clock) DIP (dual in-line package) switch pair, and +5 Vdc and +12 Vdc test points are on this PC board. The LTC DIP switches labeled 1 and 2 are shown in Figure 1-7.

Switch 1 is the BEVENT Enable switch. When it is ON it enables the Q22-Bus BEVENT timing signal, allowing software to control the LTC.

**NOTE – BEVENT Enable**
**At this time, the KA630 CPU does not use BEVENT timing; the BEVENT Enable switch should be OFF.**

Switch 2 is the Restart Enable switch. When it is ON, it allows the front control panel Restart switch to operate as described in Table 1-3. Setting the Restart Enable switch to OFF disables the front control panel Restart switch.

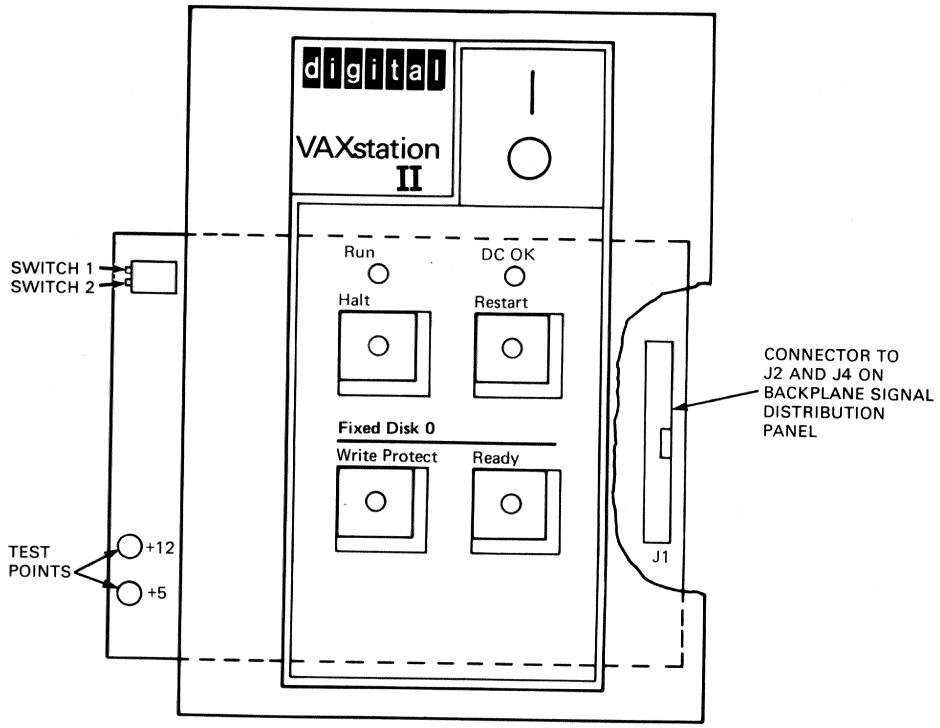



Figure 1-7 Control Panel and PC Board

The PC board also contains the system push-button switches, LEDs, and a 20-pin connector (J1) for the backplane assembly cable. A bracket on the rear of the molded front panel holds the system power ON/OFF switch.

### 1.3.3 Mass Storage

The front bezel covers two slots used for mounting standard 13.3 cm (5.25 in) mass storage devices. The top (or right) slot usually contains a diskette or tape drive. The bottom (or left) slot usually contains a fixed disk drive.

### 1.3.4 Backplane Assembly

The backplane assembly consists of three major parts:

- BA23-A mass storage signal distribution panel (Figure 1-8)
- Sheet-metal mounting bracket
- Q22-Bus backplane.

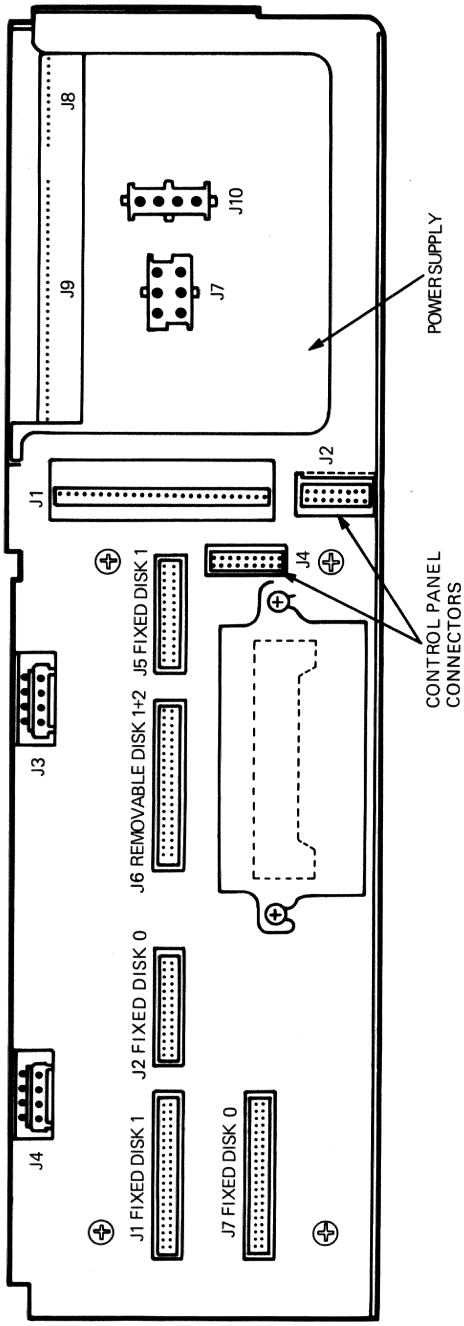



Figure 1-8 Signal Distribution Panel and Power Connections

**1.3.4.1 Mass Storage Signal Distribution Panel –** RX50 diskette and RD5n fixed disk drives installed in the BA23 enclosure connect to the mass storage signal distribution panel. Figure 1-9 shows the internal cabling for the BA23 enclosure.

A TK50 tape drive installed in a BA23 enclosure connects directly to its controller module.

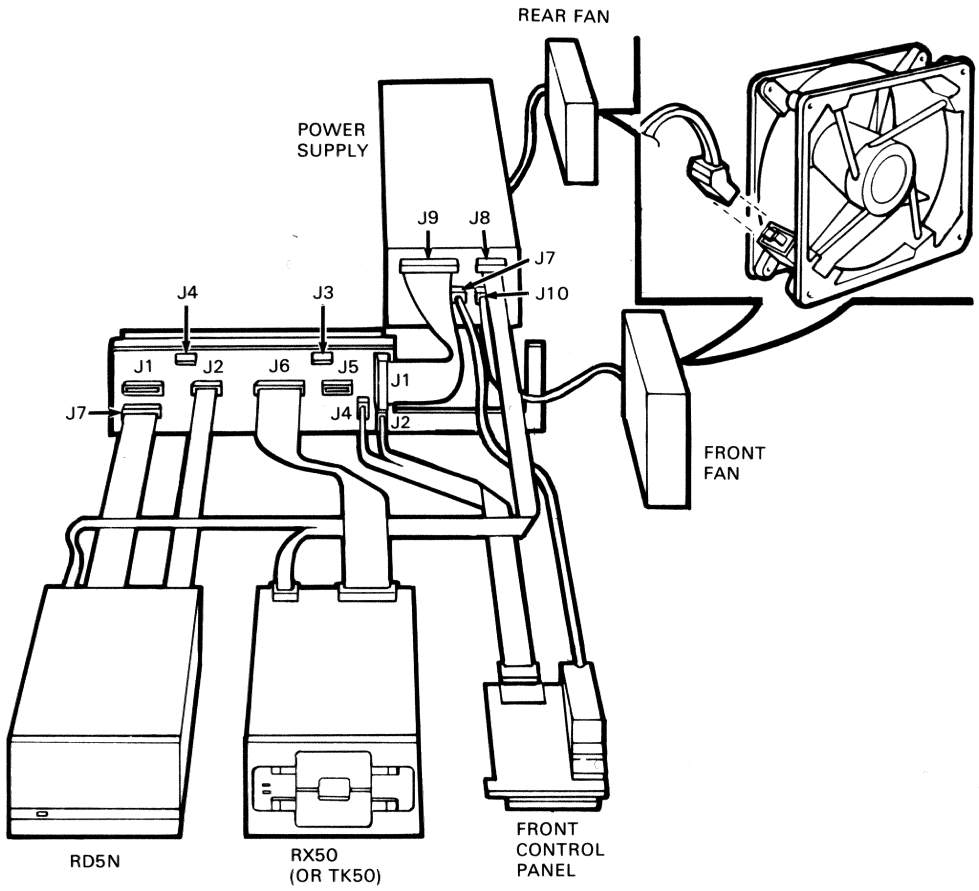



Figure 1-9 Internal Cabling

The signal distribution panel carries the signals from an RQDX controller module installed in the Q22-Bus backplane. Six connectors on the signal distribution panel provide the following.

J7 (Two connectors) Provide the signals to the first fixed disk drive (fixed disk 0)
J2 to be booted. The ROM code commonly labels this drive DU0.

J6 Provides the signals to an RX50 diskette drive. An RX50 diskette drive contains two disk units (removable disk 1 and 2). The ROM code commonly labels these as DU1 and DU2 (disk unit 1 and disk unit 2) when a fixed disk drive (DU0) is present.

J5 Provide the signals to the second fixed disk drive (fixed disk 1) to be booted.
J1 The ROM code commonly labels this drive DU1.

J4 Provides the signals to the control panel PC board from the mass storage signal distribution panel.

**NOTE – Fixed Disk Drive 1**
**At this time, MicroVAX II systems do not support a second fixed disk drive installed in the BA23 enclosure.**

**1.3.4.2 H9278 Backplane –** The backplane supports a maximum of 30 ac loads and 20 dc loads. The ac load is the amount of capacitance a module presents to a bus signal line. One ac load equals 9.35 pF. The dc load is the amount of dc leakage a module presents to a bus signal line. One dc load is approximately 105 $\mu$A. The backplane itself presents seven ac loads and zero dc loads.

Four connectors on backplane side 2 perform the following functions. (Figure 1-10)

J4 Terminate the mass storage power cable when no mass storage device
J3 is installed.

J2 Carries the signals from an installed CPU module to the control panel PC board.

J1 Connects to the power supply backplane cable carrying dc power and power supply signals.

The backplane PC board has four layers:

- 2 signal layers
- 1 ground layer
- 1 power layer.

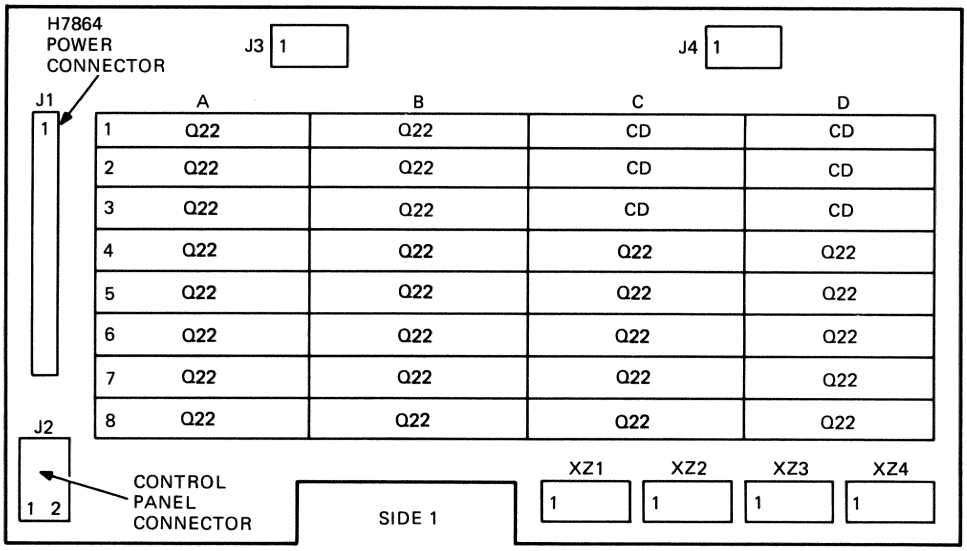
Chapter 4 explains the backplane configuration rules.

The backplane implements the extended LSI-11 Bus, which uses 22-bit addressing. This bus is commonly called the "Q22-Bus."

The backplane has eight slots for system modules, with four connectors (A, B, C, and D) in each slot. (Figure 1-10) The connectors function in pairs, AB and CD. A dual-height module has two edge-connectors that mate with connectors in pair AB or CD. Two dual-height modules can occupy one backplane slot.

A quad-height module has four edge-connectors that mate with both pairs AB and CD in a backplane slot. One quad-height module occupies an entire backplane slot.

Q22-Bus signals are carried by connector pair AB in slots 1 through 8, and connector pair CD in slots 4 through 8. In slots 1, 2, and 3, pair CD are called the "CD interconnect."




NOTES:
1. CONNECTORS J1, J2, J3, AND J4 ARE MOUNTED ON SIDE 2.
2. XZ1—4 ARE BACKPLANE TERMINATOR SOCKETS. THE SIP TERMINATION RESISTORS MOUNTED IN XZ1—4 MUST BE REMOVED WHEN EXPANDING BEYOND THIS BACKPLANE.
3. J3 AND J4 ARE NOT POWER SOURCES. THEY ARE USED TO SUPPLY POWER TO THE BACKPLANE WHEN THE RD51-A FIXED DISK DRIVE OR RX50-AA DISKETTE DRIVE IS NOT INSTALLED.

Figure 1-10 Backplane Module Slots

The CD interconnect carries signals between slots 1, 2, and 3, but not Q22-Bus signals. Only modules conforming to the CD interconnect specification should be installed in the CD position. Slot 1 is used by the CPU module. Any dual-height Q22-Bus module can be installed in the AB position of slots 2 and 3.

**NOTE – Grant Continuity**
**If only one dual-height module is installed in any of the slots 4 through 8, the configuration may require an M9047 grant card in the empty half of the slot.**

### 1.3.5 Power Supply and Fans

The power supply (Figure 1-11) includes protection against excessive voltage, excessive current, and temporary fluctuations in the ac supply.

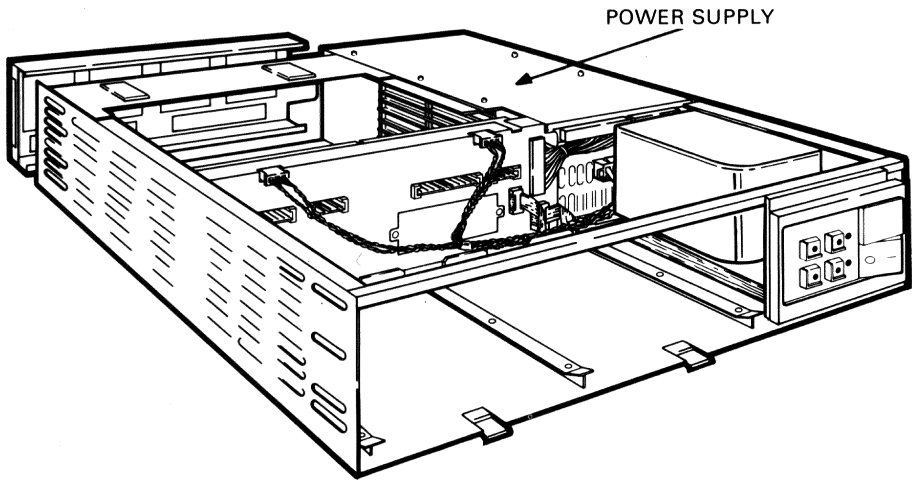



Figure 1-11 Power Supply Location

The 230 W power supply provides +5 Vdc at 4.5 to 36.0 A and +12 Vdc at 0.0 to 7.0 A to the:

- Backplane
- Fixed disk drive
- Diskette or tape drive.

The power supply generates system control signals BDCOK H, BPOK H, and BEVENT L to the backplane. When the system power is stable, the power supply asserts BDCOK H and BPOK H. The LTC switch on the control panel PC board enables the BEVENT L, which is an external line clock interrupt request to the CPU.

The power supply includes two +10 Vdc 0.45 A fan outputs for the front and rear dc fans. The fan voltages can be increased to +12 Vdc by changing a power supply jumper; however, the 630QA module thermal and acoustical specifications are based on +10 V. The fan power requirement does not affect the 230 W output specification. Table 1-4 lists the power supply specifications.

**Table 1-4 H7864 Power Supply Specifications**

| Parameter | Specification |
|---|---|
| **+5 Vdc Output** | |
| Voltage | +5.1 Vdc ± 2.5% |
| Current | 36.0 A max.<br>4.5 A min. |
| Overcurrent | 37.0 A min. (averaged over 1 ms – must not trip)<br>42.0 A max. (averaged over 1 ms – must trip) |
| Ripple and Noise | 50.0 mV peak-to-peak max. |
| **+12 Vdc Output** | |
| Voltage | +12.1 Vdc ± 2.5% |
| Current | 7.0 A max.<br>0.0 A min. |
| Normal Overcurrent | 7.2 A min. (averaged over 1 s – must not trip)<br>8.0 A max. (averaged over 1 s – must trip) |
| Startup Overcurrent | 9.0 A for 10 s min. (must not trip)<br>10.0 A for 5 s min. (must not trip)<br>11.5 A for 1 s min. (must not trip)<br>13.0 A for 500 μs (must trip) |
| Ripple and Noise | 75.0 mV peak-to-peak max. |

A remote power control connector is located at the rear of the power supply. (Figure 1-12) An ac input connector provides compatibility with international line cords. A circuit breaker protects the input power line. The voltage select (VOLT SEL) switch selects one of two ranges:

| **Position** | **Range** |
|---|---|
| 120 V | 88 – 128 Vac |
| 240 V | 176 – 256 Vac |

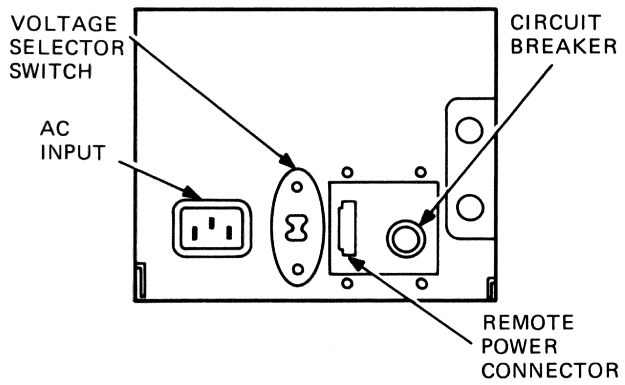



Figure 1-12 Power Supply, Rear View

The rear fan power cable is an integral part of the H7864 power supply.

At its front the power supply has four connectors. (Figure 1-8)

J10 Provides front fan power.

J9 Provides backplane power. The backplane power cable terminates in backplane connector J1.

J8 Provides the mass storage power cable signals. The mass storage power cable is terminated in backplane connector:

- J4 if an RD52 fixed disk drive is not installed, and
- J3 if an RX50 diskette drive is not installed.

J7 Provides front control panel power.

### 1.3.6 Rear I/O Distribution Panel

External devices connect to the system through the rear I/O distribution panel of the BA23 enclosure.

Each module that connects to an external device comes with an internal cable, a filter connector, and an insert panel. Together, these three items are referred to as a cabinet kit. Chapter 3 provides cabinet kit information for modules that support external devices.

The filter connectors mount in the insert panels. The insert panels install in cutouts in the rear I/O distribution panel. The BA23 rear I/O distribution panel accepts up to six insert panels, two of which can be 50-pin connector insert panels.

Figure 1-13 shows the rear I/O distribution panel with the CPU module's SLU display insert panel installed. The SLU insert is usually installed in the top (or left) cutout.

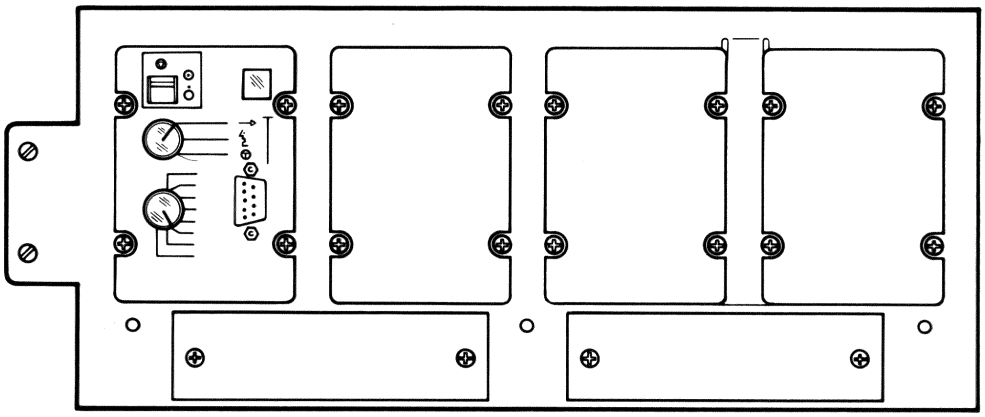


Figure 1-13 Rear I/O Distribution Panel

The dimensions of the rear I/O distribution panel cutouts are:

- Two type A: 1.6 × 8.1 cm (0.6 × 3.2 in)
- Four type B: 6.2 × 8.1 cm (2.5 × 3.2 in).

Dimensions of the corresponding insert panels are:

- Type A: 2.5 × 10.1 cm (1.0 × 4.0 in)
- Type B: 6.6 × 8.2 cm (2.6 × 3.2 in).

In addition, a removable bracket between the third and fourth cutouts allows three more type A insert panels to be installed with an adapter plate. Figure 1-14 shows typical type A and type B insert panels, and the adapter plate.

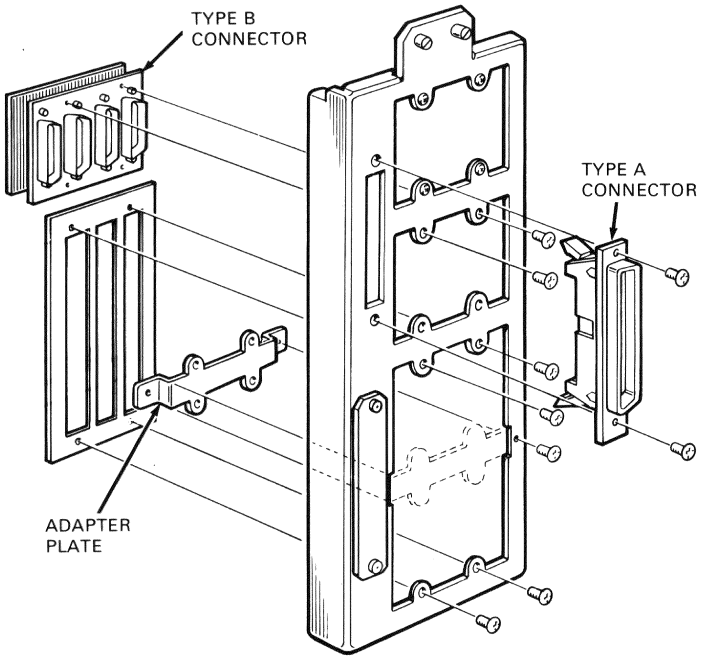



Figure 1-14 I/O Insert Panels and Adapter Plate

## 1.4 GRAPHICS SUBSYSTEM

The major physical units of the graphics subsystem are:

- Monitor
- Keyboard
- Mouse.

### 1.4.1 VR260 Monitor

The VR260 is a 48 cm (19 in) diagonal, non-interlaced, 60 MHz, input bandwidth, monochrome monitor. (Figure 1-15) It can display graphics and text with a resolution of 1024 × 864 pixels (horizontal × vertical). It has a horizontal scan rate of 54 kHz and a 60 Hz refresh rate. Table 1-5 lists the monitor's physical and electrical specifications.

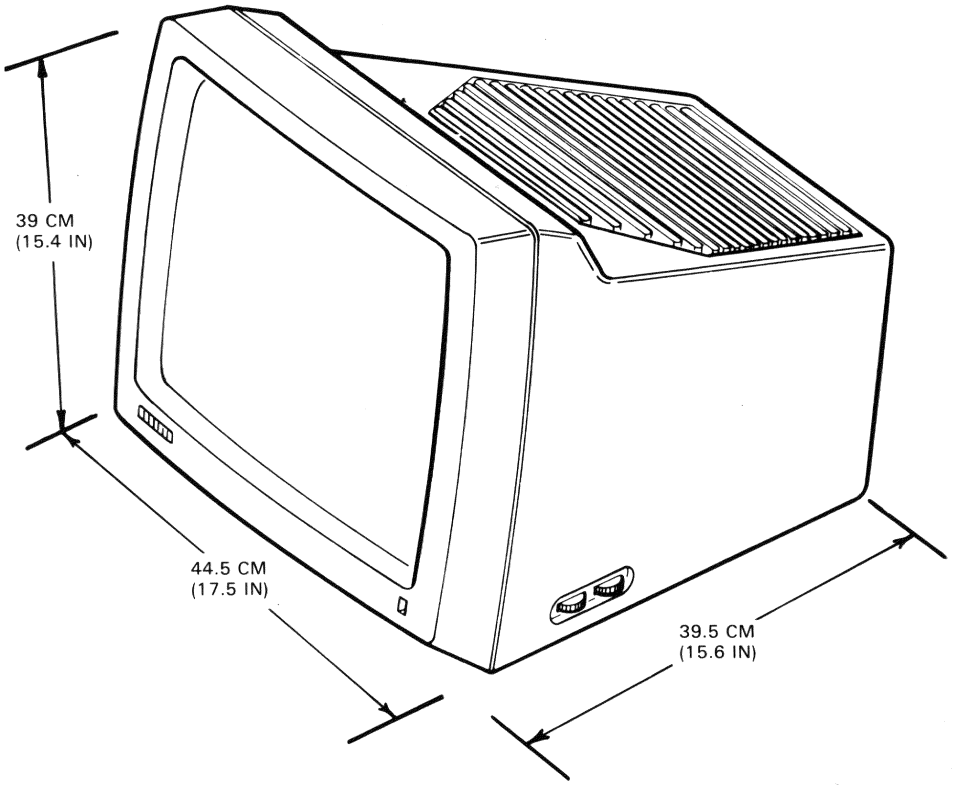



Figure 1-15 VR260 Monitor

**Table 1-5 VR260 Monitor Physical and Electrical Specifications**

| | |
|---|---|
| Height | 38.10 cm (15.00 in) |
| Width | 45.72 cm (18.00 in) |
| Depth | 40.64 cm (16.00 in) |

**Table 1-5 VR260 Monitor Physical and Electrical Specifications (Cont.)**

| | |
|---|---|
| Weight | 20.50 kg (45.00 lb) |
| Viewable Area | 1024 × 864 pixels |
| AC Power Requirement | 120 Vac at 1.0 A<br>240 Vac at 0.6 A |

### 1.4.2 LK201 Keyboard

The VAXstation II keyboard, LK201-AA, (Figure 1-16) is connected to the VCB01 video controller subsystem through the I/O distribution panel insert and a coiled, 4.78 m (19 ft), cable (BC18P-10). The keyboard's physical and electrical specifications are listed in Table 1-6.

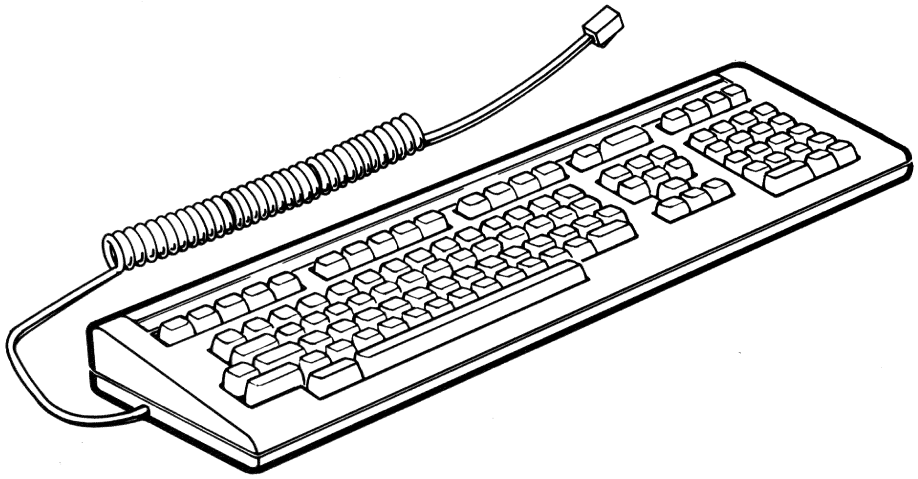


Figure 1-16 LK201 Keyboard

**Table 1-6 LK201-AA Keyboard Physical and Electrical Specifications**

| | |
|---|---|
| Height | 5.10 cm (2.00 in) |
| Width | 53.30 cm (21.00 in) |
| Depth | 17.20 cm (6.75 in) |
| Weight | 2.30 kg (5.00 lb) |
| DC Power Requirement | +12.0 Vdc at 350 mA |

### 1.4.3 VS10X Mouse

The mouse (Figure 1-17) is a hand-held device that moves a pointer displayed on the monitor screen. It is attached to and receives power from the VCB01 subsystem through the I/O distribution panel insert and a 3.7 m (12 ft) cable. The mouse generates relative-position data (quadrature-encoded, X and Y axis), and has three buttons for event signaling. The mouse's physical and electrical specifications are listed in Table 1-7.

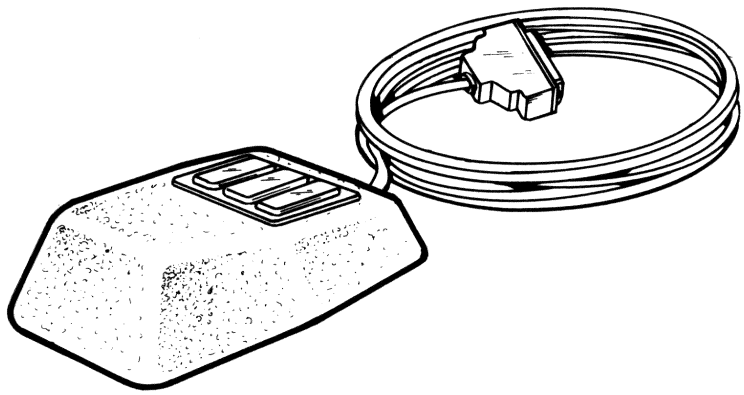


Figure 1-17 VS10X Mouse Device

**Table 1-7 VS10X Mouse Physical and Electrical Specifications**

| | |
|---|---|
| Height | 3.30 cm (1.30 in) |
| Width | 7.00 cm (2.75 in) |
| Length | 9.50 cm (3.75 in) |
| Weight | 0.50 kg (1.10 lb) |
| DC Power Requirement | +5.0 Vdc ± 10% at <150 mA |
| Accuracy | 7.87 pulses/mm (200 pulses/in) |
| Rate of Movement | 25.4 cm/s (10 in/s) or less |

**1.4.3.1 Mouse Connector Pin Assignments –** The mouse uses a 7-pin micro-DIN-type connector. These pins are shown in Figure 1-18. Note that the top of the connector is three pins wide and the bottom is two pins wide. The numbers and names of these pins are listed in Table 1-8.

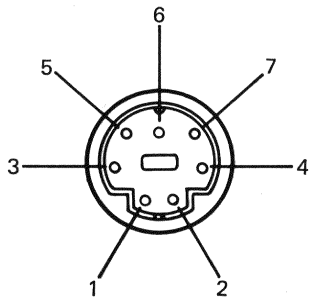



Figure 1-18 Mouse Connector Pin Assignments

**Table 1-8 Mouse Connector Pin Assignments**

| Pin | Name (Function) |
|---|---|
| 1 | GND (Signal ground and return for power) |
| 2 | TXD (Serial out from mouse) |
| 3 | RXD (Serial in to mouse) |
| 4 | GND/–12 V (–12 V for RS-232) |
| 5 | +5 V |
| 6 | Not used |
| 7 | Not used |
| Shell | Protective ground |

# System Description 2

This chapter describes the major functional components of the VAXstation II subsystems:

1. MicroVAX II processor
2. Graphics subsystem
3. Mass storage subsystem.

## 2.1 MicroVAX II PROCESSOR

In the base system, the MicroVAX II processor comprises the KA630 CPU module and an MS630 memory expansion module.

### 2.1.1 KA630-A CPU

The KA630-A CPU includes:

- MicroVAX processor chip, which provides a subset of the VAX instruction set and data types, as well as full VAX memory management.

  VAX data types:

  - Byte, word, longword, quadword
  - Character string
  - Variable-length bit field.
  - The remaining VAX data types are supported through software emulation.

  VAX instruction set:

  - Integer and variable
  - Address
  - Variable-length bit field

  - Control and procedure call
  - Queue
  - MOVC3/MOVC5.
  - The remaining VAX instructions, including floating point for the KA630-AB version, are supported through software emulation.
- 1 Mbyte of on-board memory, with support for one or two MS630 memory modules.
- Support for up to 4 Gbytes ($2^{32}$) of virtual memory.
- Console SLU with externally selectable baud rate. The console SLU is accessed using four VAX IPRs (internal processor registers).
- Interval timer, with 10 ms interrupts. Interrupts are enabled via an IPR.
- 64-Kbyte boot/diagnostic ROM, which provides:
  - A subset of the VAX console program
  - Power-up diagnostics
  - Boot programs for standard devices.
- Q22-Bus map/interface, provides DMA (direct memory access) for all local memory. The KA630-A processes Q22-Bus interrupt request levels BR7 through BR4.

The KA630-A CPU communicates with mass storage and peripheral devices via the Q22-Bus. The KA630-A communicates with MS630 memory modules through a MicroVAX local memory interconnect in the CD rows of backplane slots 1 through 3, and through a cable between the CPU and MS630 memory modules.

The KA630-A CPU module (Figure 2-1) has three connectors:

J1 Connects to an MS630 memory module cable.

J2 Connects to the configuration and display connector cable from the CPU patch panel insert.

J3 Connects to the console SLU connector internal cable from the CPU patch panel insert.

**CAUTION – CPU Slot Position**
**A KA630-A CPU module must be installed only in backplane slot 1, 2, or 3 (all three contain the MicroVAX local memory interconnect). It must not be installed in slots 4 through 8.**

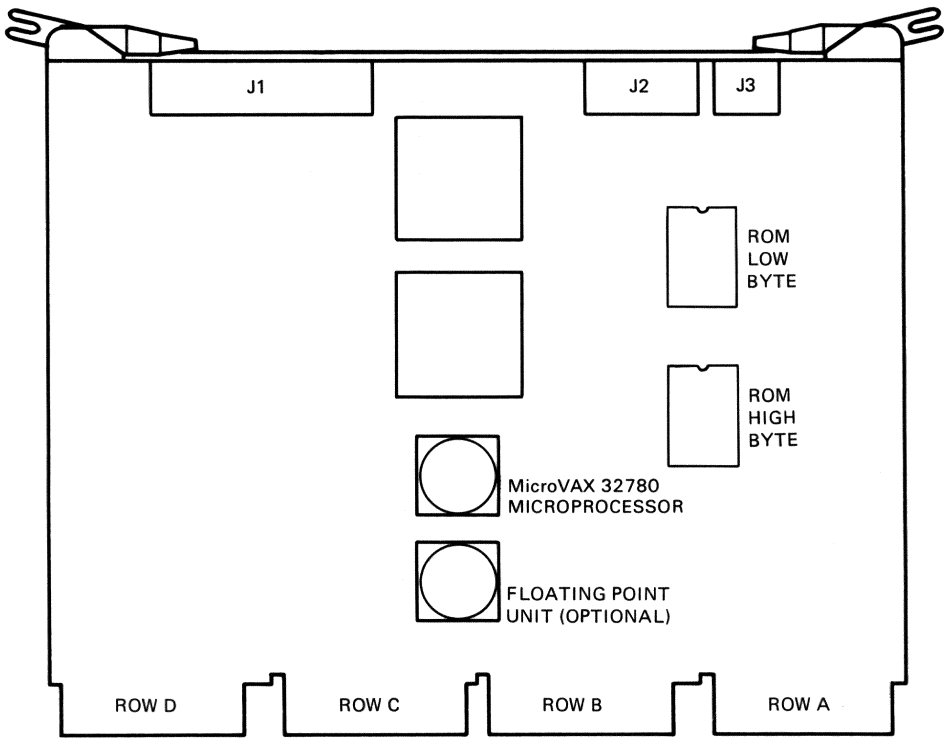



Figure 2-1 KA630-A CPU Module

**2.1.1.1 Console Program –** The console program, resident in two ROM chips on the module, receives control whenever the processor halts. For the KA630-A CPU, a halt means only that processor control has passed to the console program, not that instruction execution stops. The processor halts as a result of:

- System power-up or Restart button pushed
- An external halt signal
- Halt instruction execution
- A system error.

At power-up, the system enters one of three power-up modes. The mode is selected with a switch on the CPU patch panel insert (Paragraph 2.1.2). The console program then determines console device type and console language.

If the console device supports the MCS (multinational character set), the console program can be directed to output the console program in any one of 11 languages. The user language is recorded in battery backed-up RAM (Paragraph 2.1.2), which retains the language selection when the system is turned off.

If the console device does not support the MCS, there is no language prompt, and the console program defaults to English. The message "Performing normal system tests" is displayed. A diagnostic test countdown is displayed on the console terminal, in the CPU patch panel insert segmented-LED display, and in LEDs on the CPU module. These diagnostics test the CPU, memory system, and Q22-Bus interface. The diagnostic test codes and messages are described in Chapter 5.

If a halt has been caused by a condition other than power-up, the console program will branch directly to service the halt. Depending on the type of halt, the console program may branch to diagnostics, a restart sequence, a primary bootstrap routine, or console I/O mode.

If halts are enabled by the switch on the CPU patch panel insert (Paragraph 2.1.2), the console program will enter console I/O mode in response to any halt condition, including system power-up. Console I/O mode allows the user to control the system through the console terminal by use of a console command language (described in Appendix A). The console I/O mode prompt is >>>.

**2.1.1.2 Primary Bootstrap Program (VMB) –** If halts are disabled by the CPU patch panel switch, and the diagnostic tests are completed successfully, the console program will try to bootstrap (load and start) an operating system. The console program first searches for a 64-Kbyte error-free segment of system memory. Next, it copies VMB (the primary bootstrap program) from the console program ROM into the segment at base address +512. The console program then branches to VMB. VMB attempts to bootstrap an operating system from one of the devices listed in Table 2-1, starting at the top.

**Table 2-1 Console Program Boot Sequence**

| Priority | Controller | Type – Designation | Q22-Bus CSR Address |
|---|---|---|---|
| 1 | RQDX<br>RC25<br>KDA | MSCP (Disk) – DUAn<br>– DAAn<br>– DJAn | 17772150 (first)<br>Floating (additional) |
| 2 | TK50 | MSCP (Tape) – MUAn | 17774500 (first)<br>Floating (additional) |
| 3 | MRV11 | PROM – PRAn | Program searches for a valid signature block at 4K boundaries within the Q22-Bus address range. |
| 4 | DEQNA | ETHERNET – XQAn | 17774440 (first)<br>17774460 (additional) |

When VMB determines that a controller is present, it searches in order of increasing unit number for a bootable unit with a removable volume. If it finds none, it will repeat the search for a nonremovable volume.

The system can also be directed to enter VMB through console I/O mode by use of the boot command, followed by the unit designation and number; for example, B DUA0.

When the operating system is booted, the processor no longer executes instructions from the console program ROM. The processor is then in program I/O mode, and terminal interaction is controlled by the operating system.

### 2.1.2 CPU Patch Panel Insert

The CPU patch panel insert (Figure 2-2), mounted in the rear I/O distribution panel, contains:

- 3 switches
- 1 segmented-LED display
- 1 external connector
- 2 internal connectors
- 1 BBU (battery backup unit).

Table 2-2 describes the CPU patch panel insert's switches.

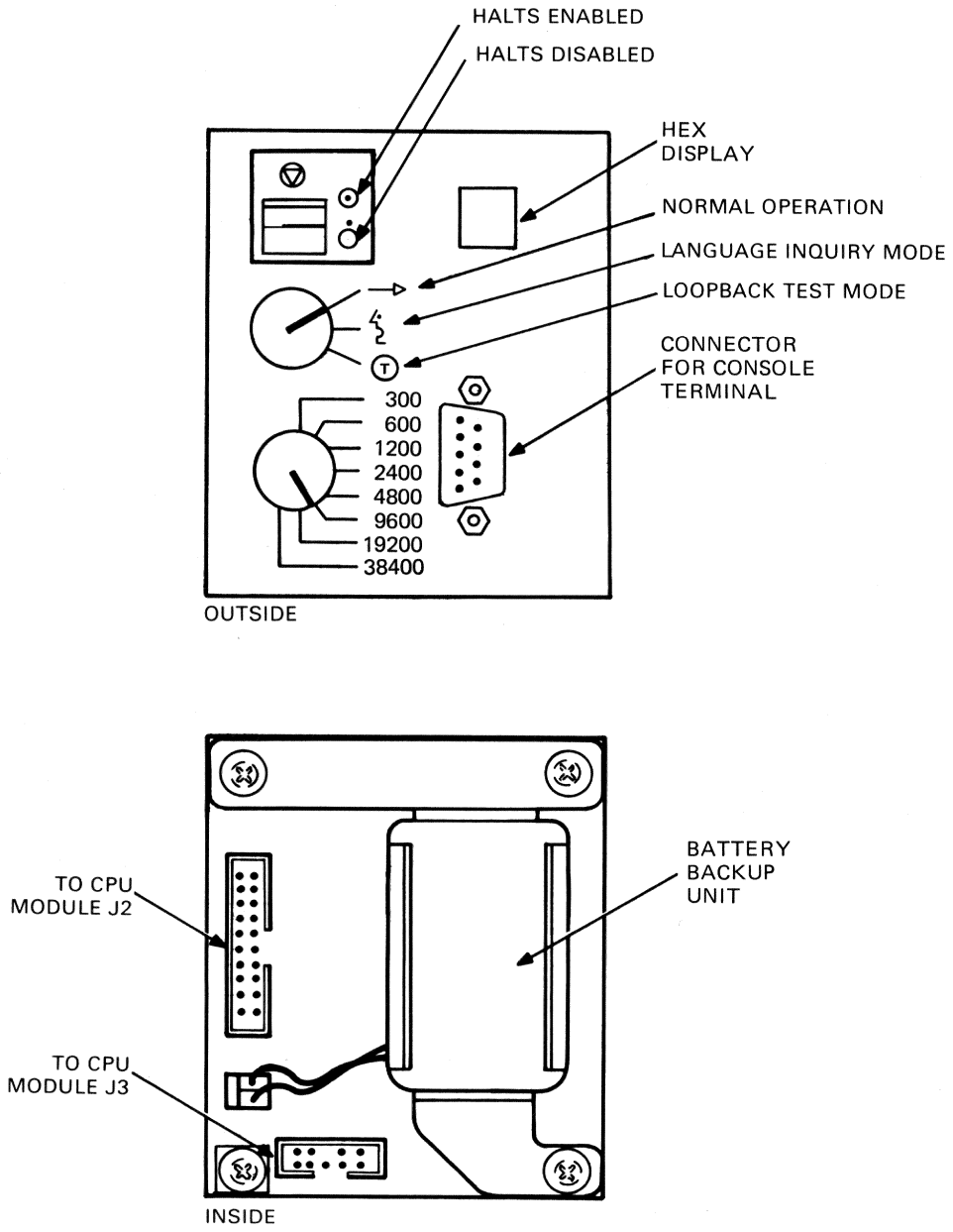



Figure 2-2 CPU Patch Panel Insert

**Table 2-2 CPU Patch Panel Insert Switches**

| Switch | Position | Function |
|---|---|---|
| Halt Enable | Dot | Factory setting; halts are disabled. On power-up or restart, the system will enter VMB at the completion of start-up diagnostics. |
| | Circled dot | Halts are enabled. On power-up or restart, the system will enter console I/O mode at the completion of start-up diagnostics. |
| Power-Up Mode | Arrow | Factory setting; Run. If the console terminal supports MCS, the user will be prompted for language only if the BBU has failed. Full start-up diagnostics are run. |
| | Face | Language Inquiry. If the console terminal supports MCS, the user will be prompted for language on every power-up and restart. Full start-up diagnostics are run. |
| | Circled T | Test. ROM programs run wrap-around SLU tests. |
| Baud Rate | 1 through 8 | Factory-set to 4800 baud. Sets the baud rate of the console terminal serial line. The baud rate selection must match the console terminal's baud rate. |

The segmented-LED displays the number of the currently executing power-up test or bootstrap procedure. If a failure occurs, the number displayed represents the FRU that is the most probable cause of the failure. Test numbers are defined in Chapter 5. The 9-pin external and internal SLU connectors connect the console terminal cable to the cable from connector J3 on the KA630-A CPU module.

The 20-pin internal configuration and display connector connects the three switches and the segmented-LED display to the cable from connector J2 on the KA630-A CPU module.

When system power is off, the BBU (battery backup unit) provides power to the TOY (time-of-year) clock chip on the KA630-A CPU module. The code for the user's language is stored in RAM on the TOY chip, and is lost if the BBU fails.

For more information, refer to the *KA630-A CPU Module User's Guide* (EK-UVAX2-TM).

### 2.1.3 MS630 Memory Module

The MS630 memory module provides memory expansion for the KA630-A CPU module. It is available in three versions (Table 2-3), all populated with 256 K RAMs.

**Table 2-3 MS630 Memory Modules**

| Version | Part Number | Capacity | Height |
|---|---|---|---|
| MS630-AA | M7607-AA | 1 Mbyte | Dual |
| MS630-BA | M7608-AA | 2 Mbyte | Quad |
| MS630-BB | M7608-BA | 4 Mbyte | Quad |

One or two MS630 modules can be used in the VAXstation II. The MS630 modules interface with the KA630-A CPU through the MicroVAX local memory interconnect and an "over-the-top" cable. The MicroVAX local memory interconnect is implemented in the CD rows of backplane slots 1, 2, and 3. The over-the-top cable is connected to J1 on the KA630-A CPU and the corresponding 50-pin connector(s) on the MS630 module(s). There are no hardware settings on the MS630 module.

**CAUTION – MS630 Memory Module Slot Position**
**An MS630-B module must be installed only in backplane slot 2 or 3. It must not be installed in slots 4 through 8. The MS630-AA can be installed only in the CD rows of slots 2 and 3.**

For an overview of module configuration, see Chapter 3, Paragraph 3.1.2.

## 2.2 GRAPHICS SUBSYSTEM

### 2.2.1 VCB01 Video Controller Module

The VCB01 controller kit includes the M7602-YA controller module, an I/O distribution panel insert, and a module-to-insert cable.

The VCB01 is a quad-height, Q22-Bus bit-mapped video option module (Figure 2-3) that provides workstation capability for Q22-Bus systems.

An on-board, 256-Kbyte, MOS RAM bit-map memory (also called video memory) resides in the Q22-Bus address space. In the VAXstation II, a subset of the bit-mapped video memory is displayed on the 48 cm (19 in) VR260 monochrome monitor. This subset is sometimes called screen memory. The VCB01 relies on the CPU to generate all images stored in video memory.

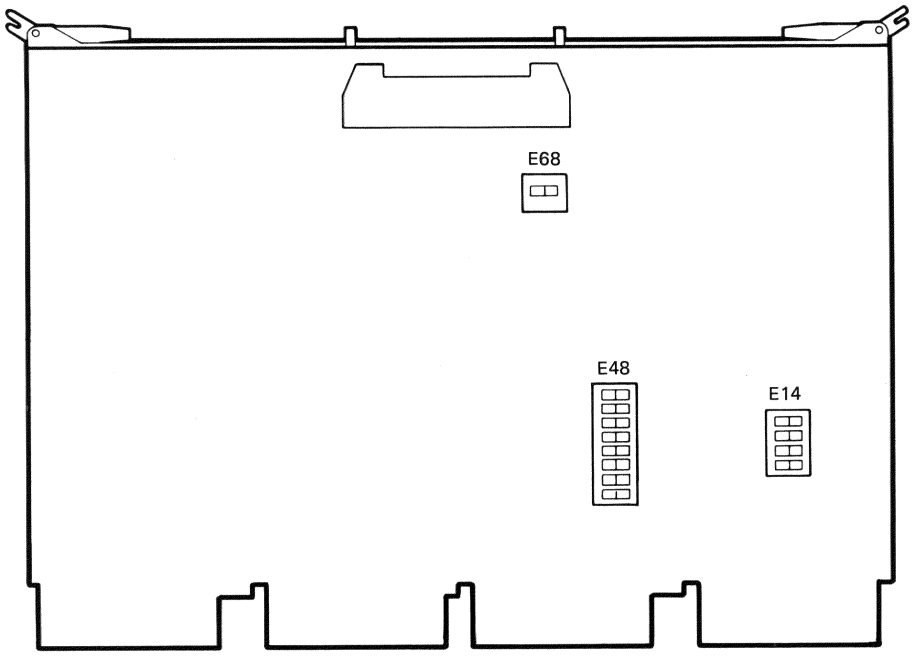



Figure 2-3 VCB01 Video Controller Module

The VCB01 also provides several basic I/O functions, including:

- Cursor controls
- Mouse interface
- Keyboard interface
- Primitives for VT100-style split-screen scrolling.

The VCB01 contains switches to select:

- MSA (memory starting address)
- CSR (control and status register) base address
- Display density.

**2.2.1.1 Memory Starting Address (MSA) –** Switches 1 through 4 of switch-pack E14 select the starting address for the 256-Kbyte block of MicroVAX physical memory where the VCB01 module resides. To take advantage of certain MicroVAX architectural features when programming bit-map operations, the video memory always resides in the topmost 256 Kbytes of the I/O physical address space. Therefore, all the MSA switches are set to OFF; that is, address bits <21:18> select the 256-Kbyte block starting at 3C0000 (hexadecimal). (Note that this is equivalent to address 3FFC0000 in the I/O physical address space. See Paragraph C.2.1.) Refer to Table 2-4.

**Table 2-4 VCB01 MSA Selection**

| Address Bit: | A21 | A20 | A19 | A18 | |
|---|---|---|---|---|---|
| Switch E14: | 1 | 2 | 3 | 4 | |
| Switch Setting:* | 1 | 1 | 1 | 1 | |
| | | _____ | _____ | _____/ | |
| MSA Address: | 1 | | 7 | | 000 000† |

* 0 = off; 1 = on
† <A17:A00> = 0

**2.2.1.2 CSR Base Address –** In the system I/O page, 32 locations are allocated to the VCB01 module. These locations allow the CPU and VCB01 to exchange control and status information through hardware registers on the VCB01. As a group, these registers are called CSRs, but the first register is specifically named the CSR. Switches 1 through 7 of switch-pack E48 correspond to address bits <12:06> and select the base address for these registers. (Table 2-5) In the VAXstation II system, E48 switches S1:S7 are set to 1E80 (hexadecimal). (See Appendix C, Figure C-19.)

**Table 2-5 CSR Base Address Select**

| Address Bit: | A12 | A11 | A10 | A09 | A08 | A07 | A06 | |
|---|---|---|---|---|---|---|---|---|
| Switch E48: | 1 | 2 | 3 | 4 | 5 | 6 | 7 | |
| Switch Setting:* | 1 | 1 | 1 | 1 | 0 | 1 | 0 | |
| | | _____ | _____ | _____/ | _____ | _____ | _____/ | |
| CSR Address: | 1777 | | 7 | | | 2 | | 00† |

* 0 = off; 1 = on
† <A05:A00> = 0

**2.2.1.3 Display Density –** The VCB01 module can drive either full-page or half-page monitors, as selected by switch E68 and switch S8, respectively, of switch-pack E48. The VR260 monitor used in the VAXstation II system is a full-page monitor, and is selected as shown in Table 2-6. Half-page monitors are not supported.

**Table 2-6 VR260 Monitor Display Density Selection**

| |
|---|
| E68 = On (C2) |
| E48/S8 = Off |

For more detailed information on the VCB01 video controller module see Appendix C.

### 2.2.2 VR260 Monitor

The VR260 monitor has three external controls (on/off, contrast, and brightness) and one indicator (power-on LED). Internal alignment controls and adjustments are described in Chapter 6.

The monitor has a self-contained power supply and its own ac power cord. It is connected to the system via the VCB01 I/O panel insert by the BC18P-10 cable. The keyboard and data pad are connected at the monitor end of this cable.

### 2.2.3 LK201 Keyboard

The LK201 keyboard is driven by a microprocessor and contains a set of microdiagnostics. Communication between the keyboard and the VCB01 module is full-duplex, serial/asynchronous at 4800 baud, and conforms to EIA standard RS423. The keyboard lead is terminated in a 4-pin modular connector that plugs into the monitor end of the BC18P-10 video cable.

### 2.2.4 VS10X Mouse

The hand-held VS10X mouse controls the pointer image (icon) on the monitor screen. It provides relative pointer position to the VCB01 in the form of X-coordinate and Y-coordinate pulse outputs. Three push buttons on the mouse perform software-defined functions. The mouse is connected to the VCB01 I/O panel insert with a 3.7 m (12 ft) 10-conductor cable.

## 2.3 MASS STORAGE SUBSYSTEM

The base system's mass storage subsystem can be configured differently from that shown in Table 1-1. For an overview of ordering information and module configuration see Chapter 3.

### 2.3.1 RQDX2 Disk Controller

Order: RQDX2-AA
Controller kit includes:

- RQDX2 M8639-YB controller module
- 17-00285-02 50-pin signal cable

For more information, refer to the *RQDX2 Controller Module User's Guide* (EK-RQDX2-UG).

The quad-height RQDX2 controller module provides the interface between the Q22-Bus and the fixed disk and diskette drives. It is an intelligent controller with on-board microprocessors. Data is transferred using DMA; control and status communication between the host and controller uses MSCP (mass storage control protocol).

The RQDX2 can control up to four drives. Each fixed disk drive counts as one drive; each RX50 dual diskette drive counts as two.

Figure 2-4 shows the jumper and LED locations for the RQDX2 controller module.

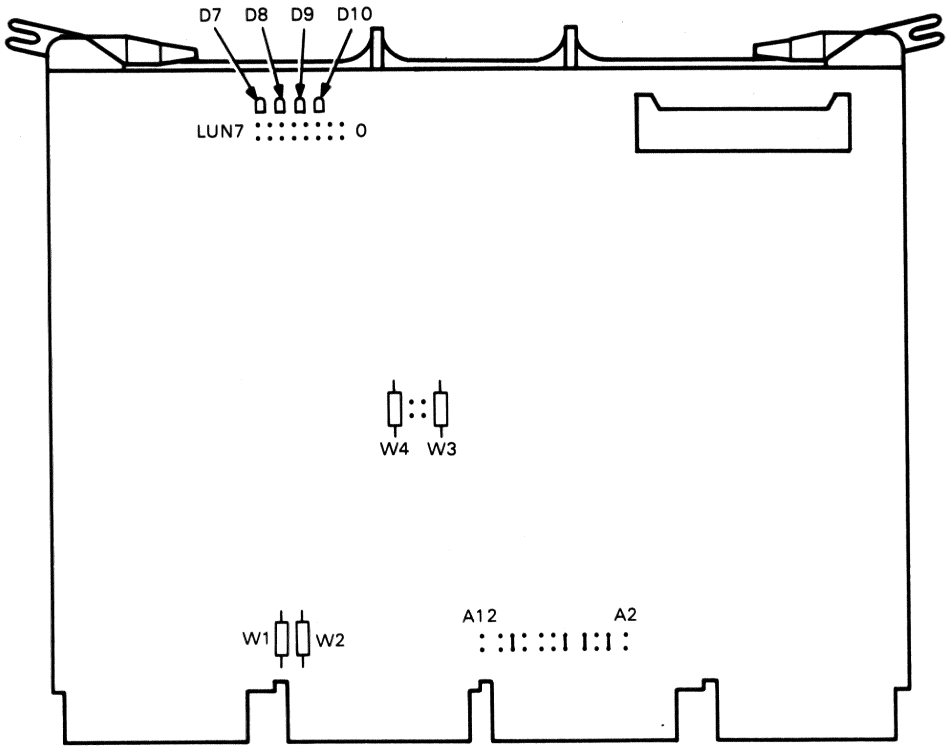



Figure 2-4 RQDX2 Controller Module

**2.3.1.1 CSR Address and Interrupt Vector –** The CSR address of the first RQDX2 module is fixed at 17772150 (factory-set). If a second RQDX2 is installed, its CSR address is floating, and set with jumpers A12:A2. (Table 2-7)

**NOTE – MSCP Device CSR Address**
**The RQDX2 controller module is an MSCP device. The first MSCP device in a system is assigned a CSR address of 17772150. If more than one MSCP device is installed, the CSR address of the second device must be set within the floating range 17760010 through 17763776.**

**Table 2-7 RQDX2 Controller Module CSR Address**

| Address Bit/ Jumper: | A12 | A11 | A10 | A09 | A08 | A07 | A06 | A05 | A04 | A03 | A02 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Jumper Position:* | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 |
| (factory-set) | | _____/ | | | _____/ | | | _____/ | | | |
| CSR Address: | 1777 | | 2 | | | 1 | | | 5 | | 0 † |
| Jumper Position: | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 |
| | | _____/ | | | _____/ | | | _____/ | | | |
| CSR Address: | 1776 | | 0 | | | 3 | | | 3 | | 4 |
| Jumper Position: | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 |
| | | _____/ | | | _____/ | | | _____/ | | | |
| CSR Address: | 1776 | | 0 | | | 3 | | | 5 | | 4 |
| Jumper Position: | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | _____/ | | | _____/ | | | _____/ | | | |
| CSR Address: | 1776 | | 0 | | | 3 | | | 7 | | 4 |

* 0 = removed; 1 = installed
† <A01:A00> = 0

The RQDX2 interrupt vector is set under program control. The first RQDX2 interrupt vector is fixed at 154. If a second RQDX2 is installed, its interrupt vector is floating.

**2.3.1.2 Logical Unit Number –** In addition to the CSR address and interrupt vector, the RQDX2 LUN (logical unit number) jumpers LUN0 through LUN7 must be configured. The jumpers represent a binary-weighted value and can be configured to assign any four LUNs to an RQDX2, starting with any LUN. The RQDX2 module is shipped with no LUN jumpers installed. No LUN jumpers installed assigns LUNs 0 through 3 to the module, and is the correct configuration for the first RQDX2 in a system. (Table 2-8) If a second RQDX2 is installed, jumper LUN2 would normally be installed, assigning LUNs 4 through 7 to the second RQDX2; and so on.

**Table 2-8 RQDX2 Controller Module LUN Jumpers**

| Jumper: | LUN7 | LUN6 | LUN5 | LUN4 | LUN3 | LUN2 | LUN1 | LUN0 | LUNs |
|---|---|---|---|---|---|---|---|---|---|
| Value: | | | 32 | 16 | 8 | 4 | 2 | 1 | |
| Jumper Position:* | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 3:0 |
| | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 4:7 |
| | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 8:11 |
| | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 12:15 |
| | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 16:19 |
| | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 20:23 |
| | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 24:27 |
| | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 28:31 |
| | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 32:35 |

* 0 = removed; 1 = installed

### 2.3.2 RD52 and RD53 Fixed Disk Drives

Order: RD5nA-AA
Disk kit (n = 2 or 3) includes:

- RD5n-A Disk drive
- 17-00282-00 20-wire signal distribution cable
- 17-00286-00 34-wire signal distribution cable

For more information, refer to the *RD52-D, -R Fixed Disk Drive Subsystem Owner's Manual* and the *113-UC/11C23-UE RD52 Upgrade Installation Guide.*

The RD52 and RD53 are fixed disk drives with formatted storage capacities of 31 and 71 Mbytes, respectively.

In addition to the cables listed above, a cable from the power supply must be connected to each RD drive in the system. If an RD5n drive is added to the system, it must be formatted. The formatting utility is included in the maintenance section of the MicroVAX II Diagnostics Kit.

**2.3.2.1 RD52 Configuration –** The RD52 read/write PC board has five pairs of pins (Figure 2-5) that are used to select the drive. To configure an RD52 as drive DU0, place a jumper on pin-pair DS3.

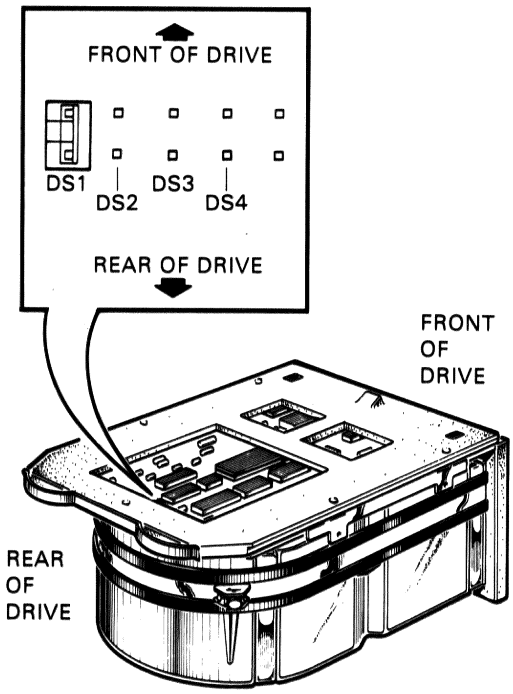



Figure 2-5 RD52 Fixed Disk Drive

**2.3.2.2 RD53 Configuration –** The RD53 read/write PC board has four switches at its rear edge. With the rear of the drive at the left, the switches are numbered:

1
2
3
4

To configure an RD53 as drive DU0, press switch 3.

### 2.3.3 RX50 Diskette Drive

Order: RX50A-AA
Diskette drive kit includes:

- RX50-AA Diskette drive
- 17-00867-00 34-wire signal distribution cable

The RX50 drive (Figure 2-6) is a random-access, dual diskette storage device that uses two single-sided 13.3 cm (5.25 in) diskettes. It has a total formatted capacity of 818 Kbytes (409 Kbytes per diskette). The diskettes are inserted into slots behind the drive's two access doors. A light next to each slot indicates when the system is reading or writing the diskette in that slot.

One RQDX2 controller supports only one RX50 diskette drive.

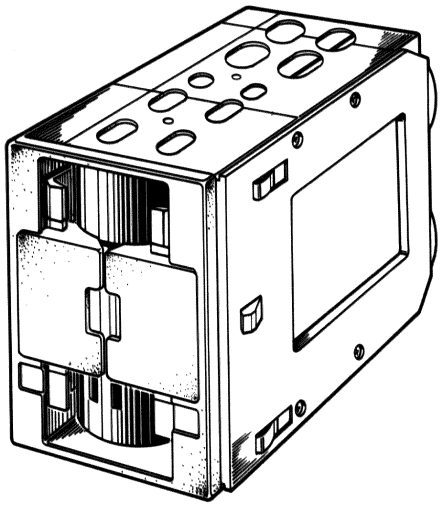


Figure 2-6 RX50 Diskette Drive

### 2.3.4 TK50 Tape Drive Subsystem

Integral TK50 tape drive subsystem:

Order: TK50-AA
Tape drive and tape cartridge

TQK50-AA
M7546 controller module and internal cable

Stand-alone TK50 tape drive subsystem:

Order: TK50-DA, -DB (DA = 120 V, DB = 240 V line cord)
Tape drive and tape cartridge

TQK50-AB
M7546 controller module, internal cable, and filter connector

The TK50 is a streaming tape drive subsystem (Figure 2-7) that uses 95-Mbyte magnetic tape cartridges for backup data storage.

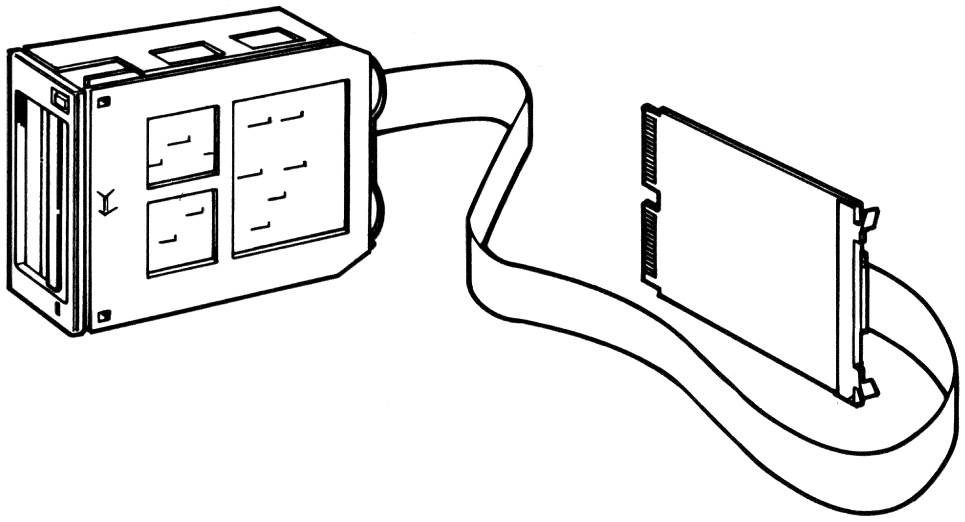


Figure 2-7 TK50 Tape Drive Subsystem

The M7546 controller module (Figure 2-8) provides the interface between the TK50-AA tape drive and the Q22-Bus.

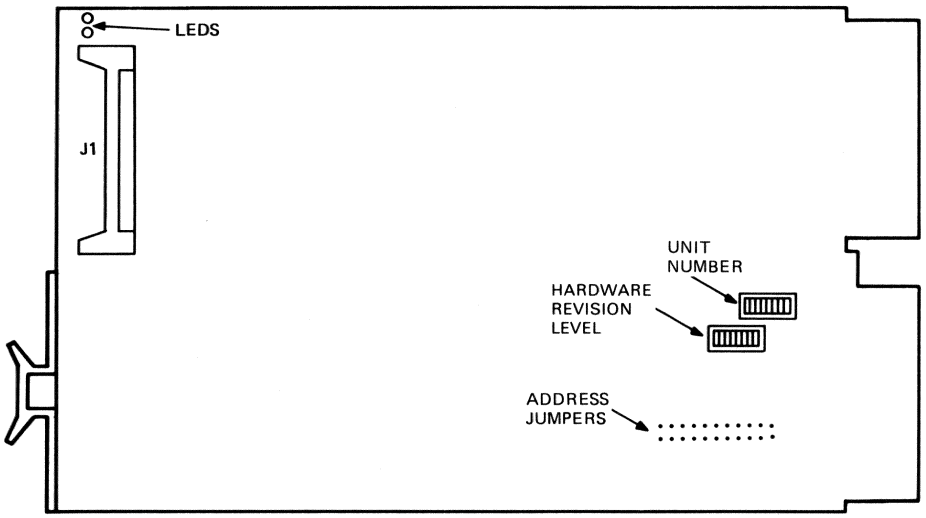



Figure 2-8 M7546 Controller Module

**2.3.4.1 M7546 Controller Module CSR Address and Interrupt Vector –** The M7546 controller module is a TMSCP (tape mass storage control protocol) device. The CSR address of the first M7546 module is fixed at 17774500 (factory-set). If a second TK50 subsystem is installed, the CSR address of the second M7546 module is floating in the range 17760010 through 17763776, and set with jumpers A12:A2. (Table 2-9)

**Table 2-9 M7546 Controller Module CSR Address**

| Address Bit/ Jumper: | A12 | A11 | A10 | A09 | A08 | A07 | A06 | A05 | A04 | A03 | A02* |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Jumper Position:† (factory-set) | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |
| CSR Address: | 1777 | | 4 | | | 5 | | | 0 | | 0 ‡ |
| Jumper Position: | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| CSR Address: | 1776 | | 0 | | | 4 | | | 0 | | 4 |
| Jumper Position: | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| CSR Address: | 1776 | | 0 | | | 4 | | | 4 | | 4 |

* Jumper A2 is closest to the module's edge.
† 0 = removed; 1 = installed
‡ <A01:A00> = 0

The interrupt vector is fixed at 260 and is set under program control.

**2.3.4.2 M7546 Controller Module Revision Level and Unit Number –** Two sets of DIP switches on the M7546 controller module (Figure 2-8) configure the hardware revision level and the unit number. The switches in both DIPs have binary-weighted values.

The hardware revision level DIP switch is factory-set to match the module revision level stamped on the back of the module. (Table 2-10)

**Table 2-10 M7546 Controller Module Revision Level Switches**

| Revision Level | Switch* 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 † |
| 1 (A) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 2 (B) | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 3 (C) | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |

* Switch 8 is closest to the module's edge.
† 0 = open; 1 = closed

The unit number can be specified with the unit number DIP switches. (Table 2-11) If the MicroVMS operating system is installed, these switches can remain at the factory setting.

**Table 2-11 M7546 Controller Module Unit Number Switches**

| Unit Number | Switch* 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |
|---|---|---|---|---|---|---|---|---|
| 0† | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 ‡ |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 2 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 3 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |

* Switch 8 is closest to the module's edge.
† Factory setting
‡ 0 = open; 1 = closed

# Options 3

## 3.1 GENERAL

This chapter describes the options currently supported by the VAXstation II system. Each option's section includes configuration set-ups and a description of the cabinet kit required to install the module. Device reference documentation is also listed. Option bus loading is listed in Chapter 4.

### 3.1.1 Ordering Options

Usually, to get all the parts needed to install an option, both a module and a cabinet kit must be ordered. For example:

- DEQNA-M M7504 module
- CK-DEQNA-KB cabinet kit

### 3.1.2 Module Configuration

When a device is installed, both its device address, commonly called a CSR (control and status register) address, and its interrupt vector must be set. The CSR address and interrupt vector are either fixed or floating.

A fixed address or vector indicates the device has a system memory address reserved for its CSR address or vector. Devices having fixed CSR addresses and vectors are usually shipped with their addresses set to the reserved memory address. If two devices of the same type are installed, the factory set addresses of the second device must be changed.

A floating CSR address or vector is assigned a memory location within an octal range. The exact address or vector within the range depends on which devices are in the system. The ranges are:

- Floating CSR address: 17760010–17763776
- Floating interrupt vector: 00000300–00000777.

Guidelines in Chapter 4 describe how to determine floating CSR address and interrupt vector settings.

Addresses and vectors are usually set with switches or jumpers on the module. Table 3-1 shows the 22-bit binary equivalent for the CSR address 17761540 (octal).

**Table 3-1 Example of a 22-bit CSR Address**

| 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | | 7 | | | 7 | | | 6 | | | 1 | | | 5 | | | 4 | | | 0 | | |

As Table 3-1 shows, floating CSR addresses in the range 17760010–17763776 can be set in bits <11:01>; bits <21:12> are not affected. Fixed CSR addresses above 17763776 can be set in bits <12:01>; bits <21:13> are not affected. Because each device typically uses a block of addresses, bits <02:00> are usually not changed. Therefore, typical switch settings affect only bits <12:03> to cover the range of both floating and fixed CSR addresses. (Table 3-2)

**Table 3-2 Example of Address Bits <12:03>**

| Address Bit: | A12 | A11 | A10 | A09 | A08 | A07 | A06 | A05 | A04 | A03 | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Switch Setting:* | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | |
| Octal Address:† | 6 | | 1 | | | 5 | | | 4 | | 0‡ |

* 0 = off; 1 = on
† If A12 switch = 1, 22-bit address = 17771540.
‡ <A02:A00> = 0

In a similar way, interrupt vectors are typically configured in bits <08:03>. (Table 3-3)

**Table 3-3 Example of Vector Bits <08:03>**

| Vector Bit: | V08 | V07 | V06 | V05 | V04 | V03 | |
|---|---|---|---|---|---|---|---|
| Switch Setting:* | 0 | 1 | 1 | 0 | 1 | 0 | |
| Octal Address: | | 3 | | | 2 | | 0† |

* 0 = off; 1 = on
† <V02:V00> = 0

## 3.2 DEQNA ETHERNET CONTROLLER

Order: DEQNA-M
M7504 module

CK-DEQNA-KB
Cabinet kit (type A filter connector and internal cable)

The dual-height DEQNA module connects a Q-Bus system to an Ethernet network. The Ethernet is an LAN (local-area network) that supports data exchange between processors through coaxial cable at a data rate of 1.2 Mbytes/s, over a moderate distance of up to 2.8 km (1.74 mi).

The module is configured using three jumpers, W1 through W3. (Figure 3-1) Jumpers W2 and W3 are factory-set and do not need to be changed.

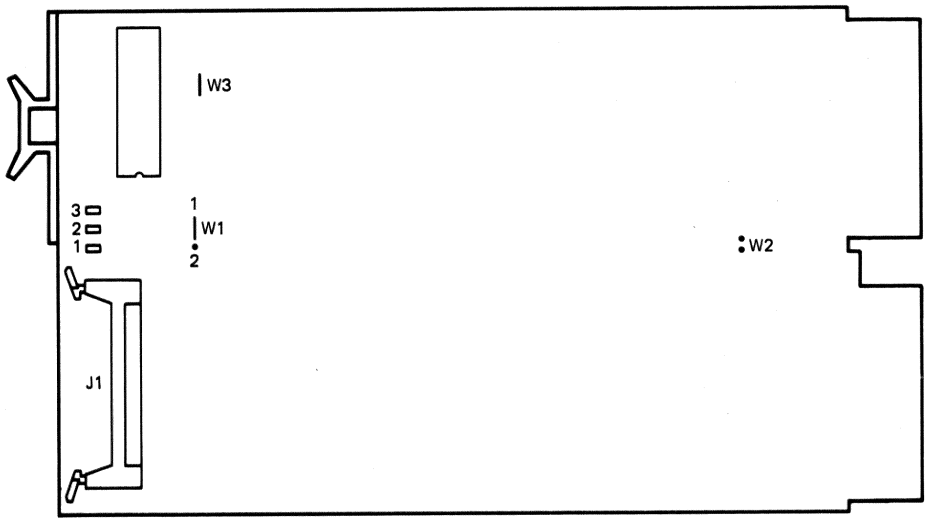



Figure 3-1 DEQNA Ethernet Controller Module

### 3.2.1 CSR Address and Interrupt Vector

Jumper W1 determines the CSR address assignment. The DEQNA CSR addresses are fixed as follows. (Table 3-4)

**Table 3-4 DEQNA CSR Address Settings**

| DEQNA | CSR Address |
|---|---|
| 1 | 17774440 |
| 2 | 17774460 |

If two DEQNA modules are to be installed, move jumper W1 of the second DEQNA onto the left and center pins. (Figure 3-1)

Software writes the interrupt vector into a read/write register. No hardware configuration is required. The interrupt vectors are listed in Table 3-5. Figure 3-2 shows the internal cabling for the DEQNA.

**Table 3-5 DEQNA Interrupt Vectors**

| DEQNA | Interrupt Vector |
|---|---|
| 1 | 120 |
| 2 | Floating |

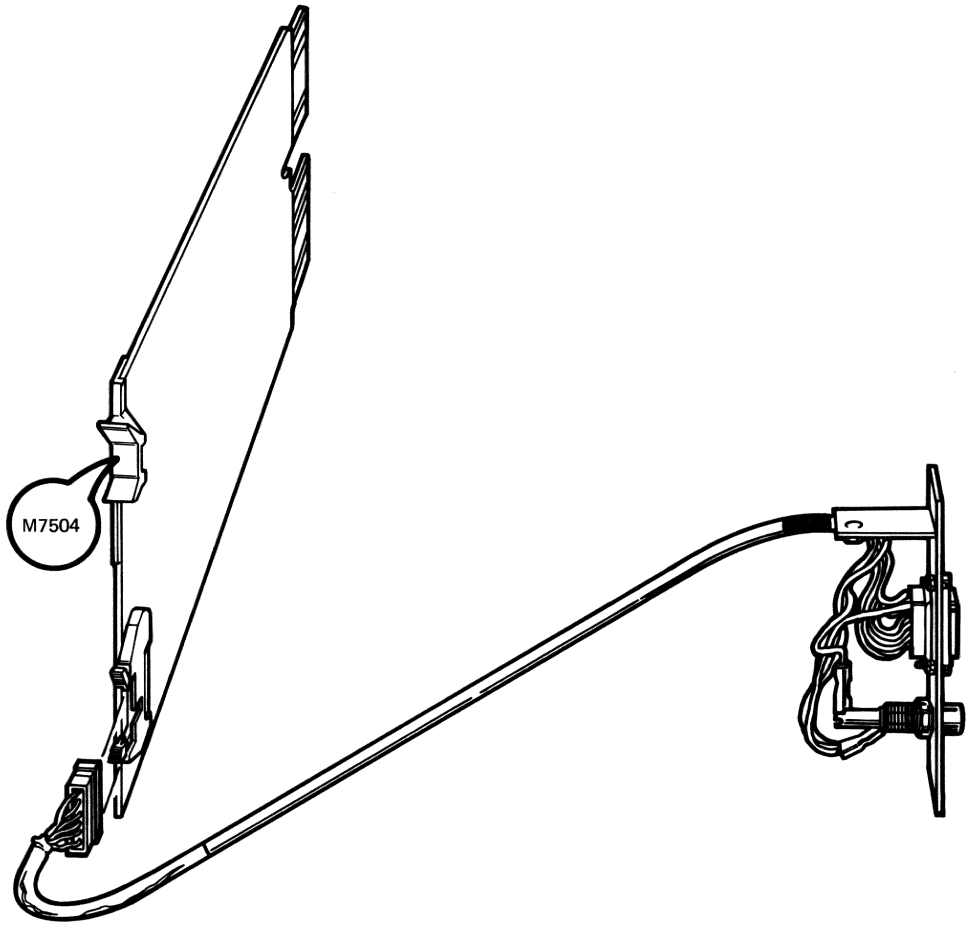



Figure 3-2 DEQNA Module Internal Cabling

## 3.3 DZQ11 ASYNCHRONOUS MULTIPLEXER

Order: DZQ11-M
M3106 module

CK-DZV11-DB
Cabinet kit (type B filter connector and internal cable)

The dual-height DZQ11 module (Figure 3-3) connects the Q22-Bus to as many as four asynchronous, serial lines. It conforms to the RS-232-C and RS423-A interface standards. The DZQ11 supports dial-up (auto-answer) operation with full-duplex modems.

### 3.3.1 CSR Address and Interrupt Vector

The floating CSR address and floating interrupt vector are set with two DIP switch sets, E28 and E13. (Figure 3-3) Tables 3-6 and 3-7 show the factory and common settings. E13 switch 7 is not used. For normal operation, E13 switch 8 must be ON, and switches 9 and 10 must be OFF. Figure 3-4 shows the module's internal cabling.

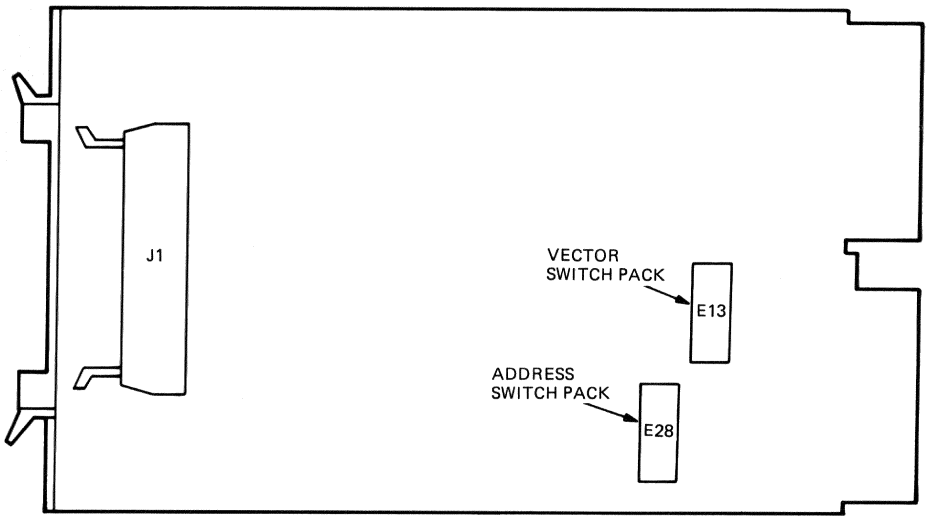



Figure 3-3 DZQ11 Module

**Table 3-6 DZQ11 Module CSR Address**

| Address Bit: | A12 | A11 | A10 | A09 | A08 | A07 | A06 | A05 | A04 | A03 | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Switch E28: | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | |
| Switch Setting:* | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | |
| (factory-set) | | _____/ | | | _____/ | | | _____/ | | | |
| CSR Address: | 1776 | | 0 | | | 0 | | | 1 | | 0† |
| Switch Setting: | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | |
| | | _____/ | | | _____/ | | | _____/ | | | |
| CSR Address: | 1776 | | 0 | | | 1 | | | 0 | | 0 |

* 0 = open; 1 = closed
† <A02:A00> = 0

**Table 3-7 DZQ11 Module Interrupt Vector**

| Vector Bit: | V08 | V07 | V06 | V05 | V04 | V03 | |
|---|---|---|---|---|---|---|---|
| Switch E13: | 1 | 2 | 3 | 4 | 5 | 6 | |
| Switch Setting:* | 0 | 1 | 1 | 0 | 0 | 0 | |
| (factory-set) | _____/ | | | _____/ | | | |
| Vector Address: | | 3 | | | 0 | | 0† |
| Switch Setting: | 0 | 1 | 1 | 0 | 1 | 0 | |
| | _____/ | | | _____/ | | | |
| Vector Address: | | 3 | | | 1 | | 0 |

* 0 = open; 1 = closed
† <V02:V00> = 0

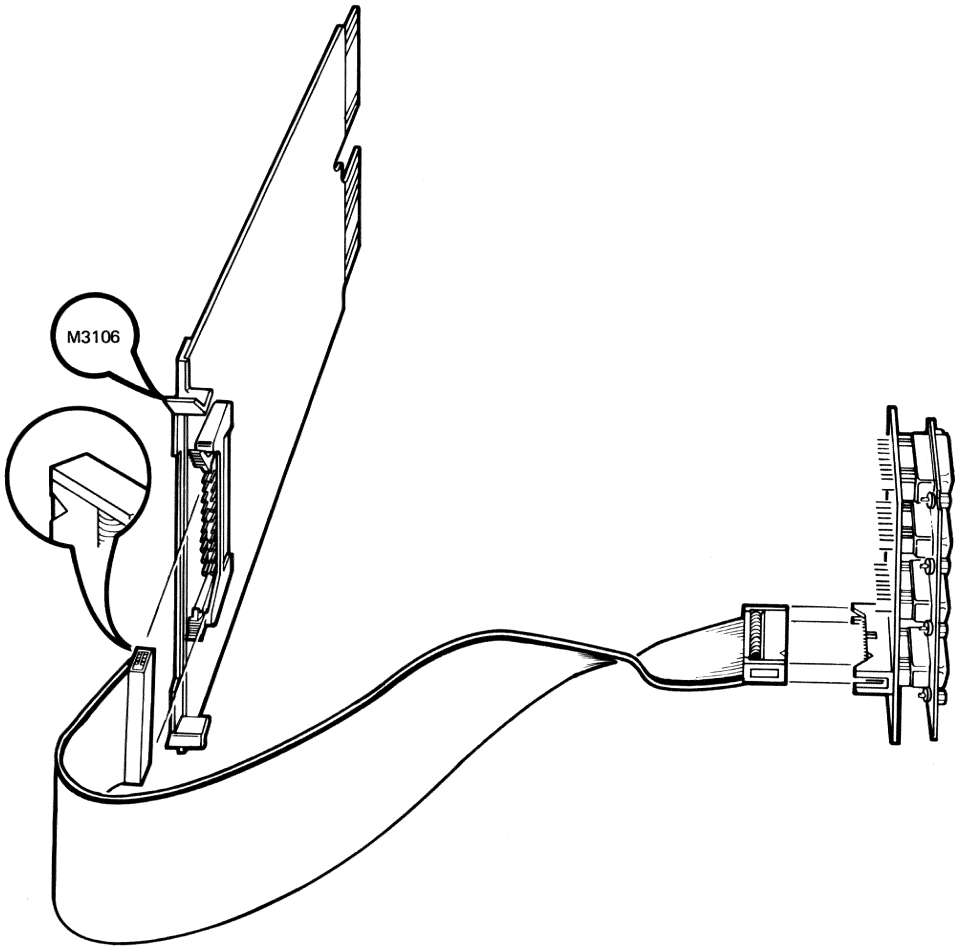



Figure 3-4 DZQ11 Module Internal Cabling

## 3.4 GRAPHICS TABLET

The graphics tablet (Figure 3-5) consists of a digitizing tablet, 4-button puck or 2-button stylus, and a 5-foot power/signal cable. The puck and stylus are interchangeable. The tablet may be used instead of the mouse as the pointing device for menu selection, graphics entry, and cursor control.

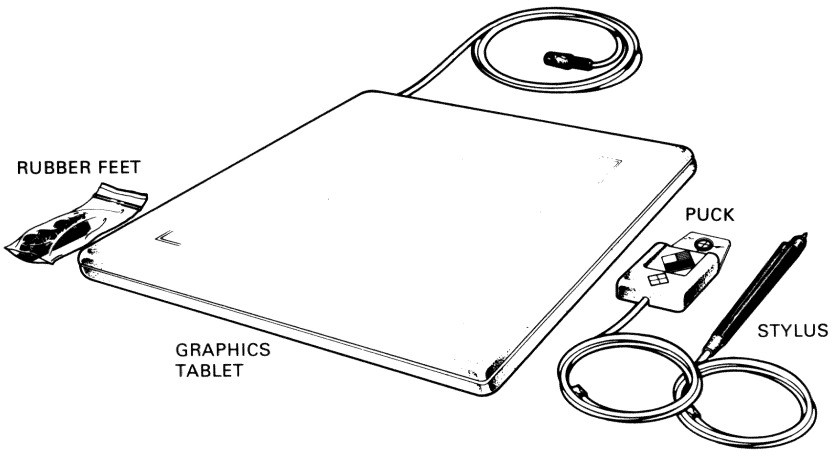



Figure 3-5 Graphics Tablet Components

The digitizing tablet is an input device that sends X-Y coordinates to the VAXstation II system to accurately indicate the position of the stylus or cursor on the tablet's surface. The tablet has a resolution of 0.005 inches (200 counts per inch). The tablet has an active area of 279 mm × 279 mm (11 in × 11 in). The tablet's physical specifications are given in Table 3-8.

**Table 3-8 Graphics Tablet Physical and Electrical Specifications**

| | |
|---|---|
| Height | 20 mm (0.80 in) |
| Width | 412 mm (16.20 in) |
| Length | 406 mm (16.0 in) |
| Weight | 3.2 kg (7.0 lbs) |
| DC power | 300 mA at +12 V ±0.5% regulation |
| Active area | 279 mm × 279 mm (11 in × 11 in) |
| Proximity (nominal) | 12.7 mm (0.5 in) puck<br>6.3 mm (0.25 in) stylus |

### 3.4.1 Baud Rate Selection

Tablet communications with the host are via an asynchronous, full-duplex, serial interface at 4800 baud (±2%) and 9600 baud (±2%).

The default baud rate of the tablet is 4800 bits/s. The baud rate is changed to 9600 bits/s by sending the ASCII character "B" (42 hexadecimal) to the tablet.

The tablet is switched back to the default baud rate by sending a "BREAK" (minimum of two character times), or by requesting a self-test of the tablet.

Baud rate selection is controlled by software, with the appropriate commands being issued by the software driver. Baud rate is not user-selectable. A modification to the software driver is necessary.

### 3.4.2 Graphics Tablet Connector Pin Assignments

The tablet uses a 7-pin micro-DIN-type connector. The pins are shown in Figure 3-6. Note that the top of the connector is three pins wide and the bottom is two pins wide. The numbers and names of these pins are listed in Table 3-9.

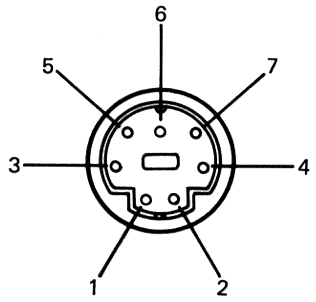



Figure 3-6 Graphics Tablet Connector Pins

**Table 3-9 Graphics Tablet Pin Assignments**

| Pin | Name (Function) |
|---|---|
| 1 | GND (Signal ground and return for power) |
| 2 | TXD (Serial out from tablet) |
| 3 | RXD (Serial in to tablet) |
| 4 | Not used |
| 5 | Not used |
| 6 | +12 V |
| 7 | Device present – connected to pin 1 |
| Shell | Protective ground |

## 4.1 CONFIGURATION RULES

You must consider the following when configuring a VAXstation II system.

1. Physical priority
2. Backplane and I/O distribution panel expansion space
3. Power requirements
4. Bus loading
5. CSR addresses and interrupt vectors

### 4.1.1 Physical Priority

System performance is affected by the backplane slot positions of the system modules. Observe the following rules when installing modules.

- KA630-An CPU is installed in slot 1.
- MS630-AA memory modules are installed in the CD position of slots 2 and 3. M9047 grant continuity cards are required in unoccupied AB positions of slots 2 and 3.

  If any other dual-height modules are installed in slots 2 or 3, they must occupy the AB (that is, Q22-Bus) half of the slot. M9047 grant continuity cards are not required.
- MS630-Bn memory modules are installed in slots 2 and 3.

**NOTE – Reserve Slots 2 and 3**
**When slots 2 and 3 are not occupied, M9047 grant continuity cards must be installed in the AB position, and the slots reserved for future memory expansion.**

- Dual-height modules can be installed in either the AB or CD position of slots 4 through 8. If only one dual-height module is installed in any of these slots, the configuration may require an M9047 grant card in the empty half of the slot.

Modules should be installed in the following sequence, with no intervening empty slots. The relative priority of the modules is based on their preferred interrupt and DMA priority.

1. KA630-An CPU
2. Memory expansion modules (two maximum):

   MS630-BB
   MS630-BA
   MS630-AA
3. DZQ11 (M3106) asynchronous communications module
4. DEQNA (M7504) Ethernet communications module
5. VCB01 (M7602) bit-map video controller
6. Mass storage controller:

   TK50 (M7546) TMSCP/DMA
   RQDX2 (M8639-YB) MSCP/DMA

### 4.1.2 Expansion Space

All eight backplane slots accept Q22-Bus modules. Figures 4-2 and 4-3 show the occupied and available slots in typical configurations.

Module I/O panel inserts are installed in either the type A or type B distribution panel cutouts. Table 4-1 lists the type of insert used with each module. The configuration worksheet (Figure 4-1) is used determine the number of inserts that can be installed.

### 4.1.3 Power Requirements

System module and mass storage device current and power requirements must not exceed the following.

- Current: +5 Vdc = 36 A
  +12 Vdc = 7 A
- Power: 230 W

**CAUTION – Maximum Current**
**Maximum +5 Vdc and +12 Vdc current cannot be drawn at the same time. The 230 W power limit will be exceeded.**

Table 4-1 lists the module current requirements. The configuration worksheet (Figure 4-1) is used to determine the current and power used.

### 4.1.4 Bus Loads

The number of backplane bus loads available are:

- 30 ac
- 20 dc

Table 4-1 lists the ac and dc bus loads for each module. The configuration worksheet (Figure 4-1) is used to determine the number of bus loads used.

**Table 4-1 Current, Bus Load, and Insert Requirements**

| Options | Module | Current | | Bus Loads | | Power | Inserts* | |
|---|---|---|---|---|---|---|---|---|
| | | +5 V | +12 V | ac | dc | Watts | A | B |
| KA630-AA | M7606 | 6.2 | 0.14† | 2.7 | 1.0 | 32.68 | | 1 |
| KA630-AB | M7606 | 5.9 | 0.14† | 2.7 | 1.0 | 31.18 | | 1 |
| MS630-AA | M7607 | 1.0† | – | – | – | 5.00 | | |
| MS630-BA | M7608 | 1.3† | – | – | – | 6.50 | | |
| MS630-BB | M7608 | 1.8† | – | – | – | 9.00 | | |
| VCB01-KP | M7602 | 5.0 | – | 3.0 | 1.0 | 25.00 | | 1 |
| DEQNA-KP | M7504 | 3.5 | 0.5 | 2.2 | 0.5 | 23.50 | 1 | |
| DZQ11-M | M3106 | 1.0 | 0.36 | 1.5 | 1.0 | 9.32 | | 1 |
| RQDX2 | M8639-YB | 6.4 | 0.25 | 2.0 | 1.0 | 35.00 | | |
| TQK50-An | M7546 | 2.2 | – | 2.0 | 1.0 | 11.00 | | |
| RX50-AA | | 0.8 | 1.8 | – | – | 25.60 | | |
| RD52-A | | 1.0 | 2.5 | – | – | 35.00 | | |
| RD53-A | | 0.9 | 2.5 | – | – | 34.50 | | |
| TK50-AA | | 1.35 | 2.4 | – | – | 35.55 | | |

* A = 2.5 × 10.0 cm (1.0 × 4.0 in)
B = 6.6 × 8.2 cm (2.6 × 3.2 in)
† Maximum

ADD THESE COLUMNS

| BACKPLANE SLOT | MODULE | CURRENT (AMPS) +5 V | CURRENT (AMPS) +12 V | POWER (WATTS) | I/O PANEL INSERTS B (2 x 3) | I/O PANEL INSERTS A (1 x 4) |
|---|---|---|---|---|---|---|
| 1 AB CD | | | | | | |
| 2 AB CD | | | | | | |
| 3 AB CD | | | | | | |
| 4 AB CD | | | | | | |
| 5 AB CD | | | | | | |
| 6 AB CD | | | | | | |
| 7 AB CD | | | | | | |
| 8 AB CD | | | | | | |
| MASS STORAGE 1 | | | | | | |
| 2 | | | | | | |
| TOTAL THESE COLUMNS: | | | | | | |
| MUST NOT EXCEED: | | 36.0 | 7.0 | 230 | 4 | 2* |

* IF MORE THAN TWO TYPE A FILTER CONNECTORS ARE REQUIRED, AN ADAPTER TEMPLATE (PN 74-27740-01) MAY BE USED. THIS WILL ALLOW THREE ADDITIONAL TYPE A FILTER CONNECTORS, BUT WILL REDUCE THE AVAILABLE TYPE B CUTOUTS TO TWO.

Figure 4-1 Configuration Worksheet

### 4.1.5 CSR Addresses and Interrupt Vectors

Modules must be set to the correct CSR address and interrupt vector (Table 4-2). Observe the following rules when using Table 4-2.

1. An F in the Vector column means the device has a floating vector. Assign a vector to each option installed, starting at 300 and continuing in the following sequence.

   300, 310, 320, 330, 340, 350, 360, 370

2. An F in the CSR Address column means the device has a floating CSR address. Use Table 4-3 to determine the floating CSR address.

3. If a module's vector and CSR address are both floating, an additional module of the same type will also have a floating vector and floating CSR address.

**Table 4-2 CSR Addresses and Vectors**

| Option | Module | Vector | CSR Address |
|---|---|---|---|
| KA630-A | M7606 | – | – |
| MS630-A | M760x | – | – |
| VCB01-KP | M7602 | – | 17777200 |
| DEQNA-KP | M7504 | 120 | 17774440 |
| DZQ11-M | M3106 | F | F |
| RQDX2 | M8639-YB | 154 | 17772150 |
| TQK50-An | M7546 | 260 | 17774500 |

**Table 4-3 Floating CSR Addresses**

| Option | Number | CSR Address |
|---|---|---|
| DZQ11-M | 1 | 17760010 |
| DZQ11-M | 2 | 17760100 |

## 4.2 CONFIGURATION EXAMPLES

Many VAXstation II configurations are possible. Figure 4-2 shows a completed configuration worksheet for a base system.

Figure 4-3 shows a base system that has been expanded with the addition of two 4-Mbyte MS630 memory modules and a DEQNA Ethernet controller module.

ADD THESE COLUMNS

| BACKPLANE SLOT | MODULE | CURRENT (AMPS) +5 V | CURRENT (AMPS) +12 V | POWER (WATTS) | I/O PANEL INSERTS B (2 x 3) | I/O PANEL INSERTS A (1 x 4) |
|---|---|---|---|---|---|---|
| 1 AB CD | KA630-AA (QUAD) | 6.2 | 0.14 | 32.68 | 1 | |
| 2 AB CD | M9047 MS630-AA | -- 1.0 | -- | 5.00 | | |
| 3 AB CD | M9047 [EMPTY] | -- | -- | -- | | |
| 4 AB CD | VCB01-KP (QUAD) | 5.0 | -- | 25.00 | 1 | |
| 5 AB CD | RQDX2 (QUAD) | 6.4 | 0.25 | 35.00 | | |
| 6 AB CD | | | | | | |
| 7 AB CD | | | | | | |
| 8 AB CD | | | | | | |
| MASS STORAGE 1 | RX50-AA | 0.8 | 1.80 | 25.60 | | |
| 2 | RD52-A | 1.0 | 2.50 | 35.00 | | |
| TOTAL THESE COLUMNS: | | 20.4 | 4.69 | 158.28 | 2 | 0 |
| MUST NOT EXCEED: | | 36.0 | 7.0 | 230 | 4 | 2* |

* IF MORE THAN TWO TYPE A FILTER CONNECTORS ARE REQUIRED, AN ADAPTER TEMPLATE (PN 74-27740-01) MAY BE USED. THIS WILL ALLOW THREE ADDITIONAL TYPE A FILTER CONNECTORS, BUT WILL REDUCE THE AVAILABLE TYPE B CUTOUTS TO TWO.

Figure 4-2 Base System Worksheet

ADD THESE COLUMNS

| BACKPLANE SLOT | MODULE | CURRENT (AMPS) +5 V | CURRENT (AMPS) +12 V | POWER (WATTS) | I/O PANEL INSERTS B (2 x 3) | I/O PANEL INSERTS A (1 x 4) |
|---|---|---|---|---|---|---|
| 1 AB CD | KA630-AA (QUAD) | 6.2 | 0.14 | 32.68 | 1 | |
| 2 AB CD | MS630-BB (QUAD) | 1.8 | -- | 9.00 | | |
| 3 AB CD | MS630-BB (QUAD) | 1.8 | -- | 9.00 | | |
| 4 AB CD | DEQNA-KP M9047 | 3.5 -- | 0.5 -- | 23.50 -- | | 1 |
| 5 AB CD | VCB01-KP (QUAD) | 5.0 | -- | 25.00 | 1 | |
| 6 AB CD | RQDX2 (QUAD) | 6.4 | 0.25 | 35.00 | | |
| 7 AB CD | | | | | | |
| 8 AB CD | | | | | | |
| MASS STORAGE 1 | RX50-AA | 0.8 | 1.80 | 25.60 | | |
| 2 | RD52-A | 1.0 | 2.50 | 35.00 | | |
| TOTAL THESE COLUMNS: | | 26.5 | 5.19 | 194.78 | 2 | 1 |
| MUST NOT EXCEED: | | 36.0 | 7.0 | 230 | 4 | 2* |

* IF MORE THAN TWO TYPE A FILTER CONNECTORS ARE REQUIRED, AN ADAPTER TEMPLATE (PN 74-27740-01) MAY BE USED. THIS WILL ALLOW THREE ADDITIONAL TYPE A FILTER CONNECTORS, BUT WILL REDUCE THE AVAILABLE TYPE B CUTOUTS TO TWO.

Figure 4-3 Expanded System Worksheet

# Diagnostics 5

This chapter presents an overview of MicroVAX II diagnostic and maintenance tools, and also provides fault isolation guidelines.

## 5.1 KA630 SELF-TESTS

The MicroVAX II boot and diagnostic ROM tests the basic functions of the KA630 CPU module. Testing can occur in either power-up mode or console I/O mode.

### 5.1.1 Power-up Mode

In power-up mode, the ROM-based diagnostics and boot programs test the KA630 CPU module's ability to load and run an operating system, the MicroVAX Maintenance System, or other diagnostic software.

Table 5-1 describes each test in the ROM-based diagnostic and lists its hexadecimal code. While each test is being run, the hex (hexadecimal) value is displayed:

- In the segmented LED on the CPU patch panel insert
- In four red LEDs (in binary form) on the KA630-An CPU module (Figure 5-1), and
- For values less than 9, on the console terminal.

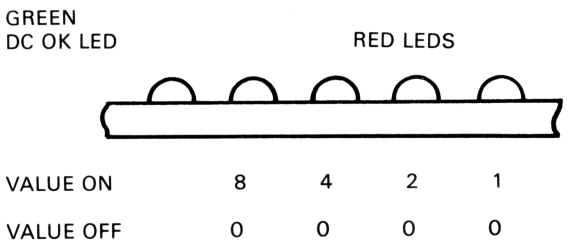



Figure 5-1 CPU Module LEDs

The green DC OK LED indicates the same conditions as the front control panel DC OK indicator (Table 1-3). The sum of lighted red LEDs is a hexadecimal value that indicates the same condition as a value listed in Table 5-1.

If a test fails, the test sequence halts, and the code of the failed test remains displayed. Table 5-1 also lists the field replaceable unit(s), or FRU(s), that most likely caused the test to fail.

**Table 5-1 Diagnostic LED Status and Error Messages**

| Hex Value | TEST NAME – CONSOLE TERMINAL MESSAGE/ Most Likely Failed FRU(s) |
|---|---|
| F | WAITING FOR DC OK |
| | 1. KA630-An module (does not recognize DC OK assertion)<br>2. Power supply (negating DC OK on bus)<br>3. Q22-Bus device (negating DC OK on bus)<br>4. Backplane (DC OK shorted to another signal) |
| E | WAITING FOR P OK |
| | 1. KA630-An module (does not recognize P OK assertion)<br>2. Power supply (negating P OK on bus)<br>3. Q22-Bus device (negating P OK on bus)<br>4. Backplane (P OK shorted to another signal) |
| D | RUNNING CHECKSUM TEST ON ROM |
| | 1. KA630-An module |
| C | SEARCHING FOR RAM MEMORY REQUIRED FOR ROM PROGRAMS |
| | 1. KA630-An module<br>2. MS630 module(s)<br>3. KA630-An/MS630 interconnect cable (short- or open-circuited) |
| B | READ KA630-An IPCR REGISTER (accesses Q22-Bus) |
| | 1. KA630-An module<br>2. Q22-Bus device (preventing the CPU from acquiring the bus)<br>3. Backplane (preventing the CPU from acquiring the bus) |

**Table 5-1 Diagnostic LED Status and Error Messages (Cont.)**

| Hex Value | TEST NAME – CONSOLE TERMINAL MESSAGE/ Most Likely Failed FRU(s) |
|---|---|
| A | TESTING VCB01 VIDEO CONSOLE DISPLAY (if present)<br>1. Keyboard for VCB01 (defective or not connected)<br>2. Video display for VCB01 (defective or not connected)<br>NOTE: A failed monitor is indicated by no video display. The system does not detect a failed monitor. If the keyboard is connected through the BC18P cable, the system will boot.<br>3. VCB01 module<br>4. KA630-An module (cannot read or write Q22-Bus; may be shorting Q22-Bus)<br>5. Q22-Bus device (preventing the CPU from acquiring the bus)<br>6. Backplane (preventing the CPU from acquiring the bus)<br>7. VCB01 I/O distribution panel insert |
| 9 | IDENTIFYING CONSOLE TERMINAL<br>1. KA630-An module (If console does not respond within six seconds, CPU will proceed to 7.) |
| 8 | LANGUAGE INQUIRY OR CPU HALTED<br>When the LED is stopped at 8, the system is either:<br>a) preparing to ask the user to select the language to be used,<br>b) informing the user that the CPU is halted, or<br>c) actually indicating a failure.<br>If the system is not indicating a halt, but waiting for a language to be entered, within 2 to 6 minutes (depending on console terminal's baud rate) a time-out occurs and testing continues.<br>Before the console terminal displays the message for test 8, it should display a header message reporting the CPU version number and other system information. If the LED on the CPU patch panel displays 8 (or a lower test number) and the console terminal does not display a header message, suspect:<br>1. KA630-An module (probably the console interface)<br>2. Console cables (defective or not connected)<br>3. Console baud rate (mismatched) |

**Table 5-1 Diagnostic LED Status and Error Messages (Cont.)**

| Hex Value | TEST NAME – CONSOLE TERMINAL MESSAGE/ Most Likely Failed FRU(s) |
|---|---|
| | NOTE: There is no baud rate setting when the graphics subsystem is used as the console terminal. This test applies to base-MicroVAX II systems, or to printers connected to the CPU SLU port. |
| | 4. Console terminal (defective or power off)<br>5. Console I/O distribution panel insert |
| 7 | RUNNING DATA TESTS ON RAM MEMORY |
| | 1. KA630-An module (RAM memory failure)<br>2. MS630 module<br>3. Backplane (CD interconnect short- or open-circuited)<br>4. KA630-An/MS630 interconnect cable (short- or open-circuited) |
| 6 | RUNNING ADDRESS TESTS ON RAM MEMORY |
| | 1. MS630 module<br>2. Backplane (CD interconnect short- or open-circuited)<br>3. KA630-An/MS630 interconnect cable (short- or open-circuited) |
| 5 | RUNNING TESTS THAT USE Q22 BUS MAP TO ACCESS LOCAL MEMORY |
| | 1. KA630-An module<br>2. Q22-Bus device (preventing the CPU from acquiring the bus)<br>3. Backplane (preventing the CPU from acquiring the bus) |
| 4 | CPU INSTRUCTION AND REGISTER TESTS |
| | 1. KA630-An module |
| 3 | RUNNING INTERRUPT TESTS |
| | 1. KA630-An module<br>2. Q22-Bus device (incorrectly requesting interrupt)<br>3. Backplane (Q22-Bus BR line short-circuited) |
| 2 | SEARCHING FOR BOOTSTRAP DEVICE |
| | NOTE: Before continuing here, try the procedures in the Troubleshooting section of the *VAXstation II Owner's Manual, BA23 Enclosure.* |
| | Before assuming drives or controllers are defective, check their signal and power cables. After checking the cables, check the devices' power-up LEDs. (See Paragraph 5.2.) |

**Table 5-1 Diagnostic LED Status and Error Messages (Cont.)**

| Hex Value | TEST NAME – CONSOLE TERMINAL MESSAGE/ Most Likely Failed FRU(s) |
|---|---|
| | 1. RQDX controller module, RD5n fixed disk drive, RX50 diskette drive, or interconnect cable (defective or not properly connected)<br>2. TQK50 controller module, TK50 tape drive, or interconnect cable (defective or not properly connected)<br>3. DEQNA module<br>4. KA630-An module |
| 1 | BOOTSTRAP DEVICE FOUND |
| | 1. Q22-Bus bootstrap device<br>2. Signal cable to bootstrap device (defective or not connected)<br>3. Power cable to bootstrap device (defective or not connected)<br>4. KA630-An module |
| 0 | TESTING COMPLETED |

### 5.1.2 Console Mode

In console I/O mode, the TEST command is used to select any of the ROM tests; the EXAMINE command displays the contents of registers and memory; and the BOOT command, with an appropriate qualifier, selects the boot device. Console commands are described in more detail in Appendix A.

**5.1.2.1 Console Terminal Error Messages –** The following is an example of the console terminal error message format.

KA630.XX

Performing normal system tests.

7..

? <subtest> <p1> <p2> <p3>

Failure.
Normal operation not possible.

Where:

KA630.XX

Identifies the processor and the console program ROM version number.

Performing normal system tests.

The system is performing the tests programmed in the ROM.

7..

The countdown sequence, showing the system is progressing through its tests. The numbers displayed indicate the same conditions as the numbers displayed in the segmented LED on the CPU patch panel insert. (Table 5-1)

? <subtest> <p1> <p2> <p3>

A diagnostic message including the question mark, a subtest code number, and up to three parameters: indicates the countdown sequence has been interrupted. Parameters are described in Appendix B.

Failure.
Normal operation not possible.

The test failed and the console program is not executing.

## 5.2 DEVICE SELF-TESTS

Several VAXstation II devices and options also have the on-board capability to perform power-up self-tests, and report the results in on-board LEDs. Figures 5-2 through 5-4 show these LEDs, and Tables 5-2 through 5-4 describe what they indicate.

### 5.2.1 DEQNA Ethernet Controller Module

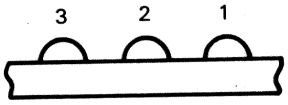



Figure 5-2 DEQNA Module LEDs

**Table 5-2 DEQNA Module LEDs**

| LED 3 | LED 2 | LED 1 | Description/ Most Likely Failed FRU(s) |
|---|---|---|---|
| ON | ON | ON | Performing DEQNA station address PROM test.<br>1. DEQNA module<br>2. KA630 module<br>3. Q22-Bus device<br>4. Backplane |
| ON | ON | OFF | Performing DEQNA internal loopback test.<br>1. DEQNA module |
| ON | OFF | OFF | Performing DEQNA external loopback test.<br>1. DEQNA module<br>2. Cabling (short- or open-circuited, or not connected)<br>3. Fuse in I/O distribution panel insert |
| OFF | OFF | OFF | DEQNA passed all power-up tests. |

### 5.2.2 RQDX2 Mass Storage Controller Module

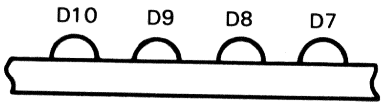



Figure 5-3 RQDX2 Module LEDs

**Table 5-3 RQDX2 Module LEDs**

| LED D10 | D9 | D8 | D7 | Description |
|---|---|---|---|---|
| NOTE: The RQDX2 controller module is the most likely failed FRU in all cases. | | | | |
| ON | ON | ON | ON | Beginning power-up testing. |
| OFF | OFF | OFF | ON | Performing T11 processor test. |
| OFF | OFF | ON | OFF | Performing T11 timer/counter/address generator test. |
| OFF | OFF | ON | ON | Performing Q22-Bus timer/counter/address generator test. |
| OFF | ON | OFF | OFF | Performing serializer/deserializer test. |
| OFF | ON | OFF | ON | Performing CRC generator test. |
| OFF | ON | ON | OFF | Performing hardware version test. |
| OFF | ON | ON | ON | Performing ROM checksum test. |
| ON | OFF | OFF | OFF | Performing RAM test. |
| ON | OFF | OFF | ON | Performing diagnostic interrupt test. |
| ON | OFF | ON | OFF | Performing shuffle oscillator test. |
| ON | OFF | ON | ON | Performing valid configuration test. |
| ON | ON | OFF | OFF | Not used. |
| ON | ON | OFF | ON | Not used. |
| ON | ON | ON | OFF | Not used. |
| OFF | OFF | OFF | OFF | Testing completed. |

### 5.2.3 TQK50 Tape Controller Module

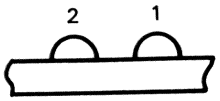



Figure 5-4 TQK50 Module LEDs

**Table 5-4 TQK50 Module LEDs**

| LED 2 | LED 1 | Description/ Most Likely Failed FRU(s) |
|---|---|---|
| ON then OFF | OFF | Module/drive interaction test fails.<br>1. TQK50 module<br>2. TK50 drive<br>3. Interconnect cable |
| OFF | ON | Module failed power-up test.<br>1. TQK50 module |
| OFF | OFF | Module power-up test and module/drive interaction test both failed.<br>1. TQK50 module<br>2. TK50 drive<br>3. Interconnect cable |
| ON then OFF | ON | Module and drive working correctly. |

## 5.3 MicroVAX MAINTENANCE SYSTEM (MMS)

The MicroVAX Maintenance System (MMS) is a combination diagnostic/ maintenance operating system. The system is available in: 1) the verification version, provided with each MicroVAX II system, and 2) the maintenance version, shipped with the MicroVAX II Maintenance kit. The verification version is described here. (The maintenance version is described in the *MicroVAX II System Maintenance Guide.*) The verification version provides configuration verification and system-level testing.

MMS is menu-driven, and can be loaded from tape or diskette into any MicroVAX II system. Figure 5-5 shows the menu tree of MMS functions.

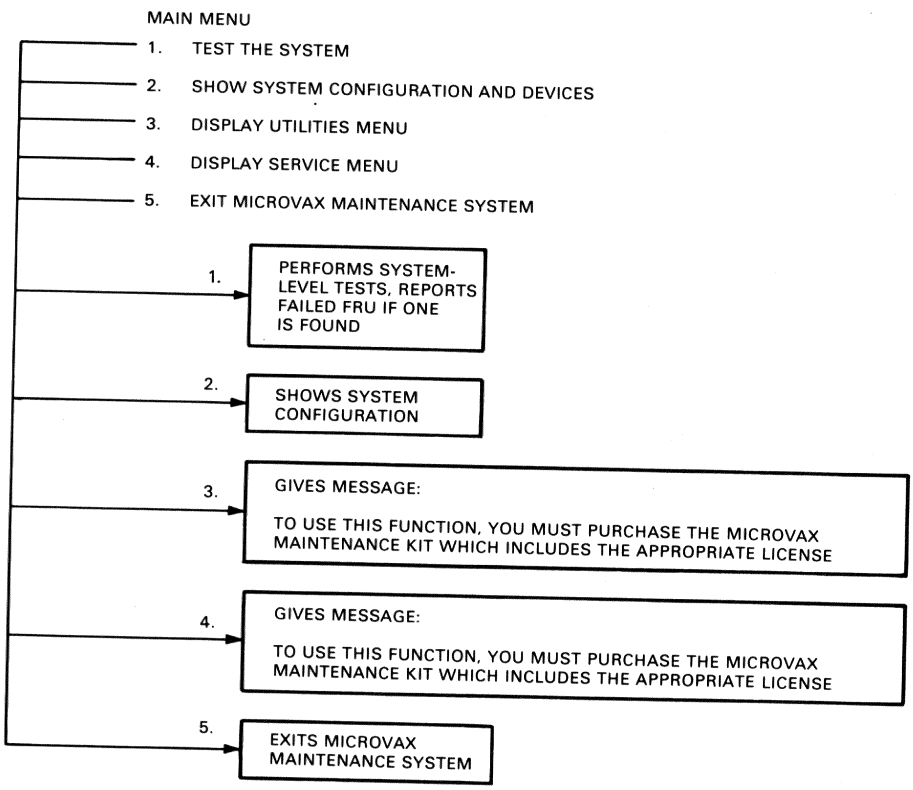



Figure 5-5 MicroVAX Maintenance System Menu Tree

### 5.3.1 Configuration Verification

MMS verifies the system installation by determining which devices are installed, and then displaying the system configuration it recognizes. An installation problem appears when the terminal display does not include a device known to be installed.

### 5.3.2 System Tests

MMS runs system-level functional and exerciser tests. Any user can run system-level tests on all recognized devices, at any time, without loss of data.

## 5.4 TROUBLESHOOTING

**NOTE**
**Before going on, read the Problem/Solution section of the *VAXstation II Owner's Manual, BA23 Enclosure.***

The primary VAXstation II troubleshooting tools are:

- Front panel indicators
- Power-up self-tests
- *VAXstation II Owner's Manual, BA23 Enclosure*
- *VAXstation II Technical Manual, BA23 Enclosure*
- *VAXstation Maintenance Guide*
- MicroVAX Maintenance System.

Most VAXstation II system problems will be:

- Unknown system-level problems (system fails to boot)
- Suspected device-level problems (system can boot; problem may be intermittent). Problems in the:
  - CPU
  - Memory
  - Graphics subsystem
  - Mass storage devices
  - Communications devices.

The following are suggested troubleshooting methods for each type of problem.

### 5.4.1 Unknown System-Level Problems

Follow these steps to diagnose unknown system-level problems:

1. Read the message on the console terminal.
   - If the test number is 7, 6, 5, 4, or 3, use Table 5-1 to isolate the failed FRU.
   - If the test number is 2, 1, or 0, use Table 5-1 and the module LEDs to isolate the failed FRU.

2. If the terminal screen is blank, check the segmented LED on the CPU patch panel insert.
   - The LED has run through power-up tests. The panel insert could be in loop-back mode, bypassing the console terminal.
   - The LED value is not F. The console terminal cable or the console-to-patch-panel cable is faulty or disconnected.
   - The LED value is F. The CPU, the patch panel insert, or the CPU-to-patch-panel-insert cable is faulty or disconnected.
3. If the segmented LED is blank, check the front panel indications, and continue as shown in Figure 5-6.

Figure 5-6 shows the general procedure for troubleshooting the system when either the operating system or the MMS fails to boot.

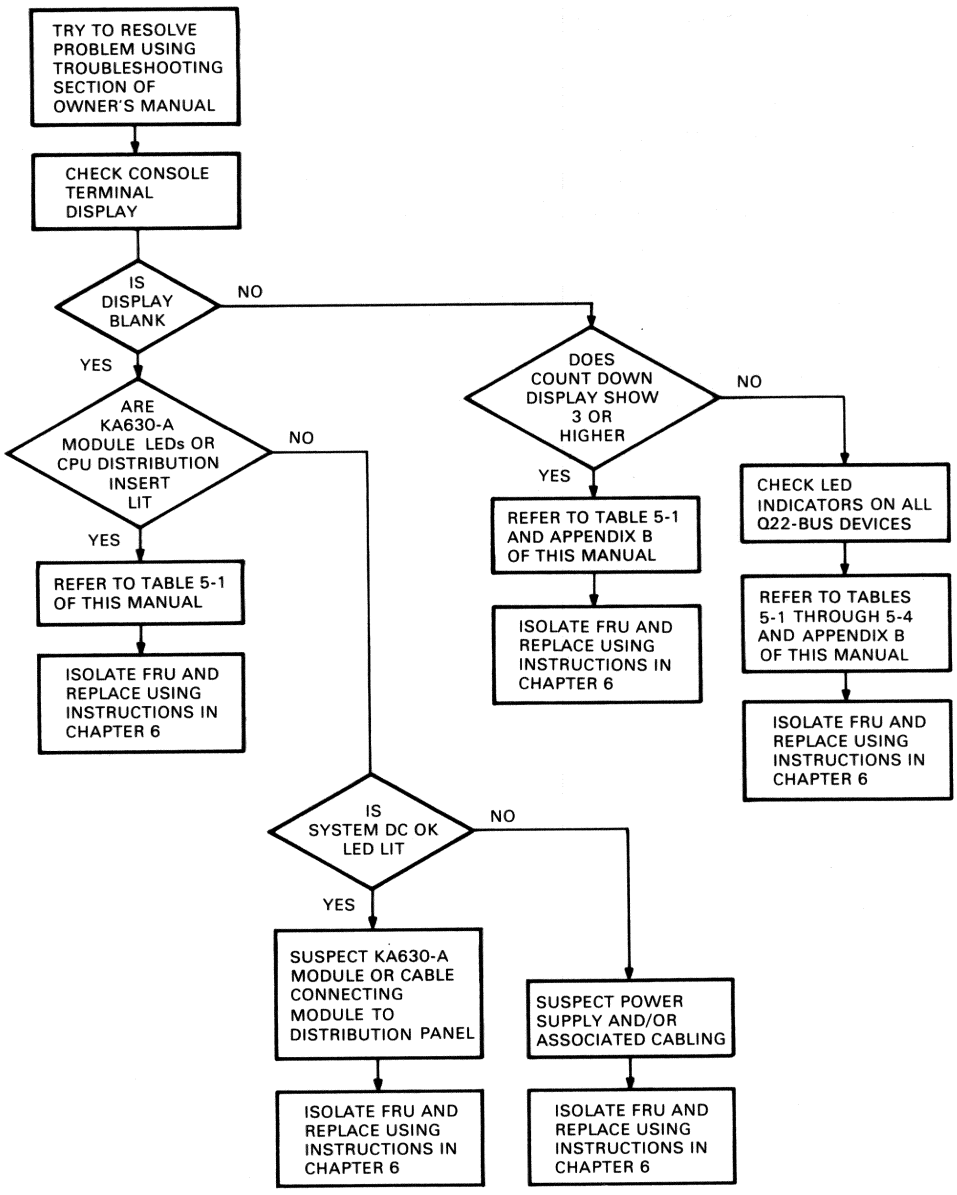



Figure 5-6 Boot Failure Troubleshooting Flowchart

### 5.4.2 Device-Specific Problems

Follow these steps to diagnose a device-specific problem:

1. Boot the MicroVAX Maintenance System.
2. Select the configuration procedure from the Main Menu. The screen display should list all the devices known to be installed. If an installed device does not appear in the display:
   - The device is faulty or disconnected. See Chapter 6 for removal and replacement information.
   - The device address is wrong. See Chapter 6 for removal and replacement information, and Chapter 4 for configuration information.
3. Select the system-level tests from the Main Menu. Within 6 minutes the test results should be displayed. When testing has started, one of the following should occur.
   - The test locates a failed FRU. See Chapter 6 for removal and replacement procedures.
   - The test fails, but a failed FRU is not identified. See the *VAXstation Maintenance Guide.*
   - The test passes, but a system problem exists. Check the device LEDs.

Figure 5-7 shows the general troubleshooting procedure for device-specific problems.

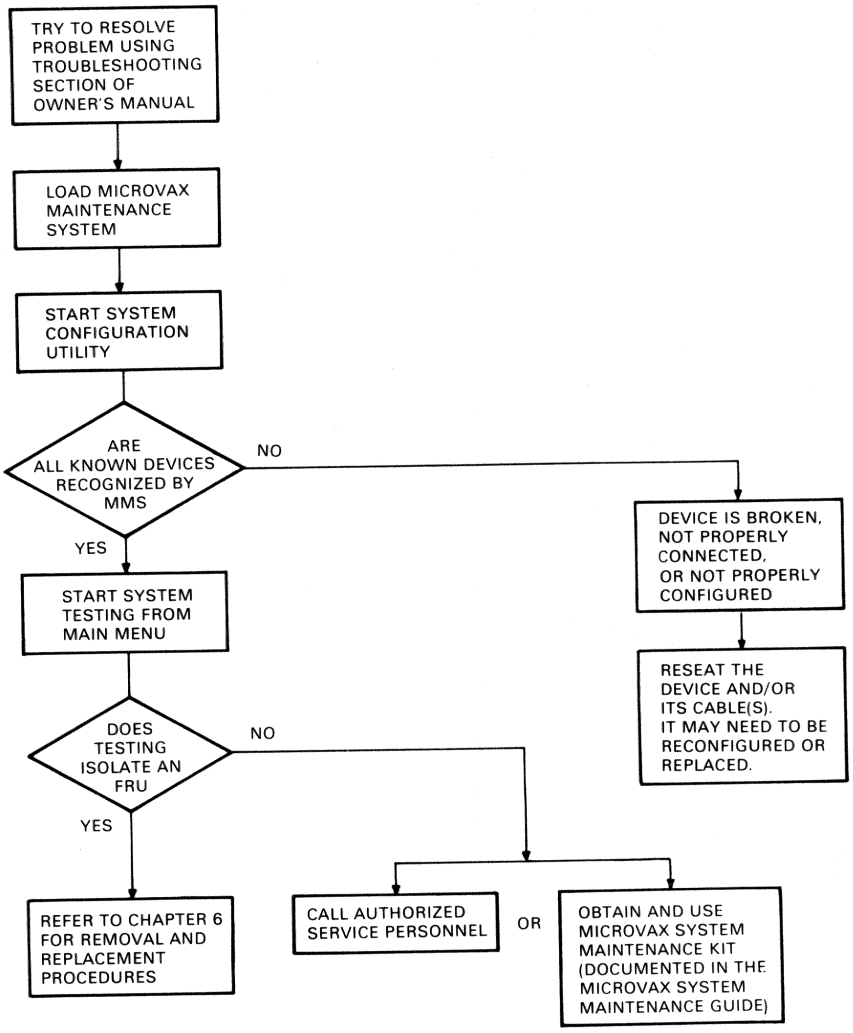



Figure 5-7 Device-Specific Failure Troubleshooting Flowchart

### 5.4.3 VR260 Monitor Troubleshooting Procedures

Table 5-5 lists some symptoms of common problems with the VR260 monitor. When troubleshooting, follow the suggested corrective actions in the order listed.

**Table 5-5 VR260 Monitor Failure Indications**

| Symptom | Corrective Action |
|---|---|
| No LED or screen display | Check that the power switch is on. |
| | Check the power cord connection. |
| | Check the 120/240 Vac setting. |
| | Remove the rear bulkhead assembly and check the connection to the ac transformer assembly. |
| | Check the deflection board connections. |
| | Replace the deflection board. |
| Flashing LED | Check the deflection board connections, including the chassis ground. |
| | Make sure the high voltage anode lead has a good connection with the CRT. |
| | Replace the deflection board. |
| Compressed raster or no video display | Check the VAXstation II diagnostic display. If other than a pass indication (.), fix the VAXstation II before proceeding with adjustment/repair of the VR260 monitor. |
| | Ensure proper VAXstation-to-VR260 monitor cabling. |
| | Remove the rear bulkhead assembly and check the cable connections to the video amplification board. |
| | Remove the video amplification board and check the CRT pin connections. |
| | Replace the video amplification board. |
| Raster present but no video display | Check for a pass indication (.) on the VAXstation. |
| | Ensure good CRT connections. |
| | Replace the video amplification board. |

**Table 5-5 VR260 Monitor Failure Indications (Cont.)**

| Symptom | Corrective Action |
|---|---|
| LED off but video display is present | Remove the LED bezel assembly and check for good connection.<br>Replace the LED.<br>Ensure proper cable connections from the deflection board to the LED bezel assembly. |

# FRU Removal and Replacement 6

## 6.1 GENERAL

This chapter describes the removal and replacement procedures for the VAXstation II system's field replaceable units (FRUs). Only qualified personnel should perform these procedures. Table 6-1 lists the FRUs and their part numbers.

**CAUTION – Static Electricity**
**Static electricity can damage semiconductor devices. Always use a grounded wrist-strap (part number 29-11762-00) and grounded work surface when handling system components and modules with exposed semiconductor devices.**

**Table 6-1 Field Replaceable Units (FRUs)**

| FRU | Part Number |
|---|---|
| KA630-AA CPU module | M7606-AA |
| KA630-AB CPU module | M7606-BA |
| MS630-AA memory module (1 Mbyte) | M7607-AA |
| MS630-BA memory module (2 Mbyte) | M7608-AA |
| MS630-BB memory module (4 Mbyte) | M7608-BA |
| VCB01 video controller module | M7602 |
| VCB01 I/O distribution panel insert | 70-21495-01 |
| VR260 monitor | VR260-AA |
| Deflection board | 54-15624-01 |
| Video amplification board | 54-15626-00 |
| Rear bulkhead | 70-21266-01 |
| Brightness/contrast assembly | 70-21863-01 |
| Video (monitor/keyboard) cable | BC18P-10 |
| Keyboard | LK201-CA |
| Mouse | 30-20038-01 |
| H7864-A power supply | 30-21749-01 |
| DZQ11 asynchronous communications module | M3106 |

**Table 6-1 Field Replaceable Units (FRUs) (Cont.)**

| FRU | Part Number |
|---|---|
| DEQNA Ethernet controller module | M7504 |
| DEQNA cabinet kit | CK-DEQNA-KB |
| RQDX2 mass storage controller module | M8639-YA |
| RX/RD power cable | 70-20435-1K |
| RD52 fixed disk drive | 30-21721-02* |
| RD52-AA* | 30-23227-02* |
| RD52 read/write module | 29-24992-00 |
| RD53 fixed disk drive | RD53-AA |
| RD5n signal cable (20 wire) | 17-00282-00 |
| RD5n signal cable (34 wire) | 17-00286-00 |
| RX50 diskette drive | RX50-AA* |
| RX50 signal cable | 17-00285-02 |
| TK50 tape drive | TK50-AA |
| TQK50 controller module | M7546 |
| TK50 tape drive cable and trap door | 70-22313-01 |
| Grant card | M9047 |
| Power supply ac power cable with ac switch | 70-20434-01 |
| System dc fan (rear) | 12-17556-01 |
| System dc fan (front) | 12-17556-01 |
| DC fan power cable | 70-20449-00 |
| Backplane assembly | 70-19986-00 |
| Q22-Bus backplane | H9278-A |
| Backplane dc power cord | 70-20450-01 |
| Signal distribution panel | 54-15633-00 |
| Loopback connectors | 12-15336-00 |
| Front control panel | 70-22007-01 |
| Control panel cable | 70-20451-1C |
| Patch and filter assembly | 70-19979-00 |
| 630QA patch panel | 54-17644-01 |
| SLU cable (10 pin) | 17-00624-01 |
| LED cable (20 pin) | 17-00712-02 |
| Adapter plate | 74-28684-01 |
| I/O distribution panel | 70-19979-0 |
| Front bezel (rackmount) | 74-29501-01 |
| Front bezel (floorstand/tabletop) | 74-29559-0 |

**Table 6-1 Field Replaceable Units (FRUs) (Cont.)**

| FRU | Part Number |
|---|---|
| Rear bezel | 74-27560-0 |
| Pedestal (floorstand) | 74-27012-0 |
| Plastic enclosure skins | 70-20469-01 |
| Rackmount kit | 70-22025-01 |
| Chassis support kit | 70-20761-01 |

* When adding one of these drives to a system without disk drives, use the RX50Q-AA, RD51Q-AA, or RD52Q-AA option, which includes the drive and signal cables.

## 6.2 CONTROL PANEL

Refer to Figure 6-1.

### 6.2.1 Removal

1. Unplug the ac power cord from the wall socket.
2. Remove the front plastic cover by holding each end and pulling the cover away from the system.
3. Remove the front chassis retaining bracket.
4. Push the subsystem forward.
5. Remove the subsystem storage cover.
6. Remove the four screws retaining the control panel assembly.
7. Disconnect the Berg connector from the control panel.
8. Remove the power supply connector from J7 on the power supply.

### 6.2.2 Replacement

1. Reverse the removal procedure.
2. Make sure the LTC switch and the Restart Enable switch on the control panel's printed circuit board are in the out position.

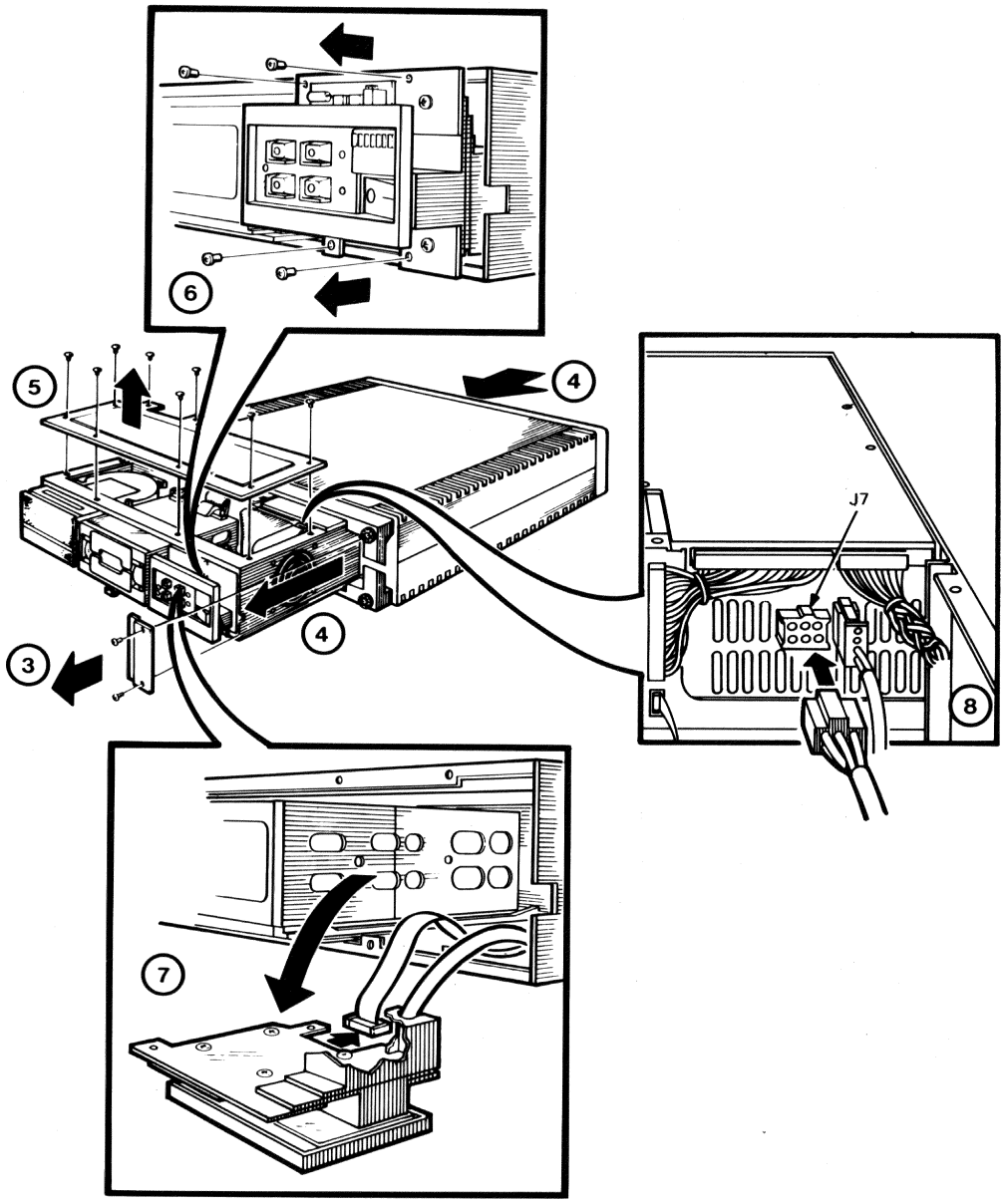



Figure 6-1 Control Panel Removal

## 6.3 RX50 DISKETTE DRIVE/TK50 TAPE DRIVE

The diskette and tape drives are single FRUs. Do not disassemble them or remove any of their printed circuit boards. All adjustments require a special test configuration.

**NOTE**
**The following removal/replacement procedure applies to the TK50 tape drive as well.**

### 6.3.1 RX50 Diskette Drive Removal

Refer to Figure 6-2.

1. Remove the front and rear bezels and the ac power cord.
2. Remove the front chassis retaining bracket.
3. Push the subsystem forward.
4. Remove the subsystem storage cover.
5. Disconnect the signal cable and the dc power cable from the diskette drive by pulling straight up on the connectors.
6. Push down on the release tab, slide the drive forward, and remove it.

### 6.3.2 RX50 Diskette Drive Replacement

1. Reverse the removal procedure.
2. Remove the cardboard shipping insert from a newly installed RX50 diskette drive.
3. Use only formatted RX50K diskettes, available from Digital and its licensed distributors.

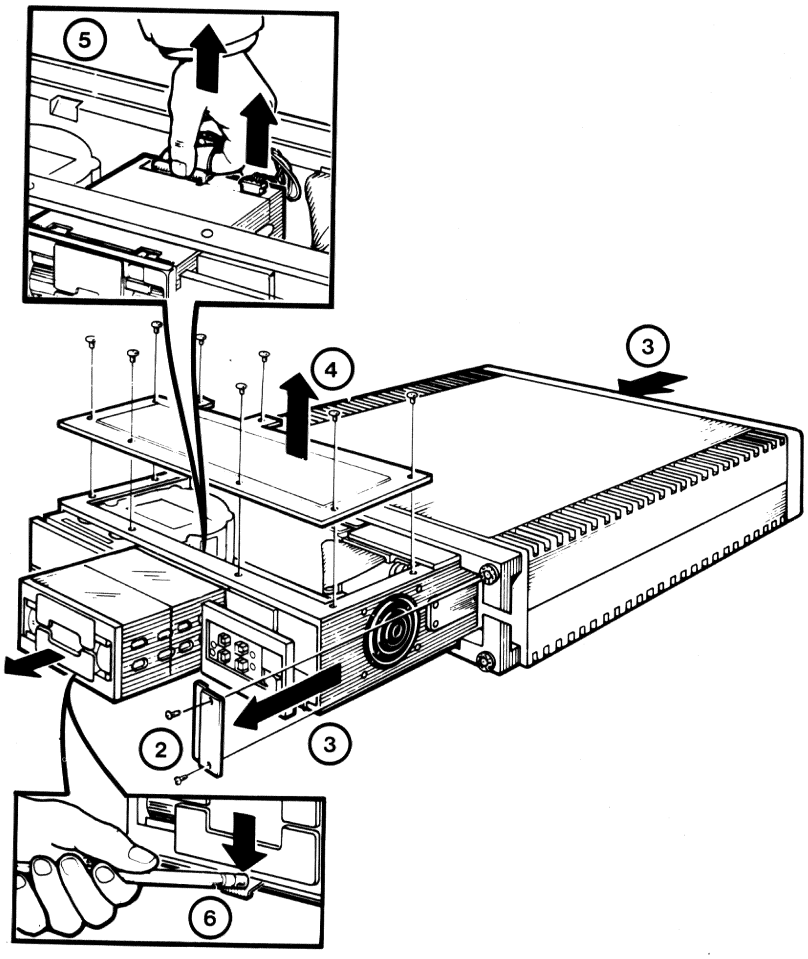



Figure 6-2 RX50 Diskette Drive Removal

### 6.3.3 TK50/TQK50 Interconnect Cable Removal

A cable connects the TK50 tape drive to its TQK50 controller module. This interconnect cable runs through the trap door on the signal distribution panel, and beneath the modules in the card cage. When the TK50 drive has been removed (following the procedure in Paragraph 6.3.1), remove the interconnect cable as follows.

1. Release the interconnect cable from the wire-tie that holds it to the trap door on the signal distribution panel.
2. Remove the two screws that hold the trap door to the signal distribution panel, and remove the door. (Figure 6-3)
3. Disconnect the RQDX controller cable (also behind the trap door), and move it to the side to provide working room.
4. Go to the rear of the enclosure and remove the module in slot 8 (the bottom slot) of the backplane. (See Paragraph 6.9.)
5. From the back of the enclosure, pull the TK50/TQK50 interconnect cable through the signal distribution panel, backplane, and card cage.

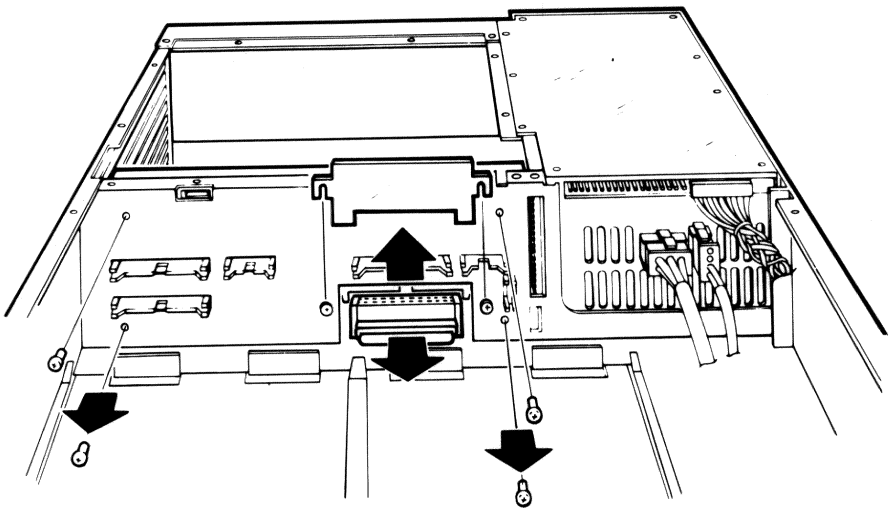


Figure 6-3 Trap Door Removal

### 6.3.4 TK50/TQK50 Interconnect Cable Replacement

1. Reverse the removal procedure.
2. When replacing the interconnect cable, be sure to observe the "THIS SIDE UP" marking on the cable. As a check, the striped side of the cable should be nearer the front fan of the enclosure.
3. It is easier to push the cable through from the front of the enclosure to the back, rather than from back to front.

4. When installing a TK50 tape drive in a BA23 enclosure that has not previously contained a TK50 drive, make sure also to install the new trap door shipped with the drive. Do not try to use the trap door that originally came with the system.

## 6.4 RD5n FIXED DISK DRIVE

Refer to Figure 6-4.

### 6.4.1 Removal

**CAUTION – Fixed Disk Drive**
**Handle fixed disk drives with care. Dropping or bumping a drive can damage the disk surface.**

1. Remove the front and rear bezels and the ac power cord.
2. Remove the front chassis retaining bracket.
3. Push the subsystem forward.
4. Remove the subsystem storage cover.
5. Remove the power plug and the two ribbon cables from the RD5n drive.
6. Push down on the release tab, slide the drive forward, and remove it.
7. Package any disk drive to be returned in the replacement disk drive's shipping carton. If the shipping carton is not available, one may be ordered (part number 99-90045-01).

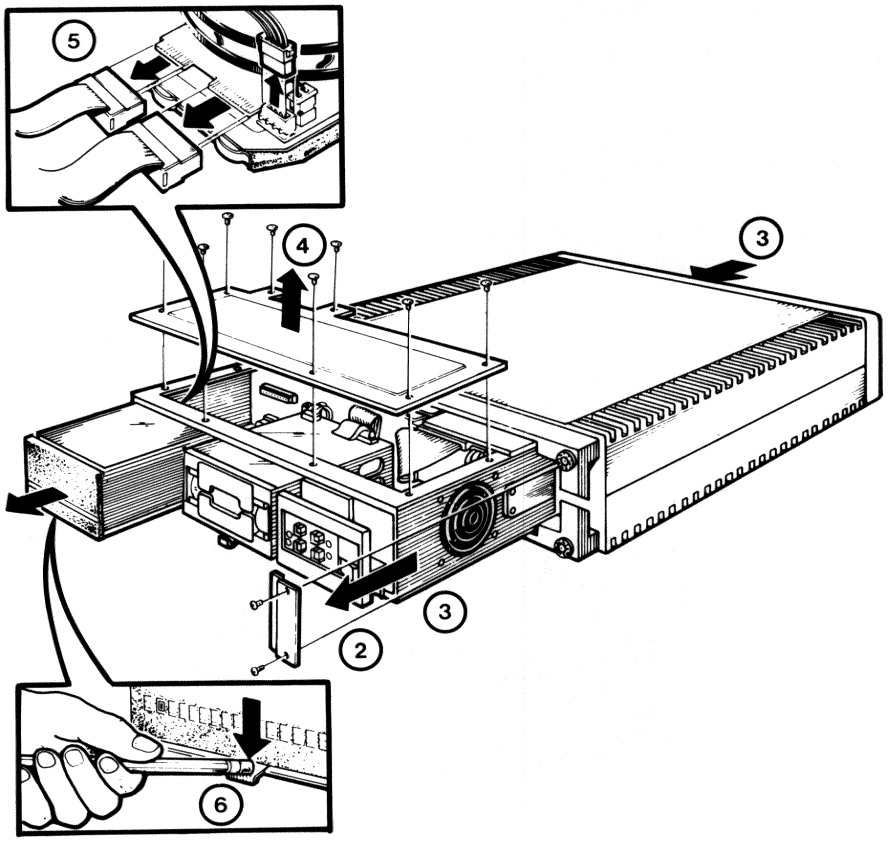



Figure 6-4 Fixed Disk Drive Removal

### 6.4.2 Replacement

1. Reverse the removal procedure.
2. To configure an RD5n drive as DU0 or DUA0, see Chapter 2, Paragraph 2.3.2.
3. You must format a newly installed RD5n disk drive before testing the system and using the drive. Write-protect any other RD5n disk drives present in the system before you format a newly installed RD5n disk drive. Remember to write-enable these drives when you finish formatting the new drive.

### 6.4.3 RD52 MPCB Removal

Replace the MPCB (main printed circuit board) only in RD52 disk drives with the part number 30-21721-02.

Screws located on the skid plate and MPCB have different sizes. Make sure you reinstall the screws in their proper locations.

1. Remove the four Phillips screws retaining the skid plate and ground clip. Set the skid plate aside. (Figure 6-5)

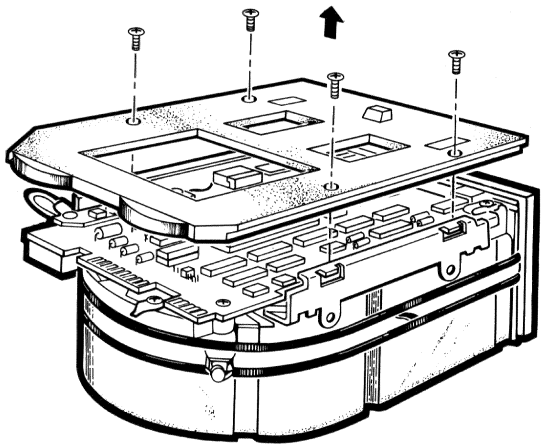


Figure 6-5 Skid Plate Removal (RD52)

2. Unplug the 2-pin connector. (Figure 6-6)

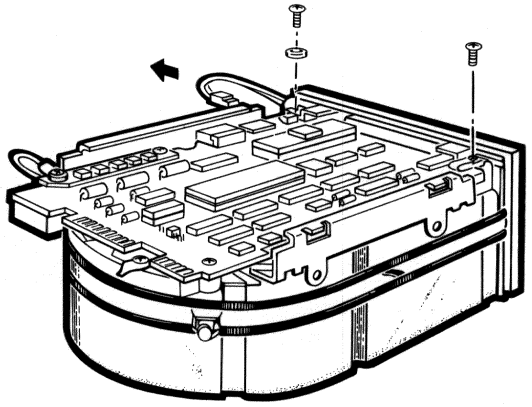


Figure 6-6 2-pin Connector and Screws Removal (RD52)

3. Remove the two Phillips screws that attach the front bezel to the drive.
4. Remove the front bezel by pulling it away from the drive. The bezel is held in place with pop fasteners. (Figure 6-7)

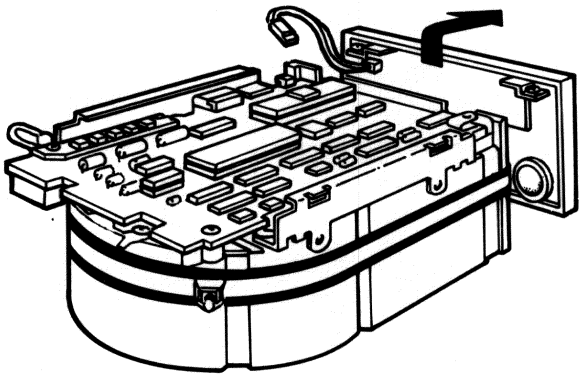


Figure 6-7 Front Bezel Removal (RD52)

5. Remove the three Phillips screws from the heatsink, grounding strip, and the corner opposite the heatsink. (Figure 6-8)

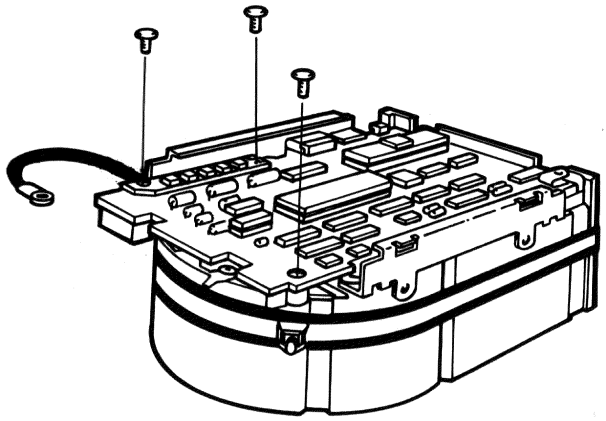


Figure 6-8 Heatsink Screws Removal (RD52)

6. Lift the MPCB straight up until it clears the chassis. This disconnects P4, a 12-pin fixed plug. (Figure 6-9)
7. Disconnect P5, a 10-pin connector.

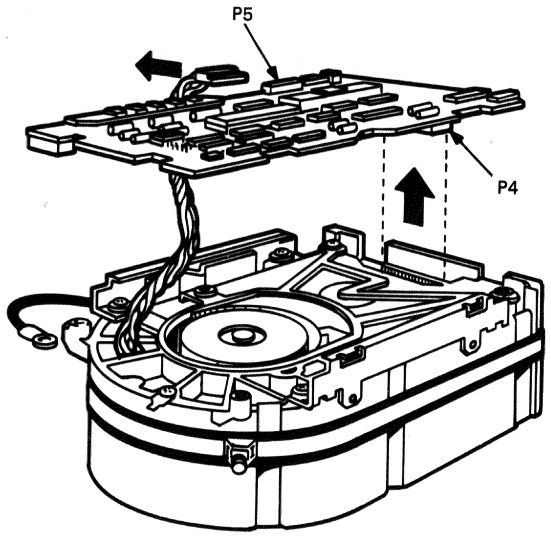



Figure 6-9 MPCB Removal (RD52)

### 6.4.4 RD52 MPCB Replacement

Reverse the removal procedure.

### 6.4.5 RD53 Device Electronics Board Removal

The RD53 device electronics board is the only part of an RD53 drive that is replaceable. Always try replacing the device electronics board before you replace an entire RD53 drive.

1. Remove the four Phillips screws retaining the skid plate and ground clip. Set the plate aside. (Figure 6-10)
2. Loosen the two captive screws that hold the device electronics board in place.
3. Rotate the board upward (the board pivots in hinge slots at the front of the drive). Being careful not to strain any connectors or cables, tilt the board at its hinge until it comes to rest against the outer frame.

**CAUTION – Flexible Circuit**
**Flexible circuit material is fragile and requires careful handling to avoid damage.**

4. Disconnect the motor control board connector, J8, and the preamplifier board connector, J9, from the read/write board. Both connectors and cables are fragile, so handle them with care.
5. Lift the board out of the hinge slots.

### 6.4.6 RD53 Device Electronics Board Replacement

1. Reverse the removal procedures.
2. Be sure the new board's jumpers and switches are set to the same positions as the replaced board's jumpers and switches were.

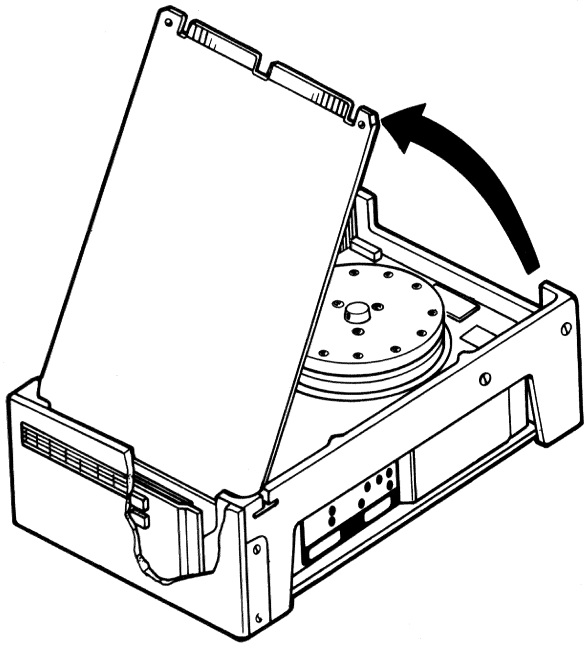


Figure 6-10 RD53 Device Electronics Board Removal

### 6.4.7 RD5n/RQDX Interconnect Cable Removal

RD5n and RX50 drives are connected to the signal distribution panel, which is in turn connected to the RQDX controller module via an interconnect cable. This cable runs from the signal distribution panel, underneath the modules in the card cage, to the back of the RQDX module. Once you have removed the drives from the BA23 enclosure, use the following procedure to remove the interconnect cable.

1. Release the TK50 interconnect cable (if present) from the wire-tie that holds it to the trap door on the signal distribution panel.
2. Remove the two screws that attach the trap door to the signal distribution panel, and remove the door. (Figure 6-11)
3. Disconnect the TK50 controller cable (behind the trap door), and move it to the side to provide working room.
4. Disconnect the RD5n/RQDX interconnect cable from the connector, which was exposed when the trap door was removed.

5. Go to the rear of the enclosure and remove the module in slot 8 (the bottom slot) of the backplane. (See Paragraph 6.9.)
6. From the back of the enclosure, pull the RD5n/RQDX interconnect cable through the signal distribution panel, backplane, and card cage. You may also have to remove the TK50/TQK50 cable to get the RD5n/RQDX cable out.

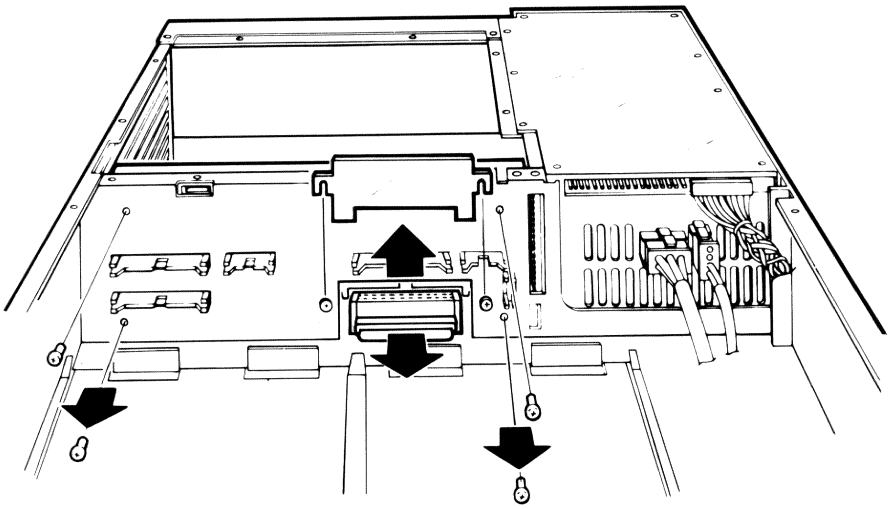


Figure 6-11 Trap Door Removal

### 6.4.8 RD5n/RQDX Interconnect Cable Replacement

1. Reverse the removal procedure.
2. When replacing the cable, it is easier to push the cable through from the front of the enclosure to the back, rather than from back to front.
3. When replacing the TK50/TQK50 interconnect cable, be sure to observe the "THIS SIDE UP" marking on the cable. As a check, the striped side of the cable should be nearer the front fan of the enclosure.

## 6.5 BACKPLANE ASSEMBLY

### 6.5.1 Removal

1. Remove the front and rear bezels and all cables. Label them for reinstallation later.
2. Remove the rear retaining bracket and slide the subsystem completely out through the back.
3. Remove both the subsystem storage cover and the Q22-Bus module cover. (Figure 6-12)
4. Open the rear I/O distribution panel assembly by loosening the two captive screws, and disconnect any cables attached to the I/O panel. Label the cables for reinstallation later, noting the orientations of the red stripe on any cables you remove.
5. Remove all the system modules. (Figure 6-13) (See Paragraph 6.9.)
6. If present, remove the cowling from the front fan.
7. Remove any RX50 and RD5n drives that are present. (See Paragraphs 6.3 and 6.4.)
8. Remove the RX50 and RD5n drive signal cables from J6, J2, and J7 on the signal distribution panel.
9. Remove the power supply connectors and front control panel connectors from J1, J4, and J2 on the signal distribution panel and J9 on the power supply.

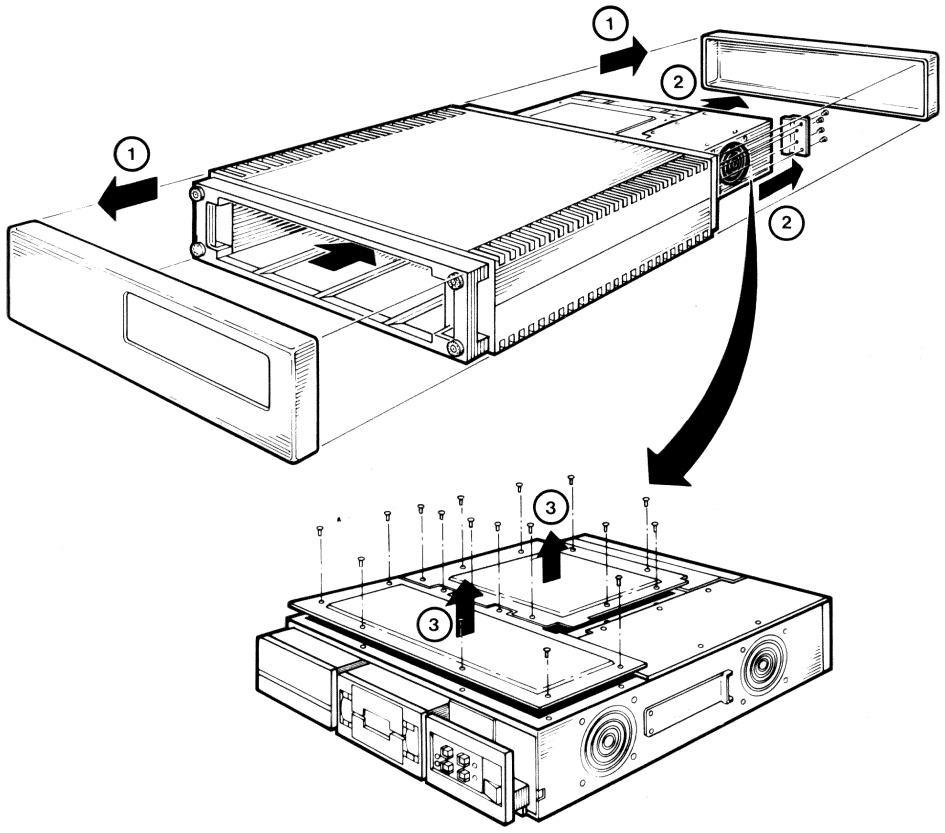



Figure 6-12 Backplane Removal (Steps 1–3)

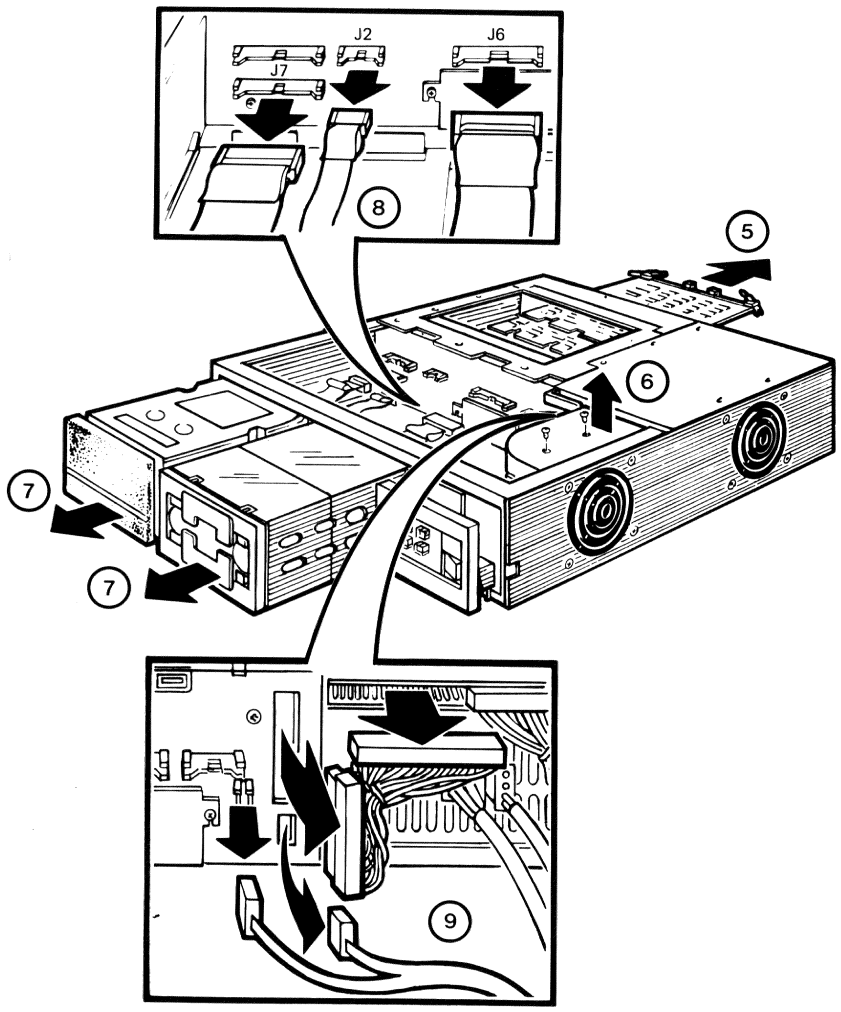



Figure 6-13 Backplane Removal (Steps 4–9)

10. Loosen the two screws retaining the small access cover. Remove the cover and disconnect the cable from side two of the backplane. (Figure 6-14)
11. Remove the four screws holding the backplane assembly to the chassis.

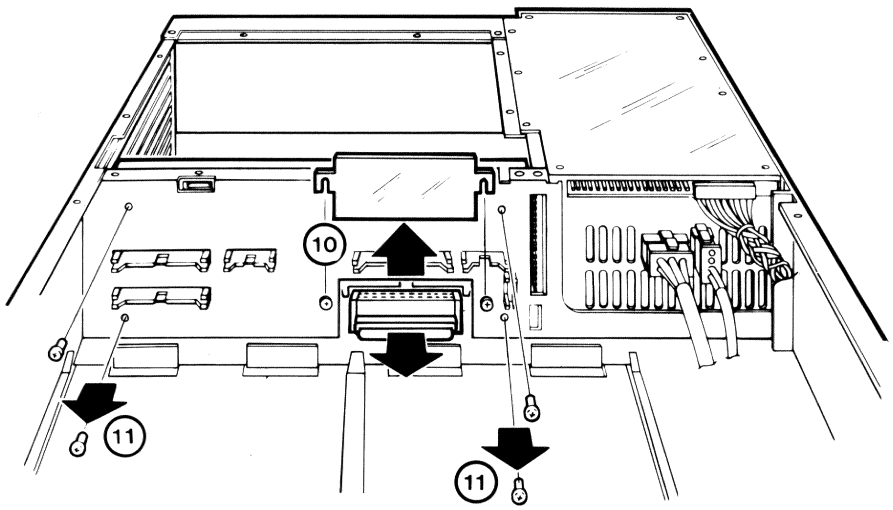



Figure 6-14 Backplane Removal (Steps 10 and 11)

12. Pivot the CD side of the backplane assembly 45 degrees toward the rear and lift it straight up. (Figure 6-15)

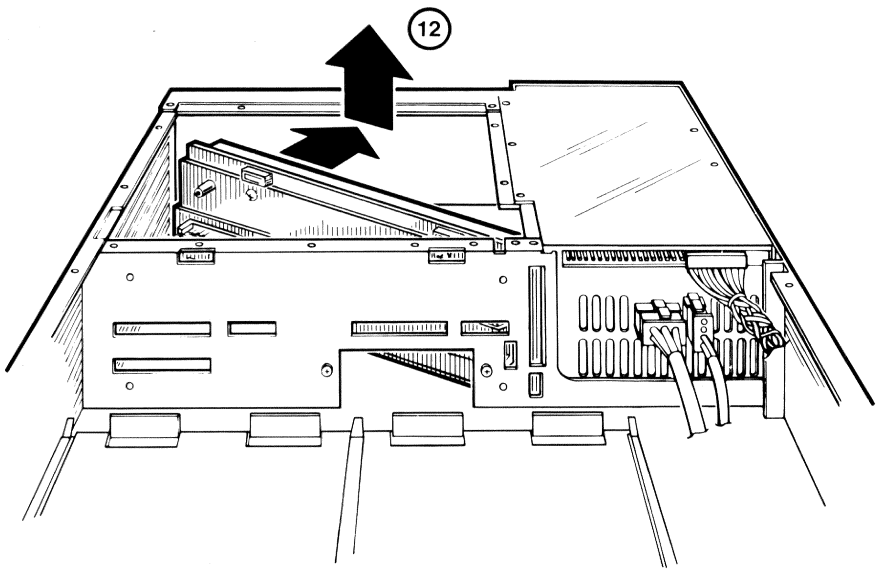



Figure 6-15 Backplane Removal (Step 12)

### 6.5.2 Replacement

Reverse the removal procedure.

## 6.6 H7864-A POWER SUPPLY

The H7864-A power supply is not adjustable, nor does it contain replaceable printed circuit boards. The +5 Vdc and +12 Vdc regulators are fixed. Voltage tolerance is +5.1 Vdc (±2.5%) for the +5 Vdc regulator, and +12.1 Vdc (±2.5%) for the +12 Vdc regulator. Ripple is 50 mV peak-to-peak at +5 Vdc, and 75 mV peak-to-peak at +12 Vdc.

### 6.6.1 Removal

Refer to Figure 6-16.

1. Remove the front and rear bezels and all cables.
2. Remove the rear chassis retaining bracket and slide the subsystem completely out through the back.
3. Remove the subsystem storage cover.
4. If present, remove the fan cowling and cowling holder.
5. Disconnect the backplane power connector from J9 on the power supply and J1 on the signal distribution panel.
6. Disconnect the mass storage power connector from J8.
7. Disconnect the front fan power connector and the front control panel power connector from J10 and J7. These connectors are keyed and have a locking assembly.
8. Remove the five screws holding the power supply to the chassis.

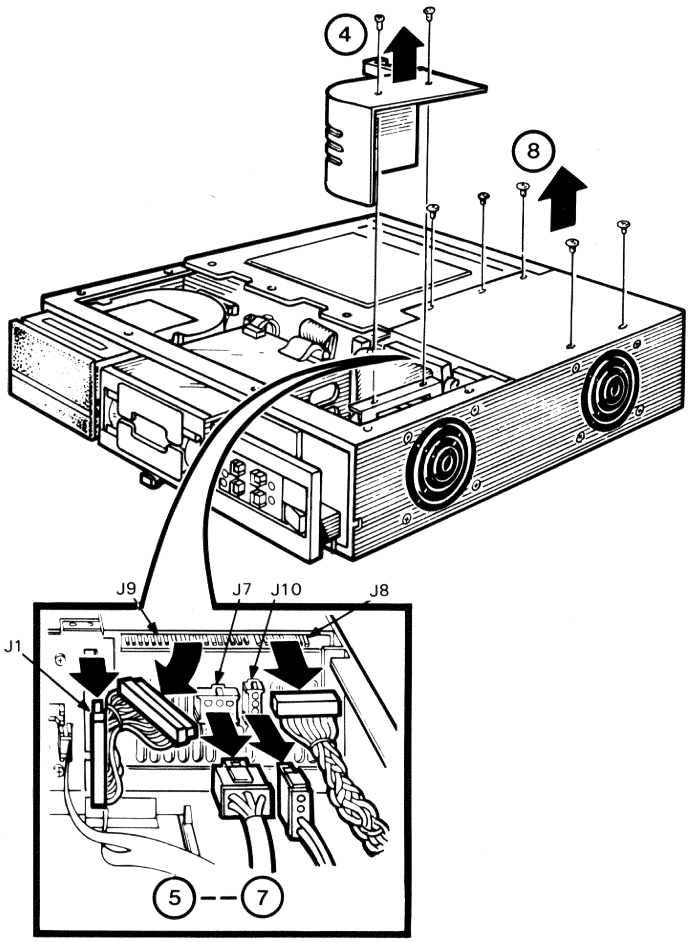



Figure 6-16 Power Supply Removal

9. Lift the power supply assembly out of the chassis and rest it on top of the Q22-Bus module cover. (Figure 6-17)
10. Disconnect the power connector from the rear cooling fan.

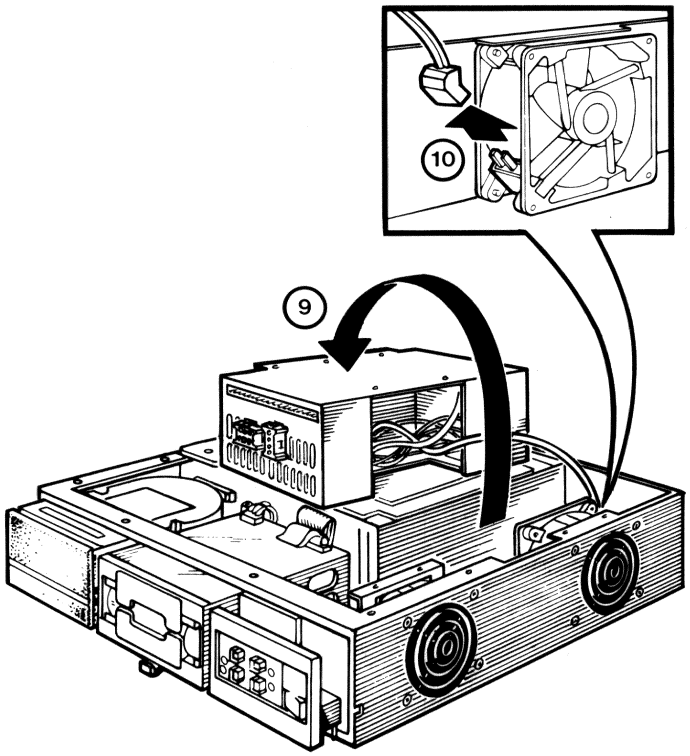



Figure 6-17 Power Supply and Fan Connector Removal

### 6.6.2 Replacement

1. Place the replacement power supply on top of the Q22-Bus module cover and connect the rear fan power cable.
2. Place the power supply in position. The rear fan power cable is not keyed. Observe the polarity of the connector. The curve of the connector must match the curve of the fan housing. (Figure 6-18) Make sure you route the rear fan cable over the top of the rear fan. (Figure 6-19)
3. Reverse steps 1 through 8 of the removal procedure to finish installing the power supply.

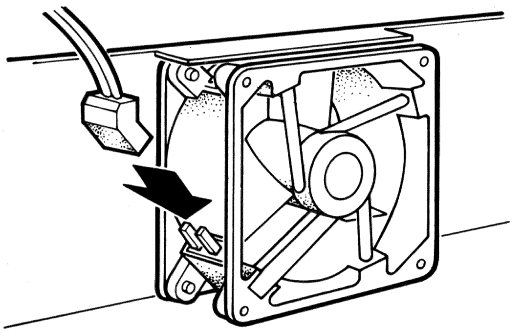


Figure 6-18 Rear Fan Connector

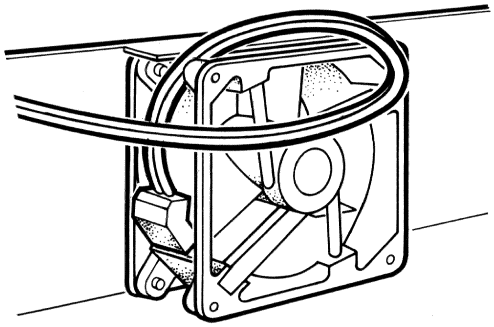


Figure 6-19 Rear Fan Cable Position

## 6.7 REAR COOLING FAN

Refer to Figure 6-20.

### 6.7.1 Removal

1. Remove the front and rear bezel and all cables.
2. Remove the rear retaining bracket and remove the subsystem from the enclosure.
3. Remove the power supply unit and disconnect the rear fan power connector. (See Paragraph 6.6.)
4. Remove the four screws and spacers that hold the fan to the chassis and remove the fan.

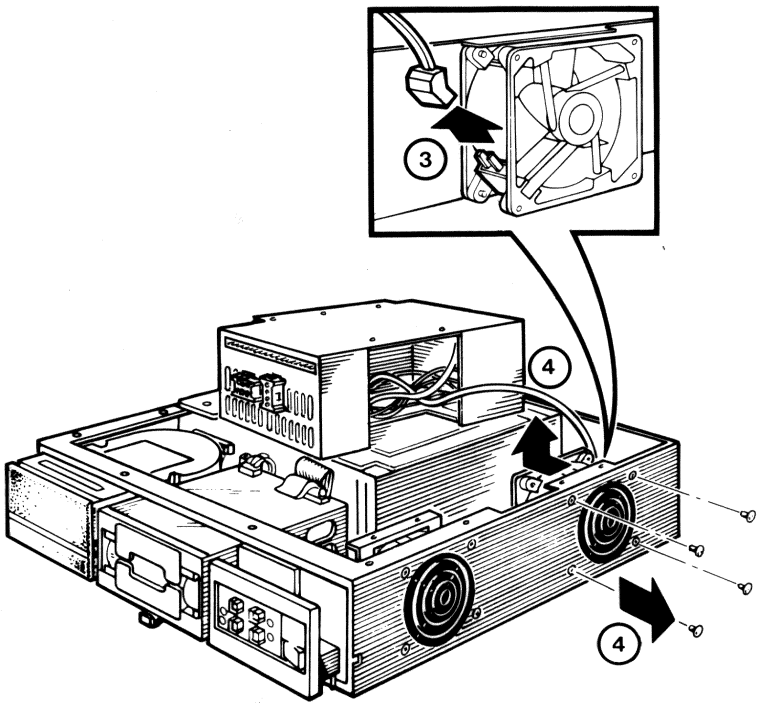



Figure 6-20 Rear Fan Removal

### 6.7.2 Replacement

Refer to Figure 6-21.

1. Relocate the four screws and place the fan guard on the screws. Make sure the cross members of the fan guard face the inside of the unit.
2. Place the spacers on the screws and secure the fan. Make sure the fan is oriented as shown. The airflow must be away from the power supply.
3. Reverse steps 1 through 3 of the removal procedure. The rear fan power cable is not keyed. Observe the polarity of the connector. The curve of the connector must match the curve of the fan housing as shown in Figure 6-19.

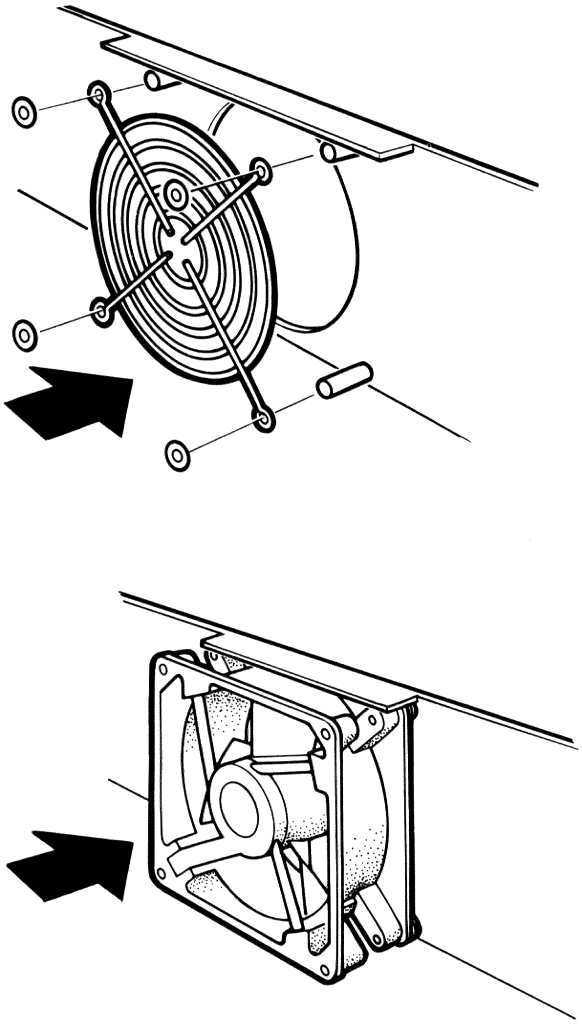


Figure 6-21 Rear Fan Replacement

## 6.8 FRONT COOLING FAN

Refer to Figure 6-22.

### 6.8.1 Removal

1. Disconnect the ac power cable and remove the front bezel.
2. Remove the front retaining bracket and push the subsystem forward.
3. Remove the subsystem storage cover.
4. If present, remove the front fan cowling.
5. Disconnect the front fan power cord from J10 on the power supply and from the fan.

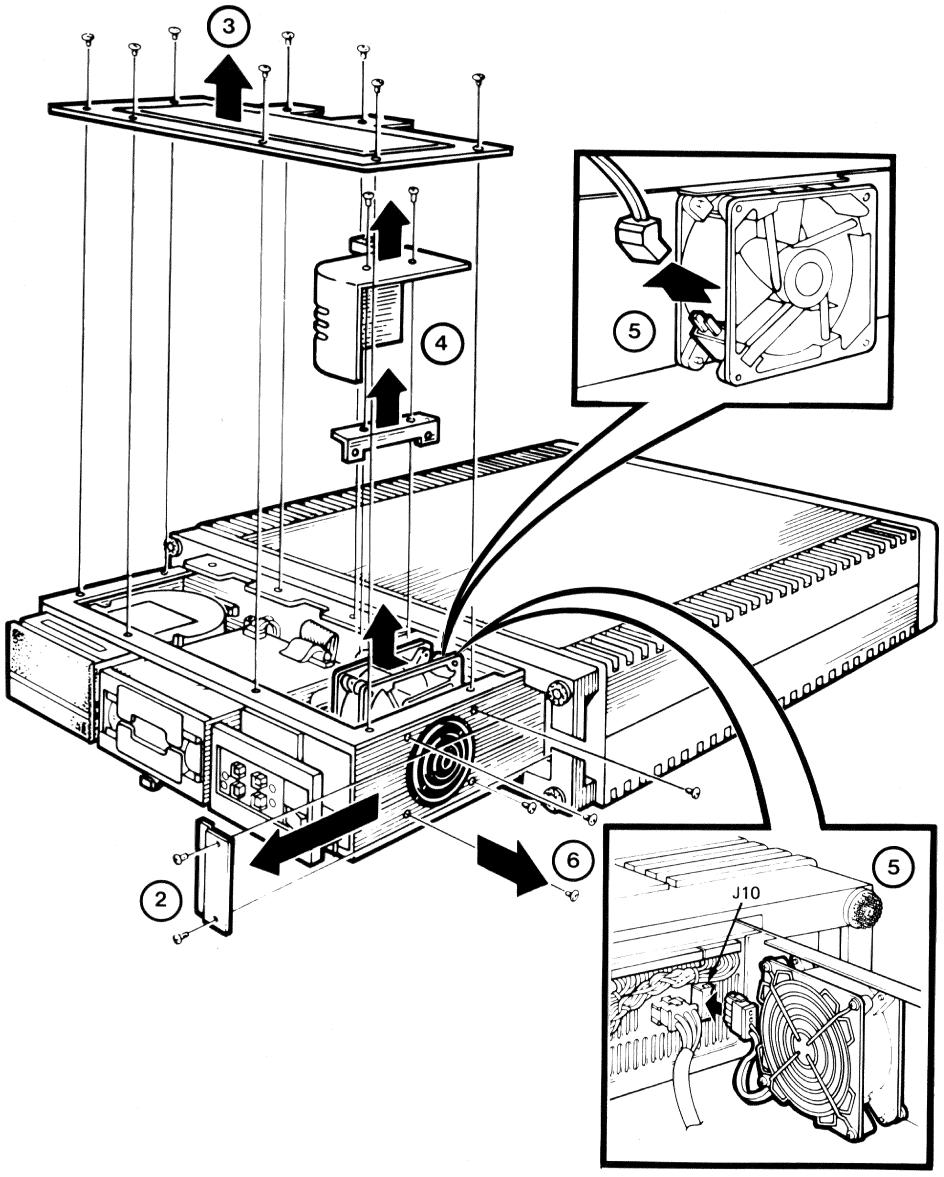



Figure 6-22 Gaining Access to the Front Fan

6. Remove the four screws and spacers that hold the fan and fan guard to the chassis, and remove the fan. (Figure 6-23)

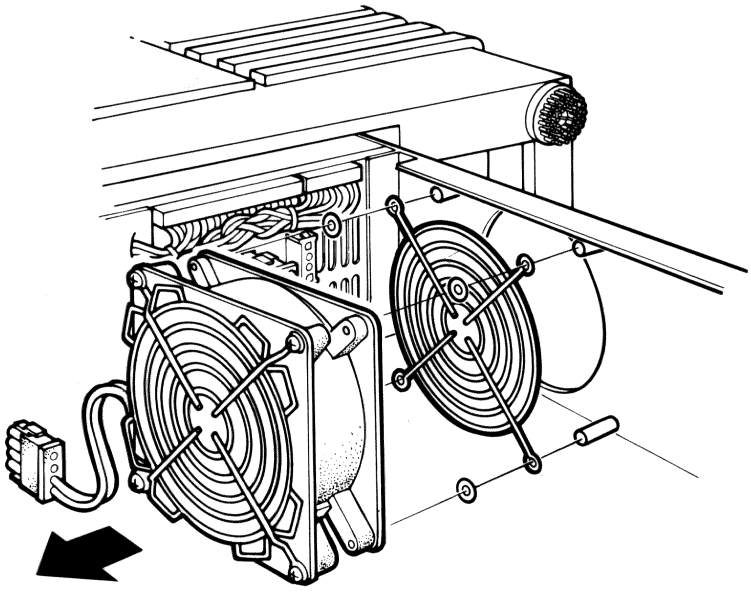


Figure 6-23 Front Fan Removal

### 6.8.2 Replacement

1. If present, remove the power cable and fan guard from the intake side of the old fan and fit them to the replacement fan. (Figure 6-24)
2. The front fan power cable is not keyed. Observe the polarity of the connector. The curve of the connector must match the curve of the fan housing as shown in Figure 6-24.

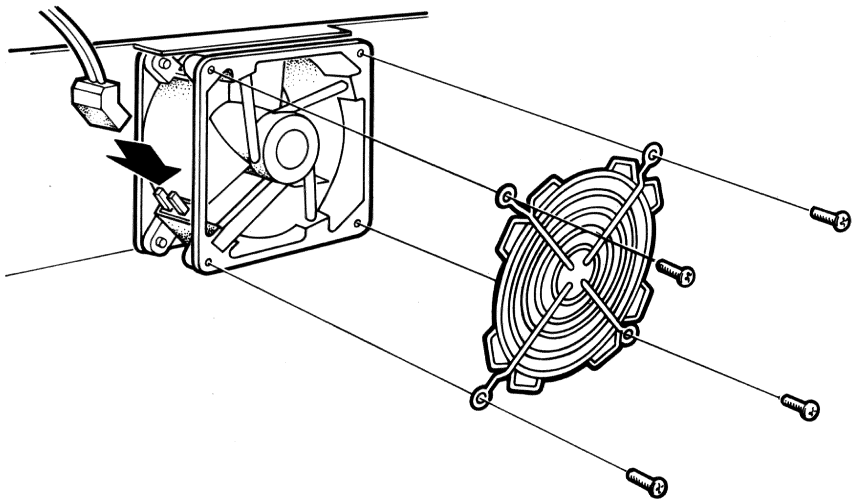


Figure 6-24 Connect Front Fan

3. Relocate the four screws and place the fan guard on the screws. Make sure the cross members of the fan guard face the inside of the unit. (Figure 6-25)
4. Place the spacers on the screws and secure the fan. Make sure the fan is oriented as shown. The airflow must be away from the mass storage area.
5. Reverse steps 1 through 6 of the removal procedure to finish installing the front cooling fan.

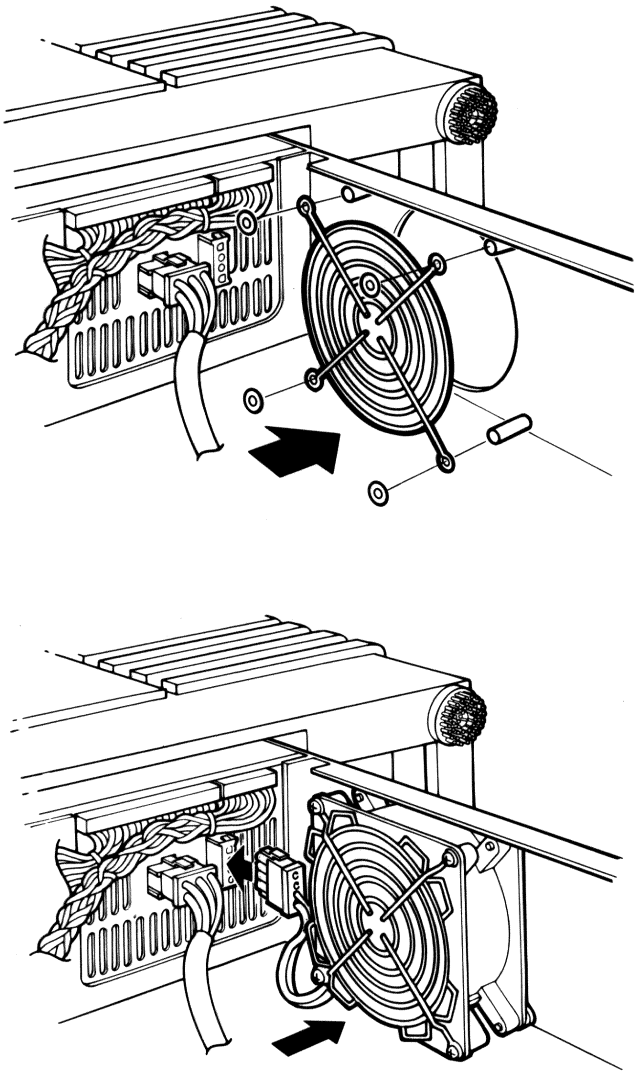


Figure 6-25 Front Fan Replacement

## 6.9 MODULES

### 6.9.1 Precautions

- Static electricity can damage semiconductor devices. Always use a grounded wrist-strap (part number 29-11762-00) and grounded work surface when handling system components and modules with exposed semiconductor devices.
- Remove and install modules carefully to prevent damage to module components, other modules, or possible changes to the switch settings.
- Replacement modules come wrapped in special antistatic packaging material. A silica gel packet is also included to prevent damage from moisture. Use this antistatic packaging material and silica gel packet to protect any modules you store, transport, or return.
- If dual-height Q22-Bus modules are installed in backplane slots 1, 2, or 3, they must occupy the AB rows.
- An MS630-AA module must occupy the CD rows of slot 1, 2, or 3.
- Dual-height modules can be installed in either the AB or CD rows of slots 4 through 8. If only one dual-height module is installed in a slot, the configuration may require an M9047 grant card in the empty half of the slot.

### 6.9.2 Removal

Refer to Figure 6-26.

1. Remove the ac power cable from the wall outlet.
2. Remove the rear bezel and all cables. Label the cables for reinstallation later.
3. Loosen the two screws retaining the rear I/O distribution panel assembly. Swing the assembly open and remove the ground-strap screws.
4. Disconnect any cables attached to the back of the I/O distribution panel assembly. Note their specific locations and the orientation of the red stripe on each cable.
5. Slide the modules partially out of the backplane and remove the cables attached to them. Note the orientation of the red stripe on each cable.

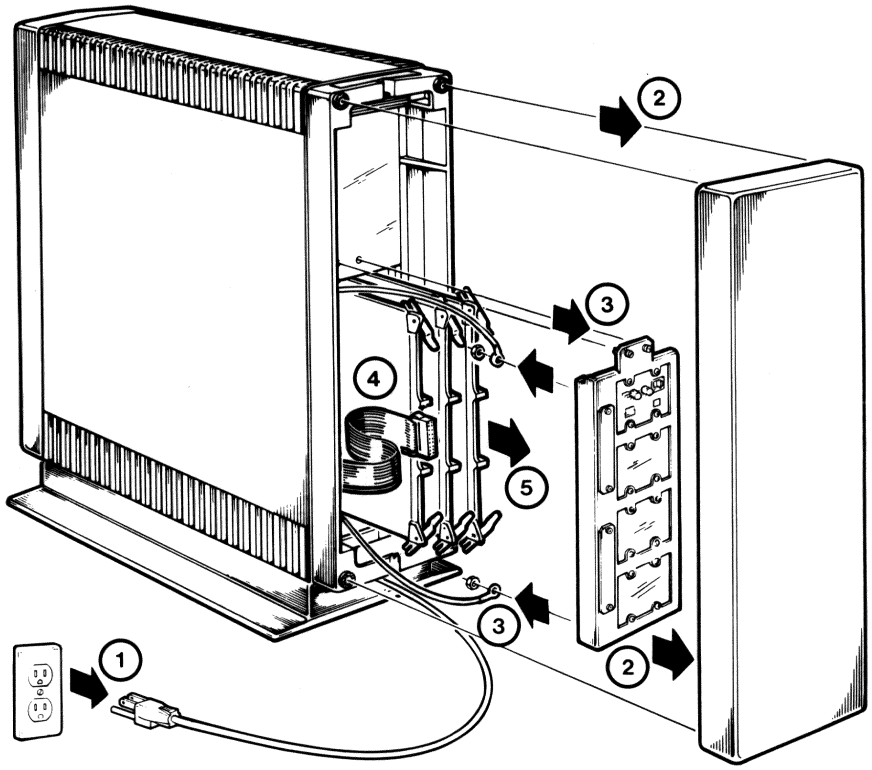



Figure 6-26 System Module Removal

6. Remove the modules from the chassis. Each Q22-Bus quad-height module has levers at each end that lock the module in place and assist in releasing the module from the backplane. (Figure 6-27)

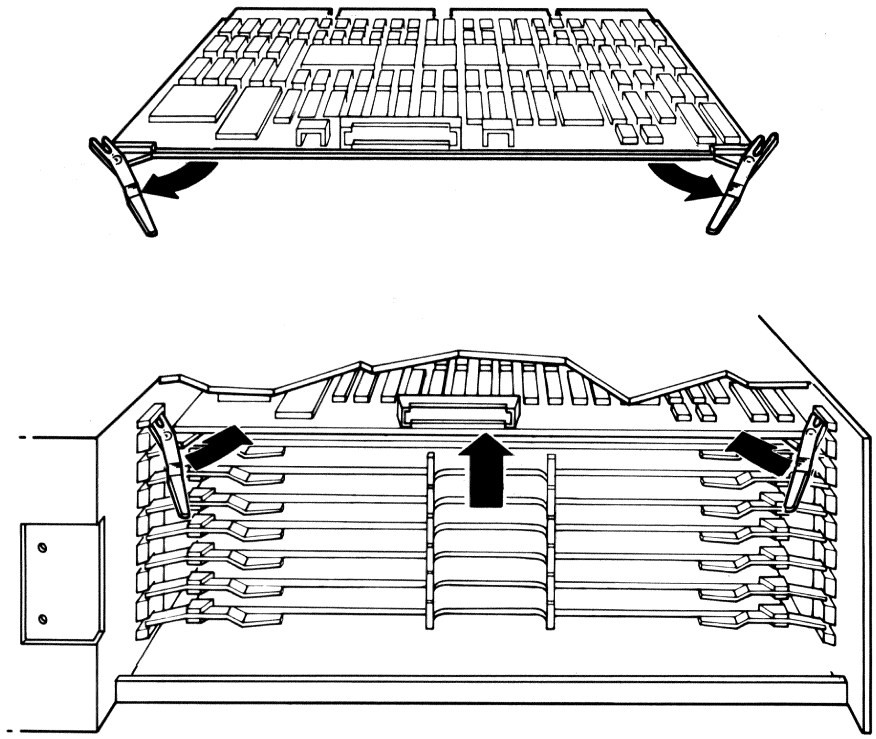


Figure 6-27 Module Locking Levers

### 6.9.3 Replacement

1. Make sure you set the jumper and switch configuration of the replacement modules correctly. Check the setting against the old module, or refer to the User's Guide or Installation Guide supplied with the new module.
2. Reverse steps 1 through 6 of the removal procedure.
3. Retest the system to confirm the system is working correctly. Refer to the Troubleshooting section of the *VAXstation II Owner's Manual, BA23 Enclosure* for instructions.

## 6.10 I/O DISTRIBUTION PANEL INSERT

### 6.10.1 Removal

Refer to Figure 6-28.

1. Remove the ac power cord from the wall outlet.
2. Remove the rear bezel and all cables attached to the panel insert that is to be removed. Label the cables for reinstallation later.
3. Loosen the two screws retaining the rear I/O distribution panel assembly. Swing the assembly open and remove the ground-strap screws.
4. Disconnect any cables attached to the panel insert. Note the orientation of the red stripe on each cable.
5. Remove the four screws holding the panel insert to the rear I/O distribution panel assembly and remove the insert.

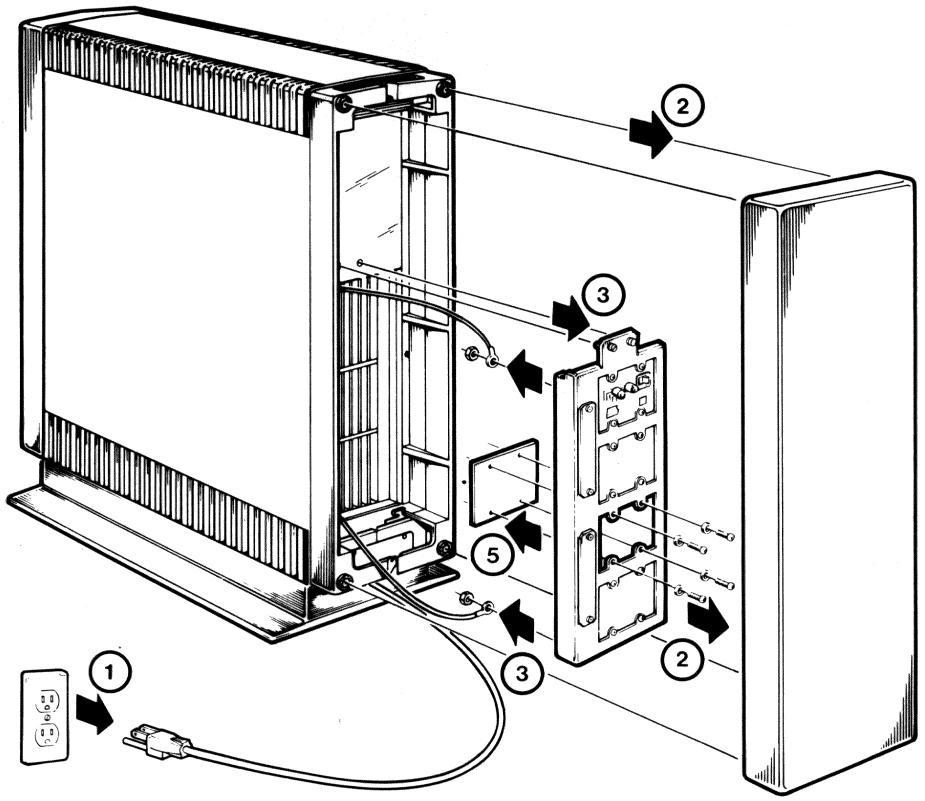



Figure 6-28 I/O Distribution Panel Insert Removal

### 6.10.2 Replacement

Reverse the removal procedure.

## 6.11 TIME-OF-YEAR CLOCK (BATTERY BACKUP UNIT)

### 6.11.1 Removal

1. Remove the ac power cord from the wall outlet.
2. Remove the rear bezel and the console terminal cable from the CPU patch panel insert. (Figure 6-29)

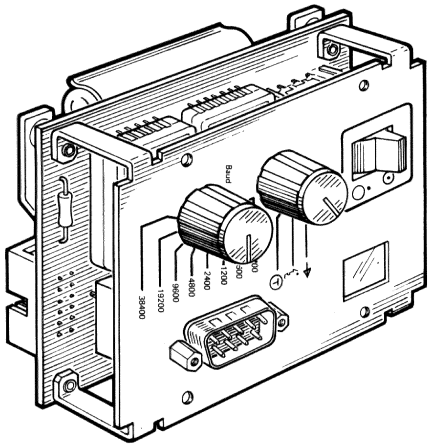



Figure 6-29 CPU Patch Panel Insert

3. Loosen the two screws retaining the rear I/O distribution panel assembly. Swing the assembly open and remove the ground-strap screws.
4. Disconnect all CPU module cables from the CPU patch panel insert. Note the orientation of the red stripe on each cable removed.
5. Remove the four screws holding the CPU patch panel insert to the rear I/O distribution panel assembly and remove the panel insert.
6. Disconnect the battery backup unit (BBU) from the CPU patch panel insert. (Figure 6-30)
7. Carefully spread the plastic BBU holder and pop the battery backup unit out. (Figure 6-31)

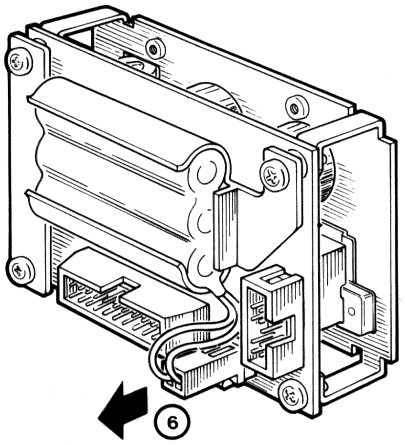



Figure 6-30 Disconnect the Battery Backup Unit

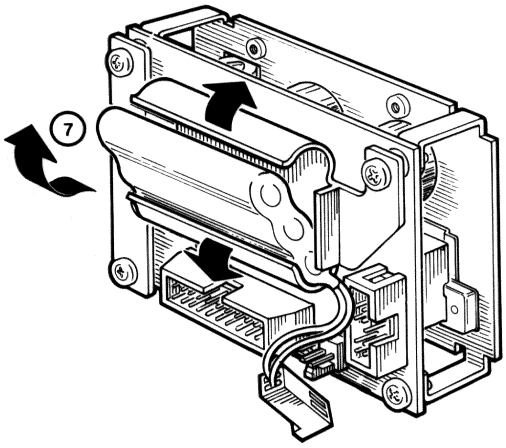



Figure 6-31 Battery Backup Unit Removal

### 6.11.2 Replacement

Reverse the removal procedure.

## 6.12 VR260 MONITOR

The VR260 monitor comprises five assemblies:

- Cover and rear bezel
- Deflection board
- CRT
- Chassis
- Power LED.

In the following procedures, the left and right sides of the monitor are at the left and right as you face the screen.

Before starting any procedure:

1. Turn off the monitor's power.
2. Remove the power cord from the monitor's rear bulkhead.
3. Remove the BC18P-10 video cable from the monitor's rear bulkhead.

**NOTE**
**All repair and adjustment procedures on the monitor should be performed by qualified Field Service personnel *only*. The procedures also require the use of special MicroVAX Maintenance Kit diagnostic software.**

### 6.12.1 Cover and Rear Bezel

#### 6.12.1.1 Removal –

1. Carefully place the monitor on its face.
2. Unscrew the four rubber feet from the bottom.
3. Remove the tilt/swivel base.
4. Remove the four screws from the enclosure's rear corners.
5. Lift off the cover.
6. Lift off the rear bezel.

**6.12.1.2 Replacement –** To replace the cover and rear bezel, reverse the removal procedure.

### 6.12.2 Deflection Board

The deflection board and left-side chassis door are removed as a unit. (Figure 6-32)

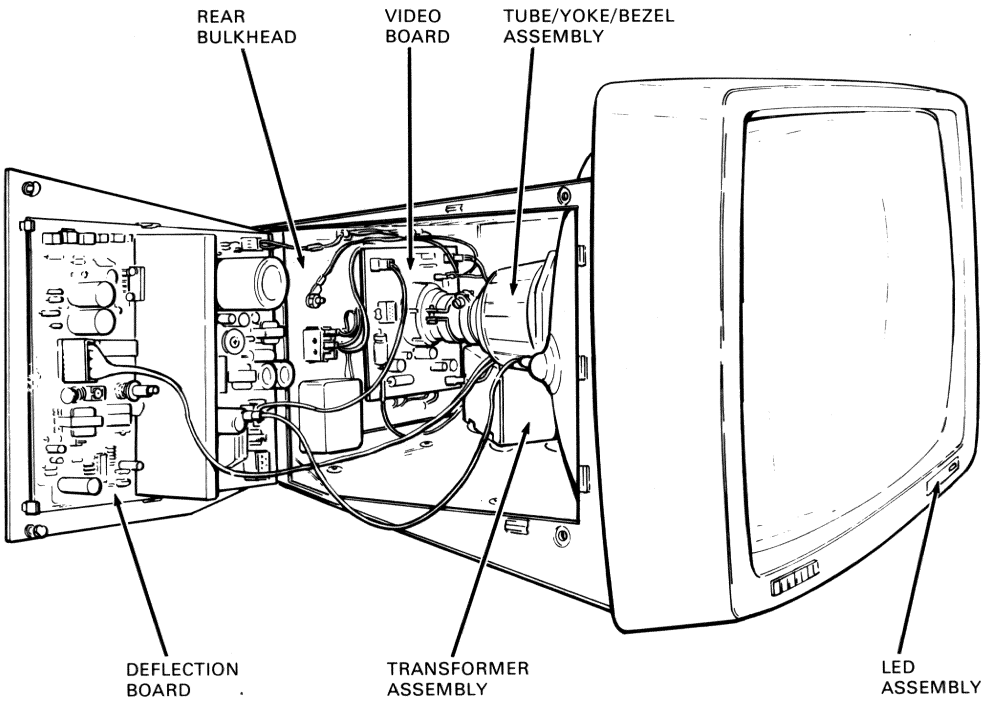



Figure 6-32 Deflection Board and Chassis Door Locations

#### 6.12.2.1 Removal –

1. Remove the monitor cover and rear bezel. (See Paragraph 6.12.1.1.)
2. Place the monitor on its bottom.
3. Loosen the two 1/4-turn fasteners at the front corners of the left-side chassis door, and open the door.
4. On the deflection board, disconnect:
   - J1 – 3-pin/2-wire power transformer connection
   - J2 – 12-pin/10-wire CRT socket board connection
   - J3 – 6-pin/4-wire CRT yoke connection
   - J4 – 1-wire slip-on ground connection
   - J5 – 3-pin/2-wire CRT socket board connection.
5. To remove the board/door assembly, lift the door up and pull it out.
6. Insert a grounded screw driver under the anode cap and make contact with the anode clip to discharge the anode.
7. Disconnect the anode lead (remove the anode cap from the CRT).
8. Remove the deflection circuit board from the six plastic clips holding it to the door.

**6.12.2.2 Replacement –** To replace the deflection board assembly, reverse the removal procedure.

### 6.12.3 CRT Assembly

The CRT assembly (Figure 6-32) is replaced as a unit and comprises the:

- CRT
- Yoke
- Socket board
- Monitor enclosure front bezel.

#### 6.12.3.1 Removal –

1. Remove the monitor cover and rear bezel. (See Paragraph 6.12.1.1.)
2. Remove the deflection board assembly. (See Paragraph 6.12.2.1.)
3. On the CRT socket board, disconnect the video input cable from J13 in the lower left corner.
4. On the chassis rear bulkhead, remove the ground wire (CRT socket board ground wire) from the upper slip-on terminal.
5. On the top front of the chassis, at its center, remove the screw that fastens the braided ground-strap between the CRT and chassis.
6. Carefully return the monitor to a face-down position.
7. At the left and right front edges of the chassis, remove the three screws fastening the CRT assembly to the side of the chassis. Lift the chassis from the CRT assembly.

**6.12.3.2 Replacement –** To replace the CRT assembly, reverse the removal procedure.

### 6.12.4 Power LED

On the front of the monitor enclosure, the green LED that indicates "power on" is held in place with double-sided, transparent, adhesive tape. (Figure 6-33)

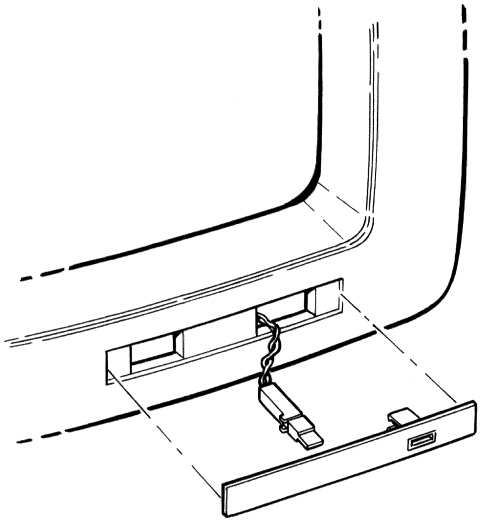


Figure 6-33 Power LED Removal/Replacement

#### 6.12.4.1 Removal –

1. Using a knife tip or similar tool, carefully pry the LED/bezel assembly free of the enclosure.
2. Disconnect the LED wires.

#### 6.12.4.2 Replacement –

1. Connect the LED wires. The black wire is connected to the notched connector leg.
2. Remove the protective paper backing from the double-sided tape on the LED/bezel assembly.
3. Press the LED/bezel assembly in place.

### 6.12.5 Monitor Alignment

The only special tools required for monitor alignment are a metric measuring tape and the diagnostic test patterns. (Figure 6-34)

Alignment should be checked and needed adjustments made after replacing either the deflection board or the CRT assembly.

All internal adjustments are accessible through appropriately labeled holes in the top and left side of the chassis.

FOCUS and G2 do not interact with any other internal adjustments. The remaining adjustments should be performed in the order listed to minimize the effects of interaction.

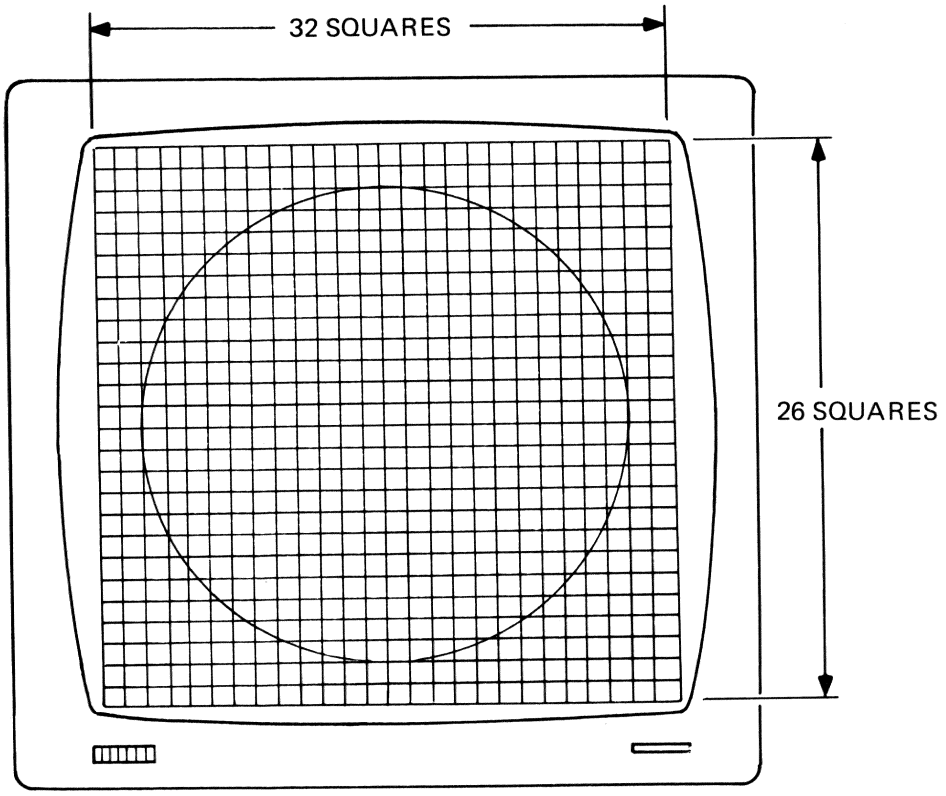



Figure 6-34 Monitor Alignment Patterns

1. Turn the monitor's and system's power on.
2. Set the monitor's BRIGHTNESS and CONTRAST controls to their maximum positions.
3. After 30 seconds, adjust BRIGHTNESS until the raster disappears.
4. Adjust CONTRAST for the best picture.
5. Run the display adjustment diagnostic and select the circle cross-hatch pattern.
   a. Set BRIGHTNESS to a viewing level.
   b. Set CONTRAST to extinguish the raster.
   c. On the left side of the chassis (Figure 6-35), adjust LIN (horizontal linearity) for horizontally uniform squares across the display. Note that the display size should be near or at maximum, and positioned toward the left of the screen.
   d. On the top of the chassis (Figure 6-36), adjust VL (vertical linearity) for vertically uniform squares.
   e. On the top of the chassis (Figure 6-37), adjust FOCUS for best vertical/horizontal line convergence. Use cross-hatch pattern intersections approximately three squares toward the center from any screen corner.

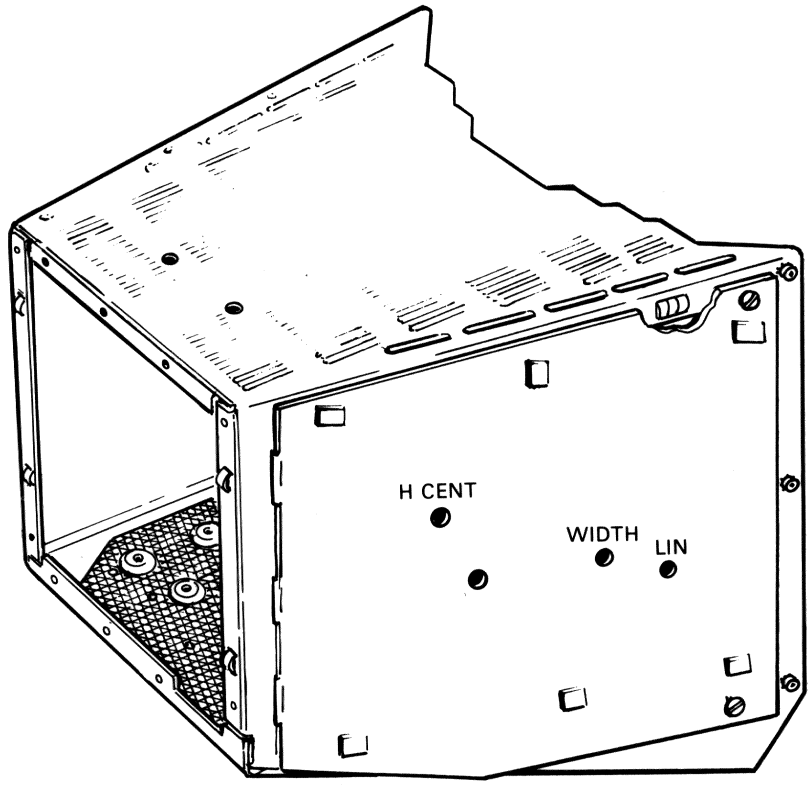



Figure 6-35 VR260 Monitor Adjustments (H CENT, WIDTH, and LIN)

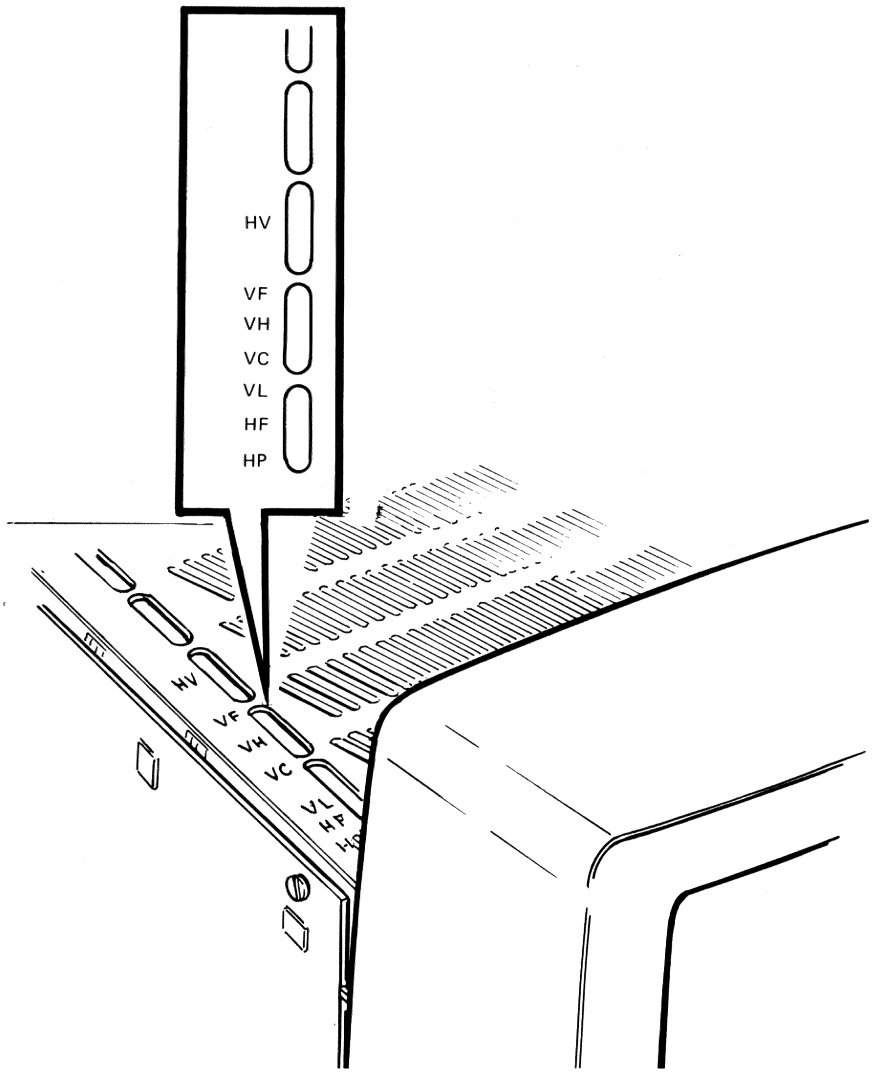



Figure 6-36 VR260 Monitor Adjustments (Top)

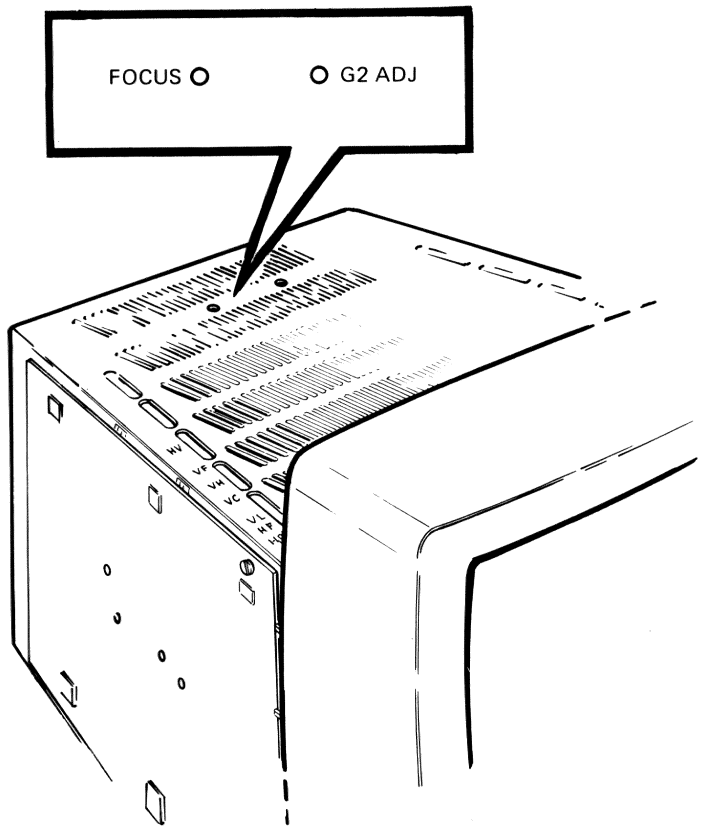



Figure 6-37 VR260 Monitor Adjustments (FOCUS and G2)

6. Select an all white screen.
   a. Adjust CONTRAST and BRIGHTNESS for normal viewing with a visible raster.
   b. On the left side of the chassis, adjust H CENT (horizontal centering) for a centered raster.
   c. On the top of the chassis, adjust HP (horizontal phase) to center the video in the raster.
   d. Adjust BRIGHTNESS to extinguish the raster.
   e. Set CONTRAST to a normal viewing level.

f. On the left side of the chassis, adjust WIDTH for a display width of 334 mm.

g. On the top of the chassis, adjust VH (vertical height) and VC (vertical centering) so that the display touches both the top and bottom edges of the screen.

h. Set VH for a display height of 282 mm.

7. Select the circle cross-hatch pattern.

   a. Check the vertical and horizontal linearity of the squares. Readjust if needed.

   b. Check the vertical and horizontal centering, height, and width of the squares. Readjust if needed.

   c. Check G2:

      1) Set CONTRAST to minimum and BRIGHTNESS to maximum. A raster should be faintly visible.

      2) If no raster is visible, adjust G2 until a raster is faintly visible.

# Appendix A
# Console Commands

## A.1 CONSOLE COMMAND SYNTAX

The console terminal accepts commands up to 80 characters long. Longer commands result in error messages. The character count does not include rub-outs, rubbed-out characters, or the terminating <RETURN>.

You can abbreviate a command by dropping characters from the end of its keyword. However, it is necessary to supply enough letters of the keyword for the system to distinguish one command from another.

The console treats multiple, adjacent spaces and tabs as a single space. Leading and trailing spaces and tabs are ignored. Command qualifiers can appear after the command keyword, or after any symbol or number in the command.

All numbers (addresses, data, counts) are hexadecimal; but, symbolic register names include decimal digits. The hexadecimal digits are:

0 1 2 3 4 5 6 7 8 9 A B C D E F

The console accepts both upper- and lowercase letters in hexadecimal numbers (A through F) and commands.

## A.2 REFERENCES TO PROCESSOR REGISTERS AND MEMORY

The KA630-A console mode is implemented in macrocode executed from ROM. For this reason, the actual processor registers cannot be modified by the command interpreter. When console I/O mode is entered, the console saves the processor registers in a scratch page, and all command references to them are directed to the corresponding scratch page locations, not to the registers themselves. When the console returns to program mode, the saved registers are restored. It is only then that changes take effect. References to processor memory are handled normally, except where noted below.

Normally, the scratch page is a free page on the interrupt stack, so the console does not modify the machine state. If a free page on the interrupt stack cannot be located, the console program uses the last valid page in contiguous physical memory, and the original machine state is lost. Normally, this should occur only upon power-up.

EXAMINE and DEPOSIT command references to the console scratch page must be qualified by the "/U" qualifier. (Access is primarily to simplify console program debugging.) The BINARY LOAD and UNLOAD commands may not reference the console scratch page.

## A.3 CONSOLE COMMANDS

### A.3.1 BINARY LOAD and UNLOAD

X <address> <count> <RETURN> <checksum>

The X command is used by automatic systems communicating with the console. It is not intended for operator use. The console loads or unloads (that is, writes or reads memory) the specified number of data bytes, starting at the specified address.

If count bit 31 is clear, the console is to receive data and deposit it in memory. If count bit 31 is set, the console is to read data from memory and send it. The remaining count bits are the number (positive) of bytes to load or unload.

The console accepts the command when it receives the <RETURN>. The next byte the console receives is the command checksum, which is note echoed. The command checksum is verified by adding all command characters, including the checksum (but not including the terminating <RETURN>, rub-outs, or characters deleted by rub-out), into an 8-bit register that is initially set to zero. If no errors occur, the result is zero. If the command checksum is correct, the console responds with the input prompt, and either sends data to the requester or prepares to receive data. If the command checksum is in error, the console responds with an error message. The intent is to prevent the operator from inadvertently entering a mode where the console is accepting keyboard characters as data, with no possible escape sequence.

For a BINARY LOAD command (count bit 31 is clear), the console responds with the input prompt, then accepts the specified number of data bytes to deposit into memory, and an additional byte of received data checksum. The data is verified by adding all data characters and the checksum character into an 8-bit register initially set to zero. If the final register content is not zero, the data or checksum is in error, and the console responds with an error message.

For a BINARY UNLOAD command (count bit 31 is set), the console responds with the input prompt, followed by the specified number of binary data bytes. As each byte is sent, it is added to a checksum register initially set to zero. At the end of the transmission, the 2's complement of the low byte of the register is sent.

If the data checksum is incorrect on a load, or if memory or line errors occur during the data transmission, the transmission is completed before the console issues an error message. If an error occurs during loading, the loaded memory contents are *unpredictable.*

Echo is suppressed during the data string and checksum reception.

During a BINARY UNLOAD, the console can be controlled with control characters (<CTRL>C, <CTRL>S, <CTRL>O, etc.). The same control is not possible during a BINARY LOAD because all received characters are valid binary data.

Data being loaded with a BINARY LOAD command must be received by the console at a rate of 1 byte/s or higher. Within 10 seconds of the <RETURN> terminating the command line, the console must receive the command checksum preceding the data. Within 10 seconds of the last data byte, the data checksum must be received. If any of these timing requirements are not met, the console aborts the transmission by issuing an error message and prompting for input.

The entire command, including the checksum, may be sent to the console as a single burst of characters at the console's specified character rate. The console is able to receive at least 4 Kbytes of data in a single X command.

### A.3.2 BOOT

BOOT [<qualifier list>] [<device>]

The device specification format is "ddcu", where "dd" is a 2-letter device mnemonic, "c" is an optional 1-digit controller number, and "u" is a 1-digit unit number.

The console initializes the processor and starts VMB running. VMB boots the operating system from the specified or default device.

Qualifier:

- /R5:<data> – After initializing the processor and before starting VMB, R5 is loaded with the specified data. This allows a console user to pass a parameter to VMB. (To remain compatible with previous processors, /<data> will also be recognized to have the same result.)

### A.3.3 COMMENT

! <comment>

The comment command (exclamation point) is ignored. It is used to annotate console I/O command sequences.

### A.3.4 CONTINUE

CONTINUE

The processor begins instruction execution at the address currently contained in the program counter. Processor initialization is not performed. The console enters program I/O mode.

### A.3.5 DEPOSIT

DEPOSIT [<qualifier list>] <address> <data>

Deposits the data into the specified address. If no address space or data size qualifiers are specified, the defaults are the last address space and data size used in a DEPOSIT or EXAMINE command. After processor initialization, the default address space is physical memory, the default data size is long, and the default address is zero.

If the specified data is too large to fit in the data size to be deposited, the console ignores the command and issues an error response. If the specified data is smaller than the data size to be deposited, it is extended on the left with zeros. The address may also be one of the following symbolic addresses.

- PSL – (Processor status longword) No address space qualifier is legal. When PSL is examined, the address space is identified as "M" (machine-dependent).
- PC – (Program counter – General register 15) The address space is set to /G (defined below).
- SP – (Stack pointer – General register 14) The address space is /G.
- Rn – (General register n) The register number is in decimal. The address space is /G. For example:

  D R5 1234 is equivalent to D/G 5 1234
  D R10 6FF00 is equivalent to D/G A 6FF00

- + - (plus sign) The location immediately following the last location referenced in an EXAMINE or DEPOSIT. For references to physical or virtual memory spaces, the location referenced is the last address, plus the size of the last reference (1 for byte, 2 for word, 4 for long). For other address spaces, the address is the last address referenced, plus one.
- – - (minus sign) The location immediately preceding the last location referenced in an EXAMINE or DEPOSIT. For references to physical or virtual memory spaces, the location referenced is the last address minus the size of this reference (1 for byte, 2 for word, 4 for long). For other address spaces, the address is the last address referenced, minus one.
- * - (asterisk) The location last referenced in an EXAMINE or DEPOSIT.
- @ - (at sign) The location addressed by the last location referenced in an EXAMINE or DEPOSIT.

Qualifiers:

- /B - The data size is byte.
- /W - The data size is word.
- /L - The data size is longword.
- /V - The address space is virtual memory. All access and protection checking occurs. If the access would not be allowed to a program running with the current PSL, the console issues an error message. Virtual space DEPOSITs cause the PTE<M> bit to be set. If memory mapping is not enabled, virtual addresses are equal to physical addresses.
- /P - The address space is physical memory.
- /I - The address space is internal processor registers. These are the registers addressed by the MTPR and MFPR instructions.
- /G - The address space is the general register set, R0 through PC (R15).
- /U - Access to console program memory is allowed. This qualifier also disables virtual address protection checks.
- /N:<count> - The address is the first of a range. The console deposits to the first address, then to the specified number of succeeding addresses. Even if the address is the symbolic address "–", the succeeding addresses are at larger addresses. The symbolic address specifies only the starting address, not the direction of succession. For repeated references to preceding addresses, use "REPEAT DEPOSIT – <data>".

**NOTE**
**Only memory can be accessed as bytes or words. Registers, the PSL, and the IPRs must be accessed using the longword reference. This means that the /B and /W qualifiers cannot be used with the /I and /G qualifiers.**

For example:

| | |
|---|---|
| D/P/B/N:1FF 0 0 | Clears the first 512 bytes of physical memory. |
| D/V/L/N:3 1234 5 | Deposits 5 into four longwords starting at virtual address 1234. |
| D/N:8 R0 FFFFFFFF | Loads general registers R0 through R8 with −1s. |
| D/N:200 − 0 | Starting at previous address, clear 513 bytes. |

If conflicting address space or data sizes are specified, the console ignores the command and issues an error response.

### A.3.6 EXAMINE

EXAMINE [<qualifier list>] [<address>]

Examines the contents of the specified address. If no address is specified, "+" is assumed. The address may also be one of the symbolic addresses described under DEPOSIT.

Qualifiers:

- EXAMINE can use the same qualifiers as DEPOSIT
- RESPONSE: <tab> <address space identifier> <address> <tab> <data>

The address space identifier can be:

- P – Physical memory. Note that when virtual memory is examined, the address space and address in the response are the translated physical address.
- G – General register.
- I – Internal processor register.
- M – Machine-dependent (used only for display of the PSL).

### A.3.7 FIND

FIND [<qualifier list>]

The console searches main memory starting at address zero for a page-aligned 64-Kbyte segment of good memory, or an RPB (restart parameter block). If the segment or block is found, its address plus 512 is left in SP. If the segment or block is not found, an error message is issued, and the contents of SP are *unpredictable.* If no qualifier is specified, /RPB is assumed.

Qualifiers:

- /MEMORY – Search memory for a page-aligned 64-Kbyte segment of good memory. The search includes a read/write test of memory and leaves the contents of memory *unpredictable.*
- /RPB – Search memory for a restart parameter block. The search leaves the contents of memory unchanged.

### A.3.8 INITIALIZE

INITIALIZE

A processor initialization is performed. The following registers are set (all values are hexadecimal).

| | |
|---|---|
| PSL | 041F0000 |
| IPL | 1F |
| ASTLVL | 4 |
| SISR | 0 |
| ICCS | 0 |
| RXCS | 0 |
| TXCS | 80 |
| MAPEN | 0 |

All other registers are *unpredictable.*

The previous console reference defaults (the defaults used to fill in unsupplied qualifiers for DEPOSIT and EXAMINE commands) are set to physical address, longword size, and address 0.

### A.3.9 HALT

HALT

The HALT command has no effect; the processor is already halted when in console I/O mode.

### A.3.10 REPEAT

REPEAT <command>

The console repeatedly displays and executes the specified command. The repeating is stopped when the operator types <CTRL>C. Any valid console command may be specified for the command, with the exception of the REPEAT command.

### A.3.11 START

START [<address>]

The console starts instruction execution at the specified address. If no address is given, the current PC is used. If no qualifier is present, macroinstruction execution is started. If memory mapping is enabled, macroinstructions are executed from virtual memory. The START command is equivalent to a DEPOSIT to PC, followed by a CONTINUE. No INITIALIZE is performed.

### A.3.12 TEST

TEST [<test number>]

The console invokes a diagnostic test program denoted by <test number>. Valid hexadecimal test numbers are 3 through 7, and B. If a test number is not supplied, no test is performed.

### A.3.13 UNJAM

UNJAM

An I/O bus reset is performed.

# Appendix B
# Console Error Messages and Explanations

**Table B-1 Console Error Messages**

| Hex Value | Message | Explanation |
|---|---|---|
| 02 | EXT HLT | <BREAK> was typed at the console; QBINIT or QHALT was asserted. |
| 04 | ISP ERR | Caused by attempt to push interrupt or exception state onto the interrrupt stack; when the interrupt stack is mapped NO ACCESS or NOT VALID. |
| 05 | DBL ERR | A second machine check occurred while the processor was attempting to report a machine check to the operating system. |
| 06 | HLT INST | The processor executed a HALT instruction in kernel mode. |
| 07 | SCB ERR3 | Vector bits <1:0> = 3. |
| 08 | SCB ERR2 | Vector bits <1:0> = 2. |
| 0A | CHM FR ISTK | A change mode instruction was executed when PSL<IS> was set. |
| 0B | CHM TO ISTK | Exception vector bit <0> was set for a change mode. |
| 0C | SCB RD ERR | A hard memory error occurred during a processor read of an exception or interrupt vector. |
| 10 | MCHK AV | An access violation or invalid translation occurred during machine check exception processing. |
| 11 | KSP AV | An access violation or invalid translation occurred during invalid kernel stack pointer exception processing. |

**Table B-1 Console Error Messages (Cont.)**

| Hex Value | Message | Explanation |
|---|---|---|
| 15 | CORRPTN | The console data base was corrupted. The console simulates a power-up sequence and rebuilds its data base. |
| 16 | ILL REF | The requested reference would violate virtual memory protection, address is not mapped, is invalid in the specified address space, or value is invalid in the specified destination. |
| 17 | ILL CMD | The command string cannot be parsed. |
| 18 | INV DGT | A number has an invalid digit. |
| 19 | LTL | The command was too large for the console to buffer. The message is issued only after the <RETURN> terminating the command is received. |
| 1A | ILL ADR | The specified address is not in the address space. |
| 1B | VAL TOO LRG | The specified value does not fit in the destination. |
| 1C | SW CONF | For example, an EXAMINE command specifies two different data sizes. |
| 1D | UNK SW | The switch is not recognized. |
| 1E | UNK SYM | The EXAMINE or DEPOSIT symbolic address is not recognized. |
| 1F | CHKSM | An X command's command or data checksum is incorrect. If the data checksum is incorrect, this message is issued, and is not abbreviated to "Illegal command." |
| 20 | HLTED | The operator entered a HALT command. |
| 21 | FND ERR | A FIND command failed to find either the RPB or 64 Kbytes of good memory. |
| 22 | TMOUT | Data failed to arrive in the expected time during an X command. |
| 23 | MEM ERR | Parity error detected. |
| 24 | UNXINT | An unexpected interrupt or exception occurred. |
| 40 | NOSUCHDEV | No bootable devices found. |
| 41 | DEVASSIGN | Device is not present. |

**Table B-1 Console Error Messages (Cont.)**

| Hex Value | Message | Explanation |
|---|---|---|
| 42 | NOSUCHFILE | Program image not found. |
| 43 | FILESTRUCT | Invalid boot device file structure. |
| 44 | BADCHKSUM | Bad checksum on header file. |
| 45 | BADFILEHDR | Bad file header. |
| 46 | BADIRECTORY | Bad directory file. |
| 47 | FILNOTCNTG | Invalid program image file. |
| 48 | ENDOFFILE | Premature end-of-file encountered. |
| 49 | BADFILENAME | Bad file name given. |
| 4A | BUFFEROVF | Program image does not fit in available memory. |
| 4B | CTRLERR | Boot device I/O error. |
| 4C | DEVINACT | Failed to initialize boot device. |
| 4D | DEVOFFLINE | Device is off-line. |
| 4E | MEMERR | Memory initialization error. |
| 4F | SCBINT | Unexpected SCB exception or machine check. |
| 50 | SCBZNDINT | Unexpected exception after starting program image. |
| 51 | NOROM | No valid ROM image found. |
| 52 | NOSUCHNODE | No response from load server. |
| 53 | INSFMAPREG | Invalid memory configuration. |
| 54 | RETRY | No devices bootable, retrying. |

# Appendix C
# VCB01 Video Controller Module

This appendix has two major sections. Section C.1 is a functional description of the VCB01 video controller module's hardware. Section C.2, which contains programming information, describes the programmable functions of the VCB01; that is, the functions that can be specified and/or examined by software.

## C.1 HARDWARE

### C.1.1 Overview

Figure C-1 is a simplified block diagram of the VCB01 module, showing its major functional areas, excluding its connections with the power supply and timing generator. Figure C-2 is a functional block diagram of the VCB01, showing its major address and data paths. The following sections describe the functional operation of each major area.

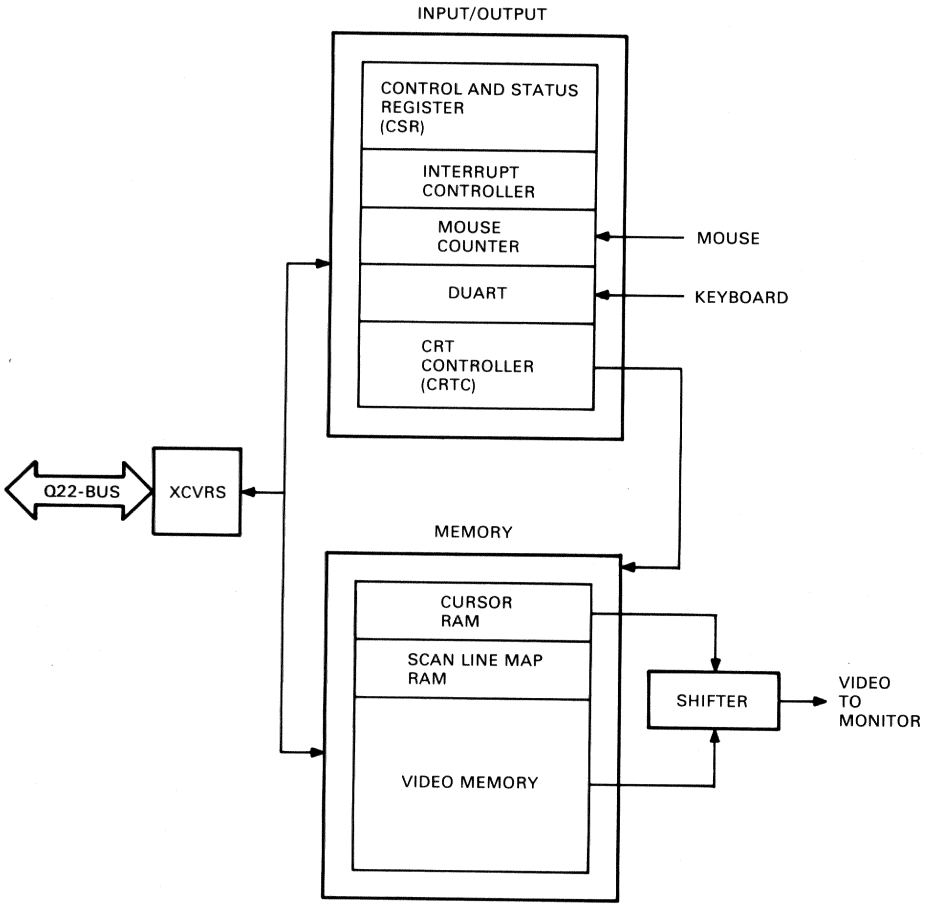



Figure C-1 VCB01 Module, Simplified Block Diagram

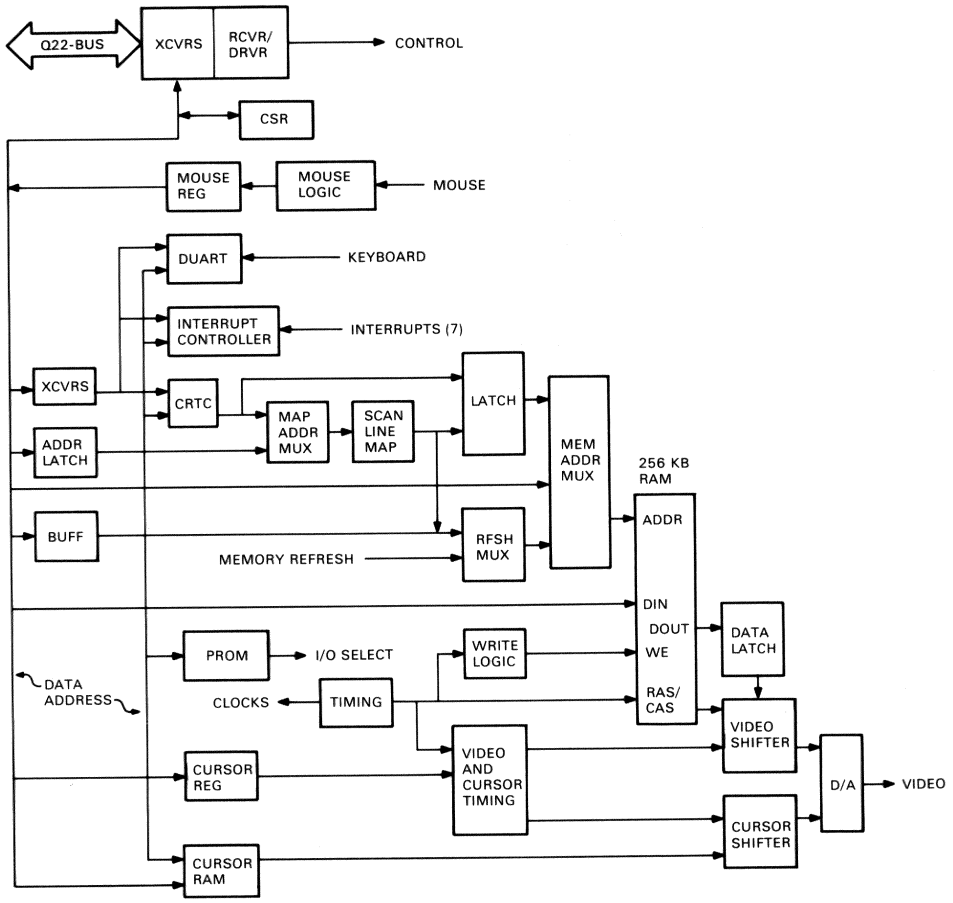



Figure C-2 VCB01 Module, Functional Block Diagram

### C.1.2 Timing

Refer to Figure C-3. Basic timing for the VCB01 is provided by an on-board 69.1968 MHz oscillator, providing a 14.45 ns clock. (An alternate on-board 32 MHz oscillator is not used.) This frequency is divided through a pair of flip-flops and a counter to generate the clocks listed in Table C-1. A timing PAL (programmable logic array) uses these clocks to generate the CRTC (CRT controller) clock input as well as timing for other functions. (For more on CRTC timing, see Paragraph C.1.4.1.)

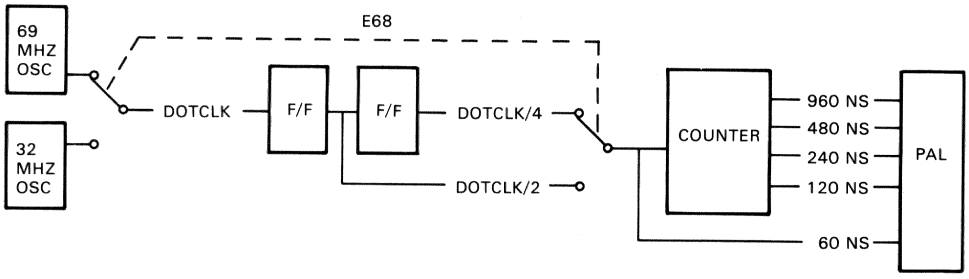



Figure C-3 VCB01 Module, Simplified Timing Generator

**Table C-1 VCB01 Clocks**

| Name | Period (ns) Actual | Nominal |
|---|---|---|
| D12DOTCLK | 14.45 | 15.0 |
| D10DOTCLK/2 | 28.90 | 30.0 |
| D12DOTCLK/4 | 57.80 | 60.0 |
| D1260NS | 57.80 | 60.0 |
| D11120NS | 115.60 | 115.5 |
| D11240NS | 231.20 | 231.0 |
| D11480NS | 462.40 | 462.5 |
| D11960NS | 924.80 | 925.0 |

Another on-board oscillator provides a 3.7 MHz clock to the keyboard/auxiliary DUART (dual universal asynchronous receiver/transmitter).

**NOTE – Nominal Values**
**In most cases, the following descriptions and explanations rely on the nominal values listed in Table C-1.**

### C.1.3 Q22-Bus/CPU Interface

The VCB01 interface to the Q22-Bus uses standard DC005 transceivers and a DC004 protocol chip, and a 9519A interrupt controller. (Figure C-4) The interface supports the following.

- Write word — DATO
- Read word — DATI
- Read/modify/write word — DATIO
- Write byte — DATOB
- Write block — DATBO
- Read block — DATBI
- Read interrupt vector

The VCB01 can perform a block data transfer of up to two words. The block must be longword-aligned (BDAL<01:00> = 0).

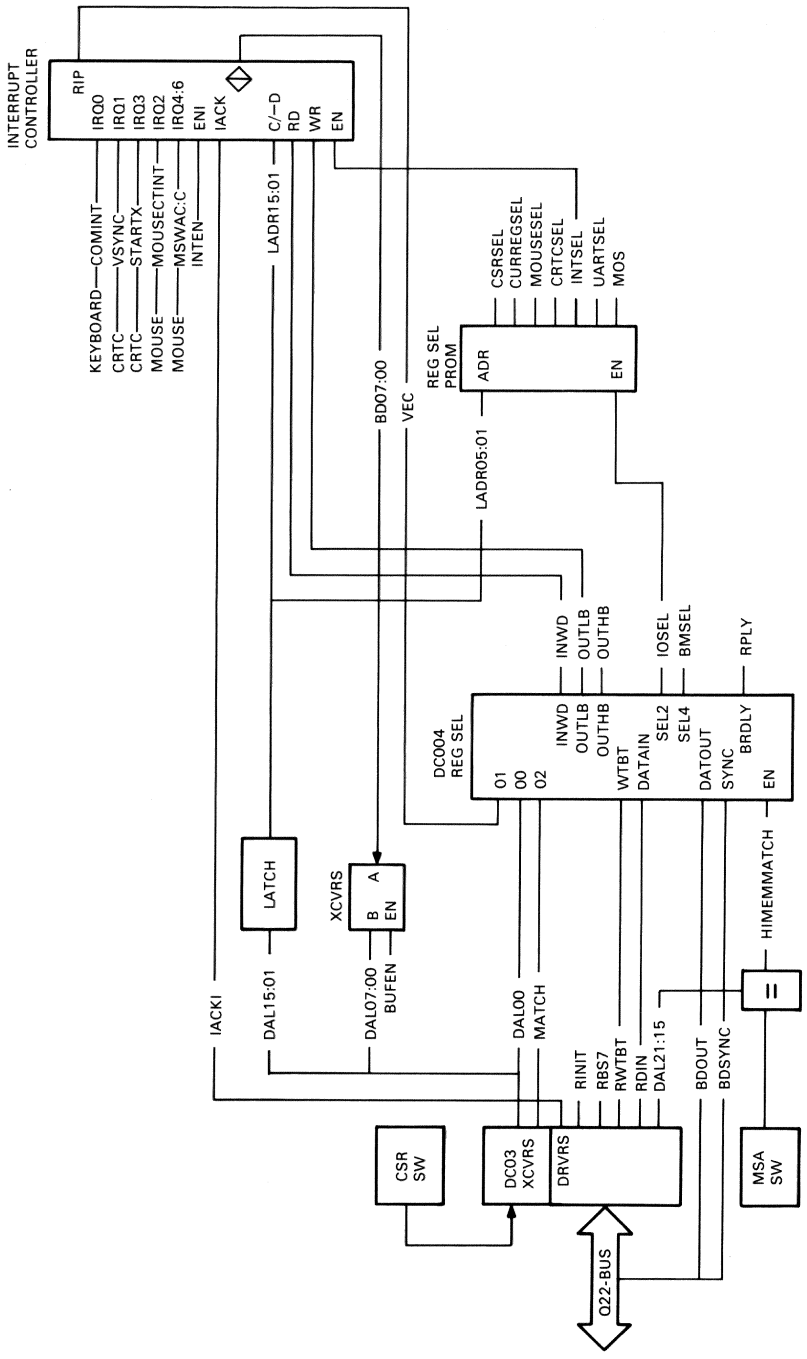



Figure C-4 VCB01 Q22-Bus Interface

**C.1.3.1 Interrupt Controller –** The 9519A interrupt controller handles eight interrupt requests on priority levels 0 (highest) to 7 (lowest):

0 – DUART

1 – Vertical sync

2 – Mouse

3 – Cursor start

4 – Mouse button A

5 – Mouse button B

6 – Mouse button C

7 – (Spare)

A set of internal registers control specific features of interrupt controller operation. The registers are described in section C.2.

Figure C-4 shows the control and data paths for the interrupt controller. Each interrupt level has its own vector, stored in the controller's internal 8 × 32 response memory. When an interrupt is requested on any level, the group interrupt (GINT) signal asserts BIRQ4. When the CPU acknowledges the request, the controller selects the highest priority request, asserts RIP (response in process), and outputs the vector on BDAL<07:00>.

**C.1.3.2 Registers –** Control and status information is exchanged between the VCB01 and the CPU through hardware registers and 32 16-bit locations in the I/O Page. These 32 locations are described in Section C.2. (See Table C-3.)

**CSR –** Figure C-5 shows the read and write paths for the CSR. Note that the CSR comprises separate input and output registers. (See Table C-4 for bit descriptions.) The input register data comes from BDAL<06:02>. The CSR output register returns CSR bit status on BDAL<10:06,04:02>.

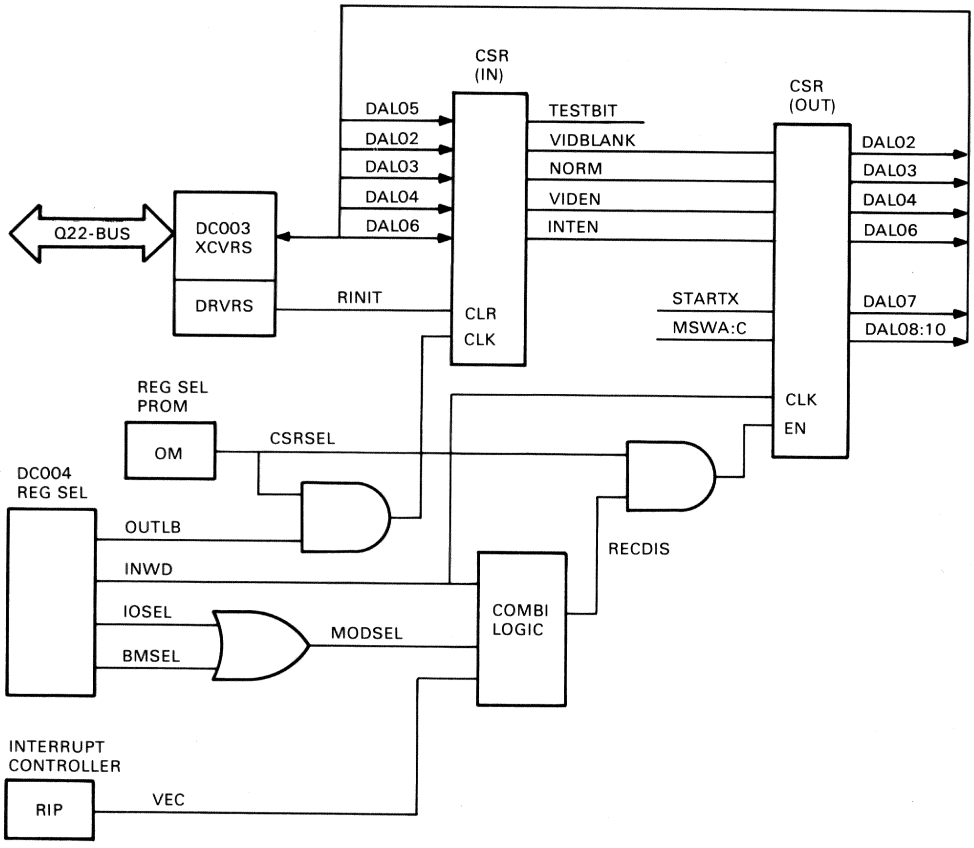



Figure C-5 VCB01 CSR Read/Write Paths

### C.1.4 CRTC

The CRT controller generates CRT (cathode-ray tube) timing, video refresh addresses, and controls cursor position. The CRTC is programmable, and accessed through the CRTC address pointer and the CRTC data register. (See Paragraph C.2.2.4.)

**C.1.4.1 CRTC Timing –** The horizontal frequency (approximately 54 kHz) and vertical frequency (60 Hz) of the VR260 monitor, along with the 925 ns clock (nominal; see Table C-1), determine the timing sequence for transferring an image from video memory to the CRT screen.

The dual-ported video memory is accessed in both halves of a 925 ns access cycle, as shown in Figure C-6. During the first half-cycle, the memory is addressed and updated from the Q22-Bus. During the second half-cycle, the memory is addressed by the video refresh address from the CRTC, and read to refresh the CRT screen. (The update and refresh cycles are described in more detail in Paragraph C.1.5.)

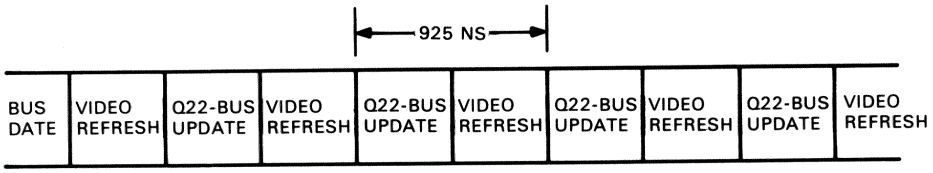



Figure C-6 Video Memory Access Cycle

In CRTC terminology, the 462.5 ns video refresh half-cycle is equivalent to a *character time.* The number and duration of the character times determine the period of HSYNC (horizontal sync); that is, the time for each horizontal scan line. Using the VR260 monitor with a horizontal frequency of 54 kHz, the HSYNC period is 18.5 $\mu$s, or 40 character times. (Figure C-7) Note that time and frequency values are nominal. The horizontal retrace period (horizontal blanking) is the difference between the total time for one horizontal scan line and the displayed (unblanked) part of the scan line. For the VR260, this is 40 − 32 = 8 character times, or 3.7 $\mu$s horizontal blanking.

In a similar way, the CRTC controls vertical timing. (Figure C-8) In a 60 Hz VR260 monitor, the VSYNC period is 16.667 ms. Of this, approximately 0.7 ms is vertical retrace (vertical blanking) time and the screen is unblanked for 15.9 ms. With a horizontal scan line time (HSYNC period) of 18.5 $\mu$s, a total of 901 horizontal scan lines can be generated during the VSYNC period (16.6 ms), with 864 scan lines displayed during the 15.9 ms vertical unblanking time.

In CRTC terminology, vertical timing is programmed in terms of *character row* (or *character line*) times. A character row comprises 16 horizontal scan lines. For the displayed portion of the vertical scan, the CRTC vertical displayed parameter is 54 (for 54 character rows, or 864 scan lines). For the total vertical scan, the vertical total parameter of the CRTC is 55 (for 56 minus 1 character rows). This equates to 896 horizontal scan lines, where 901 need to be generated. Therefore, the CRTC vertical adjust parameter (must be less than 16) is 5, providing the required number of scan line times for the VR260 to complete the 16.6 ms vertical scan.

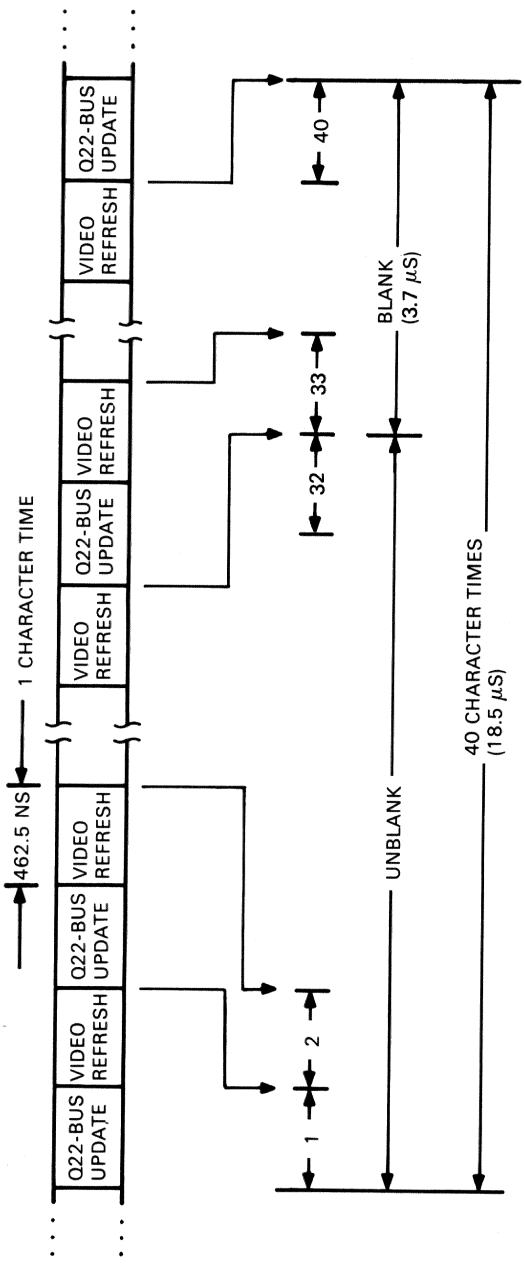



Figure C-7 CRTC Horizontal Timing

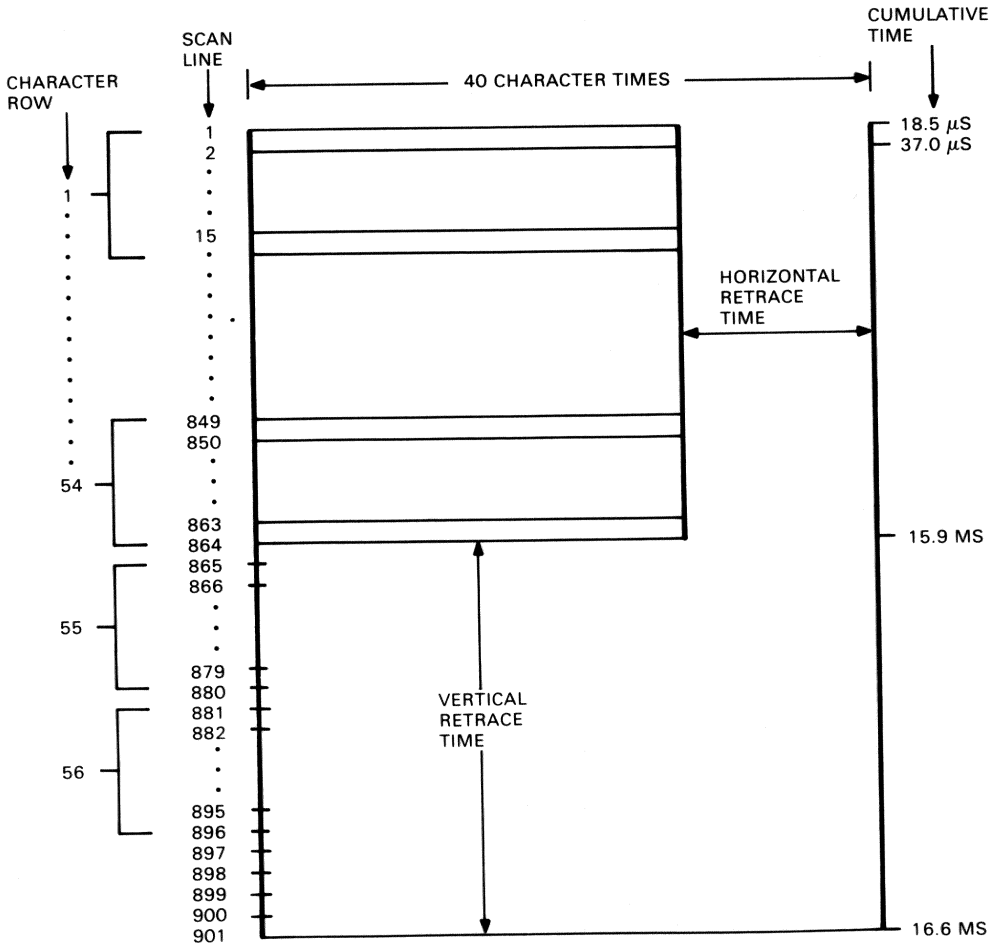



Figure C-8 CRTC Vertical Timing

During the time the display is blanked, the 462.5 ns video refresh cycles are used to refresh the video memory RAMs. The dynamic RAM refresh address is generated by a 4-bit refresh counter.

Other timing values programmed in the CRTC include sync pulse width, start of sync, and start of display enable.

The CRTC also contains a video refresh register and cursor start and end address registers. The refresh register contains the address of the first video memory address to be read at the end of vertical blanking. The cursor start address register contains the scan line where the cursor starts, and control bits to enable the cursor, cause it to blink, and set the rate at which it blinks.

### C.1.5 Video Memory

The video memory is a 256-Kbyte dual-ported MOS RAM array. It is a *single-plane* (or *1-plane*) bit-mapped memory; that is, the value (on or off) of each pixel on the screen corresponds to the value (1 or 0) of only one bit in memory. Each pixel is defined by its X,Y position in the memory, where Y represents a scan line 1 pixel (bit) high and 1024 pixels (bits) long (X). There are 2048 scan lines in video memory. (Figure C-9)

**NOTE – Coordinate System**
**The top, left corner of the screen is (X,Y) coordinate (0,0). The bottom, right corner of the screen is (X,Y) coordinate (1023,863).**

Video memory is dual-ported, giving access to the Q22-Bus to update video memory, and to the scan line map to refresh the monitor screen (video refresh).

The 32 64 K × 1 dynamic RAMs (refresh is required) that make up the array are arranged in 32-bit words. The byte, word, or longword operand is specified by Q22-Bus BDAL<17:00>. BDAL<17:07> specify one of the 2048 scan lines, and BDAL<06:00> specify one of the 128 bytes within the scan line. Individual bits are controlled by CPU bit operations.

For video refresh, video memory is addressed through the scan line map as an X-Y address space. The scan line map selects any 864 scan line segment of video memory, each line having 1024 pixels.

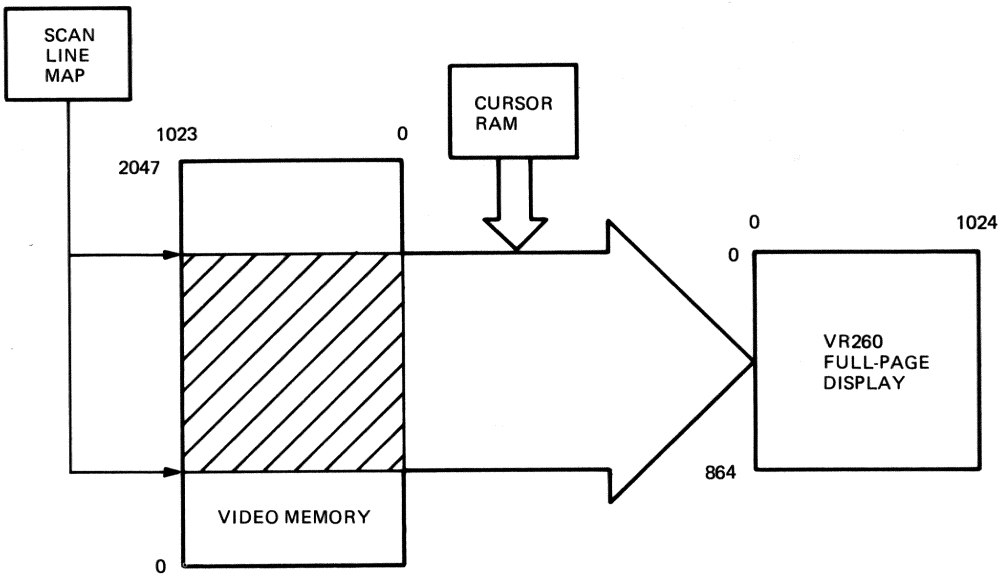



Figure C-9 VR260 Monitor Display Mapping

**C.1.5.1 Scan Line Map –** The scan line map comprises two 2 K × 8 static RAMs (refresh is not required). It is configured as a 1 K × 11 RAM; that is, the MSB (most significant bit) of the address is disabled, and the five MSBs of the output are not used. It translates the 10 MSBs of the CRTC start address output (video refresh address) into an 11-bit video memory physical address, mapping any 864 of the 2048 video memory scan lines to the VR260 monitor (Figure C-9). If the VCB01 is used in half-page mode, the scan line map maps only the lowest 800 pixels of any 480 scan lines to a half-page monitor.

The scan line map is addressed as the upper 2 Kbytes of VCB01 address space (see Figure C-18), making these video memory addresses unavailable for storing and refreshing video images. (Note that read and write operations to these addresses access both the scan line map and video memory.) Therefore, the 11 LSBs (least significant bits) of location MSA + 254 K (MSA + 260096) are the 11 bits output from the scan line map. They point to the video memory address of the first video scan line; MSA + 254 K + 2 points to the next scan line, and so on.

**C.1.5.2 Video Memory (Update Memory) –** As Figure C-10 shows, video memory is addressed by eight lines from the memory address mux (multiplexer). These lines are multiplexed, 8-bit, row and column addresses. The row and column addresses are latched in memory at the appropriate time by RAS and CAS (row address strobe and column address strobe) inputs, providing a 16-bit memory address.

The memory address mux output, D4MA07:00, is one of the following, selected by the combinations of D11UPDATE and –D11COL (read as "not D11COL").

0 – Video refresh column address

1 – Video refresh row address

2 – Update memory column address

3 – Update memory row address

Video memory is updated from the Q22-Bus every 925 ns. To update the image in video memory, the row address on BDAL<14:07> is selected by:

D11UPDATE = High

–D11COL = High

The column address on BDAL<17:15,06:02> is selected by:

D11UPDATE = High

–D11COL = Low

The addresses are latched by D11RAS0 and D11CAS0 from the timing PAL.

The input data (two 16-bit words) on BDAL<15:00> is written into each of the four bytes of the 32-bit memory by four write-enable signals, D12WE03:00, from a 32 × 8 write PROM.

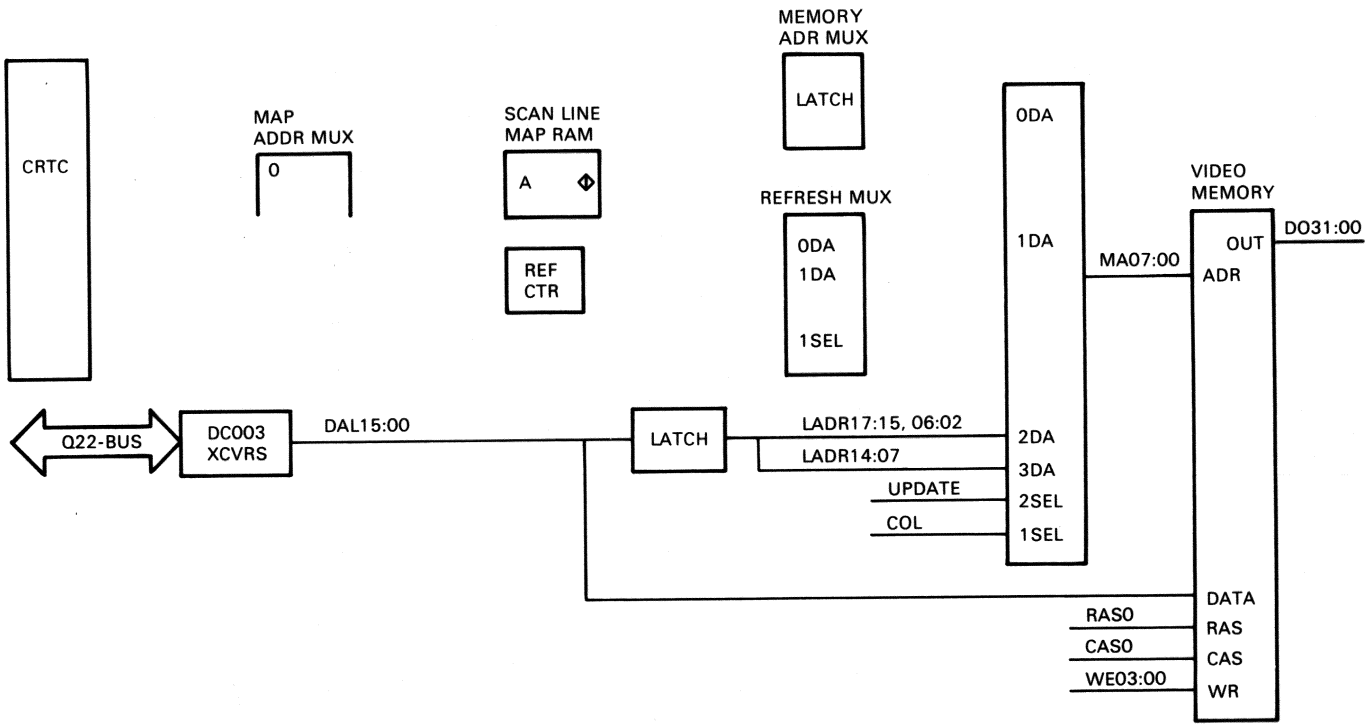



Figure C-10 Video Memory Write (Update)

**C.1.5.3 Video Memory (Video Refresh) –** Figure C-11 shows the read-access paths to video memory. To refresh the monitor screen, the row address on D5CR07:00 is selected through memory address mux input 1 – DA by:

D11UPDATE = Low

–D11COL = High

The column address on D5LMAP10:08 and D5LCADR04:00 is selected through input 0 – DA by:

D11UPDATE = Low

–D11COL = Low

The row address is selected through refresh mux input 0 – DA (this mux is described in more detail below), and is supplied by the scan line map on D5MAPDAT07:00. The scan line map also supplies the three MSBs of the column address on D5LMAP10:08. The five LSBs of the column address, D5LCADR04:00, are supplied by the CRTC. This 16-bit (8 row, 8 column) video memory read address is interpreted as shown in Table C-2, and described below.

**Table C-2 Video Refresh Address Derivation**

| | | | |
|---|---|---|---|
| Address: | Row | Column | |
| | Memory Address MA_ | Memory Address MA_ | |
| | 07 06 05 04 03 02 01 00 | 07 06 05 04 03 02 01 00 | |
| Source: | Scan Line Map | | CRTC |
| | MAPDAT_ | LMAP_ | LCADR_ |
| | 07 06 05 04 03 02 01 00 | 10 09 08 | 04 03 02 01 00 |
| | 11 bits address 2048 lines (32 words per line) | | 5 bits address (32 words) |

For video refresh, video memory represents 2048 scan lines with 1024 pixels per line. Therefore, each line of the video image requires 32 32-bit words. Because each memory address reads one 32-bit word, 32 addresses are required to read one scan line. To read a specific line for display, the 11-bit scan line map outputs, D5MAPDAT07:00 and D5LMAP10:08, provide the 11 MSBs of the memory address. Each of the 32 32-bit words in that line are read by incrementing the 5 LSBs of the memory address, supplied by the CRTC as D5LCADR04:00. In the VAXstation II system using the VR260 monitor, only 864 of the 2048 lines are

displayed, and all 1024 bits (32 32-bit words) of any scan line are displayed. The 32 words correspond to the 32 character times that the screen is unblanked. (Figure C-7)

The scan line map is addressed by the 10 MSBs of the CRTC address output, D5RA03:00 and D5CADR13:08, through map address mux input 0. (This mux is described in more detail below.) The CRTC start address register contains the value of the first address output by the CRTC; the address is then updated at the CRTC clock rate (determined by the timing PAL). Timing is such that 864 scan line map locations will be addressed during vertical display time, and 37 addressed during vertical retrace time. (Figure C-8) The CRTC output address will then be reset to the value of the start address register, and the process repeated. Continuing the address update during vertical retrace provides the addresses needed for dynamic RAM refresh (described below).

The contents of each scan line map location is the 11 MSBs of a video memory address.

**C.1.5.4 Video Memory (RAM Refresh) –** Figure C-11 shows that the only difference between the video memory read path and the dynamic RAM refresh path (Figure C-12) is that the row address, D5CR07:00, is supplied by the refresh counter through input 1 – DA of the refresh mux.

The RAM refresh row address, D4REF07:00, is selected through the refresh mux when D5DE (display enable) from the CRTC is not asserted. D5DE is de-asserted during horizontal retrace time and vertical retrace time.

The refresh counter is updated during every video memory update cycle (every 925 ns; see Figure C-6) when D5DE is not asserted. Therefore, every video refresh cycle during horizontal and vertical retrace times is a RAM refresh cycle, and updated row and column addresses are generated each cycle.

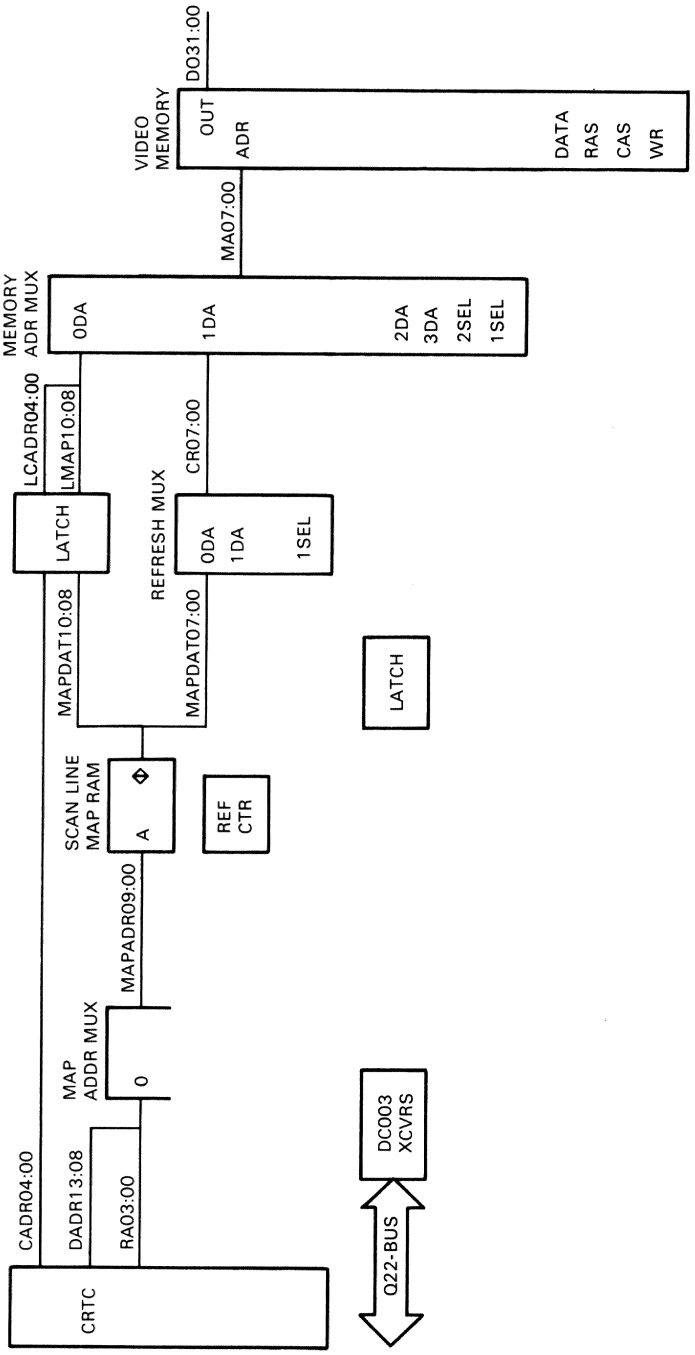



Figure C-11 Video Memory Read (Video Refresh)

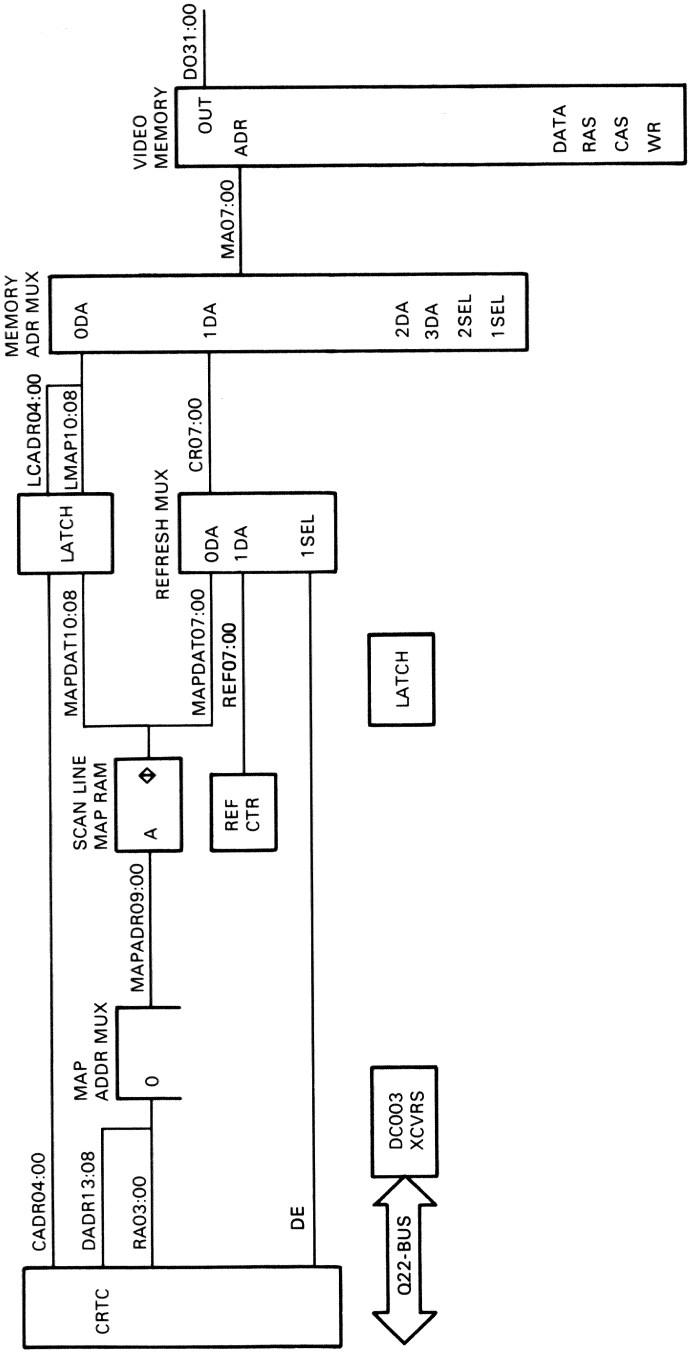



Figure C-12 Video Memory Read (RAM Refresh)

**C.1.5.5. Scan Line Map (Update) –** The 864 video memory addresses to be read for video refresh are stored in the scan line map. (Figure C-13)

When D11UPDATE is asserted, the scan line map is addressed from the Q22-Bus through input 1 of the map address mux. If the bit-map memory (video memory) is being addressed (D3BMSEL asserted) and the upper 2 Kbytes are being addressed (BDAL<17:11> asserted), the buffer is enabled, and write data is gated through to the scan line map RAM I/O pins. The write is enabled to each of the RAMs by D12WRSCANHB:LB from the 32 × 8 write PROM.

**C.1.5.6 Cursor –** The cursor is a 16 × 16 pixel image stored in the cursor RAM (static RAM). The output of the cursor RAM is logically combined with the output of video memory, by either ANDing or ORing the two outputs.

The cursor image is stored by writing to the upper 16 locations of the VCB01 address space (MSA + 256 K – 16).

The cursor can be positioned at any point on the screen, within the limits of the coordinate system. The cursor origin is its top, left corner; its minimum (X,Y) position is (0,0) and its maximum (X,Y) position is (1007,847). The cursor Y-position is determined by the contents of the CRTC cursor start, end, and address registers; its X-position is stored in the cursor X-position register.

**C.1.5.7 Cursor RAM (Write) –** Refer to Figure C-14. When the top 16 locations (BDAL<17:05> asserted) of bit-map memory are addressed (D3BMSEL asserted) during an update cycle (D11UPDATE asserted), the 16 cursor RAM locations are addressed by BDAL<04:01> through input 0 of the cursor address mux.

The data (cursor image) on BDAL<15:00> is written into the RAM when D12WRCURSHB:LB are asserted by the 32 × 8 write PROM.

**C.1.5.8 Cursor RAM (Read) –** To read the cursor RAM and display the cursor image, the RAM is addressed by a 4-bit address counter through input 1 of the cursor address mux. The counter is enabled (through combinational logic) by the CURS and HSYNC outputs of the CRTC.

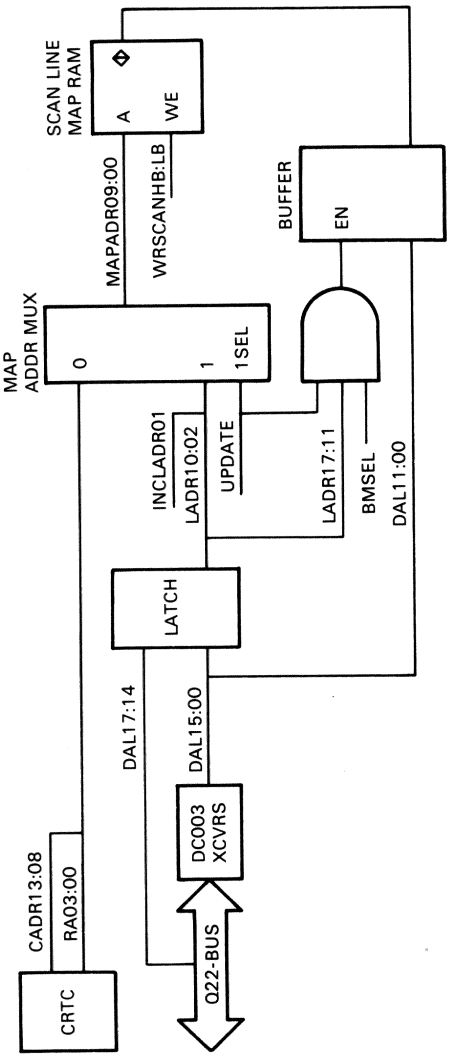



Figure C-13 Scan Line Map Write (Update)

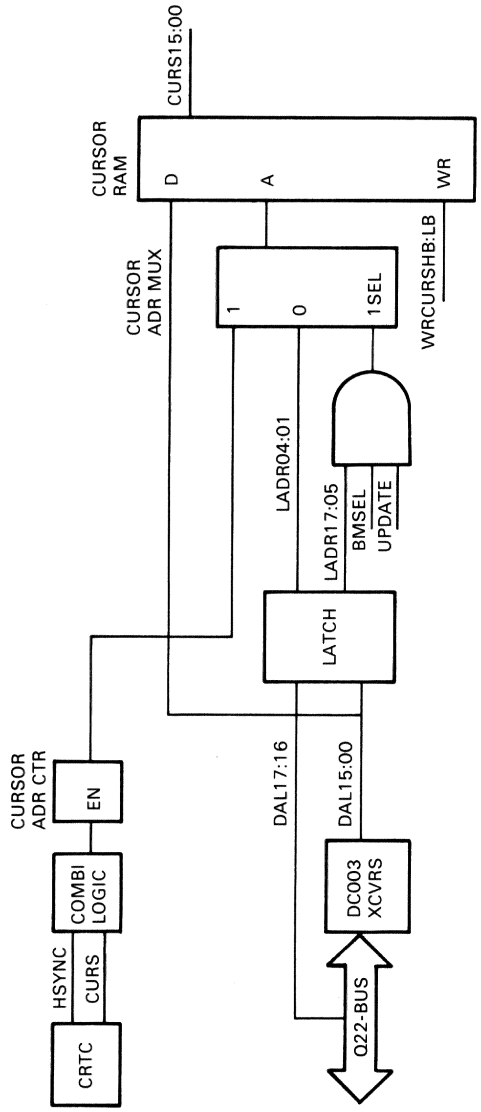



Figure C-14 Cursor RAM Read/Write

### C.1.6 Mouse

The mouse position logic comprises flip-flops driven by commutator brushes (Figure C-15) and push buttons. The flip-flops provide signal settling (de-bouncing) and pulse shaping, and generate square-wave outputs. The square-wave leading edges are counted, giving an effective resolution of 100 counts per 2.54 cm (1 in).

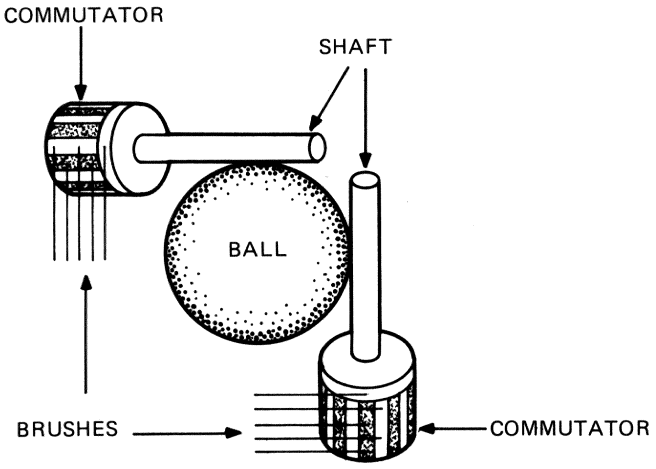



Figure C-15 Mouse Construction

The X and Y commutators each provide a distance signal (D15CLK1B and D15CLK1A) and a direction signal (D15CLK2B and D15CLK2A), which control the clock and count direction of X and Y counters. (Figure C-16) The mouse push buttons are input to the interrupt controller and CSR.

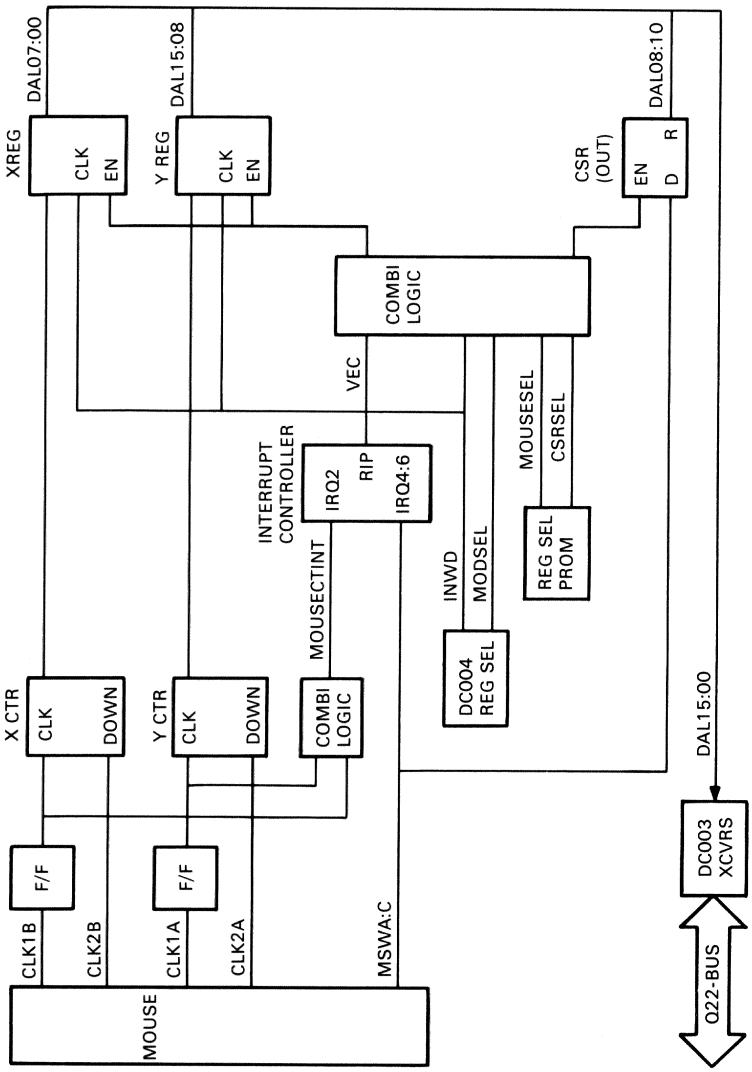



Figure C-16 Mouse Interface

Mouse direction is determined by the direction of the count; that is, up or down. The direction of count is determined by the phase relationship between the distance and direction outputs. When the mouse is moved in one direction, the distance output leads the direction output; mouse travel in the opposite direction reverses the phase relationship. This phase relationship is a result of commutator construction.

Another characteristic of mouse construction is that the period, and therefore, the number, of square-wave edges-per-inch varies with direction of travel. For example, if the mouse is moved in an exact vertical direction, the Y-axis would output the maximum number of edges-per-inch, indicating the maximum rate-of-change; the X-axis output would be flat, indicating no rate-of-change. If the mouse is moved in a direction that is halfway between vertical and horizontal, both the X-axis and Y-axis will output the same number of edges-per-inch.

Each time the mouse is moved an interrupt request is generated (D15MOUSECTINT). The accumulated X and Y count is transferred to BDAL<15:00> through the X and Y registers as a result of a bus DATI function (D3INWD). Normally, this occurs during vertical sync time; that is, every 16.6 ms. The distance the mouse traveled in that time is proportional to the change in the accumulated count.

### C.1.7 Keyboard

The keyboard is driven by an 8051 microprocessor, and contains a set of microdiagnostics. The keyboard logic detects and encodes keystrokes, and transmits the information to the DUART. (Figure C-17) The programmable DUART serializes/deserializes parallel bus data (BDAL<07:00>), implements the EIA RS423 interface, and generates an interrupt request (D14COMINT) to the interrupt controller. An on-board 3.6864 MHz oscillator supplies the baud rate clock input to the DUART.

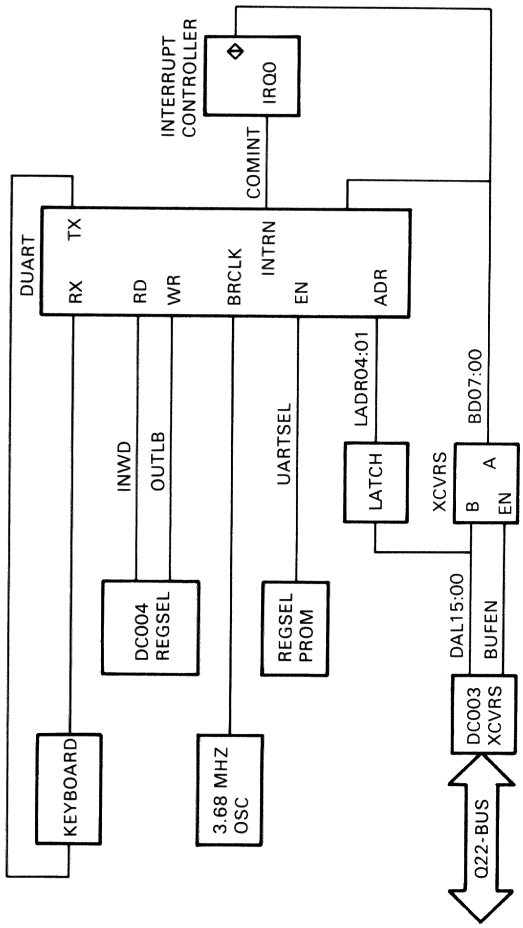



Figure C-17 Keyboard Interface

## C.2 PROGRAMMING INFORMATION

This section describes the programmable functions of the VCB01 video controller module; that is, the functions that can be specified and/or examined by software.

### C.2.1 Address Space

The MicroVAX architecture specifies a 1-Gbyte (gigabyte) physical address space, divided into a memory space and I/O space. (Figure C-18)

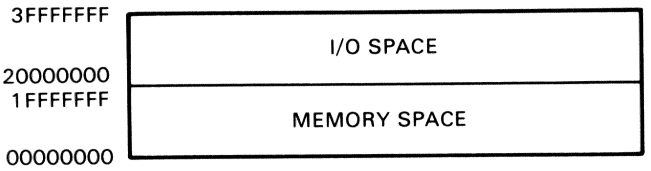



Figure C-18 MicroVAX Physical Address Space

In the MicroVAX, address bit <29> selects either the memory space or I/O space, bit <28> is a *no-cache indicator*, bits <27:22> are ignored, and bits <21:00> select a location within memory space or I/O space.

In the VAXstation II, the VCB01 video memory resides in the I/O physical address space, in the highest 256 Kbytes addressable by BDAL<21:00>. Figure C-19 shows the location on the VCB01 video memory in the VAXstation II physical address space. The MSA (memory starting address) of the 256-Kbyte VCB01 block is switch-selectable.

The 256-Kbyte VCB01 address space comprises the three segments, shown in Figure C-20. The scan line map RAM overlays the upper 2 Kbytes of the 256-Kbyte bit-mapped RAM; the cursor RAM overlays the upper 32 bytes of the scan line map RAM. As described in Section C.1, these are all separate RAMs, not part of the same RAM.

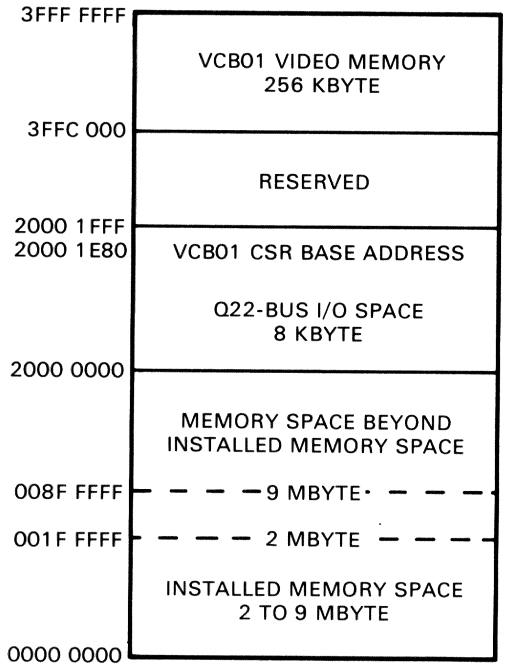



Figure C-19 VAXstation II Physical Address Space

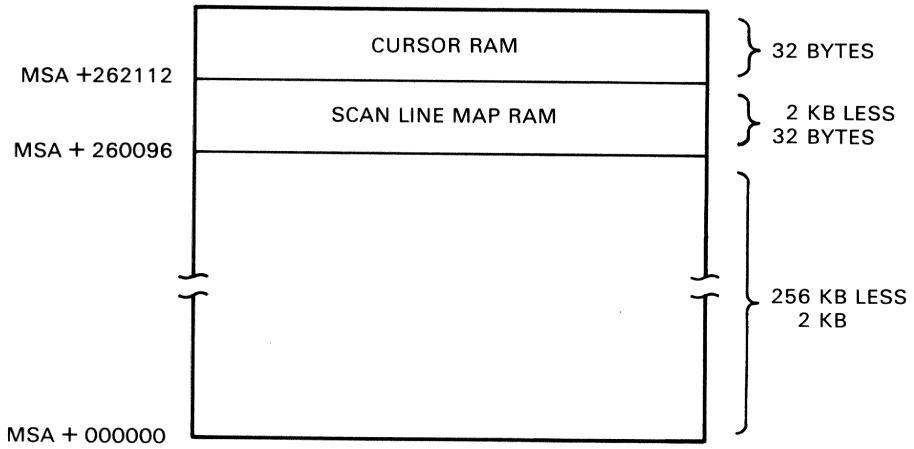



Figure C-20 VCB01 256-Kbyte Address Space

### C.2.2 VCB01 Registers

Control and status information is exchanged between the VCB01 and the CPU through 32 16-bit locations in the I/O page. These locations are listed in Table C-3 and described below.

**NOTE – Bit Descriptions**
**Many of the bit descriptions in the following tables include a value in parenthesis; for example: (1 = chip armed). This usually indicates the initialized value of the bit.**

**Table C-3 VCB01 Registers**

| Address* | Name |
|---|---|
| BASE | CSR – Control and status register |
| BASE+2 | Cursor X-position |
| BASE+4 | Mouse position register |
| BASE+6 | (Spare) |
| BASE+8 | CRTC address pointer register |
| BASE+10 | CRTC data register |
| BASE+12 | ICDR – Interrupt controller data register |
| BASE+14 | ICSR – Interrupt controller command/status register |
| BASE+16 through BASE+31 (Spares) | |
| BASE+32 | UART mode registers 1A and 2A |
| BASE+34 | UART status/clock select register A |
| BASE+36 | UART command register A |
| BASE+38 | UART transmit/receive buffer A |
| BASE+40 | (Spare) |
| BASE+42 | UART interrupt status/mask register |
| BASE+44 | (Spare) |
| BASE+46 | (Spare) |
| BASE+48 | UART mode registers 1B and 2B |
| BASE+50 | UART status/clock select register B |
| BASE+52 | UART command register B |
| BASE+54 | UART transmit/receive buffer B |
| BASE+56 through BASE+62 (Spares) | |

* BASE = CSR base address

**C.2.2.1 Control and Status Register –** The CSR bits are shown and described in Figure C-21 and Table C-4. Note that following a Q22-Bus BINIT, bits <06:02> are cleared (= 0).

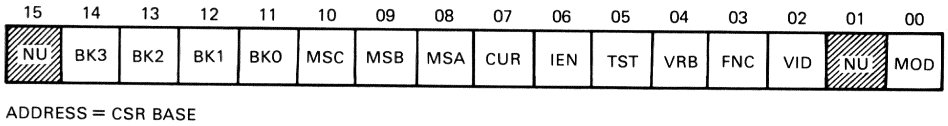



Figure C-21 VCB01 CSR Format

**Table C-4 VCB01 CSR Bits**

| Bits | Access | Description |
|---|---|---|
| <15> | | (Spare – not used) |
| <14:11> | READ | Memory bank switch 0:3 (MSA switch E14 S1:S4) |
| <10:09> | READ | Mouse switch C:A (0 = closed) |
| <07> | READ | Cursor active (1 = cursor on) |
| <06> | RD/WR | Interrupt enable (1 = enabled) |
| <05> | RD/WR | Test bit (used with loopback connector) |
| <04> | RD/WR | Enable video read-back (1 = enabled) |
| <03> | RD/WR | Cursor function (1 = OR, 0 = AND) |
| <02> | RD/WR | Enable video output (1 = enabled) |
| <01> | | (Spare – not used) |
| <00> | READ | 19 in/15 in mode (1 = 19 in) |

**C.2.2.2 Cursor X-Position –** This register (Figure C-22 and Table C-5) contains the horizontal position location of the top left corner of the 16 × 16 (pixel) cursor image. The value is in pixels and must not allow the cursor to be positioned beyond the maximum X pixel. That is, the maximum value is 1007 (1023 – 16) for a VR260 monitor, and 783 (799 – 16) for a 38 cm (15 in) monitor.

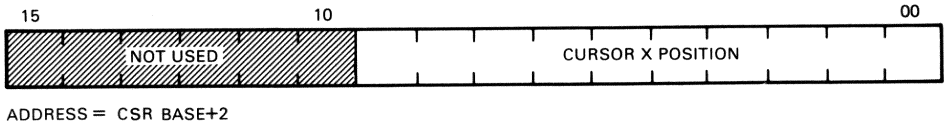



Figure C-22 VCB01 Cursor X-Position Format

**Table C-5 VCB01 Cursor X-Position Bits**

| Bits | Access | Description |
|---|---|---|
| <15:10> | | (Not used) |
| <09:00> | WRITE | Cursor X-position in pixels. |

**C.2.2.3 Mouse Position Register –** This register (Figure C-23 and Table C-6) contains mouse X- and Y-position values. The values are counted up or down, in proportion to the direction and amount of mouse movement.

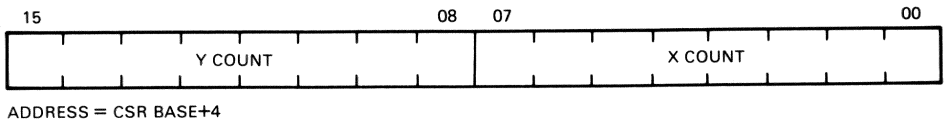



Figure C-23 Mouse Position Register Format

**Table C-6 Mouse Position Register Bits**

| Bits | Access | Description |
|---|---|---|
| <15:08> | READ | Mouse Y-position count |
| <07:00> | READ | Mouse X-position count |

### C.2.2.4 CRTC Registers –

**CRTC Address Register Pointer –** This register points to the 1 of 17 internal CRTC registers (Table C-7) that is to receive the data contained in the CRTC data register (described below). It also contains three status bits. (Figure C-24 and Table C-8)

**Table C-7 CRTC Internal Registers**

| Reg | Name | Description |
|---|---|---|
| 00 | Horizontal Total | The total number of character times in a line, minus 1. |
| 01 | Horizontal Displayed | The total number of displayed characters in a line. |
| 02 | HSYNC Position | Defines the number of character times until HSYNC (horizontal sync). |
| 03 | HSYNC/VSYNC Widths | Four bits each are used to define the HSYNC pulse width and the VSYNC (vertical sync) pulse width. |
| 04 | Vertical Total | Total number of character rows on the screen, minus 1. |
| 05 | Vertical Total Adjust | The number of scan lines to complete the screen. |
| 06 | Vertical Displayed | The number of character rows displayed. |
| 07 | VSYNC Position | The number of character rows until VSYNC. |
| 08 | Mode | Controls addressing, interlace, and cursor. |
| 09 | Maximum Scan Line | The number of scan lines in a character row, minus 1. |
| 10 | Cursor Scan Start | Defines the scan line at which the cursor starts. |
| 11 | Cursor Scan End | Defines where the cursor ends. |
| 12<br>13 | Start Address High<br>Start Address Low | Defines the RAM location where video refresh begins. |

**Table C-7 CRTC Internal Registers (Cont.)**

| Reg | Name | Description |
|---|---|---|
| 14 | Cursor Address High | Defines the cursor position in RAM. |
| 15 | Cursor Address Low | |
| 16 | Light Pen Position High | Contains the position of the light pen. |
| 17 | Light Pen Position Low | |

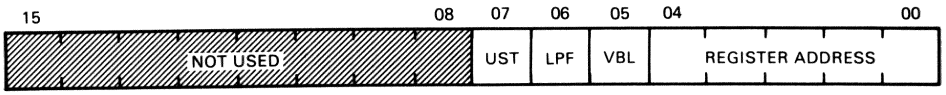



Figure C-24 CRTC Address Register Pointer Format

**Table C-8 CRTC Address Register Pointer Bits**

| Bits | Access | Description |
|---|---|---|
| <15:08> | | (Not used) |
| <07> | READ | Update strobe (not used) |
| <06> | READ | Light pen register full (1 = full) |
| <05> | READ | Vertical blank (1 = Vblank time) |
| <04:00> | WRITE | CRTC internal register address (Table C-7) |

**CRTC Data Register –** This register (Figure C-25 and Table C-9) contains the eight bits of data to be loaded into the internal CRTC register addressed by bits <04:00> of the CRTC address pointer register.

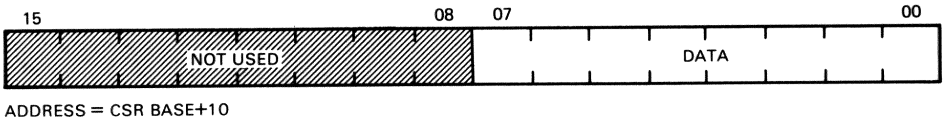



Figure C-25 CRTC Data Register Format

**Table C-9 CRTC Data Register Bits**

| Bits | Access | Description |
|---|---|---|
| <15:08> | | (Not used) |
| <07:08> | RD/WR | CRTC internal register data |

**C.2.2.5 Interrupt Controller Registers –** Using a set of internal registers, the interrupt controller handles eight interrupt requests on priority levels 0 (highest) to 7 (lowest):

0 – DUART

1 – Vertical sync

2 – Mouse

3 – Cursor start

4 – Mouse button A

5 – Mouse button B

6 – Mouse button C

7 – (Spare)

A vector for each request level is stored in an internal 8 × 32 response memory. The response memory cannot be read and is unaffected by a RESET command.

The internal registers are accessed through the ICSR (interrupt controller command/status register) and ICDR (interrupt controller data register). The registers are described in the following paragraphs.

**ICDR –** The interrupt controller data register (Figure C-26 and Table C-10) contains the data for/from the internal interrupt controller register addressed by the last PRESELECT command.

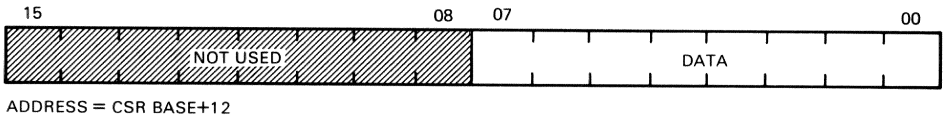



Figure C-26 ICDR Register Format

**Table C-10 ICDR Bits**

| Bits | Access | Description |
|---|---|---|
| <15:08> | | (Not used) |
| <07:08> | RD/WR | Interrupt controller internal register data |

**ICSR –** The internal interrupt controller registers are accessed through the ICDR and the ICSR (interrupt controller command/status register). The ICSR is a command register on write operations and a status register on read operations. (Figure C-27 and Table C-11)

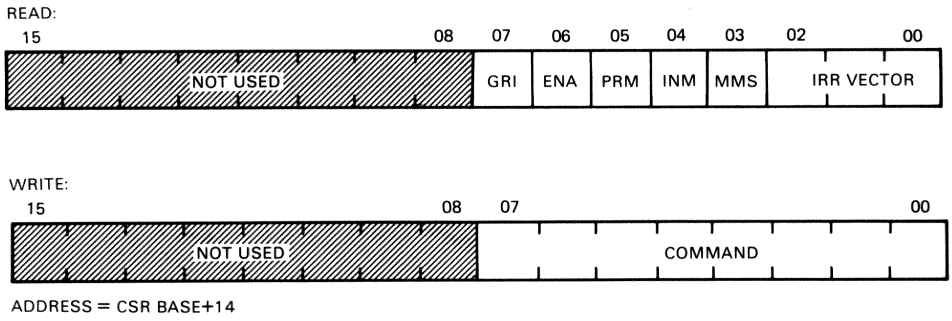



Figure C-27 ICSR Format

**Table C-11 ICSR Bits**

| Bits | Access | Description |
|---|---|---|
| <15:08> | | (Not used) |
| <07> | READ | Group interrupt (1 = interrupt pending). Vector is in bits <02:00>. |
| <06> | READ | Enable (1 = chip enabled). |
| <05> | READ | Priority mode (1 = rotating, 0 = fixed). |
| <04> | READ | Interrupt mode (1 = polled, 0 = interrupt). |
| <03> | READ | Master mask (1 = chip armed). |
| <02:00> | READ | Binary vector of the highest unmasked bit in the IRR (interrupt controller interrupt response register). Valid only when bit <07> is set. |
| <07:00> | WRITE | Command. (See Table C-12.) |

**Table C-12 ICSR Commands**

| ICSR* <07:00> | Command | Description |
|---|---|---|
| 00000000 | RESET | Sets the IMR (interrupt mask register) to all ones. Clears to zeros the: IRR (interrupt response register), ISR (interrupt service register), ACR (auto clear register), and mode register. Response memory and byte count registers are not affected. |
| 00010xxx | CLEAR IRR AND IMR | Clears all bits in the IRR and IMR. |
| 00010BBB | CLEAR ONE IRR AND IMR BIT | Clears both the IRR bit and the IMR bit specified in <02:00>. |
| 00110xxx | SET IMR | Sets all IMR bits to ones. |
| 00111BBB | SET ONE IMR BIT | Sets the IMR bit specified in <02:00>. |
| 01000xxx | CLEAR IRR | Clears all IRR bits to zeros. |
| 01001BBB | CLEAR ONE IRR BIT | Clears the IRR bit specified in <02:00>. |
| 0110xxxx | CLEAR HIGHEST PRIORITY ISR BIT | Clears the highest priority bit set in the ISR. |
| 01110xxx | CLEAR ISR | Clears all ISR bits to zeros. |
| 01111BBB | CLEAR ONE ISR BIT | Clears the ISR bit specified in <02:00>. |
| 100MMMMM | LOAD MODE BITS M4:M0 | Sets the five low-order bits of the mode register to the value in <04:00>. |

**Table C-12 ICSR Commands (Cont.)**

| ICSR* | Command | Description |
|---|---|---|
| 1010MMNN | CONTROL MODE BITS M7:M5 | Sets mode register bits 6 and 5 to the value in <06:05>. Mode register bit 7 is set according to <01:00>, as follows.<br>01 00 Bit 7<br>0 0 Unchanged<br>0 1 Set<br>1 0 Cleared<br>0 0 (Illegal) |
| 1011xxxx | PRESELECT IMR FOR WRITING | All future write operations to the ICDR load the data into the IMR. |
| 1100xxxx | PRESELECT ACR FOR WRITING | All future write operations to the ICDR load the data into the ACR. |
| 11100LLL | PRESELECT RESPONSE MEMORY FOR WRITING | All future write operations to the ICDR load the data into the response memory at the interrupt request level location specified in <02:00>. |

* x = 1 or 0 (does not matter)

**IRR** – The 8-bit interrupt request register stores pending interrupt requests. An IRR bit is set when the corresponding interrupt request line is asserted, and is automatically cleared when the request is acknowledged. The IRR bits can be read, set, and cleared through the ICSR and ICDR. RESET clears the IRR.

**IMR** – The 8-bit interrupt mask register is used to enable (bit cleared) or disable (bit set) the corresponding interrupt request lines. A set IMR bit does not disable the IRR bit, and the request will remain pending until the IMR bit is cleared. Only unmasked interrupts generate the group interrupt output. All IMR bits are set by RESET.

**ISR** – The 8-bit interrupt service register stores the acknowledge status of interrupt requests. When an interrupt is acknowledged, the controller selects the highest priority request pending, clears its IRR bit, and sets its ISR bit. ISR bits can be automatically cleared at the end of the acknowledge cycle or on specific command. The ISR can be read through the ICSR and ICDR. RESET clears the IRR.

**ACR –** The 8-bit auto clear register specifies the clearing mode for the ISR. A set ACR bit specifying the corresponding ISR bit will be automatically cleared at the end of the acknowledge cycle; a cleared ACR bit means the corresponding ISR bit must be cleared by the CPU through the ICSR and ICDR. The ACR can be read through the ICSR and ICDR. RESET clears the ACR.

**Mode –** The 8-bit interrupt controller mode register controls many controller options. The mode register is loaded through the ICSR and ICDR. It cannot be read. Bits 00, 02, and 07 are available to the ICSR on read operations. RESET clears the mode register. The bits are described in Table C-13.

**Table C-13 Interrupt Controller Mode Register Bits**

| Bits | Description |
|---|---|
| <07> | MM – Master mask. Enables (set) and disables (cleared) group interrupts to the CPU. |
| <06:05> | RP1:RP0 – Register preselect. Select the internal register to be read when the CPU reads the ICDR: |

| RP1 | RP0 | Register |
|---|---|---|
| 0 | 0 | ISR |
| 0 | 1 | IMR |
| 1 | 0 | IRR |
| 1 | 1 | ACR |

| | |
|---|---|
| <04> | REQP – Interrupt request polarity. Determines interrupt request transition direction for setting IRR bits. Set = low to high, cleared = high to low. (Should always be cleared.) |
| <03> | GIP – Group interrupt (GINT) polarity. When set, GINT is asserted high; when cleared, GINT is asserted low. (Should always be cleared.) |
| <02> | IM – Interrupt mode. When set, polled mode is selected, and group interrupt disabled. The controller will not interrupt the CPU. To determine if there are any pending interrupts, the CPU must read the ICSR. When cleared, interrupt mode is selected, and group interrupt functions normally. |
| <01> | VS – Vector selection. When cleared, each interrupt will generate its own vector (contained in response memory). When set, all interrupts generate the same vector (request level 0 vector). |

**Table C-13 Interrupt Controller Mode Register Bits (Cont.)**

| Bits | Description |
|---|---|
| <00> | PM – Priority mode. When cleared (fixed priority), level 0 interrupt requests are the highest priority, level 7 the lowest. When set (rotating priority), the last interrupt level serviced becomes the lowest priority level. |

**C.2.2.6 UART Registers –** The registers shown and described in Figures C-28 through C-32 and Tables C-13 through C-18 are all used to communicate with and control the keyboard/auxiliary DUART.

Note that mode registers 1A and 2A are accessed by two successive references to the same I/O address. The same is true for the channel B mode registers. Also note that the following registers serve different functions on reads and writes.

| Register (A and B) | Read | Write |
|---|---|---|
| Status/clock select | UART status | Tx/Rx clock select |
| Transmit/receive buffer | Receive data | Transmit data |
| Interrupt status/mask | Interrupt status | Interrupt mask |

**Mode Registers 1A and 2A –** These UART registers are accessed by two successive references to the same I/O address.

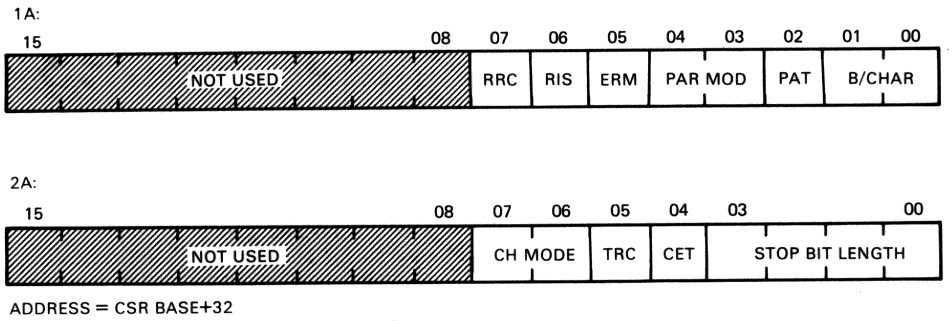



Figure C-28 Mode Registers 1A and 2A Format

**Table C-14 Mode Registers 1A and 2A Bits**

| Bits | Access | Description |
|---|---|---|
| <15:08> | | (Not used) |
| 1A: | | |
| <07> | RD/WR | Rx (receive) RTS (request-to-send) control (1 = no) |
| <06> | RD/WR | Rx interrupt select (1 = FIFO full) |
| <05> | RD/WR | Error mode (1 = block) |
| <04:03> | RD/WR | Parity mode (10 = no parity) |
| <02> | RD/WR | Parity type (1 = odd) |
| <01:00> | RD/WR | Bits per character (11 = 8) |
| 2A: | | |
| <07:06> | RD/WR | Channel mode (00 = normal) |
| <05> | RD/WR | Tx (transmit) RTS control (1 = no) |
| <04> | RD/WR | CTS (clear-to-send) enable Tx (1 = no) |
| <03:00> | RD/WR | Stop bit length (0111 = 1 bit) |

**Mode Registers 1B and 2B –** (ADDRESS = CSR BASE + 48) See mode registers 1A and 2A.

**Status/Clock Select Register A –** This register returns UART status information on a read, and selects the transmit and receive baud rates on a write.

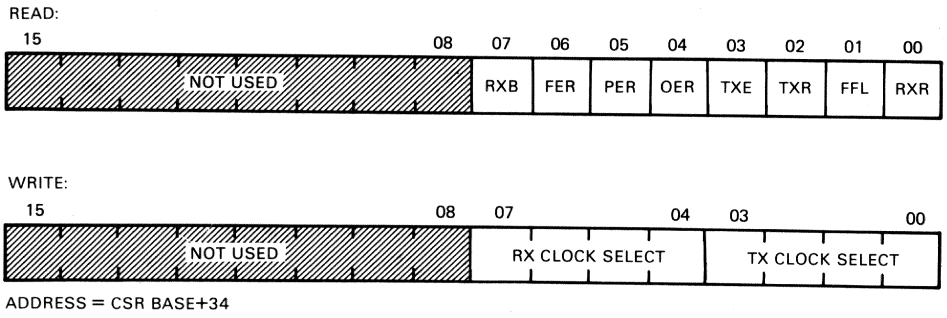



Figure C-29 Status/Clock Select Register A Format

**Table C-15 Status/Clock Select Register A Bits**

| Bits | Access | Description |
|---|---|---|
| <15:08> | | (Not used) |
| <07> | READ | Received break (1 = yes) |
| <06> | READ | Framing error (1 = yes) |
| <05> | READ | Parity error (1 = yes) |
| <04> | READ | Overrun error (1 = yes) |
| <03> | READ | Transmitter empty (1 = yes) |
| <02> | READ | Transmitter ready (1 = yes) |
| <01> | READ | FIFO full (1 = yes) |
| <00> | READ | Receiver ready (1 = yes) |
| <07:04> | WRITE | Receiver clock select (1001 = 4800 baud) |
| <03:00> | WRITE | Transmitter clock select (1001 = 4800 baud) |

**Status/Clock Select Register B –** (ADDRESS = CSR BASE + 50) See status/clock select register A.

**Command Register A –** All the bits in this UART register are access-only.

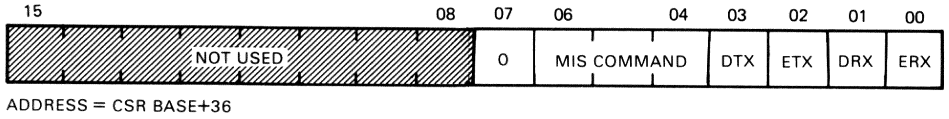



Figure C-30 Command Register A Format

**Table C-16 Command Register A Bits**

| Bits | Access | Description |
|---|---|---|
| <15:08> | | (Not used) |
| <07> | WRITE | (Spare – must be zero) |
| <06:04> | WRITE | Miscellaneous commands:<br>000 NOP (no operation)<br>001 Reset mode register pointer (Causes the mode register pointer to point to register 1.)<br>010 Reset receiver<br>011 Reset transmitter<br>100 Reset error status (Clears error status bits <07:04> in status/clock select register.)<br>101 Reset channel A break-change interrupt (Clears interrupt status/mask register bit <02>.)<br>110 Start break<br>111 Stop break |
| <03> | WRITE | Disable transmitter (1 = yes) |
| <02> | WRITE | Enable transmitter (1 = yes) |
| <01> | WRITE | Disable receiver (1 = yes) |
| <00> | WRITE | Enable receiver (1 = yes) |

**Command Register B –** (ADDRESS = CSR BASE + 52) See command register A.

**Transmit/Receive Buffer A –**

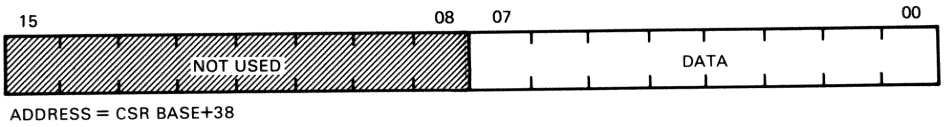



Figure C-31 Transmit/Receive Buffer A Format

**Table C-17 Transmit/Receive Buffer A Bits**

| Bits | Access | Description |
|---|---|---|
| <15:08> | | (Not used) |
| <07:00> | READ | Receive data |
| <07:00> | WRITE | Transmit data |

**Transmit/Receive Buffer B –** (ADDRESS = CSR BASE + 54) See transmit/receive buffer A.

**Interrupt Status/Mask Register –** This register transfers interrupt status on a read. On a write, set bits enable the UART interrupt request associated with the corresponding status bit.

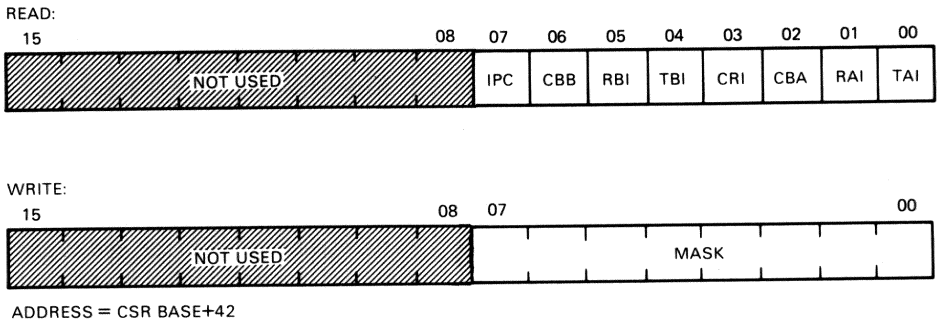



Figure C-32 Interrupt Status/Mask Register Format

**Table C-18 Interrupt Status/Mask Register Bits**

| Bits | Access | Description |
|---|---|---|
| <15:08> | | (Not used) |
| <07> | READ | Input port change (1 = yes) |
| <06> | READ | Change in break B (1 = yes) |
| <05> | READ | Receiver ready/FIFO full B (1 = yes) |
| <04> | READ | Transmitter ready B (1 = yes) |
| <03> | READ | Counter ready (1 = yes) |
| <02> | READ | Change in break A (1 = yes) |
| <01> | READ | Receiver ready/FIFO full A (1 = yes) |
| <00> | READ | Transmitter ready A (1 = yes) |
| <07:00> | WRITE | Bit-for-bit mask to enable interrupt request associated with the above status bits (00000010 = enable receiver ready interrupt on channel A) |

### C.2.3 Programming

**C.2.3.1 Cursor –** The cursor image is stored in the cursor RAM and occupies the upper 16 locations (32 bytes) of the VCB01 address space (Figure C-20).

The cursor position is determined by the cursor X-position register (Paragraph C.2.2.2) and the CRTC internal registers: cursor scan start, cursor scan end, and cursor address high (Table C-7). These registers are loaded as follows.

1. The four Y-position LSBs determine where the cursor starts within a character row, and are loaded into the CRTC cursor start register and cursor end register. Note that the cursor start register includes the cursor enable bit and the cursor blink rate bit.
2. The next six Y-position bits determine in which character row the cursor starts. These bits are loaded into the CRTC cursor address high register.

   After these registers have been loaded, the CRTC generates a cursor signal, which starts a 16 scan line counter. This counter addresses the cursor RAM.
3. The cursor X-position is loaded into the cursor X-position register.

The minimum X- and Y-positions are zero. The maximum X-position is the last pixel minus 16. The maximum Y-position is last scan minus 16. For best display presentation, all cursor operations, such as loading position or changing the image, should be performed when the cursor is off or during vertical retrace time.

T, MR-16348; 1-1, MR-16358; 1-2, MR-15162; 1-3, MR-15212; 1-4, MR-15183; 1-5, MR-13454; 1-6, MR-16355; 1-7, MR-16356; 1-8, MR-15165; 1-9, MR-16359; 1-10, MR-11887; 1-11, MR-15213; 1-12, MR-09535; 1-13, MR-15683; 1-14, MR-15163; 1-15, MR-16347; 1-16, MR-16448; 1-17, MR-16354; 1-18, MR-16357; 2-1, MR-14502; 2-2, MR-14503/14504; 2-3, MR-14616; 2-4, MR-14234; 2-5, MR-14704; 2-6, MR-15289; 2-7, MR-14044; 2-8, MR-14083; 3-1, MR-14072; 3-2, MR-15584; 3-3, MR-15244; 3-4, MR-15583; 3-5, MR-15802; 3-6, MR-16357; 4-1, MR-15964; 4-2, MR-16409; 4-3, MR-16410; 5-1, MR-15684; 5-2, MR-15686; 5-3, MR-15687; 5-4, MR-15688; 5-5, MR-15689; 5-6, MR-15690; 5-7, MR-15691; 6-1, MR-15184; 6-2, MR-15174; 6-3, MR-15692; 6-4, MR-16401; 6-5, MR-14719; 6-6, MR-14743; 6-7, MR-15217; 6-8, MR-15220; 6-9, MR-15224; 6-10, MR-15693; 6-11, MR-15692; 6-12, MR-15193; 6-13, MR-15180; 6-14, MR-15181; 6-15, MR-15182; 6-16, MR-15208; 6-17, MR-15207; 6-18, MR-15169; 6-19, MR-15170; 6-20, MR-15194; 6-21, MR-15225/15226; 6-22, MR-15222; 6-23, MR-15227; 6-24, MR-15211; 6-25, MR-15228/15223; 6-26, MR-15188; 6-27, MR-15221; 6-28, MR-15195; 6-29, MR-13827; 6-30, MR-15191; 6-31, MR-15192; 6-32, MR-16341; 6-33, MR-16339; 6-34, MR-16350; 6-35, MR-16340; 6-36, MR-16344; 6-37, MR-16351; C-1, MR-14633; C-2, MR-14634; C-3, MR-14635; C-4, MR-14636; C-5, MR-14641; C-6, MR-14640; C-7, MR-16360; C-8, MR-14638; C-9, MR-16352; C-10, MR-14648; C-11, MR-14632; C-12, MR-14631; C-13, MR-14647; C-14, MR-14564; C-15, MR-09709; C-16, MR-14618; C-17, MR-14617; C-18, MR-14628; C-19, MR-16420; C-20, MR-14627; C-21, MR-14575; C-22, MR-14576; C-23, MR-14577; C-24, MR-14578; C-25, MR-14587; C-26, MR-14588; C-27, MR-14589; C-28, MR-14590; C-29, MR-14591; C-30, MR-14592; C-31, MR-14593; C-32, MR-14594.