EG 3014
EG 3020
EG 3021
EG 3022

EXPANSION

TECHNICAL MANUAL

BY EACA

PREFACE

This manual is written to give a brief view of the theory of operation and technical information of the Expander EG3014 and the optional interface boards that can be added to it. The manual can be regarded as a reference or a reminder to the experienced technical people. It is expected that the reader should have the basic knowledge of digital electronics in order to make full use of this manual.

Please do not hesitate to inform us about any errors, mistakes and information out of date. We are pleased to correct the mistakes and up-date this manual.

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INTRODUCTION

The Expander EG3014 provides useful interfaces to the main unit of the Video Genie System. It includes 32K bytes of dynamic RAM memory, floppy disk controller and interface, and parallel printer interface. There are optional interface boards that can be added to the Expander. They are the RS-232-C interface and S-100 Bus interface.

The circuits of these interfaces are described briefly part by part so that the users may understand their Expander more quickly and modify it to suit their own use.

1. EG3014 EXPANDER

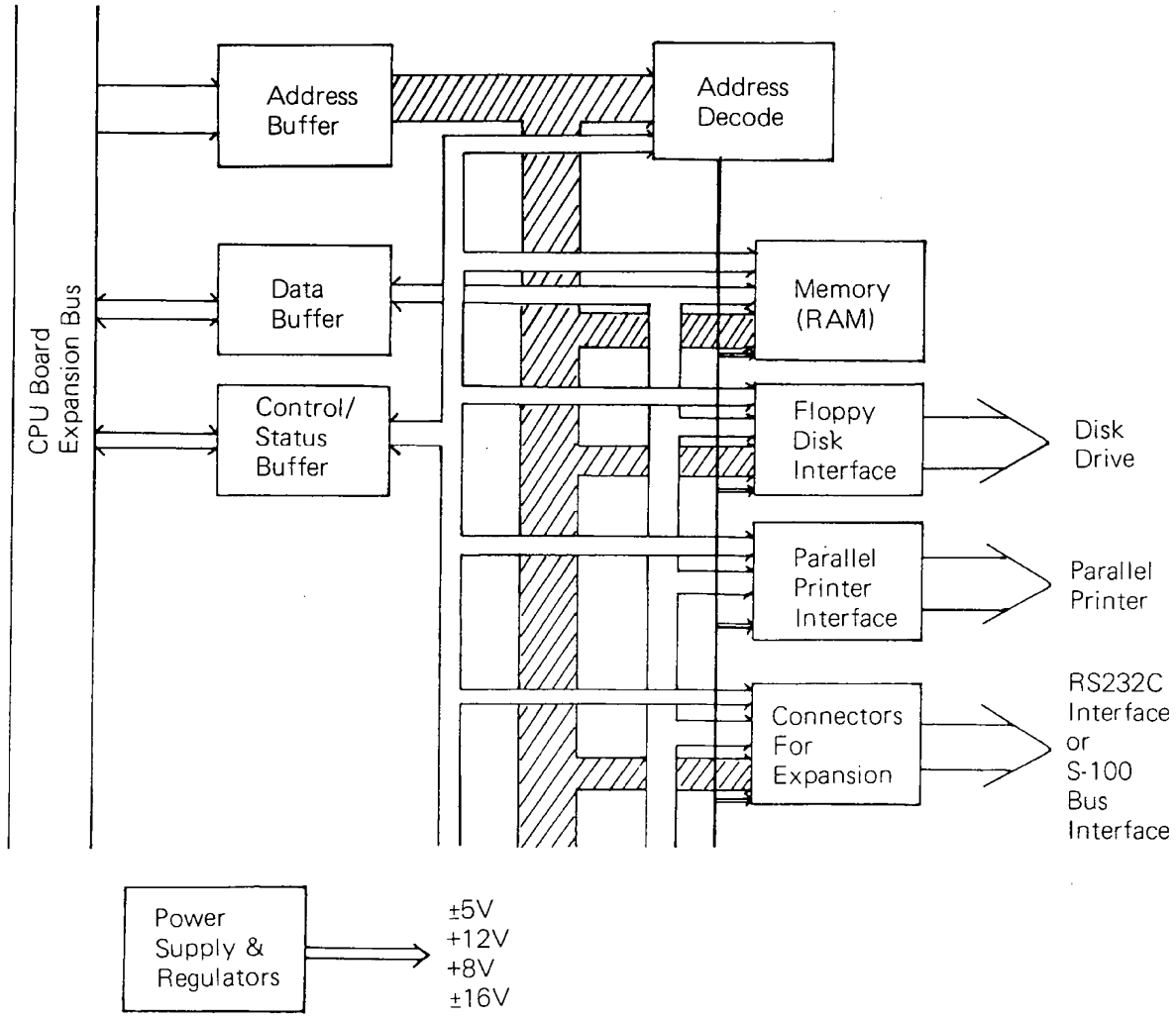
INTRODUCTION

This expander board can be divided into six parts:

1) buffers and address decode
2) memory (RAM)
3) floppy disk interface
4) parallel printer interface
5) connectors for further expansion
6) power supply and regulators

These functional blocks are illustrated in Fig 1.1.

Fig 1.1



1.1 BUFFERS AND ADDRESS DECODE LOGIC

The data lines, address lines, and control and status lines are buffered by 74LS244. The buffers are Z28, Z30, Z33, Z26 and Z20. In order to minimize the ringing and transient on the signal lines, resistance terminators (680 and 220 ohms) are added at the inputs of the address buffers and the control and status buffers.

Z29 and Z32 provide the memory block select signals, $\overline{32K}$ and $\overline{48K}$ to control $\overline{CAS}$ of the RAM's, Z34 generates the decoded read/write signals to the floppy disk interface. Z27 and Z31 give enable signals of a serial port, F8H or F9H, and of a parallel printer port of FDH.

1.2 MEMORY (RAM)

This part consists of dynamic RAM chips, address multiplexer, data buffers (74LS244) and control timing logic. The RAM chips are 4116, 16K x 1 bits each and of 250nsec access time. The row and column addresses are obtained from two multiplexers, Z9 and Z19 (74LS157). The control timing logic generates RAS, MUX and CAS from Z10, and the simplified circuit and timings are shown in Fig 1.2.

We may get 16K byte RAM's from this expansion unit just by inserting RAM chips into the sockets of Z11 through Z18. Z11 is the MSB and Z18 the LSB. Z1 through Z8 are sockets for the higher 16K bytes of RAM.

Fig 1.2 **GENERATION OF RAS, MUX AND CAS**

(a)

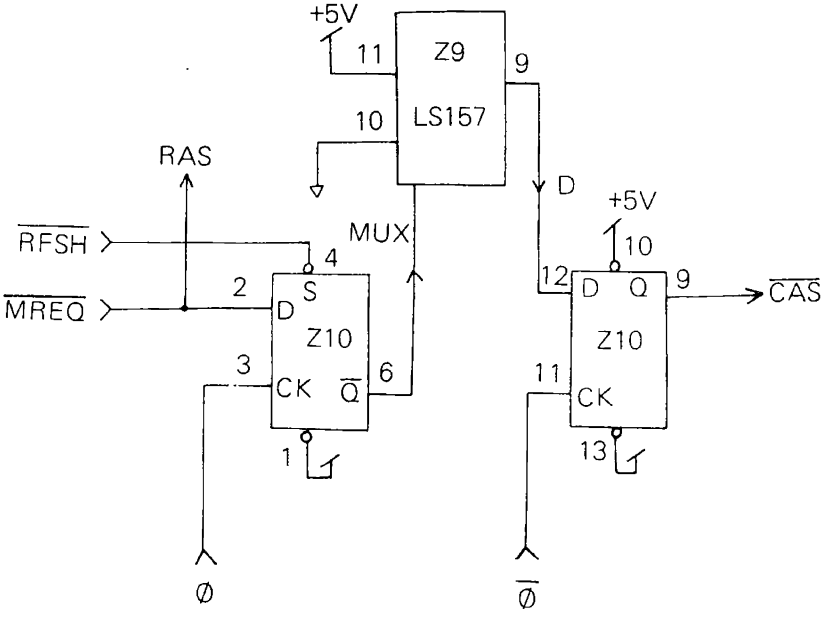
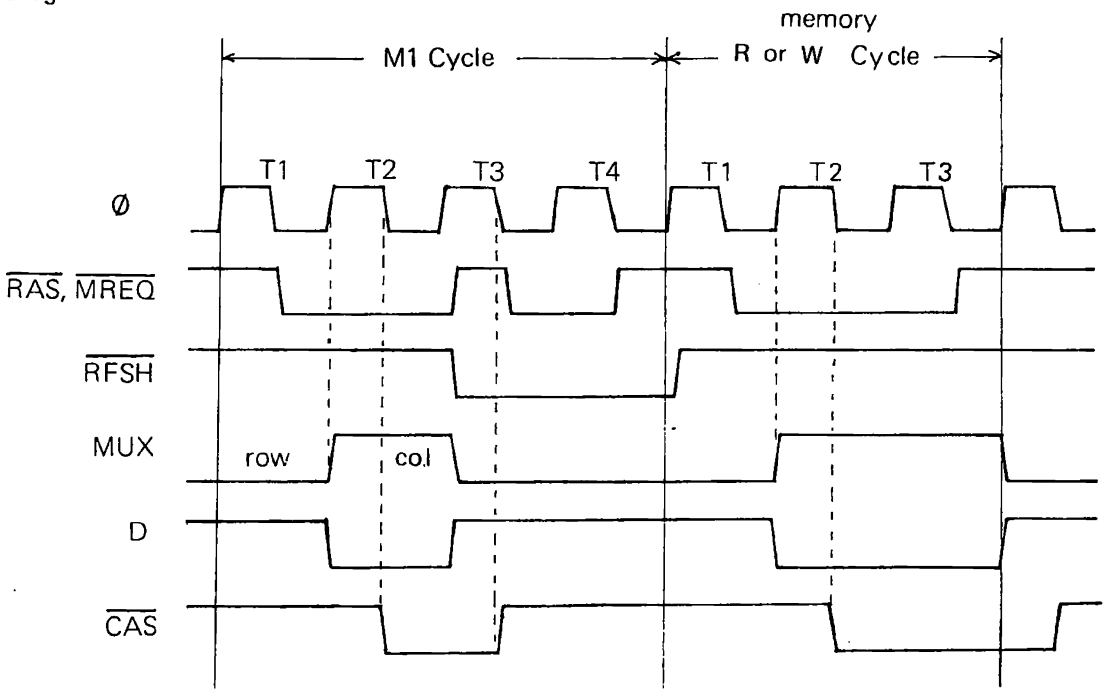


Fig 1.2

(b) Timing Diagram



1.3 FLOPPY DISK INTERFACE

1.3.1 Controller chip and Clock

The floppy disk controller (FDC) used is FD1771 which operates at 1 MHz. This clock is derived from a 8 MHz crystal oscillator and a divide-by eight counter, Z54. An interrupt for a real time clock occurs every 25 msec. This 40 Hz interrupt signal is obtained from a series of dividers, Z54, Z50, Z45 and Z44.

1.3.2 Drive Select

In order to select a drive, it is required to write a logical one to the corresponding bit of the latch, Z42. The data lines assigned for drive selection are as follows.

Port	Data Bit	Drive Select Signal
	DØ	DS1
37EØWR	D1	DS2
	D2	DS3
	D3	DS4
	(active 'one')	(active 'zero')

Any time selecting a drive, a signal $\overline{\text{Motor On}}$ of about 2 sec. duration is generated by the one-shot, Z47 and sent to the drive to turn on its motor.

1.3.3 Address Decode

The address decode for this floppy disk interface is assigned as in Table 1.1.

Table 1.1

Control Signal	Signal To	Function
37EØRD	Interrupt Logic	Read Interrupt Status
37EØWR	Drive Select	Select Drive Ø – 3
37ECRD	Disk Controller	Read Data From Disk Controller
37ECWR	Disk Controller	Write Data To Disk Controller
(active low)		

Transfer of data between the Disk Controller and CPU is accomplished by the following signals in Table 1.2.

Table 1.2

Address		37ECRD	37ECWR
A1	AØ	($\overline{RE}$)	($\overline{WR}$)
Ø	Ø	Status Register	Command Register
Ø	1	Track Register	Track Register
1	Ø	Sector Register	Sector Register
1	1	Data Register	Data Register

1.3.4 Data Separation

1.3.4.1 Internal Data Separator

FD1771 provides an internal data separation by pulling HIGH the signals, $\overline{XTDS}$ (pin 25) and FDCLOCK (pin 26). The raw READ DATA from the disk drive is fed into FDDATA (pin 27 of FD1771). Note that FD1771 has the compatibility of soft sectored recording format on the diskette.

Practical experience tells us that an external data separator is more reliable in data recovery than the internal data separation. $\overline{XTDS}$ is pulled LOW to select external data separation. The separated clock and data are fed into FDCLOCK and FDDATA respectively.

In each case, select the jumpers J1, J3 and J4 referring to the schematics and component layout diagram. Normally, these jumpers are connected in the mode of external data separation.

1.3.4.2 External Data Separator

The external data separator can be simplified as in Fig 1.3a Fig 1.3b shows the timings of the data separator.

Fig 1.3 **EXTERNAL DATA SEPARATOR**

a) Circuit

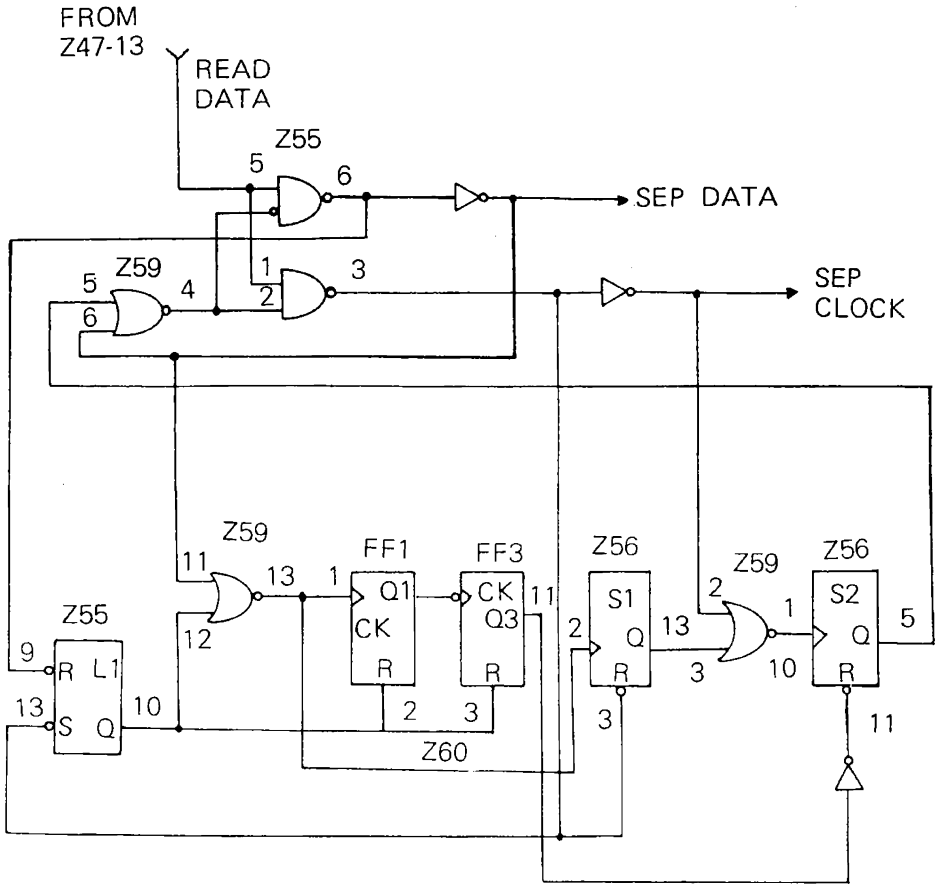
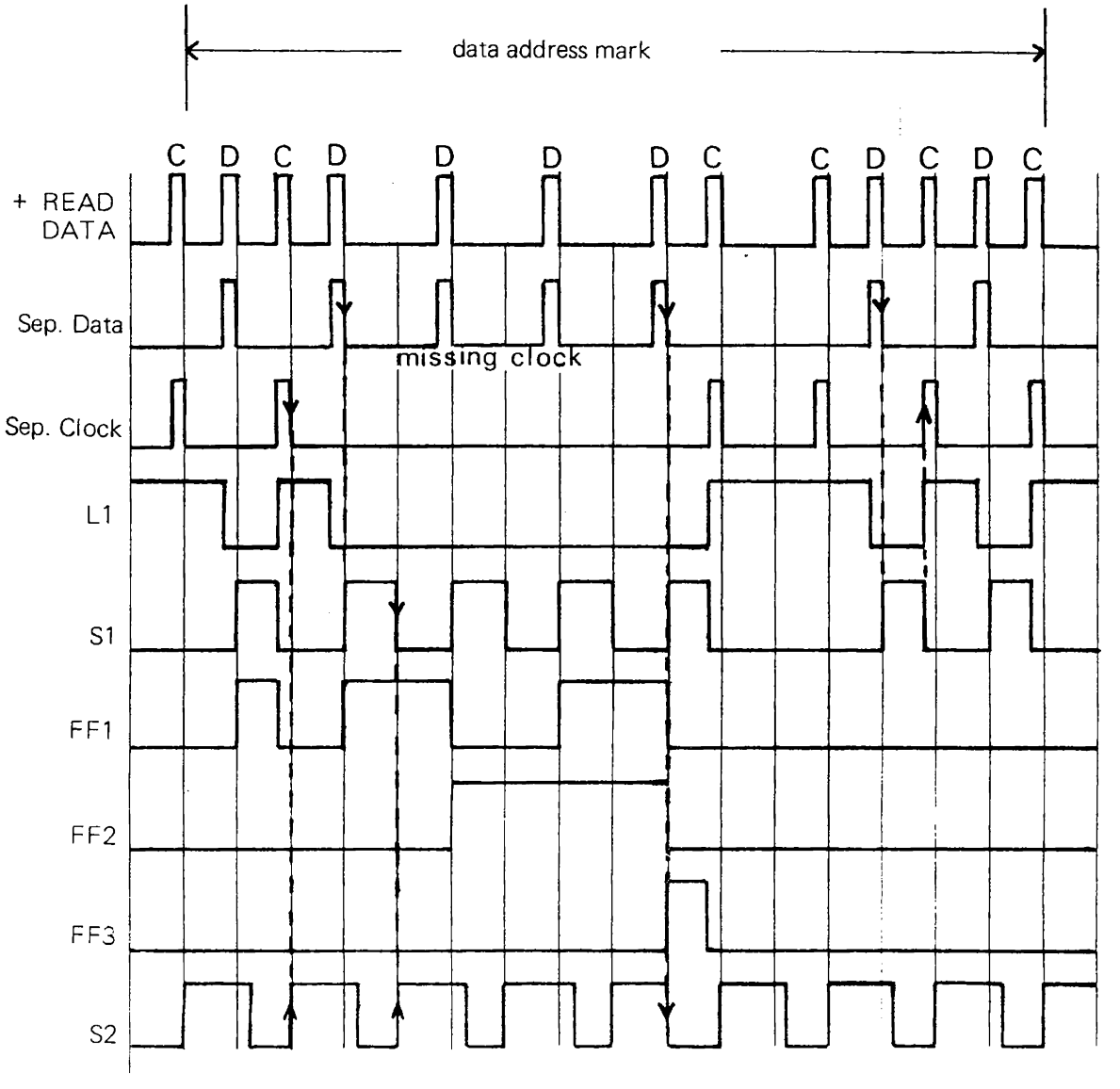


Fig 1.3 **EXTERNAL DATA SEPARATOR**

(b) Timing Diagram



The raw READ DATA which are negative-going pulses pass through Z47 (one-shot). Positive-going pulses with width of about 200 nsec. are obtained from output of Z47 (pin 13). Z55 forms a data window and a clock window for separating the data pulses and clock pulses. When Z56-5 is HIGH, the data window is opened with the clock window closed, and when Z56-5 is LOW, the clock window is opened with the data window closed.

Z56 (S2) is a one-shot with output pulse of 5 μsec in width, and Z56 (S1) has pulse width of 4 μsec. One-shot S2 is normally triggered by the falling edge of the separated clock. S1 is triggered by the falling edge of the separated data. During the missing clock period in case of data address mark, S2 is triggered to HIGH by the falling edge of S1. Therefore, the separation stays in sync through the missing clock period. At the end of three missing clocks, FF3 (Z60) will go HIGH at the falling edge of the separated data. In turn, S2 output will be reset to LOW, and this will open the clock window. Fortunately, a separated clock appears, and FF3 (Z60) is reset to a LOW level again. S2 is released from reset, and will work normally to control the clock and data windows.

1.3.5 Side Select

Since the Side Select signal is generated, double-sided drives can be used. One double-sided drive will replace two single-sided drives. This Side Select signal is derived from the Drive Select signals. For instance, jumpers in positions 2 and 4 at J5 are added. When Side Select is HIGH, the Side of diskette corresponding to DS1 and DS3 respectively are accessed. When Side Select is LOW, the sides of diskette corresponding to DS2 and DS4 respectively are accessed.

1.3.6 Card-Edge Pin Assignment for Floppy Disk Interface

(Refer to the component layout diagram)

Pin	Signal	Description
odd pins	GND	odd pins of 1 through 33 all GND
2	NC	
4	NC	
6	SIDE SELECT	To double-sided drives * cut open
8	INDEX/SECTOR	Input to FDC, active LOW
10	DS1	(Output from FDC,
12	DS2	(active LOW
14	DS3	(Drive Select 1, 2 and 3
16	MOTOR ON	Output from FDC, active LOW
18	DIR SEL	Output from FDC, step out when HIGH, step in when LOW
20	STEP	Output from FDC, active LOW-to-HIGH
22	WRITE DATA	Output from FDC, low going pulses.
24	WRITE GATE	Output from FDC, write data when LOW, read data when HIGH
26	TRACK ØØ	Input to FDC, active LOW
28	WRITE PROTECT	Input to FDC, active LOW
30	READ DATA	Input to FDC, low going pulses
32	DS4	Output from FDC, Drive Select 4, active LOW * Side Select from Q2
34	NC	

1.4 PARALLEL PRINTER INTERFACE

This 8-bit printer port is of address FDH or 37E8H and is enabled by the decoded signal $\overline{PPR}$. The serial printer port, $\overline{SPR}$, when LOW will disable this parallel printer port.

This Interface consists of a 8-bit data latch, (Z48 and Z49) and a buffer (Z53) for the status lines from the printer. There are also two one-shots (Z57); one generates the signal $\overline{DATA\ STRB}$ which strobes the data into the register of a printer, and the other generates a positive pulse at Z52-13 to activate the BUSY line, bit 7 of status lines. This positive pulse is generated just after the data are clocked into the latch, and inhibits further data transfer from the CPU to the printer before the printer sets the signal BUSY.

1.4.1 Printer Status

The status lines are assigned as below.

Bit	Status (active HIGH)
7	BUSY
6	OUT OF PAPER
5	DEVICE SELECTED
4	ALWAYS HIGH

1.4.2 Card-Edge Pin Assignment for Parallel Printer Interface

(Refer to the component layout diagram)

Pin	Signal	Pin	Signal
1	DATA STROBE	2	GND
3	DØ	4	GND
5	D1	6	GND
7	D2	8	GND
9	D3	10	GND
11	D4	12	GND
13	D5	14	GND
15	D6	16	GND
17	D7	18	GND
19	NC	20	GND
21	BUSY	22	GND
23	OUT OF PAPER	24	GND
25	UNIT SELECT	26	NC
27	NC	28	NC
29	NC	30	NC
31	NC	32	NC
33	NC	34	NC

1.5 CONNECTORS FOR FURTHER EXPANSION

There are two connectors provided on the expander board; one has 50 pins (P2) and the other 20 pins (P1). The 50-pin connector may be for S-100 bus interface board and the 20-pin connector for RS232C interface board. The positions of the connectors refer to the component layout diagram.

1.5.1 Pin Assignment for the 50-pin Connector

Pin	SIGNAL	ACTIVE LEVEL	DESCRIPTION
1	+16V		SEMI-REGULATED
2	CLOCK		2 MHz, 50% DUTY CYCLE
3	−16V		SEMI-REGULATED
4	$\overline{\text{MEMDIS}}$	L	HIGHEST 32K MEMORY DISABLE
5	+8V		SEMI-REGULATED
6	FX	L	RESERVED PORT ADDRESS
7	D4		DATA BIT 4
8	$\overline{\text{INTA}}$	L	DATA IN ENABLE
9	BD6		DATA BIT 6
10	BD5		DATA BIT 5
11	BDØ		DATA BIT Ø
12	BD7		DATA BIT 7
13	BD2		DATA BIT 2
14	BD1		DATA BIT 1
15	BA2	H	ADDRESS LINE 2
16	BD3		DATA BIT 3
17	BAØ	H	ADDRESS LINE Ø
18	BA1	H	ADDRESS LINE 1
19	BA15	H	ADDRESS LINE 15
20	BA14	H	ADDRESS LINE 14
21	BA4	H	ADDRESS LINE 4
22	BA11	H	ADDRESS LINE 11
23	BA6	H	ADDRESS LINE 6
24	BA5	H	ADDRESS LINE 5
25	BA12	H	ADDRESS LINE 12
26	BA7	H	ADDRESS LINE 7
27	BA9	H	ADDRESS LINE 9
28	BA10	H	ADDRESS LINE 10
29	BA8	H	ADDRESS LINE 8
30	BA13	H	ADDRESS LINE 13
31	Ø		MASTER CLOCK, 1.8 MHz
32	BA3	H	ADDRESS LINE 3
33	$\overline{\text{PHLDA}}$	L	PROCESSOR HOLD ACKNOWLEDGE
34	$\overline{\text{PINT}}$	L	INTERRUPT REQUEST
35	$\overline{\text{HALT}}$	L	PROCESSOR HALT ACKNOWLEDGE
36	$\overline{\text{PHANTOM}}$	L	MEMORY DISABLE FOR BOOT-STRAPPING
37	$\overline{\text{IORQ}}$	L	I/O REQUEST CYCLE
38	$\overline{\text{PWAIT}}$	L	PROCESSOR WAIT CONTROL SIGNAL

PIN	SIGNAL	ACTIVE LEVEL	DESCRIPTION
39	$\overline{WR}$	L	PROCESSOR WRITE CYCLE
40	$\overline{PHOLD}$	L	PROCESSOR HOLD CONTROL SIGNAL
41	$\overline{CCDBS/STATDBS}$	L	CONTROL SIGNALS AND STATUS DISABLE
42	$\overline{DODBS/ADDBS}$	L	DATA OUTPUTS AND ADDRESS LINE DISABLE
43	$\overline{NMI}$	L	NON-MASKABLE INTERRUPT
44	$\overline{RESET}$	L	RESET CONTROL SIGNAL
45	$\overline{M1}$	L	OP-CODE FETCH CYCLE
46	$\overline{RFSH}$	L	REFRESH CYCLE
47	$\overline{MREQ}$	L	MEMORY REQUEST CYCLE
48	RD	L	PROCESSOR READ CYCLE
49	GND		
50	GND		

1.5.2 Pin Assignment for the 20-pin Connector

PIN	SIGNAL	ACTIVE LEVEL	DESCRIPTION
1	BD5		DATA BIT 5
2	BD4		DATA BIT 4
3	BD7		DATA BIT 7
4	BD6		DATA BIT 6
5	BD1		DATA BIT 1
6	BDØ		DATA BIT Ø
7	BD3		DATA BIT 3
8	BD2		DATA BIT 2
9	$\overline{BWR}$	L	PROCESSOR WRITE CYCLE
10	BAØ	H	ADDRESS LINE Ø
11	$\overline{BRD}$	H	PROCESSOR READ CYCLE
12	$\overline{SRESET}$	L	SYSTEM RESET
13	8 MHz Ø		8 MHz, 50% DUTY CYCLE
14	SP*	L	SERIAL PORT SELECT
15	−16V		SEMI-REGULATED
16	$\overline{PPR}$	L	PARALLEL PRINTER PORT SELECT
17	+12V		REGULATED
18	+5V		REGULATED
19	$\overline{SPR}$	L	PARALLEL PRINTER DISABLE
20	GND		GROUND

1.6 POWER SUPPLY AND REGULATORS

The power supply provides three semi-regulated output voltages: +8V, +16V and −16V. The specifications for these voltages are as follows:

Voltage	No Load Voltage		Full Load Voltage		Remark
	min.	max.	min.	max.	
+8V	10.5V	11.5V	8V	9V	F.L. +8V @1.2A
+16V	20V	24V	15V	18V	F.L. +16V @150mA
−16V	20V	24V	15V	18V	F.L. −16V @100mA

There are three voltage regulators on the expander board. IC regulators 7805 (Z62) and 7812 (Z61) are used to supply +5V and +12V respectively. A simple regulator with transistor 03 and 5.6V zener diode regulates −16V to obtain −5V supply for the RAM's and FD1771.

2. EG3020 RS–232 INTERFACE

This RS-232-C Interface is an optional board to be plugged into the 20-pin connector (P1) of EG3014 expander. This board consists of six parts:

1. UART
2. Baud rate generator
3. Address decode
4. Level shifters
5. Busses
6. Voltage regulator (–12V)

2.1 UART

The UART chip used is TR1863 or AY-3-1014A which needs single +5V supply. It has 8 received data lines output to the CPU and 8 data lines input to the UART. The serial data format can be determined by properly setting the control bits. This can be done by turning ON or OFF the dip switches, S1 – S5 of DP1.

2.1.1 Control Bits

(ON = 'Ø' and OFF = '1')

2.1.1.1 No Parity (NP)

S1: logic	parity
Ø	with parity bit
1	no parity bit added

2.1.1.2 Number of stop Bits (TSB)

S2: logic	stop bit
Ø	1
1	2
1	1½ if 5 bits/character is selected.

2.1.1.3 Number of Bits/Character (NB2, NB1)

S3: NB2	S4: NB1	Bits/Character
0	0	5
0	1	6
1	0	7
1	1	8

2.1.1.4 Odd/Even Parity Select (EPS)

S5: logic	pairty
Ø	odd
1	even

2.1.2 Clock

The transmitter and the receiver use the same clock whose frequency is 16 times the desired baud rate.

2.2 BAUD RATE GENERATOR

The baud rate is obtained by dividing the 8 MHz clock, and has eight choices from 110 to 19200 baud. They can be selected by flipping the switches of DP2. Z10 and Z11 (74LS161) are programmed to be divide-by 11 and divide-by 13 respectively.

2.3 ADDRESS DECODE

The address decode is accomplished by Z1 (74LS138). SP* is a serial port enable signal with addresses F8 and/or F9. See Table 2.1. If S7 of DP1 is ON, a serial printer mode is selected, and SPR is the signal fed back to the expander board to disable the parallel printer interface.

Table 2.1 Address Decode

PORT	ADDRESS	INPUT TO CPU	OUTPUT TO INTERFACE
SERIAL INPUT	F8H	DATA	STATUS
SERIAL OUTPUT	F9H	STATUS	DATA
SERIAL PRINTER	FDH	STATUS	DATA

The mode of operation can be chosen as below.

	DP1		
MODE	S6	S7	S8
Serial Printer	OFF	ON	OFF
Communication	ON	OFF	ON

The bit assignment for status ports is illustrated in Table 2.2

Table 2.2 STATUS PORTS

DATA	COMMUNICATION		SERIAL PRINTER
BIT	OUT PORT F8H	IN PORT F9H	IN PORT FDH
DØ	Request-to-send	Data Available 1 = true	unused
D1	Data Terminal Ready	Overrun Error 1 = true	unused
D2	UART reset 1 = true	Framing Error 1 = true	unused
D3	unused	Parity Error 1 = true	unused
D4	unused	Carrier Detect	Carrier Detect
D5	unused	Data Set Ready	Data Set Ready
D6	unused	Clear-to-send	Always LOW
D7	unused	Transmitting Buffer Empty 0 = true	Transmitting Buffer Empty 0 = true

2.4 TTL/EIA LEVEL SHIFTERS

Drivers/level shifters are required to interface this RS232-C interface with data communication equipment. EIA RS232-C standard specifies that signal voltage levels should have threshold of ±3V. Logic '1' or OFF means signal voltage less than −3V, and logic '0' or ON means signal voltage greater than +3V.

Driver 1488 (Z2) with ±Vcc of ±12V is used for signals output to the RS-232-C bus. Line receiver 1489 (Z3) is used for signals inputs from the RS-232-C bus to the interface board.

2.5 BUSSES

2.5.1 The pin assignment for the RS-232-C Bus is as follows:

PIN	SIGNAL	DESCRIPTION
1	PGND	Protective Ground
2	TXD	Transmit Data (OUT)
3	RXD	Receive Data (IN)
4	RTS	Request-to-send (OUT) 'ON' – peripheral to transmit data 'OFF' – peripheral to receive (or non-transmit)
5	CTS	Clear-to-send (IN) 'ON' – peripheral can receive data. 'OFF' – no data should be transferred.
6	DSR	Data Set Ready (IN) 'ON' – peripheral handshaking completed 'OFF' – handshaking not ready
7	SGND	Signal Ground
8	CD	Carrier Detect (IN) 'ON' – peripheral is receiving a carrier 'OFF' – no carrier is received or the signal is too bad for data recognition
20	DTR	Data Terminal Ready (OUT) 'ON' – peripheral should be connected to the communication channel. 'OFF' – remove connection to the channel

2.5.2 Pin connections between the Expander and this RS-232-C Interface:

PIN	SIGNAL	DESCRIPTION
1	BD5	DATA BIT 5
2	BD4	DATA BIT 4
3	BD7	DATA BIT 7
4	BD6	DATA BIT 6
5	BD1	DATA BIT 1
6	BDØ	DATA BIT Ø
7	BD3	DATA BIT 3
8	BD2	DATA BIT 2
9	$\overline{\text{BWR}}$	PROCESSOR WRITE
10	BAØ	ADDRESS LINE Ø
11	BRD	PROCESSOR READ
12	$\overline{\text{SRESET}}$	SYSTEM RESET
13	8 MHz Ø	8 MHz, 50% DUTY CYCLE
14	SP*	SERIAL PORT SELECT
15	−16V	SEMI-REGULATED
16	$\overline{\text{PPR}}$	PARALLEL PRINTER PORT SELECT
17	+12V	REGULATED
18	+5V	REGULATED
19	$\overline{\text{SPR}}$	PARALLEL PRINTER DISABLE
20	GND	GROUND

2.6 VOLTAGE REGULATOR

+5V and +12V have been regulated on the expander board. −12V supply is required for the level shifter 1488. So, a simple regulator with Q1 (9012) and a 13V zener diode is used to supply −12V from the semi-regulated −16V.

3. EG3021 DOUBLE DENSITY ADAPTER (FLOPPY DISK)

3.1 INTRODUCTION

This optional board facilitates both single density and double density formats of floppy disk storage. It is to be plugged onto the 40-pin IC socket of Z41 (1771) of the expansion board, EG3014. Jumpers at J1-1 and J4 should be removed, and jumper at J1-2 should be connected on the expansion board.

This adapter board consists of two floppy disk controller chips, chip select decode logic and multiplexer, a 16 MHz crystal oscillator, write precompensation logic, and data separator.

3.2 FLOPPY DISK CONTROLLERS

The two chips used are FD1771 and FD1791. The FD1771 controls the operation of single density (FM) storage and the FD1791 controls the operation of double density (MFM) storage. The pin-out of FD1771 is similar to that of FD1791. Some exceptions are that FD1791 has two write precompensation outputs ie. EARLY and LATE, and does not require –5V supply.

3.3 CHIP SELECT DECODE LOGIC AND MULTIPLEXER

Z11, Z12, Z9 and Z6 form the decode logic to select either FD1771 or FD1791, and to control the division of Z4 (74LS161) of the data separator. The selection is enabled at the rising edge of the signal, 37ECWR when BD3 through BD7 are logic '1', and AØ and A1 are logic 'Ø'.

This chip select is also the selection of either single density or double density, and is assigned as below.

BDØ	Operation
Ø	single density
1	double density

The signals, STEP, DIRC, WD and WG of FD1771 and FD1791 are multiplexed by Z8 which is controlled by the chip select signal mentioned above.

3.4 16 MHz CLOCK GENERATOR

The clock generator is composed of a 16 MHz crystal and three logic inverters. This clock is required by the data separation and the write precompensation.

3.5 WRITE PRECOMPENSATION

The write precompensation is aimed at eliminating the predictable bit shift. The bit shift may be caused by some particular data patterns, and the inner tracks have greater bit shift than the outer tracks. The bit shift is compensated by shifting the bits to be written on the diskette in the opposite direction. The WRITE DATA which are expected to be early are delibrately shifted late. Also the WRITE DATA which are expected to be late are delibrately shifted early.

The circuit of write precompensation contains a delay circuit, Z13 (74LS74), and a multiplexer Z7 (74LS153). Z7 is controlled by the signals, EARLY and LATE from Z1 (FD1791).

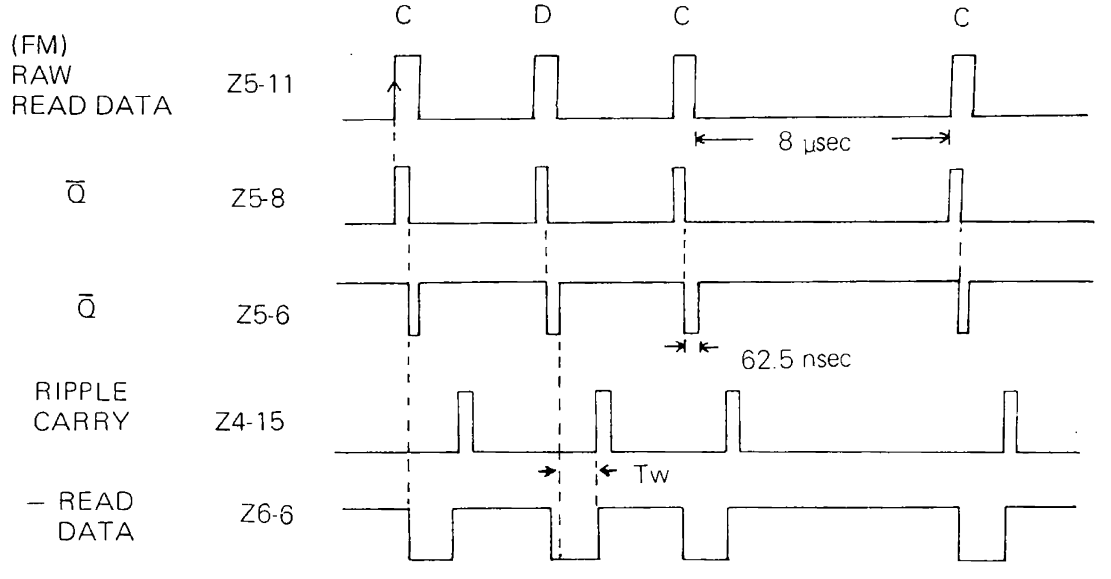
3.6 DATA SEPARATOR

Counter type data separator is employed for both single density and double density operations.

3.6.1 Single Density

The data window and clock window are controlled by the counter output, pin 11 of Z3 (74LS161). The raw READ DATA before entering the window gating passes through a pulse shaping circuit formed by Z5 and Z6 (74LS74). Assume that single density operation is enabled and Z4 pin 5 becomes logic 'Ø'. Then Z4 is a divide-by 8 counter. The operation of the pulse shaping circuit can be illustrated by the following timing diagram in Fig 3.1.

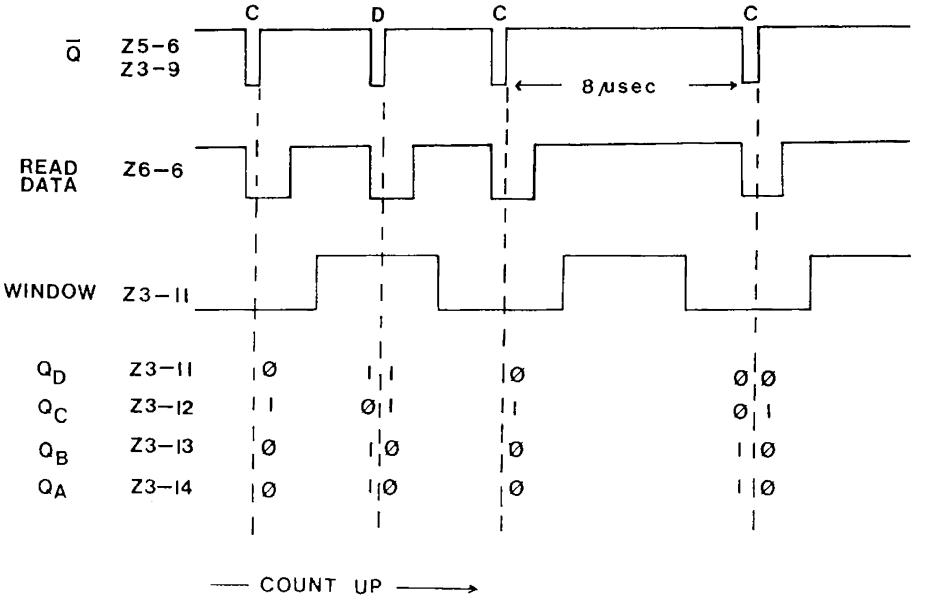
Fig 3.1 **PULSE SHAPING OF READ DATA**



Note: Tw is equal to the duration of 8 clock pulses of the 16 MHz clock, and is about 500 nsec.

During single density operation, Z4 is a divide-by eight counter. Z3 counts up by one state whenever Z4 has finished a divide-by eight counting cycle, and the RIPPLE CARRY output of Z4 becomes active HIGH. The window generated at Z3-11 can be illustrated below in Fig. 3.2.

Fig 3.2 **DATA SEPARATION – SINGLE DENSITY (FM)**



Whenever the clock pulse of a bit cell is encountered, Z3-9 becomes LOW-going and Z3 will count up from the preset state, Ø1ØØ (binary). If a data pulse is encountered, Z3 is forced to continue to count up from the state, 11ØØ. In this way, the counters Z3 and Z4 are phase-locked and synchronous with the READ DATA.

Separated data and separated clock are fed to the inputs FDDATA and FDCLOCK of FD1771 respectively.

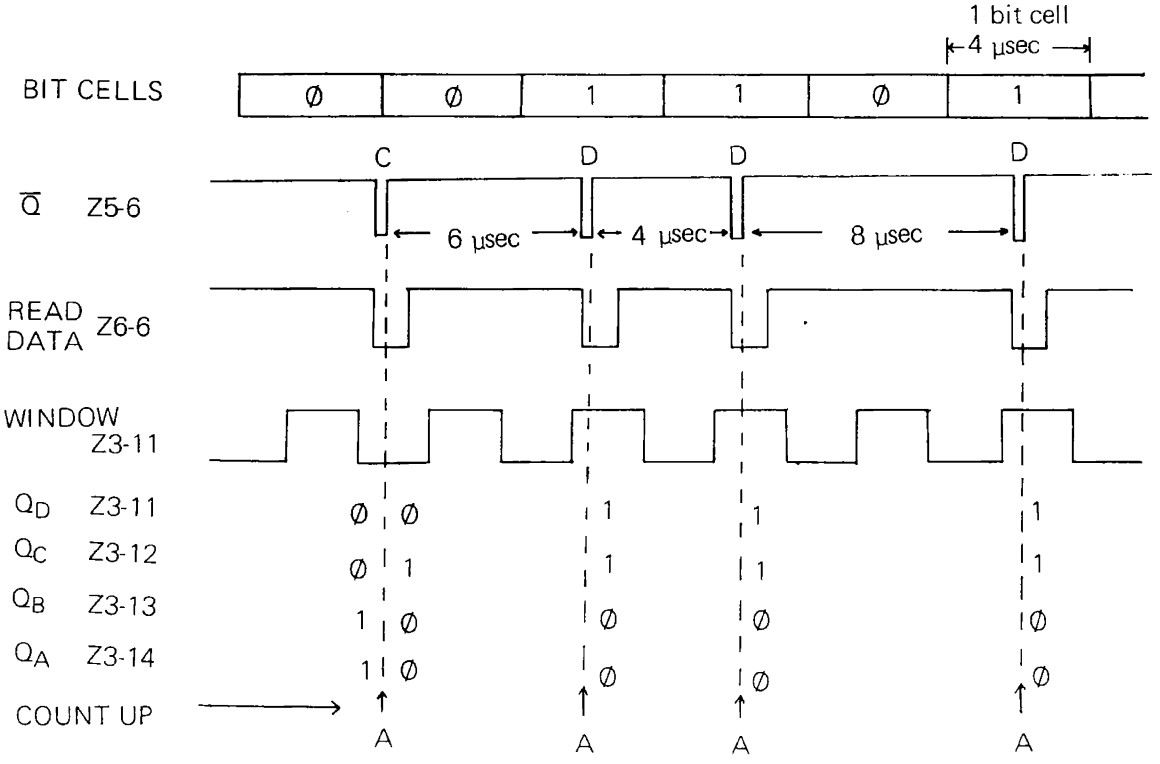
3.6.2 Double Density

During double density operation, the generation of data window is similar to that in single density operation except that the counting frequency of Z3 is doubled, and that the READ DATA is in MFM format. Z4 is programmed to become a divide-by 4 counter.

FD1791 requires two external signals for data recovery, RAW READ and READ CLOCK. Hence, READ DATA is directly applied to pin 27 of FD1791. READ CLOCK is the window required to be generated by the counters. VFOE (pin 33 of FD1791) is normally active LOW during read operation so that the window signal can be applied to the READ CLOCK input of FD1791.

The timing diagram of generating the window is shown in Fig. 3.3.

Fig 3.3 **DATA SEPARATION – DOUBLE DENSITY (MFM)**



Note: A is the phase correction point of the counters, Z3 and Z4.

Recall that MFM format follows the rule in which a clock bit is present at the leading edge of current bit cell if there is no data bit at the preceding bit cell, and if there is also no data bit at the current bit cell. Therefore, the maximum time interval between two data pulses is 8 µsec, that is, the counters may count up asynchronously with the READ DATA for a maximum period of 8 µsec.

4. EG3022 S–100 BUS INTERFACE

4.1 INTRODUCTION

This S-100 Bus Interface is an option to be added to the expander, EG3014. It is designed to be plugged into the 50-pin connector (P2) on the expander board. This interface contains a mother board of two 100-pin connectors for S-100 bus standard boards to be added.

4.2 ADDRESS LINES

There are 16 address lines from AØ to A15. They are terminated by resistor arrays, 220 ohms and 680 ohms on the mother board.

4.3 DATA LINES

The eight data lines from the expander are split into 8 DATA IN lines and 8 DATA OUT lines. These lines are buffered by Z8 and Z9 (74LS244).

4.4 CONTROL/STATUS LINES

The control/status lines of S-100 bus are generated from the expander signals by simple combinational logic gates, Z5, Z10 and Z12. Most of these lines are buffered by Z11 and Z13 (74LS244) and are terminated by resistor arrays which are on the mother board.

The signal, FX* is active LOW when any port address from F8 to FF are selected. This signal will disable the DATA IN buffer (Z8 and Z9) of the S-100 Bus.

Remark:
Port address from F8 to FF are reserved and cannot be used in S-100 BUS boards which are to be added to the expander, EG3014.

4.5 VECTORED INTERRUPT LINES

There are eight interrupt lines, and VIØ has the highest priority. These interrupt lines are encoded into a 3-bit vector (V2, V1 and VØ) by a priority encoder 74148 (Z3). The format of the interrupt vector is:

D7	D6	D5	D4	D3	D2	D1	DØ
1	1	V2	V1	VØ	1	1	1

Z3 – 15 will send out an interrupt request signal to the CPU through the line PINT when any one of the vectored interrupt lines is activated by pulling that line to a LOW level.
The interrupt acknowledge signal, SINTA when active will gate the interrupt vector into the data bus.

4.6 POWER LINES

Semi-regulated +8V, +16V and –16V dc supply lines are required in S-100 Bus. The S-100 Bus interface board contains a voltage regulator, Z1 (7805). Z1 regulates +8V supply into +5V for the TTL logic IC's of the S-100 Bus interface board.

4.7 BUS AND CONNECTOR PIN ASSIGNMENT

There are 3 connections from the expander to the S-100 Bus:

i) between the expander and the S-100 Bus interface board.
ii) between the S-100 Bus interface board and the mother board.
iii) between the mother board and the S-100 Bus.

4.7.1 Pin Assignment for the 50-pin Connector between the Expander and the S-100 Bus Interface Board

(Refer to the component layout diagram)

PIN	SIGNAL	PIN	SIGNAL
1	+16V	2	2 MHz CLOCK
3	–16V	4	$\overline{\text{MEMDIS}}$
5	+8V	6	$\overline{\text{FX*}}$
7	BD4	8	$\overline{\text{INTA}}$
9	BD6	10	BD5
11	BDØ	12	BD7
13	BD2	14	BD1
15	BA2	16	BD3
17	BAØ	18	BA1
19	BA15	20	BA14

PIN	SIGNAL	PIN	SIGNAL
21	BA4	22	BA11
23	BA6	24	BA5
25	BA12	26	BA7
27	BA9	28	BA10
29	BA8	30	BA13
31	PHI (1.78 MHz)	32	BA3
33	$\overline{\text{PHLDA}}$	34	$\overline{\text{PINT}}$
35	$\overline{\text{HALT}}$	36	$\overline{\text{PHANTOM}}$
37	$\overline{\text{IORQ}}$	38	$\overline{\text{PWAIT}}$
39	$\overline{\text{WR}}$	40	$\overline{\text{PHOLD}}$
41	$\overline{\text{CCDBS/STATDBS}}$	42	$\overline{\text{DODBS/ADDBS}}$
43	$\overline{\text{NMI}}$	44	$\overline{\text{RESET}}$
45	$\overline{\text{M1}}$	46	$\overline{\text{RFSH}}$
47	$\overline{\text{MREQ}}$	48	$\overline{\text{RD}}$
49	GND	50	GND

4.7.2 Pin Assignment for the Connectors between the S-100 Bus Interface Board and the Mother Board

(Refer to the component layout diagram)

4.7.2.1 50-pin PCB Solder-to-board Connector

PIN	SIGNAL	PIN	SIGNAL
1	$\overline{\text{VI1}}$	26	NC
2	GND	27	$\overline{\text{ADSB}}$/$\overline{\text{DOSB}}$
3	+16V	28	$\overline{\text{HOLD}}$
4	+5V	29	NC
5	$\overline{\text{VI2}}$	30	PHI (1.78 MHz)
6	$\overline{\text{VIØ}}$	31	$\overline{\text{PHLDA}}$
7	−16V	32	$\overline{\text{PWR}}$
8	+8V	33	NC
9	$\overline{\text{VI6}}$	34	$\overline{\text{RESET}}$
10	$\overline{\text{VI5}}$	35	PDBIN
11	$\overline{\text{VI4}}$	36	A5
12	$\overline{\text{VI3}}$	37	NC
13	MREQ	38	NC
14	NC	39	AØ
15	$\overline{\text{NMI}}$	40	A4
16	$\overline{\text{VI7}}$	41	A1
17	$\overline{\text{CDSB}}$/$\overline{\text{SDSB}}$	42	D01
18	MWRT	43	A3
19	$\overline{\text{CDSB}}$/$\overline{\text{SDSB}}$	44	A15
20	$\overline{\text{PHANTOM}}$	45	A12
21	$\overline{\text{REFSH}}$	46	A9
22	GND	47	A2
23	GND	48	A6
24	$\overline{\text{ADSB}}$/$\overline{\text{DOSH}}$	49	A7
25	$\overline{\text{INT}}$	50	A8

Note: description of these signals refers to Section 4.7.3

4.7.2.2 34-pin PCB Solder-to-board Connector

PIN	SIGNAL	PIN	SIGNAL
1	A1Ø	18	NC
2	A14	19	NC
3	DOØ	20	NC
4	A13	21	NC
5	D05	22	NC
6	D02	23	DIØ
7	D04	24	SOUT
8	A11	25	DI1
9	DI2	26	SM1
10	D07	27	SMEMR
11	DO6	28	SINTA
12	DO3	29	SINP
13	DI5	30	$\overline{\text{SWO}}$
14	DI3	31	$\overline{\text{POC}}$
15	DI4	32	2 MHz CLOCK
16	DI6	33	SHLTA
17	DI7	34	GND

Note: description of these signals refers to Section 4.7.3

4.7.3 Pin Assignment for the S-100 Bus Connector on the Mother Board
(Refer to the component layout diagram)

PIN	SIGNAL	ACTIVE LEVEL	DESCRIPTION
1	+8V		semi-regulated, max 2A
2	+16V		semi-regulated, max 500mA
3	NC		
4	$\overline{\text{VI0}}$	LO/C	vectored interrupt line Ø — line 7
5	$\overline{\text{VI1}}$	LO/C	
6	$\overline{\text{VI2}}$	LO/C	
7	$\overline{\text{VI3}}$	LO/C	
8	$\overline{\text{VI4}}$	LO/C	
9	$\overline{\text{VI5}}$	LO/C	
10	$\overline{\text{VI6}}$	LO/C	
11	$\overline{\text{VI7}}$	LO/C	
12	NMI	LO/C	Non-maskable interrupt
13	NC		
14	NC		
15	NC		
16	NC		
17	NC		
18	$\overline{\text{SDSB/CDSB}}$	LO/C	Status signals and control signals disable
19	$\overline{\text{SDSB/CDSB}}$		
20	GND		

PIN	SIGNAL	ACTIVE LEVEL	DESCRIPTION
21	$\overline{\text{REFSH}}$	L	Dynamic Ram refreshing signal
22	$\overline{\text{ADSB/DOSB}}$	LO/C	Address lines and data output disable
23	$\overline{\text{ADSB/DOSB}}$		
24	Ø		Master clock, 1.7 MHz
25	NC		
26	PHLDA	H	Processor HOLD acknowledge
27	NC		
28	NC		
29	A5	H	Address line 5
30	A4	H	Address line 4
31	A3	H	Address line 3
32	A15	H	Address line 15
33	A12	H	Address line 12
34	A9	H	Address line 9
35	DO1		Data out bit 1
36	DOØ		Data out bit Ø
37	A1Ø		Address line 1Ø
38	DO4		Data out bit 4
39	DO5		Data out bit 5
40	DO6		Data out bit 6
41	DI2		Data in bit 2
42	DI3		Data in bit 3
43	DI7		Data in bit 7
44	SM1	H	Op-code fetch cycle
45	SOUT	H	I/O out control signal
46	SINP	H	I/O in control signal
47	SMEMR	H	Memory read cycle
48	SHLTA	H	Process halt acknowledge
49	CLOCK		2 MHz, 50% duty cycle
50	GND		
51	+8V		
52	−16V		Semi-regulated, max 100mA
53	GND		
54	NC		
55	NC		
56	NC		
57	NC		
58	NC		
59	NC		
60	NC		
61	NC		
62	NC		
63	NC		
64	NC		
65	$\overline{\text{MREQ}}$		Memory request cycle
66	NC		
67	PHANTOM	LO/C	Phantom enable for bootstrapping
68	MWRT	H	Memory write control signal
69	NC		
70	GND		
71	NC		
72	NC		

PIN	SIGNAL	ACTIVE LEVEL	DESCRIPTION
73	$\overline{\text{INT}}$	LO/C	Primary interrupt request
74	$\overline{\text{HOLD}}$	LO/C	Bus hold control signal
75	$\overline{\text{RESET}}$	LO/C	Reset control signal
76	NC		
77	$\overline{\text{PWR}}$	L	Processor write control signal
78	PDBIN	H	Processor read control signal
79	AØ	H	Address line Ø
80	A1	H	Address line 1
81	A2	H	Address line 2
82	A6	H	Address line 6
83	A7	H	Address line 7
84	A8	H	Address line 8
85	A13	H	Address line 13
86	A14	H	Address line 14
87	A11	H	Address line 11
88	DO2	H	Data out bit 2
89	DO3	H	Data out bit 3
90	DO7	H	Data out bit 7
91	DI4	H	Data in bit 4
92	DI5	H	Data in bit 5
93	DI6	H	Data in bit 6
94	DI1	H	Data in bit 1
95	DIØ	H	Data in bit Ø
96	SINTA	H	Interrupt acknowledge
97	$\overline{\text{SWO}}$		Processor write cycle
98	NC		
99	$\overline{\text{POC}}$	L	Power on clear signal
100	GND		

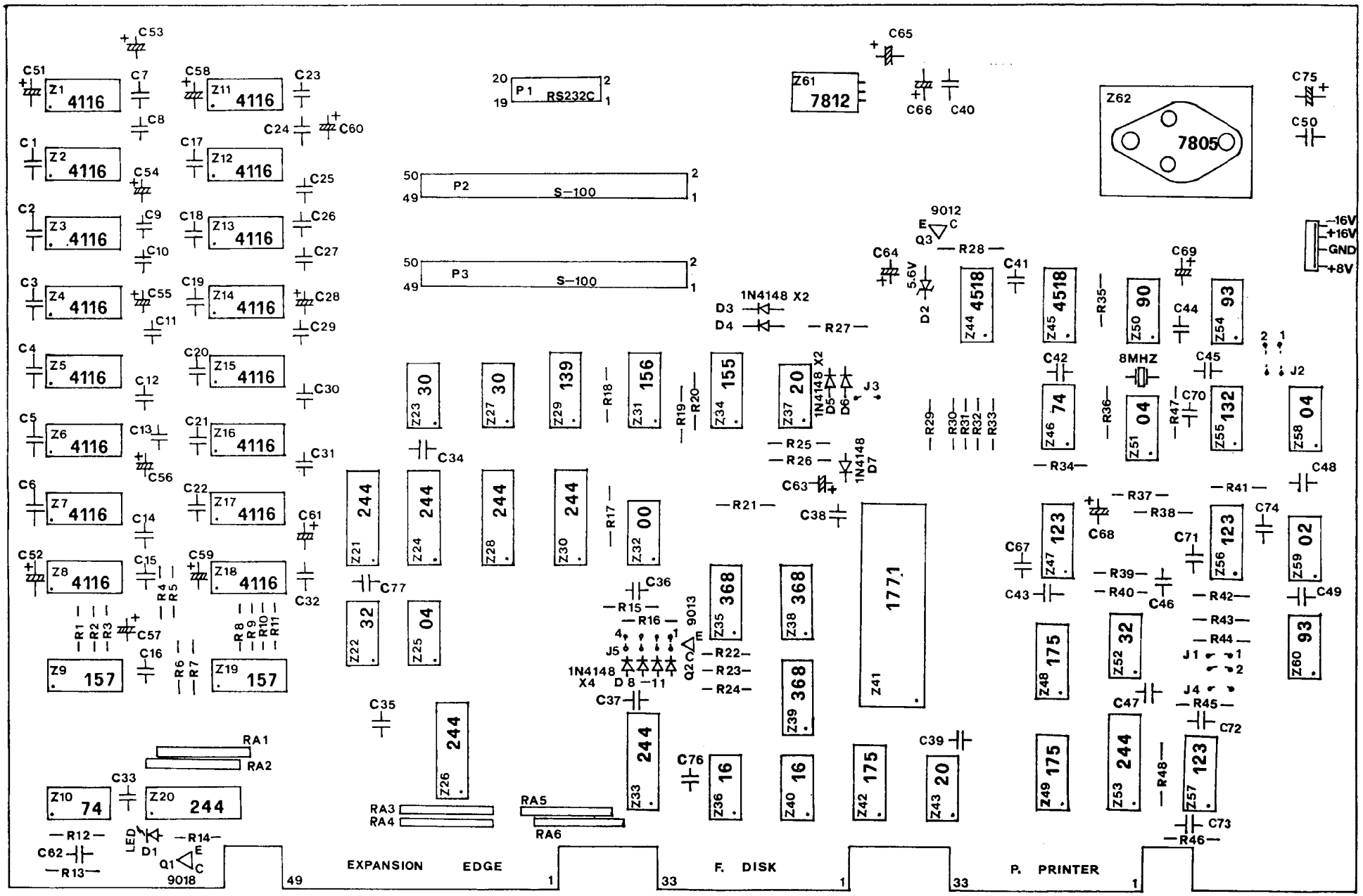
5. COMPONENT LAYOUT DIAGRAM

EG3014

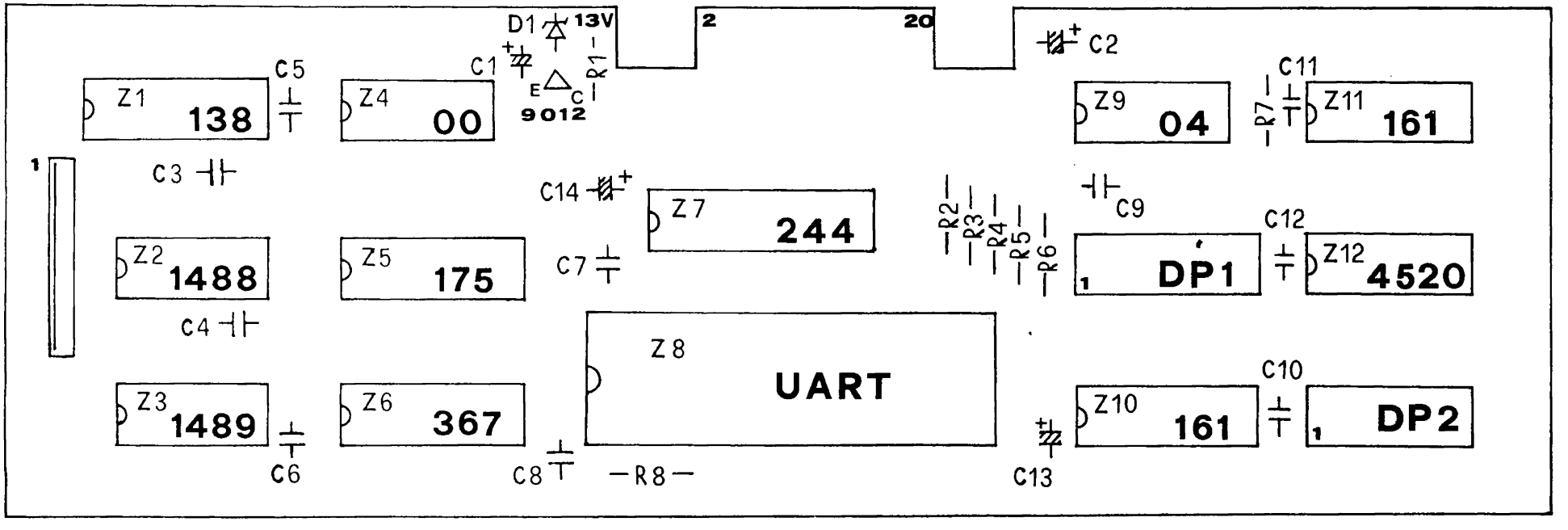
EG3020

EG3021 and

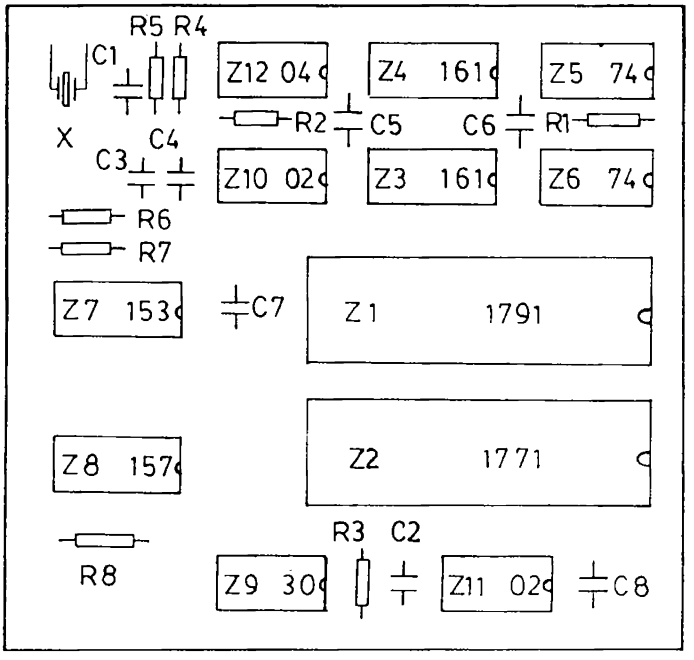
EG3022



EG3014 EXPANDER

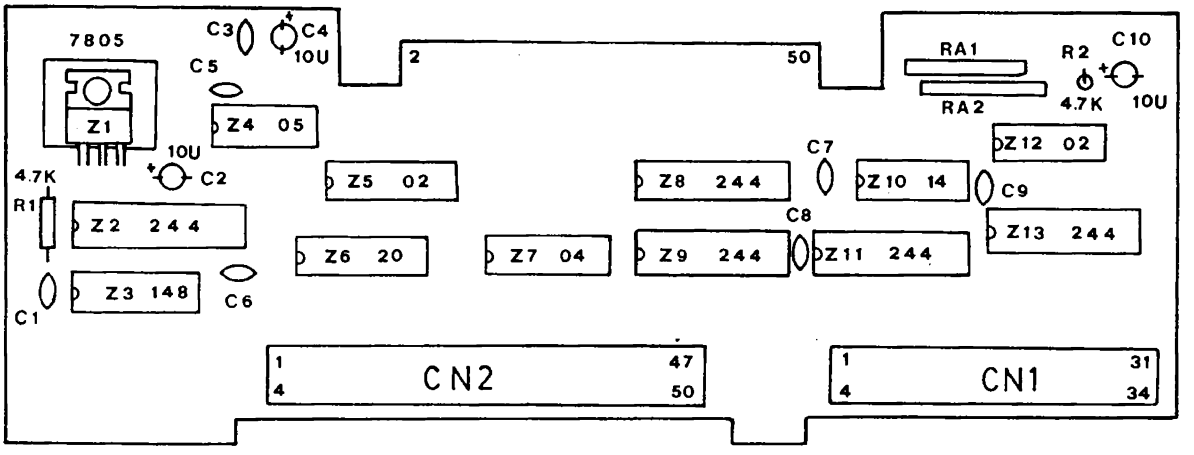


EG3020 RS-232-C INTERFACE

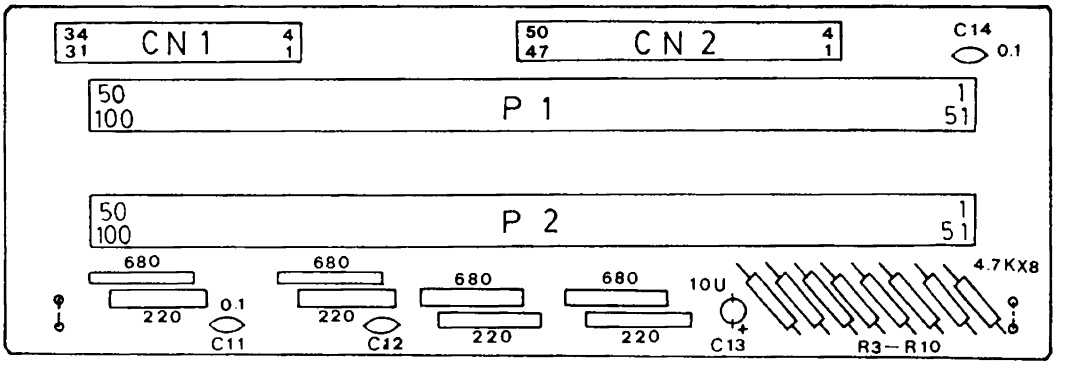


EG-3021 LAYOUT DIAGRAM

EG 3021 DOUBLE DENSITY ADAPTER (FLOPPY DISK)



S-100 INTERFACE



MOTHER BOARD

EG3022 S-100 BUS INTERFACE

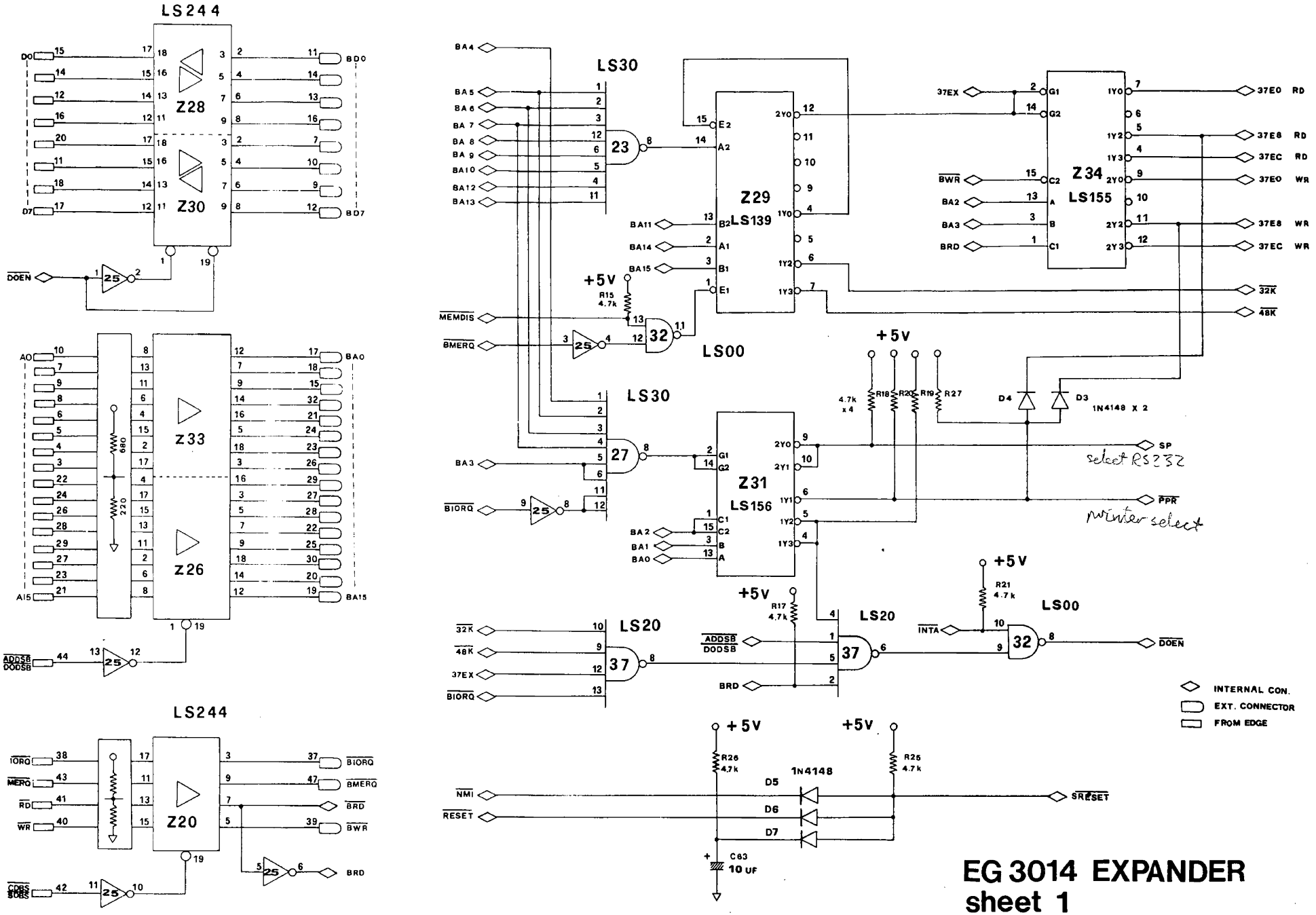
6. SCHEMATICS

EG3014

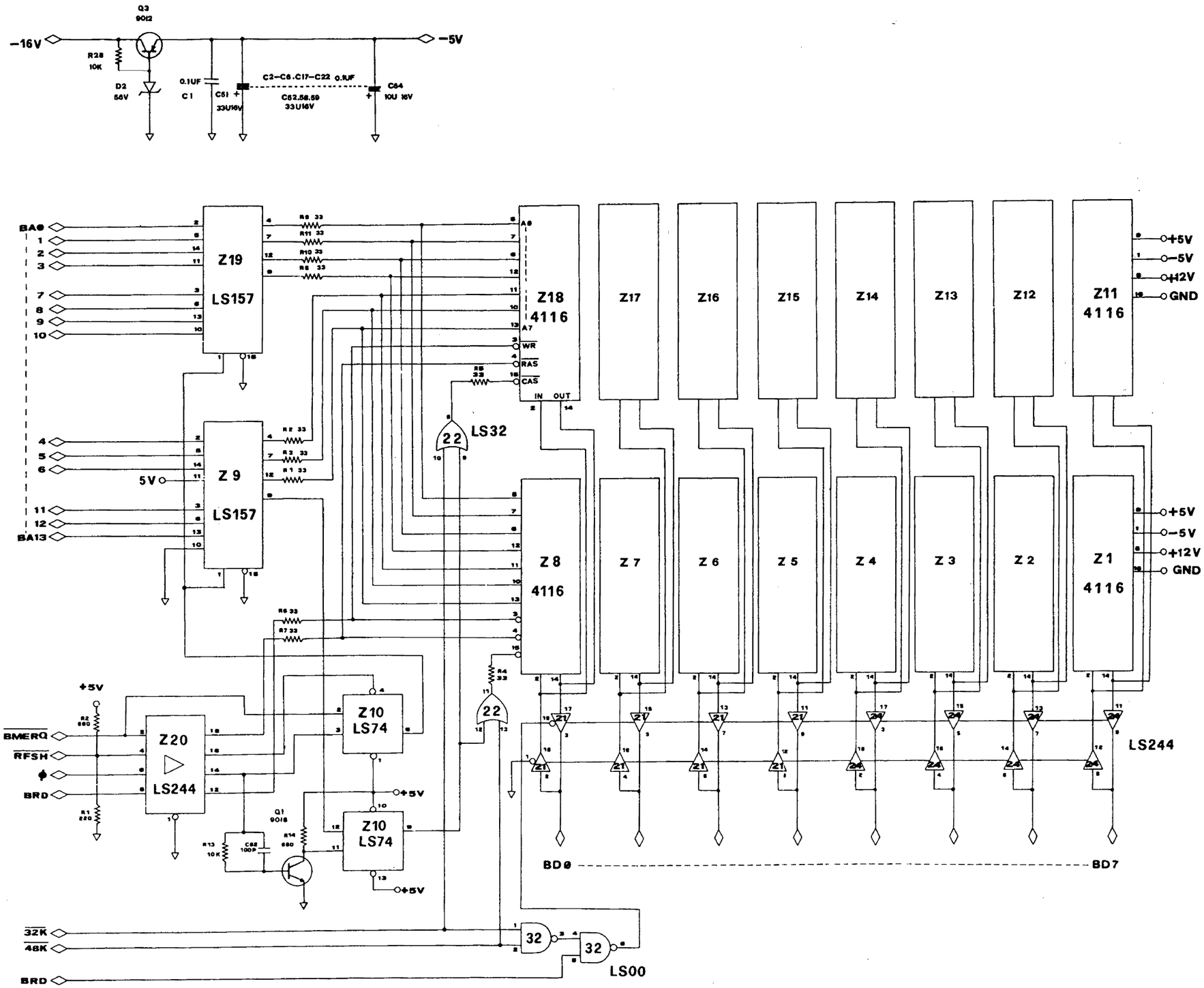
EG3020

EG3021 and

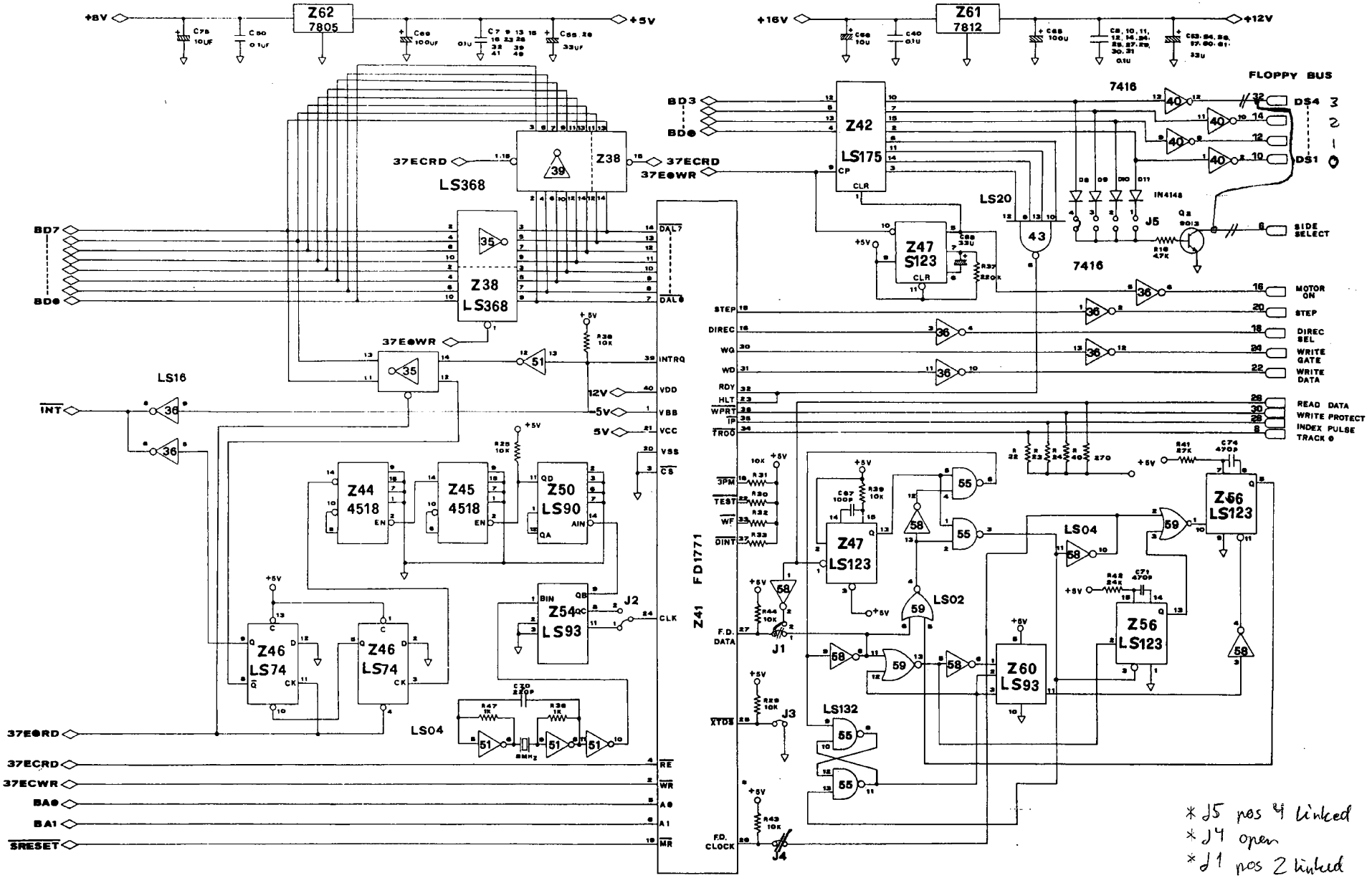
EG3022



EG 3014 EXPANDER
sheet 1



EG3014 EXPANDER
sheet 2


+8V
Z62
7805
+5V
+16V
Z61
7812
+12V
FLOPPY BUS
7416
Z42
LS175
LS368
Z38
37ECRD
37E●WR
BD7
BD●
Z47
S123
LS20
IN4148
J5
SIDE SELECT
MOTOR ON
STEP
DIREC SEL
WRITE GATE
WRITE DATA
READ DATA
WRITE PROTECT
INDEX PULSE
TRACK 0
LS16
INT
INTRQ
VDD
VBB
VCC
VSS
CS
Z44
4518
Z45
4518
Z50
LS90
Z54
LS93
J2
CLK
Z46
LS74
LS04
LS02
LS132
Z60
LS93
Z56
LS123
Z41 FD1771
F.D. DATA
F.D. CLOCK
J1
J3
J4
RE
WR
A0
A1
MR
SRESET
BA0
BA1
37ECWR
* J5 pos 4 linked
* J4 open
* J1 pos 2 linked
pos 1 open
EG3014 EXPANDER
sheet 3

PRINTER BUS

5V

R18 4.7K

52

21 BUSY

Z53 LS244

23 OUT PAPER

25 UNIT SEL

GND
2 4 6 8 10 12
14 16 18 20 22 24

BD7

Z48 LS175

17 DATA 8

15

13

11 DATA 5

N.C.
others

BDØ

Z49 LS175

9 DATA 4

7

5

3 DATA 1

C73 02u

R46 100K

Z57 LS123

02

59

BRD

52

PPR

48

LS32

R34 4.7K

01

51

SPR

from RS232

52

BWR

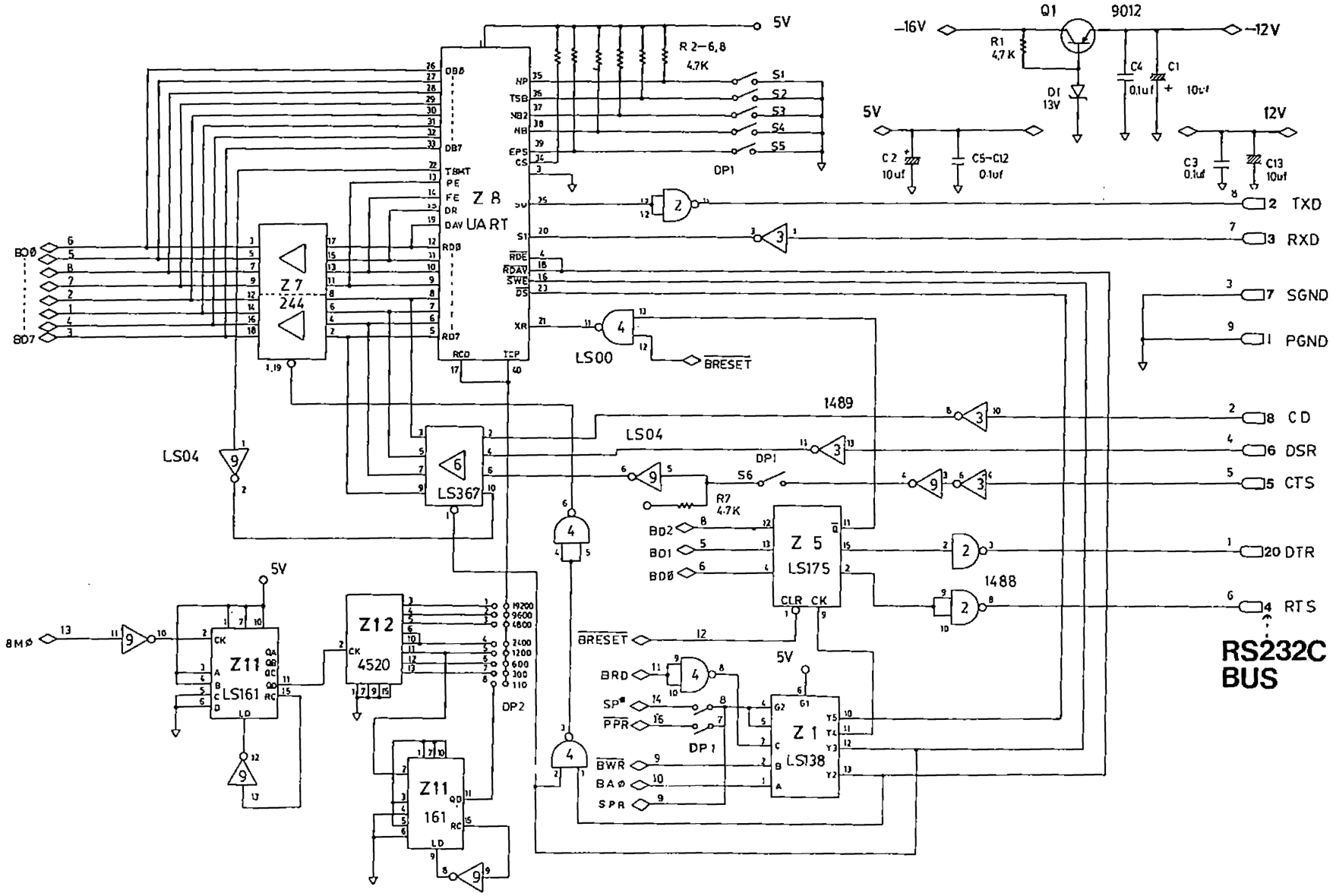
C72 220p

R45 20K

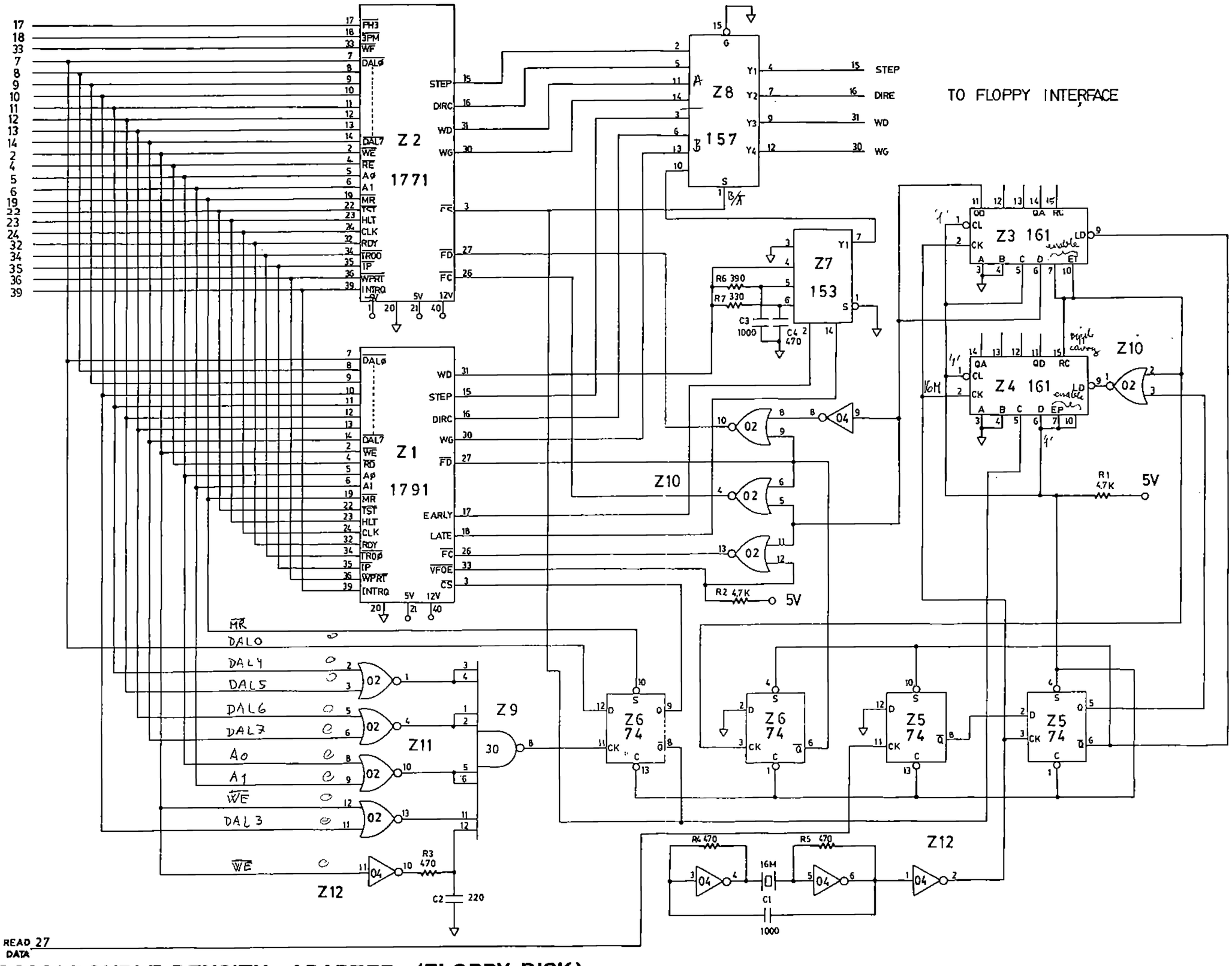
Z57 LS123

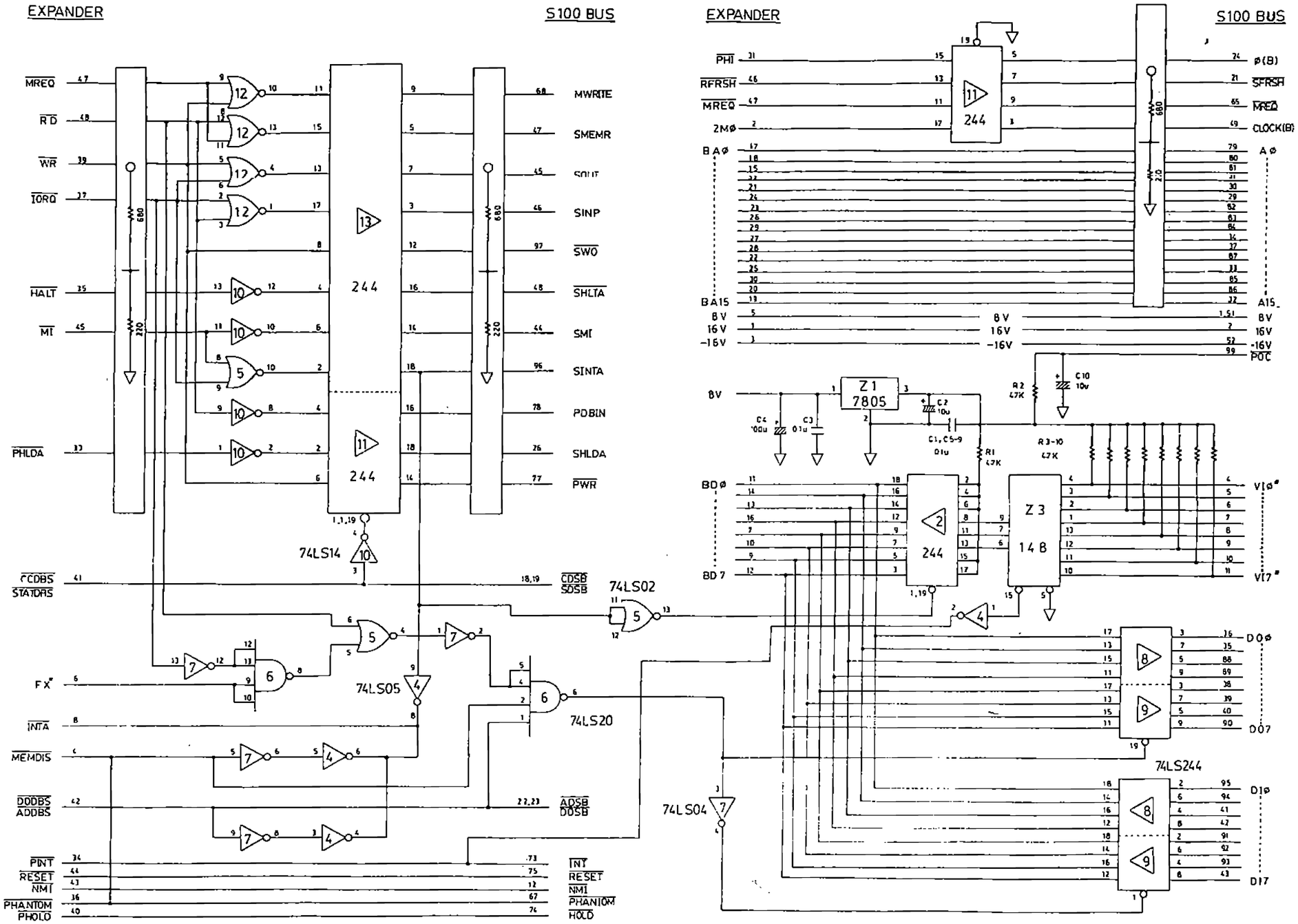
1 DATA STRB

EG3014 EXPANDER
sheet 4



EG3020 RS-232-C INTERFACE


TO FLOPPY INTERFACE
Z2 1771
Z1 1791
Z8 157
Z7 153
Z3 161
Z4 161
Z10
Z9
Z11
Z12
Z6 74
Z5 74
STEP
DIRC
WD
WG
EARLY
LATE
VFOE
R6 390
R7 330
C3 1000
C4 470
R1 4.7K
R2 4.7K
R3 470
R4 470
R5 470
C1 1000
C2 220
16M
5V
12V
DAL0
DAL4
DAL5
DAL6
DAL7
A0
A1
MR
WE
READ DATA



EG3022 S—100 BUS INTERFACE

APPENDIX

A

Pin Connections between the Expander and the Video Genie System.

PIN	SIGNAL	PIN	SIGNAL
1	GND	2	GND
3	A7	4	A6
5	A5	6	A4
7	A1	8	A3
9	A2	10	A0
11	D5	12	D2
13	NC	14	D1
15	D0	16	D3
17	D7	18	D6
19	+5V	20	D4
21	A15	22	A8
23	A14	24	A9
25	NC	26	A10
27	A13	28	A11
29	A12	30	PHI
31	$\overline{\text{PINT}}$	32	NC
33	NC	34	$\overline{\text{PHLDA}}$ or $\overline{\text{BA}}$
35	$\overline{\text{PHANTOM}}$	36	$\overline{\text{HALT}}$
37	$\overline{\text{PWAIT}}$	38	$\overline{\text{IORQ}}$
39	$\overline{\text{PHOLD}}$	40	$\overline{\text{WR}}$
41	$\overline{\text{RD}}$	42	$\overline{\text{CCDBS/STADBS}}$
43	$\overline{\text{MREQ}}$	44	$\overline{\text{DODBS/ADDBS}}$
45	$\overline{\text{M1}}$	46	$\overline{\text{RESET}}$
47	$\overline{\text{RFSH}}$	48	$\overline{\text{NMI}}$
49	GND	50	GND

Note: For the pin positions, refer to the component layout diagram.

EACA INTERNATIONAL LTD

13 Chong Yip Street

Eaca Industrial Building

Kwun Tong, Kowloon, HONG KONG

Telex: 54035 ECHK HX

Cable: "ECHUNG" H.K.

Tels: 3-896323 (8 Lines)