EPSON

TECHNICAL MANUAL

PX-8

H8490021-

INTRODUCTION

The EPSON PX-8 is a general-purpose portable computer driven by an incorporated rechargeable battery. Standard features include a micro cassette drive, ROM capsule and RS-232C interface allowing the machine to independently handle a variety of applications. The system can also be expanded by connecting peripheral equipment such as a printer. Long time steady operation has been realized by employing the battery-powered supply system with its large capacity of 1100 mAH. A recharge control circuit to protect the battery from overcharge and an auxiliary battery (90 mAH) for backup have been added to enhance reliability.

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CHAPTER 1
GENERAL DESCRIPTION

1.1 Specifications

(1) Dimension: 297 mm (width) x 216 mm (depth) x 4 7mm (height)

(2) Weight: Approx. 2.3 kg

(3) Environment:

- Temperature

Operating	5 ~ 35°C
Recharging	5 ~ 35°C
Not operating	−20 ~ 60°C (below 30°C for a long period of time)
Storing data (not operating)	0 ~ 40°C

- Humidity

Operating	10 ~ 80% (non-condensing)
Not operating	5 ~ 85% (non-condensing)

(4) Power:

- Consumption: Approx. 325 mW (when micro cassette, speaker, ROM capsule, RS-232C, SERIAL are not operating)
- Battery: Two Ni-cd rechargeable batteries

	Main battery	Auxiliary battery
Voltage	4.8V	4.8V
Capacity	1100 mAH	90 mAH
Charging current	330 mA MAX.	10 mA MAX.
Charging voltage	5.6 ~ 6.4V	5.7 ~ 6.0V

- AC adapter output: 6.0V, 600 mA

(5) Keyboard: 72 keys (include 9 function keys)
3 mode indication lamps

(6) LCD: 480 (width) x 64 (height) dots (80 x 8 characters per screen)
1/64 duty, adjustable VIEW ANGLE

(7) Microcassette™:

Tape speed	2.4 cm/s
Drive	Center capstan
Track	Two-truck, one-channel
Frequency characteristic	315 ~ 4KHz
Data file	Sequential file with directory

(8) Interface

- RS-232C:

Connector	8-pin mini-DIN connector
Voltage	±8V (ON/OFF control by software)
Transmission speed	75 ~ 19200 BPS
Mode	Full duplex/half duplex

- SERIAL:
  - Connector: 8-pin mini-DIN connector
  - Voltage: ±8V (ON/OFF control by software)
  - Transmission speed: 150, 600, 4800, 38.4K BPS
- Speaker: Audio response controlled by software or by micro cassette (with adjustable volume)
- Analog input:
  - Input voltage: 0 ~ 2.0V
  - A/D converter: 6-bit (Resolution: approx. 0.03V)
- Bar code: Can connect to high-resolution (0.19mm) or low-resolution (0.33mm).

(9) CPU and memory

- Main CPU: Z-80, 2.45MHz
- Slave CPU: 6303, 614kHz
- Auxiliary CPU: 7508, 200kHz (with battery backup)
- Main RAM: 64kB D-RAM (with battery backup)
- Video RAM: 6kB static RAM (with battery backup)
- ROM: 32kB
- ROM capsule: Two capsules can be incorporated. (8 ~ 32kB per capsule)

1.1.1 Available models

The following models are available for this computer. However, major differences among these models are restricted to keyboard and AC adaptor specifications, the internal hardware is the same.

Table 1-1

Model	Keyboard	AC adaptor
H101A AA	ASCII (U.S.A.)	H00AAA: 120V 60 Hz
H101A AC	ASCII	H00AAA: 120V 60 Hz, H00AAU-B: 240V 50 Hz, H00AAU-A: 240V 50 Hz
H101A BA	HASCII (U.S.A.)	H00AAA: 120V 60 Hz
H101A UA	England	H00AAU-A: 240V 50 Hz
H101A FA	France	H00AAF: 220V 50 Hz
H101A GA	Germany	H00AAG: 220V 50 Hz
H101A SA	Sweden	H00AAG: 220V 50 Hz
H101A DA	Denmark	H00AAG: 220V 50 Hz
H101A NA	Norway	H00AAG: 220V 50 Hz

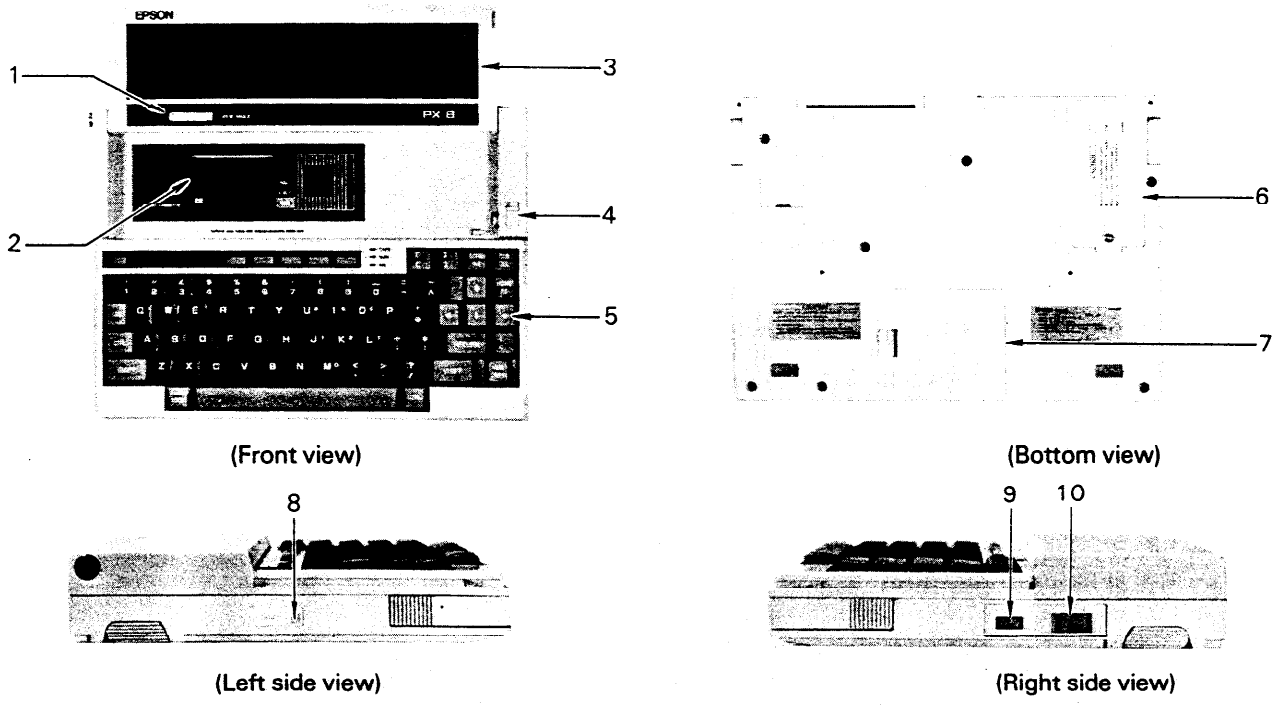
1.1.2 Specifications of option

Optional features are summarized in the table below. They provide you with system expansion to meet your specific demands or flexible system configuration by using universal option.

Table 1-2

Name	Application/Descriotion
#723 cable	For floppy disk drive (serial)
#724 cable	For acoustic coupler (RS-232C)
#725 cable	For printer (RS-232C)
#726 cable	Null modem (for interconnection between two EPSON PX-8 computers via RS-232C interfacing)
CX-20/21	Acoustic coupler
PF-10	3.5 inch floppy disk drive
TF-15/TF-20	5.25 inch floppy disk drive
RAM DISK UNIT	Additional 120/60 kB RAM
UNIVERSAL UNIT	A through-hole circuit board and a case
MODEM UNIT	Built-in modem (for U.S.A. only)
MULTI UNIT	RAM + MODEM (for U.S.A. only)
EPSON PRINTER	Verious models with RS-232C interface

1.2 Names of Major Parts



(Front view)

(Bottom view)

(Left side view)

(Right side view)

(Rear side view)

Fig. 1-1

Table 1-3 Major Component

No.	Name
1	VIEW ANGLE VOLUME (adjustable view angle due to temperature complement)
2	Microcassette (program load/save and sound generation)
3	LCD panel unit
4	LCD panel open switch
5	Keyboard unit
6	Battery cover (to replace main battery)
7	ROM cartridge cover (for replacement of ROM capsule, and INITIAL RESET)
8	Reset switch
9	Speaker volume (internal/external speaker volume adjustment)

No.	Name
10	Power switch
11	Speaker output (for external speaker)
12	Analog input interface (analog input/ joystick)
13	Bar code reader interface
14	RS-232C interface (for connection to acoustic coupler/printer, etc.)
15	High-speed serial interface (for connection to floppy disk drive)
16	Expansion interface (for connection to optional unit/universal unit)

1.3 Major parts

The main unit consists of five parts and a case as shown in Fig. 1-2.

① MAPLE board

A control board realizing compact size and low power consumption with CMOS, flat package type multifunction gate arrays and various chips on it.

② Micro cassette

Consists of control board and driving mechanism. Reads and writes data from and to the tape.

③ Keyboard

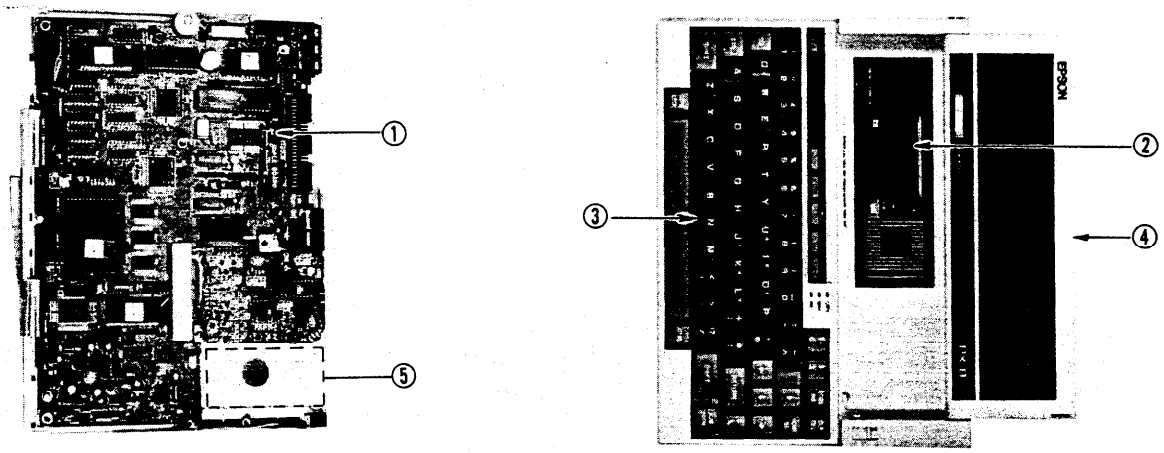
Has 72 keys on it (73 keys for Japanese use), 9 of which are function keys. Also has three indicators which show the input mode.

④ LCD

Consists of 480 (width) x 64 (height) dots, can display a total of 480 characters.

⑤ Main battery

A rechargeable Ni-cd battery with a capacity of 1100 mAH. It supplies power necessary for the normal circuit operation.

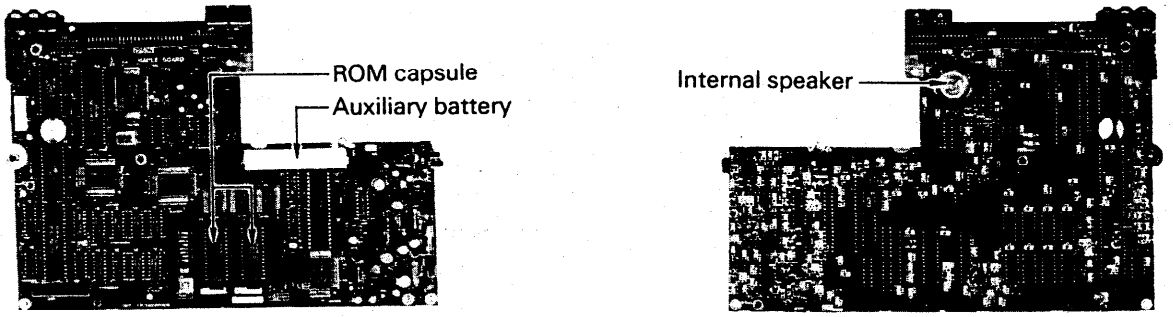


Bottom side

Fig. 1-2

1.3.1 MAPLE board

Power consumption is considerably reduced by employing power-saving C-MOS. On-board integration has become easy by employing customized LSIs and chips. Although both sides of the boards are utilized, the back side mainly includes chips such as resistors and capacitors.



Front view

Rear view

Fig. 1-3

External interfaces (shown in Table 1-4) and two ROM capsules on the board provide a system configuration suitable for your needs or implementation of an application program. An auxiliary rechargeable battery of 90 mAH is also incorporated which supplies power in order to ensure normal circuit operation when the voltage of the main battery falls down below a certain value.

Table 1-4 External Interfaces

Item	Function	Note
RS-232C	110 ~ 19200 BPS, RS-232C level	Operator-selectable: transmission speed, X-ON/OFF, etc.,
SERIAL	38400 BPS MAX., RS-232C level	Operator-selectable: transmission speed, X-ON/OFF, etc.,
Bar code	Read at TTL level	Read program and bar code reader are required.
Analog input	Analog or joystick input (with trigger)	Analog input line has +5V pull up function.
External speaker	0 ~ 6V output	8Ω 0.2W

1.3.2 Microcassette

The microcassette consists of a control board and drive mechanism. Operations such as FF, REW, etc. are controlled by software, resulting in high reliability compared with manual control. Increased chip implimentation has permitted a reduction in size of the control board.
This cassette drive operates at a tape speed of 2.4 cm/s, and reads or writes data effectively utilizing a tape counter and directory which contains file names, file starting addresses, etc.

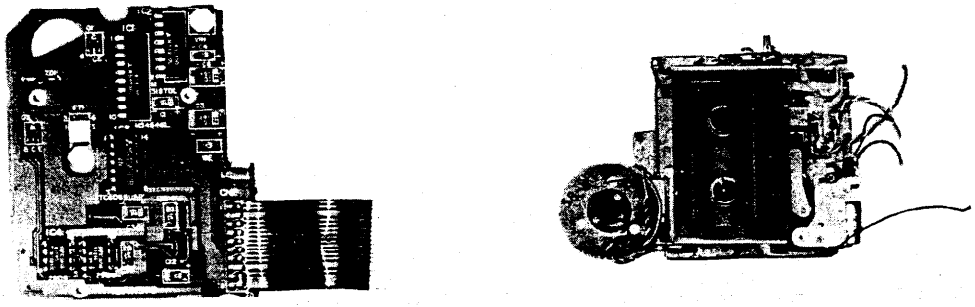


Fig. 1-4

Mechanical components include a tape drive motor and its driving mechanism, R/W heads and their mechanisms, reels, etc. The control board controls the revolving speed of motor, load/unload of R/W heads and R/W operation.
To enable sound output, it provides signals to an internal or external speaker after amplifying them twice. For reading data, duplicated amplification circuits eliminate high frequency component (noise) and detect the peak of signal to ensure highly reliable sound output.

1.4 Interface

As shown in Table 1-3, the unit has eleven connectors: among them, CN3, CN4 and CN5 have a slide-lock mechanism.

Table 1-5 Interface Connectors

Name	Number of pins	Function
CN1	3	AC adapter connection interface
CN2	2	Main battery connection interface
CN3	20	Incorporated microcassette interface
CN4	22	Keyboard interface
CN5	16	LCD interface
CN6	8	High speed serial interface
CN7	8	RS-232C interface
CN8	50	Expansion interface
CN9	3	Bar code reader interface
CN10	3	Analog input interface
CN11	2	External speaker interface

Note: CN5 is integrated on the back of MAPLE board.

Table 1-6 CN1 (AC Adaptor) Pin Assignments

Pin No.	Signal name	Definition
1	VCH	Charging voltage
2	—	Undefined
3	GND	Ground

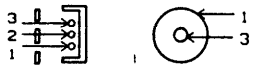


Table 1-7 CN2 (Battery Connection) Pin Assignments

Pin No.	Signal Name	Definition
1	VB	Main battery voltage
2	GND	Ground

1.3.3 Keyboard

Matrix keyboard uses mechanical contact switches. Switches, reverse-current protection diode and mode indication LED lamps are implemented on the control board.

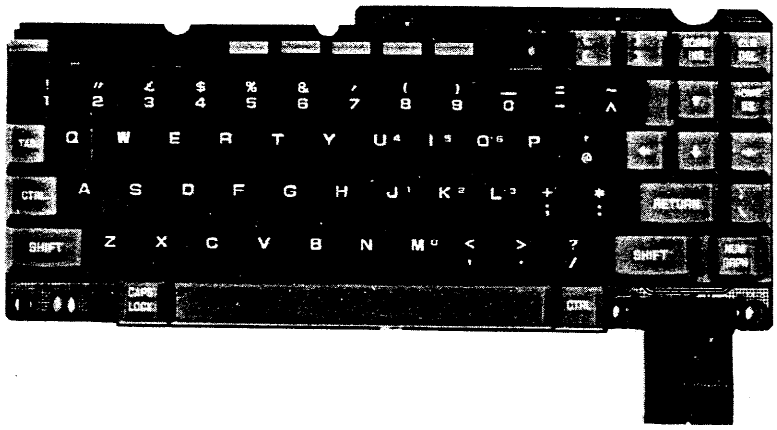


Fig. 1-5

1.3.4 LCD

The LCD is a twist pneumatic (TNM) effect type liquid-crystal display. The screen angle can be changed arbitrarily. VIEW ANGLE volume is provided to correct the change of liquid crystal display condition caused by temperature rise or fall.

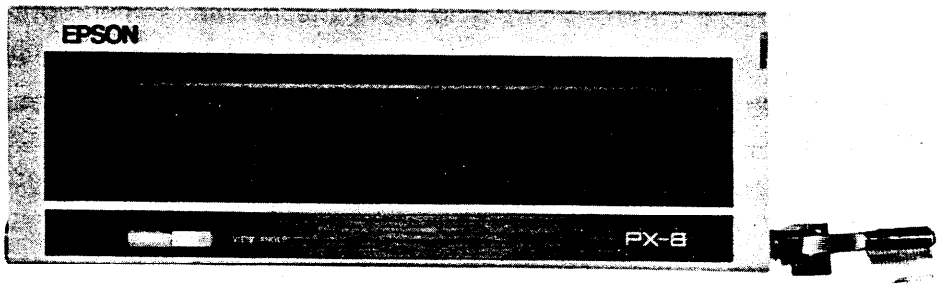


Fig. 1-6

1.3.5 Main battery

The main battery is Ni-Cd with a nominal voltage of 4.8V. When the battery is fully charged, the voltage is 5.0V or more, enough to provide power for circuit operation. The battery can be easily removed and replaced by removing the battery cover on the bottom of the unit.

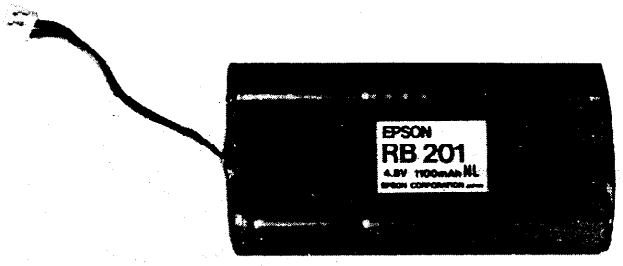
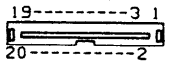


Fig. 1-7

Table 1-8 CN3 (Incorporated Microcassette) Pin Assignments

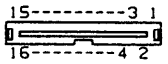


Pin No.	Signal Name	Definition
1	VLSW	Circuit voltage supply (through read gate)
2	VLR	Circuit voltage supply (read amp. power supply)
3, 4	GND	Ground
5	RDSP	Sound output of read data
6	WE	
7	RDMC	Read signal
8	WD	Write data
9	HMT	Head pinch motor control
10	CNTR	Counter
11	MT B	Capstan motor drive control
12	MT A	Capstan motor drive control
13	HSW	Head switch status
14	MT C	Capstan motor speed control
15, 16	VBSW	Battery voltage supply (for motor)
17	ERAH	Erase signal
18, 19, 20	GND	Ground

Table 1-9 CN4 (Keyboard Interface) Pin Assignments

Pin No.	Signal Name	Definition
1	KSC 0	Key scan signal
2	KSC 1	Key scan signal
3	KSC 2	Key scan signal
4	KSC 3	Key scan signal
5	KSC 4	Key scan signal
6	KSC 5	Key scan signal
7	KSC 6	Key scan signal
8	KSC 7	Key scan signal
9	KSC 8	Key scan signal
10	KRTN 0	Key return signal
11	KRTN 1	Key return signal
12	KRTN 2	Key return signal
13	KRTN 3	Key return signal
14	KRTN 4	Key return signal
15	KRTN 5	Key return signal
16	KRTN 6	Key return signal
17	KRTN 7	Key return signal
18	LED 0	CAPS LOCK MODE
19	LED 1	NUMERIC MODE
20	LED 2	INSERT MODE
21, 22	GND	Ground

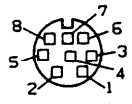
Table 1-10 CN5 (LCD Interface) Pin Connections



Pin No.	Signal Name	Definition
1	VLD	Circuit voltage: +5
2	YDO	Y data
3	YSCL	Y shift clock
4	YSPU	Speed up signal
5	YDIS	Y display signal
6	FS	Frame signal
7	LP	Latch pulse signal
8	XECL	X enable clock
9	XSCL	X shift clock
10	XD0	X data 0
11	XD1	X data 1
12	XD2	X data 2
13	XD3	X data 3
14	GND	Signal ground
15, 16	VL	Circuit voltage

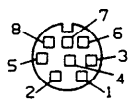
* View from the rear side of the board.

Table 1-11 CN6 (High Speed Serial Interface) Pin Connections



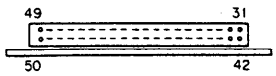
Pin No.	Signal Name	Definition
1	GND	Signal ground
2	$\overline{\text{PTX}}$	Transmit data (output)
3	$\overline{\text{PRX}}$	Receiving data (input)
6	PIN	Receiving mode (input)
7	POUT	Transmit mode (output)
E	FG	Chassis ground

Table 1-12 CN7 (RS-232C Interface) Pin Assignments



Pin No.	Signal Name	Definition
1	GND	Signal ground
2	TXD	Transmit data (output)
3	RXD	Receiving data (input)
4	RST	Request-to-send (output)
5	CTS	Clear-to-send (input)
6	DSR	Data set ready (output)
7	DTR	Data terminal ready (output)
8	CD	Carrier detect
E	FG	Chassis ground

Table 1-13 CN8 (Expansion) Interface



Pin No.	Signal Name	Direction	Definition
1	AB12	O	Address bus 12
3	AB14	O	Address bus 14
5	AB 1	O	Address bus 1
7	AB15	O	Address bus 15
9	AB 4	O	Address bus 4
11	AB 6	O	Address bus 1
13	AB10	O	Address bus 10
15	AB 8	O	Address bus 8
17	DB 0	I/O	Data bus 0
19	DB 2	I/O	Data bus 2
21	DB 4	I/O	Data bus 4
23	DB 6	I/O	Dat bus 6
25	$\overline{\text{BURQ}}$	O	Bus request
27	$\overline{\text{M1}}$	O	Machine cycle 1
29	VL	O	Circuit voltage: +5V
31	GND	—	Signal ground
33	$\overline{\text{RS}}$	O	Reset
35	$\overline{\text{RD}}$	O	Read
37	$\overline{\text{WR}}$	O	Write
39	VCH	O	Charging voltage
41	DCAS	O	Data CAS
43	$\overline{\text{INTEX}}$	I	External interruption
45	$\overline{\text{RXD}}$	I	Serial received data
47	VB1	O	Battery voltage
49	CG	—	Chassis ground

Pin No.	Signal Name	Direction	Definition
2	AB11	O	Address bus 11
4	AB13	O	Address bus 13
6	AB 2	O	Address bus 2
8	AB 0	O	Address bus 0
10	AB 3	O	Address bus 3
12	AB 5	O	Address bus 5
14	AB 7	O	Address bus 7
16	AB 9	O	Address bus 9
18	DB 1	I/O	Data bus 1
20	DB 3	I/O	Data bus 3
22	DB 5	I/O	Data bus 5
24	DB 7	I/O	Data bus 7
26	$\overline{\text{BUAK}}$	O	Bus acknowledge
28	$\overline{\text{WAIT}}$	I	Wait
30	$\overline{\text{HLTA}}$	O	Halt acknowledge
32	GND	—	Signal ground
34	SPI	I	Speaker
36	$\overline{\text{MRQ}}$	O	Memory request
38	$\overline{\text{CLK}}$	O	2.45 MHz
40	$\overline{\text{IORQ}}$	O	I/O request
42	DW	O	Data write
44	OFF	O	Initializilng signal of IC "6A"
46	$\overline{\text{TXD}}$	O	Serial send data
48	$\overline{\text{BK2}}$	I	Bank exchange
50	CG	—	Chassis ground

Table 1-14 CN9 (Bar Code Read Interface) Pin Assignments

Pin No.	Signal name	Definition
1	G	Signal ground
2	+5	Circuit voltage
3	BRDT	Bar code reader data

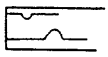
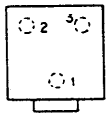


Table 1-15 CN10 (Analog Input Interface) Pin Assignments

Pin No.	Signal name	Definition
1	G	Signal ground
2	ANIN	Analog input
3	TRIG	Analog trigger input



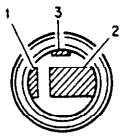
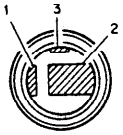


Table 1-16 CN11 (External Speaker Interface) Pin Assignments

Pin No.	Signal name	Definition
1	EXSPG	Speaker ground
2	EXSP	Speaker signal



1.5 Connection Cable (option)

Fig. 1-8 shows in a diagram the information cables for all the available peripheral devices.

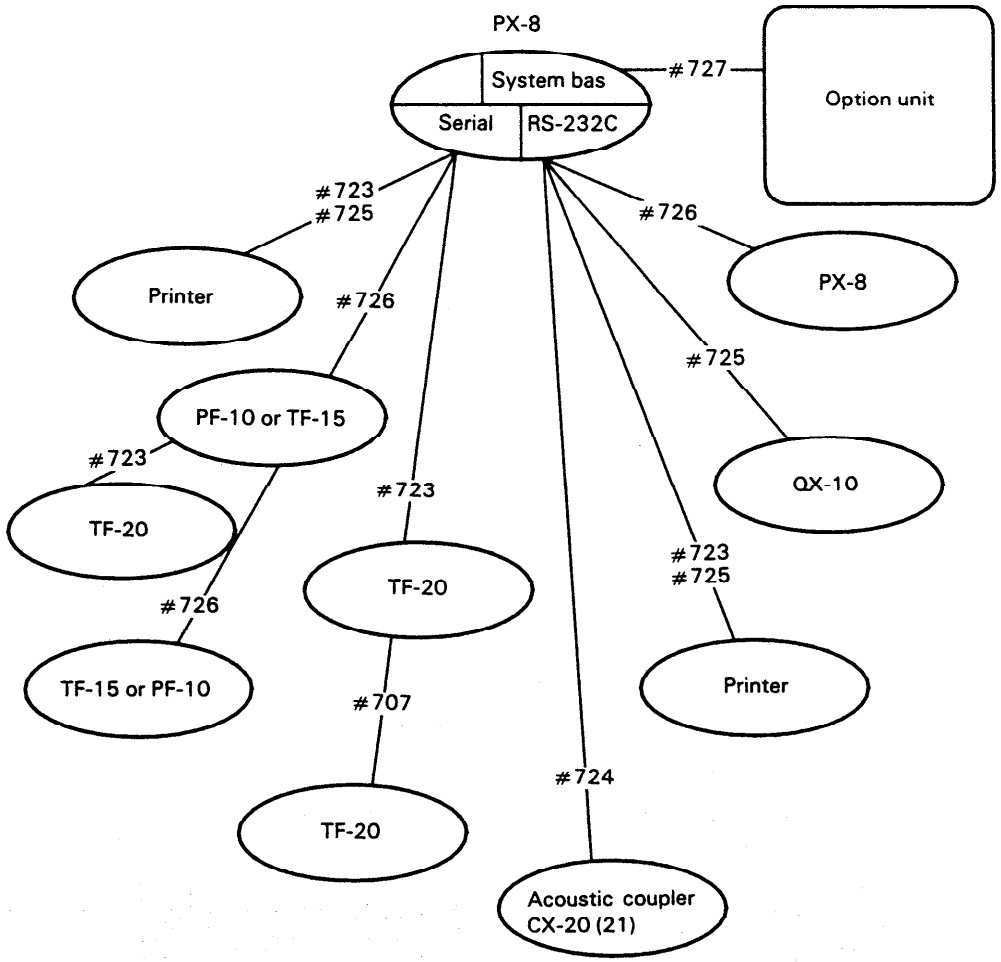


Fig. 1-8 Peripheral Device Information Cables

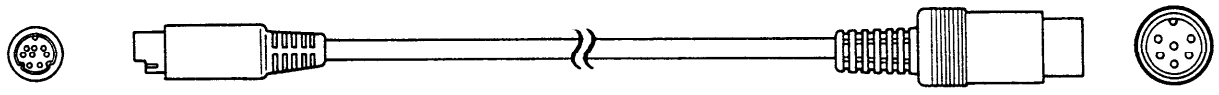
Table 1-17 Information Cables Specific to the PX-8 Computer

No.	Interface	Part No.
#723	High speed serial	Y204080000 (Y204080400···JAPAN)
#724	RS-232C	Y204080100 (Y204080500···JAPAN)
#725	RS-232C	Y204080200 (Y204080600···JAPAN)
#726	High speed serial/RS-232C	Y204080300 (Y204080700···JAPAN)
#727	Expansion interface	Y204301000

(1) #723 cable

Usage : Connection to dedicated floppy disk drive

Connector: Round-type miniature, DIN6



No.	Signal Name	Color
1	GND	Black
2	PTX	Brown
3	PRX	Red
4	——	——
5	——	——
6	PIN	Orange
7	POUT	Blue
8	——	——
E	CGND	(Shield)

No.	Signal Name	Color
1	PRX	Red
2	PIN	Orange
3	PTX	Brown
4	POUT	Blue
5	GND	Black
6	——	——
E	CGND	(Shield)

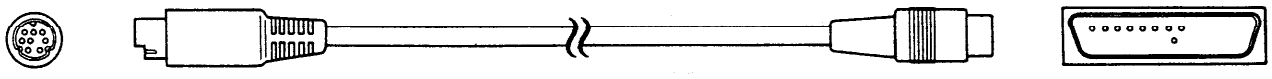
Fig. 1-9

#723, simple serial cable, consists of two lines: the send/receive data line and the I/O control line. Therefore, devices which can be connected via this cable are intelligent terminals only (that is, dedicated floppy disk drives) that can be controlled by PIN, POUT.

(2) #724 cable

Usage : Connection to acoustic coupler

Connector: Round-type miniature, DB25



No.	Signal Name	Color
1	GND	Black
2	TXD	Brown
3	RXD	Red
4	RTC	Orange
5	CTS	Blue
6	DSR	Purple
7	DTR	Gray
8	CD	White
E	CG	Shield

No.	Signal Name	Color
1	CG	Shield
2	TXD	Brown
3	RXD	Red
4	RTS	Orange
5	CTS	Blue
6	DSR	Purple
7	GND	Black
8	CD	White
20	DTR	Gray

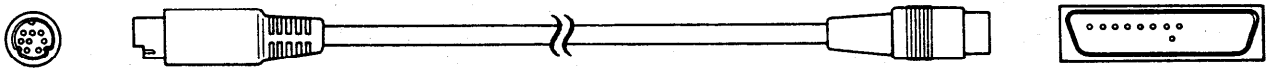
Fig. 1-10

This MODEM connector cable conveys RS-232C interface signals.

(3) #725 cable

Usage : Connection to printer with RS-232C interface

Connector: Round-type miniature, DB25



No.	Signal Name	Color
1	GND	Black
2	TXD	Brown
3	RXD	Red
4	RTS	Orange
5	CTS	Orange
6	DSR	Purple
7	DTR	Gray
8	CD	White
E	CG	Shield

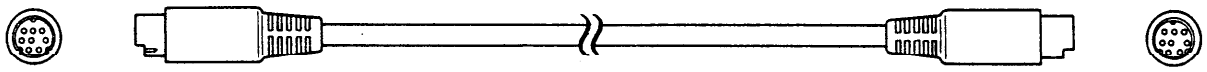
No.	Signal Name	Color
1	CG	Shield
2	RXD	Red
3	TXD	Brown
4	——	White
5	——	White
6	DSR	Gray
7	GND	Black
8	CD	Orange
20	DTR	Purple

Fig. 1-11

(4) #726 cable

Usage : Connection between two units or more

Connector: Round-type miniature Round-type miniature



No.	Signal Name	Color
1	GND	Black
2	TXD	Brown
3	RXD	Red
4	RTS	Orange
5	CTS	Orange
6	DSR	Purple
7	DTR	Gray
8	CD	White
E	CG	Shield

No.	Signal Name	Color
1	GND	Black
2	TXD	Red
3	RXD	Brown
4	RTS	White
5	CTS	White
6	DSR	Gray
7	DTR	Purple
8	CD	Orange
E	CG	Shield

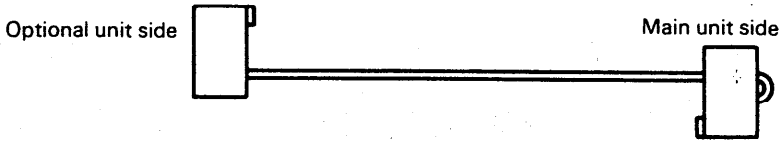
Fig. 1-12

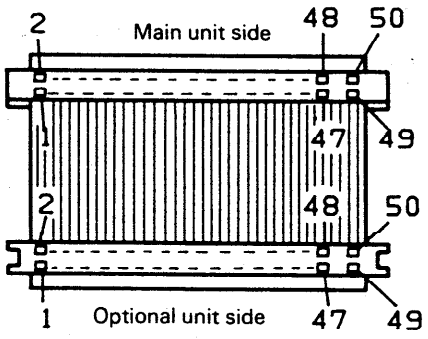
An shown in Fig. 1-11, control lines of DSR and DTR, and connected lines of CTS and RTS (connected to CD) are crossing respectively. Therefore, when transmitting data or receiving, both units must open RS-232C interfaces.

(5) #727 cable

Usage : Connection to optional unit

Connector: ERC-AA50 – 30 (S)





See Page 1-13 CN8 for signals.

CHAPTER 2
PRINCIPLES OF OPERATIONS

2.1 General

This chapter describes various functions of the main control board (called MAPLE board) which is the center of this computer. The microcassette drive and option units are described in Chapter 3. The MAPLE board uses a diversity of fully customized ICs (referred to as gate arrays throughout this manual), masked ROMs, and other chip elements (resistor, capacitor, transistor, and diode chips) which simplify component mounting. As many CMOS elements as possible have been used in order to lower power consumption. In addition, the computer provides the following features in order to control functions specific to battery powering:

(1) Battery backup:
Protects data in RAM.

(2) Battery distribution (main and auxiliary battery power supplies):
Ensures a more reliable battery backup.

(3) Charge control:
Prevents excess Ni-Cd battery charging.

(4) Power distribution:
Outputs the supply voltages only while the computer is in operation in order to minimize battery consumption.

(5) Low voltage detection:
Automatically changes the main battery to the auxiliary battery supply.

In addition, the computer is provided with a software automatic power-off feature which prevents the battery from being discharged out if the computer is inadvertently left on.

2.1.1 Major Components

The MAPLE board has elements mounted on both the sides. A speaker and elements such as resistor packages, etc. are mounted on one side, while elements such as connectors, switches, and LSI chips, etc. are mounted on the opposite side as shown in Fig. 2-1. Table 2-1 lists major board elements together with a summary of their function.

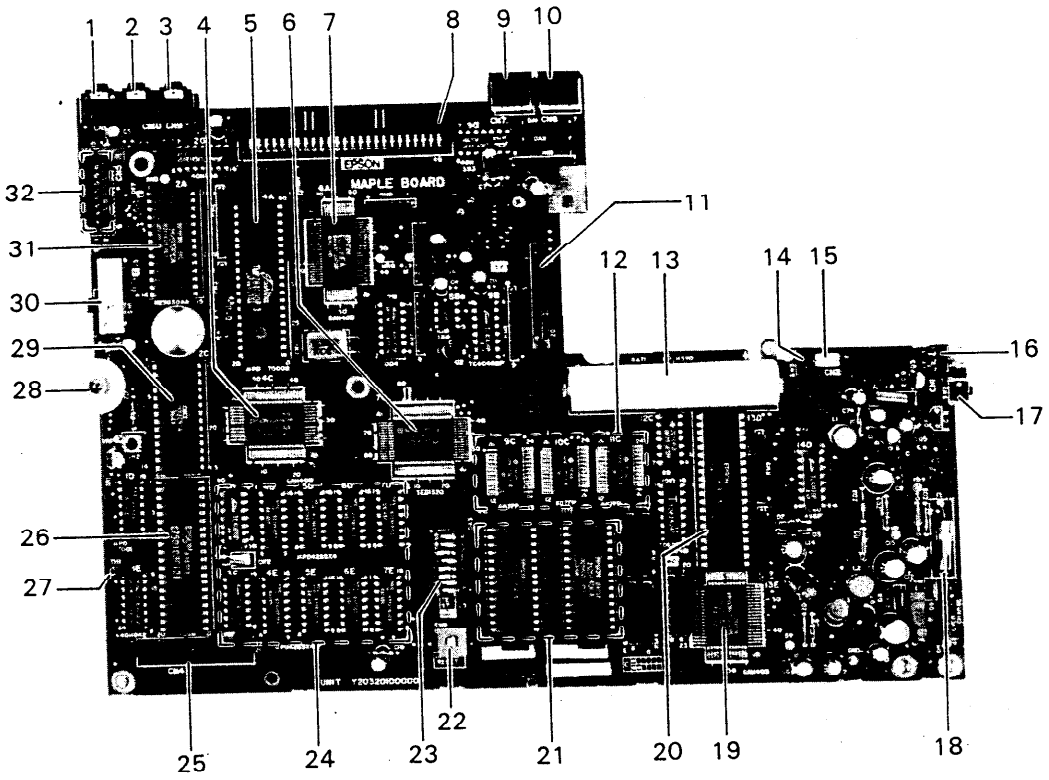


Fig. 2-1 MAPLE Board Element Layout

Table 2-1 MAPLE Board Major Components

No.	Name	Function
1	CN11	External speaker connector
3	CN9	Barcode reader connector
5	Main CPU	Z80 CPU package
7	Gate array	GAH40D package
9	CN7	RS-232C interface connector
11	CN3	Microcassette interface connector
13	Auxiliary battery	90 mAH backup battery
15	CN2	Main battery connector
17	SW2	Reset switch
19	Gate array	GAH40S package
21	ROM capsule	(32 kB x 2)
23	SW4	8-position DIP switch
25	CN4	Keyboard interface connector
27	TH1	Thermistor (for temperature sensing)
29	Serial controller	82C51 package
31	ROM	32kB ROM

No.	Name	Function
2	CN10	Analog signal input connector
4	Gate array	GAH40M package
6	LCD controller	SED 1320 package
8	CN8	Expansion interface connector
10	CN6	Serial interface connector
12	V-RAM	6kB LCD RAM
14	SW3	Auxiliary battery control switch
16	CN1	AC adaptor input (charge input) connector
18	F1	Fuse 3A
20	Sub-CPU	6303 CPU package
22	SW5	Initial reset switch
24	D-RAM	64kB x 8
26	4-bit CPU	7508 CPU package
28	VR1	Speaker volume visual angle adjustment variable resistor
30	SW1	Power switch
32	CN5	LCD interface

2.1.2 System Configuration

PX-8's main components include a main battery; the MAPLE (main) board, which along with control circuitry also contains an auxiliary battery; the LCD unit; the keyboard; and the microcassette drive assembly. The following block diagram demonstrates component configuration.

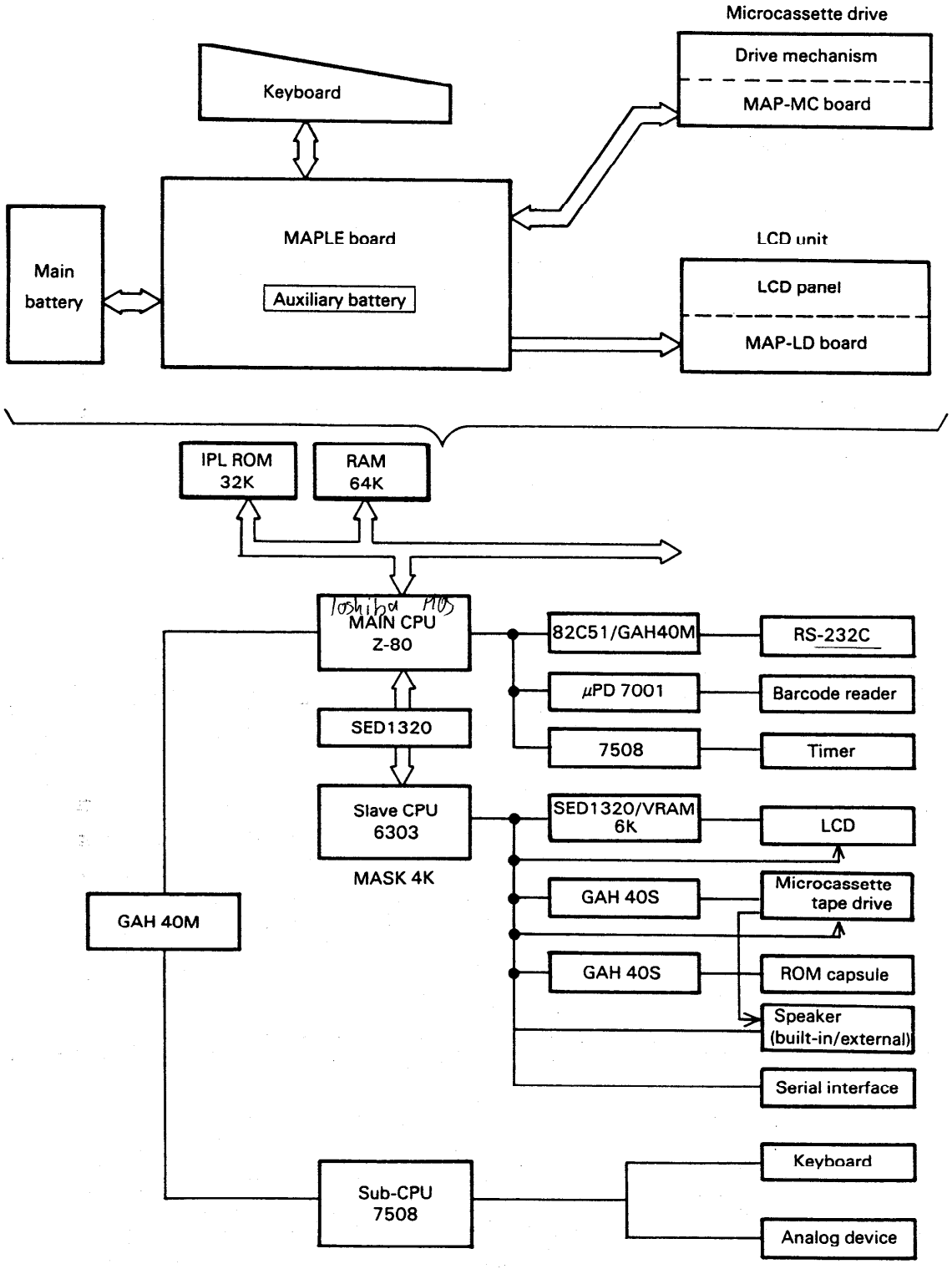


Fig. 2-2 Computer Configuration

2.2 Power Supply

This computer operates with a rechargeable Ni-Cd battery and is provided with features for minimizing power consumption and controlling battery charge. The power supply is summarized in the following:

- Batteries: Two batteries; main and auxiliary, are used.
  Main battery ..... Supplies a DC voltage of 4.8V and has a capacity of 1100 mAH. It can power all the computer circuits; backing up the commercial as AC power when not used or unavailable. It also supplies power to the attached option units.

  Auxiliary battery ..... Also supplies the DC 4.8V power. It has a capacity of 90 mAH and backs up the main battery when in a low voltage (discharged) condition.

- Charging circuit: Supplies charging current to the main and auxiliary battery when an AC adaptor is connected. This circuit, which operates in either of two modes; normal and tricle (low current) charges, under the control of a sub-CPU 7508, controls the charging current.

- Voltage detection circuit: Monitors the voltage of the main battery using an internal AD converter. The result is processed by the sub-CPU 7508 to cause the circuit to provide two functions. One is low voltage detection which allows the computer, if it is operating, to display a warning message "CHARGE BATTERY" on the LCD screen, when the battery power (i.e., voltage) falls below a certain level. In addition, this function causes the computer to stop at an appropriate point in the operation in progress. The other function determines the normal charge restart timing; causing a switch from tricle to normal charge when AC adapter is connected.

- Backup circuit: Supplies the power required to maintain data in the RAMs when the power switch is off or the computer is not connected to the AC power line. It also serves to normally operate the circuits which monitor the battery voltage and detect whether power is on.

- ±8V regulator: This voltage regulator supplies DC voltages of ±8V required for RS-232C operations. The voltages are generated from the battery voltage (VB) only when the RS-232C or serial interface is used.

- −15V regulator: Supplies a −15V DC voltage used for LCD display control. This voltage is generated from the battery voltage (VB) as long as power is on.

- 5V regulator: Supplies a +5V DC voltage used for the PROM capsule. This voltage is generated from the battery voltage (VB) only when the PROM is accessed. The regulator is provided in order to prevent a transient due to PROM access from directly affecting the VB line.

Other power circuits such as a switching circuit, which supplies the logic circuit power, are located on the MAPLE board, in addition to the above. Fig. 2-3 is a block diagram which summarizes the power supply circuits on the MAPLE board.

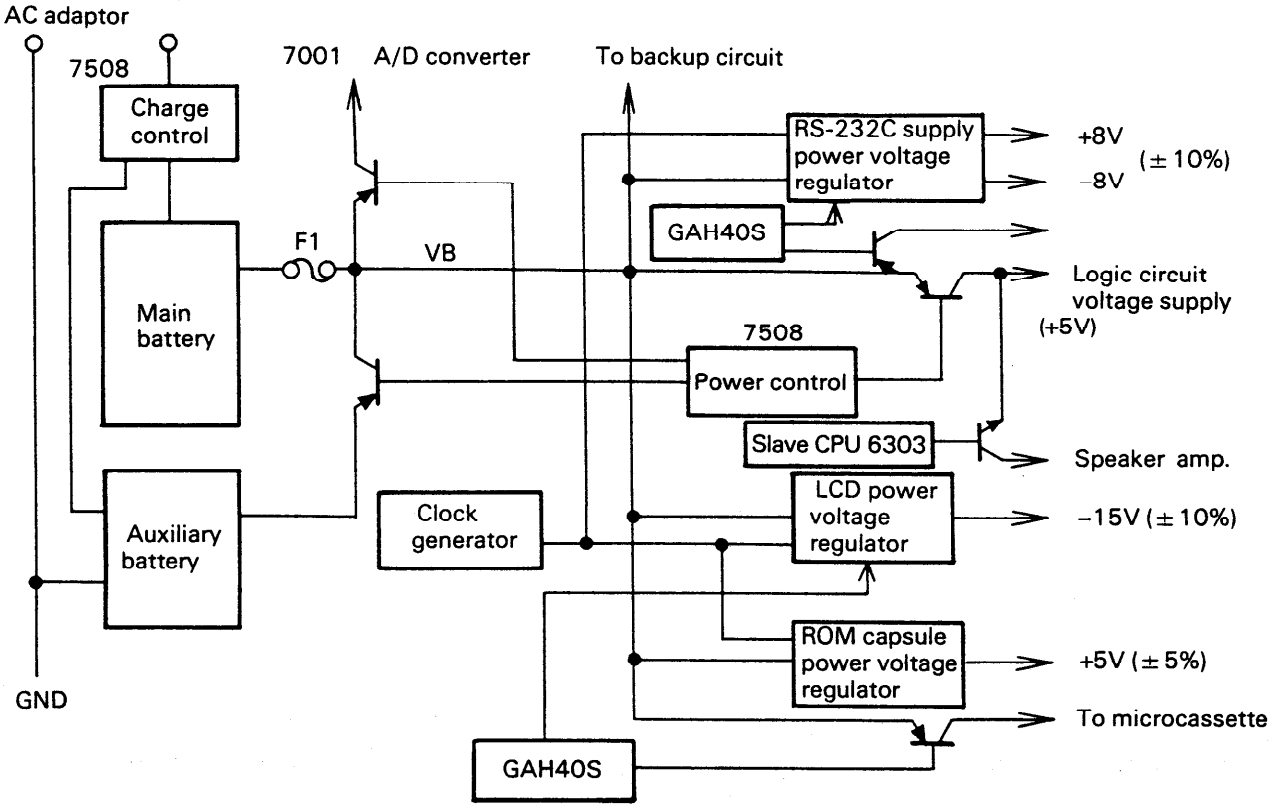


Fig. 2-3 Power Circuit Block Diagram

2.2.1 Power On/Off Control

The power circuits are controlled by the 4-bit CPU 7508 which operates under a control program stored in a mask ROM built in it. If the CPU runs away due to some reason (battery power exhaustion for example), therefore, the power supplies are completely out of control. If this occurs, the AC adaptor should be connected to charge the batteries and then SW5 should be pressed to reset the CPU 7508.

2.2.1.1 Power On

The computer is turned on by either of the following:

(1) Setting the POWER switch ON

Setting the POWER switch ON causes pin 23 of CPU 7508 (INT0) to go high (see Fig. 2-4) which interrupts the control program for turning power on.

(2) Programmed power on

Power is automatically turned on regardless of the POWER switch setting when the time specified softwarewise with a "WAKE" command coincides with that of the clock built in CPU 7508.

2.2.1.2 Power Off

Power is turned off by one of the following:

(1) POWER switch OFF

Turning the POWER switch OFF causes pin 23 of the 7508 CPU (INT0) to go low (see Fig. 2-4), interrupting the control program for turning power off.

(2) Low voltage detection

When a low VB line voltage is detected. The 7508 CPU interrupts the main CPU and current processing to be terminated at an appropriate point . At the same time, "CHARGE BATTERY" message display on the LCD screen for 30 seconds. The 7508 CPU then automatically turns power off if the POWER switch is at the ON position.

(3) Automatic (programmed) power off

The computer can be turned off by a software automatic power-off feature which uses the 7508 CPU's built in clock. This feature automatically turns power off when no I/O unit is used for a certain period of time even though the computer is in the key entry mode. Power off timing as follows:

- Default: 10 minutes
- Specified: 1 to 255 minutes (specified by using the CONFIG command)

The following is a circuit diagram including the power on/off circuit:

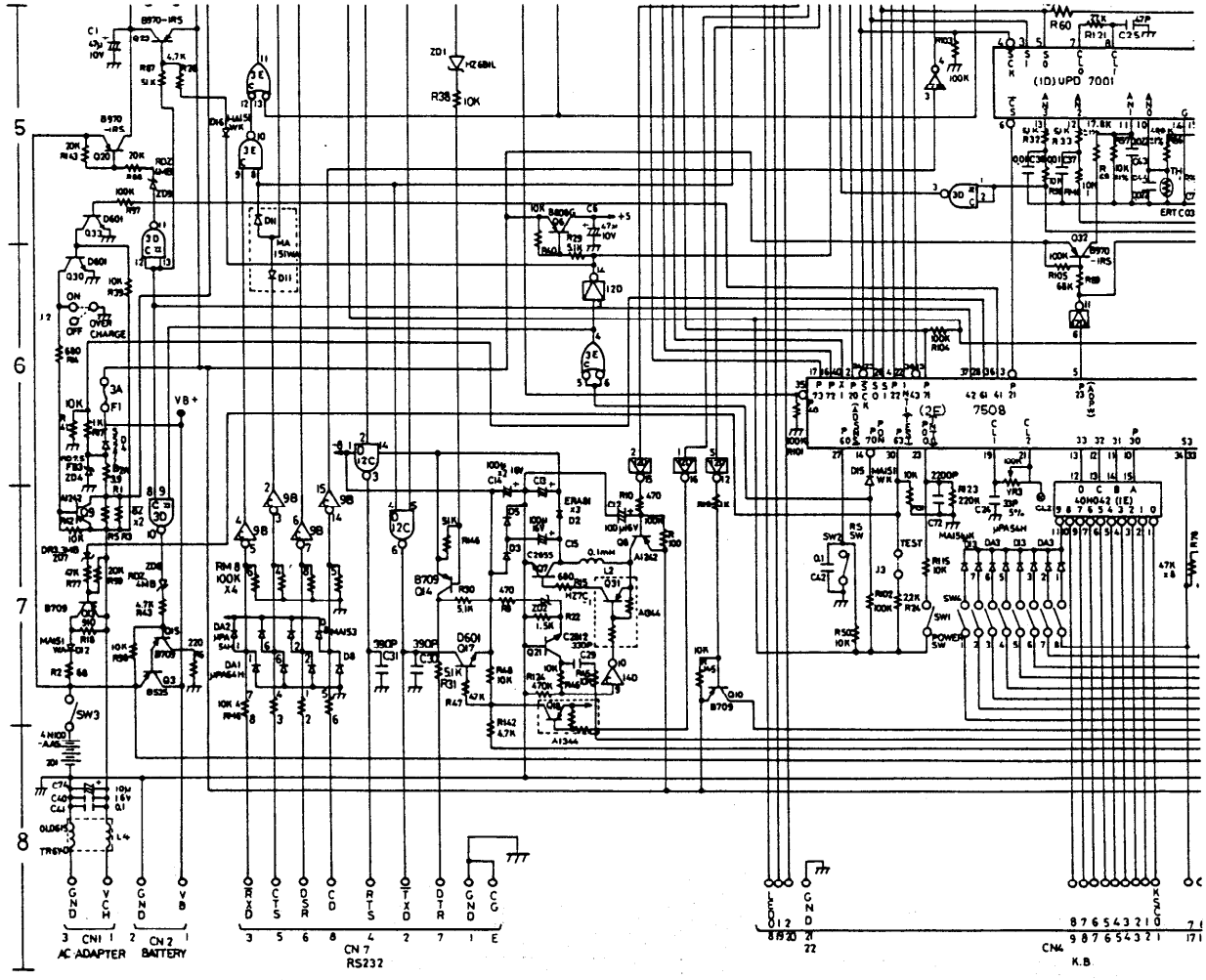


Fig. 2-4 Power On/Off Control Circuit

* The power-off operation involves the following component functions:

- Microcasette tape drive head unloading
- Microcassette tape drive power off
- P-ROM cartridge power off
- RS-232C power off
- Barcode reader power off
- Speaker power off

It also controls the emergency power supply which allows the computer operation sequence in process to be completed and status information to be stored whenever the regular power supply is depleted.

2.2.1.3 Power On/Off Timing

Power on/off has to be controlled by interrupting the sub-CPU 7508. Thus, either timing (the $\overline{\text{POWER ON}}$ or $\overline{\text{RESET}}$ signal) will be a little delayed as shown in Fig. 2-5

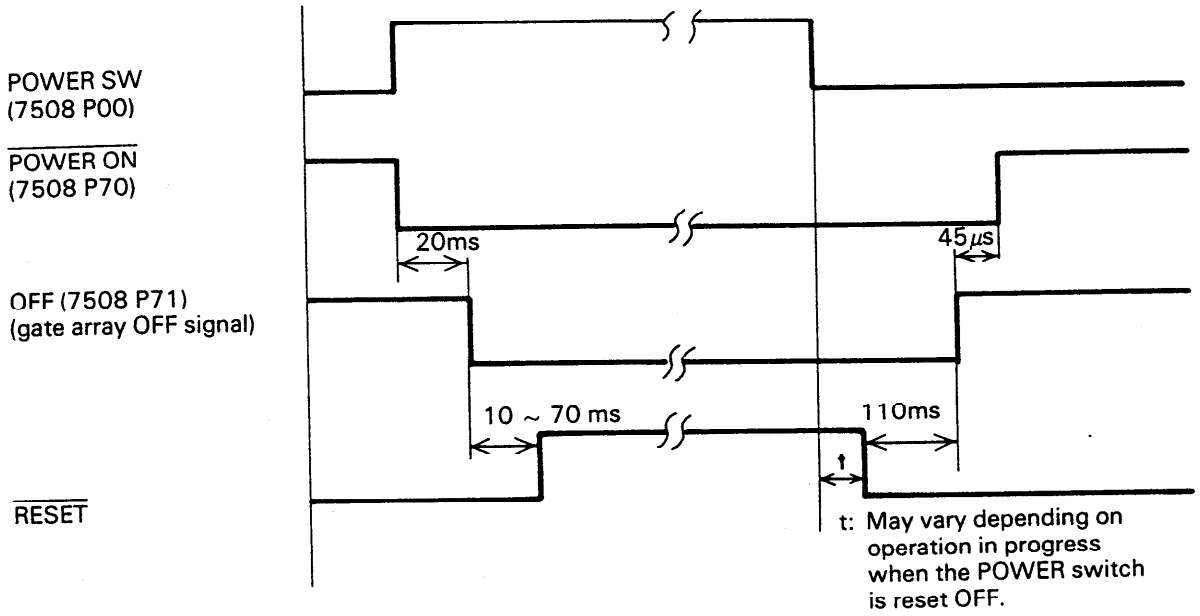


Fig. 2-5 Power On/Off Control Circuit

The time delay sequence illustrated in Fig. 2-5 above is only a sample time sequence. The power on/off operation permits any operation sequence in process, including the mechanical operation of an I/O unit (e.g., the microcassette) currently in progress, to be completed and the printer to be reinitialized before the power is off. The length of the illustrated time delay will vary according to which mechanical and/or logic sequence must be completed. The off signal is used to prevent a latch within the gate array.

2.2.1.4 Power On/Off Circuit Operations

Fig. 2-6 shows the circuit. When the POWER switch is set ON or RESET off, or an automatic power on or off is input via software, the sub-CPU control program processes the power on or off as an interrupt using port 70 as follows:

- Power on: P70 of the sub-CPU 7508 going low causes the anode of D15 to go low, turning pin 4 of IC '3E' high. This in turn causes the output at pin 14 of the next inverter, 12D, to go low. This signal is fed to transistors Q6 and Q23 through resistors R29 and D16 respectively, turning them on. This causes the VB (+) voltage to be output at the collector of Q6, supplying the operation voltage (logic circuit voltage: VL) to the elements on the board. The transistor Q23 also supplies the VB(+) voltage to the battery-backed-up elements on the board. Thus, the board is ready to operate. Port 42 of the 7508 sub-CPU controls the backup for the auxiliary battery and can enable or disable conduction through transistor Q20. When port 42 output is high, the low level at pin 11 of IC 3D breaks down zener diode ZD9, holding Q20 in conduction. In this way the LCD drive voltage is insured, the message, "CHARGE BATTERY", will be displayed whenever the main battery output voltage falls to or below the low voltage limit.

- Power off: P70 of the sub-CPU going high, causes the output of pin 14 of inverter, 12D, to go high, turning Q6 off and thereby stopping the logic circuit voltage supply. Q23 is controlled by the sub-CPU, via P42, returning it to the normal backup operation.
- When the power-off request is an interrupt, generated when the POWER switch is turned OFF or low voltage is detected. When the power is turned Off and the power off request is comitted, the current operation has to be examined and a sequence excuted which assures that the operation in progress, including any I/O operation sequence, will be resumed without error when power is restored. The sequence allows all necessary processes such as the reinitialization of the I/O device (e.g., microcassette) in operation, a warning message display, etc. to be accomplished before the logic circuit voltage supply is actually removed.
- OFF signal: The OFF signal shown in Fig. 2-5 is controlled via P71 of sub-CPU 7508. This signal is emitted to gate arrays 6A and 4C, and the expansion interface CN8. It is intended to initialize the internal circuit of the gate arrays in order to prevent their outputs from being latched; it is a so called reset signal to the gate arrays and does not control power supply to the gate arrays.

  The relationship between P70 and P42 of sub-CPU 7508 will be discussed in section 2.3, "Low Voltage Detection".

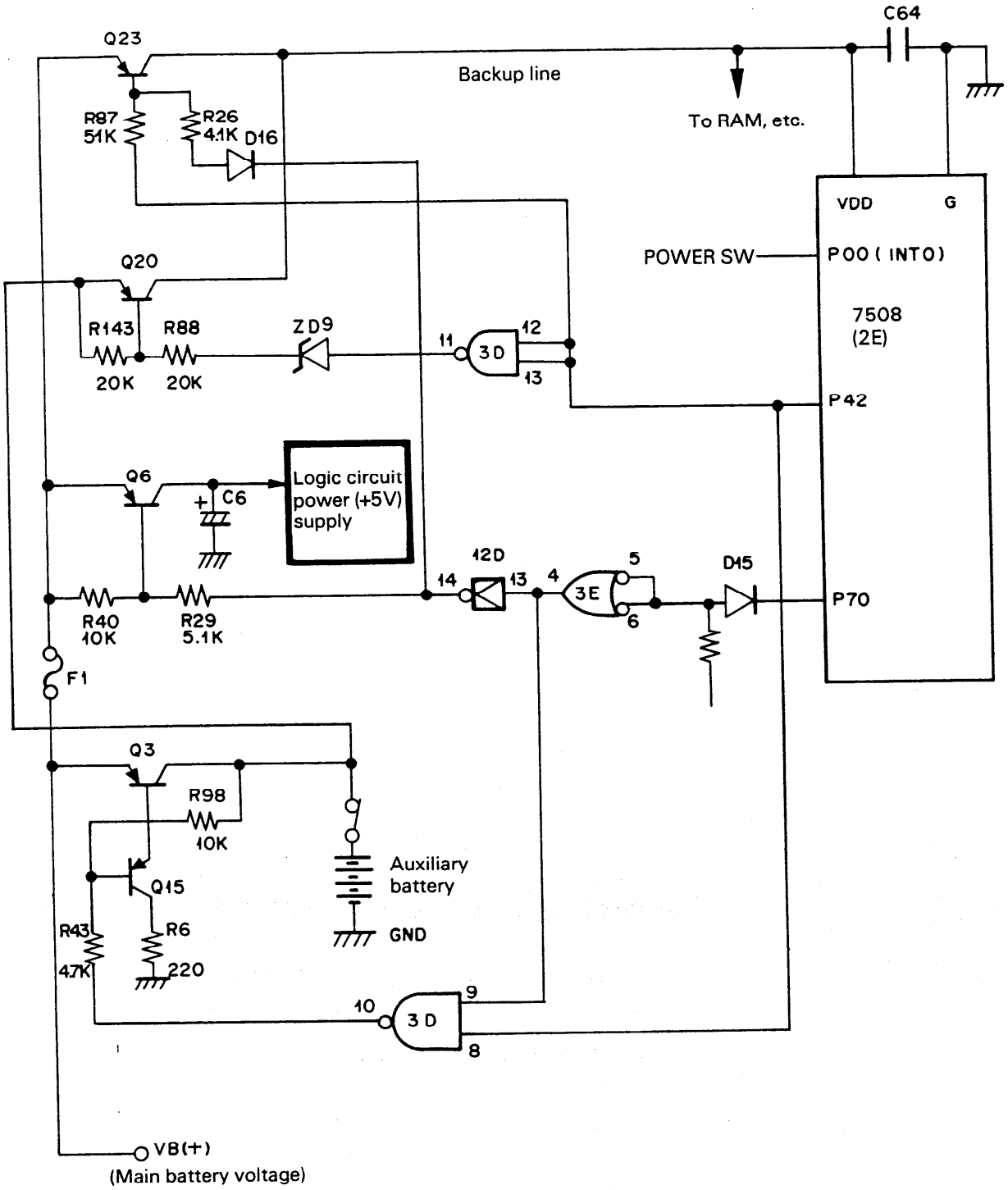


Fig. 2-6

Note:

P70: $\overline{\text{POWER ON}}$ signal
High turns power off, and
Low turns power on.

P42: Main → auxiliary battery switching signal
High selects auxiliary battery, and
Low select main battery.

2.2.2 Charging Circuit

Two 4.8V, rechargeable, Ni-Cd batteries are connected to the MAPLE board. The main battery, which is housed the bottom case and can be replaced by loosening a single screw, has the larger capacity of 1100 mAH. Its charging circuit includes an overcharge protection circuit which protects the battery from overcharge by automatically discontinuing charge. The auxiliary battery, which is mounted on the MAPLE board, has a capacity of 90 mAH. A switch is inserted in both the charging circuit and backup line which can disable the backup by the auxiliary battery.

2.2.2.1 Main Battery Charging Circuit

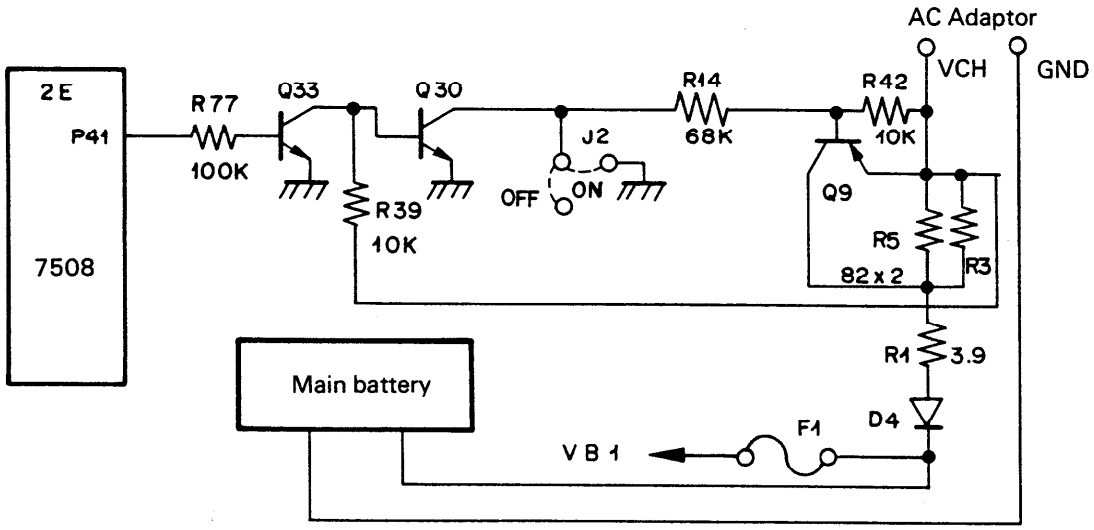


Fig. 2-7 Main Battery Charging Circuit

The charging circuit includes jumper A2 which allows two modes of charging:

When J2 is jumpered ..... No Overcharge Protection Control

Jumpering J2 causes the base of transistor Q9 to be always tied to ground, holding it in conduction. This effectively bypasses resistors R3 and R5, inserted in the charging circuit in series, and causes the charging current to be supplied to the battery through transistor Q9, current limiting resistor R1, and reverse-current preventing diode D4. This setting ecuses the battery to be continually charged as long as the AC adaptor is connected. Because of the low current limiting resistance in the mode of operation, the battery is highly liable to overcharge.

When J2 is open ..... Shipment Setting

- When J2 is open, the charge current bypassing transistor Q9 is controlled by the port 41 output of the 4-bit sub-CPU 7508. This CPU has a clock feature built in and maintains port 41 at the low level only for the first eight hours after it detects that the AC adaptor is connected, providing the same charging mode as when the jumper J2 is closed. With port 41 held low, transistor Q33 is cut off, leaving its collector at the high level (The collector is pulled up to the ac adaptor output through the resistor R39.) This maintains transistor Q30 in conduction; the collector is held at the low level, providing the same effect as if jumper J2 were closed.

- When eight hours have elapsed after the ac adaptor is connected to the AC line, port 41 of the 4-bit sub-CPU goes high, cutting off transistor Q9. This puts the circuit in the trickle charging state by inserting the resistors R3 and R5 (combined resistance, 41 ohms) in the charging path in series. The circuit constants are selected in this state so that the battery is substantially not harmed by overcharge, even if the battery is continually charged.

*Reference

Following is the sub-CPU port operation for power control:

Table 2-2 Sub-CPU Port Operation

Port	Direction	Meaning	Signal level	Function
P00	IN	Power switch interruption	Low	Power switch "OFF" interruption (H → L: ⌐↓_)
			High	Power switch "ON" interruption (L → H: _↑¬)
P23	Out	Main battery voltage detection	Low	Inactive
			High	Active ● Supply main battery voltage to A/D converter ● Supply operational voltage to A/D converter
P40	out	Reset	Low	Reset main CPU, slave CPU, etc.
			High	Inactive
P41	Out	Recharging mode control	Low	Normal recharging mode
			High	Trikle recharging mode
P42	Out	Battery back-up control	Low	Back-up with main battery
			High	Back-up with auxiliary battery
P60	In	Reset switch	Low	Active source input of "P40" and "OFF"
			High	Inactive
P61	In	AC adapter (re-charging operation) detect	Low	No AC adapter (non recharging condition)
			High	Recharging condition (AC adapter is plugged)
P63	Out	Recharging mode for auxiliary battery	Low	Normal recharging mode
			High	Trikle recharging mode
P70	Out	Powr ON	Low	Power ON
			High	Power OFF
P71	Out	"OFF" signal for gate array (6A, 4C)	Low	Active (Initialize the '4C' '6A')
			High	Inactive

2.2.2.2 Main Battery Charging

In the following text, the functions of jumper J2 are summarized. Then, the actual main battery charging operations are described based in Fig. 2-8.

(1) J2 jumper

The J2 jumper provides the following functions:

When closed: Disables the charging control; the battery is always charged as long as the AC adaptor is connected.

When open: Enables the charging control; the battery is charged as follows when the AC adaptor is connected, depending on whether power is on or off:

When power is on: The normal charge continues for the first 11 hours, and then the trickle charge is used.

When power is off: The normal charge continues for the first eight hours, and then the trickle charge is used.

* With jumper 2 open and power off, the circuit remains in the trickle charge mode, after the normal charge, for the first eight hours. However, the circuit automatically returns to the normal charge mode whenever the battery voltage falls below 5V.

(2) Charging Operations

● Fig. 2-8 is a timing diagram which illustrates the main battery charging operation when the charge control is in effect.

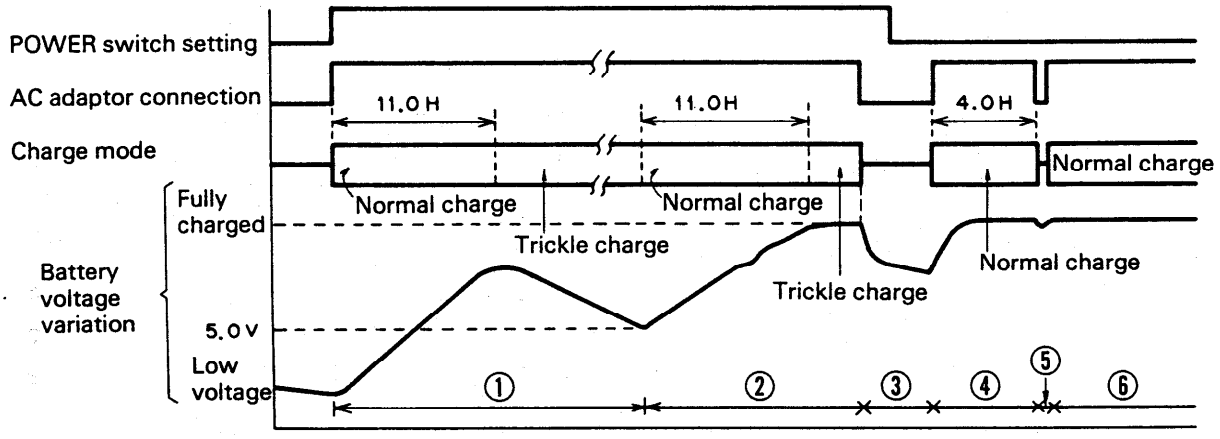


Fig. 2-8 Main Battery Charging Operation

Note: Battery voltages and charging currents:

Voltages:

When fully charged:	Approx. 5.4V
Low voltage:	Approx. 4.5 to 4.8V

Charging currents:

Main battery	
Normal charge:	150 to 200 mA
Trickle charge:	40 mA
Auxiliary battery	
Normal charge:	10 mA
Trickle charge:	1 mA

Fig. 2-8 illustrates the main battery charging operation from a low voltage. The individual steps of the operation ① through ⑦ are explained in detail in the following:

① Situation – Low voltage is detected while the computer is used with the AC adaptor connected.

The charging control is enable, and the battery is charged during normal computer use for aperiod of 11 hours. During that time, the battery may not be fully, charged depending on the particular use of the computer. After 11 hours, the charge mode changes to trickle charge in which the battery is charged at a current of approximately 40 mA. The figure shows a charging current of more than 40 mA, indicating that the battery is being discharged.

② Situation – The battery voltage falls to 5.0V while the computer is used.

Since the AC adaptor remains connected, the charge mode is switched back from trickle to normal charge. Sub-CPU 7508 always monitors the battery voltage using an A/D converter and, whenever it detects that the voltage has fallen to 5.0V or below, it automatically switches the mode through port 41. The circuit restores the same charging operation as ① above. The almost linear changes during the normal and trickle charges indicate that the charge and discharge currents remain almost constant during these durations.

③ Situation – After the AC adapter is disconnected, the computer is used for a while, and then power is turned off.

While the computer is used, the battery power decreases depending on how it is used. After power off, the battery power decreases for backing up the internal circuits.

④ Situation – The AC adaptor is connected while the power remains off.

The eight-hour normal charge starts when the AC adaptor is connected. However, it is interrupted four hours after when the adaptor is disconnected. The battery is charged at the normal charge current during this interval regardless of the battery power.

⑤ Situation – The normal charge is interrupted by replacing the adaptor connection to another AC line outlet.

⑥ Situation – The adaptor is reconnected and the normal charge is resumed.

The eight-hour normal charge starts again when the AC adaptor is reconnected.

Note 1: The main battery charging is controlled by detecting connection of the AC adaptor, regardless of the current residual battery power or the past charging operations. The 8- or 11-hour normal charge starts depending on whether power has been turned on or off when the adaptor is connected.

Note 2: The battery may not be fully charged even though the adaptor is left connected for a long period of time. It is highly likely that the battery will remain below the full charge, especially when high power consuming operations are being performed while the battery charge is in process.

When charging control is disabled

When the charging control feature is disabled, the battery is charged at the normal charge current as long as the AC adaptor is connected. Leaving the adaptor connected for a long time (overcharging the battery) may affect the life of the battery.

2.2.2.3 Auxiliary Battery Charging Circuit

As shown in Fig. 2-9, this circuit allows the user to select, via switch SW3, whether or not to enable charging and discharging (i.e., backup by the auxiliary battery). (SW3 is normally jumpered.)

When SW3 is jumpered, the battery is charged by one of the following three modes:

- When the AC adaptor is connected:
  - (1) The auxiliary battery is charged from VCH through R18.
  - (2) The auxiliary battery is charged from VCH through Q13.
- When the computer is turned on:
  - (3) The auxiliary battery is charged from the LCD power supply.
- Mode (1) is a trickle (low current) charge, which is enabled when the main battery voltage is 5.0V or below.
- Mode (2) is a normal charge which is enabled after low battery voltage (VB) condition is detected. When low voltage is detected, P63 of the sub-CPU 7508 is held low for 8.0 hours, forcing the normal (high current) charge.

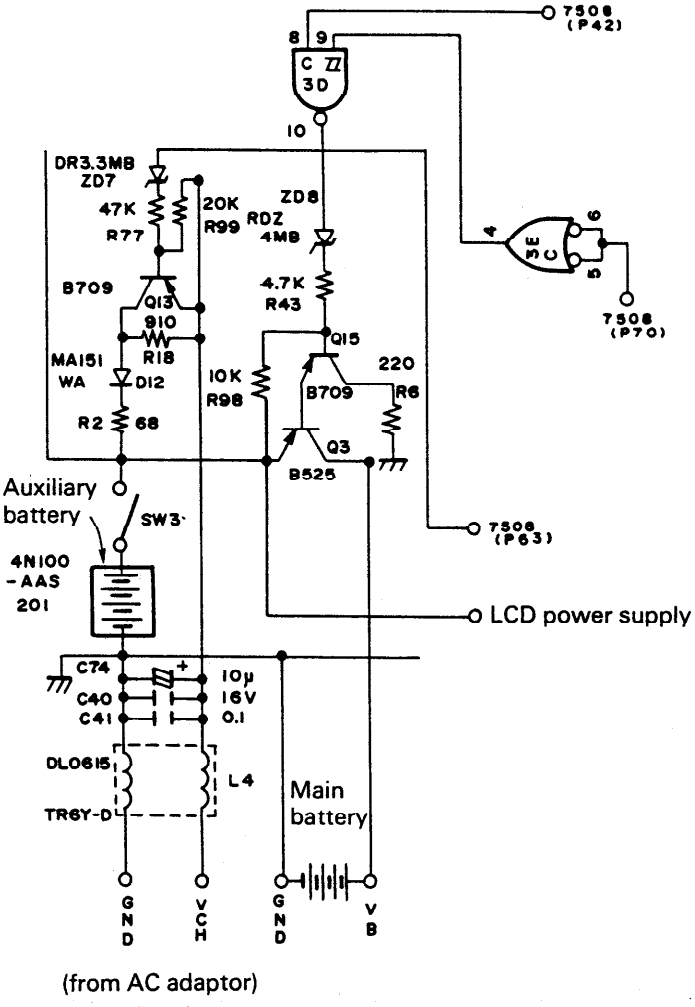


Fig. 2-9 Auxiliary Battery Charging Circuit

The low level at P63 causes a potential difference of approximately 6V (VCH voltage), which is AC adapter voltage, to appear across zener diode ZD7, breaking it down (ZD7 is a 3.3V zener diode). This lowers the base voltage of transistor Q13 below the collector voltage, putting the transistor in conduction, and providing the normal charging path from the VCH line through Q13, D12, and R2.

- Mode (3) constantly maintains the auxiliary battery in a fully charged state for emergency (the backup operation from the auxiliary voltage when low voltage is detected). Thus, the battery is continuously charged as long as the LCD power supply is available (whenever power is on) regardless of whether the ac adaptor is connected or not. See 2.2.5.2, LCD Voltage Regulator for details.

2.2.2.4 Charging Timing Detection

The sub-CPU program is designed to control auxiliary battery charging from the AC adaptor using the built-in clock. Connection of the AC adaptor. Port 61 of the sub-CPU goes high whenever the AC adaptor is connected and the main battery is being charged. Since port 61 is connected to the anode of the diode D4 in the charging circuit through the resistor R17, the presence of the VCH voltage can be detected.

2.2.2.5 Protection Against Charging Voltage Supply Failure

An overvoltage detection circuit and a reverse-current blocking circuit are provided in order to protect the batteries and their charging circuits when any abnormal voltage occurs on the output of the ac adaptor; i.e., the charging voltage. The operations of the circuits are described in the following:

(1) Protection against low voltage

The diode inserted in the charging circuit in series prevents reverse current if the charging voltage falls below the battery voltage.

(2) Protection against overvoltage

If the voltage at the cathode of the zener diode (VCH) rises to +7.5V or above, the zener diode breaks down, and protect the overvoltage condition for VB+ line.

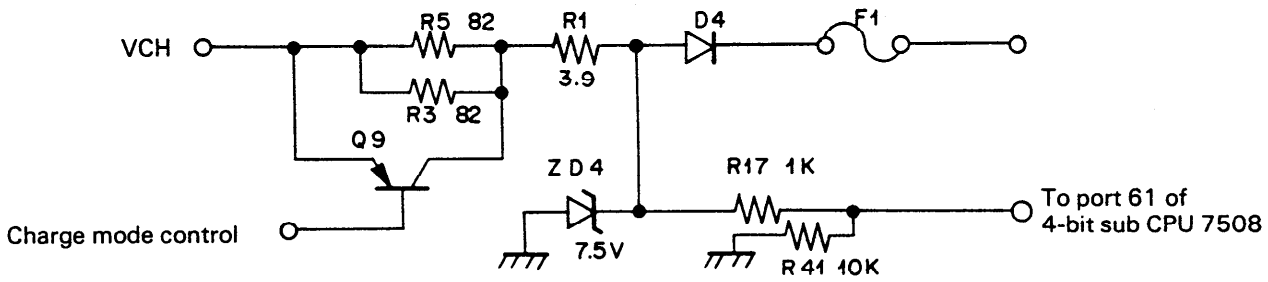


Fig. 2-10 Battery Protection Circuit

2.2.3 Low Voltage Detection

The 4-bit sub-CPU always monitors the battery voltage through an AD converter (μPD7001). When the battery voltage falls to +4.7V or below, the main battery is switched to the auxiliary battery.

2.2.3.1 Battery Voltage Detection Circuit

This circuit monitors the main battery voltage output through fuse F1 as follows:

- The built-in program of the 4-bit sub-CPU 7508 holds port 23 (pin 5) high. This causes IC 12D to hold its pin 11 low, putting transistors Q24 and Q32 in conduction. Q24 feeds the battery voltage (VB) to pin 16 of IC 1D (power terminal pin) to enable the AD converter μPD7001. Q32 feeds VB to the voltage divider (resistors R69 and R57). The divided voltage across R57 is fed to the AN 1 channel input of the AD converter which converts the input voltage to a 6-bit digital value representing a voltage value from 0V to 2.0V in a minimum increment of approximately 32 mV. When the digital value falls to D9H (approx. 1.7V) or below, the sub-CPU detects a low voltage condition.

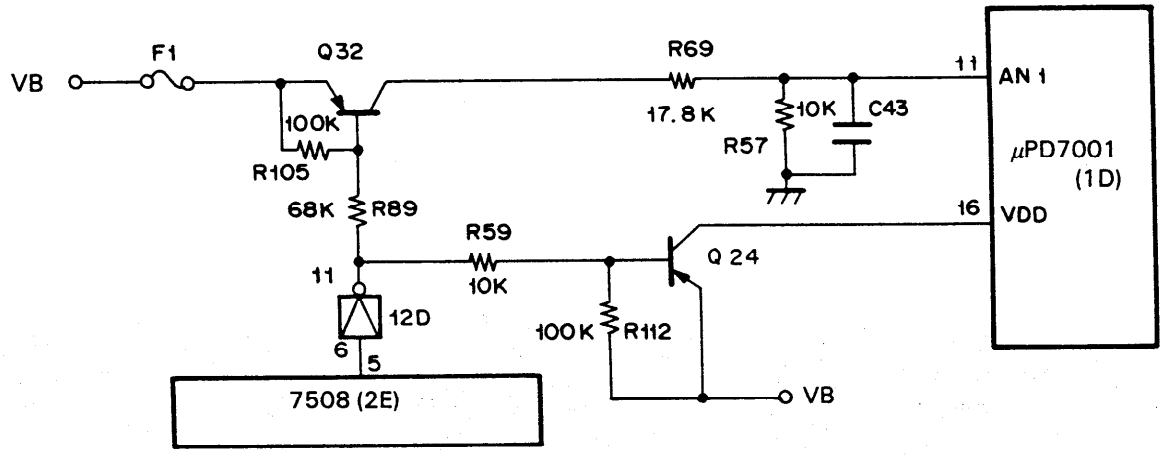


Fig. 2-11 Battery Voltage Detection Circuit

The voltage supplied to the voltage divider circuit may be considered to be the same as the VB voltage. The current flowing through Q32 is so small that the voltage drop across the transistor is negligible. Thus, the divided voltage fed to the AD converter can be represented by the following expression:

$$V_{OUT} = \frac{VB(V) \cdot R57}{R69 + R57} = \frac{VB \cdot 10000}{27800}$$

The analog output (divider output) voltage equivalent to the digital value of D9H is given by multiplying the voltage represented by the least significant bit (SLB) (32 mV) by 217 (D9H). D9H is equivalent to a voltage of approximately 1.7V at the input terminal AN1, as shown below.

$$E = \frac{2}{256} \times 217 \fallingdotseq 1.695 \text{ (V)}$$

where 256 voltage represented by LSB.

The VB voltage which causes the divided voltage to be detected to be a low voltage is approximately 4.7V as given by the following expression:

$$VB_{(X)} = \frac{(R69 + R57)}{R57} \times \frac{2}{256} \times 217 \cdots\cdots \fallingdotseq 4.71 \text{ (V)}$$

Note: The above expressions do not take into account any errors such as the divider resistance errors, etc., and they actually include a total error factor of ±0.1V.

The above low voltage detection is performed regardless of whether power is on or off. After the after low voltage is detected, port 23 of the sub-CPU (pin 5) is back low to prevent further battery power consumption. While power is off, the voltage is **monitored every 10 seconds.**

2.2.3.2 Voltage Sampling During Power Off

1. 12D, pin 11
   1D power supply control
2. 1D, pin 5
   SO (Serial Output)
3. 2E, pin 3
   1D CS control

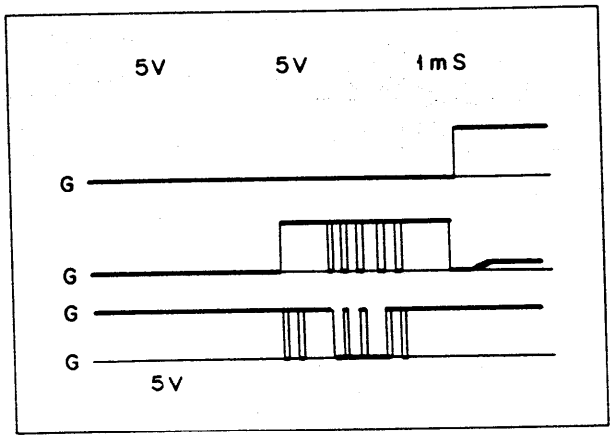


Fig. 2-12

The output at pin 11 of the IC 12D is controlled at port 23 of the 7508 (2E) sub-CPU. While power is off, it is held low for 8 ms **every 10 seconds** to power the IC μPD7001 (1D). Approximately 4 ms after the power supply to the IC, the $\overline{CS}$ signal is input to it for channel selection. Once a channel is selected, the digital data of that channel is output to 1D, pin 5.

2.2.3.3 Circuit Operation After Low Voltage Detection

The 4-bit sub-CPU raises its port 42 (pin 37) high and controls the battery switching from main to auxiliary battery power as follows:

When power is on

- Since port 70 (POW ON) of the sub-CPU is low when power is on, the output at pin 4 of IC 3E is inverted high, holding pin 10 of the IC 3D low as inverted by the IC. The resistor R98 (100 kohms) and the zener diode ZD8 (4V) are connected in series across this pin and the anode of the auxiliary battery.

  Normally, the auxiliary battery is fully charged, since it is always charged in the trickle charge mode, and has an output voltage of 4V or above. Thus, the zener diode intermittently breaks down. This in turn causes the transistors Q15 and Q3 to alternate conduction and cut-off. This operation intermittently continues until the auxiliary battery voltage reaches 4V (discharge final voltage). When Q3 starts conduction after the discharge final voltage is reached, a current flows from the auxiliary battery, which is connected to the emitter of Q3, to the collector; i.e., to the VB line, supplementing its power which is being supplied from the main battery. This operation ensures that the computer operation, such as microcassette rewind, etc., which is in progress when low voltage is detected, is normally completed.
- The high output from port 42 of the sub-CPU is also fed to the base of transistor Q20 to enable the backup voltage supply to the VB+ line from the auxiliary battery. The backup voltage supply ensures that the computer will continue to operate until an operation termination sequence is executed and the low voltage condition is detected. Subsequently, the "CHARGE BATTERY" message is displayed on the LCD panel.

When power is off

- When power is off, the high level of port 70 of the sub-CPU (POW ON) holds the output at pin 4 of the IC 3E low, disabling the AND logic consisting of pins 8, 9, and 10 of the IC 3D and holding the output at pin 10 high. This disables the power supply from the auxiliary battery to the VB line. However, the power supply to the backup line through the transistor Q23 is enabled.

2.2.4 Backup Circuit

The following elements are backed up by the battery voltage (VB) while power is off in order to protect data in the RAMs and maintain a clock feature, etc.

Table 2-3 Battery Protected Component

Location	Element name	Function
4D ~ 7D 4E ~ 7E	RAM	Main RAM (dynamic)
9C ~ 11C	V-RAM	LCD display RAM (static)
2E	4-bit sub-CPU	Power control, keyboard scanning
3D	Gate	Backup line control
3E	Gate	Power-on signal gate
4C, 6A *1D	Gate array 8-bit AD converter	Interrupt and clock control, etc. Battery voltage detection and temperature change detection (for RAM refresh rate determination), etc.

* The operating voltage is supplied for 8 ms every 10 seconds.

The backup circuit is shown in Fig. 2-13. As can be seen, the circuit is normally backed up from the VB line via the transistor Q23, regardless of whether the computer is operating or not. It is backed up from the auxiliary battery when low voltage is detected.

For details of the circuit operations, refer to the descriptions on the power on/off circuit.

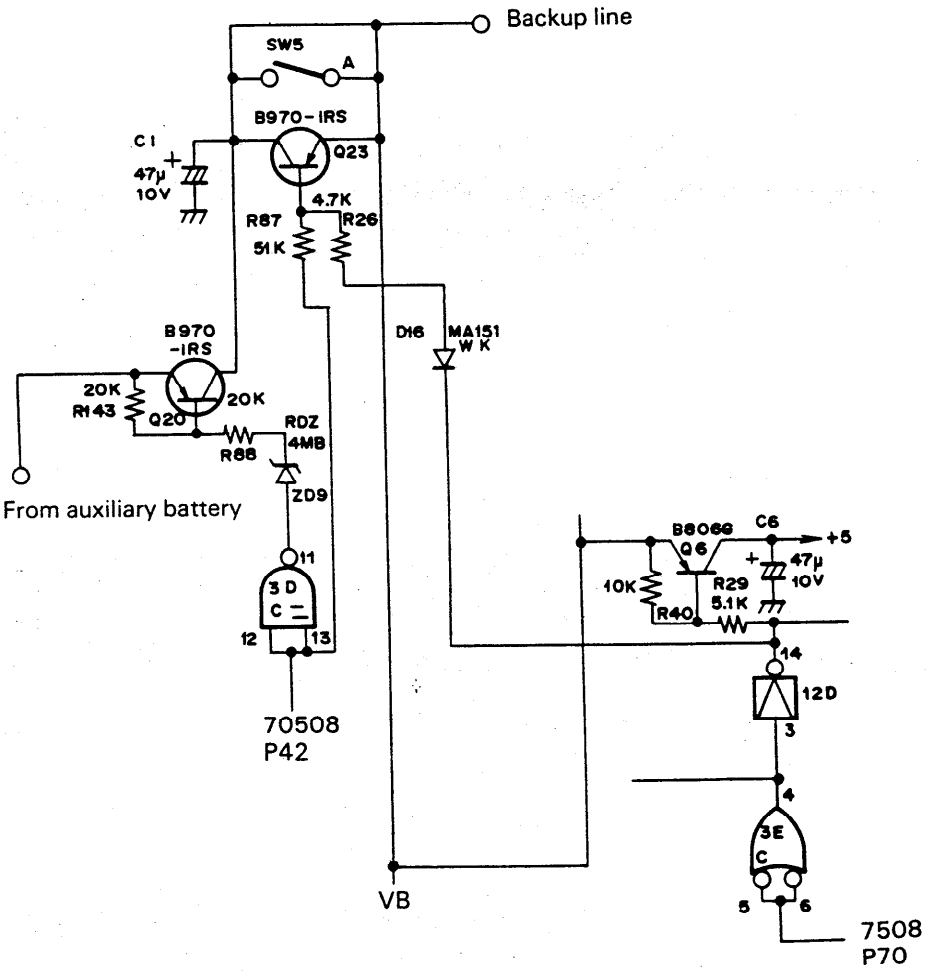


Fig. 2-13 Backup Circuit

2.2.5 DC Voltage Regulators

The MAPLE board is powered by the main or auxiliary +5V Ni-Cd battery. For circuits such as an I/O control section which requires different operating voltages and any special section which requires a larger current, however, voltage regulators are used to convert the battery voltage to the required voltages and prevent the circuit operation from being affected from a voltage drop due to use of large amount of current. The internally used voltage regulators are summarized below:

(1) +5V regulator

Purpose:	ROM capsule power source.
Control:	Enabled when the ROM capsule is reread.
Output voltage:	+5V

(2) LCD drive source regulator

Purpose:	LCD drive power source.
Control:	Always enabled.
Output voltage:	−15V (The LCD is actually driven by a voltage of 20V obtained using the potential difference from the +5V supply.)

(3) RS-232C level source regulator

Purpose:	Sources for the RS-232C levels of ±8V.
Control:	Enabled only when the RS-232C or serial interface is operated.
Output voltage:	±8V

The individual regulators are detailed in the following:

2.2.5.1 +5V Regulator

This regulator supplies power to the ROM capsule. When accessed, the ROM generates such a large transient current that, if it were directly powered by the battery, a momentary low voltage condition would occur due to a voltage drop along the power line, precluding normal operation. To prevent this, the regulator is provided as a power buffer. The circuit operation is detailed as follows (Refer to Fig. 2-14):

- The SWPR signal is low when power is off and is inverted high at pin 10 of the IC 12D. This signal maintains transistor Q28 in conduction, holding the collector low. Thus, the switching signal fed from pin 2 of IC 14D does not appear at the lower terminal of the capacitor C28 (collector of Q28) and the transistor Q19 is cut off, generating no output voltage.
- When power is off, transistor Q28 is cut off by the high level of the SWPR signal, and a clock signal of approximately 35 kHz is fed to pin 14 of IC 24D. This causes a pulse signal at the collector of the transistor Q19, which repeats, switching transistor Q5 on and off.

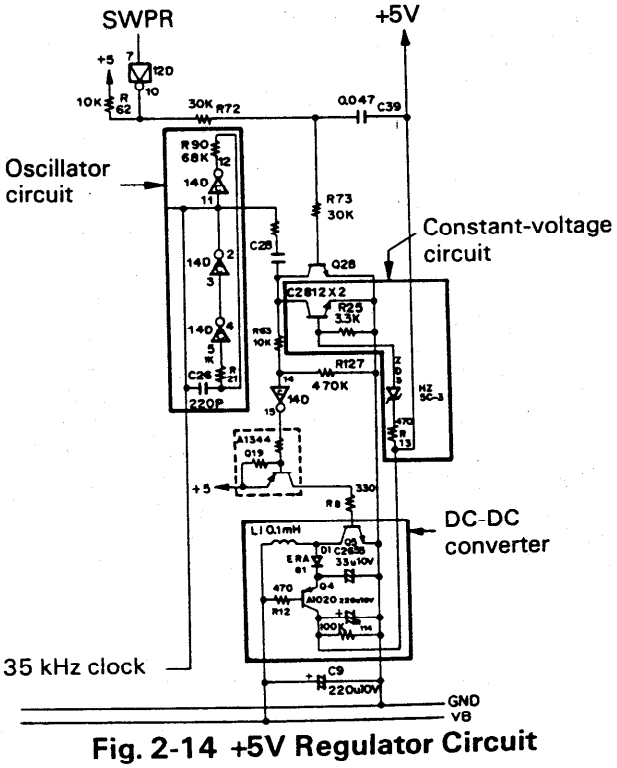


Fig. 2-14 +5V Regulator Circuit

The collector of Q5 is connected to the VB line (+5V) through inductance L1 and the emitter is grounded. When the transistor repeats switching on and off, therefore, a voltage as shown in Fig. 2-15 appears at the collector. This voltage is filtered by the electrolytic capacitor, C3, through the diode D1 to a voltage that exceeds VB. This results in a potential difference across the emitter, and base of the transistor Q4, which causes the transistor to conduct, outputting a DC voltage of approximately 7V at its collector.

Because this output is connected to the constant-voltage circuit, consisting of the resistors R13 and R25, and the zener diode ZD5, the actual output voltage is fixed at +5V by the 5V breakdown voltage of the zener diode. When the Q4 output voltage rises above +5V, ZD5 breaks down at +5V, putting transistor Q22 in conduction, which forces the switching signal to ground level. The output voltage is always maintained at +5V by disabling the switching of Q5. Variation of load is handled by the relatively large capacitance of capacitor C8 (220 μF), connected at the collector of Q4.

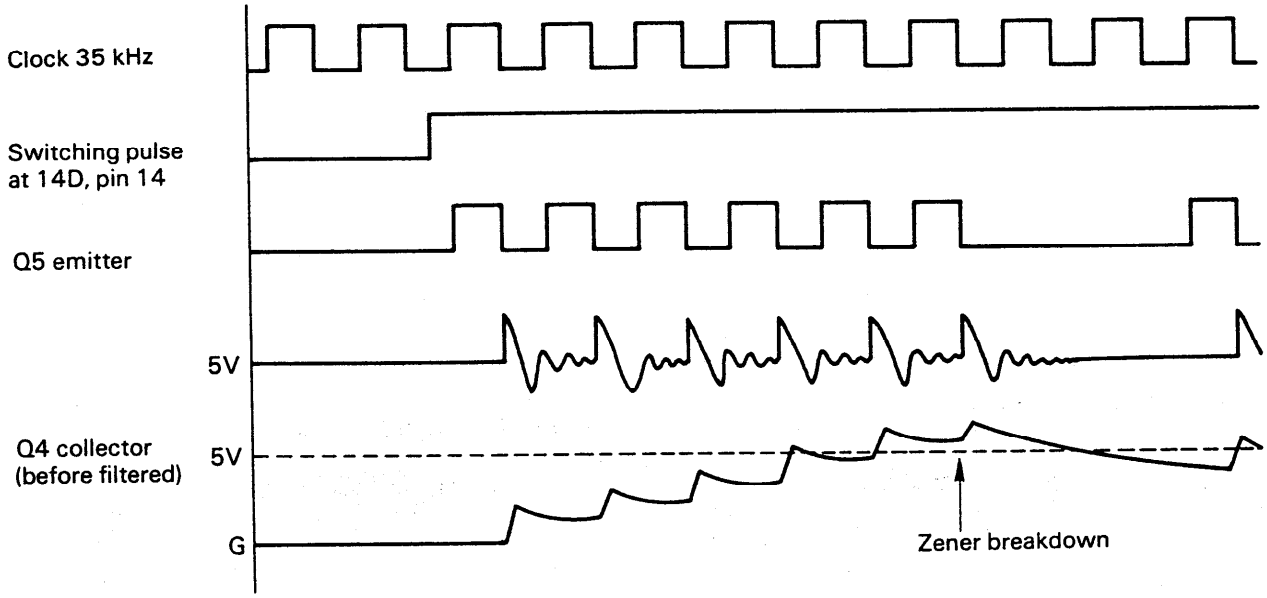


Fig. 2-15 +5V Regulator Voltages

Major actual voltage waveforms are shown below.

(1) Top – Test point: IC 14D, pin 14
(2) Center – Test point: IC 14D, pin 15
(3) Bottom – Test point: Diode D1, cathode

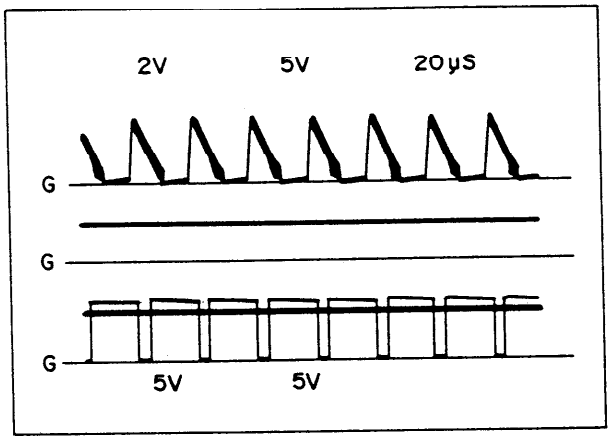


Fig. 2-16 Major Voltage Waveforms In +5V Regulator Circuit

Details of the above waveforms are enlarged below for clarity.

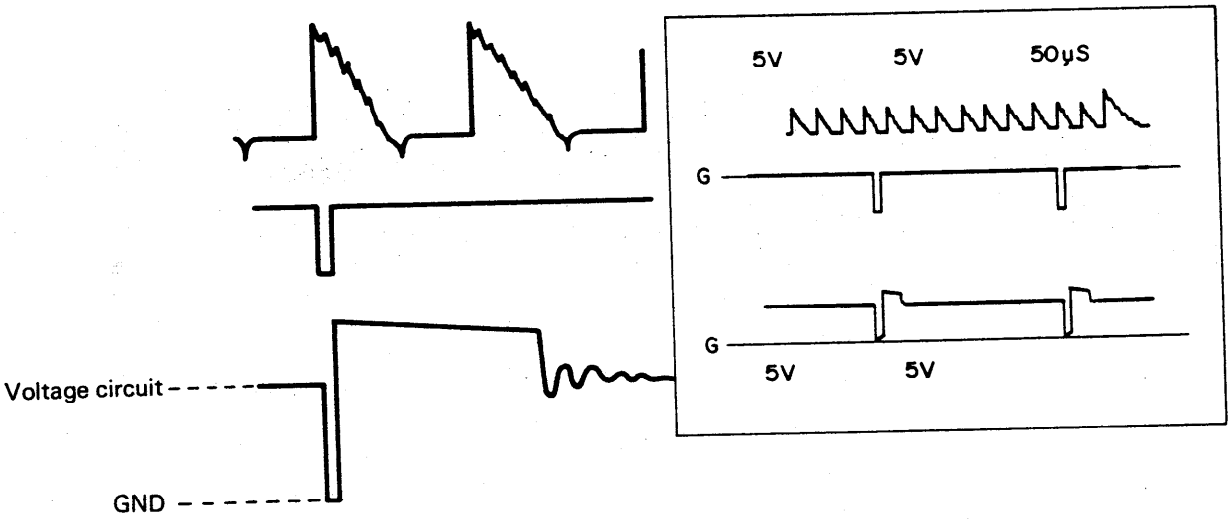


Fig. 2-17 Major Voltage Waveforms Enlarged

Though it looks as if Q5 continued to oscillate due to false images in the above photograph, it actually switches once almost every several switching clock pulses. This ratio varies depending on load.

2.2.5.2 LCD Drive Source Regulator

Two voltage supplies are required to drive the LCD display;
+5V is required for the logic circuit, and 20V is required for the X-Y drivers. A total potential difference of 20V is obtained by subtracting the –15V output voltage of this regulator from the +5V of the logic circuit power supply. Fig. 2-18 shows the regulator circuit.

Circuit Operation

The oscillator circuit generates a clock of approximately 35 kHz when the POWER switch is turned on. This clock is fed to pin 7 of the IC 14D through R55, C27, and R54. The inverted output at pin 6 is input to the base of the transistor Q29 through R20, switching it on and off.

The emitter of Q29 is connected to the +5V logic circuit power supply and the collector is connected to ground through inductance L3. As the transistor is switched on and off by the clock signal, a voltage, as shown in Fig. 2-20 , which is the counter electromotive force across L3, appears at the collector of Q29. While the collector voltage swings negative, a current flows in through diode D6, generating a negative voltage at the negative side of capacitor C17. This output is used as the LCD drive source voltage. It is also fed to the constant voltage circuit which connects the LCD drive voltage to the +5V logic circuit line through the resistor R147 and the zener diode ZD20. The zener diode has a breakdown voltage of 20V. Thus, when the output voltage rises to –15V or above, the zener diode breaks down, raising the base of the transistor Q34 to the high level of +5V. This puts the transistor in conduction and its collector is driven negative, disabling the clock signal to Q29. This stops switching of Q29 and thereby lowers the output voltage. This state is maintained until the zener breakdown comes to an end. At that time, Q29 switches again. The circuit repeats this operation to produce a stable voltage of –15V.

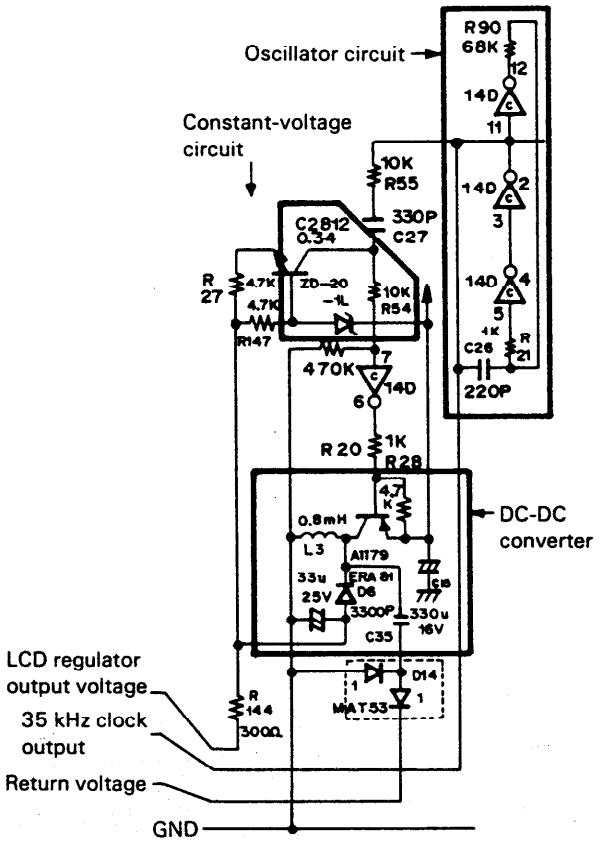


Fig. 2-18 LCD Drive Source Regulator Circuit

The signal generated at the collector of Q29 is fed to the diode D14 through the capacitor C35. The negative component of the signal is removed by a current supply from ground through diode D14, while the positive voltage is fed back to the auxiliary battery through D14.

The diode, inserted across the signal line and ground, clamps the signal to the ground level, eliminating the negative component. While the positive component is fed back to the auxiliary battery via the other diode D14.

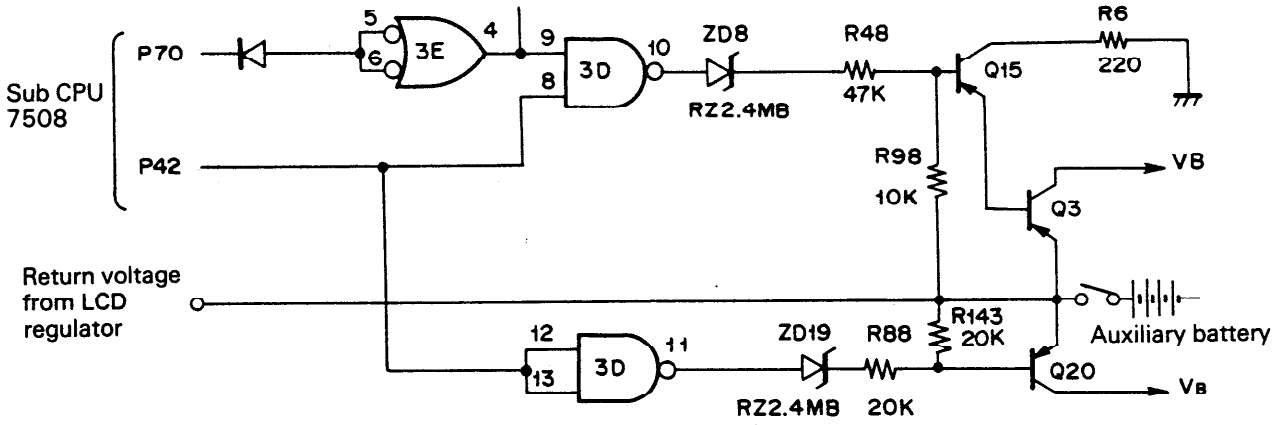


Fig. 2-19 Feedback Circuit

Fig. 2-19 is the feedback circuit redrawn for clarification. This circuit provides the charging path to the auxiliary battery while power is on.

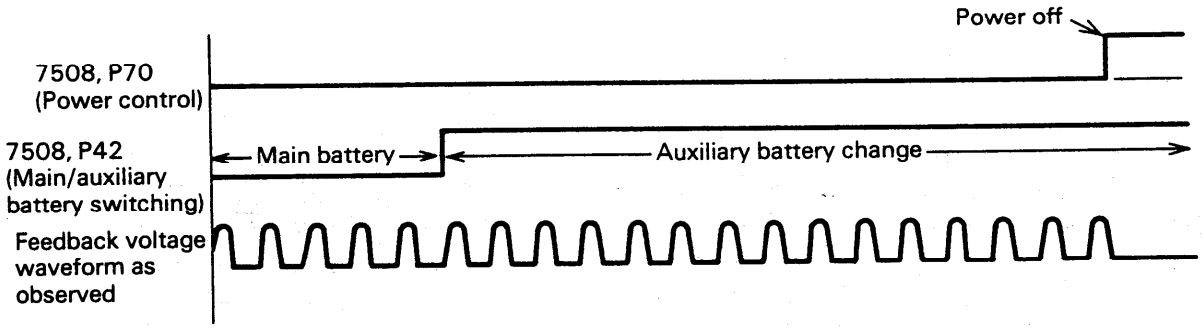


Fig. 2-20 Major Voltages of LCD Drive Power Regulator Circuit

Fig. 2-21 is a photograph of the major voltage waveforms.

(Top) Measured at IC 14D, pin 7
(Center) Measured at IC 14D, pin 6
(Bottom) Measured at diode, anode

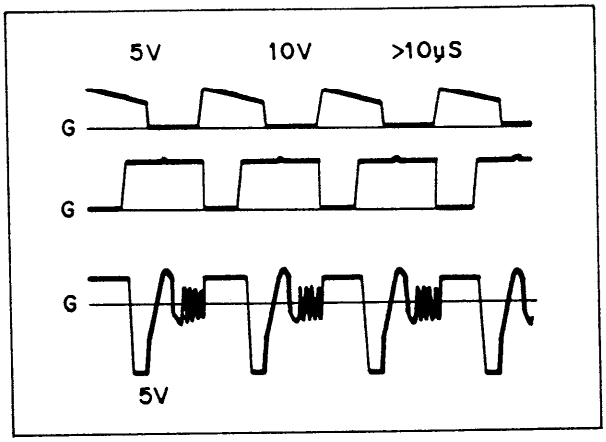


Fig. 2-21 Major Voltage Waveforms of LCD Drive Power Regulator Circuit

* The detailed voltage waveform at the anode of D6, shown below, illustrates an oscillation which occurs during charge/discharge from/to the inductance L3.

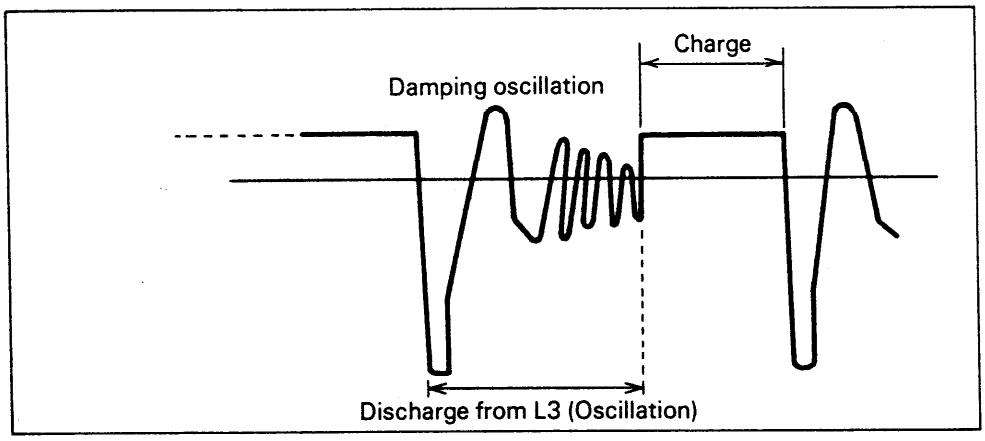


Fig. 2-22 Details of L3 Discharge and Charge Cycle

2.2.5.3 RS-232C Regulator

This regulator is also a DC-DC converter, which is enabled only when the RS-232C or the serial interface is used. The circuit includes a control feature which prevents its output voltage from being used for data transmission during a certain period of the rising time until the voltage is sufficiently stable to be used for the RS-232C levels. IC 4C performs this control function.

● Circuit Operation

IC 4C initially outputs a high signal at pin 26 (SWRS) and a low signal at pin 27 (INHRS). The SWRS signal is inverted by IC 12D and fed to the base of the transistor Q8, turning it on. This causes the battery voltage (VB, +5V) to be output at the collector of the transistor. The INHRS signal is inverted high by 12D and then input to the base transistor Q18, cutting the transistor off. Q17 is also cut off, leaving the transmission line (TXD) floating.

A pulse signal of approximately 35 kHz, generated by a CR oscillator circuit, is supplied to pin 9 of IC 14D through R45, C29, and R46. The inverted output is fed to the base of transistor Q31, switching it on and off. This causes transistor Q17 to also start switching, thus repeating a discharge/charge from or to the inductance L2. This discharge and charge voltage is half-wave rectified by the diode D2, and the positive output voltage is filtered by capacitor C13 to produce a DC voltage of +8V. −8V is generated at the negative pole of capacitor C14 by the negative component charge to capacitor C15 and a negative voltage swing at the anode of diode D3 due to the charge.

Fig. 2-23 shows the timing relationship among the voltages discussed above.

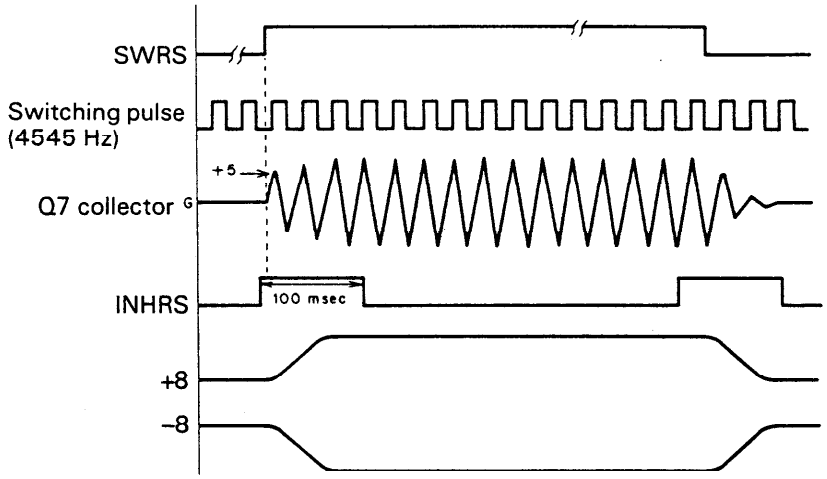


Fig. 2-23 RS-232C Power Regulator Circuit Operation Timing Diagram

The INHRS signal controls the pull-up operation (–8V) for the TXD line. It prevents irregular output voltages from reaching the TXD line. After power is turned on, if the SWRS signal has been activated, the INHRS signal is maintained low for approximately 100 ms, preventing the TXD signal line from being pulled up to unstable voltages. After power is turned off, the INHRS signal is again maintained low for approximately 100 ms in order to prevent a pull-up to unstable voltages.

- Voltage Stabilizer Circuit

The switching of transistor Q31 is controlled by a feedback from the –8V output of this DC-DC converter to the switching circuit to generate a constant output voltage.

When the –8V line voltage is lower, no potential difference is generated across the base (ground) and emitter of the transistor Q21; it is maintained in the off state because the zener diode ZD2 does not break down, and the switching circuit is not affected. When voltage rises to 7V or above, however, ZD2 breaks down at its zener voltage, generating a potential difference across the base and eimitter of Q21, turning it on. In this state, the collector is held at a negative level regardless of the switching pulse. Transistor Q31 is cut off and stops switching, lowering the output potential. This causes the breakdown of ZD2 and allows the switching to be resumed. The sequence of these circuit operations is repeated to provide two stable voltage levels of ±8V.

The RS-232C power regulator switching signal is shown in Fig. 2-24.

(1) Top: Original clock signal – Measured at IC 14D, pin 11.

(2) Bottom: Input to RS – Measured at IC 14D, pin 7.

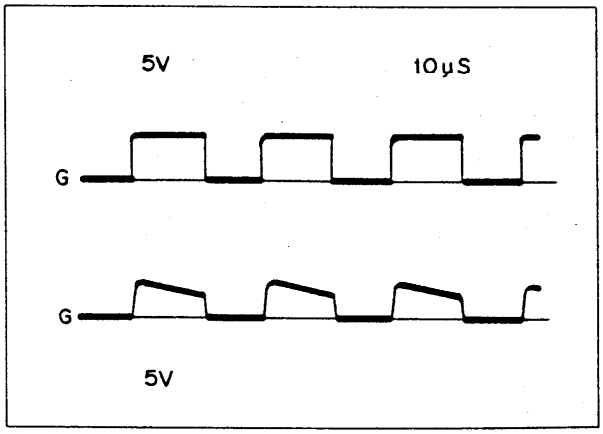


Fig. 2-24

2.3 CPU Operations

Control of memory, I/O, and various other functions is distributed among the three COMS CPUs on the MAPLE board.

(1) Main CPU (Z80).....2.45 MHz

The main CPU provides overall control of circuit operations using the external 32 kB ROM (2A). Its major control functions are:

- Expand interface (CN8) control
- RS-232C interface operation control via a serial controller
- 64 kB dynamic RAM read/write and refresh operation control via a gate array (GAH40D)
- RS-232C interface control via a serial controller (82C51)
- RS-232C clock supply via a baud rate generator (GAH40M)

(2) Sub-CPU (7508).....200 kHz

The sub-CPU provides the following circuit operation control functions independent of the main CPU using the internal 4 kB masked ROM:

- Command exchange with the main CPU via a gate array (GAH40M)
- Power on/off control
- Change mode (normal or trickle) control
- Keyboard data entry check
- DIP switch setting read
- A-D converter enabling/disabling control

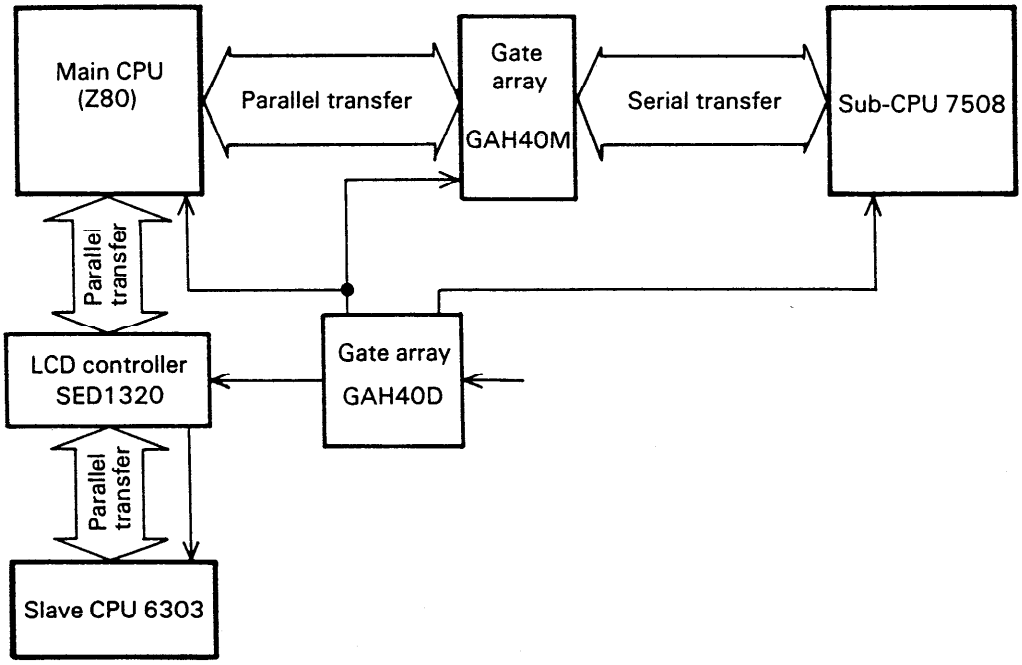
(3) Slave CPU (6303).....614 kHz

The 6303 provides the following control functions independent of the main CPU, using the internal 4 kB masked ROM:

- Command exchange with the main CPU via the LCD controller (SED1320)
- Microcassette control via a gate array (GAH40S)
- High speed serial interface control
- Speaker output control
- LCD display control via the LCD controller (SED1320)
- ROM capsule read control via a gate array (GAH40S)

2.3.1 Handshaking Between Main CPU and Sub-CPUs

The three CPUs operate using a clock supplied from a gate array (GAH40D), which has a built-in frequency divider circuit. Data and commands are exchanged between the main CPU and the two sub-CPUs as follow:



Data exchange between Z80 and 6303: Handshaking is accomplished via the LCD controller.
Data exchange between Z80 and 7508: Handshaking is accomplished via the gate array GAH40M.

Fig. 2-25 Data/Command Exchange Between Main CPU and Sub-CPUs

2.3.1.1 Data/Command Exchange Between Main CPU and Sub-CPU 7508 via GAH40M

Commands are transferred in parallell between the main CPU and gate array and serially between the gate array and sub-CPU 7508. Handshaking among the CPUs is performed via the read/write control on the serial/parallel conversion register in the gate array. Fig. 2-26 illustrates this control.

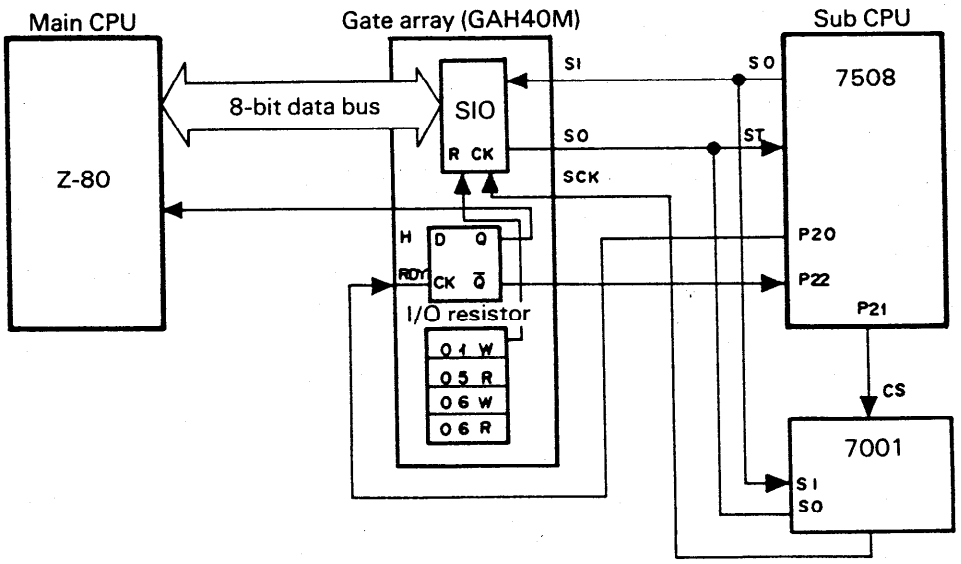


Fig. 2-26 Main CPU and 7508 Handshaking Control

Handshaking is accomplished using a flipflop (FF) within the gate array. The FF signals, when it is set, that the main CPU may access the serial I/O (SIO) register in the gate array; the sub-CPU is issued an interrupt, when it is reset, that a command has been written to the SIO from the main CPU, and is available for access by the sub-CPU.

- Operation sequence between main CPU and gate array.
  1. Main CPU reads the I/O address 05H (status register) and checks the state of bit 2 (the FF). The bit indicates, when it is on, that the main CPU may access SIO.
  2. Main CPU reads or writes SIO (I/O address 06H).
  3. Main CPU writes bit 1 of the command register (I/O address 01H) and sets FF.

- Operation sequence between the sub-CPU and gate array .
  1. Sub-CPU waits until its port 22 goes high (this occurs when FF is reset by the main CPU), indicating that main CPU has stored a command in SIO.
  2. Sub-CPU issues the shift clock (SCK) and reads in the command from SIO one bit at a time and performs the specified processing.
  3. Sub-CPU activates its port 22 to set the FF-setting. The FF informs the main CPU that the command has been received and the SIO is now available for access by the main CPU.

- Fig. 2-27 illustrates the interfacing operation between the main CPU and sub-CPU 7508 via the gate array.

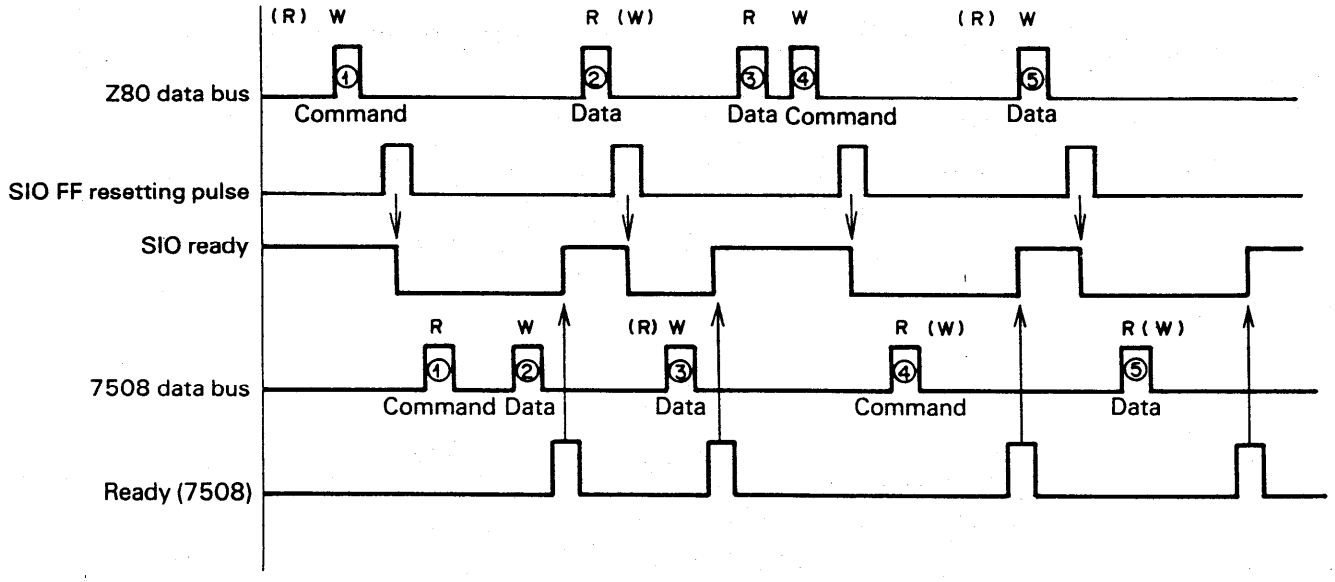


Fig. 2-27 Main CPU and Sub-CPU Interfacing Signal Timing

As can be learned from the figure, the handshake is accomplished via the SIO READY signal as follows:

When SIO READY is set : Z80 ←→GAH40M
When SIO READY is reset : 7508 ←→GAH40M

The SIO READY signal is set and reset by the following signals:
SIO READY is reset when READY FF is reset by bit 0 of Z80 I/O address 01.
SIO READY is set by 7508 port 22.

- The SIO READY signal is set and reset either by a command (data) or interrupt. The operations are illustrated by Fig. 2-28

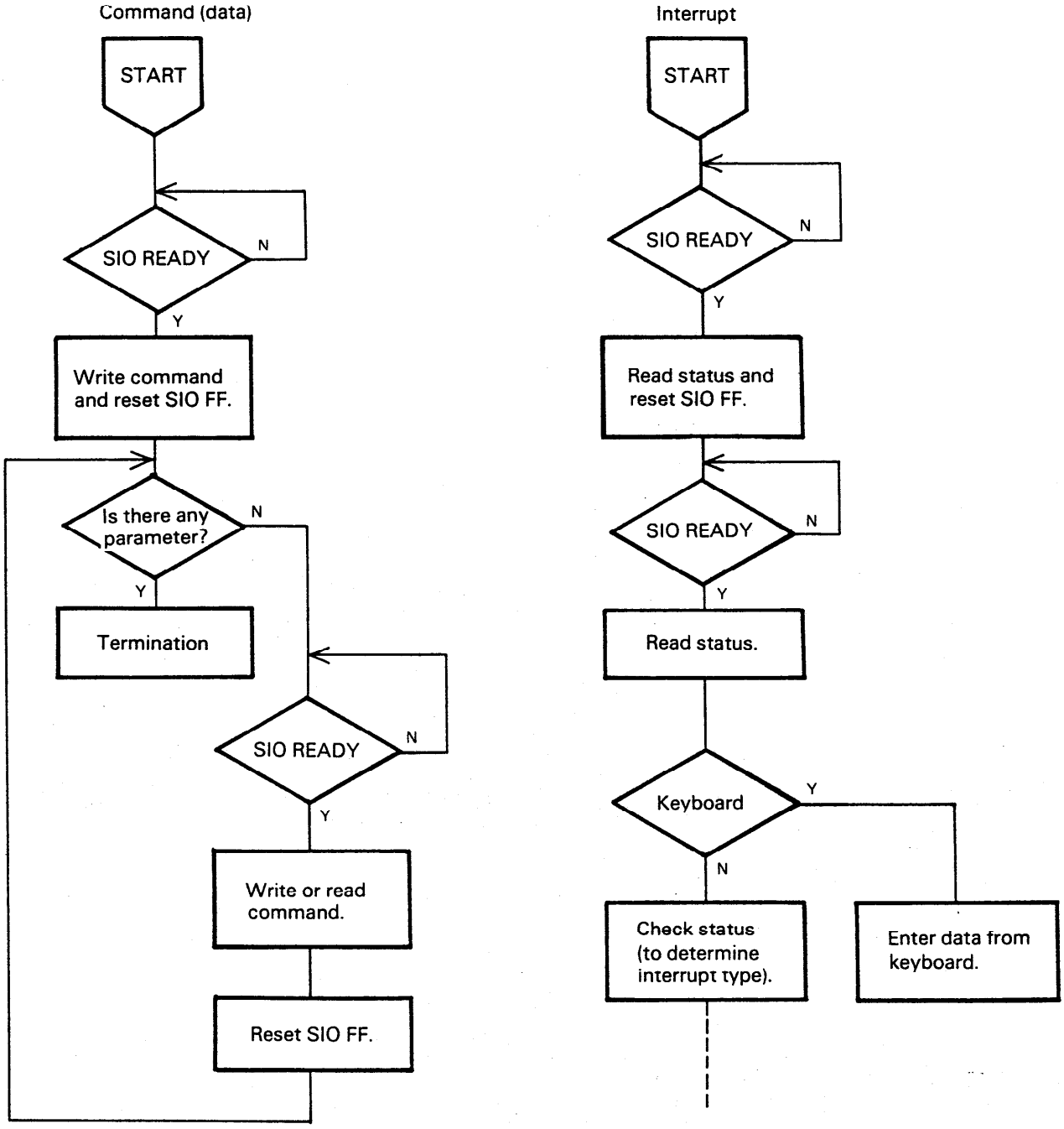


Fig. 2-28 Main CPU and Sub-CPU Interfacing Operations

(Serial Data/Command Transfer)

Data such as A-D conversion data which are exchanged between the following components are serially transferred:

(1) Between sub-CPU 7508 (2E) and A-D converter 7001 (1D)

- AN0 channel selection and temperature data transfer
- AN1 channel selection and battery voltage data transfer
- AN2 channel selection and external analog input data transfer
- AN3 channel selection and barcode data transfer

(2) Between sub-CPU 7508 (2E) and gate array GAH40M (4C)

- Channel selections listed in (1) above and data transfer
- Keyboard and DIP switch data transfer

Fig. 2-29 shows the transfer paths of the above serial data.

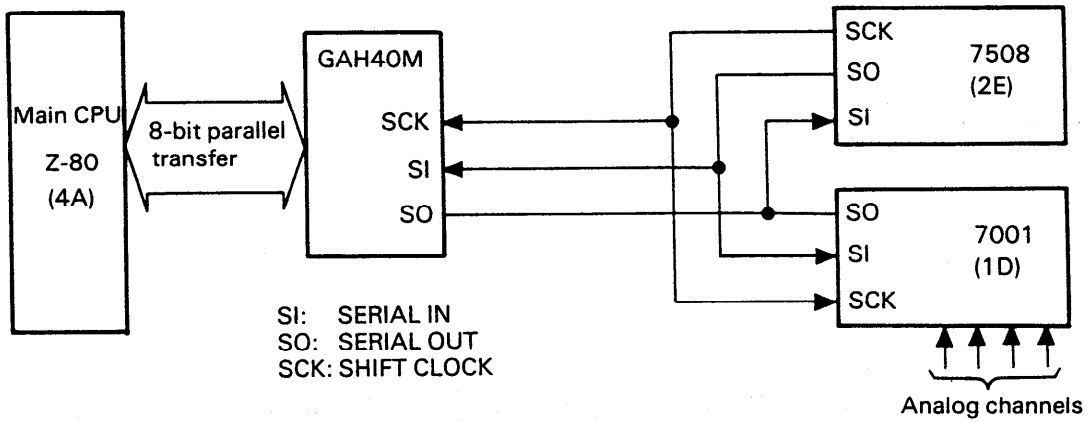


Fig. 2-29 Serial Data Transfer

The operations listed in (1) and (2) above are controlled by the appropriate commands of the main CPU and the sub-CPU 7508. The operation sequence executed when the main CPU reads data from the A-D converter 7001 is shown below.

(1) Main CPU reads I/O address 05 and examines whether bit is on (high) – examines whether a analog data read command may be issued by checking the state of the handshaking FF in the gate array GAH40M (bit 0 of I/O address 05). If the previous command has been processed, bit 0 is on, indicating that the command may be issued (as signalled by RDY SIO).

(2) Main CPU writes the 1-byte command at I/O address 06 (SIOR resistor) – stores the command in the SIOR register in the gate array GAH40M.

(3) Main CPU writes bit 1 of I/O address "01" – this causes an interrupt to sub-CPU which informs it that the command has been stored in the SIOR register (RDY SIO is reset).

(4) Sub-CPU issues eight shift clock (SCK) pulses to gate array and reads in the 8-bit command from the SIOR register.

(5) According to the received command, sub-CPU activates (lowers) the $\overline{CS}$ signal to the A-D converter to select it and then issues the channel selection data in synchronization with the shift clock.

(6) Sub-CPU deactivates (raises) the $\overline{CS}$ signal to allow the A-D converter to perform the specified A-D conversion. Then, the sub-CPU lowers the $\overline{CS}$ signal again and reads in the converted data by issuing eight read shift clock pulses.
(7) Sub-CPU sends the A-D converted data, in synchronization with the shift clock pulses, to the SIOR register in the gate array GAH40M.
(8) Main CPU reads I/O address 06 to read in the 1-byte data.

2.3.1.2 Data/Command Exchange between Main CPU and Sub-CPU 6303 via SED1320

Data/Commands are transferred in an 8-bit parallel format between Z80, the main CPU, and the sub-CPU 6303 via two registers in the gate array SED1320. Fig. 2-30 illustrates the control flow.

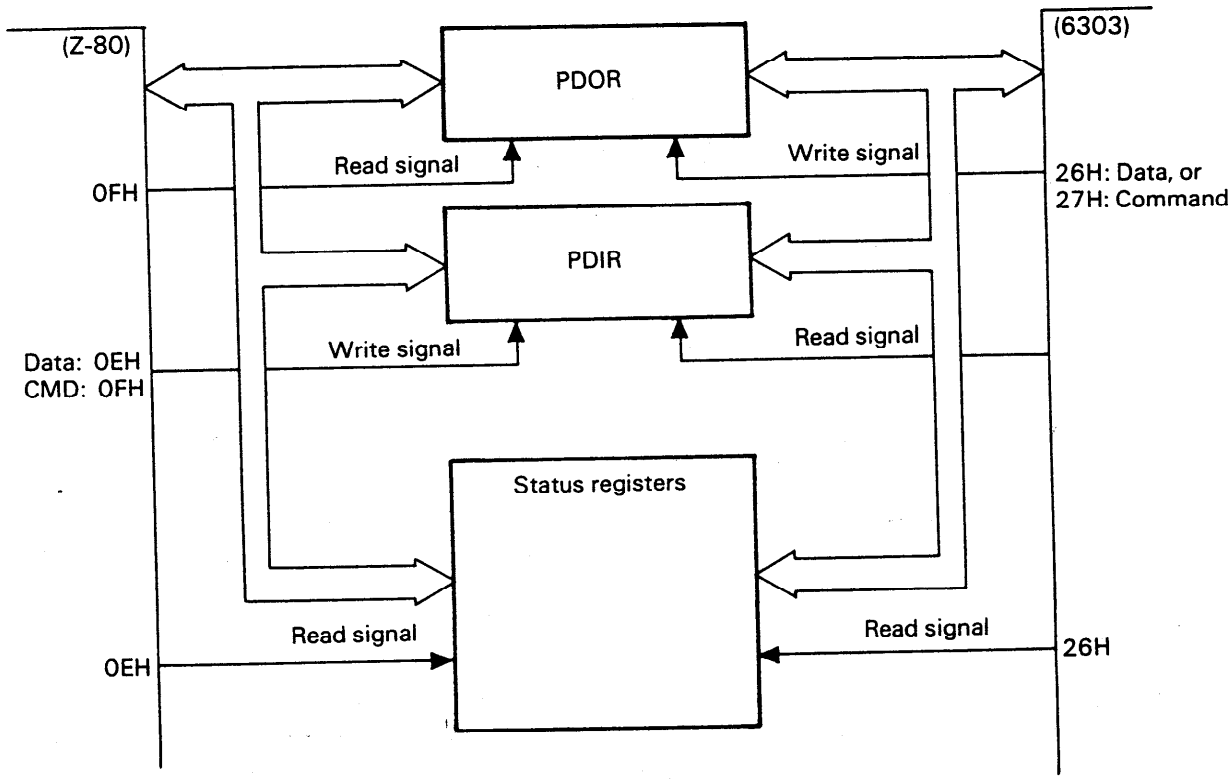


Fig. 2-30 Control Flow for Data/Command Transfer between Z80 and 6303

Handshaking between the Z80 and 6303 is performed via the two status registers in SED1320 which are respectively assigned to the CPUs. Each of the registers has Input Buffer Full (IBF), Output Buffer Full (IBF), and Flag (FI) bits as shown in Fig. 2-31. Data outputs (write) and inputs (read) are controlled by the state of these status bits. The handshaking between the two CPUs is explained below.

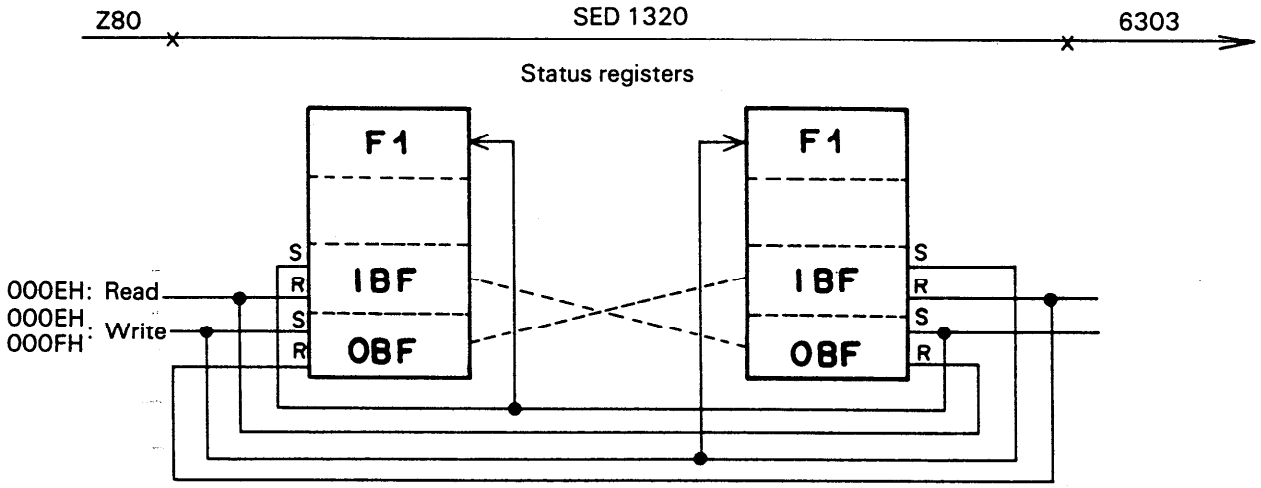


Fig. 2-31 Handshaking Between Z80 and 6303

The status registers are accessed from both Z80 and are 6303 and used as follows:

Output

When either the Z80 or 6303 outputs 1-byte data, the OBF bit of one status register and the IBF bit of the other status register are set. This informs the other CPU that the 1-byte data has been stored in the gate array SED1320, ready to be read.

Input

When the CPU reads the data from SED1320, the IBF bit of its status register and the OBF bit of the other register are reset after the data is read in. These input and output operations are asynchronous.

2.3.1.3 Memory Space

There is a memory space on the MAPLE board which includes the following RAMs and ROMs:

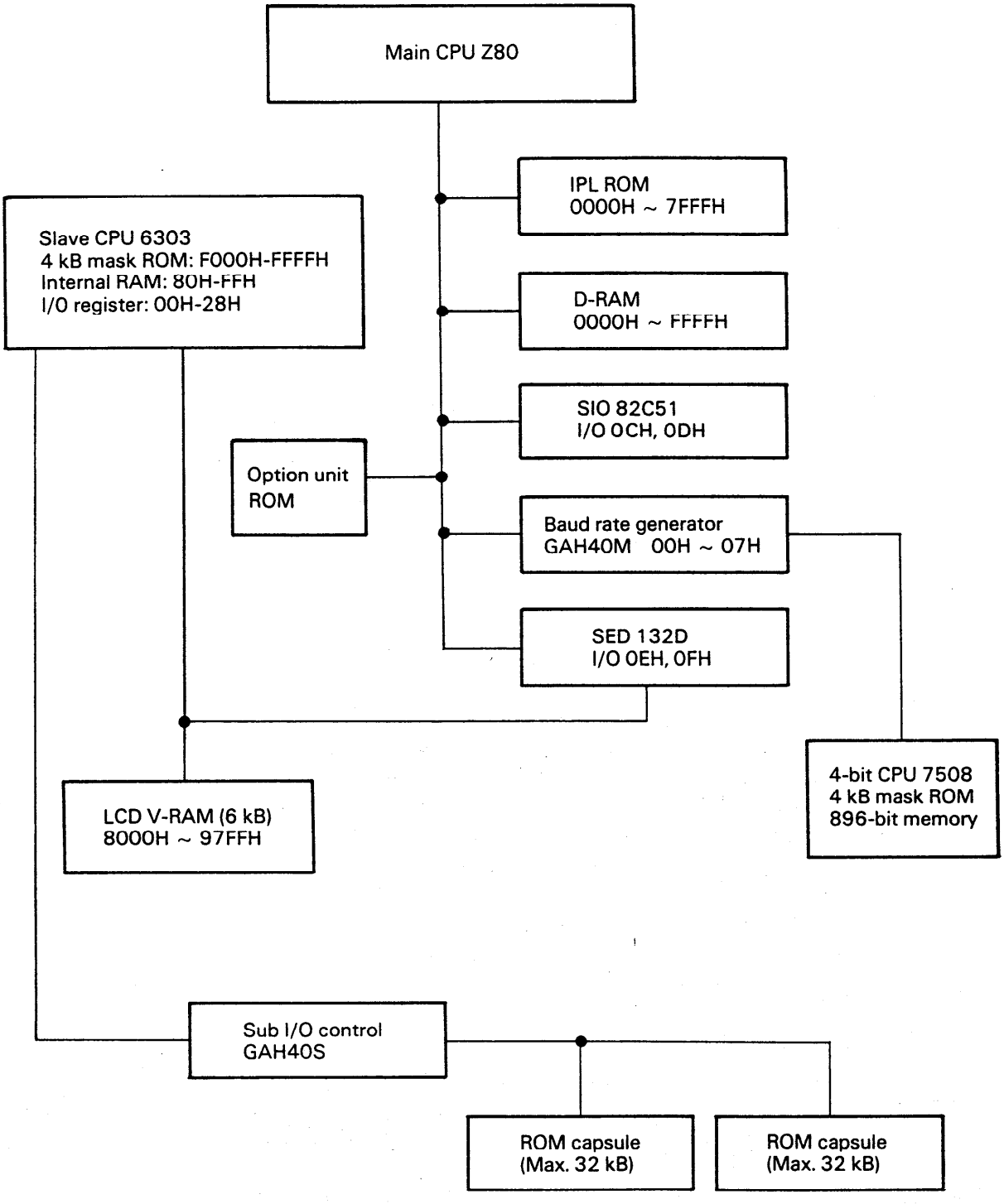


Fig. 2-32 Memory Space

2.3.2 Operations of Main CPU (70008)

The Main CPU Z80 operates using control programs contained in the 32kB ROM (2A) to control the slave CPU 6303, sub-CPU 7508, gate arrays, D-RAM, and serial controller 82C51, etc. The slave and sub-CPUs are controlled via the handshaking gate arrays.
These control operations are accomplished using the I/O addresses listed in table 2-4.

Table 2-4 I/O Address

I/O adress	Read/Write access	Circuit component	Function
0000	R	GAH40M	Input Capture register (L) command trigger
	W	GAH40M	Control register
0001	R	GAH40M	Input Capture register (H) command trigger
	W	GAH40M	Command register
0002	R	GAH40M	Input Capture register (L) barcode trigger
	W	GAH40M	Control register
0003	R	GAH40M	Input Capture register (H) barcode trigger
0004	R	GAH40M	Interrupt Status register
	W	GAH40M	Interrupt Enable register
0005	R	GAH40M	Status register
0006	R	GAH40M	Serial I/O register
	W		Serial I/O register
0007 ~ 0008			Unused
000C	W	82C51	Command
000D	R/W	82C51	Data
000E	R	SED 1320	Status
000F	R	SED 1320	Data
	W		Command register
0010 ~ 00FF			Unused

2.3.2.1 Reset

Three negative going swings of the clock signal supplied at the $\overline{RS}$ terminal cause the internal initialization of the line CPU 70008, which then waits for the reset condition to be removed. When the reset signal is discontinued, the CPU begins executing its program from address 0000H (the start address of the ROM located at 2A). The internal initialization sequence occurs as follows:

- Resetting the Program Counter (PC) to 0000H
- Resetting the Interrupt Enable flipflop (IFF) to 0
- Resetting the Index register (I) and the memory Refresh register (R) to 00
- Resetting the interrupt mode to 0
- Forcing all address/data bus lines in the high impedance state
- Diactivating all control signals

2.3.2.2 Memory Bank Switching

The main CPU controls memory using 16 address lines, making it capable accessing a memory space of 64k bytes from address 0000 to FFFF. However, the CPU memory space includes a 32k byte ROM and an option unit ROM, in addition to the 64k byte dynamic RAM. To allow the CPU to access this entire memory space which is greater than 64k bytes, bank switching signals are used.

Note: When a RAM disk is used as option unit, no memory back switching is made but the main CPU controls the external RAM as an I/O port.

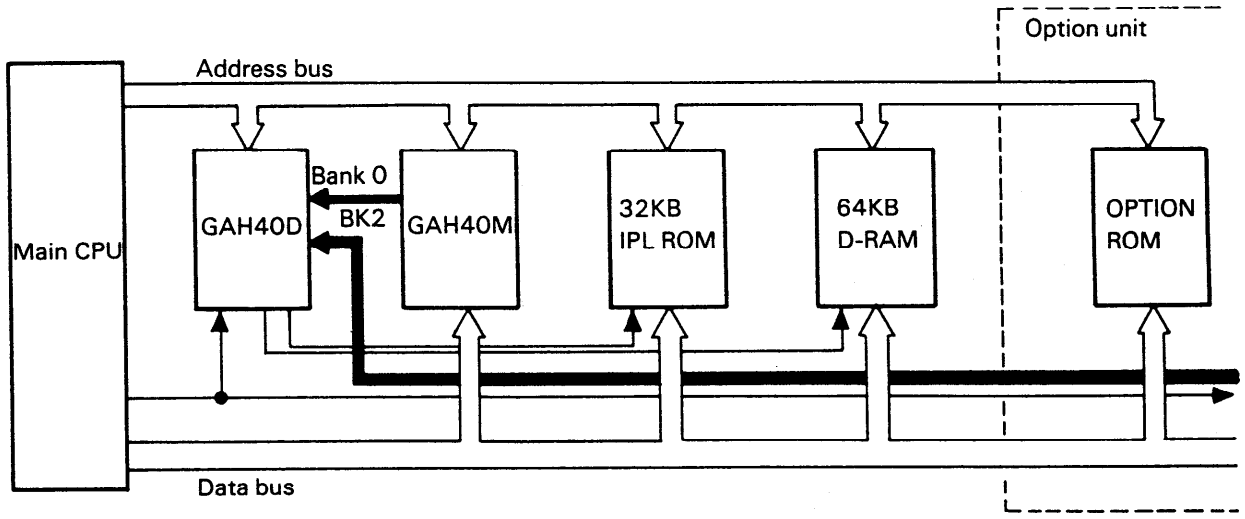


Fig. 2-33 Memory Configuration

The entire memory space is divided into the four banks (listed in Table 2.5), which are selected by a combination of the BANK 0 and BK 2 signals shown in Fig. 2-32.

Table 2-5 Memory Bank Selection

BK2 / BANK 0 / Address	1	1	0	0
	0	1	0	1
FFFF ~ 8000	D-RAM (H)	D-RAM (H)	OPTION ROM (H)	OPTION ROM (H)
7FFF ~ 0000	IPL ROM	D-RAM (L)	IPL ROM	OPTION ROM (L)

As shown in Fig. 2-33, two band control signals, BANK 0 and $\overline{\text{BK 2}}$, are used, both are fed to the gate array GAH40D. Because $\overline{\text{BK 2}}$ is pulled up on the MAPLE board, only the left two D-RAMs and IPL ROM are addressed when no option unit (with ROM) is available.

2.3.2.3 Interrupt

There are only two external interrupt signals to the main CPU; $\overline{INTR}$ and $\overline{BURQ}$. The $\overline{NMI}$ signal is not used. The main CPU interrupts are discussed in the following.

1. INTR interrupts

The INTR interrupts include the interrupts INT0 through INT5 from the sub-CPU 7508, the serial controller 82C51, the RS-232C interface, the gate array GAH40M, and the option unit. These interrupts multiplexed by GAH40M and fed to the main CPU as single interrupt request via the gate array GAH40D (Fig. 2-34).

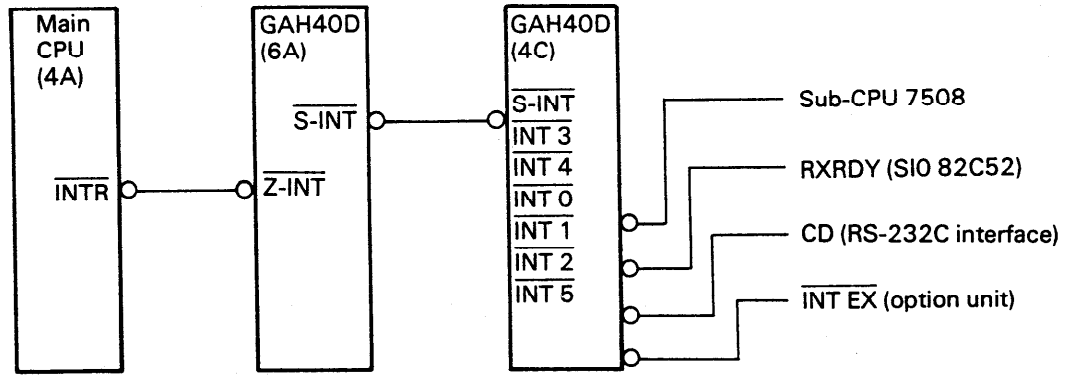


Fig. 2-34 INTR Interrupt Request Routing

The two interrupt requests of INT3 (Input Capture flag) and INT4 (Overflow flag) are generated within GAH40M. All six interrupts are controlled in GAH40M from the main CPU by the corresponding interrupt control bits at I/O address 0004 listed in Table 2-6

Table 2-6 Interrupt Control Bits

Interrupt control bit	Bit name	Interrupt vector	Interrupt control bit	Bit name	Interrupt vector
7	Unused	—	3	IER 3 (ICF)	F6
6	Unused	—	2	IER 2 (RS-232C)	F4
5	IER 5 (Option unit)	FA	1	IER 1 (SIO 82C51)	F2
4	IER 4 (OVF)	F8	0	IER 0 (sub-CPU 7508)	F0

When the INTR signal is generated with the interrupt enabled (i.e., the corresponding IER bit ON), the main CPU enters the interrupt processing program after the current instruction has been executed.

2. $\overline{BURQ}$ interrupt

This interrupt request singal is fed from the option unit o the main CPU. When it goes low, the main CPU forces the address bus, daga bus, and system control terminals ($\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$, and $\overline{WD}$) in to a high impedance state, making the buses available for use by the option unit after the current instruction has been executed.

*The interrupt request signals and their function summaries are listed in Table 2-7 in priority order.

Table 2-7 Interrupt Request Signal and Their Priority

Interrupt Priority order	Signal name	Function	Vector address
Highest	$\overline{BURQ}$	External bus request from **option unit**	—
↓	$\overline{NMI}$	Unused	—
↓	INTR (INT 0)	Alarm and low voltage detection from **sub-CPU 7508**	F0
↓	INTR (INT 1)	1-byte received from **serial controller 82C51**	F2
↓	INTR (INT 2)	CD signal from RS-232C interface	F4
↓	INTR (INT 3)	Barcode trigger within **gate array GAH40M**	F6
↓	INTR (INT 4)	Free running counter overflow within **gate array GAH40M**	F8
Lowest	INTR (INT 5)	Interrupt from option unit	FA

3. Intrerrupt vectors

When accepting an enabled interrupt request via the $\overline{Z\text{-}INT}$ terminal of GAH40D, the main CPU makes an indirect call to the interrupt processing routine using the contents of the I register and the read vector address – this call is called madkable interrupt mode 2 operation.

Fig. 2-35 shows the signal timing from the time the interrupt is accepted until the interrupt routine is entered by the indirect call. A concept of the controlling scheme is also presented.

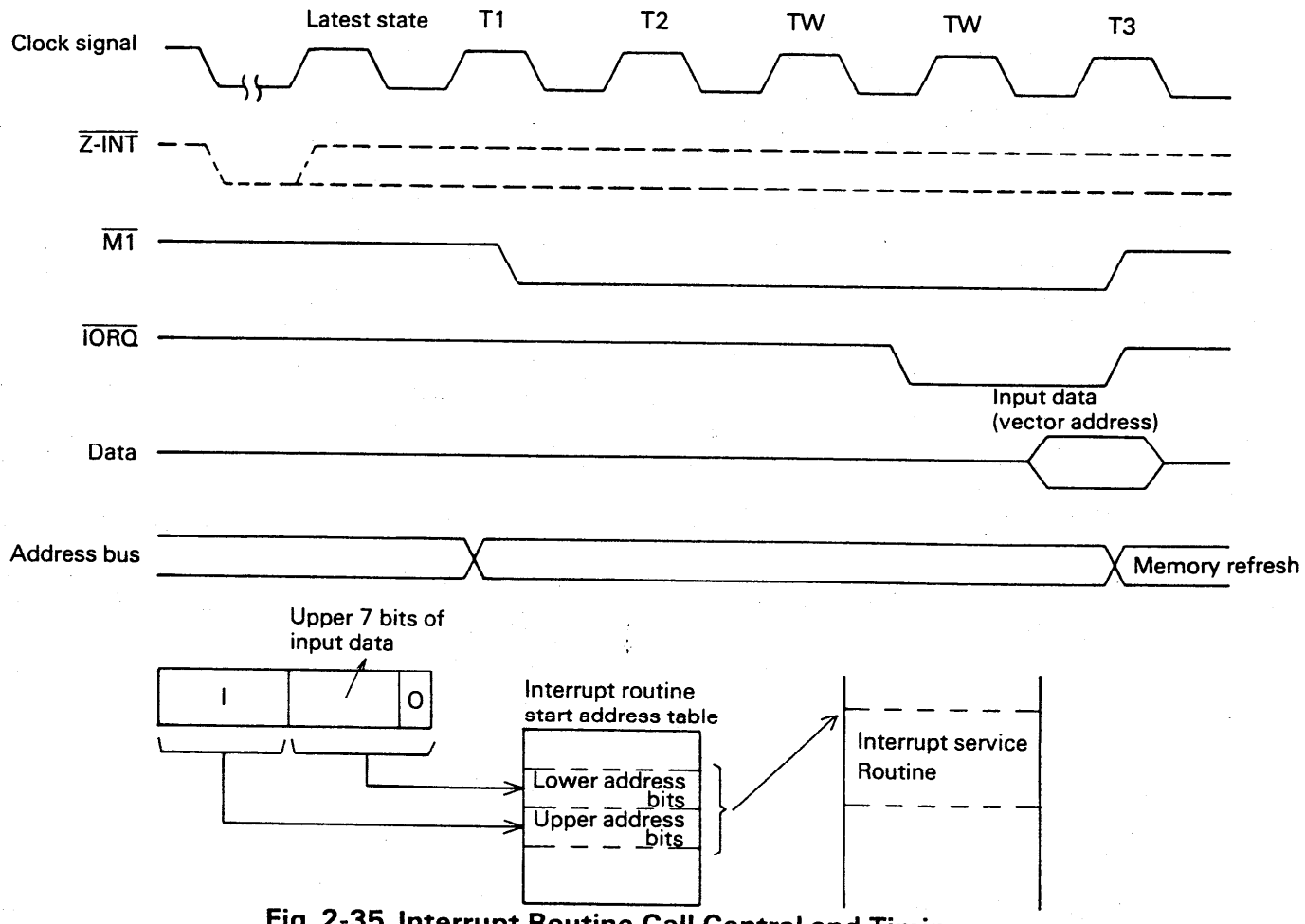


Fig. 2-35 Interrupt Routine Call Control and Timing

When the $\overline{\text{Z-INT}}$ signal is activated, the main CPU samples the signal at the rising edge of the clock signal in the last state of the current instruction execution and generates an M1 cycle which includes two extra wait cycles. Then, the CPU reads data (a vector address) from GAH40M at the rising edge of T3 in the M1 cycle and begins the interrupt processing.

Observed Memory Control Signal Waveforms

(Top) CLK:
Measured at 4A, pin 6
(Second from top) M1:
Measured at 4A, pin 27
(Second from bottom) $\overline{\text{MRQ}}$
Measured at 4A, pin 19
(Bottom) RF:
Measured at 4A, pin 28

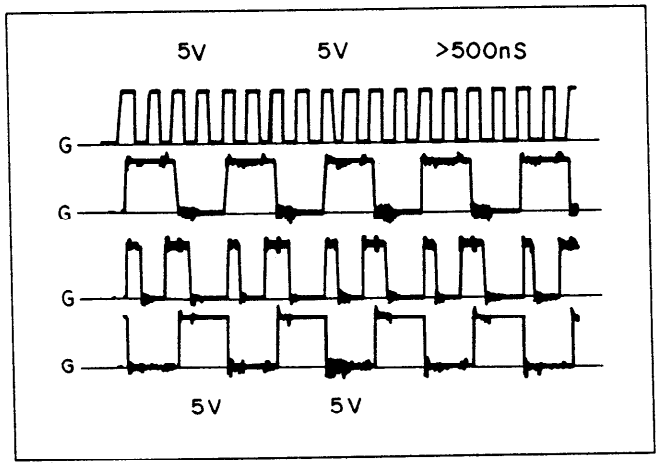


Fig. 2-36 CLK, M1, $\overline{\text{MRQ}}$, and RF

(Top) CLK:
Measured at 4A, pin 6
(Second from top) $\overline{\text{MRQ}}$:
Measured at 4A, pin 19
(Second from bottom) $\overline{\text{RF}}$:
Measured at 4A, pin 28
(Bottom) $\overline{\text{RD}}$:
Measured at 4A, pin 21

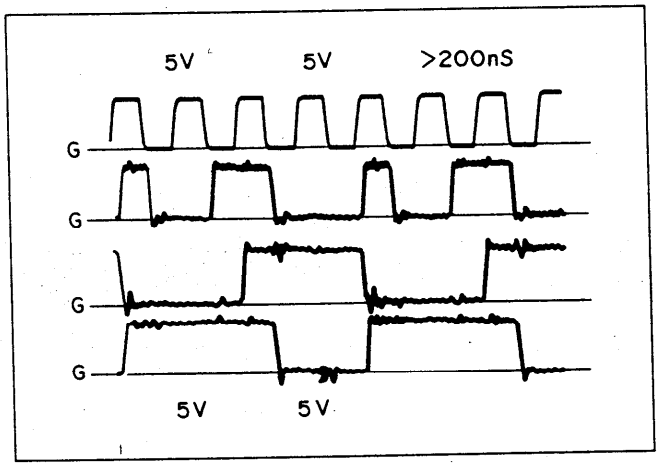
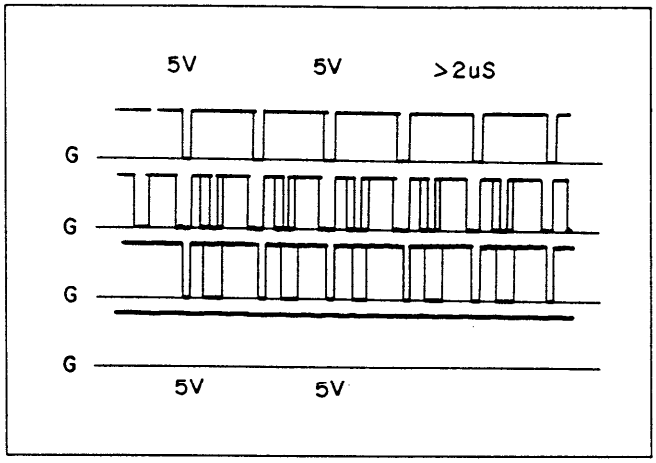


Fig. 2-37 CLK, $\overline{\text{MRQ}}$, $\overline{\text{RF}}$, and $\overline{\text{RD}}$

Observed D-RAM Control Signal Waveforms

(Top) W1:
Measured at 6A, pin 18
(Second form top) $\overline{RAS1}$:
Measured at 6A, pin 17
(Second from bottom) $\overline{CAS1}$:
Measured at 6A, pin 44
(Bottom) $\overline{RF}$:
Measured at 6A, pin 40



Enlarged

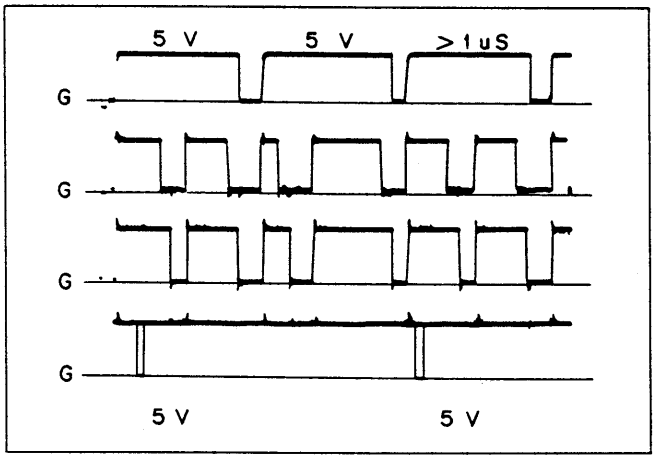


Fig. 2-38 W1, $\overline{RAS1}$, $\overline{CAS1}$, and $\overline{RF}$

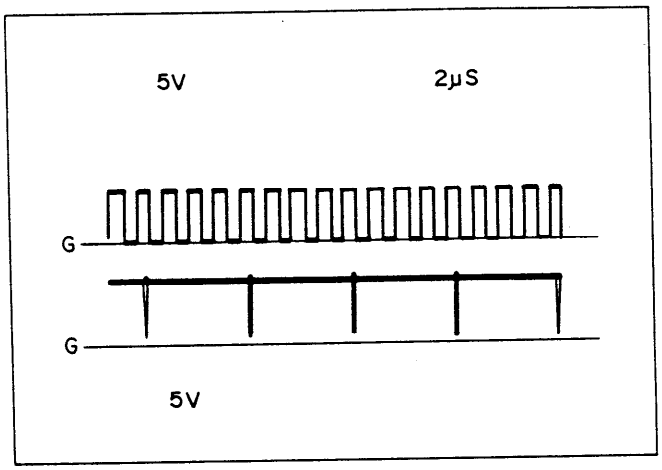
Observed D-RAM Refresh Signal Waveforms

(Top) $\overline{\text{Z-RF}}$:

Measured at 6A, pin 29

(Bottom) $\overline{\text{FR}}$:

Measured at 6A, pin 40



Enlarged

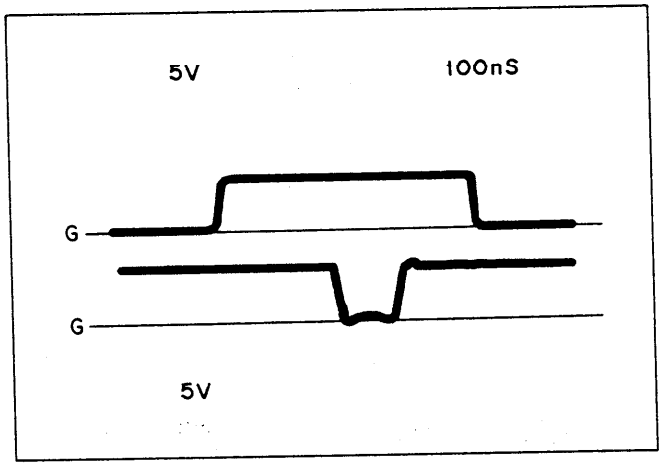


Fig. 2-39 $\overline{\text{Z-RF}}$ and $\overline{\text{RF}}$

2.3.3 Operations of Slave CPU 6303

The slave CPU 6303 is an 8-bit CMOS CPU, which controls the microcassette tape (MCT), liquid crystal display (LCD), ROM files, external speaker, and serial interface.

2.3.3.1 Operation Modes

The operation mode of the 6303 slave CPU is determined by the state of three ports, P20, P21, and P22. Performance of mode setting is a hardware based function, occurring immediately after power up or whenever the reset switch is pressed. When the reset signal goes high, the CPU latches the state of the three ports in an internal register. When the reset signal is deactivated, the operation mode is determined according to the information latched.

The slave CPU performs the following sequence of operations after each deactivation of the reset signal:

- Latches bits 2, 1, and 0 of port 2 in the Program Control Register.
- Sets the vector address FFFE and the contents of the byte location addressed by FFFF to the program counter.
- Sets the interrupt mask bits.
- A data address is read from the vector address, FFFF, is sent to the program counter,and initiates program execution from that address.

* Program Control Register (0003H) – stores the state of ports 20, 21, and 22, used for determining the operation mode.

Fig. 2-40 illustrates a sample CPU operation mode selection, mode 6 (multiplexed/partial decode), from the shown combination of port states.

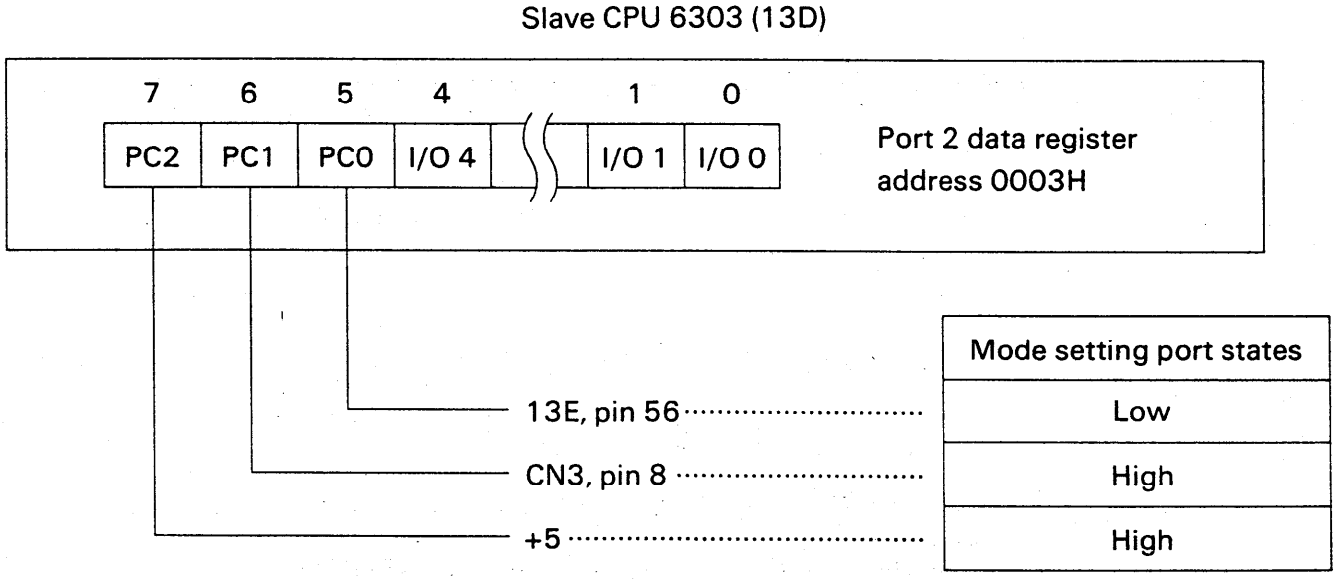


Fig. 2-40 Slave CPU Operation Mode Selection Example

Mode selection reults in the following memory mapping:

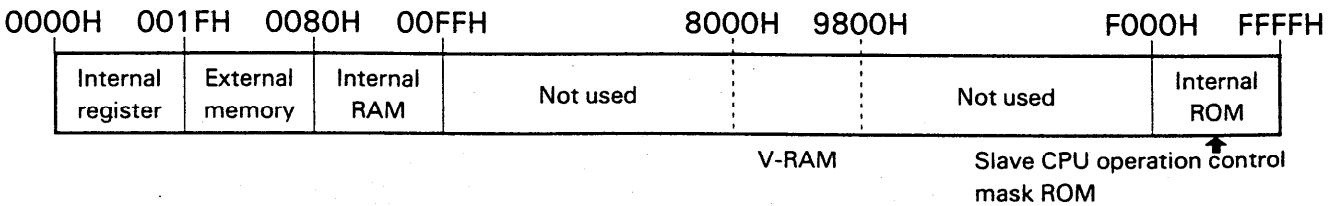
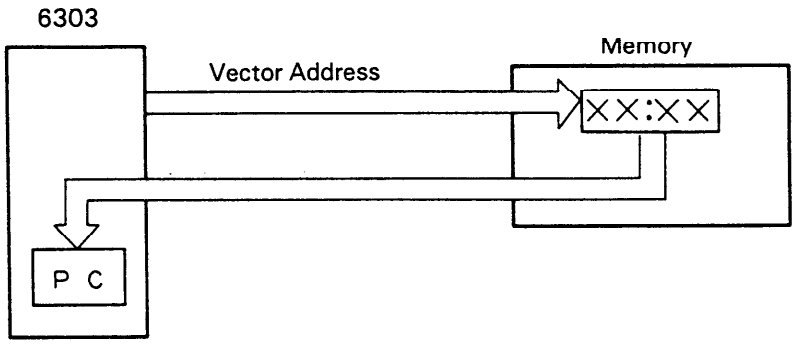


Fig. 2-41 Resultant Memory Mapping Example

Fig. 2-42 illustrates the vector address operation.

* Vector address – program counter



* The CPU stores the contents of the location addressed by the vector address in the program counter.

Fig. 2-42 Vector Address Operation

2.3.3.2 Internal Registers and External Memories

Tabel 2-8 lists the internal registers and external memory locations whitch are used as various control addresses.

Table 2-8 Internal Registers and External Momory Locations

	Address	Function	Read/ Write	Bit							
				7	6	5	4	3	2	1	0
6	0000	I/O port 1 data direction register		I/O Control For Address 0002							
	0001	I/O port 2 data direction register		I/O control for address 0003							
	0002	I/O port 1 port address		Speaker power supply	Speaker output	SERIAL POUT	SERIAL PIN	μMCT HSW	μMCT WE	μMCT ERAH	μMCT HMT
3	0003	I/O port 2 port address		—	—	—	SERIAL $\overline{PTX}$	SERIAL $\overline{PRX}$	—	μMCT WD	PRD
	0004	I/O port 3 data direction register		I/O control for address 0006							
0	0005	I/O port 4 data direction register		I/O control for address 0007							
	0006	I/O port 3 port address		Address (lower 8 bits)/data bus							
3	0007	I/O port 4 port address		Address bus (upper 8 bits)							
	0008	Timer control/status register									
	0009	Counter (upper 8 bits)		Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
	000A	Counter (lower 8 bits)		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	000B	Output compare register (upper 8 bits)		Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
	000C	Output compare register (lower 8 bits)		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

	Address	Function	Read/ Write	Bit 7	6	5	4	3	2	1	0
6303	000D	Input Capture register (upper 8 bits)		Bit15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
	000E	Input Capture register (lower 8 bits)		Bit 7	Bit 6	Bit5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	000F	Control/status register		FLAG	$\overline{\text{IRQ}}$ enable	—	OSS	LATCH enable	—	—	—
	0010	Baudrate/Mode Control register		—	—	—	—	Clock control		Baudrate control	
	0011	TX and RX control/status register		RDRF	ORFE	TDRE	RIE	RE	TIE	TE	WU
	0012	Receive data register		MSB							LSB
	0013	Transmit data register		MSB							LSB
	0014	RAM control register		Stand-by power	RAM enable	—	—	—	—	—	—
GAH40S	0020	Counter (upper byte) input	R	CNTR Count	—	—	Microcassette tape drive counter data Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Counter reset	W	—	—	—	—	—	—	—	—
	0021	Counter (lower byte)	R	Microcassette tape counter data Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit0
		Command register	W	$\overline{\text{STOP}}$ CNT	$\overline{\text{FAST}}$	—	MTC	MTB	MTA	SW MCT	SW PR
	0022	P-ROM address (upper 8 byte)	W	Upper P-ROM address bits Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
	0023	P-ROM address (lower 8 byte)	W	Upper P-ROM address bits Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		P-ROM read data	R	MSB							LSB
SED1320	0024	Controller instruction register	W								
	0025	Controller data buffer	R								
		Controller data buffer	W								
	0026	Controller status register	R								
		Port data output register (data)	W								
	0027	Port data input register	R								
		Port data output register (command)	W								SED 1320 ↓ 6303
	0028	Interrupt enable register	W								

GAH
40S

2.3.3.3 Slave CPU Interrupt

$\overline{INTR}$ is the only interrupt request signal to the slave CPU 6303; the $\overline{NMI}$ signal is not used. The slave CPU interrupt is discussed in the following:

Interrupt control

As shown in Fig. 2-43, the interrupt request signal is generated in SED1320 and fed to the slave CPU via GAH40S. This signal is used when the main CPU sends a command to the slave CPU via the PDIR register in SED1320 and is reset when the slave CPU reads the CSR register in SED1320.

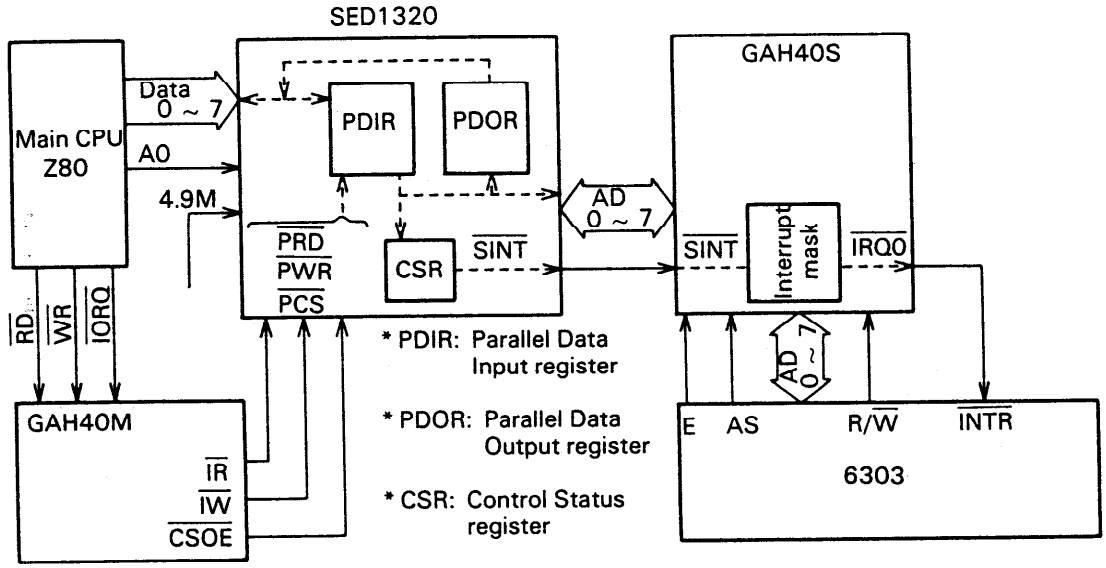


Fig. 2-43 Slave CPU Interrupt Control Block Diagram

The $\overline{INTR}$ signal is generated in SED1320 when the main CPU initiates a command, which is in turn fed to GAH40S. The signal then interrupts the slave CPU under an interrupt mask control by the slave CPU (the interrupt is disabled by bit 0 of 6303 address 0028 – enabled when the bit is 1). When interrupted, the slave CPU fetches the command by reading address 0027.

Slave CPU 6303 basic clock signal waveforms

(Top) EXTAL:
Measured at 13D, pin 3
(Center) E:
Measured at 13D, pin 40
(Bottom) AS:
Measured at 13D, pin 39

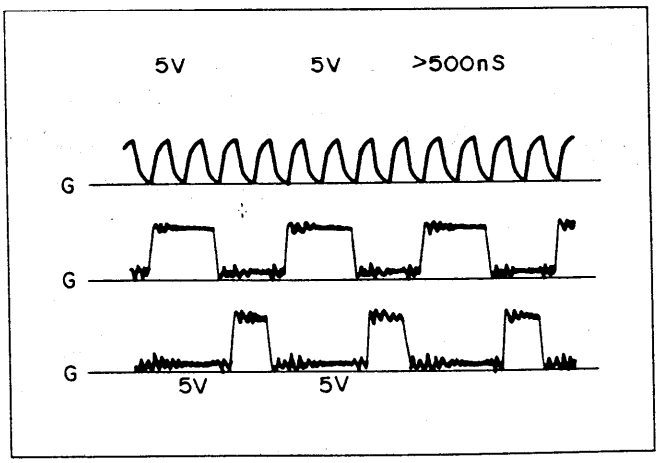


Fig. 2-44

2.3.4 Operations of the 7508 Sub-CPU

2.3.4.1 Operation During Power Off

During power off, the 7508 sub-CPU performs two important functions; it monitors pin 23 at port 00, checking for a change of state indicating the power switch has been turned on; it also monitors battery voltage every 10 seconds to assure that there is adequate power supply to maintain data in RAM and to provide backup power for the main battery.

- Battery voltage monitoring

  The sub-CPU 7508 enables port 23 (pin 5) every 10 seconds for a period of approximately 7.5 ms in order to supply the Vcc source to the A-D converter. If then turns on port 21, pin 3, (low) to put the A-D converter in the interface mode. One-byte serial data is then output with a series of eight shift clock pulses over the SI and SO signal lines respectively to select the A-D converter channel for battery voltage check (AN1). After channel selection data is issued, the 7508 returns port 21 from low to high to change the A-D converter mode from interface to A-D conversion. This causes the converter to initiate an A-D conversion through the specified channel. The converted result is stored in the shift register in the converter. After returning port 21 low (the interface mode), the 7508 issues shift clock pulses to read in the digital data, bit by bit. This data is examined to determine the main battery voltage. If the voltage is found to be below a certain level, the battery voltage line is backed up from the auxiliary battery by using a port 42.

2.3.4.2 Operation While Power Is On

While power is on, the 7508 sub-CPU performs the following functions:

- Keyboard Control – Controls the keyboard matrix using key scan signals (KSCO-8) and key return signals (KRTNO-7)
- DIP Switch (SW1) Monitoring – Checks DIP switch 1 during initialization using signals KSC9 and KRTN1-7.
- Battery Voltage Monitoring Support Functions – Includes such operations as main CPU interrupt via gate array GAH40M (Low voltage interrupt) and back-up power provision via the auxially battery.
- Analog Trigger Signal Detection – Detects a triggering signal in the analog input interface to control the A-D converter and read analog input data.

Observed Shift Clock Wave Forms

SCK:

Measured at 1D, pin 4

Figures 2-45 through 2-47 show the SCK signal waveforms which should be observed during a serial data transfer. Fig. 2-45 is an enlargement of the single negative going pulse shown in Fig. 2-47. Fig. 2-46 further enlarges one pulse in Fig. 2-44.

The three pulses shown in fig. 2-46 are used to allow the 7508 to perform the following operations, in order from left to right:

1) Fetch the command stored in the gate array GAH40M to 7508.
2) Select the μPD7008 channel.
3) Read the A-D converted data from μPD7001.

Note: Fig. 2-46 and 2-47 are enlargements of the signal shown in Fig. 2-45.

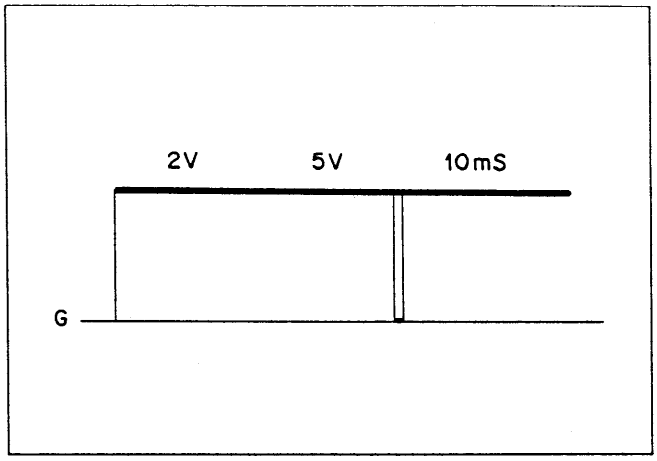


Fig. 2-45 SCK Signal Waveform (Serial Data Trans for) Enlargement

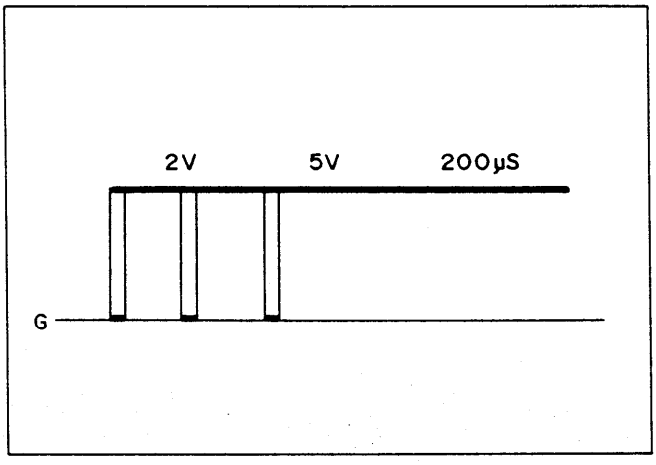


Fig. 2-46 SCK Waveform Pulse Enlargement 2 (Serial Data Transfer)

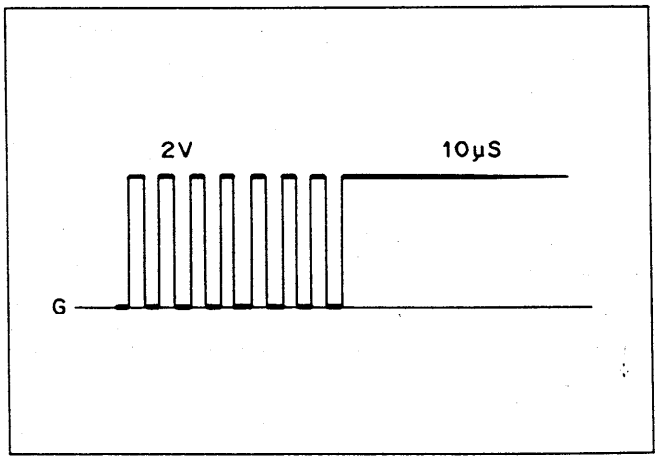


Fig. 2-47 SCK Signal Waveforms During Serial Data Transfer

2.4 Clock Generator Circuit

There are three clock oscillator circuits listed in Table 2-9 on the MAPLE board. Two clock pulse signals of these three are fed to the IC 6A, which divides and distributes them to the LSIs listed in the table. The remaining signal is generated by a CR oscillator circuit and used as the switching signal for the DC-DC converters which generate special voltages.

Table 2-9 Clock Oscillator Circuits

Oscillator Circuit	Primary Frequency	Output Frequency and Signal Destination
Main oscillator circuit (CR1)	9.8304 MHz	4.9 MHz → 7C
Clock oscillator circuit (CR2)	32.768 kHz	1.0 kHz → 2E
Voltage regulator oscillator circuit	35 kHz	35 kHz → RS-232C, (± 8V) → LCD regulator (−15V) 5V regulator (+5V)

2.4.1. CR1 Oscillator Circuit

The CR1 oscillator circuit starts functioning when power is turned on. The output is amplified by IC 7B and is then fed to IC 6A. This IC consists of two frequency divider circuits and the primary frequency is halved and quartered to produce two clock signals of 4.9 MHz and 2.45 MHz.

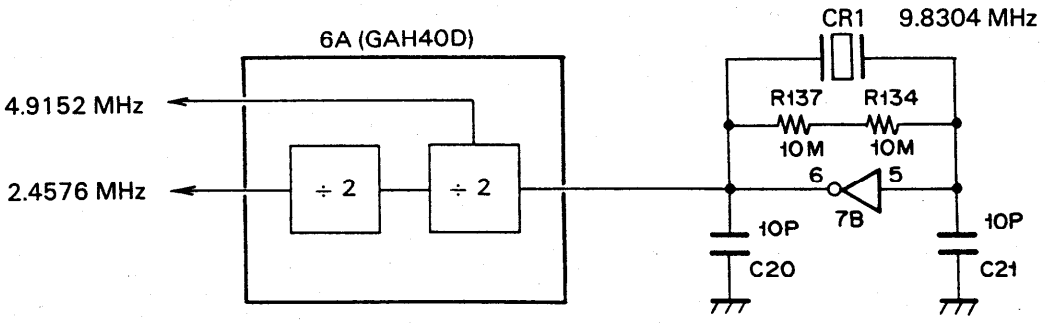


Fig. 2-48 CR1 Oscillator Circuit

The primary and divided frequency output signal waveforms are as shown in Fig. 2-49.
The 2.45 MHz clock signal is supplied to the main CPU (4A), gate array GAH40M (4A), and serial controller (2C), and used as their basic clocks.

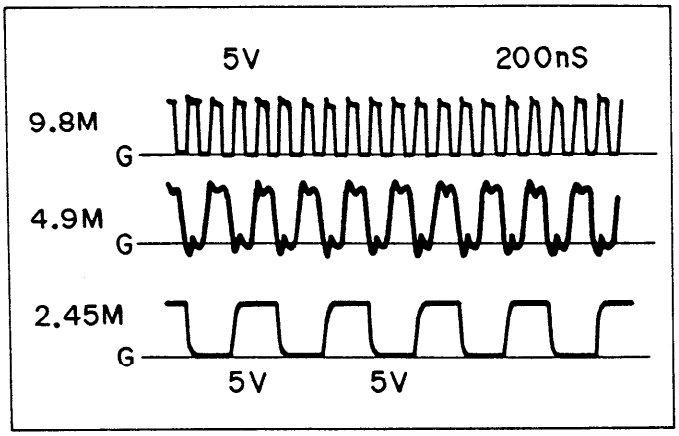


Fig. 2-49 CR1 Clock Signal Waveforms

The 4.9 MHz clock signal is supplied to the LCD controller (7C) and used as the basic clock signal for LCD display control. This signal is further halved within the controller. The output clock signal of 2.45 MHz is fed to the external clock signal input terminal (EXTAL) of the 6303 slave CPU. Thus, the signal is quartered within the slave CPU to a clock signal of 614 kHz and used as its operation clock signal.

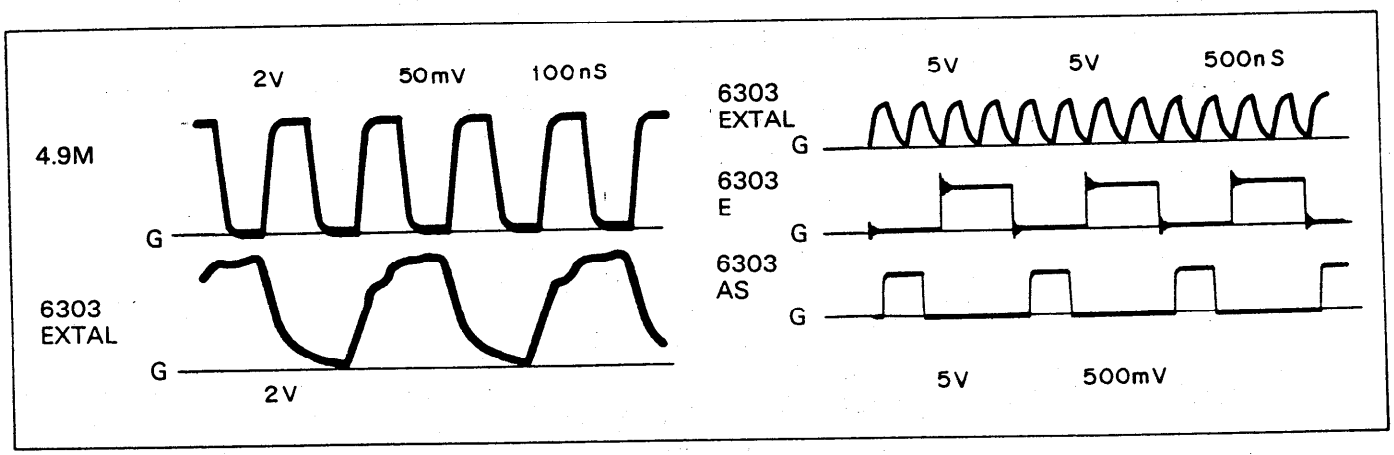


Fig. 2-50 LCD Controller and Slave CPU Operation Clock Signal Waveforms

2.4.2 CR2 Oscillator Circuit

The output of the 32.768 kHz crystal oscillator is used as the counting signal for the built-in clock and as the D-RAM refreshing timing pulse. Thus, the oscillator circuit is always backed up by the battery (from the VB line) to ensure the 32.768 kHz clock signal to be supplied to IC 6A (GAH40D), regardless whether power is on or off.

Fig. 2-51 is a circuit diagram of the CR2 oscillator circuit.

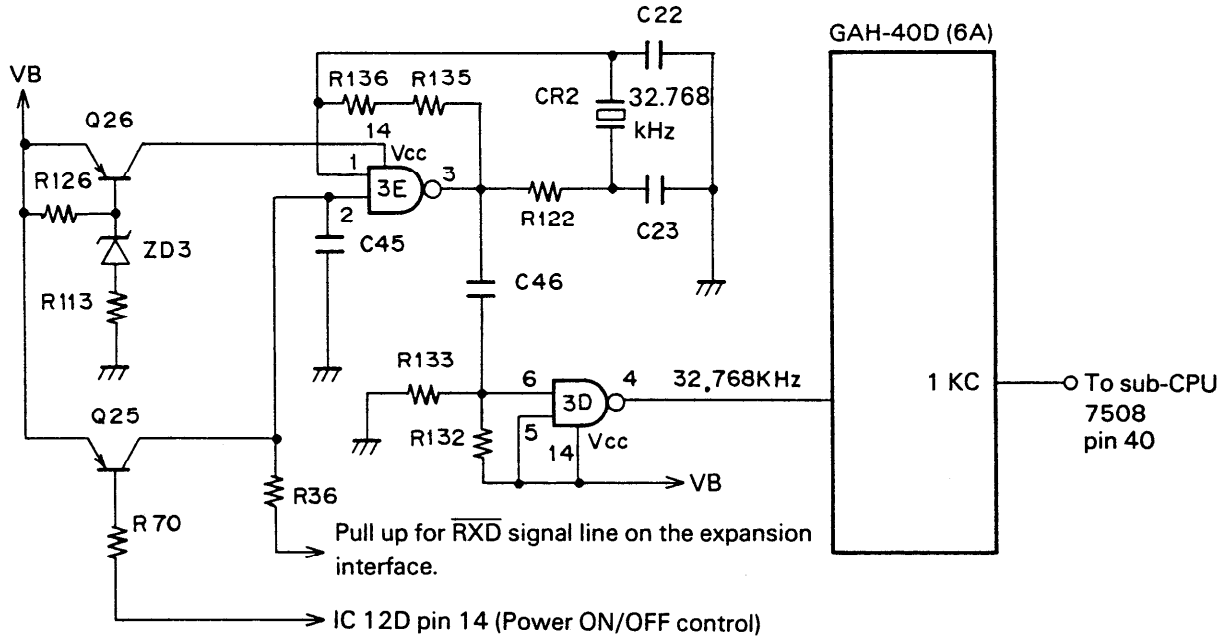


Fig. 2-51 CR2 Oscillator Circuit

The signal waveforms at various points should be observed as shown in Fig. 2-52.

* The 1 kHz output to the 7508 (pin 51 of GAH40D) is available while power is off.

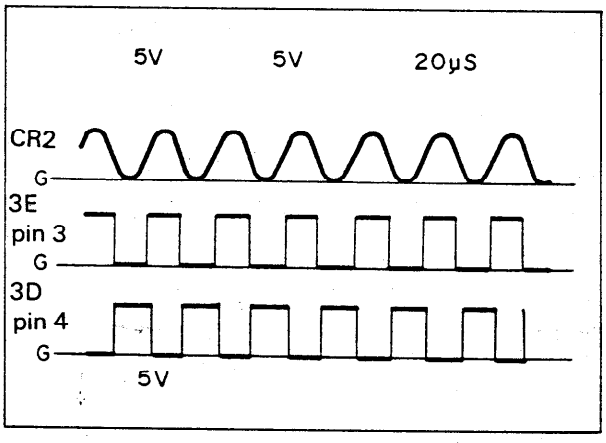


Fig. 2-52

Circuit operations

< While power is on >

While power is on, port 70 of the 4-bit sub-CPU is held low. This low signal is fed to the base of transistor Q25 after being inverted twice by ICs 3E and 12D, maintaining the transistor in conduction. This causes Vcc to be supplied to IC 3E, enabling it to oscillate.

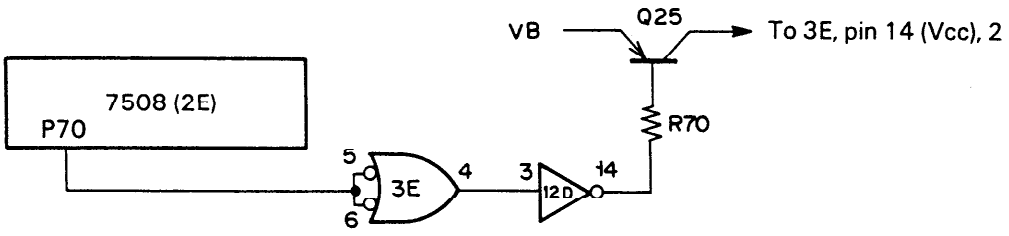


Fig. 2-53 CR2 Oscillation Control

< While power is off >

While power is off, the backup voltage VB is supplied to the collector of the transistor Q26, as well as to the base through the resistor R126. A zener diode, ZD3, is inserted across the base of Q26 and ground. ZD3 has a zener breakdown voltage of 4V and breaks down when the base potential rises towards the VB (+5V) voltage beyond 4V. The zener breakdown is removed when the base potential falls below 4V. An infinite repetition of this alternation causes Q26 to continue switching on and off, outputting a voltage of approximately 4V at the emitter. This output is connected to the same line as the collector of transistor Q25 and causes Vcc to be supplied to IC 3E, ensuring the same oscillation as when power is on.

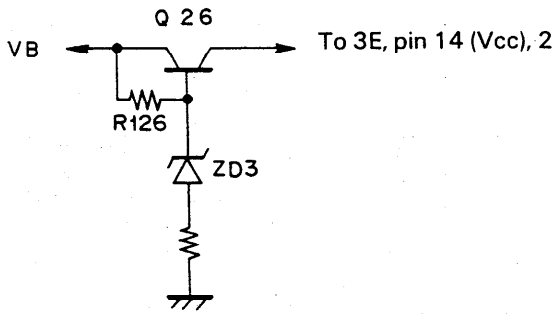


Fig. 2-54

2.4.3 Voltage Regulator Oscillator Circuit

This circuit is a CR oscillator circuit, consisting of the resistor R90 (68 kohms) and the capacitor C26 (220 pF), oscillates at a frequency of approximately 35 kHz. The output is amplified by IC 14D and supplied to the following three circuits:

a. RS-232C DC-DC converter circuit
b. LCD DC-DC converter circuit
c. ROM capsule biasing circuit

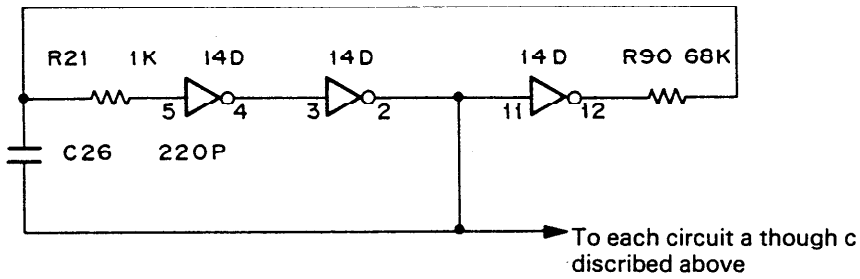


Fig. 2-55 Voltage Regulator Oscillator Circuit

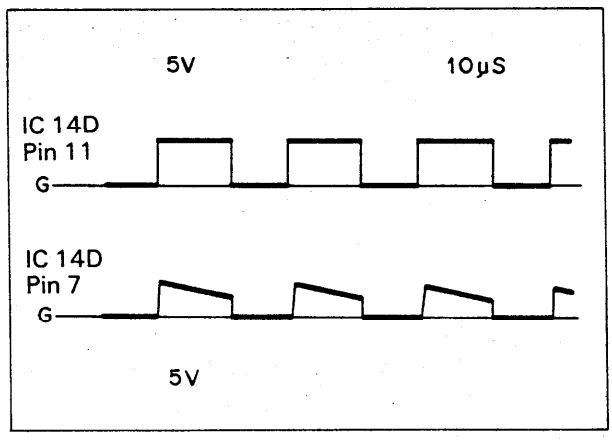


Fig. 2-56

2.4.4 Other Oscillator Circuits

Sub-CPU 7508 and A/D converter have own CR oscillator by using the external components. Sub-CPU clock is adjustable with VR3.

2.4.4.1 Sub-CPU 7508 Clock Signal Oscillator Circuit

This circuit oscillates at a frequency of approximately 200 kHz, using an external capacitor and the variable resistor VR3.

The output signal waveforms should be observed at the indicated points as in Fig. 2-57.

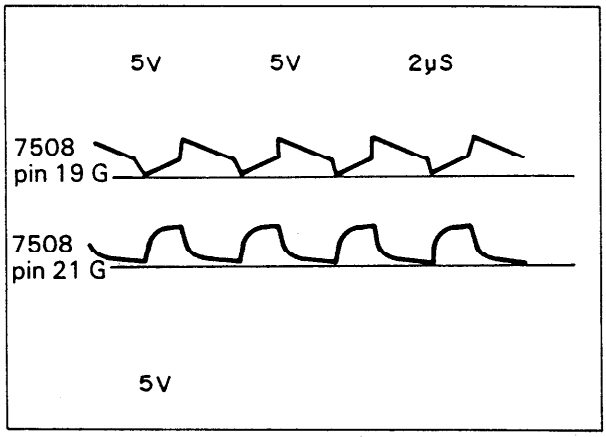


Fig. 2-57 7508 Clock Signal Oscillator Circuit Output Signal Waveforms

2.4.4.2 A-D Converter Clock Signal Oscillator.

This circuit oscillates at a frequency of approximately 480 kHz using an external capacitor and resistor. The signal waveforms at the indicated points should be observd as shown in Fig. 2-58.

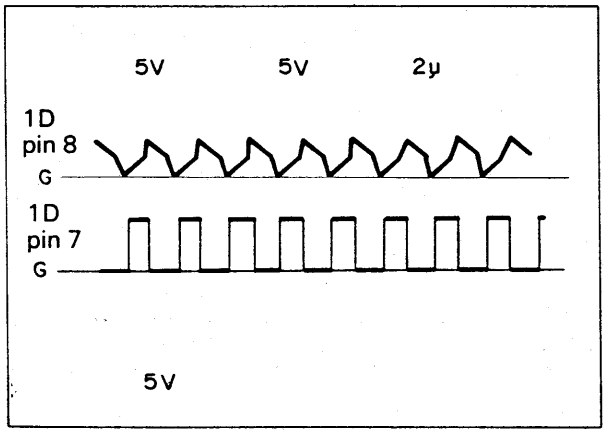


Fig. 2-58 A-D Converter Clock Signal Oscillator Waveforms

○ Figures 2-59 and 2-60 show the timing relationship among major clock signals.

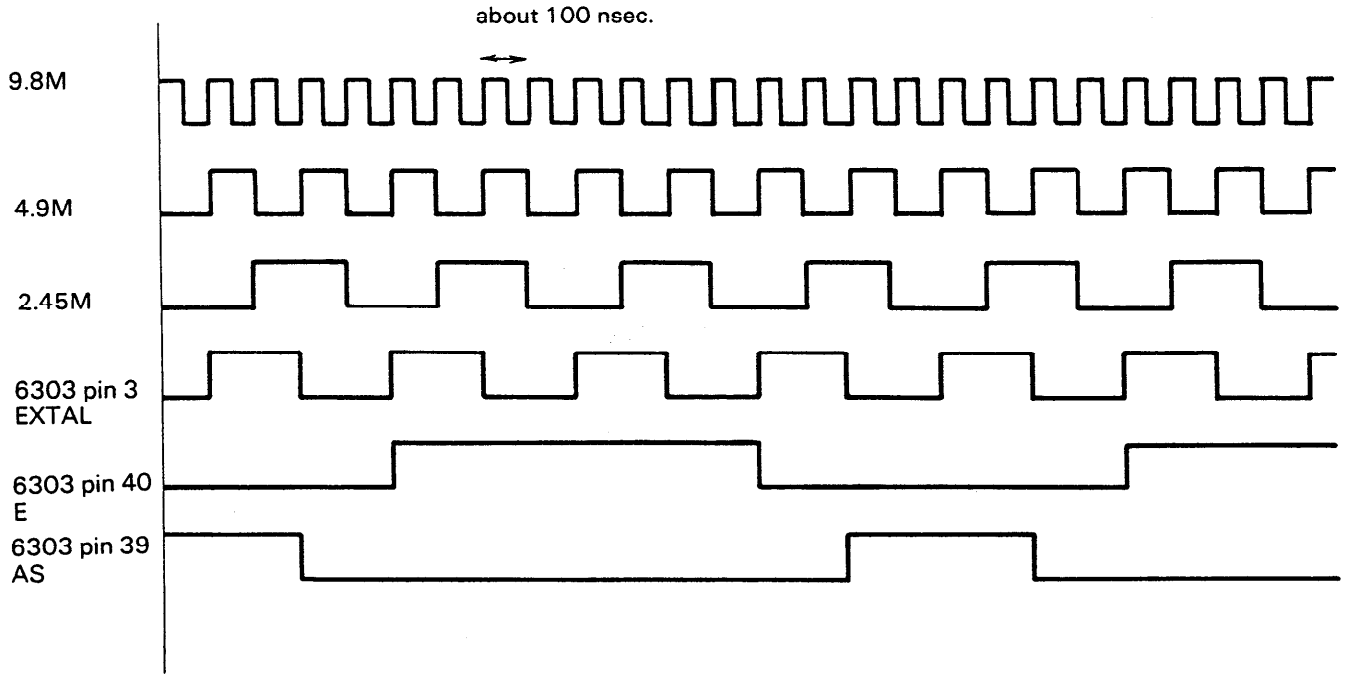


Fig. 2-59

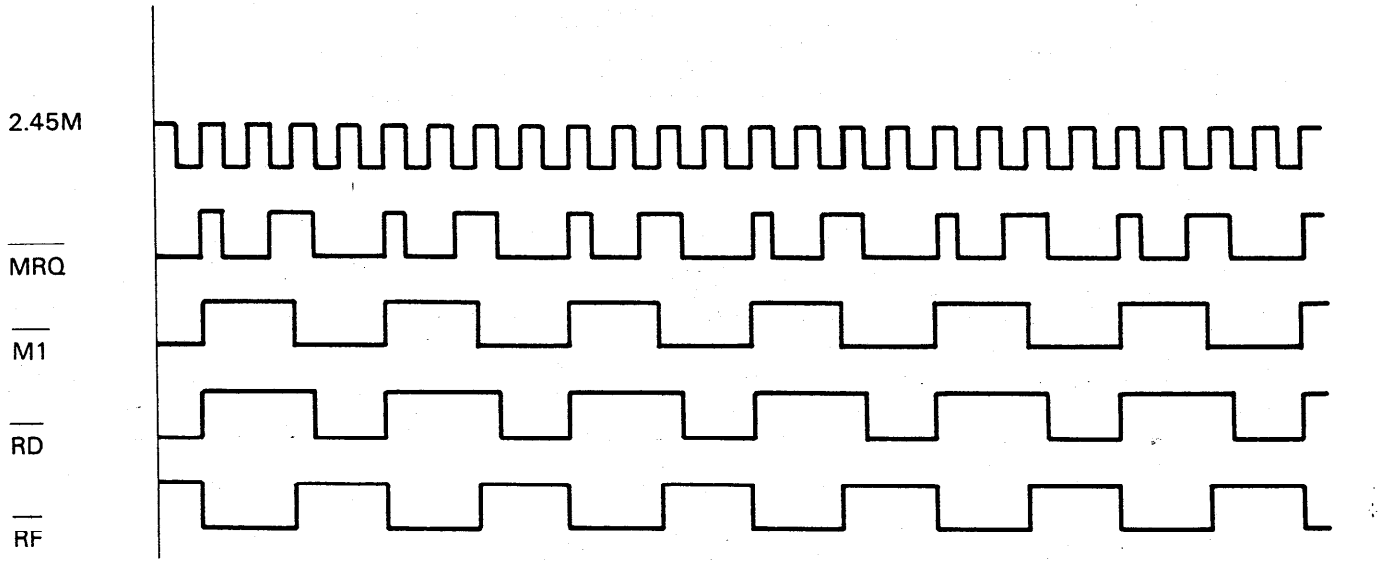


Fig. 2-60

2.5 Jumper and Switch Setting

All the jumpers and switches including a DIP switch mounted on the MAPLE board are listed in Table 2-10 together with their summarized functions.

Table 2-10 Jumper And Switch Settings

Name		Standard Setting	Circuit Drawing Coordination	Associated Signal/Function
J1		T/N	A-2	$\overline{\text{HLTA}}$: Open – Specifies Toshiba unit. Closed – Specifies NEC unit.
J2		OFF	A-6	OVERCHARGE: Open – Controls overcharge protection.
J3		OFF	C-7	TEST: Closed – Operates sub-CPU 7508 in test mode.
J4		ON	D-7	Analog Input pull-up: Closed – pulls up ANIN input line to VB through a 100 kohm resistor.
J5		**A/B	E-6/7	LP pulse hold: A – Holds 8 LP pulses. B – Provides no LP pulse holding.
SW1		OFF	C-7	Power switch
SW2		*N/O	C-7	Reset switch (main frame system rest)
SW3		ON	A-7	Auxiliary battery switch: ON – Enables backup from auxiliary battery.
SW4	1	–	C-7	Used to keyboard models.
	2	–		
	3	–		
	4	–		
	5	–		
	6	–		
	7	–		
	8	–		
SW5	A	*N/O	A-4/5	Ensures initialization during backed-up operation.
	B	*N/O	D-6	Initial reset: Sub-CPU 7508 reset

Notes:

* A push switch containing two sets of contacts.

* * A or B is selected depending on the used LCD.

Jumpers and Switches

Fig. 2-61 shows the locations of the jumpers and switches used on the MAPLE board and illustrates their setting positions (ON/OFF, A/B, etc.).

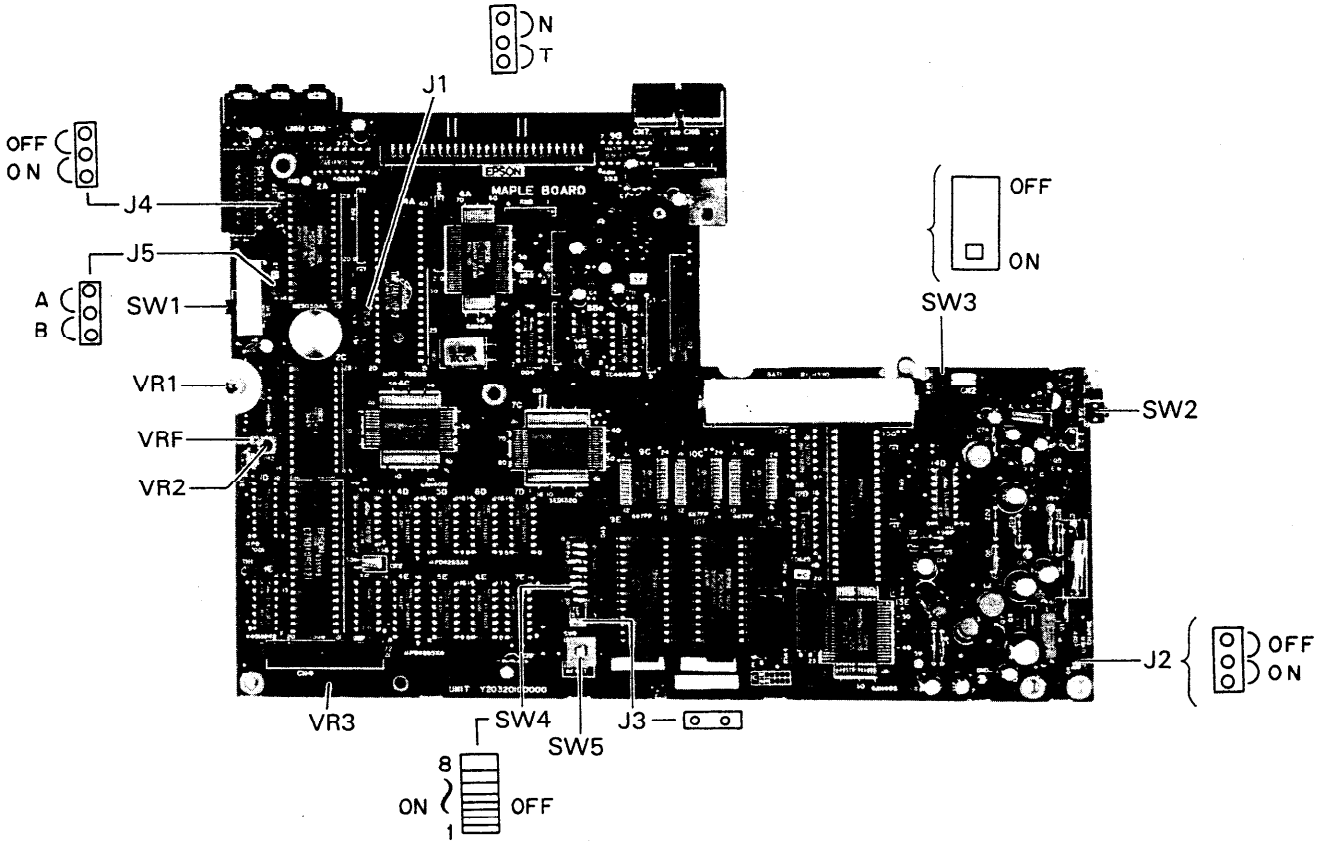


Fig. 2-61 MAPLE Board Jumpers and Switches

2.5.1 Jumpers

The functions of the individual jumpers are detailed in the following (see Table 2-10 for a summary of their functions).

2.5.1.1 J1

This jumper is provided in order to permituse of either of two available main CPU types. (The main CPU is located at 4A on the MAPLE board.) One of two terminals may be selected, T and N terminals, respectively, disable and enable the $\overline{\text{HLTA}}$ signal line, reconciling the difference in Line control between the two types of main CPUs. (The line relates to the DRAM refresh.)

T – Terminal T is selected when a TOSHIBA CPU (parts No. X400084005) is used. When the T and center terminals are jumpered, the main CPU output signal, $\overline{\text{HLTA}}$, is disabled. (The terminal is open; i.e., not connected to any other terminal.)

N – Terminal N is selected when a NEC CPU (parts No. X400070008) is used.

* Caution: Examine the main CPU type before setting this jumper.

2.5.1.2 J2

This jumper is provided to allow for protection against main battery overcharge. When the ON and center terminals are jumpered, the control by the sub-CPU 7508 is disabled, forcing a normal (high current) charge to be maintained as long as the ac adaptor is connected. This setting may result in an overcharge condition of the main battery, which may shorten its life.

2.5.1.3 J3

J3 is a maintenance purpose jumper used for testing the sub-CPU 7508. To open (set off) this jumper, put the jumper block as shown in Fig. 2-62; leaving one terminal pin open. OFF is the standard setting. The ON setting disables the normal sub-CPU operation.

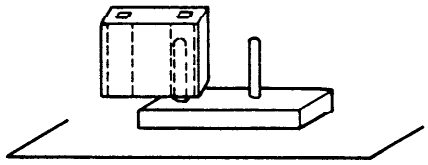


Fig. 2-62

2.5.1.4 J4

Jumper J4 allows for pull-up of the analog input (ANIN) signal input. Because the ANIN signal input voltage ranges from 0 to +2.0V, the jumper may need to be reset depending on the connected analog device.

2.5.1.5 J5

Jumper J5 is used to eliminate vertical ghost display lines which may appear due to the characteristics of the LCD unit. Its setting depends on the installed LCD unit (or the LCD panel, to be precise). J5 may need to be reset when the LCD unit is replaced so that ghosts, if observed, are eliminated.

2.5.2 Switches

Five switches are mounted on the MAPLE board as shown in Fig. 2-61. Their functions are detailed in the following.

2.5.2.1 SW1

This switch is used to turn the computer on and off. It is connected to a port of the sub-CPU 7508 which controls power on/off by sensing a setting change of this switch. Thus, it may be ineffective when the sub-CPU loeses the normal power-on/off sequence control capability because the computer can, through a programming error, got into a software loop.

2.5.2.2 SW2

This is the RESET switch which is accessible at the left side of the computer. It is connected to another port of the sub-CPU. The switch causes all of the computer sections except for the sub-CPU to be initialized, it is ineffective when the sub-CPU is not operating normally.

2.5.2.3 SW3

This switch allows the user to enable or disable the charging and discharging circuits for the auxiliary battery, soldered on the MAPLE board. It is provided in order to prevent complete auxiliary battery discharge and thereby protect the battery from deterioration when the PX-8 unit is stored unused for a long period of time. The switch must be set ON whenever the board is in service, otherwise, the normal backup operation would not be in effect. After a low voltage condition is detected, the Ni-Cd battery life is shortened if left completely discharged.

2.5.2.4 SW4

This DIP switch assembly is used to select an international character set. The individual switches are read only when the system is initialized to allow the computer to operate on the selected character set. Table 2-11 shows the available character sets and the corresponding SW4 settings.

Table 2-11 Character Set Selection SW4 Setting

Setting / Character set	SW4							
	1	2	3	4	5	6	7	8
ASCII	1	1	1	1	0	1	0	0
French	0	1	1	1	0	1	0	0
German	1	0	1	1	0	1	0	0
English	0	0	1	1	0	1	0	0
Danish	1	1	0	1	0	1	0	0
Swedish	0	1	0	1	0	1	0	0
Norwegian	0	1	1	0	0	1	0	0
Italy	1	0	0	1	0	1	0	0
Spain	0	0	0	1	0	1	0	0
HASCI	0	0	0	0	0	1	1	0
Japanese (Japanese)	1	0	0	0	0	1	0	0
Japanese (JIS)	0	0	0	0	0	0	0	0
Japanese (touch 16)	1	0	0	0	0	0	0	0

Note: 1 indicates that the switch is closed and 0 indicates that the switch is open.

- SW4-5 is used to check whether the RAM disk contents of the RAM unit are correct:
  ON: The check is made when power is turned ON in the Restart mode.
  OFF: No check is made.
- SW4-6 is used to select the charactor generator set for screen dump.
- A system initialization can be accomplished in either of the following two ways:
  1. Remove the ROM cartridge cover and press the INITIAL RESET switch (SW5).
  2. Press the RESET switch while holding the SHIFT and GRPH keys down:

2.5.2.5 SW5

SW5 is the Initial Reset switch which is used to initialize the entire computer including the sub-CPU 7508. Normally, it is pressed when the system is first initialized and a message, "SYSTEM INITIALIZE", is displayed on the LCD panel. This switch must also be pressed, however, when the computer gets into a software loop or the sub-CPU stops operating for the same some reason and, SW2 is ineffective.

The switch is an alternate singal-pole, double-throw type (containing contacts A and B). One contact is connected to the reset (RS) input terminal of the sub-CPU for initializing it. The other one (A4/5 in the circuit diagram) is inserted between the backup line power line from the auxiliary battery and the logic circuit voltage supply line. When the switch is pressed and this contact is closed, the backup voltage, which is normally supplied through the transistor Q23, is directly fed to the logic circuit voltage supply line, bypassing the transistor. This is required to slightly raise the logic circuit supply voltage in order to ensure computer reinitialization in an abnormal condition. A hardware failure may have occurred if SW5 needs to be pressed.

2.5.3 Variable Resistors

Three variable resistors are located on the MAPLE board as shown in Fig. 2-61 and one each on the LCD unit (MAP-LD board) and the microcassette tape drive (MAP-MC board), totalling five. The functions of the individual variable resistors are detailed in the following.

2.5.3.1 MAPLE Board Variable Resistors

Table 2-12 lists the three variable resistors used on the MAPLE board together with their functions.

Table 2-12 MAPLE Board Variable Resistors and Their Functions

Name	Function
VR1 (Circuit diagram coordination H7)	This variable resistor is used to control the output sound level to the built-in and external (if used) speakers.
VR2 ((Circuit diagram coordination D5)	Allows the user to adjust the reference voltage to the A-D converter (1D). An incorrect adjustment of this reference voltage may result in an error in voltage detection and A-D conversion of the barcode reader or external analog input signal by the sub-CPU.
VR3 (Circuit diagram coordination C6/7)	Allows the user to adjust the frequency of the sub-CPU driving clock signal.

2.5.3.2 MAP-LD Board Variable Resistor

This is the variable resistor VR1, found at coordination C6/7 on the circuit diagram, which allows the user to adjust the voltage supplied to the LCD drivers for the optimum liquid crystal twisting. (This adjustment affects the view angle.) It is provided in order to compensate for change in liquid crystal reaction depending on temperature.

2.5.3.3 MAP-MC Board Variable Resistor

This is the variable resistor, located at coordination E2 on the circuit diagram, which allows the user to adjust the microcassette tape speed. An incorrect adjustment of this variable resistor causes the intervals between tape read and write data pulses to deviate from the nominal value, resulting in loss of compatibility with other microcassette tape drives.

2.6 Reset

The reset signal initializes the computer circuit and is used to prevent any abnormal operation at power on (during the logic circuit power voltage rise time), after emergency shut-down due to any computer abnormality, and before subsequent restart. The resetting operation of this computer is accomplished indirectly by software. The sub-CPU internal program differs from other computers, which are reset directly by a switch operation.

Fig. 2-63 outlines the RESET signal circuits.

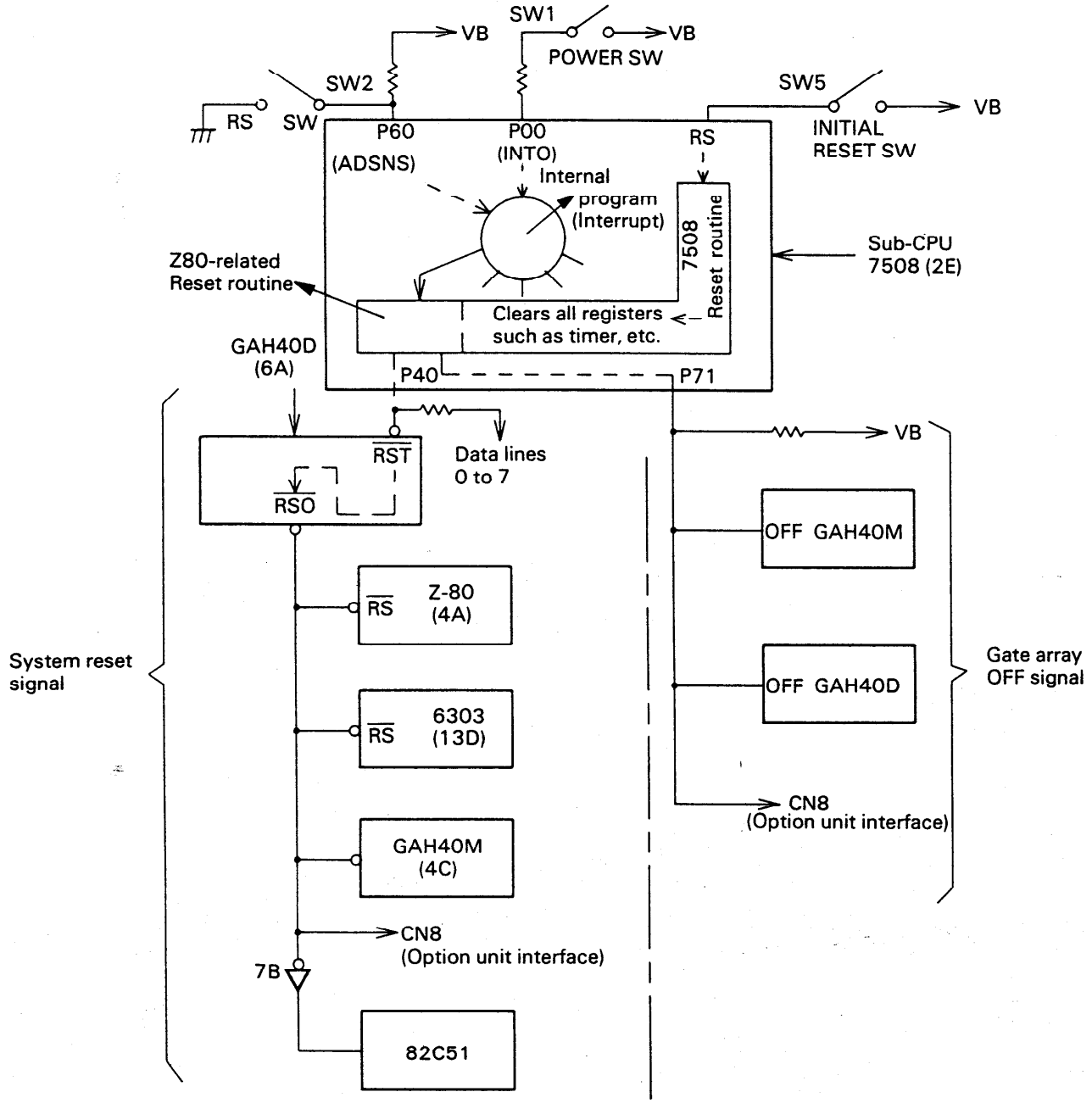


Fig. 2-63 Reset Signal Circuit Block Diagram

2.6.1 Resetting By SW1 (POWER) and SW2 (RESET)

To use either switch SW1 (POWER) or SW2 (RESET or the RS signal on the circuit diagram), it is requisite that the sub-CPU 7508 be operating normally . When either switch is pressed, the sub-CPU accepts the signal as an interrupt and turns its port 40 low. This signal is fed to the $\overline{RST}$ terminal of the gate array, GAH40D (6A), and is output from the $\overline{RSO}$ terminal, resetting the main CPU and the slave CPU, etc.

2.6.2 Resetting By SW5 (INITIAL RESET)

Switch SW5 allows the sub-CPU itself to be reset. It initializes the sub-CPU's internal settings, including the built-in calender clock setting, etc. This is the only difference between the reset from switchs and the reset by switches SW1 and SW2.

2.6.3 OFF Signal

The OFF signal is provided in association with computer resetting in order to prevent inconveniences such as latch of flipflops in the gate arrays, etc. It provides the gate arrays with the following functions:

< GAH40D >

Supplies the reset signal to Z80 and 6303, etc.
Disables the Chip Select signal to the IPL ROM.
Disables the Z80 read signal line.
Disables the interrupt signal line to Z80.
Resets all FFs.
Disables all outputs other than the above.

< GAH40M >

Prevents latching of the gate array FFs by forcing the outputs in the high impedance state.

2.7 Keyboard

The keyboard has 72 keys (including function key switches), three light emitting diodes (LEDs), 23 diodes, and three resistors for the LEDs mounted on it. The keyboard is structured in a matrix which is scanned by the sub-CPU 7508. Keyed in data are sent to the main CPU Z80 from the cub-CPU via the gate array GAH40M. In preparation for a situation where the normal keyed-in data transfer to the main CPU is hampered, the sub-CPU incorporates a 7-character key data buffer. Fig. 2-64 is a block diagram illustrating the keyboard input operation.

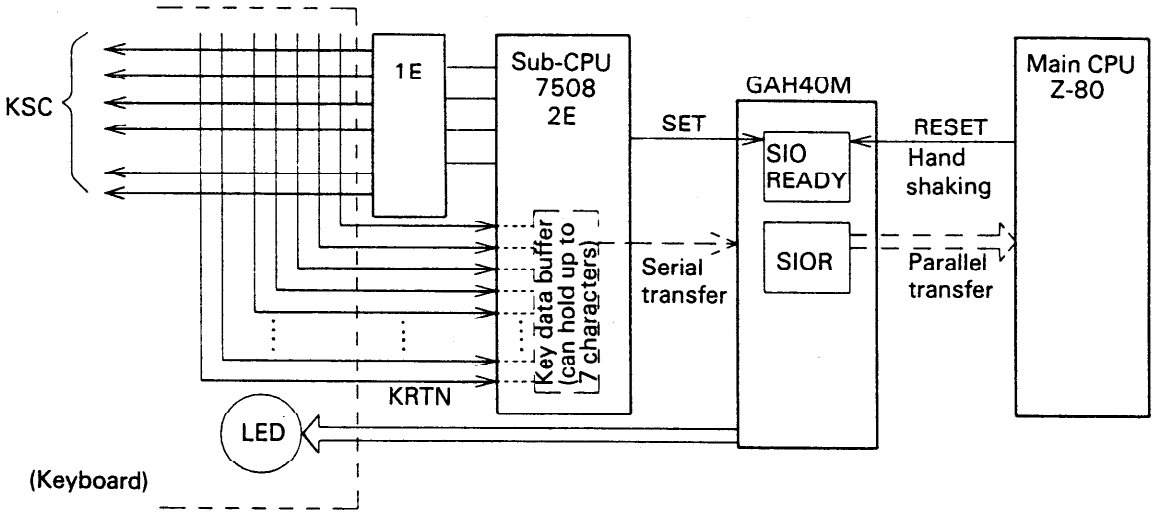


Fig. 2-64 Keyboard Input Operation Block Diagram

The keyboard keys are scanned by the sub-CPU which controls the key data outputs as follows:

(1) Key switch (CTRL, SHIFT(R), SHIFT(L), CAPS LOCK, NUM GRPH, and CTRL (right of the space-bar) output control

When any of these keys is pressed for the first time (i.e., it is stet), the sub-CPU issues a MAKE code. When it is pressed for the second time (i.e., it is released), the sub-CPU issues a BREAK code. This is required for the correct keyboard data input, because the keyboard input mode is controlled by these keys and the main CPU has to be informed whether any one of them is in effect. Fig. 2-65 illustrates a sample sequence of key strokes, which includes shift operations in the alphanumeric mode: The sub-CPU issues the MAKE and BREAK codes for the left SHFT key when it is locked and released respectively. The main CPU can display the intended upper case and lower case alphabets as shown below.

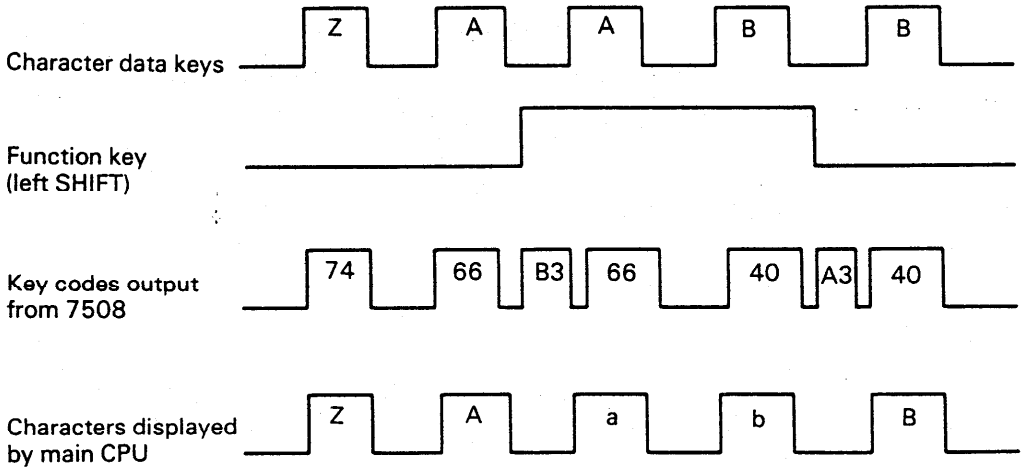


Fig. 2-65 Keyboard Data Input And Mode Control Sample

(2) Data keys (other than the function keys)

Each data key issues the corresponding KEY code shown in Table 2-13 only once, when it is pressed. When any key other than a function key depressed, its character code is repeatedly generated by the sub-CPU provided that a feature called Auto Repeat is enabled. This feature is enabled or disabled and the frequency of repetition is selected by software.

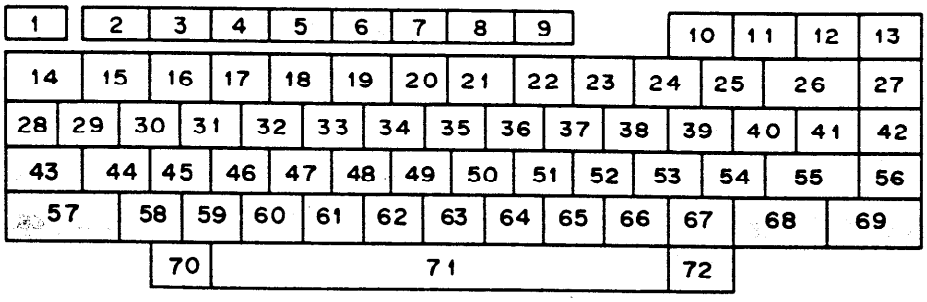


Table 2-13

Upper Code Byte / Lower Code Byte	0	1	2	3	4	5	6	7	8	9	A	B
0	2	1	29	46	62	21	37	54	12			
1	3	14	30	47	63	22	38	55	13			
2	4	15	31	48	64	23	39	56			OFF 43	ON 43
3	5	16	32	49	65	24	40	71			OFF 57	ON 57
4	6	17	33	50	66	25	41	58			OFF 70	ON 70
5	7	18	34	51	67	26	42	59			OFF 72	ON 72
6	8	19	35	52	10	27	44	60			OFF 68	ON 68
7	9	20	36	53	11	28	45	61			OFF 69	ON 69
8												
9												

2.7.1 Key Switch Structure

A key switch made up of a key top and a switch as shown in Fig. 2-66. (A dust-proof switch cover is inserted between the key top and switch of a function key.)

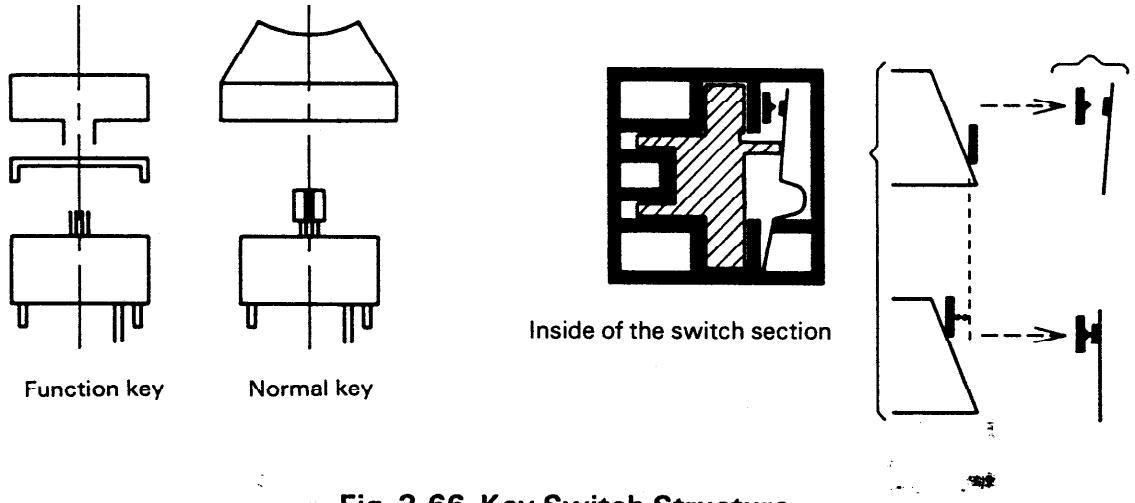


Fig. 2-66 Key Switch Structure

The switch uses a pair of mechanical contacts. The spring contact moves left and right to make and break contact according to the vertical stroke of the key stem. Fig. 2-67 illustrates the relationship between make and break of the switch contacts and key stroke. The space, shift, and retorn keys have a press load of approximately 95g, while the rest have that of approximately 65g.

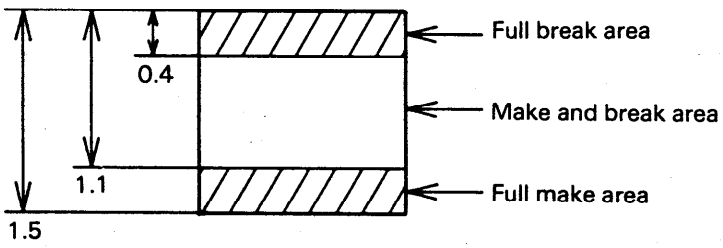


Fig. 2-67 Key Stroke And Switch Action

2.7.2 Key Signal Input

The keyboard has a 9 x 8 matrix structure which uses nine keyboard scan (KSC) signals and eight keyboard return (KRTN) signals. The scan signals are used as a reference and a pressed key is identified by examining the corresponding return signal lines for make.

Key input is controlled by the 4-bit sub CPU 7508 which is programmed to read, when the computer is initialized, the setting of the DIP SW2 assembly, as well as the key switches. The read key data and the SW2 setting are bit-serially transferred to the IC 4C (GAH40M), where the data are converted from serial to parallel, and further transferred to the main CPU. Fig. 2-68 is a block diagram of the keyboard matrix.

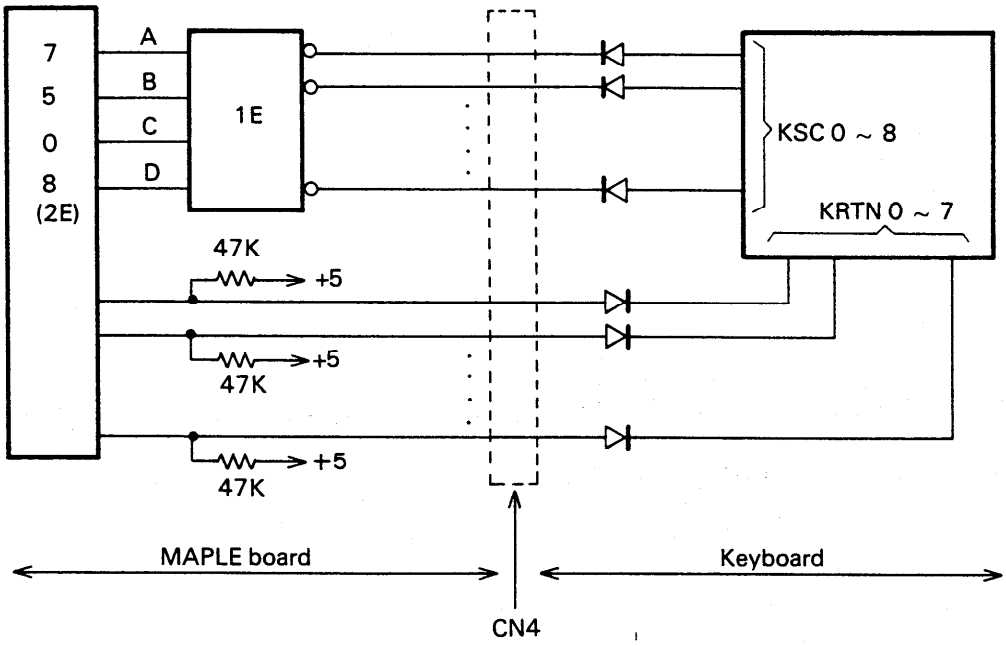


Fig. 2-68 Keyboard Matrix

Normally, IC 1E maintains all the KSC signal lines at the low level. Pressing a key causes a current to flow from the corresponding KRTN signal line on the MAPLE board to the IC through the diodes, pulling the KRTN signal line low. 7508 can detect that a key is pressed from the level change of the KRTN signal line. However, it cannot identify the pressed key which turned the line low. To accomplish this identification, the 7508 monitors the KRTN signal line while outputting pulses over the KSC signal lines as shown in Fig. 2-69. By examining both the KRTN signal line turning low and the KSC signal line, over which a negative going pulse is currently output, the 7508 is able to identify which key has been depressed.

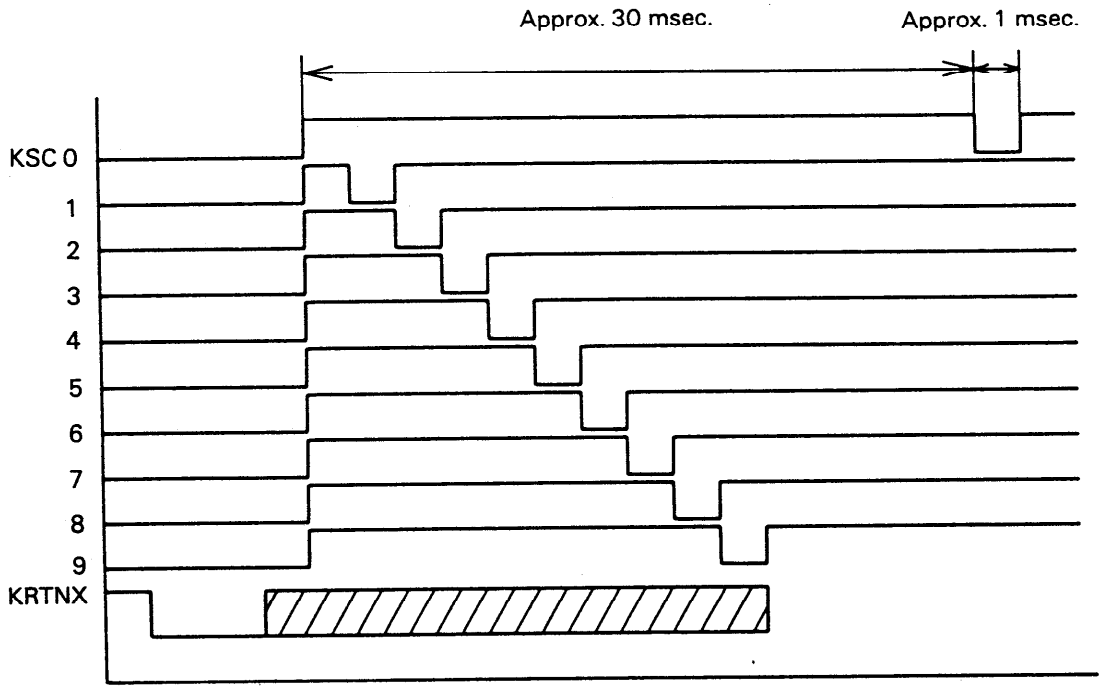


Fig. 2-69 KSC Line Pulse Signals

The KSC signals are controlled by the sub-CPU and the decoder IC 1E, as shown in Table 2-14.

Table 2-14

Input (1E)				Output									
A	B	C	D	0	1	2	3	4	5	6	7	8	9
L	L	L	L	**L**	H	H	H	H	H	H	H	H	H
H	L	L	L	H	**L**	H	H	H	H	H	H	H	H
L	H	L	L	H	H	**L**	H	H	H	H	H	H	H
H	H	L	L	H	H	H	**L**	H	H	H	H	H	H
L	L	H	L	H	H	H	H	**L**	H	H	H	H	H
H	L	H	L	H	H	H	H	H	**L**	H	H	H	H
L	H	H	L	H	H	H	H	H	H	**L**	H	H	H
H	H	H	L	H	H	H	H	H	H	H	**L**	H	H
L	L	L	H	H	H	H	H	H	H	H	H	**L**	H
H	L	L	H	H	H	H	H	H	H	H	H	H	**L**

The 7508 provides signals from ports 30 through 33 as shown in Fig. 2-70. The IC 1E generates the KSC pulse signals KSCO through KSC8 according to Table 2-14.

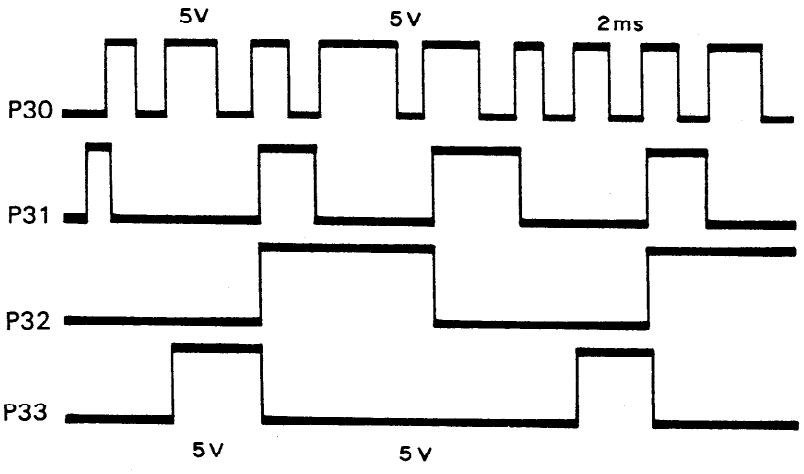


Fig. 2-70

< DIP Switch Assembly SW4 Setting Detection >

This switch assembly forms a matrix of the KSC8 line and the KRTN lines KRTNO through KTRN7 as shown in Fig. 2-71. Thus, its setting can be read in the same way as a normal key switch.

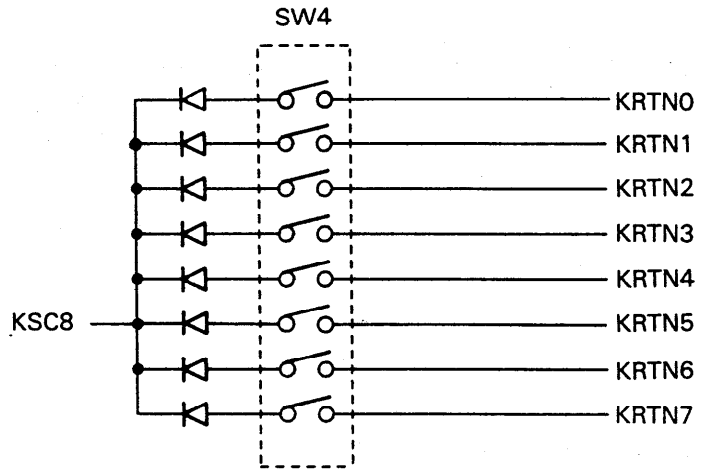


Fig. 2-71 SW4 Matrix

2.7.3 Key Input Control

When two or more keys are simultaneously pressed, keyboards which use a matrix structure such as described above may not be able to identify any of the pressed keys. To remove this inconvenience, the 7508 is programmed such that, when two or more keys are simultaneously pressed during one scan cycle (approximately 10 ms), the key operation is determined to be an error and no key input is accepted until only a single key is pressed. Assume for example that the keys A, B, and C in Fig. 2-72 are simultaneously pressed. The KSC1 signal will pull both the KRTN1 and KRTN6 lines low it and will not be able to be determined which is pressed. The KRTN1 line goes low when the KSC1 line is activated (low) because the two lines are connected via the A contacts. The KRTN6 line is pulled low during the KSC1 time because the pulse signal is routed to the KRTN6 line through A contacts, KRTN1 line, B contacts, KSC2 line, and C contacts.

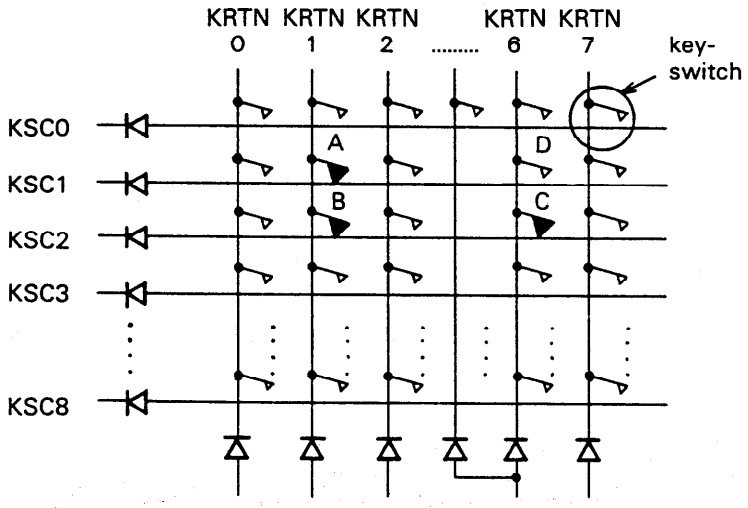


Fig. 2-72

2.7.4 Keyboard Circuit Element Layout

23 diodes and 3 resistors are placed on the keyboard, in addition to the key switches and LEDs. The diodes are put in the switch section of the keys indicated in Fig. 2-73. Their locations and names are printed on the back side of the keyboard board. The resistors are located as shown in Fig. 2-73.

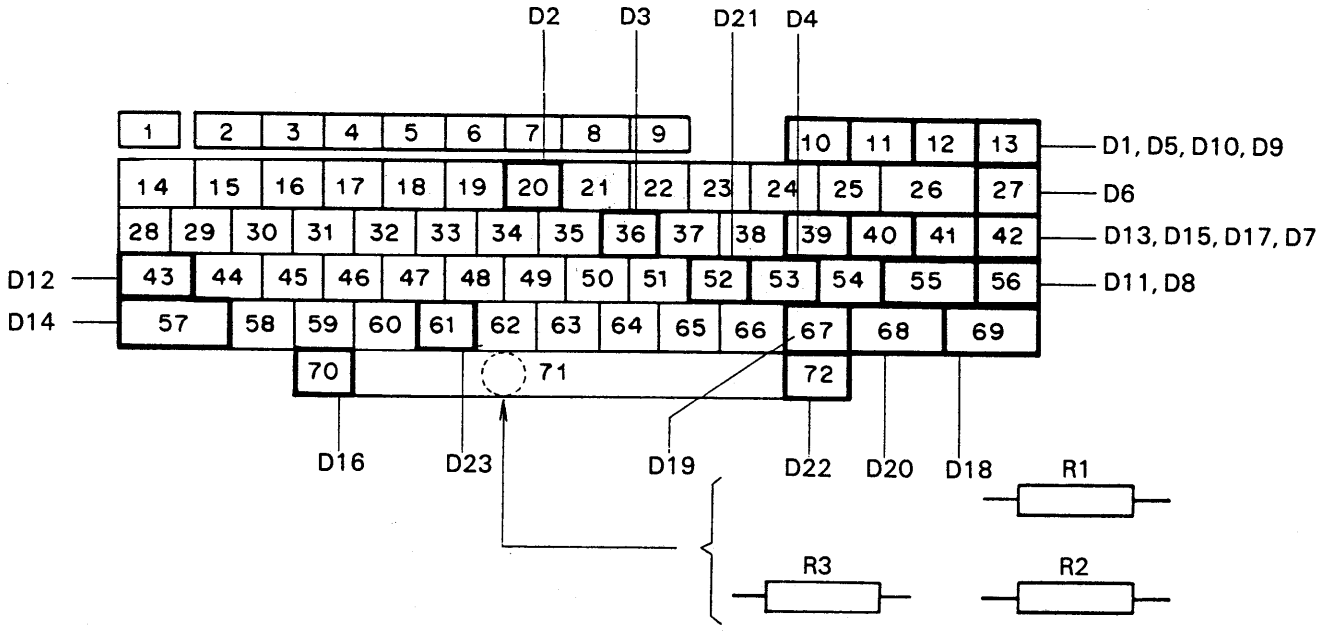


Fig. 2-73

Note: The Auto Repeat feature is ineffective for the following keys. (See Fig. 2-73)
2 ~ 9, 43, 57, 68, 69, 70, and 72

2.8 LCD Unit

The LCD unit consists of a driver board (MAP-LD) and a liquid crystal display panel, and provides a display area of 480 x 64 dots. The display panel is provided with a ratchet which allows adjustment for the optimum view angle. Fig. 2-74 is a control block diagram.

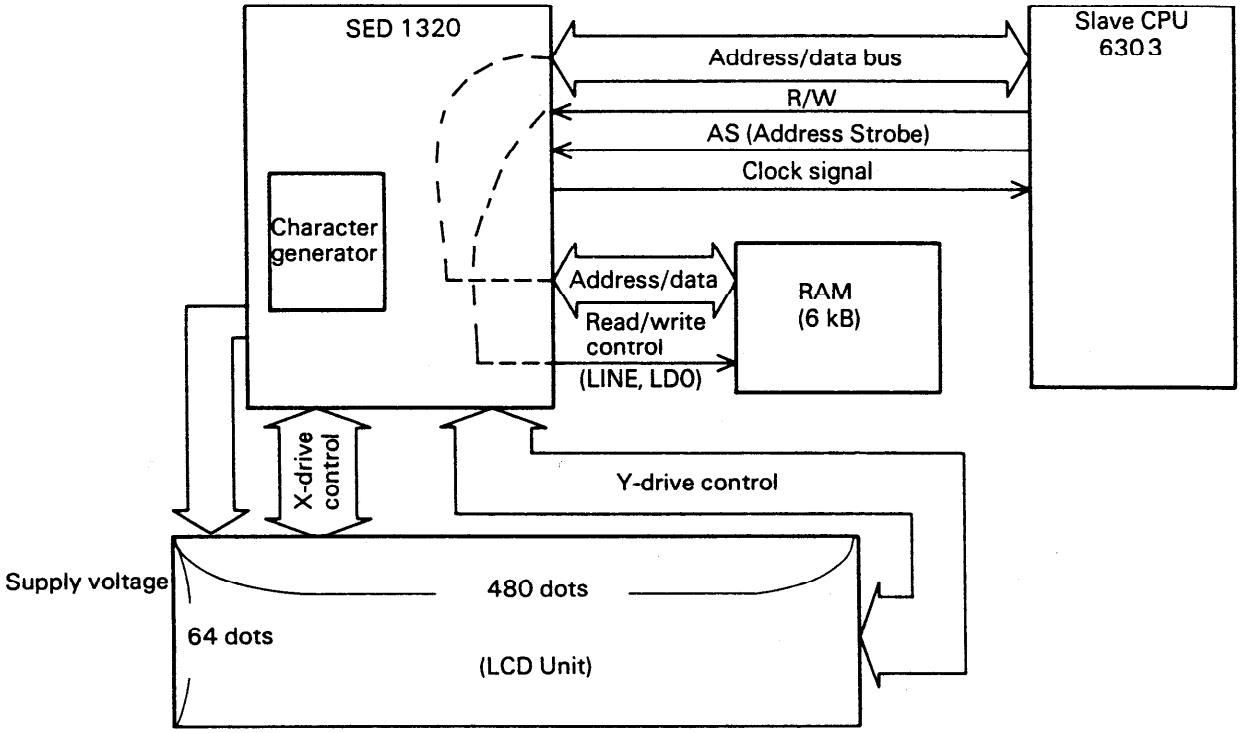
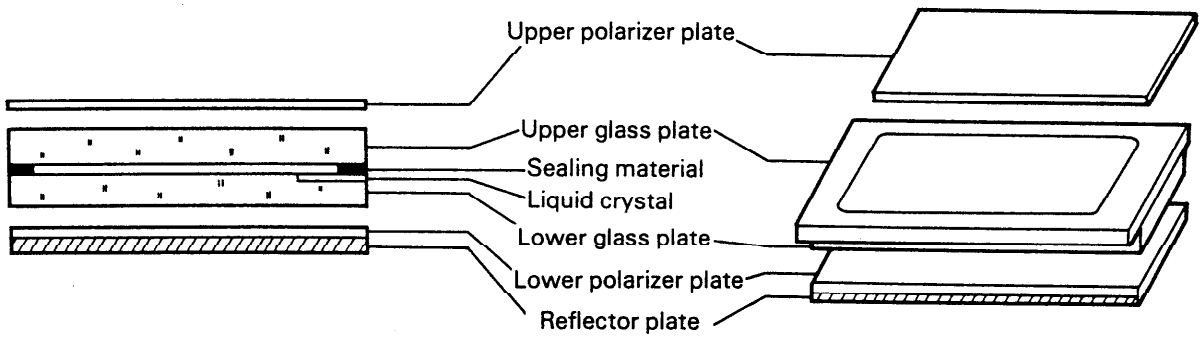


Fig. 2-74 LCD Unit Control Block Diagram

The LCD unit is controlled by the slave CPU 6303 as shown in the above block diagram. In the character mode, the character generator in SED1320 is used for display. In the graphic mode, however, the data from the 6kB RAM are displayed with all the data bits corresponding to the 480 x 64 display dots (or segments), one to one. In either mode, data are output bit-serially from SED1320 in synchronization with the X-Y drive line signals.

2.8.1 Liquid Crystal Display Panel Structure

The Liquid Crystal Display (LCD) display panel is a 480 x 64 dot matrix display panel which uses a twisted nematic (TNM) effect type liquid crystal – one of the voltage effect types. It is structured as shown in Fig. 2-75.



Note: The polarization angles of the upper and lower polalrizer plates differ by 90 degrees.

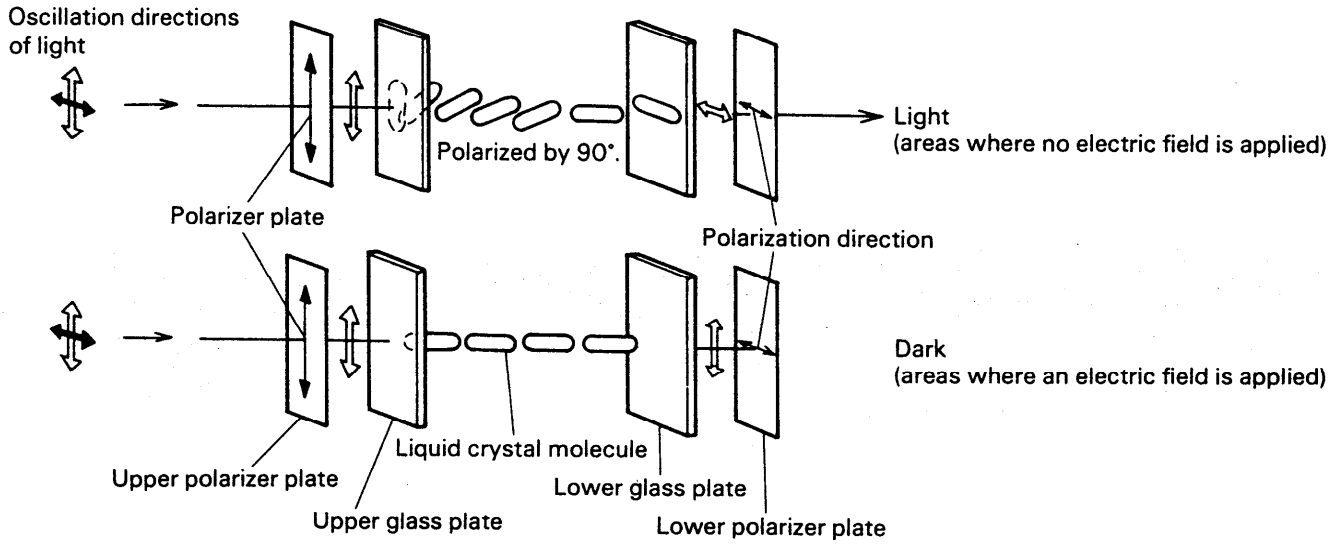


Fig. 2-75

2.8.2 Theory of Operation

The liquid crystal is confined between the upper and lower glass plates. The upper glass plate has many of electrodes regularly arranged on it. The liquid crystal characteristically shows a twisted motion, when a voltage is applied across it, depending on the magnitude of the voltage any the direction it takes determined by the direction of the applied electric field. Using of this characteristic for the display screen, light and dark contrast are produced on the panel by applying a voltage across the liquid crystal. To maintain this contrast, however, a refresh operation (a repeated application of voltage) is required simalar to the refresh system used for the dynamic RAM.

Optical contrast of the liquid crystal is produced in the mechanism as follows:. First, only the light elements which oscillate in a specific direction are transmitted through the upper polarizer plate onto the liquid crystal. The light, arriving on the liquid crystal, is affected, depending on whether an electric field is applied or not:

< When no electric field is applied >

The penetrating light is polarized by 90°. This causes the oscillation direction of the light to coincide with the polarization direction of the polalrilzer plate and the light is transmitted through it. Then, the light strikes the bottom reflector plate and is reflected, so that the panel looks light (white).

< When an electric field is applied >

The twisted orientation of the liquid crystal is corrected by the electric field and the optical activity is removed. The oscillation direction of the light penetrating the liquid crystal layer does not coincide with the polarization direction of the lower polarizer plate and is shut off by it. sults in no reflection from the bottom reflector plate so that the panel looks dark (black).

The reaction to the electric field varies depending on temperature. To compensate this, a variable resistor, called VIEW ANGLE is provided in the voltage source circuit.

- Display dot (segment)
  Each display dot has an area of 0.45 (high) × 0.41 (wide) mm². These dots are laid out at a vertical pitch of 0.5 mm and at a horizontal pitch of 0.46 mm as shown in Fig. 2-76.

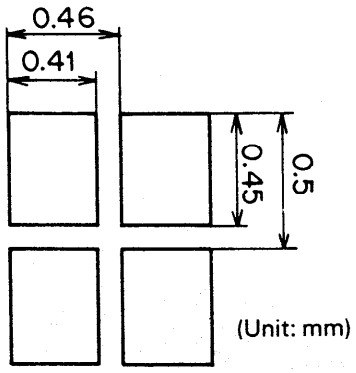


Fig. 2-76 Display Dot Dimensions And Layout

Notes:

As described above, variation of liquid crystal reaction can be compensated for by adjusting the X-Y drive line signal voltage with the sliding type variable resistor VIEW ANGLE over a certain temperature range. If the range is exceeded, however, this compensation is no longer possible, and the LCD panel may exhibit one of the following problems:

< Lower temperature >

- Liquid crystal reaction is slow and a long time is required until selected dots become visible (up to several seconds may be required)
- When the temperature further falls, no selected dots are visible over the entire panel.

< Higher temperature >

- The entire area of the panel looks dark (black) and selected dots are not easily recognizable.

- When the temperature further rises, the entire panel becomes completely black and no selected dots are visible at all.

* After being exposed to an abnormally low or high temperature, the LCD panel normally restores its original property by itself if it is left at the normal temperature for a while. If the panel is left in an abnormal temperature range beyond a certain limit of time, however, the liquid crystal may be permanently affected and the panel may not return to its original operating condition.

2.8.3 Circuit Operations

The LCD panel is structured as a 480 (horizontal) x 64 (vertical) dot matrix and dirven with eight SED1120 X-direction (vertical) drivers and one SED1130 Y-direction (horizontal) driver. The SED1120 drivers, each of which can drive 64 dots, are assigned to eight X drive lines X1 through X8, as shown in Fig. 2-77.

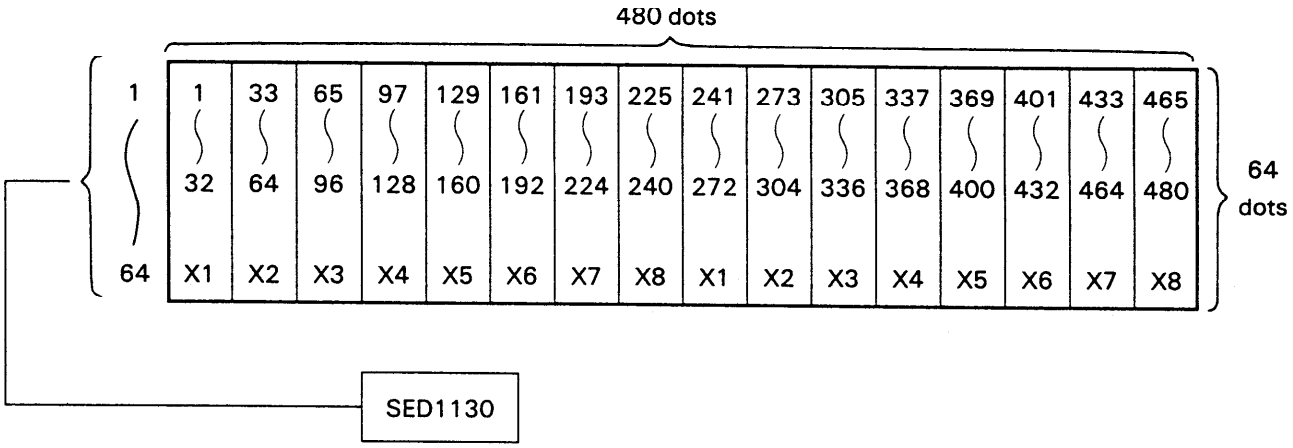


Fig. 2-77 X-Y Drive Scheme

2.8.3.1 Chip Selection

The eight SED1120 X-line drivers are cascaded as shown in Fig. 2-78. Data bits are transferred to one of these eight driver chips, one at a time, by means of a chip-enabling method designed to minimize power consumption.

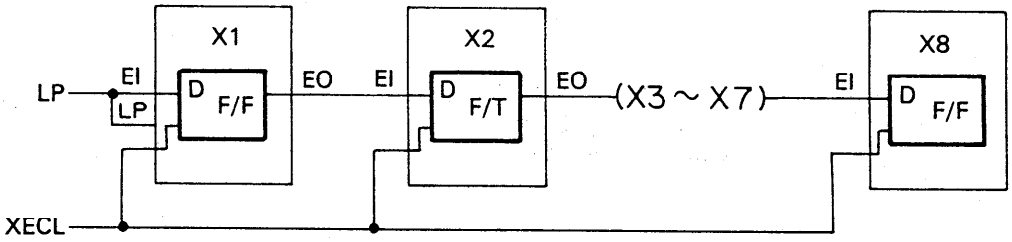


Fig. 2-78 SED1120 Data Transfer Scheme

In the above circuit, the Latch Pulse (LP) signal is supplied to the Enable Input (EI) terminal of the first (i.e., X1) SED1120 driver. Once the X1 driver is enabled (the internal flipflop is set ON) with a single LP signal pulse, the subsequent drivers X2 through X8 can be sequentially selected (or enabled) by the XECL signal.

2.8.3.2 Data Transfer

Four data lines are connected to each SED1120 driver and four-bit data is serially transferred one bit at a time. The data are transferred to a driver and are converted to parallel by an internal shift register. Fig. 2-79 outlines the timing relationship among the LCD operation signals.

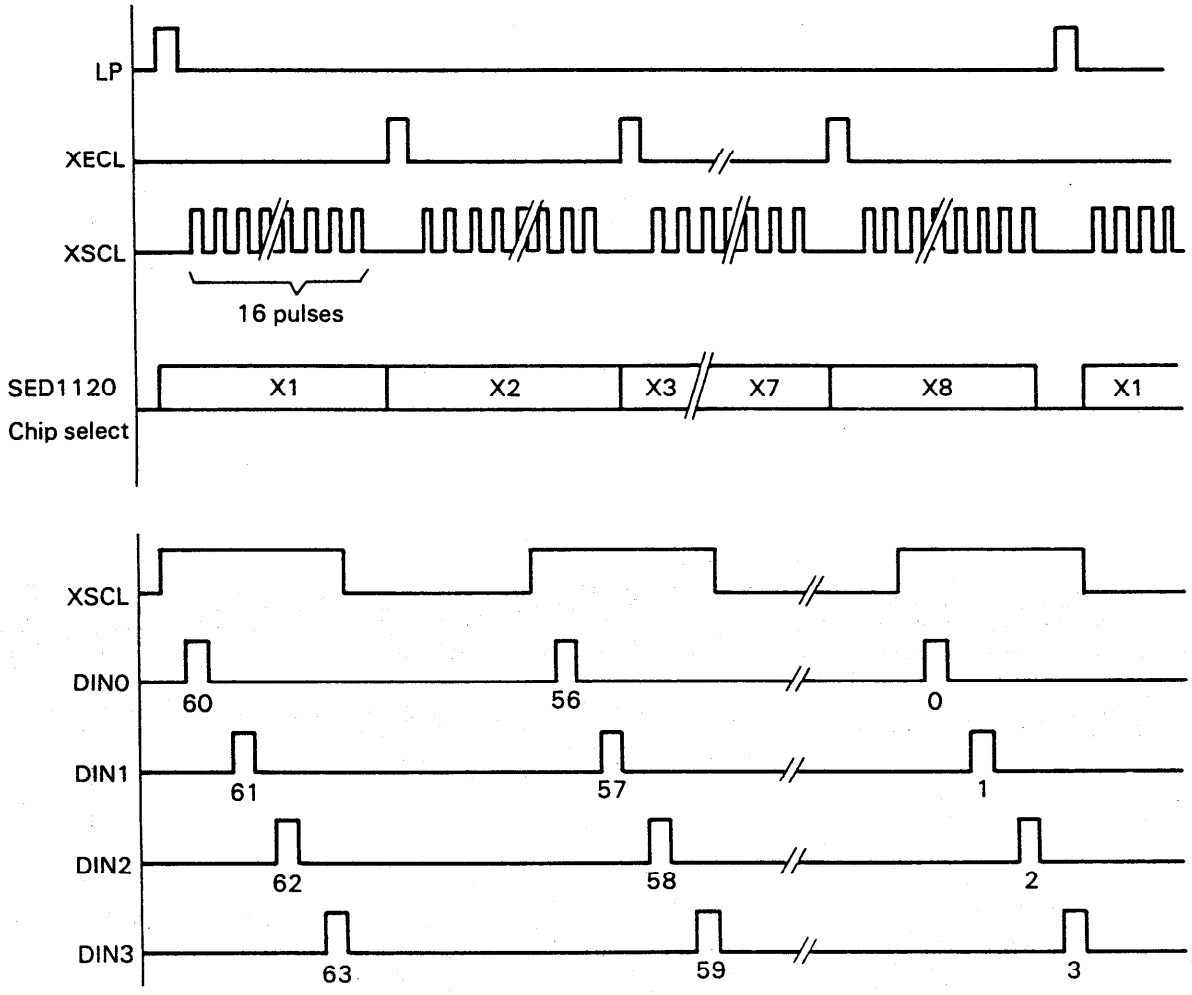


Fig. 2-79 LCD Operation Signal Timing

16 pulses of the data strobing signal XSCL are supplied to each SED1120 driver. During each of these pulses, data bits DIN0 through DIN3 are strobed. These data bits correspond to particular display dots and are transferred in sequence, beginning from those corresponding to the segments of the highest numbers as shown in the enlarged timing diagram in Fig. 2-79. This operation is repeated on all the SED1120 drives, X1 through X8, to display a single horizontal dot line. The series of operations needs to be repeated 64 times to display all dotons the entire LCD panel.

2.8.3 X-Y Display Control Timing

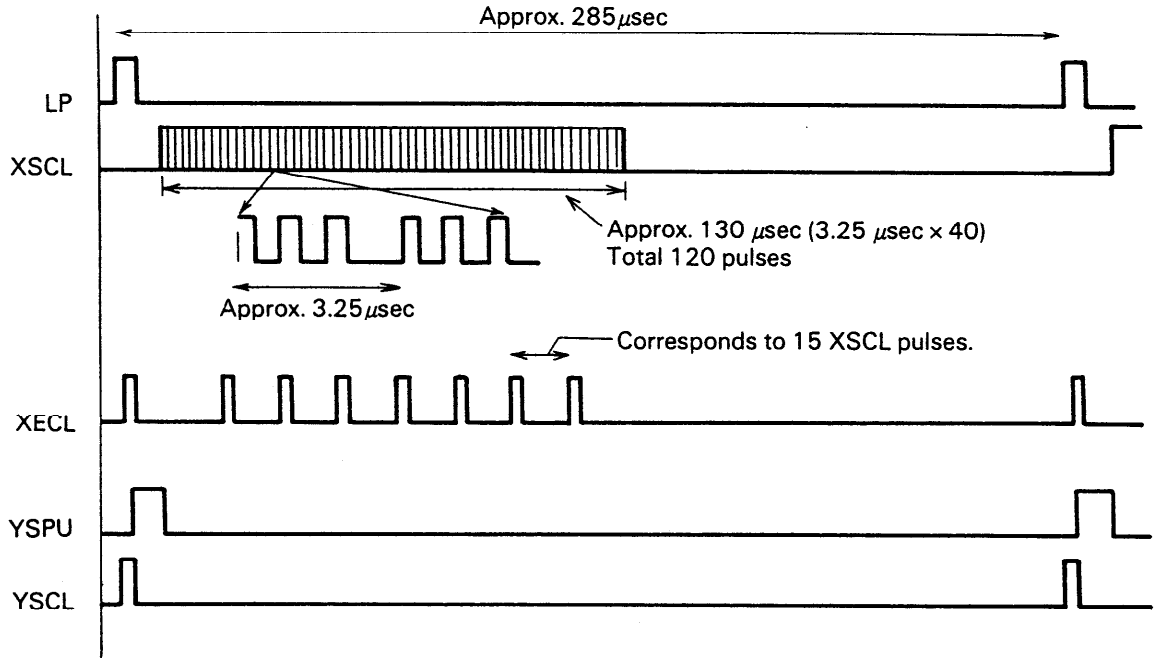


Fig. 2-80

Four displayed dots (or four data bits), are transferred by a single XSCL pulse. (480 dots = 4 x 120 x SCL pulses). The data bits for one entire dot line in the Y direction, are transferred in a duration of 130 μs.

A pulse signal LP is generated at the came frequency as the XSCL pulse signal. This signal outputs the Y-line data output signal YD00 when it is activated. This causes the Y-line drive position to be advanced by one dot to designate the next dot line.

Observed LCD X-Line Display Control Signal Waveforms

(Top) LP – measured at CN5, pin 7.

(Second from top) XSCL – measured at CN5, pin 9.

(Second from bottom) XECL – measured at CN5, pin 8.

(Bottom) XDO – measured at CN5, pin 10.

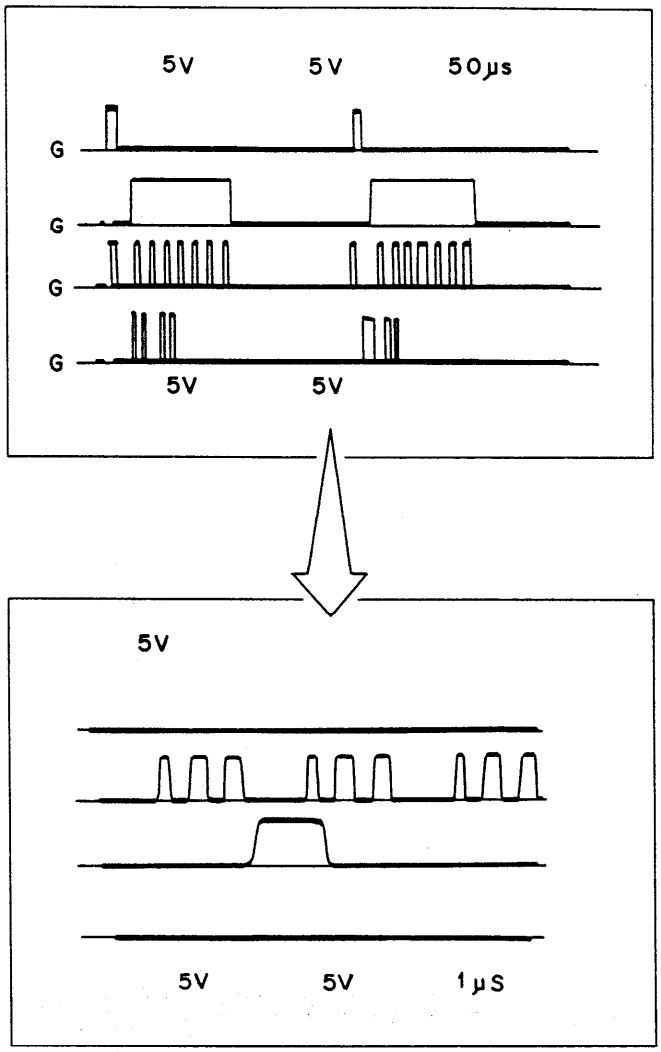


Fig. 2-81 LCD X-Line Display Control Signal Waveforms

(Top) XECL – measured at CN5, pin 8.
(Bottom) XSCL – measured at CN5, pin 3.

The XECL signal selects an X-drive IC (SED1120) from X1 to X8 on the MAP-LD board. 16 XSCL signal pulses correspond to each on XECL pulse, and four display data bits correspond to each on XSCL pulse. Thus, 64 data bits (display dots) are written to the selected X-drive IC in succession. Fig. 2-81 shows waveforms of the XECL and XSCL signals on different time base. 15 XSCL pulses correspond to the first XECL pulse and 16 XSCL pulses correspond to each of the subsequent XECL pulses.

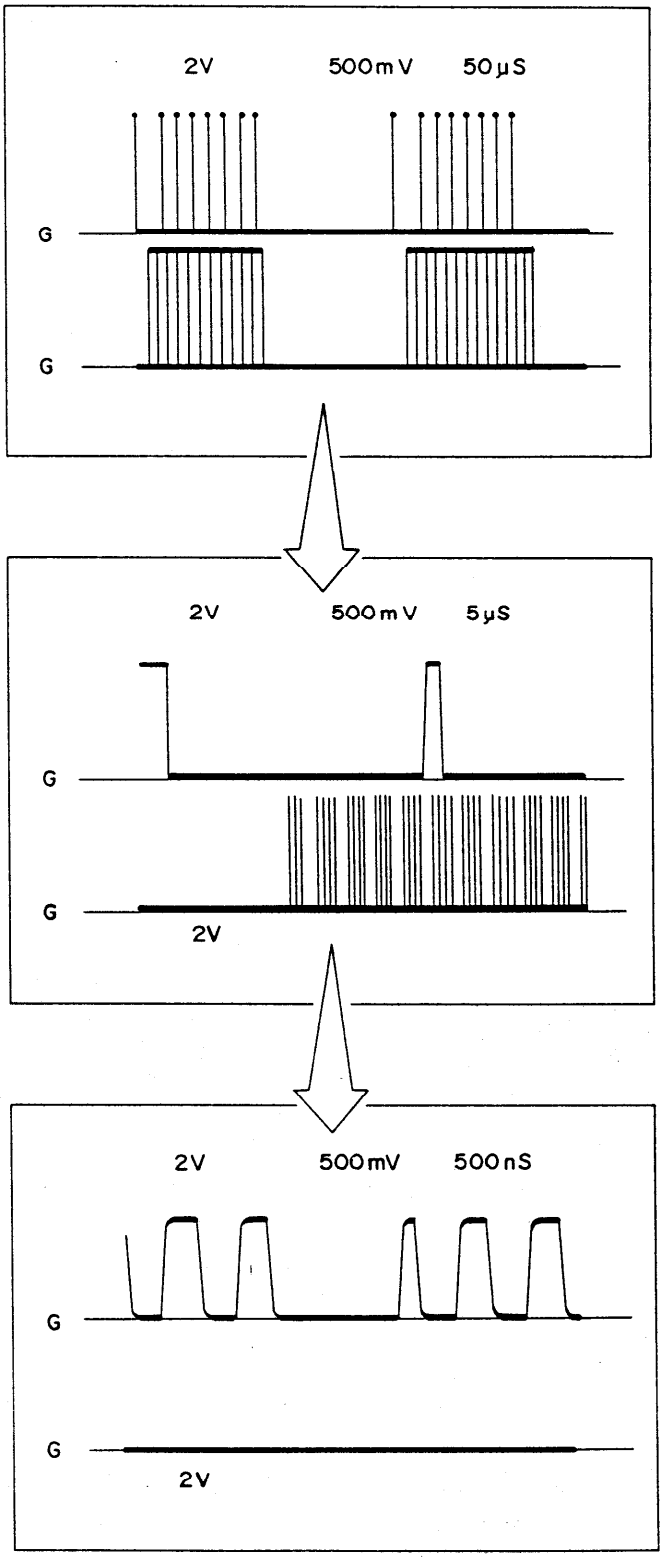


Fig. 2-81 LCD X-LINE Display Control Signal Waveforms

Observed LCD Y-Line Display Control Signal Waveforms

(Top) LP – measured at CN5, pin 7.

(Second from top) YSCL – measured at CN5, pin 3.

(Second from bottom) YSDU – measured at CN5, pin 4.

(Bottom) YSCL – measured at CN5, pin 9.

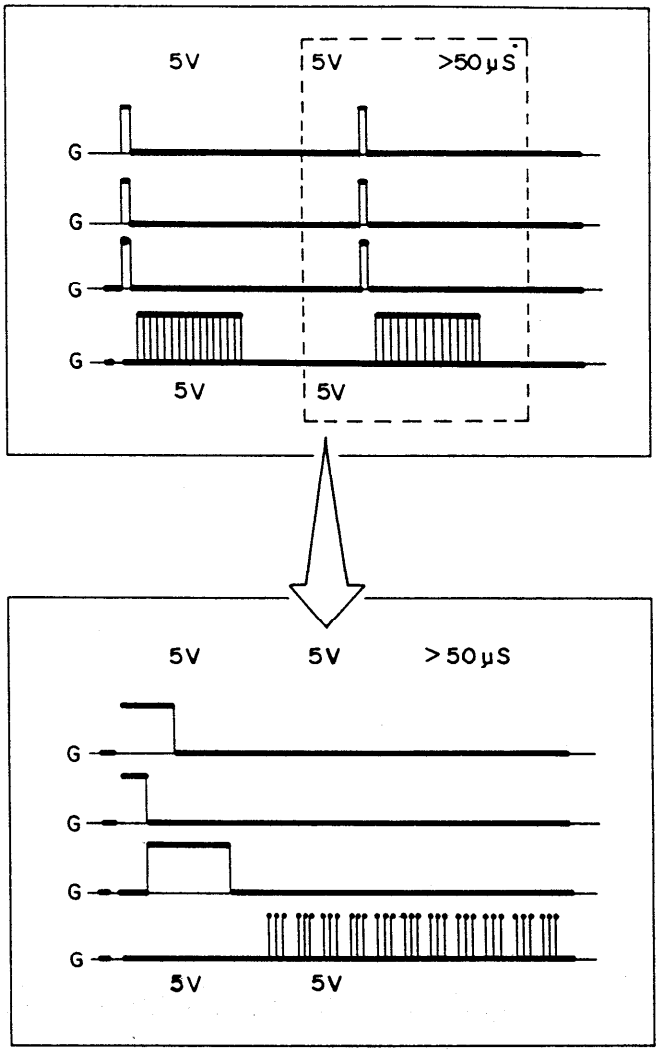


Fig. 2-83 LCD Y-Line Display Control Signal Waveforms

2.8.4 Jumper J5

This jumper allows the user to select one of two frame (FR) frequencios. It switches the FR signal to change the panel display mode. Jumper terminal A (see Fig. 2-84) is wired when the computer is shipped. Fig. 2-84 shows the FR signal generator circuit which includes the jumper Fig. 2-85 illustrates the timing relationships among various circuit signals.

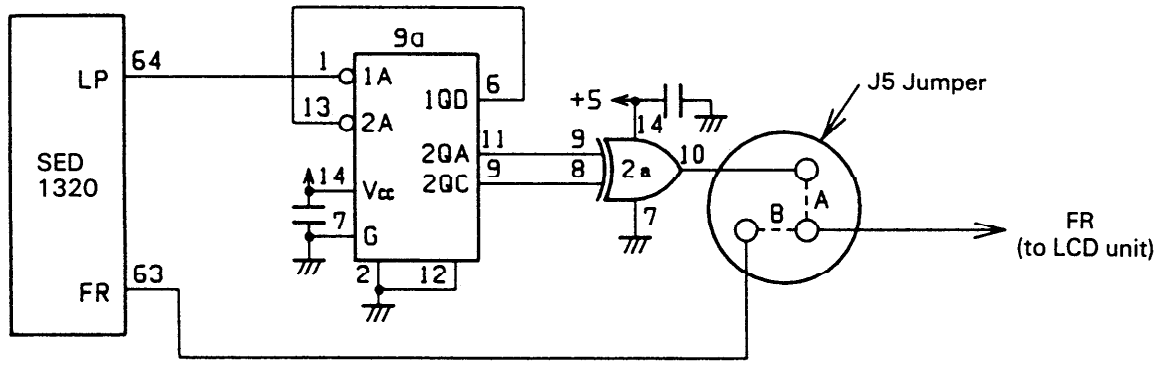


Fig. 2-84 FR Signal Generator Circuit

The LP signal is fed to the first stage of the dual 4-bit binary counter, IC 9a. The signal frequency is divided down to one sixteenth (285 μsec x 16 ÷ 4.5 msec) and is further fed to the second binary counter. Two outputs are provided from pins 11 (2QA) and 9 (2QC) of the second counter, which respectively have one 32nd and one 128th of the original LP signal frequency.

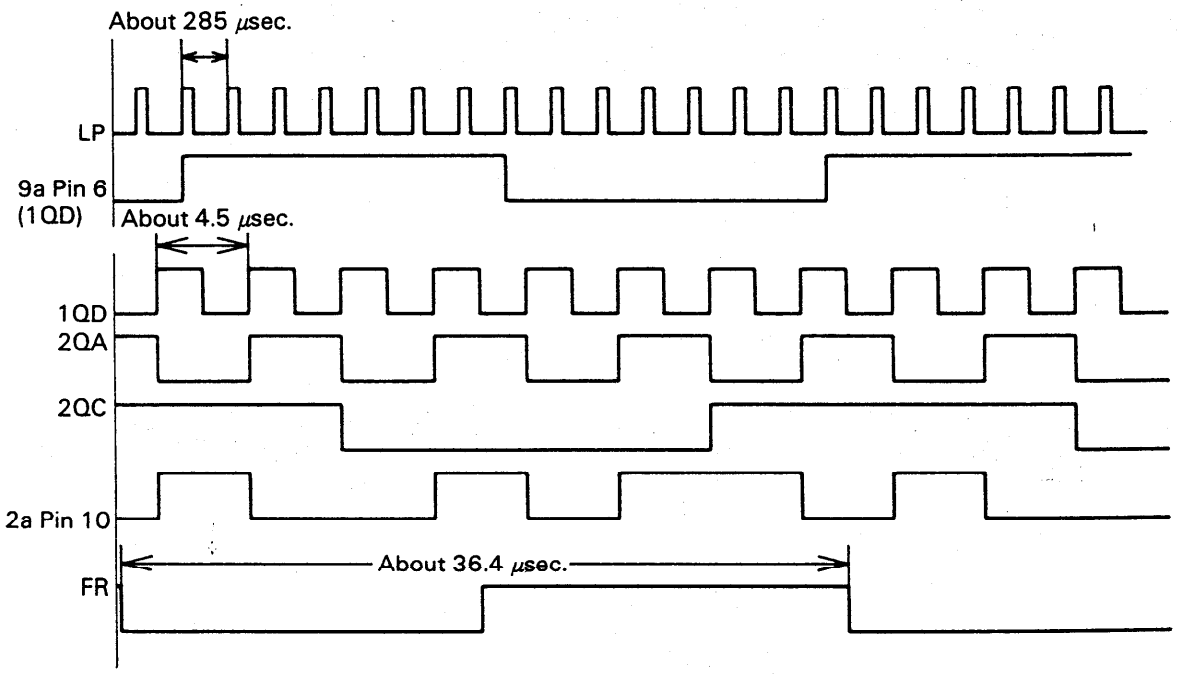


Fig. 2-85 Timing Relationship Among RF Signal Generator Circuit Signals

The FR signal is supplied to the LCD X and Y drivers to accomplish the display as follows:

Table 2-15

480 dots

1	1	3	5	7	9	11	13	15	2	4	6	8	10	12	14	16
2	17	19	21	23	25	27	29	31	18	20	22	24	26	28	30	32
3	33	35	37	39	41	43	45	47	34	36	38	40	42	44	46	48
4	49	51	53	55	57	59	61	63	50	52	54	56	58	60	62	64
5	65	67	69	71	73	75	77	79	66	68	70	72	74	76	78	80
⋮																
64	1009	1011	1013	1015	1017	1019	1021	1023	1010	1012	1014	1016	1018	1020	1022	1024

64 dots

Data are displayed on the LCD panel as dots; numbers in Table 2-15 correspond to dot positions on the display screen.. At least 64 LP pulses are required to display all the dots. Thus, a data transfer time of approximately 18.2 ms (285 μs x 64) and the same amount of non-data-transfer time – i.e., a total of approximately 36.4 ms, – are required for each 1-panel display cycle.

The data transfer and non-transfer cycles can be altered as shown in Fig. 2-86 by changing the J5 jumper connection.

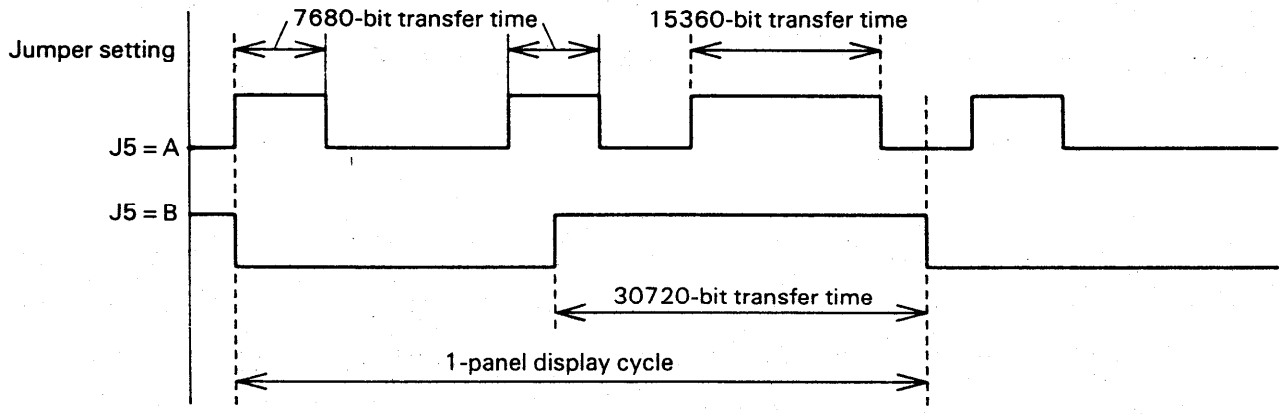


Fig. 2-86

Jumper J5 may need to be reset in order to reduce ghost display lines due to the difference in liquid crystal characteristics between LCD panels.

Fig. 2-87 shows actual waveforms of the two FR signals.
(Top) J5, A (IC 2a Pin 10)
(Bottom) J5, B (IC 7c Pin 63)

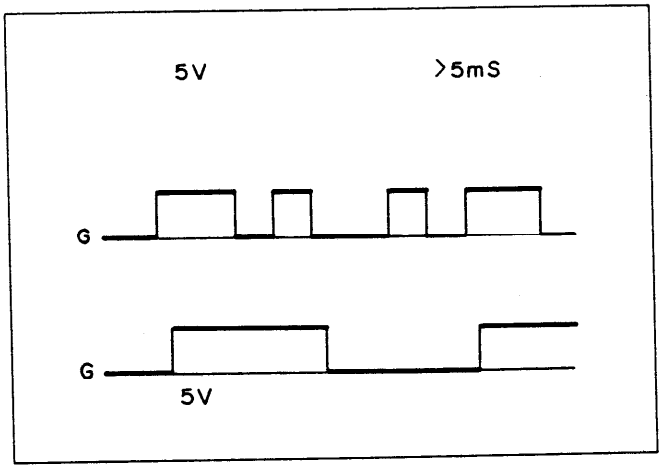


Fig. 2-87 FR Signal Waveforms

The proper FR signal should be selected by jumper J5, according to the nature of the liquid crystal display panel. If the jumper is improperly wired or not wired at all, vertical or horizontal ghost linesmay appear on the screen.

Select either signal A or B, observing which gives less ghost and better display quality.

2.9 A-D Converter

This is an A-D converter which has an analog input multiplexer and an input/output serial interface built in. A reference voltage of +2V is supplied to the converter, and is used to compare the various analog input voltages for conversion as shown in Fig. 2-88

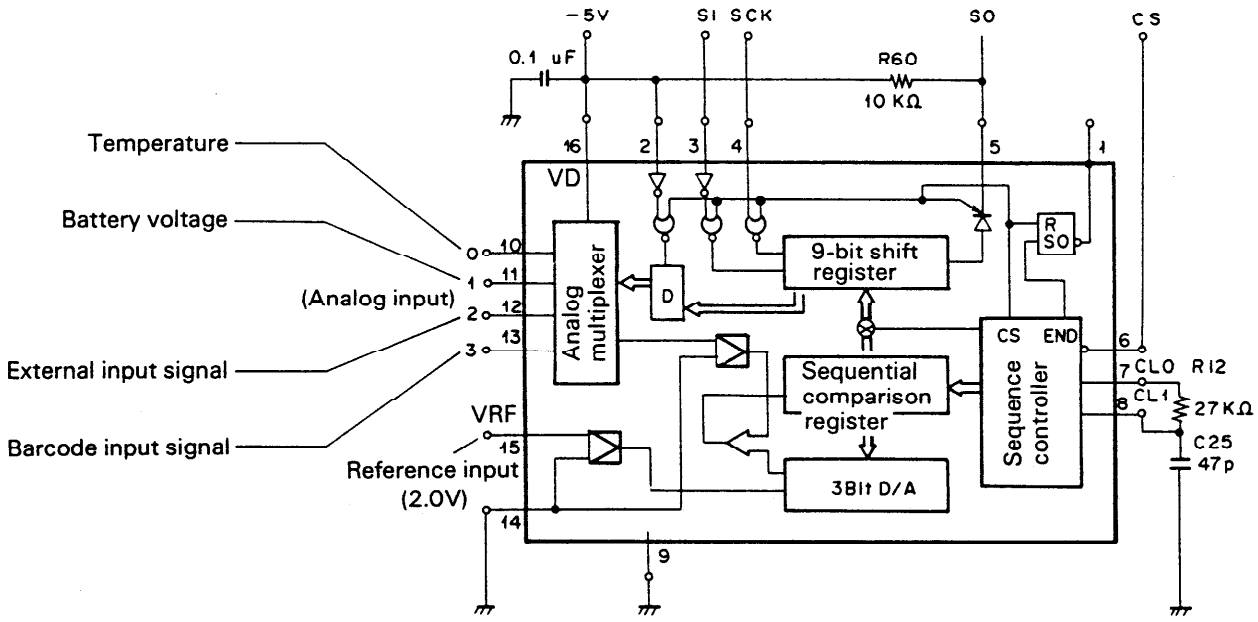


Fig. 2-88

2.9.1 Operation Control

The +2V reference voltage and a clock signal of approximately 400 kHz are fed from external circuits when the +5V source is supplied, and the converter is activated. Then, to accomplish an actual A-D conversion, the following sequence of control operations must be externally provided:

1. Channel Selection

   After activating a low $\overline{CS}$ signal , the first channel selection address bit is supplied via the SI signal line, together with one shift clock pulse from the $\overline{SCK}$ signal line. Repeating this operation eight times, with the adress bit changed each time in sequence, causes the complete desired channel address to be set to the shift register in the converter. This then goes high. This causes the least significant bits of the shift register to be set to the address latch decoder and the channel is selected according to the two bits as shown in Table 2-16.

Table 2-16 Channel Selection

Bit 0	Bit 1	Analog channel
0	0	0 (Temperature)
1	0	1 (Battery voltage)
0	1	2 (External input)
1	1	3 (Barcode)

2.9.1.1 A-D Conversion

Turning the $\overline{CS}$ signal high causes the A-D conversion, using the selected analog input channel when the sequence controller sets virtual bits to the sequential comparison register. An analog voltage equivalent to the value of the bits set in the sequential comparison register is generated by the converter and compared with the input analog voltage by a built-in comparator. It is then determined whether or not to reset any of the virtual bits, depending on the compared result. This operation is repeated until the exact combination of bits, which is equivalent to the input analog voltage, is finally set in the sequential comparison register. This sequence of operations requires a minimum of 56 clock pulses, and the entire sequence is repeated until the $\overline{CS}$ signal is turned low. Thus, the sequential comparison register is refreshed approximately 14 every μs (2.5 μs x 56 = 140 μs) because the clock cycle is approximately 400 kHz.

2.9.1.2 Converted Digital Data Read

Turning the $\overline{CS}$ low causes the sequence controller to stop operating, terminating the conversion. Approximately 12.5 μs (a duration of 5 clock pulses) after this, the internal $\overline{CS}$ signal, which is used in the sequence controller, goes low, allowing the converter to be interfaced with the external circuit via signal terminals such as SO and $\overline{SCK}$, etc. The contents of the sequential comparison register have been set to the shift register by this time. Thus, when the shift clock ($\overline{SCK}$) pulse is supplied, the digital data is output over the SO line one bit at a time at the rising edge of the pulse.

2.9.1.3 Output Data

A specific value of total error is inherent to this A-D converter due to its physical property which varies depending on reference voltage. It internally converts an input analog voltage to a digital value of eight bits. However, the total error at a reference voltage of 2.0V is equivalent to the two least significant bits. Thus, only the six most significant bits are effective.

2.9.1.4 Timing

Fig. 2-89 shows a conceptual basic operation timing of the converter. The minimum conversion time corresponds to a duration of 56 clock pulses, writch is approximately 140 μs (2.5 μs x 56 = 140 μs) because the clock cycle is approximately 400 kHz. Thus, a total data transfer time of approximately 400 μs is required for channel selection and digital data read.

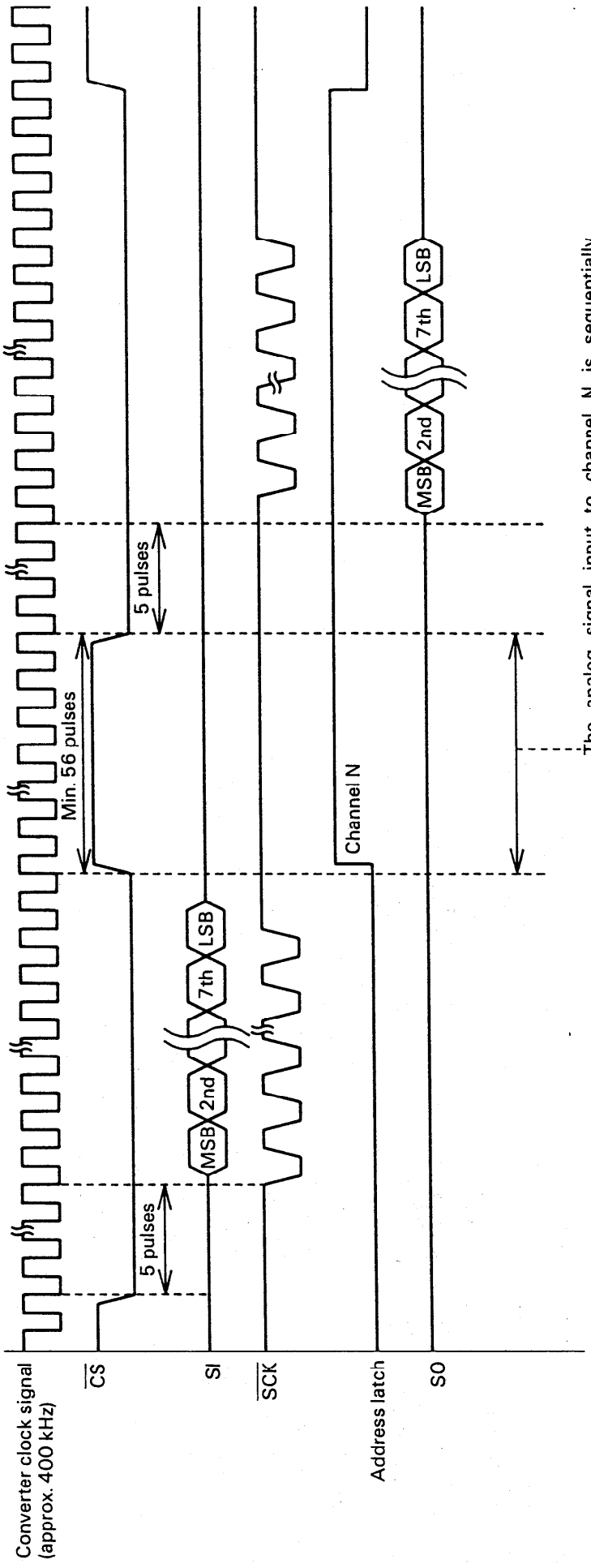

Converter clock signal
(approx. 400 kHz)
CS
SI
SCK
Address latch
SO
5 pulses
Min. 56 pulses
5 pulses
MSB
2nd
7th
LSB
Channel N
MSB
2nd
7th
LSB
The analog signal input to channel N is sequentially A-D converted and stored in the shift register in duration of time.

Fig. 2-89

2.9.2 Battery Voltage Detector Circuit

The battery voltage delection circuit detects two specific signals from low voltage (approximately 4.7V) and a recharge start voltage (approximately 5V)

When these voltage are sensed, following sequence is initialed.

- Low voltage..... approximately +4.7V
  When this voltage is detected, the 7508 forces the current computer operation to an end at an appropriate point (a point at which the terminated operation can be properly resumed) and switch the main battery to the auxiliary battery.
- Recharge start voltage ..... approximately +5V
  When this voltage is detected while the AC adaptor is connected, the 7508 switches the charge from trickle to normal mode.

2.9.2.1 Circuit Operations

Fig. 2-90 shows the battery voltage detector circuit. The battery voltage VB is fed to Ithe divider circuit, which consists of R69 and R57, through the fuse F1,and the transistor Q32. The divided voltage is supplied to channel AN1 of the A-D converter. The voltage drop across F1 and Q32 is negligible and the voltage at the AN1 terminal V_{AN1} is given as follows:

$$AN1 = \frac{VB \cdot R57}{R69 + R59} \quad \cdots\cdots AN1 \fallingdotseq 0.36 \cdot VB$$

- Low voltage: The converted digital value, which is equivalent to the low voltage of +4.7V, is D9(H) at a reference voltage of +2.0V (the digital equivalent is FF(H)). This value is approximately equivalent to 1.69V. Thus, the VB voltage of 4.7V should generate a potential of 1.75V at terminal AN1 as determined by the following expression:

$$VB_{(x)} = \frac{1.69}{0.36}$$

- Recharge start voltage: The recharge start voltage of +5V is converted to a digital value of E6(H). Thus, the potential at terminal AN1 should be 1.8V.

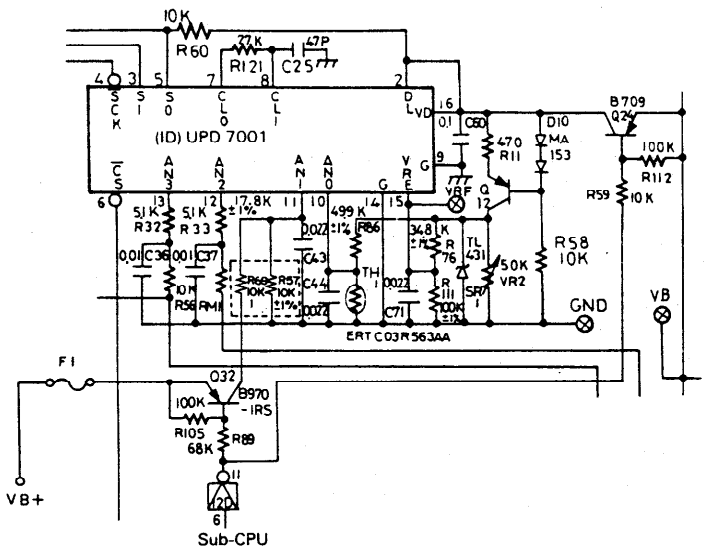


Fig. 2-90

2.9.3 Temperature Detector Circuit

When the power switch is off, battery power consumption is minimized by optinizing the refresh current according to ambient temperatures. The ambient temperature is sensed by a thermistor and fed to channel AN0 of the A-D converter which detects the reference temperatures.

2.9.3.1 Circuit Operations

Fig. 2-91 shows the temperature detector circuit, including the sensing section. The reference voltage (VRF) is adjusted to +2.0V by VR2. Thus, the potential at point (A) is given as follows, because of the voltage divider circuit consisting of R76 and R111:

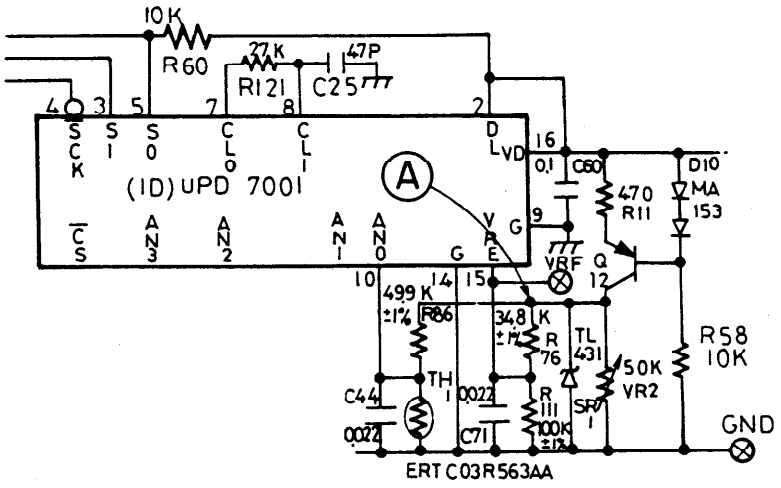


Fig. 2-91 Temperature Detector Circuit

$$VRF = \frac{R111 \cdot Vx}{R76 + R111}$$

$$Vx = \frac{VRE\,(R76 + R111)}{R111}$$

$$Vx = \frac{2\,(34.8 \times 10^3 + 100 \times 10^3)}{100 \times 10^3} = \underline{2.696\ (V)}$$

Potential at point (A)

The potential (A) is also applied to the voltage divider circuit consisting of R86 and the thermistor TH1, which is the temperature sensor. The potential at the junction of R86 and TH1, VTH, which is supplied to channel AN0, is therefore represented by the following expression:

$$VTH = \frac{R\,(TH1) \cdot 2.696}{R86 + R\,(TH1)}$$

where the thermister resistance R (TH1) has the following temperature characteristic:

$$R\,(TH1) = 56\ K \exp 4.3\left(\frac{1}{0.2732 + t} - \frac{1}{0.2982}\right)\ [t:\ ^\circ C]$$

As the temperature rises, the thermister resistance decreases, causing the voltage supply to the AN0 channel (VTH) to be lowered.

2.9.3.2 Processing By Sub-CPU After Detection

The sub-CPU 7508 converts the AN0 voltage to a digital value based on the reference voltage. The sub-CPU then finds the points that correspond to 25°C and 45°C, and controls the D-RAM refresh current for saving power consumption as follows:

<Temperature range (°C)>	<D-RAM refresh current (μA)>
45 or above	1400
25 or above	600
Below 25	300

2.9.4 Analog Input (ANIN)

The Analog Input (ANIN) terminal in the analog input interface, which is connected to the AN2 terminal of the A-D converter, provides a universal A-D conversion capability which can convert any analog voltage signal from 0V to +2V to digital data from 00 (H) to FF (H). A triggering output (TRIG) terminal is provided in this interface so that a wide variation of analog devices from a simple one such as a joystick to a complicated measurement instrument can be connected. The ANIN signal line may be pulled up to the +5V supply via the jumper J4.

The input signal is limited from 0V to +5V by voltage limiter diodes, and high frequency noises on the signal line are removed by a filter circuit, including the capacitor C37, before being connected to the A-D converter. Fig. 2-92 shows the barcode control circuit.

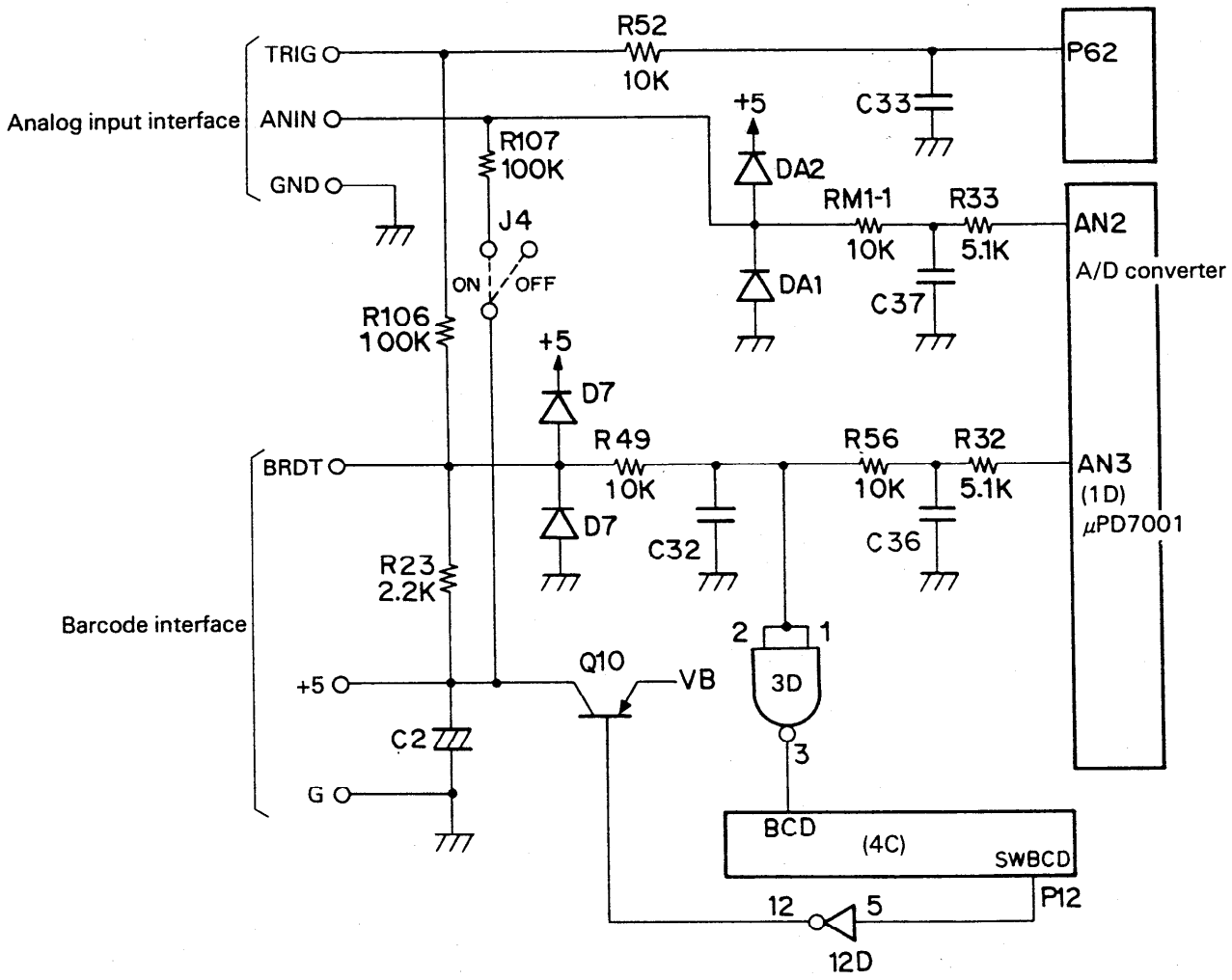


Fig. 2-92 Barcode Control Circuit

2.9.5 Barcode Input (BRDT)

The barcode input (BRDT) terminal is connected to the AN3 terminal of the A-D converter, through voltage limiter and noise limiter circuits similar to the ANIN signal line described above, and pins 1 and 2 of the NAND gate 3D. The NAND gate feeds the barcode data input signal to the read circuit, which is discussed in detail in the next section, "Barcode Interface". The AN3 channel provides a route to a special check function for any unacceptable deviation from the nominal voltage levels, +5V and the ground level, of the barcode data signal.

Barcode Interface

There are may barcode systems for each of which a different barcode data read progam is required. In addition, there are numerous models of barcode readers whose hardware characteristics (which require different barcode color pattern specifications, scanning angles, and/or reading heights, etc.). This computer incorporates an interface for TTL-compatible, hand-held barcode readers which are discussed in detail in the following:

This interface has a +5V line terminal that can be used to supply the operating power to the connected barcode reader. The supply is controlled by the barcode reader power on/off (SWBCD) signal fed from port 12 of the gate array GAH40M which can be directly controlled by bit B of main CPU address 00.

The barcode data signal line is supplied to the AN3 terminal of the A-D converter, through a voltage limiter and noise eliminator circuits, similarl to the ANIN signal line, and port 14 of GAH40M (BCD) after being inverted by the IC 3D as described above. There the signal is examined whether it is active (ON or MARK) or inactive (OFF or SPACE), and each active (MARK) duration (i.e., the pulse width) is measured under the control of the main CPU. Before proceeding to the discussions on the barcode interface circuit operations, basic functional theories of a barcode reader and a sample waveform which it generates from a given barcode pattern are discussed here.

Barcode Reader

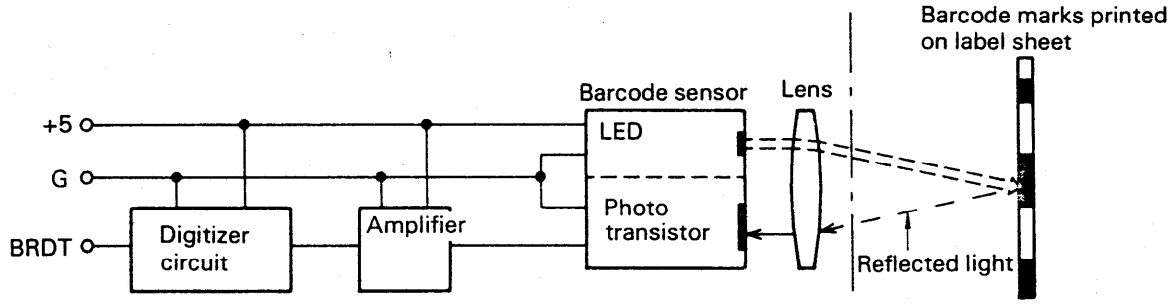


Fig. 2-93 Barcode Reader Funcational Block Diagram

As shown in Fig. 2-93, the reader has a light source and a reflected light sensor which connects the optical barcode pattern (a series of variations of contrast, generated by the black stripes and exposed white sheet) to a series of electrical pulses. Many barcode readers are of a hand-held type so that each scan inevitably causes a variation in the output pulse signal (BRDT) due to difference of scanning speed as shown in Fig. 2-94.

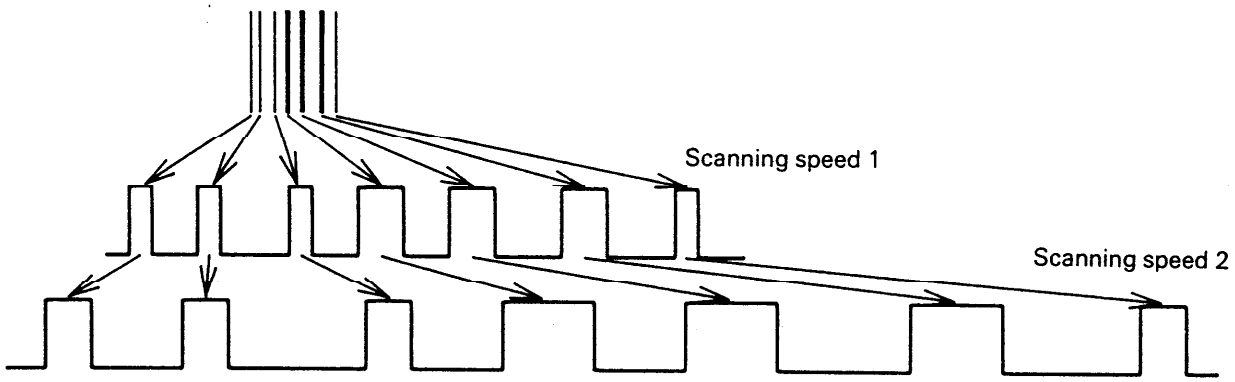


Fig. 2-94 Barcode Data Signal Variation Due To Scanning Speed Difference

If the pattern were read at almost the same scanning speed (i.e., at a constant barcode movement speed), the ratio of the corresponding marks and spaces would remain the same. Thus, the pattern could be correctly read in principle by supposedly triggering a time measurement mechanism with each pulse, measuring the time between the pulses, and processing the pulse intervals based on a reference timing obtained from the measurment. This sequence of operations are actually accomplished by software as discussed below.

Barcode Data Processing

Read barcode pattern data are detected and processed under the control of the main CPU. A trigger pulse, which is generated by the leading and/or trailing edge of each arriving barcode data pulse and a free-running counter (an endless counter which repeats counting from 0000 (H) to FFFF (H) are used to detect the pulses; a data pulse is detected by comparing the counter value at the time a trigger pulse is generated and at the time the next trigger pulse is generated.
Fig. 2-96 illustrates the operation.

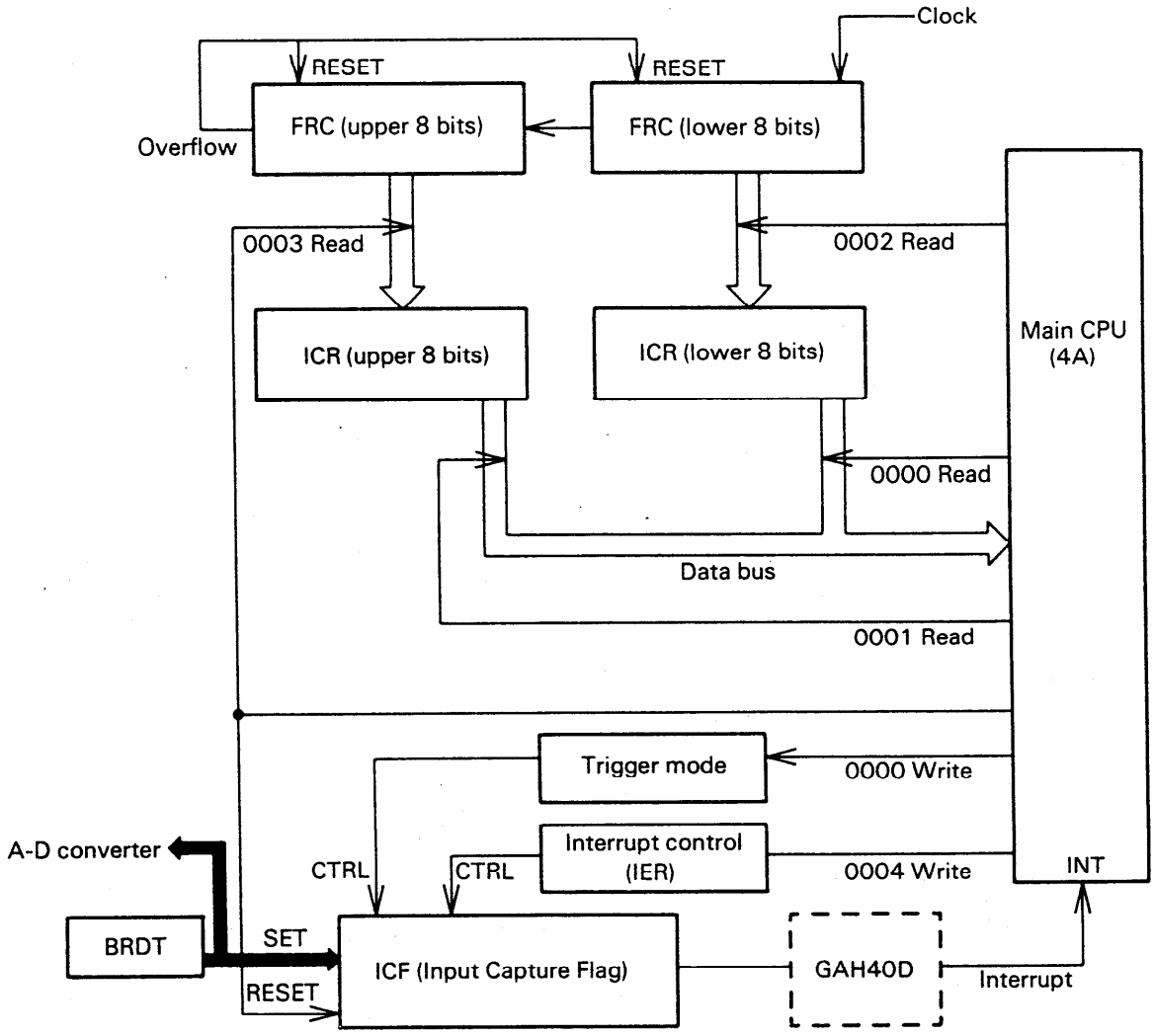


Fig. 2-95 Barcode Data Read Circuit Block Diagram

The barcode data read control is initiated by an interrupt issued from the gate array GAH40D to the main CPU. It occurs when the input capture flag (ICF) is turned ON by a barcode pattern read (i.e., reader scanning). The trigger may be generated at a different point or points on the pulse, depending on the BRDT triggering mode selected by the user. (See Table 2-17.)

Table 2-17 BRDT Triggering Modes

Address 0000		BRDT triggering mode (polarity)
Bit 1	Bit 0	
0	0	Triggering is disabled
0	1	↓ Triggering at falling edge
1	0	↑ Triggered at rising edge
1	1	↑↓ Triggered at both rising and falling edges

When interrupted, the main CPU first reads address 0002 to store the lower eight FRC bits in the corresponding lower half of ICR, then it reads address 0003 to store the upper eight FRC bits in the upper half of ICR, and resets ICF, removing the triggering signal. At the time the trigger pulse is generated, the main CPU reads addresses 0000 and 0001 to determine the FRC count value; ICR maintains this value until it is updated by the next FRC

read, while FRC continues counting until another interrupt by the BRDT trigger pulse occurs. The next pulse repeats the operation. In this manner, the main CPU can accurately read the barcode pattern data by means of software.

The BRDT signal is also connected to the A-D converter; converter output is used to examine the barcode data signal for any unacceptable deviation from the nominal voltage levels and has nothing to do with data read.

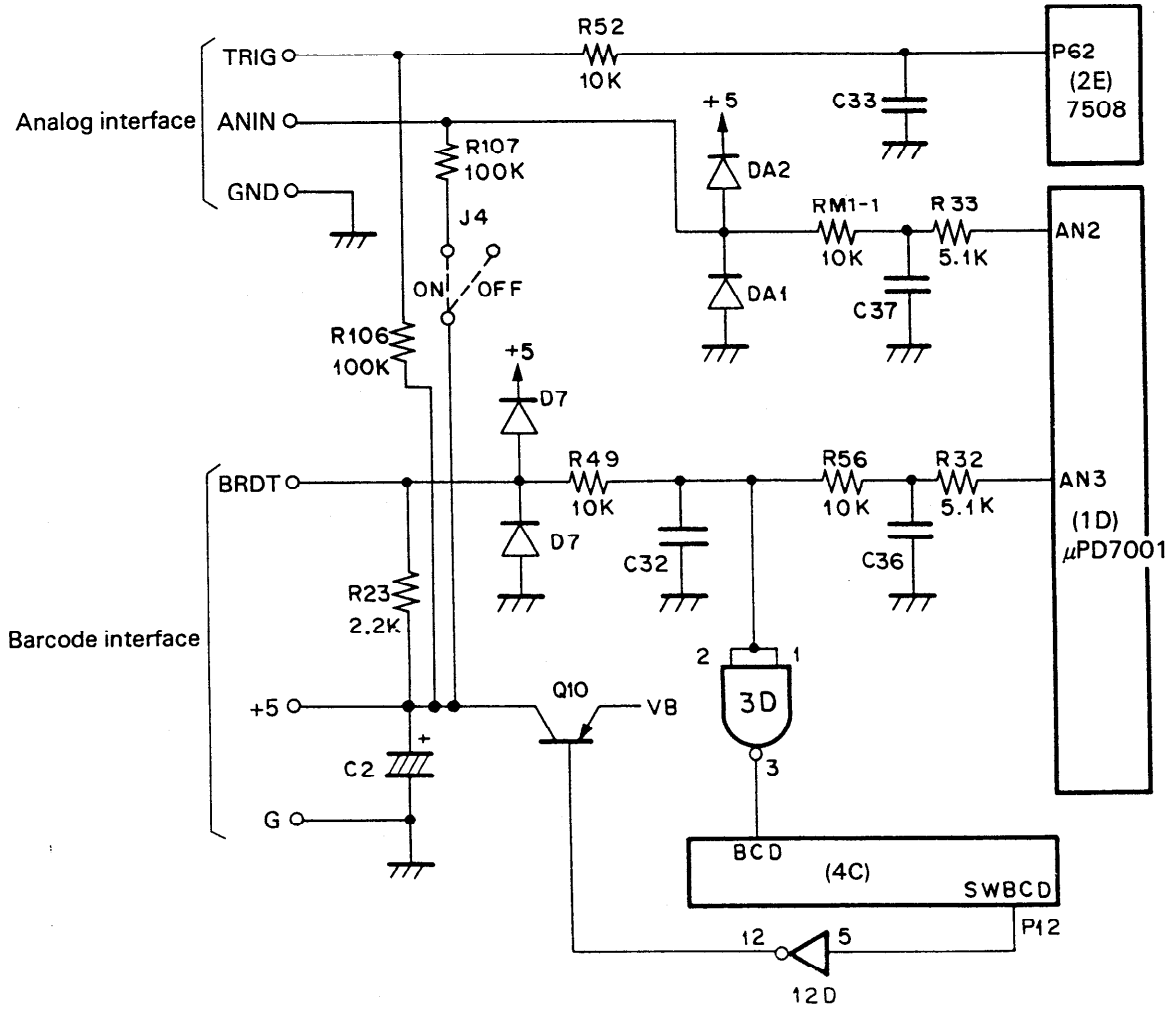


Fig. 2-96 Barcode Interface Circuit

Fig. 2-97 shows an example of the barcode patterns. (This pattern is for low-resolution of CODE 39.

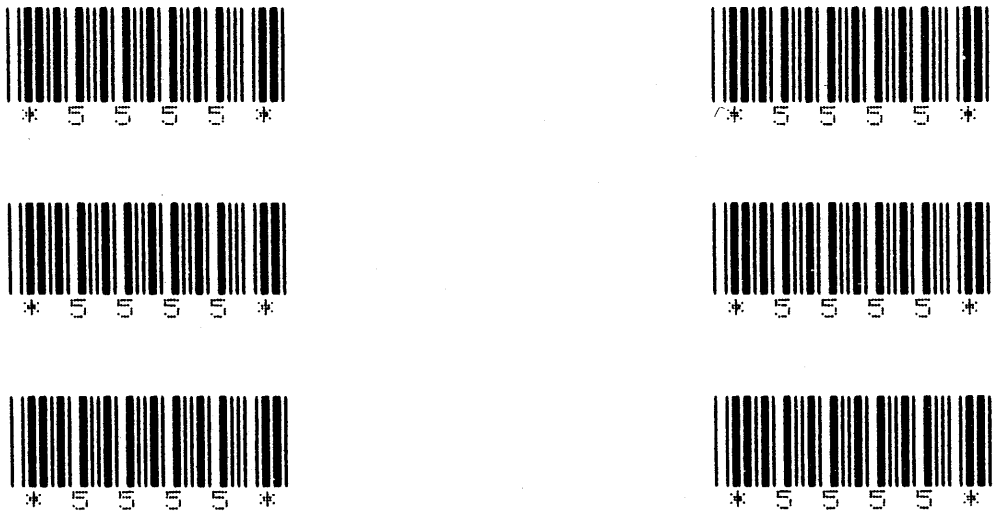


Fig. 2-97

2.10 ROM Capsule

The ROM capsule can hold two 256kB ROMs and is controlled by the gate array GAH40S. A power supply line which generates and supplies +5V power from the VB line to the capsule, as required, is also included in the circuit. Fig. 2-98 is a block diagram of the ROM capsule and its control and data lines and buses.

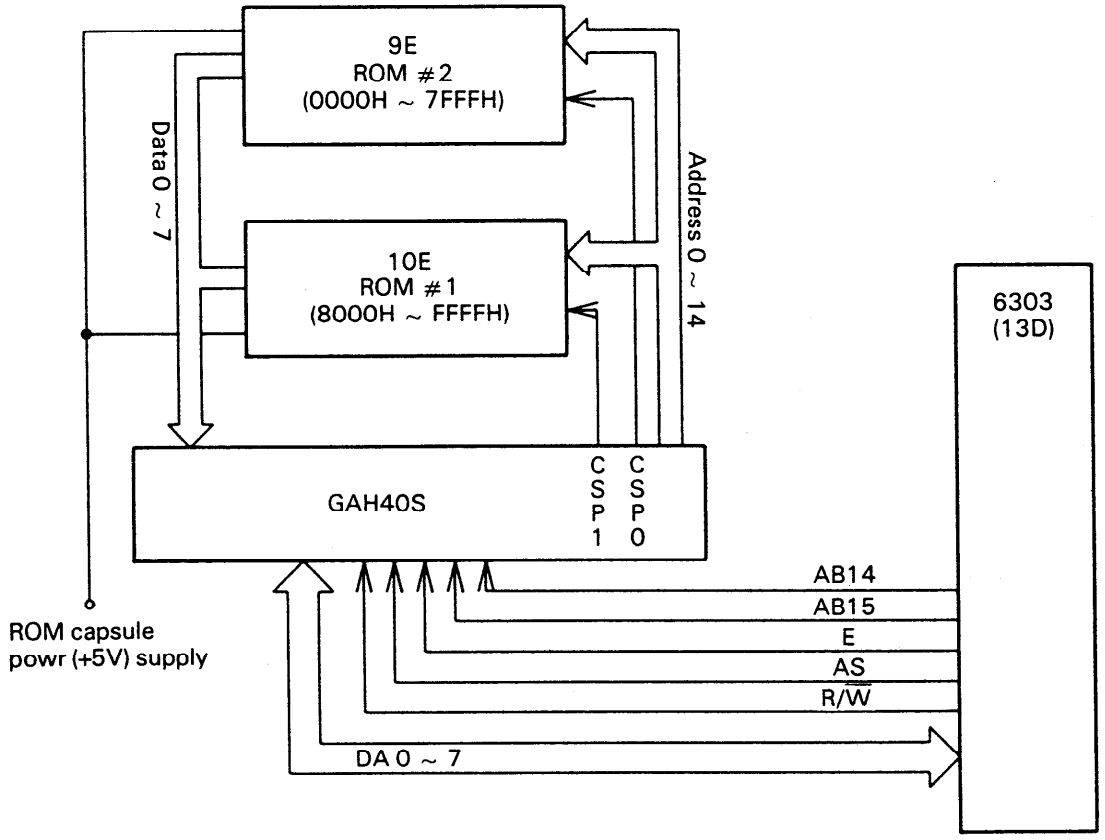


Fig. 2-98

2.10.1 Addressing

Two 2767 (8kB), 27128 (16kB), or 27256 (32kB) ROM can be mountedto the ROM capsule and are accessed via the 6303 slave CPU as follows:

The ROMs are addressed using the data address lines DA0 through DA7. An address is therefore set in GAH40S in two parts. GAH40S has two 8-bit PROM address registers; High and Low, which can be directly accessed as an I/O address from the slave CPU.

The most significant bit (MSB) of this set of address registers is used to select either ROM #1 or #2 (i.e., serves as the chip select bit). Fig. 2-99 is a block diagram conceptually illustrating ROM capsule addressing.

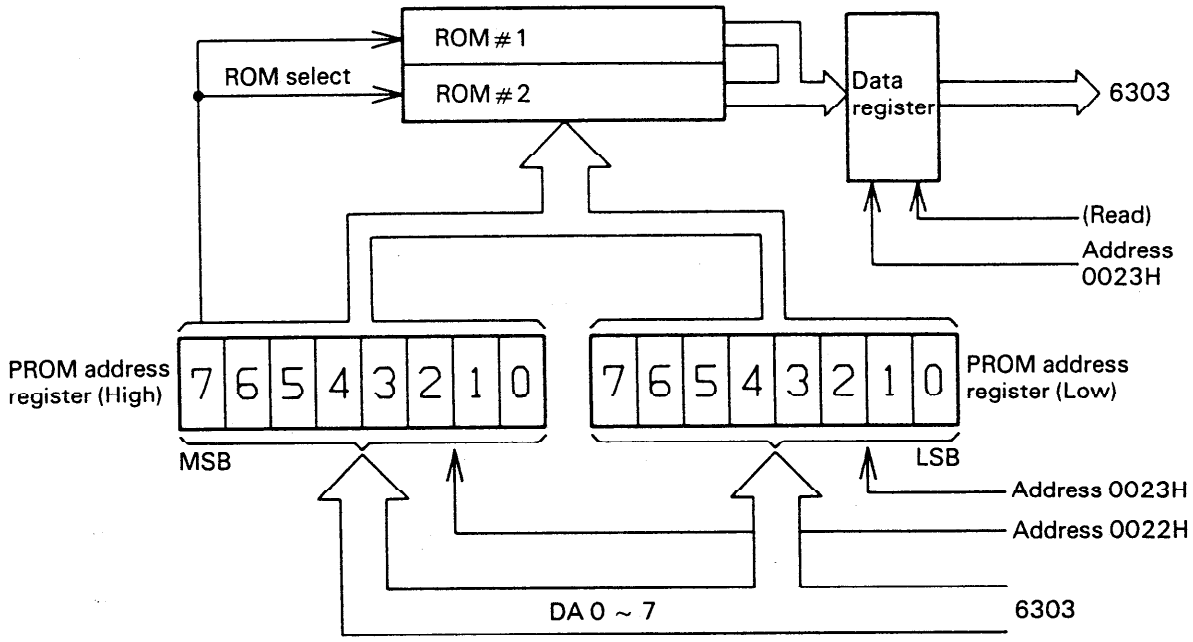


Fig. 2-99

ROM data is read by a read at I/O address 0023H from the 6303.

2.10.2 Power control

The +5V ROM power supply is controlled via, the 6303, by accessing the command register in GAH40S. The process is similar to the ROM data read. The SWPR signal, which turns the power supply on and off, corresponds to bit 0 of the command register (I/O address 0021H), which is under the direct control of the 6303.

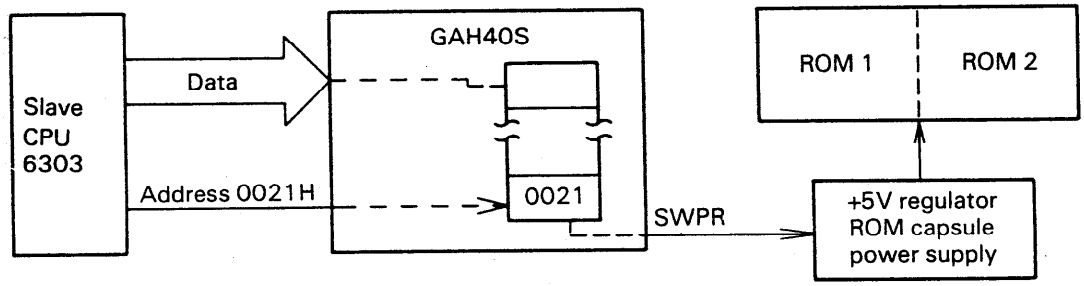


Fig. 2-100

This power supply is controlled using a 3-second timer and operates as follows:

(1) When power is off

The SWPR signal enables the voltage regulator. 50 ms later, ROM is read and the timer is triggered.

(2) When power is already on

ROM is read and the timer is triggered.

The above 3-second timer is used to enable the voltage regulator only during ROM read; the regulator is automatically disabled if ROM is not read within three seconds. ROM access is made efficient in cases where many ROM reads are repeated within a short period of time by eliminating the 50 ms wait time required for regulator stabilization. Fig. 2-101 illustrates an outline of the regulator control.

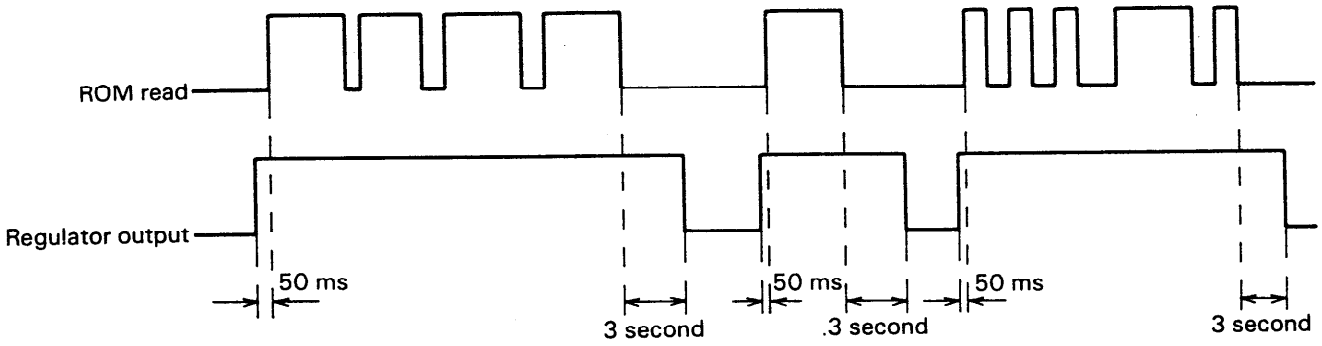


Fig. 2-101 ROM Power Voltage Regulator Control

2.10.3 ROM Data Format

It should be noted that the logical addresses (memory addresses as seen from the main CPU) and the actual ROM addresses do not completely match, as shown in Table 2-18. Logical addresses are used in the following descriptions on ROM data format.

Table 2-18

Logical address	ROM Address 2764 (8 kB)	27128 (16 kB)	27256 (32 kB)
0000 ~ 3FFF	0000 ~ 1FFF	0000 ~ 3FFF	4000 ~ 7FFF
4000 ~ 7FFF			0000 ~ 3FFF

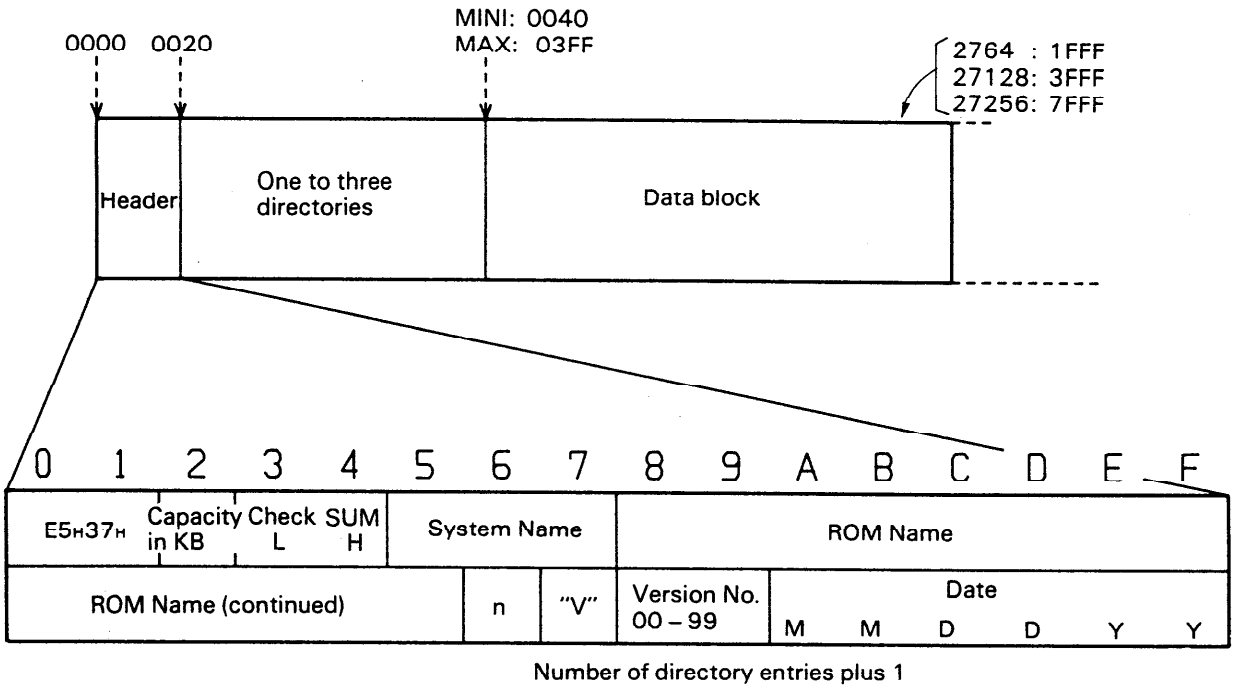


Fig. 2-102 ROM Data Format

- "E5" at the beginning of the header is the null code and has no special meaning. This null code is put here merely because the operating system deals with ROM as it would a floppy disk which always contains "E5". (The null code is written on all floppy disks when initialized.)
- "37" in the second header byte position indicates that the file is to be used with this computer.
- Two ROM capsules may be dealt with as a single floppy disk drive. By setting the most significant bit (NSB) of the third byte in the first ROM header (for lower address space) to 1, the entire second ROM capsule can be used as a data block.

2.11 RS-232C Interface

This interface is controlled by the programmable serial controller 82C51 (IC 2C). The interface requires special voltage supplies that meet the RS-232C standard. ±8V sources are provided from a DC-DC converter regulator which generates the voltages from the battery voltage (VB) under the control of IC 4C.

2.11.1 RS-232C levels

The RS-232C standard defines the space state as being between +25V and +3V inclusive, and the mark state be between –25V and –3V inclusive. This circuit uses the DC-DC converter to generate the voltage sources of ±8V from the battery voltage (+5V) for the RS-232C levels. Table 2-19 summarizes the relationship between the levels and data signals.

Table 2-19

Voltage Level	Data Signal	Timing Signal	State	Start/Stop Bit in Start-Stop System
+8V	0	On	Space	Start bit
–8V	1	Off	Mark	Stop bit

The interface circuit uses the receiver circuit shown in Fig. 2-103, which can receive up to maximum levels of ±25V.

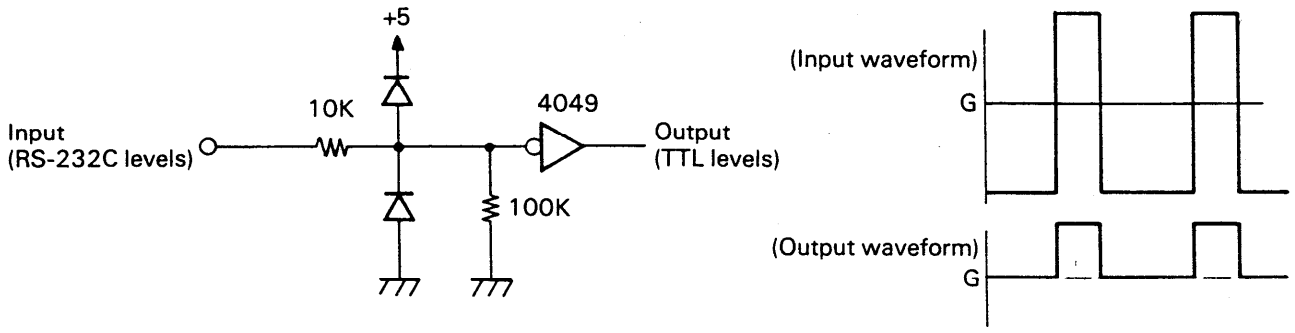


Fig. 2-103

The RS-232C input signal is converted to TTL level by the two limiter diodes after passing through the 10 kohm resistor.

REV.-A

A circuit diagram of the RS-232C interface circuit.

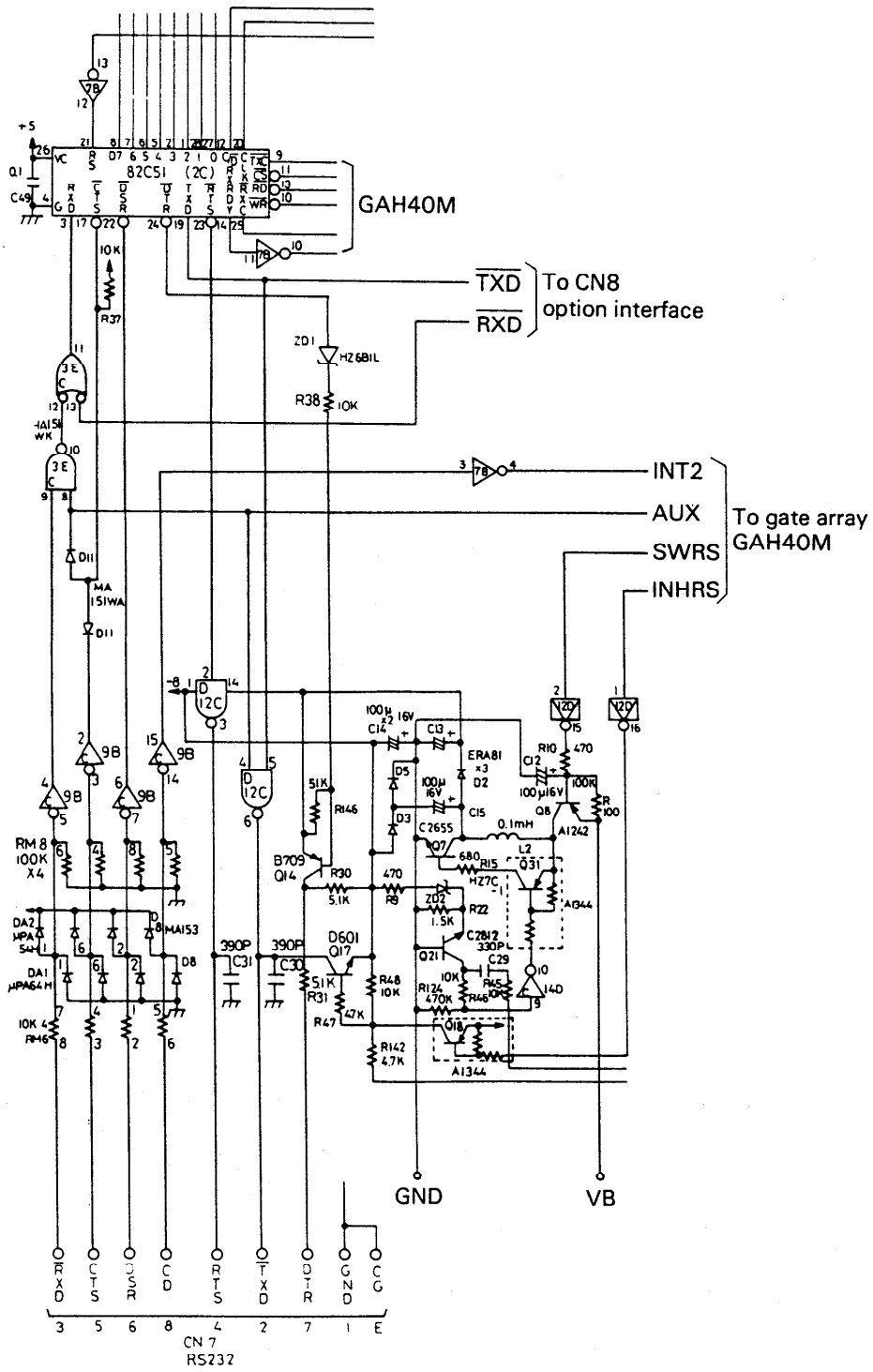


Fig. 2-104 RS-232C Interface Circuit

2.11.2 RS-232C Interface Circuit Operations

The base transmit/receive clock signal is supplied from GAH40M and data are converted from parallel to serial and vice versa at the same rate as the base signal; one sixteenth or one sixty-fourth of the base rate can be selected using the mode instruction register. The baud rate generator in GAH40M needs to be set to the desired rate before an RS-232C operation is initiated. The data read/write and interrupt are controlled by the main CPU and via the GAH40M.

2.11.2.1 Baud rate Generator Setting

The baud rate generator can be set by modifying bits 4 through 7 of the register, I/O address 00, through a write from the main CPU:

Table 2-20 Baud rate Generator Settings

Bit 7, Bit 6, Bit 5, Bit 4

BRG3	BRG2	BRG1	BRG0	TXC (8251 clock)	RXC	Baud 8251 Rate x 1/16		Baud 8251 Rate x 1/64	
						TX	RX	TX	RX
0	0	0	0	1.74545K	1.74545K	110	110	——	——
0	0	0	1	2.4K	2.4K	150	150	——	——
0	0	1	0	4.8K	4.8K	300	300	——	——
0	0	1	1	9.6K	9.6K	600	600	150	150
0	1	0	0	19.2K	19.2K	1200	1200	300	300
0	1	0	1	38.4K	38.4K	2400	2400	600	600
0	1	1	0	76.8K	76.8K	4800	4800	1200	1200
0	1	1	1	153.6K	153.6K	9600	9600	2400	2400
1	0	0	0	19.2K	1.2K	1200	75	——	——
1	0	0	1	1.2K	19.2K	75	1200	——	——
1	0	1	0	307.2K	307.2K	19.2K	19.2K	4800	4800
1	1	0	0	3.2K	3.2K	200	200	——	——

* For asynchronous transmission/reception (start-stop bit system), the transmit/receive clock rate is internally obtained by dividing the base signal down to one sixteenth or one sixtyfourth.

2.11.2.2. Data Read/Write

A read/write at I/O address 0C or 0D from the main CPU causes the Chip Select ($\overline{CS}$) signal and the Read ($\overline{RD}$) or Write ($\overline{WR}$) signal to be issued from the address decoder circuit in GAH40H. An I/O address AB0 is connected to pin 20 and dealt with as the C/$\overline{D}$ signal.

Thus, address 0D is used as the command address of the 82C51 and address 0C is used as the data address. Fig. 2-105 is a block diagram illustrating the read/write control flow.

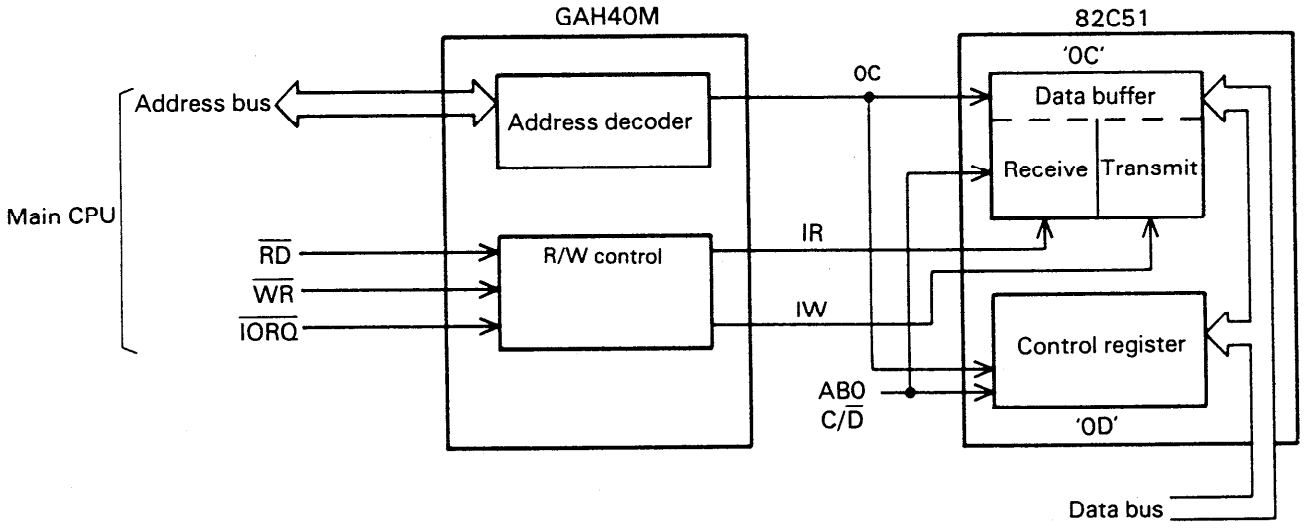


Fig. 2-105

* The transmit and receive buffers can hold only one byte each. Thus, the main CPU transfers data byte by byte.

2.11.2.3 Interfacing

The RS-232C and option unit signal lines are connected to the transmit and receive signal lines (RXD and TXD) and their input and output are controlled by the 82C51. To prevent the two input/output signals from interfering with each other, the input/output of the RS-232C signals is enabled and disabled by the AUX signal from GAH50M (which can be controlled by bit 5 of I/O address 02). Fig. 2-106 shows the control circuit.

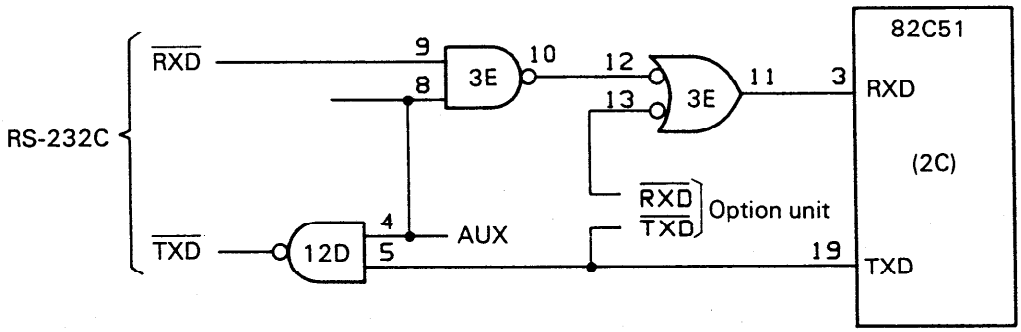


Fig. 2-106 RS-232C RXD and TXD Line Control Circuit

The AUX signal is supplied to pin 4 of IC 12D and pin 8 of the IC 3E. When this signal goes low, the two AND gates are disabled and the RS-232C interface is diactivated. And input/output from/to the option unit is possible. When the AUX signal goes high, the RS-232C interface is enabled and the option unit is deactivated.

2.11.2.4 Operation Timing

Handshaking of this interface varies depending on software specification. Fig. 2-107 illustrates the timing relationship among the interface operation signals.

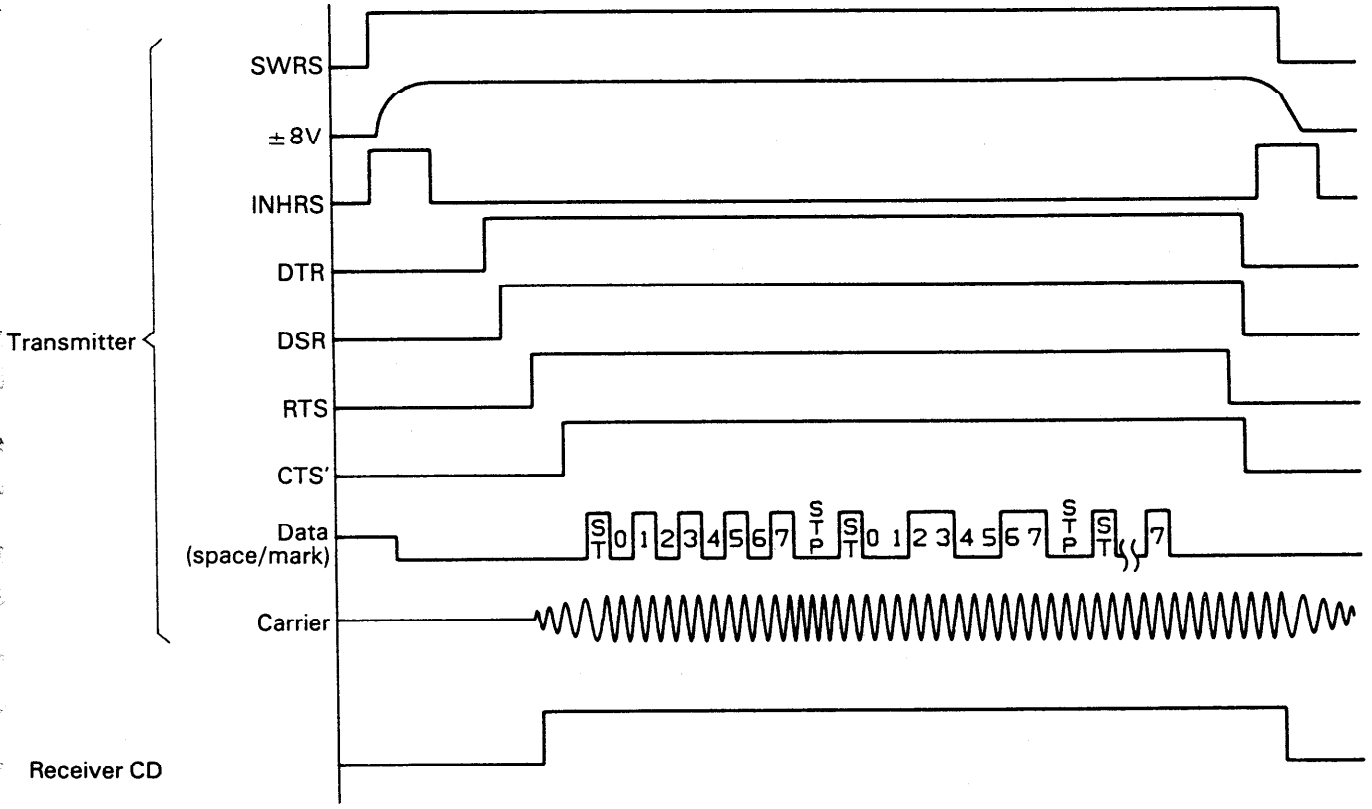


Fig. 2-107 RS-232C Interface Signal Timing Relationship

< Setting up for Communications >

The interface set-up operations are common to RS-232C transmitting and receiving . The SWRS signal from GAH40M first enables the ±8V regulator. At the same time, the INHRS signal is activated to prevent the regulator output from being supplied until it rises beyond a certain level and becomes stable. Then, the interface issues the DTR signal to check whether the connected modem is ready. If ready, the modem responds to DTR with the DSR signal and waits for the arrival of the RTS signal or carrier (CD). In the following discussions, either RS-232C interface can be transmitter or receiver.

< Transmission >

The transmitter interface issues the Request to Send (RTS) signal to its modem. This causes the modem to output a carrier over the communications line to put the receiver RS-232C interface in the receive state. After this, the modem returns the Clear to Send (CTS) signal to the transmitter interface. This causes the interface to initiate a serial data transmission. The modem modulates and transmits the data bits over the communications line.

< Reception >

The carrier, arriving over the communications line, is detected in the receiver modem after passing through a hand-pass filter. This state is informed to the receiver interface via the Carrier Detect (CD) signal. The interface assumes the Ready-to-Receiver state and the subsequently arriving data is demodulated by the modem and is read by the receiver interface. Fig. 2-108 illustrates the signal follow, including flow over the communications line.

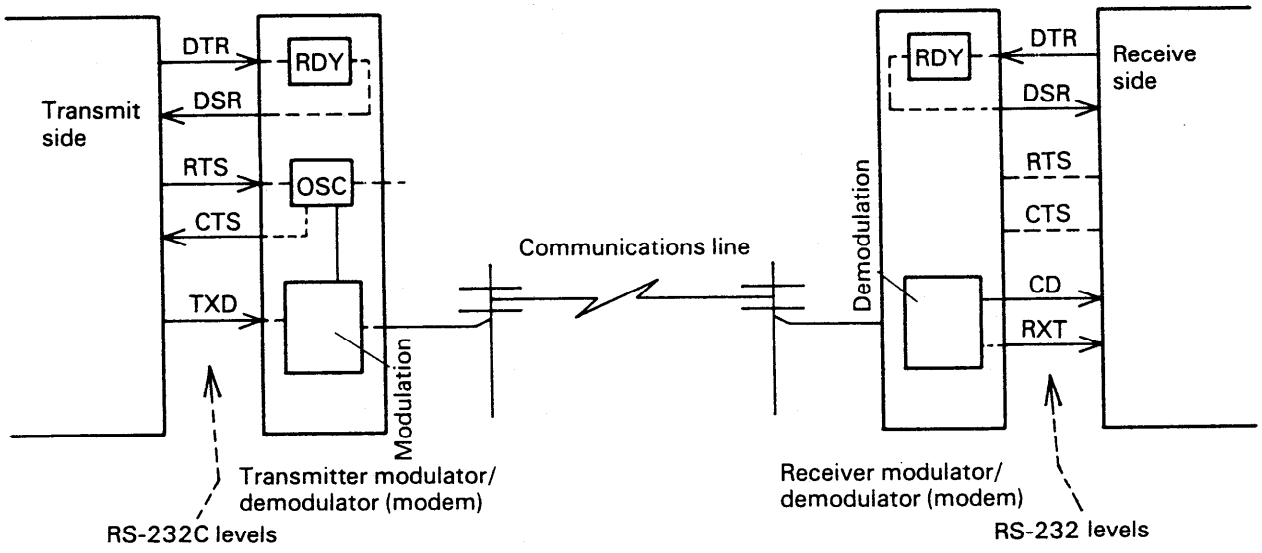


Fig. 2-108

2.11.2.5 Signal Level Conversion

An IC 75188 (USART) is inserted in two RS-232C interface output signal lines to convert the TTL levels to the RS-232C levels of ±8V.

A limiter circuit consisting of two diodes is used for the level conversion from RS-232C to TTL. Fig. 2-109 shows the individual circuits.

< Output signal lines >

There are three output signal lines; RTS, $\overline{TXD}$ and DTR. RTS and $\overline{TXD}$ are converted by the IC 12C (75188). DTR is normally pulled up to the –8V supply and it is driven to +8V only when $\overline{DTR}$ goes low.

< Input signal lines >

There are the four input signal lines; $\overline{RXD}$, CTS, DSR, and CD. These signals are converted by the limiter diode circuit shown in the figure. Mark (negative level) causes a current through the diode B, clamping the input to IC 4049 at the ground level. Space (positive level) causes a current through the diode A to the +5V supply, clamping the input at +5V.

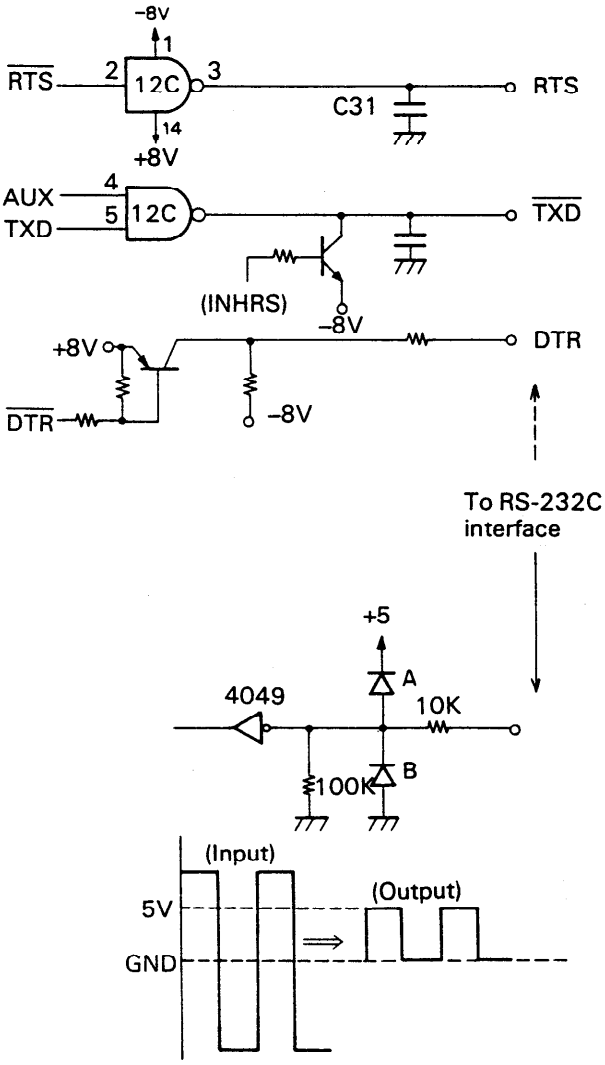


Fig. 2-109

* This interface circuit uses RS-232C levels of ±8V. The standards define the levels as follows:

- Mark – logical "1" (stop-bit level): –3V ~ –25V
- Space – logical "0" (start-bit level): +3V ~ +25V

2.11.2.6 Reception

The input interface line signals $\overline{RXD}$, CTS, DSR, and CD can always be read, regardless of whether power is on or off.

That is, the RS-232C interface supply voltage regulator needs not be turned on only for reception provided that the CD (DCD) signal is monitored with the DSR signal held high or the reception check is disabled.

- The 10 kohm current limiting resistor inserted on the receive signal line as shown in Fig. 2-110 protects the connected device from excess current or voltage drop. The next voltage limiter circuit, consisting of two diodes, and converts the RS-232C line levels from the mating transmitter to the 0/+5V TTL levels. The 100 kohm resistor pulls the limiter output down to ensure that the inverter IC 9B to functions properly.

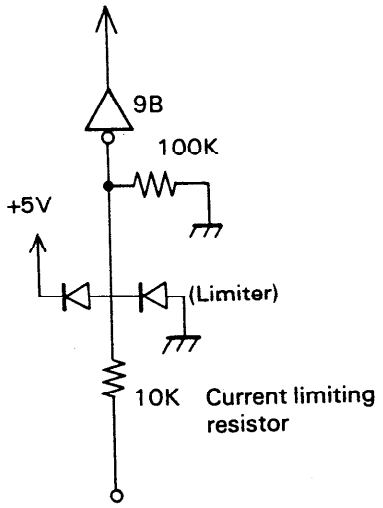


Fig. 2-110

2.11.2.7 Operation Mode Switching

The transmit/receive lines between the option unit (if connected) are connected to the transmit/receive data lines (TXD/RXD) between the serial controller 82C51 (2A), as well as to the those lines going to and from the RS-232C interface, as shown in Fig. 2-111.

These two pairs of lines cannot be controlled simultaneously. It is necessary to enable one either pair or no other. This is accomplished by the AUX signal, issued from gate array GAH40M. This signal is controlled by the main CPU using bit 5 of its I/O address 0002. When the bit is 0, the AUX signal is held low, disabling the transmit/receive data lines to/from the RS-232C interface at gates 3E and 12C respectively. When the bit is 1; i.e., the AUX signal is high, the data lines are disabled. Thus, the option unit data lines must be disabled at the option unit in order to prevent mixture of the signals.

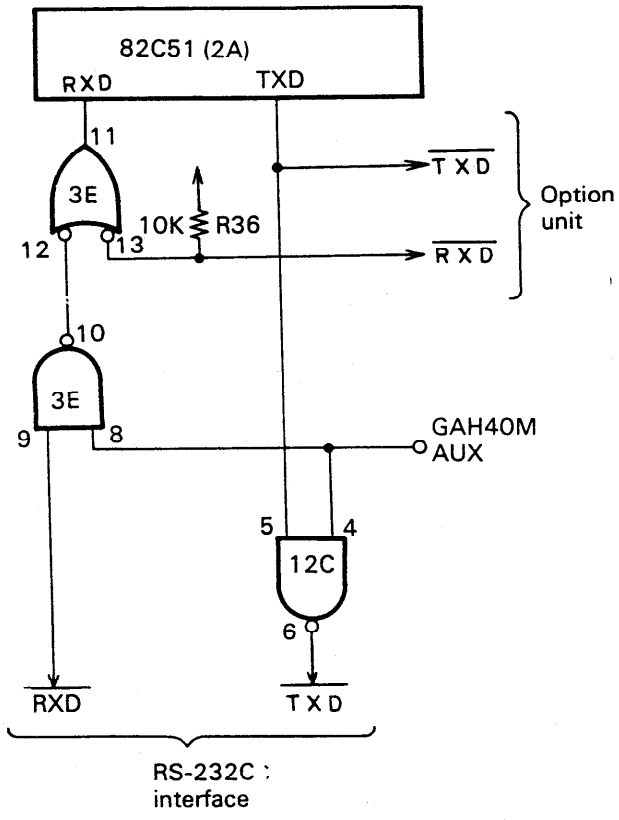


Fig. 2-111

2.12 Serial Interface

This interface is provided by using the serial port of the 6303 slave CPU. A baud rate is obtained by dividing the 614 kHz system clock supplied from the 6303 according to the command sent from the main CPU. Fig. 2-112is a circuit diagram of the serial interface.

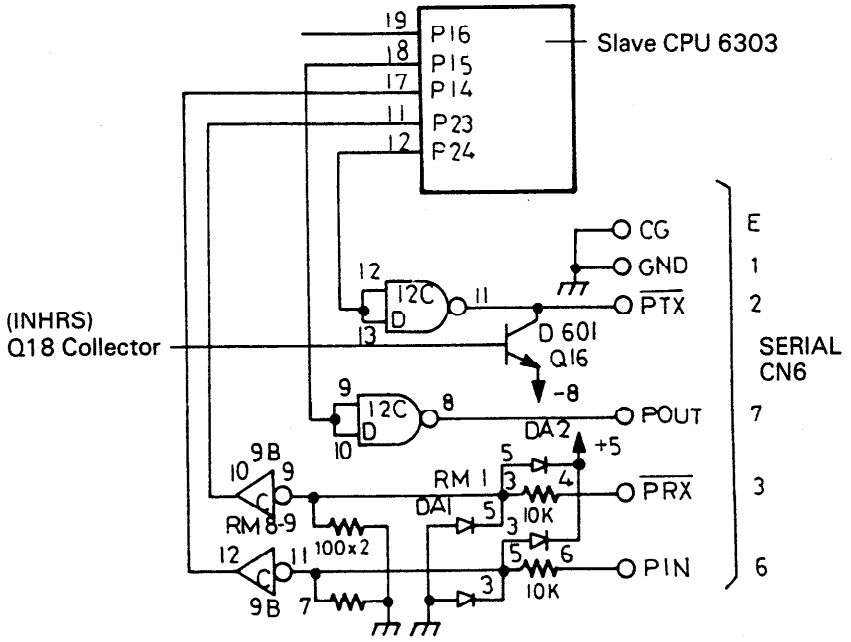


Fig. 2-112 Serial Interface Circuit

2.12.1 Power Supply

The driver (12C) and receiver (9B) circuits in this interface are the same as those used in the RS-232C interface. Thus, the same ±8V voltage regulator is required, which is also controlled by the gate array GAH40M. See paragraph 2.5.3 for details of the regulator operation.

2.12.2 Data Transmission Rate

A baud rate can be determined by varying the internal frequency division of the clock signal to the slave CPU (2.4576 MHz). One of four baud rates, 38.4K, 4800, 600, and 150 bps, can be selected. The baud rate selection is accomplished by rewriting slave CPU address 0010 (the Slave CPU transmission rate/mode control register) as shown in Table 2-21. (The original frequency of 2.4576 MHz is quartered within the slave CPU to the 614 kHz operating clock signal.)

Table 2-21 Option Unit Data Transmission Rate Selection

Address 0000		Frequency Division Ratio (Frequency Division to the Operation Clock Signal)	Transmission Rate	
Bit 1	Bit 0			
0	0	1/16	26μs	34800 bauds
0	1	1/128	208μs	4800 bauds
1	0	1/1024	1.67ms	600 bauds
1	1	1/4096	6.67ms	150 bauds

2.12.3 Interface

The signal voltage levels are the same meaning that used in the RS-232C interface, as shown in Table 2-22.

Table 2-22 Data Signal Voltage Levels

Voltage Level	Data Signal	State	Corresponds to Start or Stop Bit State.
+8V	0	Space	Start bit
–8V	1	Mark	Stop bit

- The Transmit ($\overline{PTX}$) signal line is controlled by the INHRS signal via transistor Q16 inserted across that line and the –8V supply. This is required to suppress the regulator output, preventing its rise time irregular voltage waveform from being recognized as a start bit by the connected device.
- The $\overline{PRX}$ and PIN signal lines have a 10-kohm current limiting resistor, a voltage limiter circuit, consisting of two diodes, and a 100 kohm pull-down resistor, as shown in Fig. 2-113.
  The current limiting resistor protects the connected device from overload and voltage drop.
  The voltage limiter converts the ±8V RS-232C levels to the 0/+5V TTL levels.
  The pull-down resistor ensures that the IC inverter to functions properly.

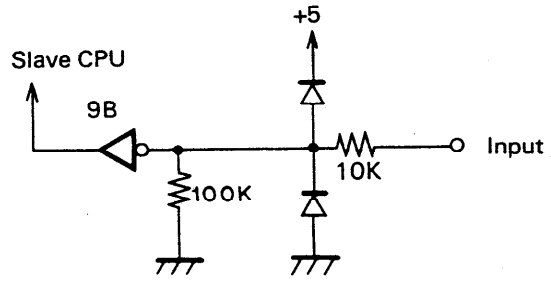


Fig. 2-113

2.12.4 Circuit Operation

The interface allows the following full-duplex data transmission between the computer and the connected device:

Number of start bits:	1 bit
Data length:	8 bits
Number of stop bits:	1 bit
Parity:	Not used.

The POUT and PIN signals, which respectively, indicates whether the computer (or the connected device) is in the transmit or receive state. However, these signals will rary depending on the connected device and/or the application program used in the computer. See Fig. 2-114.

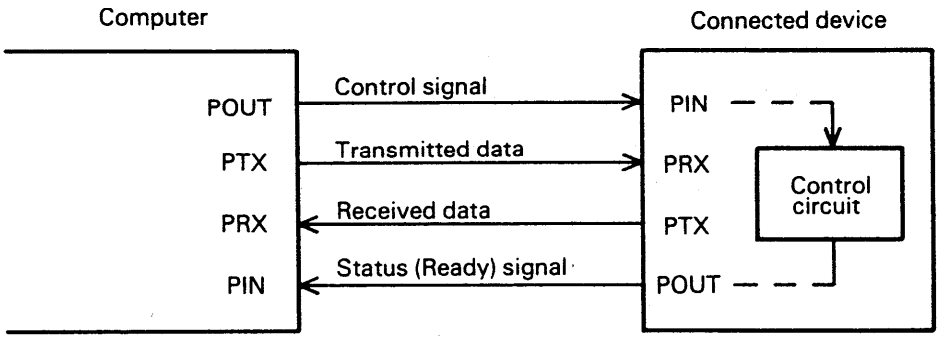


Fig. 2-114 Serial Interface Signals

2.13 Speaker Circuit

A cone speaker is built in on the back side of the MAPLE board. An external speaker can be also connected as required.

(1) Input signal

The following three signals are input to the speaker circuit:

- Microcassette read signal – may be a sound source.
- Slave CPU 6303 output.
- Expanded interface SPI signal.

(2) Output control

The output to the speaker is controlled by the slave CPU 6303 via its port 17 as follows:

Port 17 level	Control
High	Enables the speaker circuit.
Low	Disables the speaker circuit.

- The output level to the speaker can be adjusted by a variable resistor.
- The internal speaker is automatically switched to the external speaker when the speaker cord jack is connected with CN11.

(3) Speaker

The built-in speaker is a 200 mW, 8 ohm cone speaker with a frequency range from 600 Hz to 10,000 Hz.

Note: The BEEP command can specify up to 2500 Hz.

2.13.1 Circuit Operations

The speaker circuit includes an operational amplifier (NJM 386, 8B) whose operation voltage is controlled by the slave CPU 6303 via port 17. When port 17 is at the high level, the operational amplifier is activated. See Fig. 2-115.

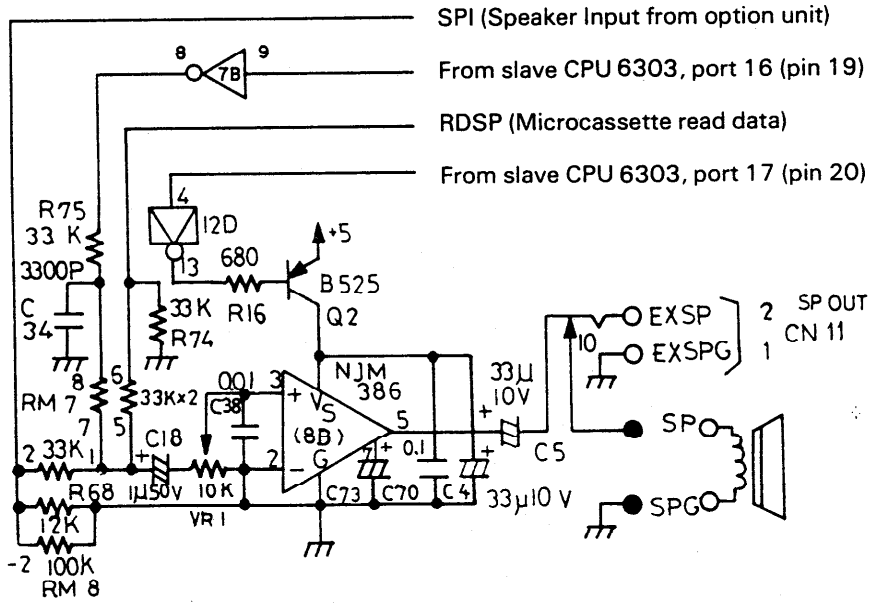


Fig. 2-115 Circuit Operations

When the operational amplifier is activated, the SPI, RDSP, and slave CPU output signals are fed to the non-inverted input terminal (pin 3) of the amplifier through the respective resistors and the capacitor C18, are amplified and the output is obtained at pin 5.

The inverted input terminal (pin 2) is grounded. When the voltage at the negative pole terminal of C18 deviates from the ground level, therefore, the voltage divided by the variable resistor VR1 is supplied to the non-inverted input terminal (pin 3) and amplified.
C18 is inserted to reject the DC component of the incoming signals.

2.13.2 System Outputs to Speaker

Any one of the sounds listed in Table 2-23 can be output to the speaker(s) from the system via the BASIC SOUND command, e.g., /n the application program.

Table 2-23 System Outputs to Speakser

Occasion	Sound
Power on in Restart mode	One short sound of selected frequency
Power on in Continue mode	One long sound of selected frequency
Before password entry	One "peeroe"
Alarm/wake while power off	Three "peeroes"
Alarm/wake display	Three "peeroe"

The buzzer is sounded by a combination of the above sounds.

Example: When the computer enters the Restart mode at the Wake time while power is off.
Three "peeroes" and one short sound of the selected frequency occur.

Ovserved Speaker Output Signal Waveforms

(Top) RD – Measured at IC3, pin 1.

(Bottom) RDSP – Measured at CN1, pin 5.

* Adjusts the volume control variable resistor VR1 at the middle when playing back AZIMUTH tapes.

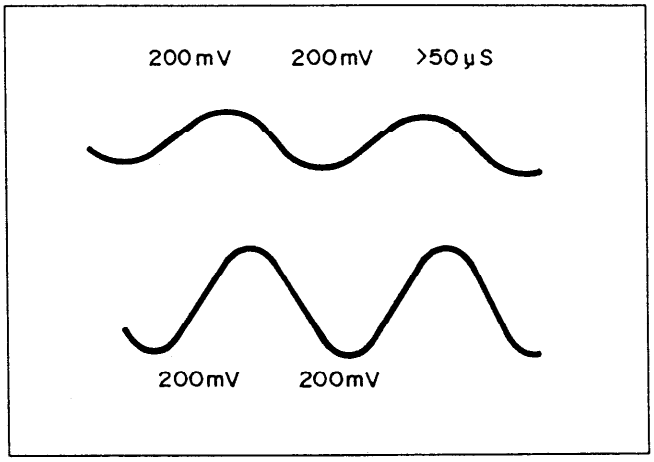


Fig. 2-116

When the variable resistor VR1 is set minimum, the RDSP signal has almost the same phase as the output signal at IC3, pin 1. However, its phase amplitude decreases as VR1 resistance increases.

2.14 Dynamic RAM

As shown in Fig. 2-117, eight address lines, one data input, and one output line are connected to the D-RAM, which is controlled by four signals; W, $\overline{RAS}$, $\overline{CAS}$, and $\overline{RF}$.

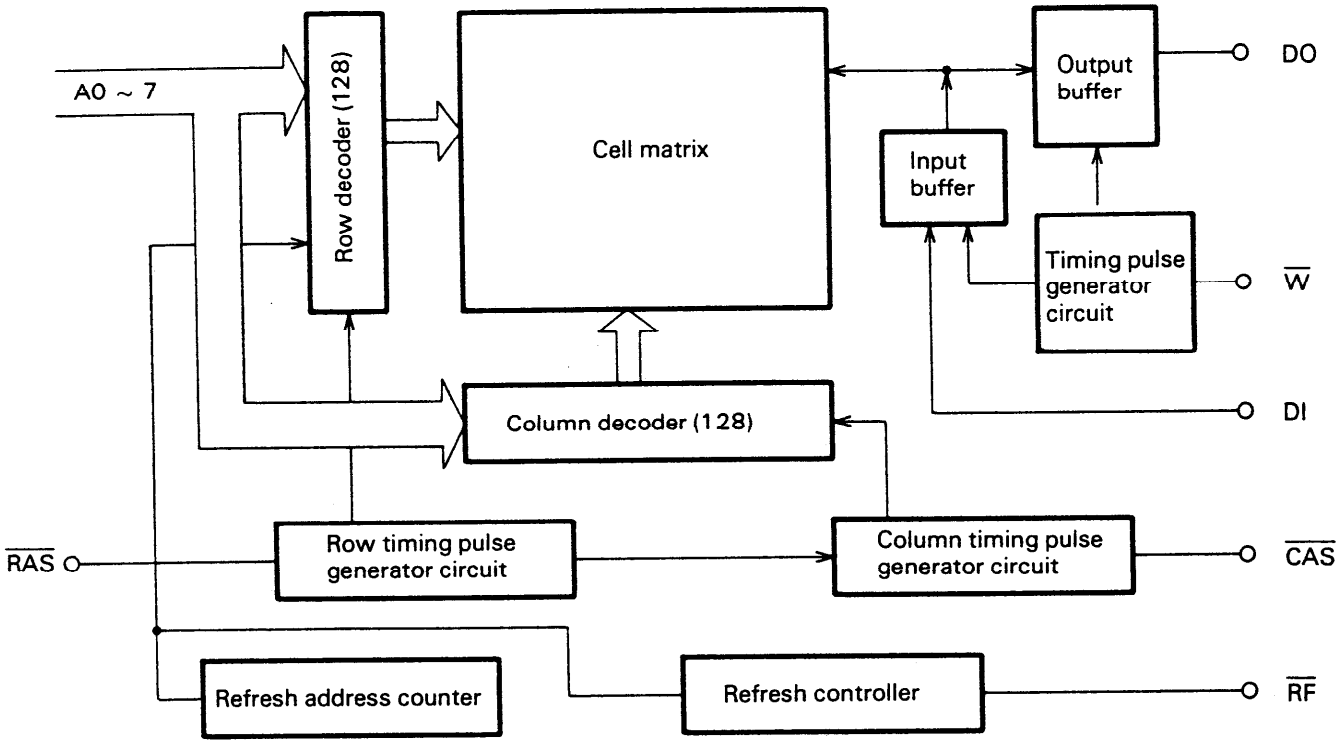


Fig. 2-117 D-RAM Control Functional Block Diagram

<Address lines>

Each D-RAM chip has a capacity of 64k bits, permitting only eight lines to be addressed at a time. Therefore, GAH40D sends the upper and lower eight bits of the 16 bit address lines from the main CPU separately. This adress mode is illustrated in Fig. 2-118.

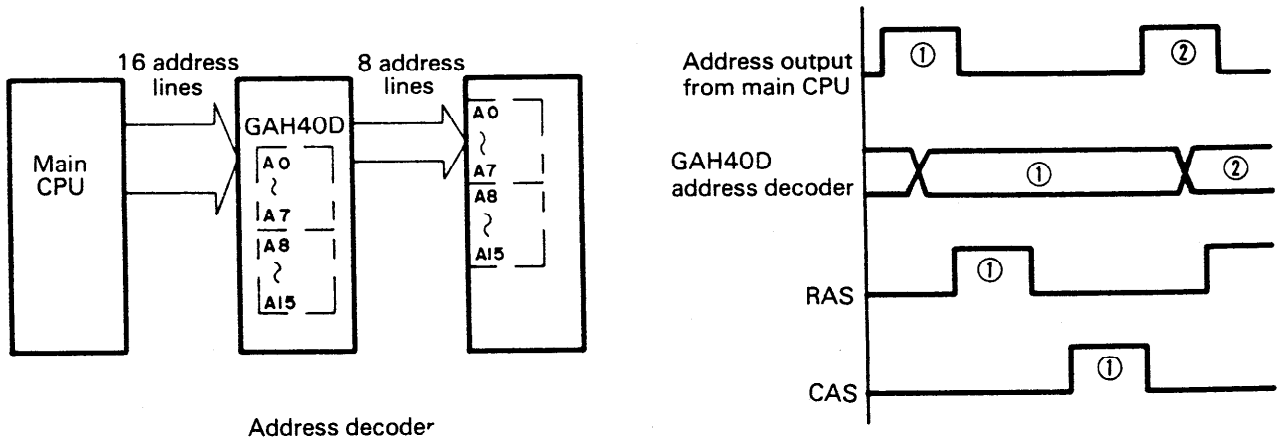


Fig. 2-118 D-RAM Addressing Control

2.14.1 D-RAM Accesses

The D-RAM is read/written and refreshed via the gate array GAH40D. The D-RAM is a quasi C-MOS product (the output section is built with C-MOS and the internal circuitry uses N-MOS), which requires a relatively large amount of operating current. Consequently, a power-saving feature is provided, which selects a minimum safe refresh current, depending on ambient temperature.

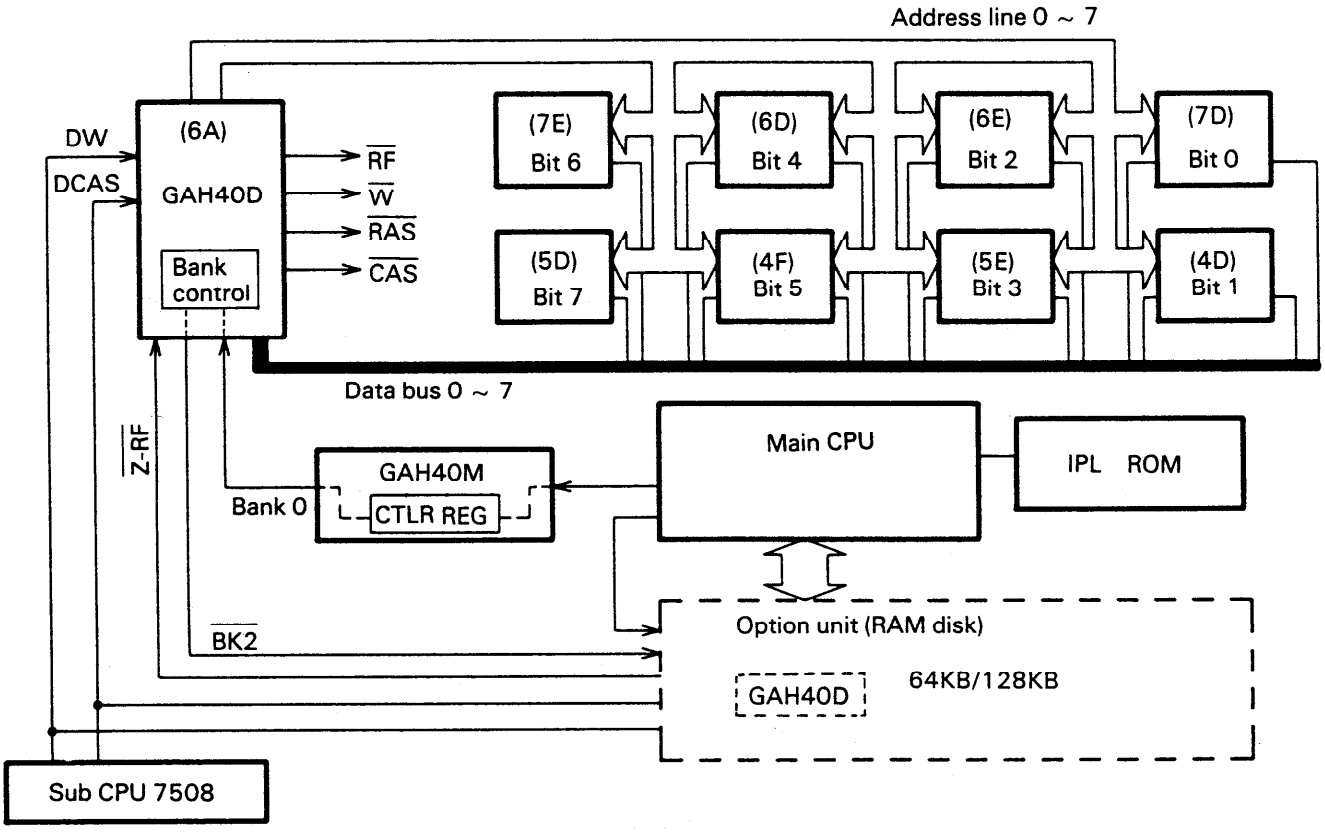


Fig. 2-119 D-RAM Configuration

An external 64kB or 128kB D-RAM memory can be expanded as an option unit, which can also be battery-backed up, as shown in Fig. 2-119; the refresh signals DW and DCAS are also supplied from the sub-CPU 7508 to the option unit.

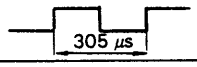
2.14.2 D-RAM Refresh by Sub-CPU

The D-RAM refresh feature is enabled whenever the D-RAM is not being accessed by the main CPU. The feature refreshes the D-RAM using two signals: DW and DCAS. Refresh is performed in one of three modes, automatically selected depending on ambient temperature.

1) Operation modes

The Sub-CPU 7508 monitors the ambient temperature, which is read as a resistance variation of a thermistor connected to channel ANO of the A-D converter 7001, and an internal control program determines one of three predetermined temperature ranges into which the read valu falls. The sub-CPU sets the states of ports 72 and 73 according to the selected temperature range. The range is indicated to the gate array, GAH40D, which internally generates two refresh control signals $\overline{CAS}$ and $\overline{WE}$, and supplies them to the D-RAM chips. Table 2-24 summarizes the relashionship between the modes and the control signals.

Table 2-24 D-RAM Refresh Mode and Contrl Signals

Refresh mode	Ambient temperature range (°C)	Control signals to D-RAM		Control signals from 7508 to GAH40D	
		$\overline{CAS}$	$\overline{WE}$	$\overline{DCAS}$	$\overline{DW}$
TH	45 ~	H	H	0	0
TM	25 ~ 45	H	L	0	1
TL	0 ~ 25	L		1	1

2.14.3 D-RAM Refresh by Main CPU

The main CPU refreshes the D-RAM by issuing the lower serven refresh address bits and the $\overline{MREQ}$ and $\overline{RF}$ signals after each operation code fetch during the M1cycle. The actual waveforms of the related signals are shown in the following:

Observed signal waveforms

$\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ signals

(Top) $\overline{\text{RAS}}$ signal – measured at IC 6A, pin 17

(Bottom) $\overline{\text{CAS}}$ signal – measured at IC 6A, pin 44

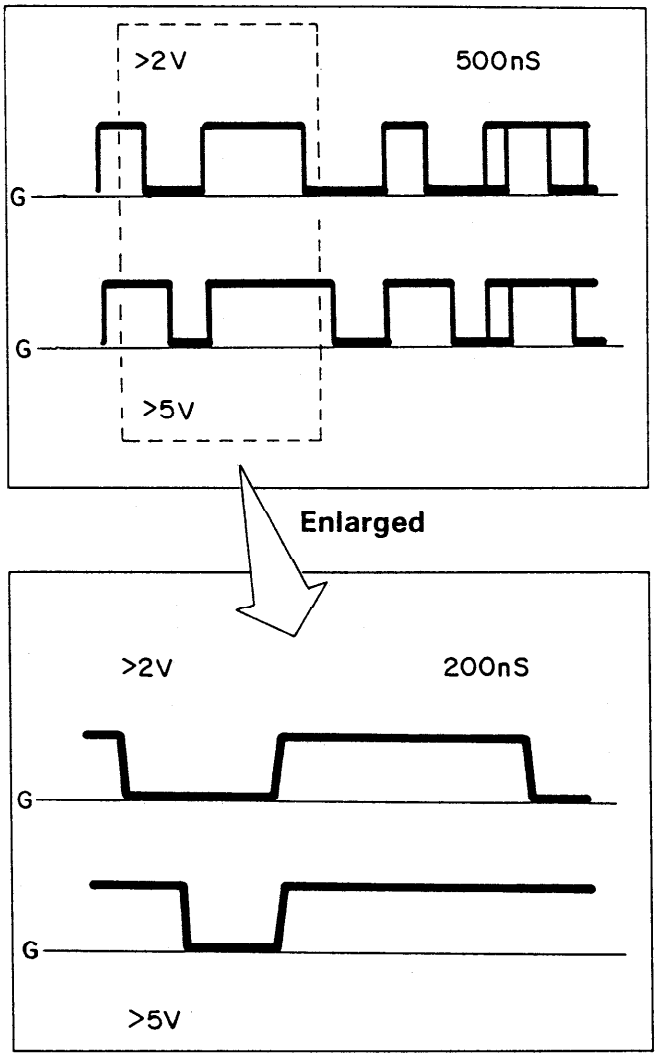


Fig. 2-120 $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ Signal Waveforms

Menu display

(Top) $\overline{\text{RF}}$ output – measured at IC 6A, pin 40

(Bottom) $\overline{\text{Z-RF}}$ input – measured at IC 6A, pin 29

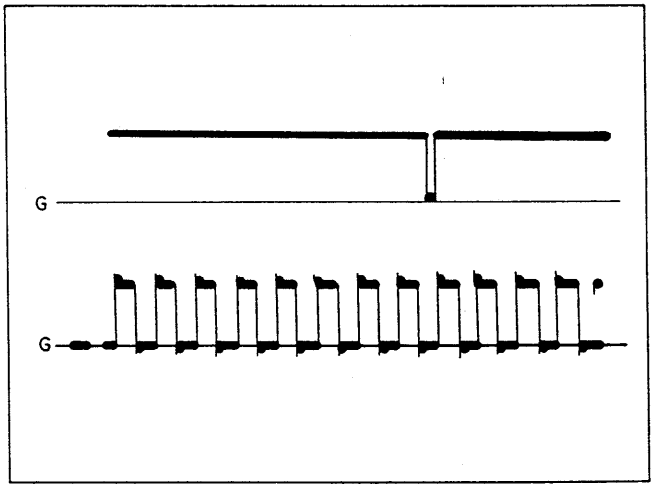


Fig. 2-121 $\overline{\text{Z-RF}}$ and $\overline{\text{RF}}$ Signal Waveforms During Menu Display

Read/write

(Top) $\overline{\text{RF}}$ ouput – measured at IC 6A, pin 40

(Bottom) $\overline{\text{Z-RF}}$ input – measured at IC 6A, pin 29

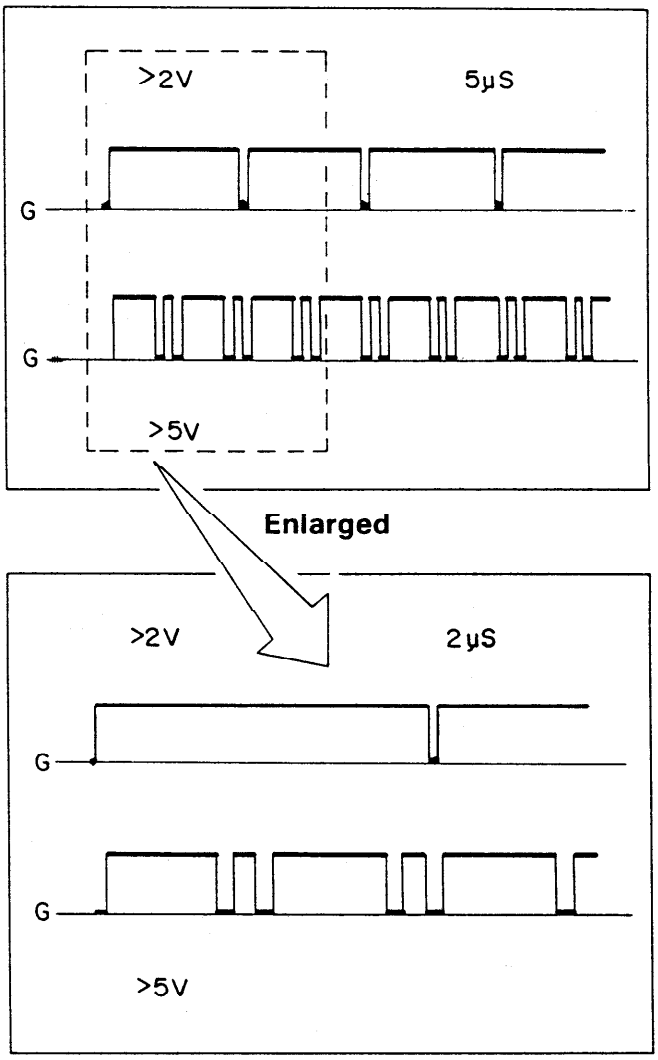


Fig. 2-122 $\overline{\text{Z-RF}}$ and $\overline{\text{RF}}$ Signal Waveforms During Read/Write

REV.-A

— MEMO —

CHAPTER 3
OPTION
(PRINCIPLES OF OPERATIONS)

3.1 Microcassette

The microcassette tape is controlled by the 6303 slave CPU. The unit requires a comparatively large power supply because of the mechanical functions it performs. It is powered only when used. Fig. 3-1 is a block diagram illustrating signal flow to and from the microcassette.

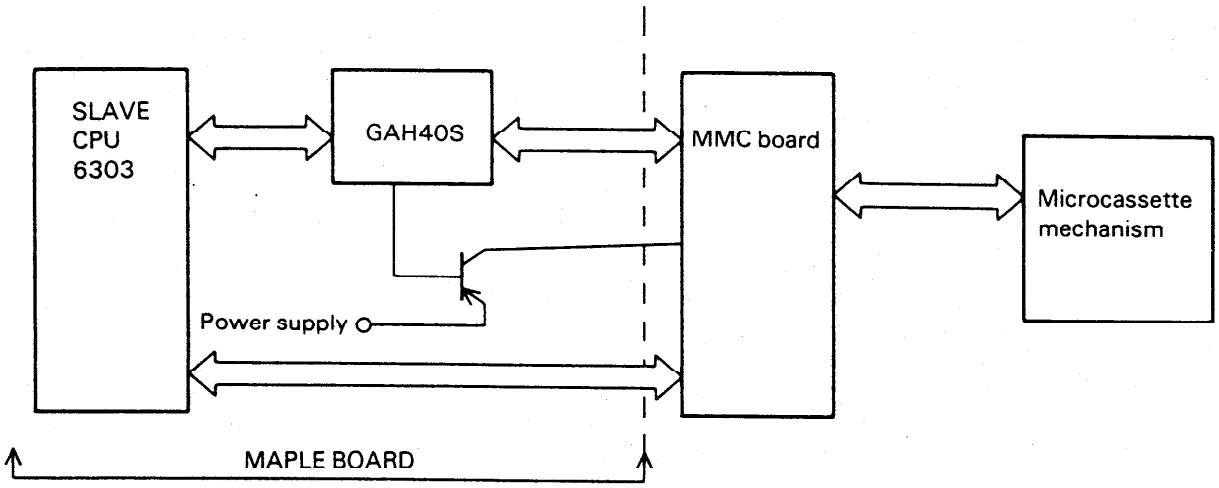


Fig. 3-1 Microcassette Tape Operation Control Block Diagram

3.1.1 Slave CPU Functions

The 6303 slave CPU directly controls all microcassette tape operations using the following signals:

- HSW: Indicates the current position of the read/write head (LOAD/ UNLOAD).
- WE: Indicates whether the microcassette is write-enabled.
  (detects the presence of the microcassette write inhibit tab).
- ERAH: Erase signal.
- HMT: Head pinch motor drive signal.
- D: Write data.

3.1.2 Gate Array Functions

The gate array issues or accepts the following signals under the control of the slave CPU:

MTA – MTC: Capstan motor drive control signal
CNTR: Tape count detection signal (photo-reflector detection signal)
RDMC: Read data
SWMC: MMC board and mechanism operation power control signal

3.1.3 Microcassette Tape Data Format

Data are recorded on a microcassette tape in blocks of 256 bytes and all cassette tapes are accessed in blocks. Fig. 3-2 illustrates the structure of a data block.

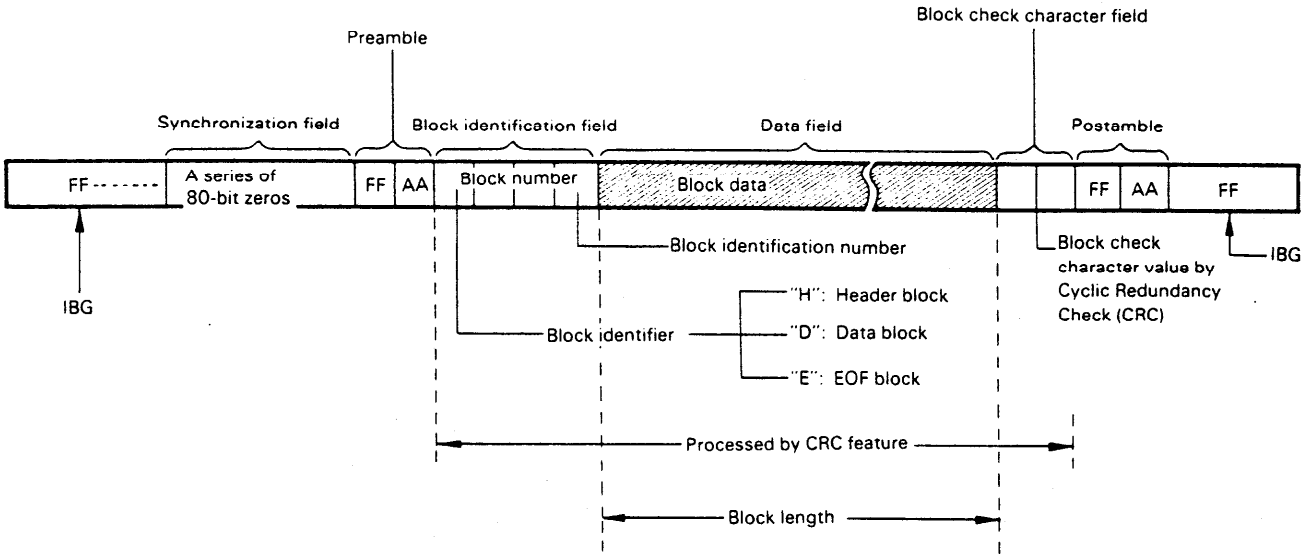


Fig. 3-2 Microcassette Tape Data Format

One tape reel (or one tape volume) consists of a directory and one or more files. The directory consists of three blocks; the first block contains identification data for the tape and directory and the second and third blocks contain control data for the files.

One file consists of a header block, one or more data blocks, and an end-of-file (EOF) block. Fig. 3-3 illustrates the general data structure of one reel.

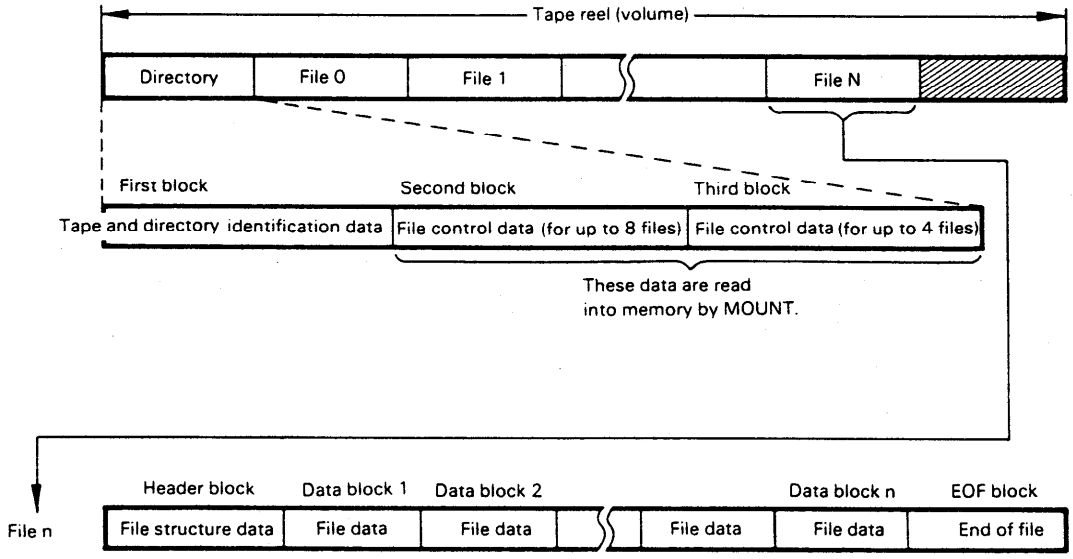


Fig. 3-3 Cassette Tape Reel Structure

3.1.4 Outline of Microcassette Mechanism

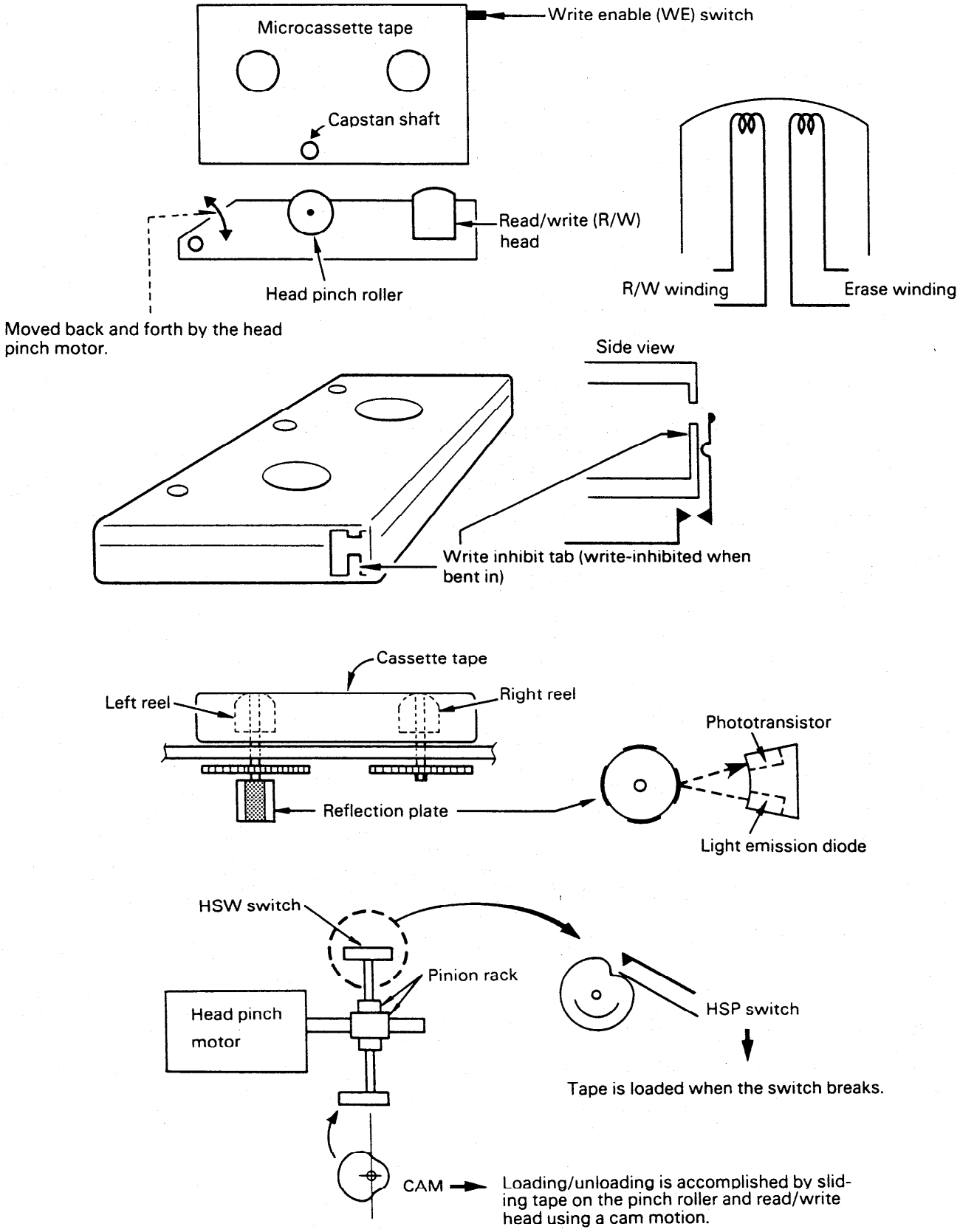


Fig. 3-4

3.1.5 MMC Board

The MMC board consists of two major sections, the motor drive control and read/write, which provide the following functions:

3.1.5.1 Motor Control Section

The motor control section occupies the upper half of the MMC board and controls the capstan motor and head pinch motor drive, and tape count detection. The individual circuits are discussed in the following:

(1) Capstan motor drive circuit

This circuit uses two ICs: IC1 and IC2. IC1 controls motor drive circuit switching and IC2 controls motor revolution speed.

- Motor drive circuit

Fig. 3-5 shows the internal circuit of IC1.

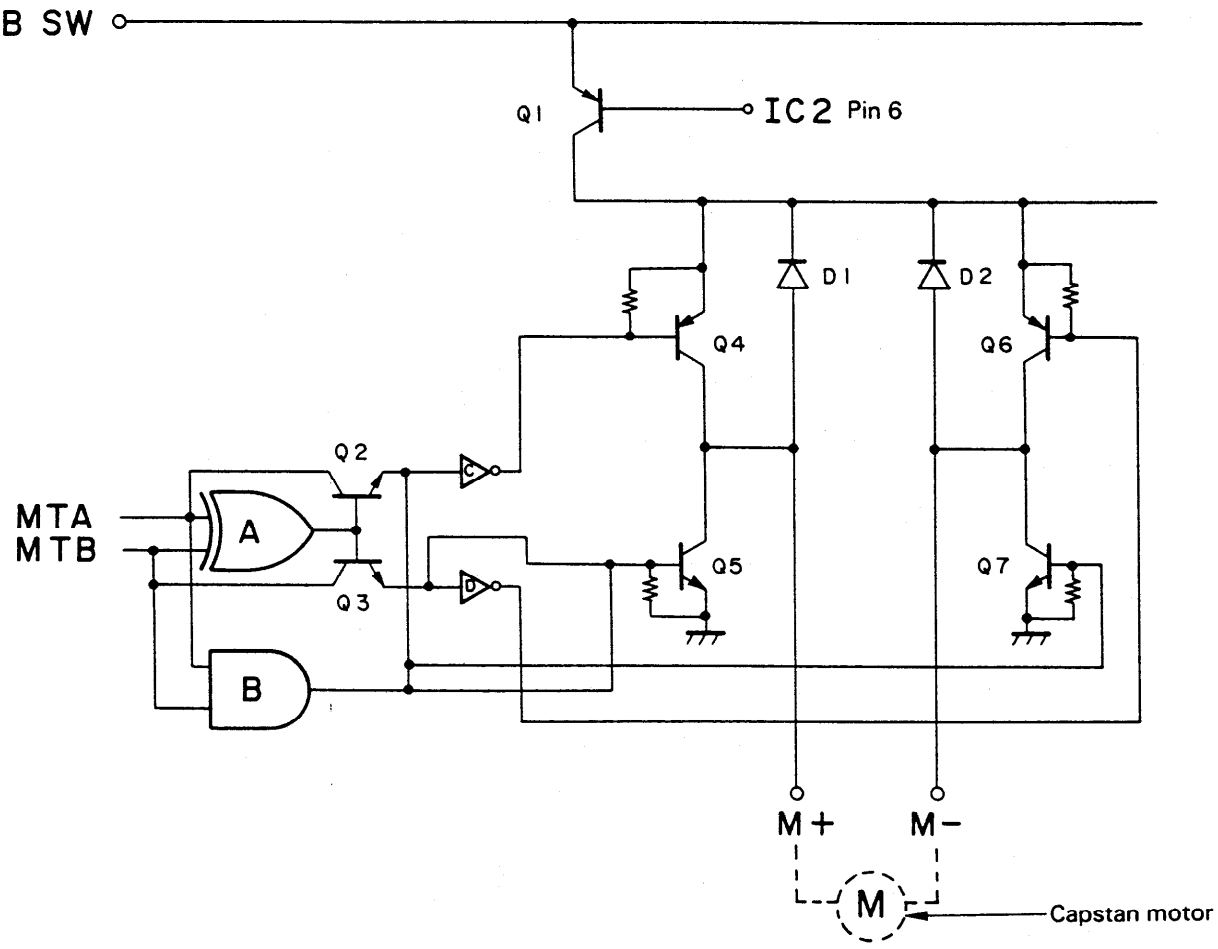


Fig. 3-5 Motor Drive IC Circuit

The circuit switches the polarity of the voltage applied to the capstan motor. Simplified circuit descriptions follow. While the actual circuit operation is more complicated, the basic operation is the same.

Table 3-1 Cassette Tape Operation Truth Table

Operation	MTC	MTB	MTA	Erase Head	Head Position
READ (Replay)	0	0	1	0	Load
WRITE (REC)	0	0	1	1	Load
REWIND (FAST)	1	1	0	0	Unload
REWIND (SLOW)	0	1	0	0	Unload
F.F. (FAST)	1	0	1	0	Unload
F.F. (SLOW)	0	0	1	0	Unload

MTA = High, MTB = Low

Since both the signals are supplied to the exclusive OR gate A, the base of the transistors Q2 and Q3 are held high, maintaining them in conduction. This causes the emitter of Q2 to be held high which in turn maintains transistor Q7 in conduction, holding the M- terminal of the capstan motor at ground level. The low signal inverted by inverter C turns transistor Q4 on which drives the external transistor Q1, supplying the VBSW voltage to the M+ terminal of the capstan motor. This results in a forward capstan motor drive which winds the tape. (The motor control transistors Q4 and A7 are in conduction.)

MTA = Low, MTB = High

Both Q2 and Q3 are in conduction similare to the above phase. However, the high level at the collector of Q3 maintains the transistor in conduction this time, causing the the M+ terminal of the capstan motor to be held at ground level. The low signal inverted by inverter D turns transistor Q6 and supplies the VBSW voltage to the M– terminal. This results in a backward capstan motor drive, which rewinds the tape. (The motor control transistors, Q5 and Q6, are in conduction.)

MTA = High, MTB = High

When both the signals are high, the low output of the exclusive OR gate A cuts off transistors Q2 and Q3, and no effective control signal can be output at the emitter of either transistor, but the high level output of AND gate B maintains transistors Q5 and Q7 in conduction, holding both the M+ and M– terminals of the capstan motor at ground level. (The motor control transistors Q5 and Q7 are in conduction.)

MTA = Low, MTB = Low

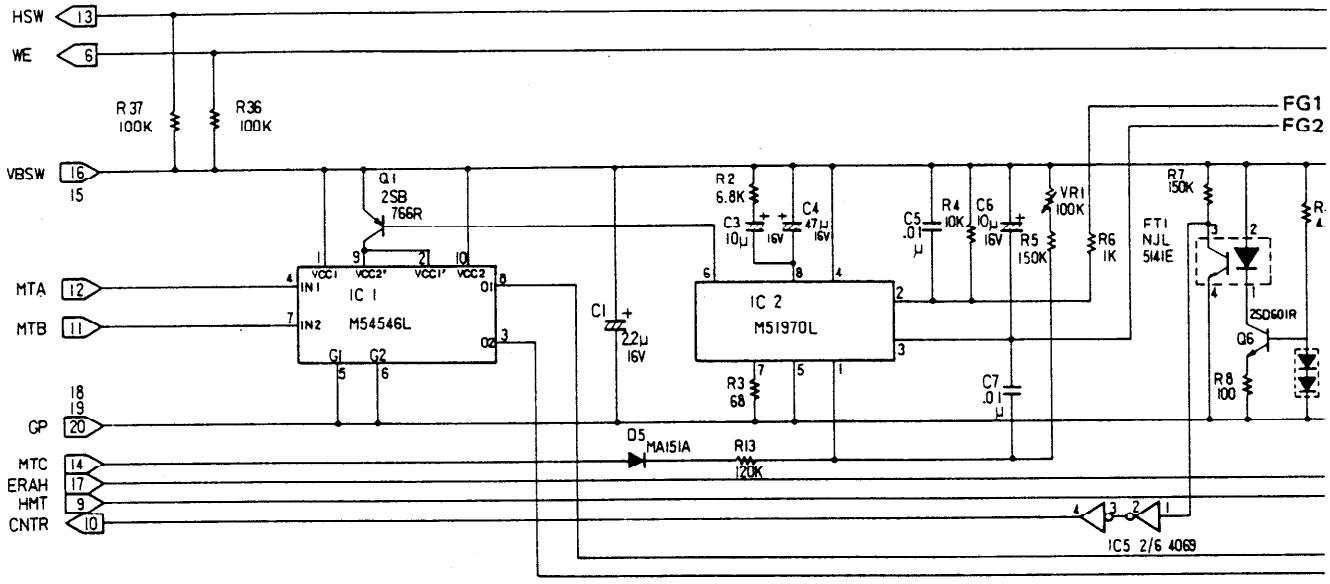


Fig. 3-6

3.1.5.2 Motor Revolution Speed Control Circuit

This circuit controls revolution of the capstan motor to ensure a cassette tape feed at a constant speed. Tape must be read/written at a speed of 2.4 cm/s. To secure this tape speed, the capstan motor must revolve at 2,400 rpm.

Because no tape speed control is desired during fast forward feed or rewind, a function which can enable or disable the tape speed control is also required. Fig. 3-7 is a block diagram of the internal circuit of IC2.

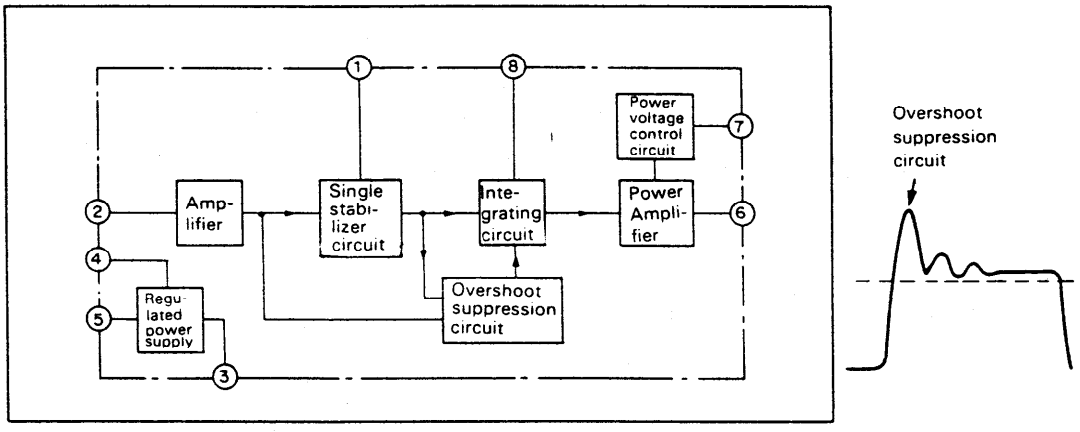


Fig. 3-7 IC2 Internal Circuit Block Diagram

The principle of the motor speed control can be illustrated by Fig. 3-8.

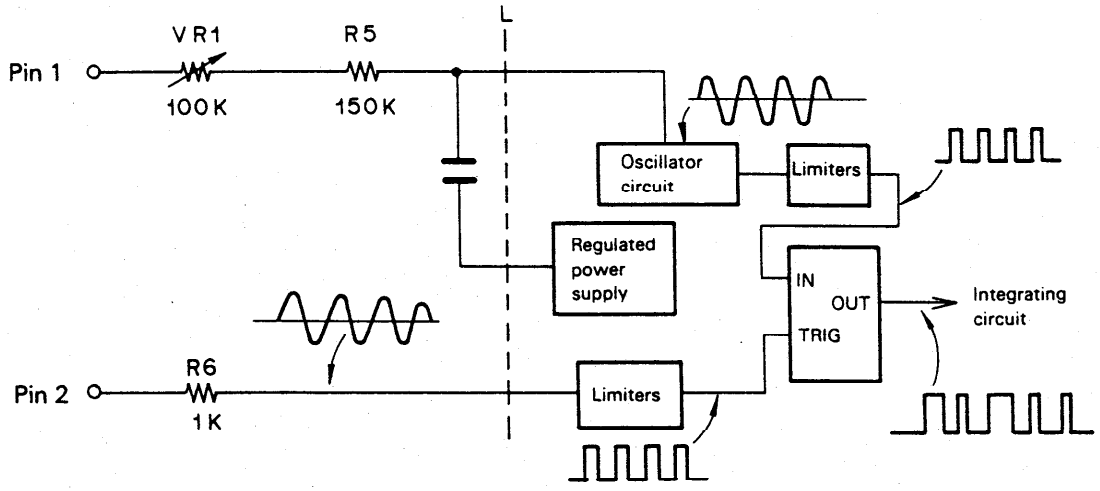


Fig. 3-8 Motor Speed Control Circuitry

Integrating Circuit

The IC output is a pulse signal as shown in Fig. 3-9. However, the capstan motor cannot be controlled by a pulse signal as the motor would oscillate. The IC output is integrated by the next stage integrating circuit, which uses the external capacitors C3 and C4. The pulse delay time (t) is determined by the capacitance of C4.

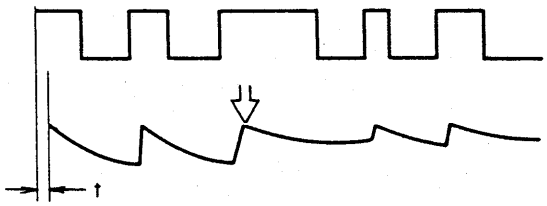
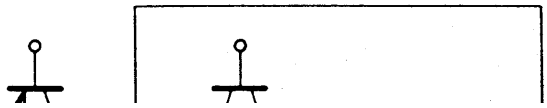


Fig. 3-9 Integrating Circuit

Current Control

The output current from the integrating circuit is amplified and the amplified current is limited to a proper value by the external resistor R3. Fig. 3-10 conceptually illustrates the principle.



3.1.5.3 Power Supply

Because IC 2 requires a negative voltage supply, pin 5 is grounded and pin 4 is connected to the VBSW voltage.

Input – Monostable Circuit

Motor speed control is accomplished by comparing the time constant determined by VR1, R5, and C7 with the frequency fed back from the capstan motor tachogenerator. The relationship between the time constant and the rpm of the capstan motor is as follows:

$$NP = \frac{1}{1.17 Rx\ C7}$$

$$2400 \cdot 10 = \frac{1}{1.17 Rx \cdot 0.01}$$

$$Rx = \frac{24 \times 10^3}{1.17 \times 0.01} \text{ ..... Approximately 205 k}\Omega$$

where N: rpm of capstan motor – 2,400 rpm
P: Number of tachogenerator poles – 10
Rx: Total resistance of VR1 and R5 (kohms)
C7: 0.01 uF (pF)

The specified speed should be attained by adjusting VR1 nearly at the center. The optimum frequency output from the tachogenerator, 400 Hz, is deviced as follows:

$$\frac{2{,}400 \text{ rpm}}{60} \times 10 \text{ (poles)} = 400 \text{ Hz}$$

3.1.6 Mechanism Control

3.1.6.1 Tape Count Detection

Tape count detection is accomplished by mirrors directly coupled to the left reel (the reel taking up tape during read/write) and a photo-reflector assembly (a single element which is a combination of a light emission diode and a phototransistor). Fig. 3-11 shows the circuit and the positional relationship between the elements.

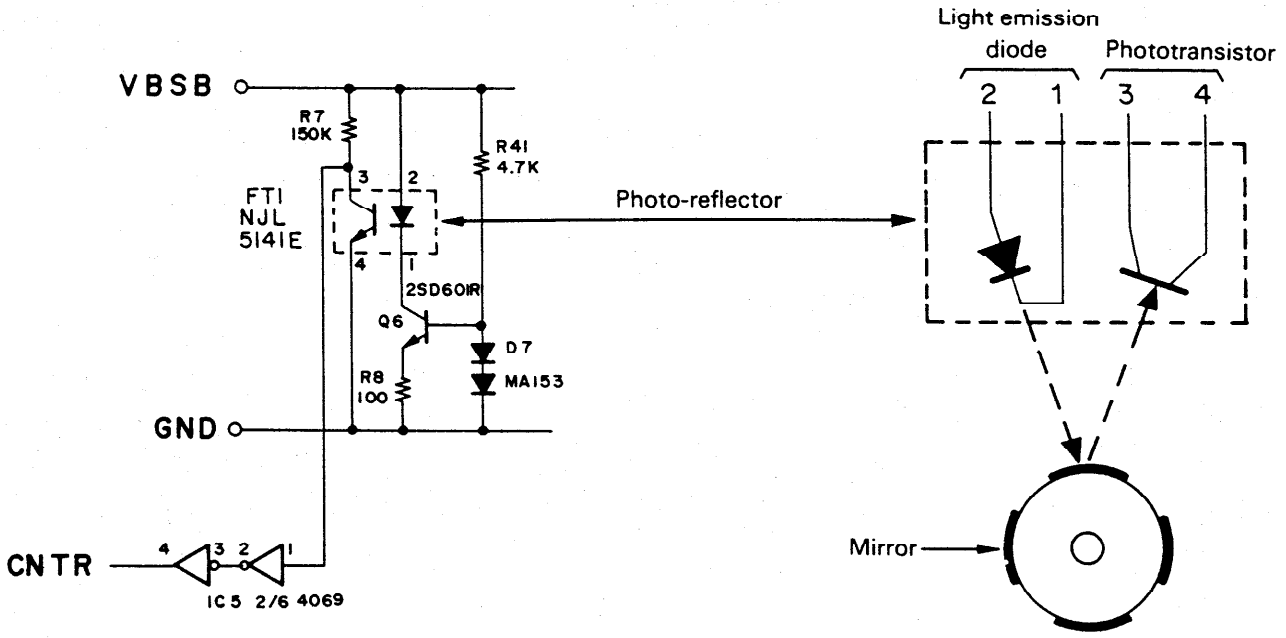


Fig. 3-11 Tape Count Detector Circuit and Positional Relationship between Elements

The reflector drum has four mirrors on it as shown in Fig. 3-11. One reel revolution is counted as four.

3.1.6.2 Head Pinch Motor Control

The head pinch motor moves the P-lever assembly consisting of the pinch roller and the read/write head. The assembly slides back and forth to accomplish tape loading and unloading. This motor always revolves in a direction and drives two cams; one is used to move the P-lever assembly back and forth and the other makes and breaks thc HSW switch, which detects the read/write head position. Fig. 3-12 shows the control circuit.

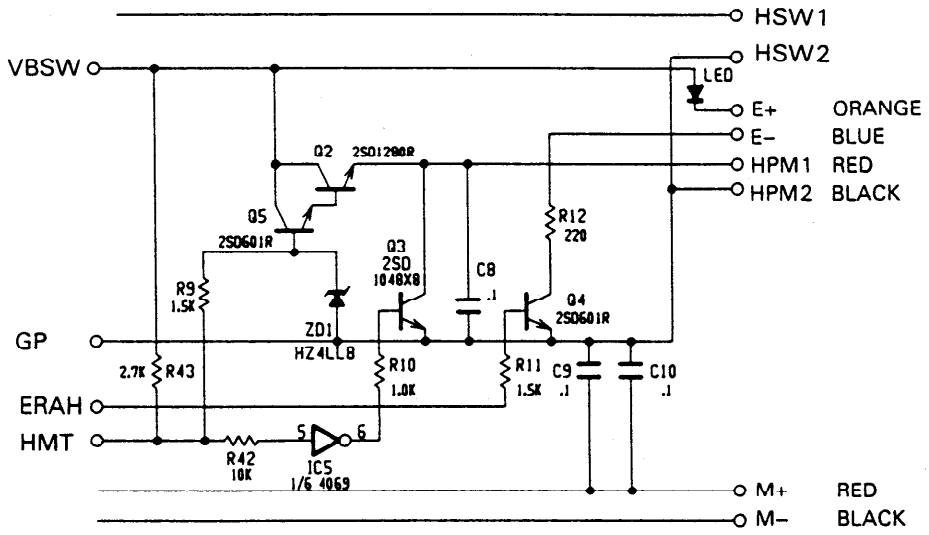


Fig. 3-12 Head Pinch Motor Control Circuit

When the HMT signal goes high, the transistors Q5 and Q2 are turned on and the VBSW voltage is supplied to HPM1 (the positive side terminal of the motor), revolving the motor which in turn causes the P-lever assembly to move back and forth.

When the HMT signal is turned low to stop the motor, the output of IC5 turns off and the output of pin 6 goes high, turns off transistors Q5, Q2, and turns on Q3. This causes the HPM1 line to be shorted to ground, and applies a brake to the motor, preventing revolution by inertia. If the motor continued revolving by inertia, the read/write head position and the pinch roller's contacting pressure against the capstan shaft would deviate from the specifications, and such failures as read/write error would occur.

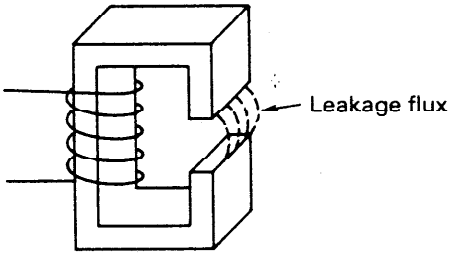
The zener diode ZD1, connected at the base of Q5 maintains the voltage supplied to the motor below the VBSW voltage (approximately 5V). – (A higher motor drive voltage would increase the motor inertia as described above.)

3.1.6.3. Erase Circuit

When the ERAH signal is activated low, transistor Q3 is turned on. This causes a current from the VBSW line to ground passing through the erase winding of the read/write head, and erasing previously written tape data. This circuit operates only during write.

Read/Write Head Structure

Both the read/write and erase heads make use of leakage flux.



Data are actually written on the tape at the copre slit where leakage flux is generate.

Fig.3-13 Read/Write Head Structure

3.1.7 Read/Write Control Section

The read/write control is located in the lower half of the MMC board and consists of a read and write circuit. However, most of the section is actually occupied by the read circuit operational amplifier.

3.1.7.1 Write Circuit (Erase and Write)

Magnetic tape write is accomplished using leakage flux as illustrated above. A logical value of 0 or 1 can be written on reversing tape by reversing the direction of the flux; i.e., the direction of the current through the write head winding.

This circuit reverses the write current direction by means of charging and discharging an electrolytic capacitor. Thus, the current waveform theoretically looks as shown in Fig. 3-14.

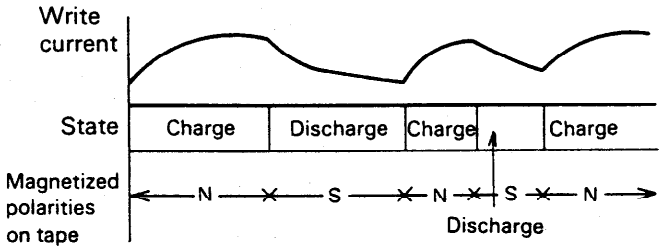
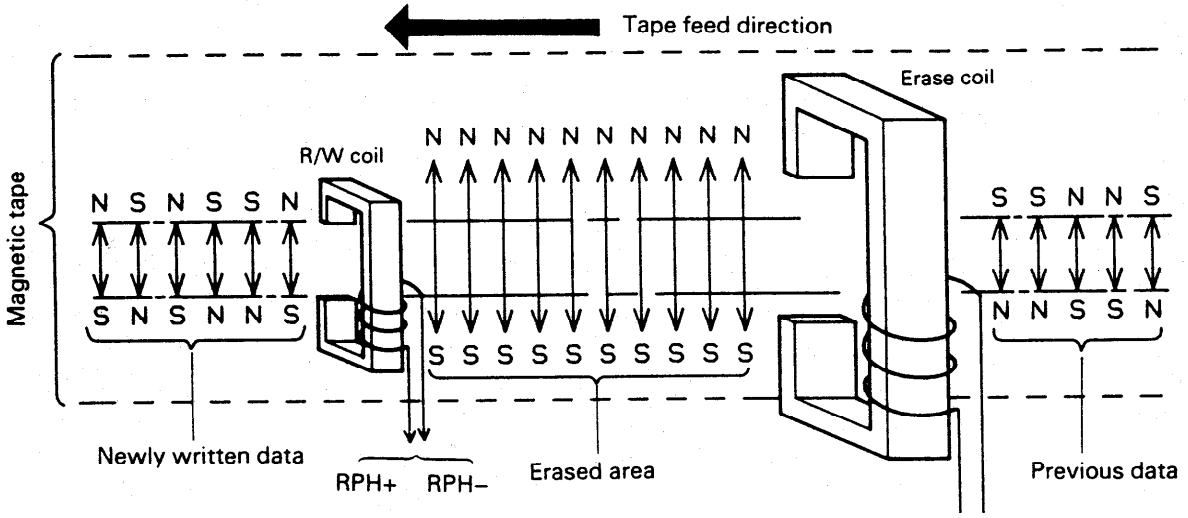


Fig. 3-14 Tape Write Current Waveform

Writing a value is ultimately generating a magnetic polarity determined by the write current direction. In order to eliminate interference which may be caused by data patterns previously written (magnetized) on the tape, the erase head is always activated during write operation initiated by the ERAH signal. New data, then will not be affected by previously magnetized polarities and the tape can be uniformly magnetized as new data is written Fig. 3-15 conceptually illustrates this operation, including the positional relationship between the read/write and erase heads.



3.1.7.2 Circuit Operations

Fig. 3-16 illustrates the write circuit. To write data, the direction of the write current through the read/write head is alternated by repeating charging and discharging the electolytic capacitor C12.

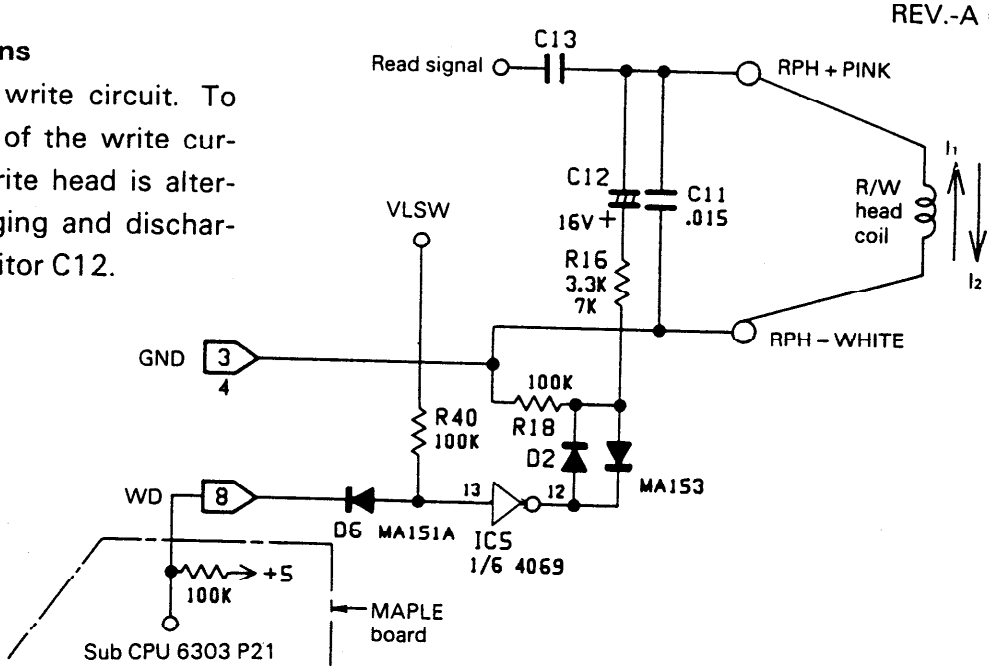


Fig. 3-16

A series of actual data bits is written on tape by alternating current to enable or disable, depending on the value of each bit, the pull-up of the input to pin 5 of IC5 to the VLSW voltage line through R4. The WD signal, which represents the logical value 0 or 1 of each data bit, usually varies its level and appears as shown in Fig. 3-17; it looks like a train of pulses.

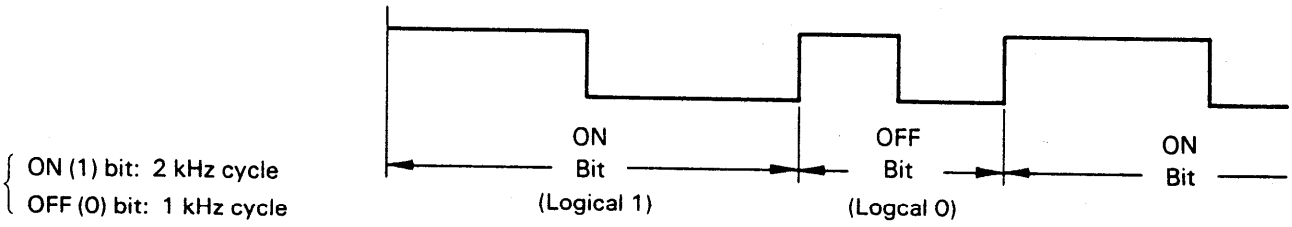
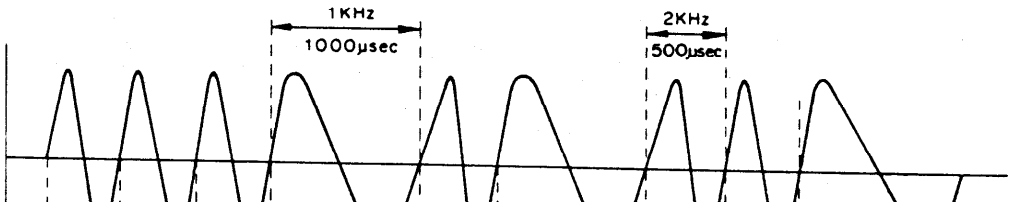


Fig. 3-17 Write Signal (WD) Pulse Train

* The flag bit is also written for each data byte and the write signal appears as shown in Fig. 3-18.



The above sample illustrates a data write (i.e. transfer) rate of approximately 1286 bps. As shown below, the rate varies depending on the bit configuration of the byte. Because the above sample data byte has four bits on and four bits off, the time required to write the entire byte (8 data bits and 1 stop bit) is:

$$4 \times 0.5 + 5 \times 1.0 = 7 \text{ ms}$$

Thus, a write time of 0.777 ms (7/9) is required per bit, resulting in the data transfer rate of approximately 1286 bps.

Circuit Operations During Non-Write

Part 21 of the 6303 slave CPU on the MAPLE board is a floating part, IC neither activate nor non-active signals are output. The WD signal line is always pulled up through a 100 kohm resistor. This causes output pin 13 of IC5 to be held low. The positive pole terminal of capacitor C12 is always grounded through the diode D2 and IC5, and no current flows through the read/write head.

Circuit Operations During Write

When the WD signal is low, a current flows from the VLSW line to port 21 through R40 and D6, lowering pin 13 of IC5 to almost 0V. This causes pin 12 to go high which allows the capacitor C12 to be charged, resulting in the write current through the read/write head in the direction indicated as I2 in Fig. 3-16.

When the WD signal goes high, C12 starts charging and results in the write current indicated as 11. This charge and discharge cycle is repeated for each data bit until the complete series of data bits is written. The diode D2 connected at pin 12 of IC5 limits the top and bottom of the signal by approximately 0.6V each as shown in Fig. 3-19. This serves to supply the optimum current waveform to the write winding.

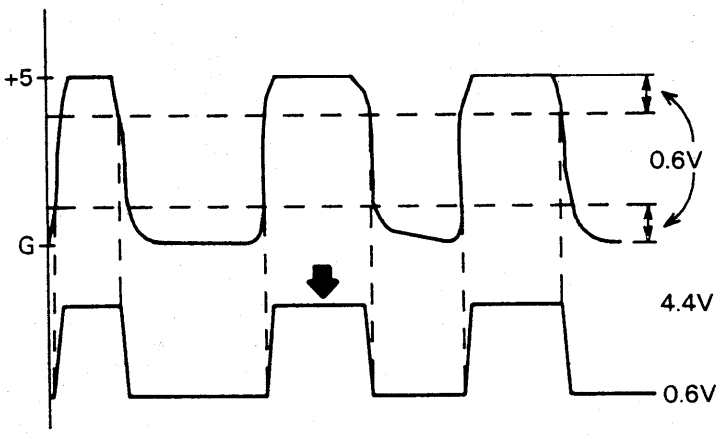


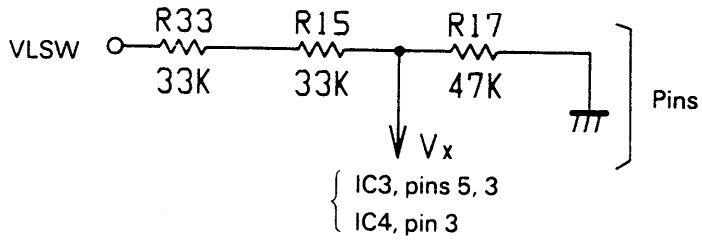
Fig. 3-19 Write Current Waveshaping

For data integrity, however, the data section of each file is written twice. Furthermore, each cassette tape reel requires a directory and a gap between blocks. Thus, the actual write time requires more than twice as long as that obtained from the above transfer rate.

Circuit Operations

The read signal from the read winding is fed to pin 6 of IC3, after its dc component is removed by capacitor C13. Divided voltage from VLR0 is supplied to pin 5 by the voltage divider circuit.

$$Vx = \frac{5 \cdot 47K}{33K + 33K + 47K} \rightarrow = 2.0\ V$$



Pins 5 through 7 of IC3 form a negative feedback amplifier ($G = -\frac{R20}{R14}$).
The output signal is fed, after its dc component is rejected by capacitor C18, to the next stage, which is also a negative feedback amplifier ($G = -\frac{R22}{R21}$).
The output of this amplifier is fed to the next filter circuit. It is also supplied to the speaker circuit on the MAPLE board. Since no phase compensation is provided in the previous stages, the signal here has some delay.

In the filter circuit, a high frequency component is removed by the T-type filter consisting of R26, R27, and C23, and the amplifier circuit. The amplifier frequency response is varied to lower the gain in a high frequency range.

The amplifier, consisting of pins 1 through 3 of IC3, detects signal peaks.

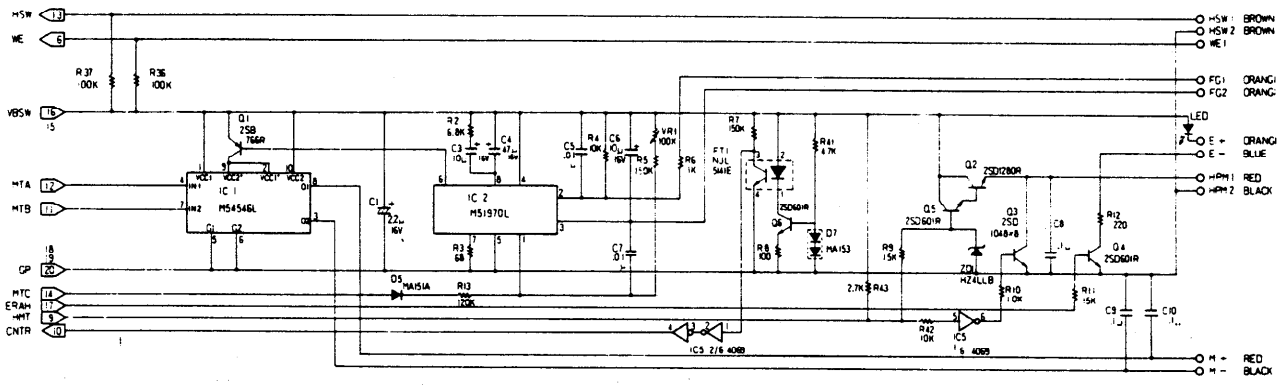


Fig. 3.20 Read Circuit

Observed read signal waveforms – (AZIMUTH tape playback signals)

(Top) Measured at IC3, pin 7 – 5 mV/DIV

(Bottom) Measured at IC3, pin 1 – 5 mV/DIV
Sweep: 0.1

} 200 μS/DIV

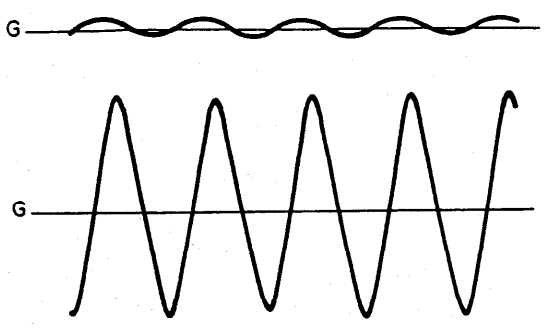


Fig. 3-21

(Top) Measured at IC4, pin 7 – 200 mV/DIV

(Bottom) Measured at IC4, pin 1 – 500mV/DIV

} 200 μS/DIV

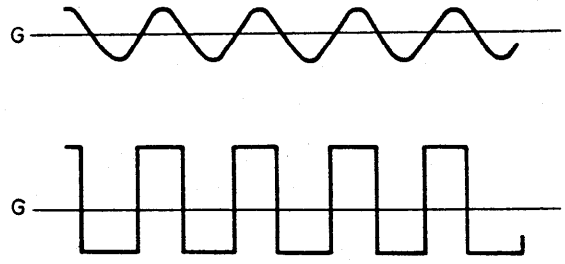


Fig. 3-22

(Top) Measured at IC4, pin 2 – 50 mV/DIV

(Bottom) Measured IC4, pin 1 – 500 mV/DIV

} 200 μS/DIV

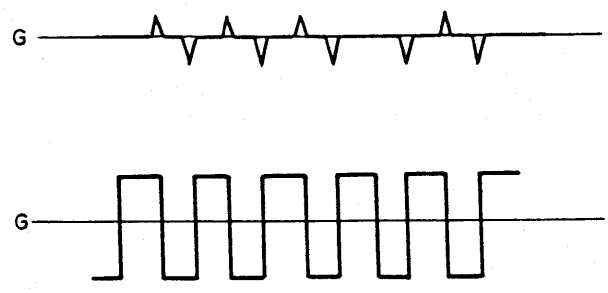


Fig. 3-23

Observed microcassette tape playback waveforms – AZIMUTH tape

(Top) Measured at IC3, pin ..... 5 mV/DIV
(Second from top) Measured at the center of R26 and R27..... 20 mV/DIV
(Second from bottom) Measured at IC4, pin 6..... 50 mV/DIV
(Bottom) Measured at IC4, pin 5. AC mode ..... 2 V/DIV

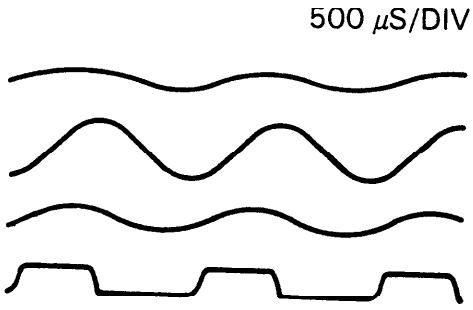


Fig. 3-24

The top three are since waves. The bottom signal is almost a square wave, due to a peak detection by a diode inserted across pins 1 and 2 of IC4.

Observed noise filter (phase compensation) circuit signal waveforms AZIMUTH – tape

(Top) Measured at IC3, pin
(Second from top) Measured at the center of R26 and R27.
(Second from bottom) Measured at IC4, pin 6.
(Bottom) Measured at IC4, pin 5. AC mode

200 mV/DIV
50 μS/DIV

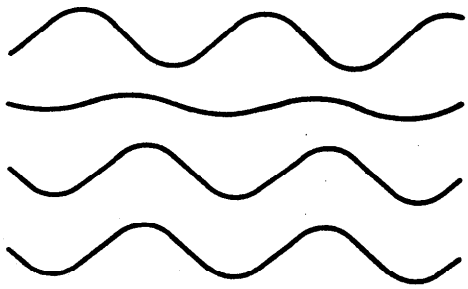


Fig. 3-25

Observed capstan motor control signal waveforms

(Top) Feedback signal from tacho generator – measured at IC2, pin 3.

(Bottom) 400 kHz basic clock signal measured at IC2, pin. 2.

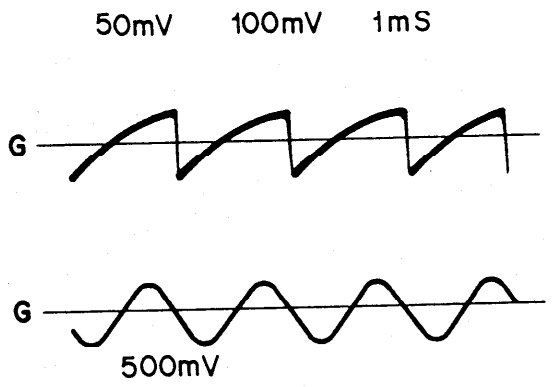


Fig. 3-26

(Top) Capstan motor drive voltage input – measured at IC, pin 2.

(Bottom) Voltage control signal – measured at IC2, pin 6.

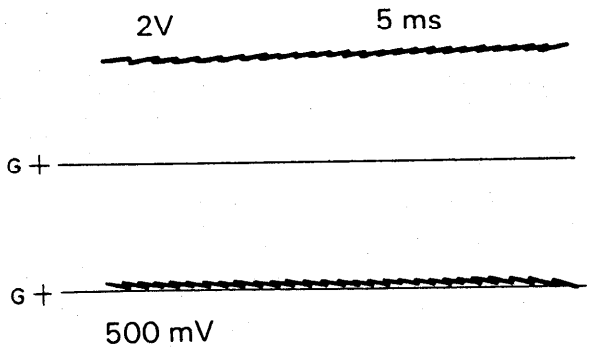
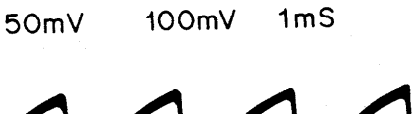


Fig. 3-27



3.2 RAM Disk Unit

Two models of 60K and 120K bytes are available. The models have the same circuit and operates exactly the same way. Only the difference is whether 64K or 128K bytes of DRAM are installed. The RAM disk unit has a Z-80 CPU built in and is operated asynchronously with the Main Frame.

3.2.1 Major Circuit Elements

The RAM disk unit is built on a circuit board which contains casing components and the following major circuit elements shown and listed below including a battery.

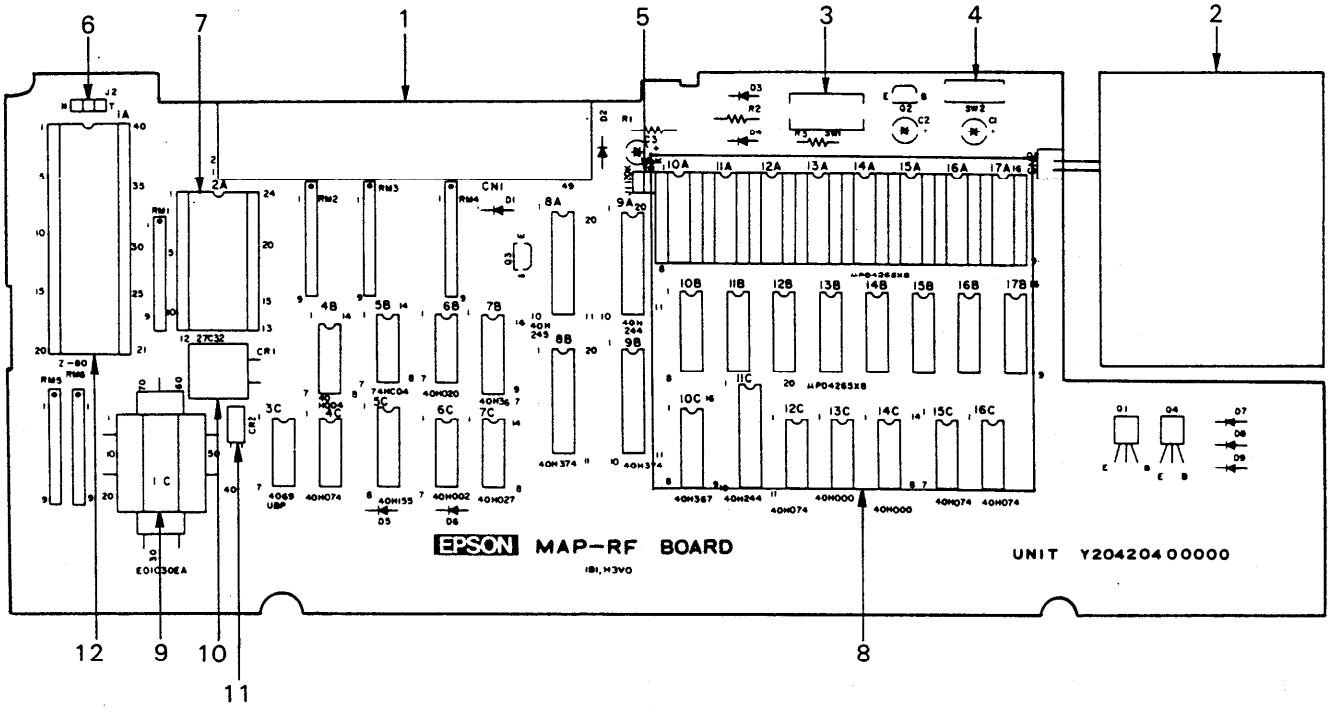


Fig. 3-29 RAM Disk Board Element Lay-Out

Table 3-2 Major Circuit Element

No.	Element	Function	No.	Element	Function
1	Connector CN1	Interface the data and address busses with Main Frame.	2	Battery	4.8V, 480mAH
3	SW 1	Write protect control ON: Protect OFF: Unprotect	4	SW 2	Connect/disconnect the built-in battery – the line normally connected.
5	Jumper J1	Define RAM capacity (60 K or 120 K).	6	Jumper J2	Z-80 CPU selection.

3.2.2 Function Circuit Blocks

Fig. 3-30 is a functional block diagram of the RAM disk unit.

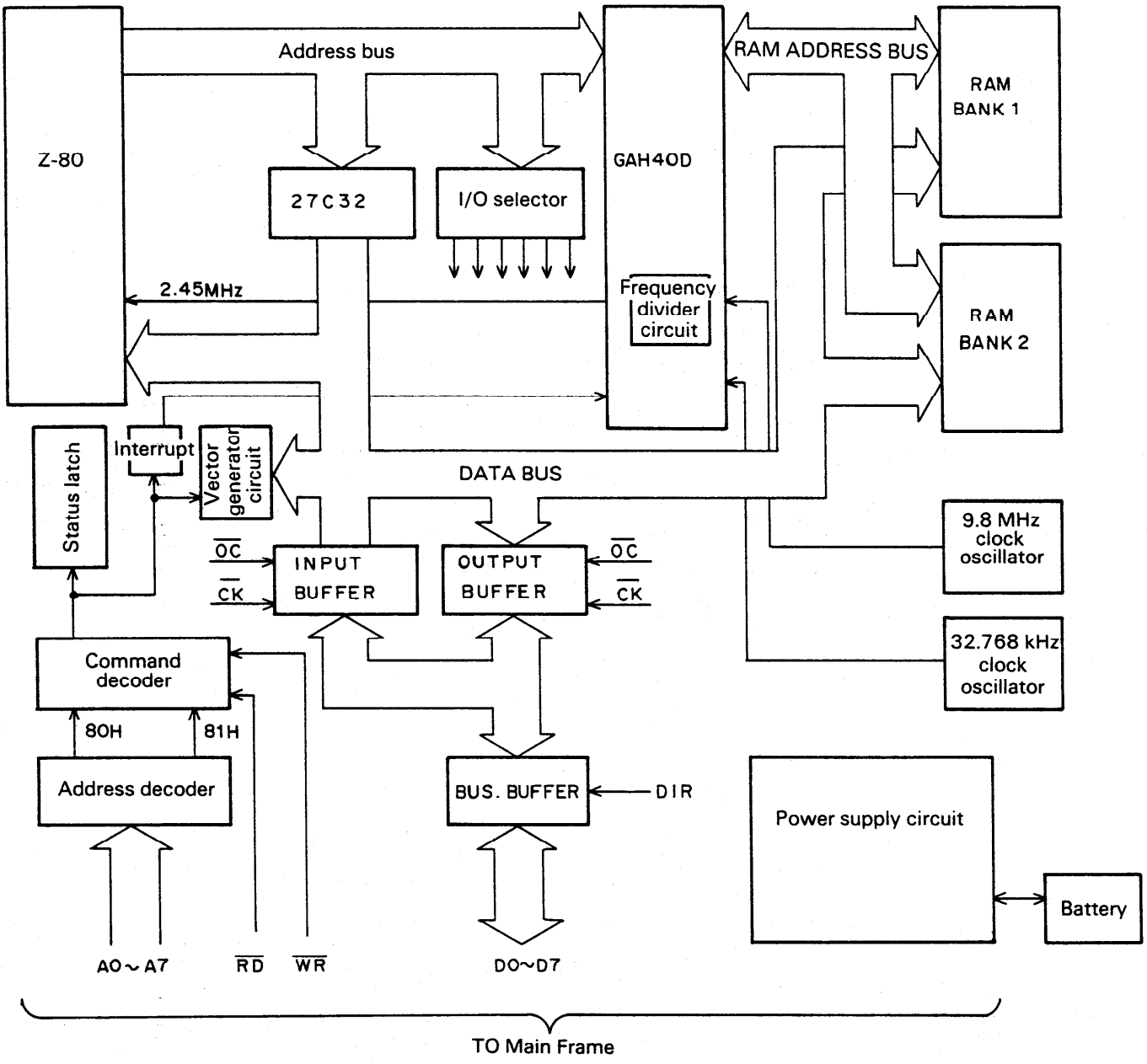


Fig. 3-30 RAM Disk Unit Block Diagram

The RAM disk unit includes a power supply circuit, hand shaking circuits such as an address and

3.2.3 Interface Signals

The RAM disk unit is connected to the Main Frame board via a cable assembly # 727. Table 3-3 lists the interface signals.

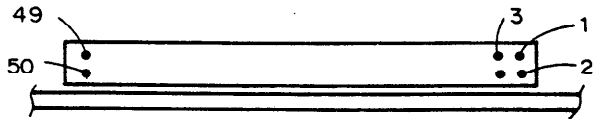


Table 3-3. RAM Disk Unit Interface Signals

Pin No.	Signal Name	Direction	Definition
1	–	–	Not used.
3	–	–	Not used.
5	AB1	Input	Address but line 1
7	–	–	Not used
9	AB4	Input	Address bus line 4
11	AB6	Input	Address bus line 6
13	–	–	Not used.
15	–	–	Not used.
17	DB0	Input/ Output	Data bus line 0
19	DB2	Input/ output	Data bus line 2
21	DB4	Input/ Output	Data bus line 4
23	DB6	Input/ Output	Data bus line 6
25	–	–	Not used.
27	–	–	Not used.
29	VL	Input	Logic circuit +5V supply
31	GND	–	Signal ground
33	$\overline{RS}$	Input	Reset
35	$\overline{RD}$	Input	Read
37	$\overline{WR}$	Input	Write
39	VCH	Input	Battery charge voltage
41	DCAS	Input	Cata CAS
43	–	–	Not used.
45	–	–	Not used.
47	VB1	Input	Battery voltage
49	–	–	Not used.

Pin No.	Signal Name	Direction	Definition
2	–	–	Not used.
4	–	–	Not used.
6	AB2	Input	Address bus line 2
8	AB0	Input	Address bus line 0
10	AB3	Input	Address bus line 3
12	AB5	Input	Address bus line 5
14	AB7	Input	Address bus line 7
16	–	–	Not used.
18	DB1	Input/ Output	Data bus line 1
20	DB3	Input/ Output	Data bus line 3
22	DB5	Input/ Output	Data bus line 5
24	DB7	Input/ Output	Data bus line 7
26	–	–	Not used.
28	–	–	Not used.
30	–	–	Not used.
32	GND	–	Signal ground
34	–	–	Not used.
36	–	–	Not used.
38	–	–	Not used.
40	$\overline{IORQ}$	Input	I/O Request
42	DW	Input	Data Write
44	OFF	Input	GAH40D Initialization
46	–	–	Not used.
48	–	–	Not used.
50	–	–	Not used.

Note:

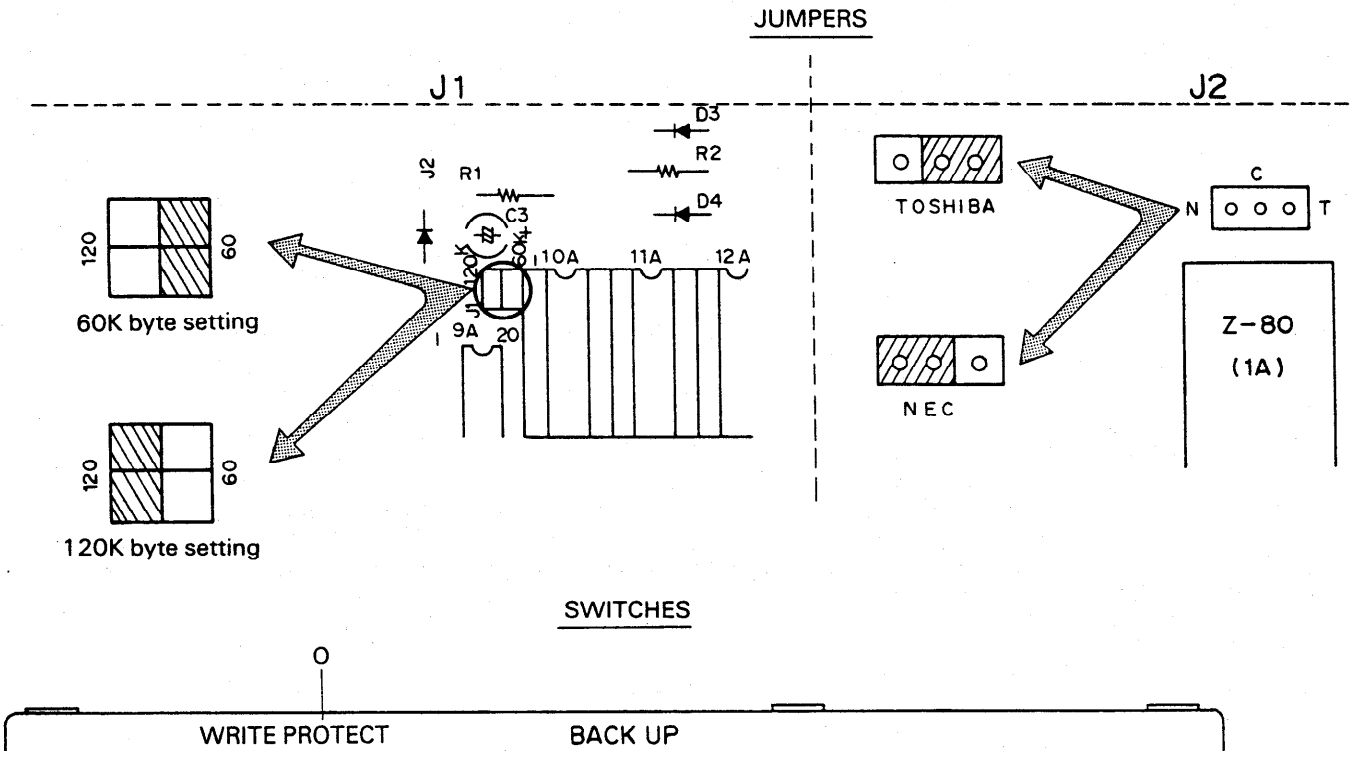
Some of the signals used in the Main Frame including the address bus lines AB7 through AB15, etc. are not used in this interface.

3.2.4 Jumpers and Switches

The following jumpers and switches are mounted on the RAM disk unit board. The switches SW 1 and SW 2 will be accessed by user.

Table 3-4 Jumper and Switch

Jumper/switch	Standard	Drawing coordination	Function
J1	—	D.E -4	Select a RAM capacity: 60K or 120K bytes, according to the installed RAM elements.
J2	—	E -2	Specifies the main CPU.
SW1	ON	ONE -4	Enable/disable DRAM write protection ON: Enables write protection – allows read only. OFF: Disables write protection – allows both read and write.
SW2	ON	A -6	Enable/disable battery backup ON: Enables battery backup – allows battery charge/discharge. OFF: Disables battery backup – battery charge/discharge is inhibited.



3.2.5 Power Supply Circuit

The RAM disk unit power supply circuit consists of a +4.8V, 450 mAH rechargeable battery, a charge circuit, a logic voltage source circuit, and a backup circuit.

1. Rechargeable battery and charge circuit

The battery is connected to the MAP-RF board via a connector CN 2. The switch (SW2) on the board allows the user to connect or disconnect the battery to the MAP-RF board.

The circuit surrounding the battery is shown below.

1) Battery backup switch SW2

This switch should be reset OFF when storing this unit alone or when not using it for a long period of time as attached to the Main Frame. With this switch reset OFF, the battery is prevented from any discharge other than the natural one so that the longest life can be ensured.

* The backup line circuit operates irrespective of the setting of this switch; when the switch is reset OFF, the line is backed up from the Main Frame battery and its working time may be shortened.

2) Battery charging

The battery is always charged toward the full via either of the following two charging paths:

When the Main Frame AC adaptor is connected to the AC power source.

V_{CH} → D2 → R1 → SW2 → CN2 → Battery

When the AC adaptor is not used but the battery voltage is lower than the VB1 supply voltage from the Main Frame.

V_{B1} → D3 → R2 → SW2 → CN2 → Battery

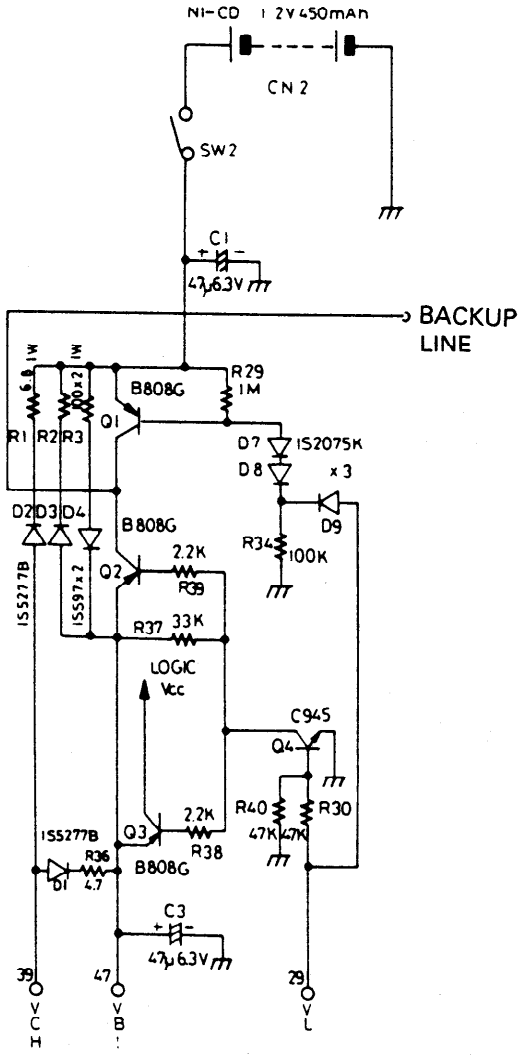


Fig. 3-32 Power Supply Circuit

2. Backup circuit

The backup circuit supplies power required to protect data in the DRAM.

Table 3-5 lists the elements backed up by this circuit.

Table 3.5 Backed Up Elements

Element	Drawing coordination	Function
1C	F-1, 2	Read/write control gate array
9A	H-1	Gate
3C	A, B-7	Gate

Element	Drawing coordination	Function
17B ~ 10B	G-2 ~ 6	D-RAM
17A ~ 10A	H-2 ~ 6	D-RAM
3C	F-3	Gate

These elements are powered from a special line called "Backup" and always active; they are powered by the operating voltage supply while Main Frame is on and from the backup voltage while off.

1) Power supply paths to the backup line

There are the six paths listed in table 3-6 which are selected to supply power to the backup line depending on the various conditions. The abbreviations used in the table mean the following:

V_{B1} : Main Frame battery voltage
V_X : RAM disk unit battery voltage
Battery: RAM disk unit battery

Tabel 3-6 Backup Line Supply Paths

Main Frame power	AC adapter	Battery voltage relation	Path
OFF	Connected	—	V_{CH} → D2 → R1 → Q1 →
	Not connected	$V_{B1} > V_X$	V_{B1} → D3 → R2 → Q1 →
	Not connected	$V_{B1} < V_X$	Battery → CN2 → SW2 → Q1 →
ON	Connected	—	V_{CH} → D1 → R36 → Q2 →
	Not connected	$V_{B1} > V_X$	V_{B1} → Q2 →
	Not connected	$V_{B1} < V_X$	Battery → CN2 → SW2 → R3 → D4 → Q2 →

The backup line is powered either transistor Q1 or Q2 depending on whether Main Frame power is on or off.

* While Main Frame is off, VL is low because the logic circuit operating voltage is not supplied.

While Main Frame Power is on, no effective potential is generated across the emitter and base of Q1 because the base is pulled up to VL, and Q1 is maintained cut off. Q4 conducts because the base input (VL) is low and the collector is held low. This maintains Q2 and Q3 in conduction. Thus, the backup line is powered via Q2 and the logic circuit voltage is supplied through Q3.

3. Logic circuit voltage

The logic circuit voltage is supplied from the collector of transistor Q3. The voltage applied to the emitter (VB1 or V_{CH} through D1 and R34) is supplied to the circuit power line. The supply circuit operates as descried above.

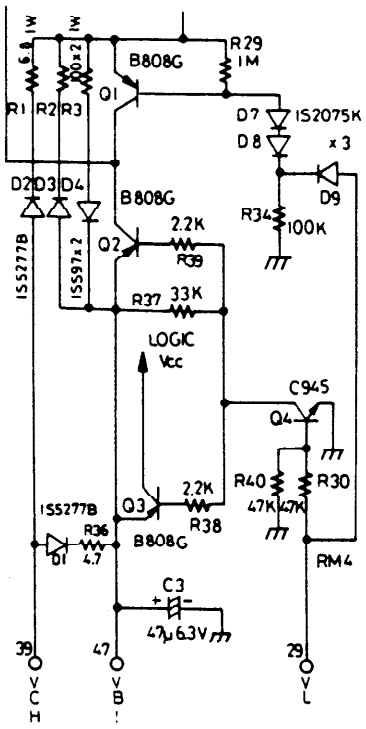


Fig. 3-33 Power Supply Circuit

3.2.6 Interface Circuit

Since this RAM disk unit and Main Frame asynchronously operate, either one must examine the status of the other to accomplish a RAM disk read/write. A function, which temporarily stores the data until it is written in RAM disk or read by Main Frame, is also required.

1. Address decoder

The RAM disk is looked upon as an I/O device by the Main Frame CPU and two I/O addresses are assigned. Fig. 3-34 shows the address decoder circuit.

Pin 10 and 13 of IC "6C" are the outputs of the decoder. As obvious from the figure, the output (pin 8) of IC "6B" must be low to enable the two decoder outputs. Either of them is selected depending on the state of A0. The output IC "6B" is low when the following relation is satisfied among the input signals to this IC and the preceding IC "7C"; $\overline{A1 - A6}$ .A7.$\overline{IORQ}$. This relation can be logically represented as in Fig. 3-34; an address 80 (H) or 81(H) is decoded to access the RAM disk unit.

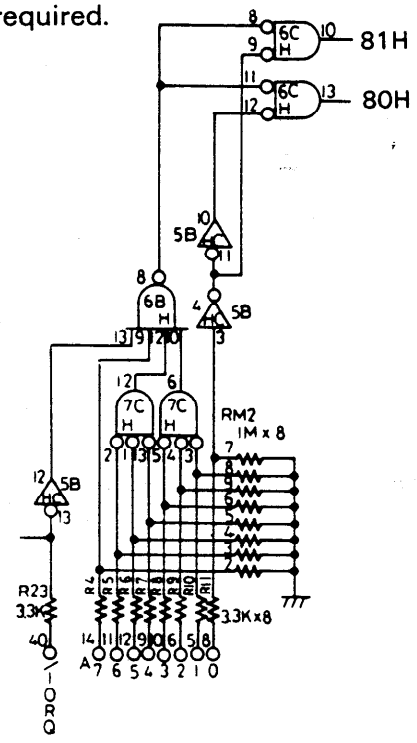


Fig. 3-34 RAM disk address decoder circuit

A7	A6	A5	A4	A3	A2	A1	A0
1	0	0	0	0	0	0	1/0

80 (H)
or
81 (H)

2. Command decoder

Four signals are generated by IC "14C" from either address supplied from the address decoder and the $\overline{RD}$ and $\overline{WR}$ signals as shown in fig. 3-35.

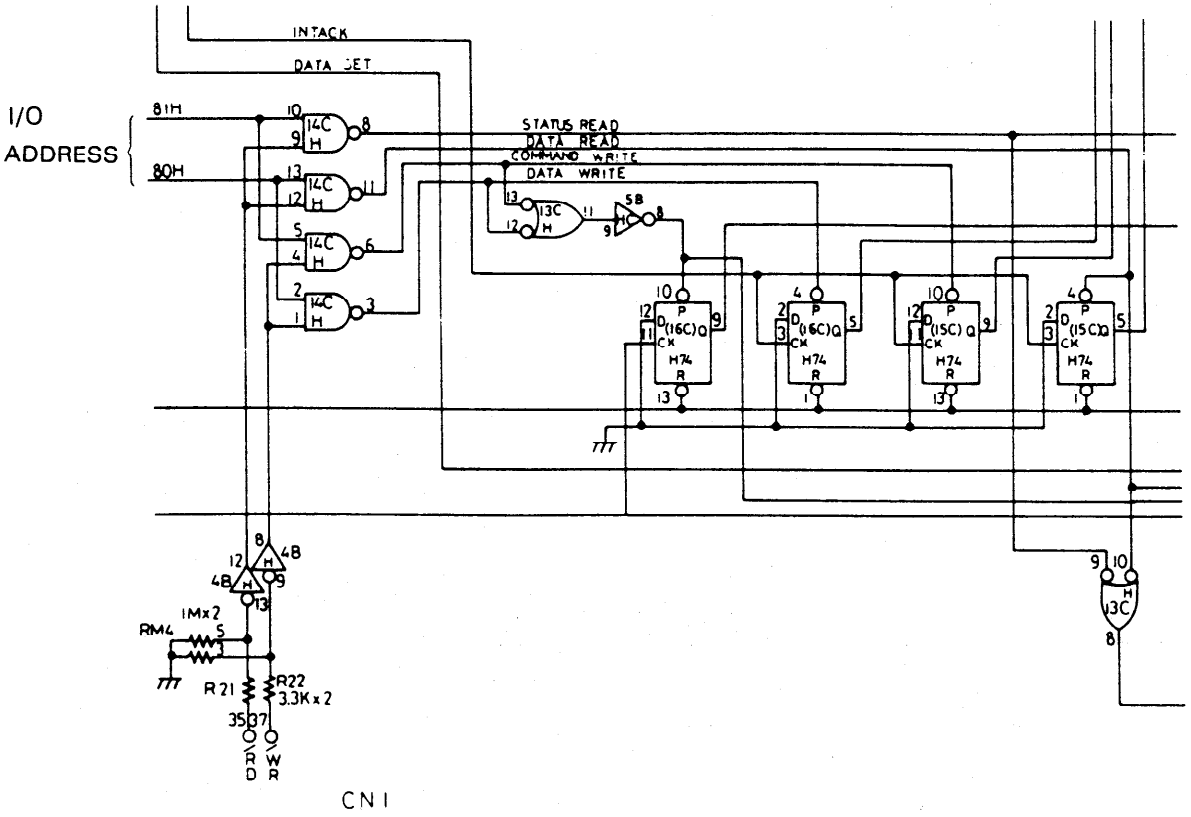


Fig. 3-35

The four I/O read/write signals provide the functions listed in table 3-7.

Table. 3-7 Command Decoder Signals

I/O Addrss	$\overline{RD}$/$\overline{WR}$ signal	Generated signal	Function
81 (H)	$\overline{RD}$	Status Read	Read RAM disk status to Main Frame
	$\overline{WR}$	Command Write	Write a command from Main Frame to RAM disk.
80 (H)	$\overline{RD}$	Data Read	Read data from RAM disk to Main Frame
	$\overline{WR}$	Data Write	Write data from Main Frame to RAM disk.

Unlike the other three, the Status Read signal reads the RAM disk status register irrespective of

* CK input: I/O port 03 (H) read by RAM disk unit - FF output read.
* R input : PX-8 reset or I/O port 01 (H) write by RAM disk unit - program reset.

3. Data and command registers

Two 8-bit registers are provided for input and output which serve as buffers (temporary data storage) used during data transfers between the RAM disk unit and Main Frame. Their input/output or read/write is controlled via an address assigned to them. The data is directed on the data bus from/to the registers under a directional control by the data bus control feature provided by a tri-state buffer IC "8A". Fig. 3-30 shows the data transfer directions and the direction control circuit.

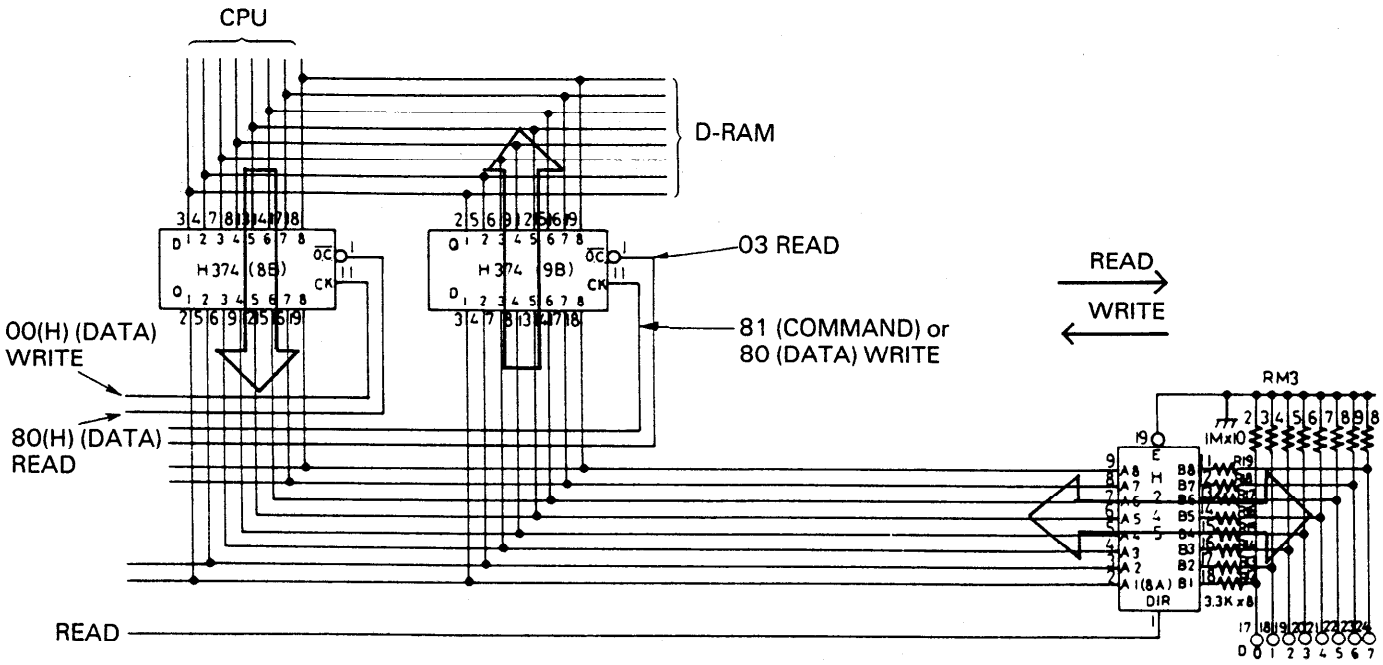


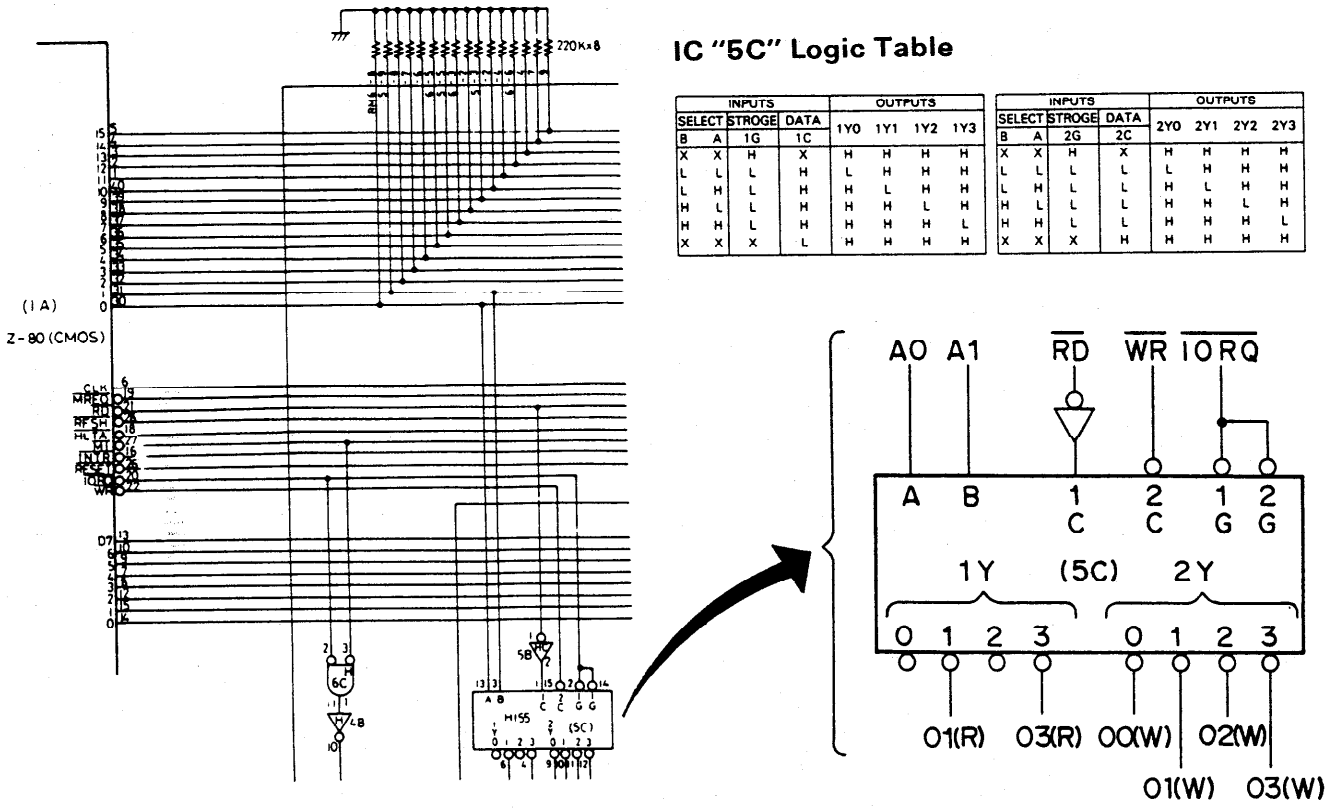
Fig. 3-36 Data Transfer Directions and Control

ICs "8B" and "9B" contain eight tri-state D-type FFs each. The FFs read and latch data from either data bus as arrowed when the "CK" signal rises. When the "$\overline{OC}$" signal goes low, the latched data becomes available onto the data bus from the output (Q) terminals.

- IC "9B" is the Input register. It latches a data directed from Main Frame via address 81 (H). This data is then transferred to the RAM disk CPU when it reads its I/O port 03 (H).

3.2.7 I/O Selector

The I/O selector (IC "5C") is the RAM disk CPU I/O address decoder which is used for handshaking in the interface. Fig. 3-37 shows the circuit and table 4-7 lists its decoding logics.



IC "5C" Logic Table

INPUTS				OUTPUTS			
SELECT		STROGE	DATA				
B	A	1G	1C	1Y0	1Y1	1Y2	1Y3
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

INPUTS				OUTPUTS			
SELECT		STROGE	DATA				
B	A	2G	2C	2Y0	2Y1	2Y2	2Y3
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

Fig. 3-37 I/O Selector Circuit

IC "5C" has six outputs whose functions are listed in table 3-8.

Table 3-8 I/O Selector Logics

Read/Write	I/O Port Address	Supplied To	Function
READ	01	7B	Read J1 and SW1 status.
	03	9B	Read data or command from input register.
	00	12C, 8B	Write data to output register.

3.2.8 Bank Control

The RAM disk unit can contain a 4 K byte IPL ROM and 64 K or 128 K byte DRAM. However, the Z-80 CPU cannot directly access DRAM above 64 K bytes. Thus, DRAM needs to be divided into banks so that entire DRAM can be accessed indirectly by selecting bank. This control is accomplised by the Bank Latch circuit and the gate array GAH40D shown in fig. 3-38.

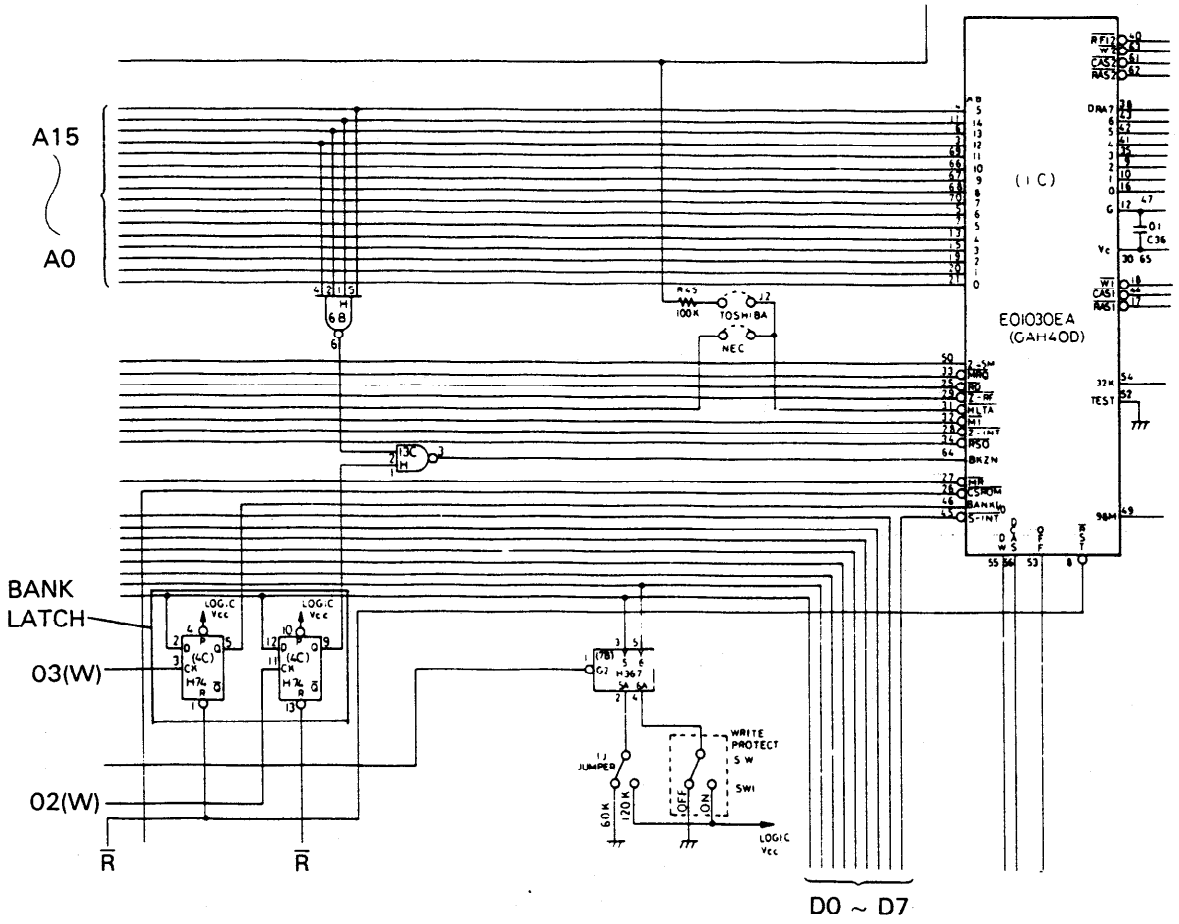


Fig. 3-38 Bank Control Circuit

1. Momory map

The bank control signals and the memory map are associated as shown in table 3-9.

Table 3-9 Bank Control Signal and Memory Map

BK 2 / BK 0/1 / Address	1	1	0	0
	0	1	0	1
FFFF				

Gate GAH40D is initialized as follows when Main Frame Power is turned on:

Bank 2 = 1, Bank 0/1 = 0

This initialization is of course accomplished by a hardware reset logic. The initialization circuit operation is described below.

- The Reset ($\overline{R}$) signal is connected to both the Bank Latch FFs located in drawing coordinations C,D-3. Thus, the two Q outputs are held-low - the output from pin 5 is the Bank 0/1 Selection signal and the output from pin 9 is the Bank 2 Selection signal. Address bus lines 12 through 15 from the Z-80 CPU are respectively connected to pins 4, 2, 1, and 5 of IC "6B" which are all low immediately after Main Frame power is turned on, raising the output (pin 6) high. This output signal is fed to IC "13C" where it is NANDED with the Bank 2 Selection signal from the Bank Latch circuit which is also low immediately after power on. Thus, the output from pin 3 is high.

The RAM disk memory address space is mapped as shwon in the second (from the left) or fourth column of table 3-9 by initialization so that the CPU accesses address 0000; i.e., the IPL ROM area.

2. Bank selection

Bank selection is accomplished by the program in IPL ROM which accesses I/O ADDRESS 02 and 03, which are connected to the Bank Latch, to change the latch setting. Thus, if a bank, which allows no IPL ROM access, were selected by simply accessing the Bank Latch, no subsequent bank selection would be possible. In order to solve this problem, the bank control program is usually written in the DRAM area from a certain address during the IPL program execution. This unit initially loads the bank control program in a DRAM 2 address space from FC00 to FFFF, and a common DRAM 2 area of the highest 64 bytes is always selected independently by gate array GAH40D regardless of bank (0/1 or 2).

3.2.9 Interrupt

As previously stated, the command (i.e., Read or Write) and 8-bit data sent from the Main Frame is temporarily stored in an internal buffer because the RAM disk unit operates asynchronously. The unit is notified of this temporary storage by an interrupt. Fig. 3-39 shows the interrupt circuit.

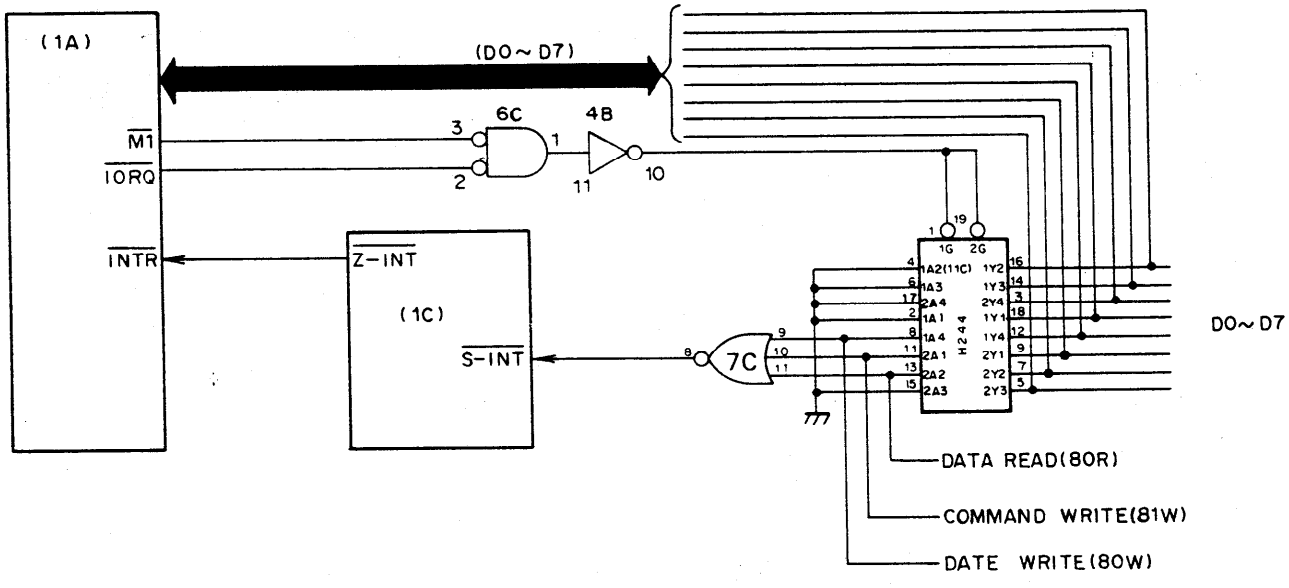


Fig. 3-39 RAM Disk Interrupt Circuit

As obvious from the drawing, the three signals other than Status Read, which instructs an immediate read, are fed to the OR circuit of IC "7C" via D-type FFs "15C" and "16C" whose output is connected to the $\overline{\text{S-INT}}$ terminal of gate array "1C". This input signal is output from the gate array as the $\overline{\text{Z-INT}}$ signal to the $\overline{\text{INTR}}$ terminal of the CPU as the interrupt input. When the AND condition between $\overline{\text{M1}}$ and $\overline{\text{IORQ}}$ is met (indicating that a vector address is output on the data bus in the CPU mode 3) after an interruption occurs, a byte data corresponding to the RAM disk command signal is output on the data bus from the right terminals of IC "11C". This data is the interrupt vector which is fed to the CPU. There are the following interrupt vectors corresponding to the RAM disk command signals:

Command signal	**Interrupt vector**	
Data Read	02	Each of these vector address calls a specific routine that processes the corresponding command and data.
Command Write	04	
Data Write	08	

After an interrupt is accepted, the D-type FF which caused the interrupt ("15C" or "16C") is initialized. Fig. 3-40 shows the related circuit. The vector address is output and the D-type command buffer FF is reset by the same signal INTACK. However, the FF is reset at the rising edge to ensure the interrupt vector to be completely fed to the CPU as shown in fig. 3-41.

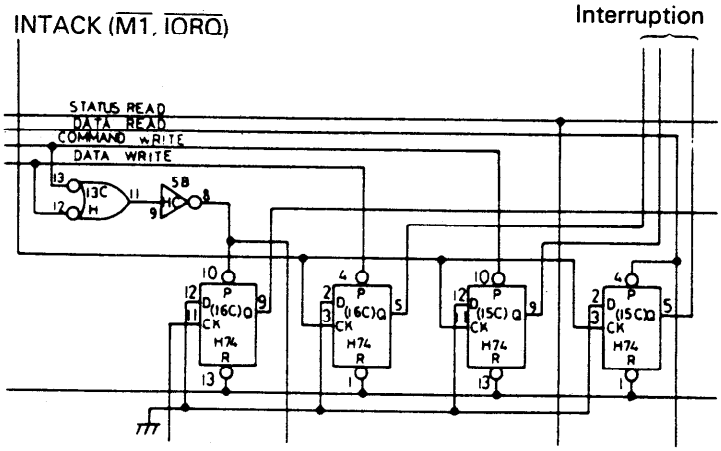
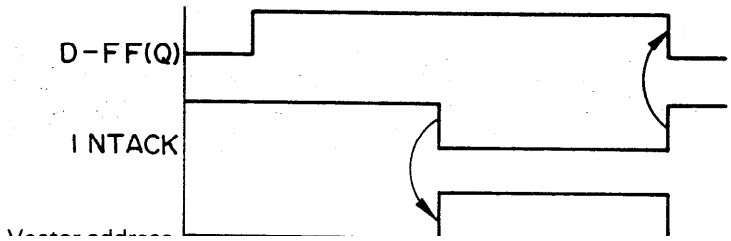


Fig. 3-40



3.2.10 Clock Signals

Two clock signals of 9.8 MHz and 32.768 kHz are generated in the RAM disk unit. 9.8 MHz clock signal is divided in gate array GAH40D to 2.45 MHz and fed to the CPU. The 32.768 kHz clock signal is also divided in the gate array and used as the DRAM refreshing signal. Fig. 3-42 shows the clock signal oscillator circuits.

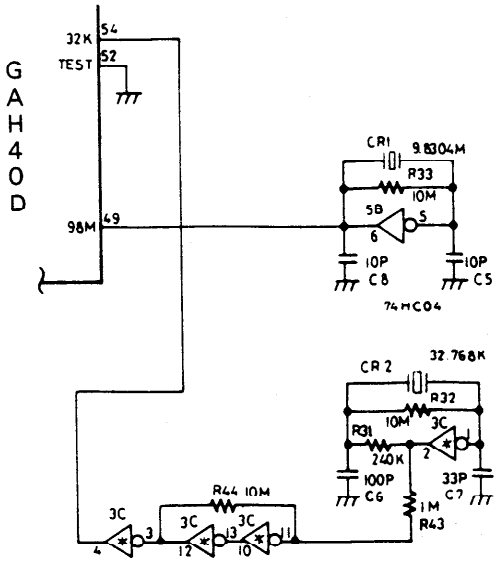


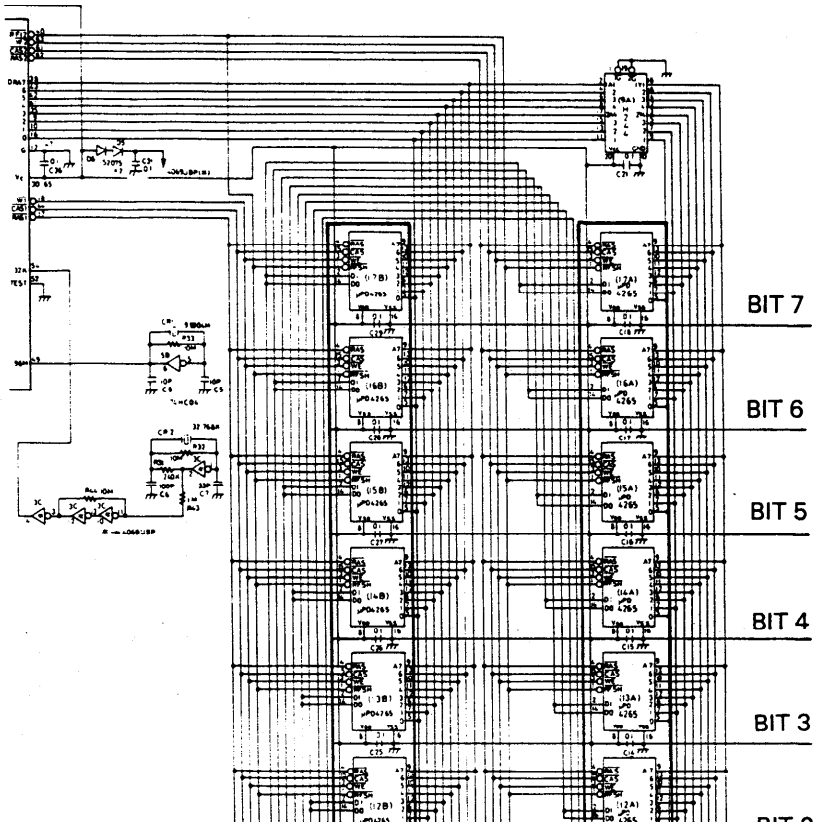
Fig. 3-42

3.2.11 DRAM Banks

The DRAM circuit is organized as shown in fig. 3-43 and controlled by gate array GAH40D.

It is read/written and refreshed (also while Main Frame power is off) in the same way as Main Frame RAM. This unit has two DRAM banks of 64 K bytes each and can provide a capacity of 64 K or 128 K bytes. Two signals DCAS and DW, which determine a refresh mode while power is off, are applied from Main Frame.

- IC "9C" is provided to ensure the address output that can drive 128 K bytes of RAM.



3.2.12 Jumpers and Switch

The combination of jumper J1 and switch SW1 allows the IPL program to be read via I/O port address 01. Jumper J2 selects a CPU model.

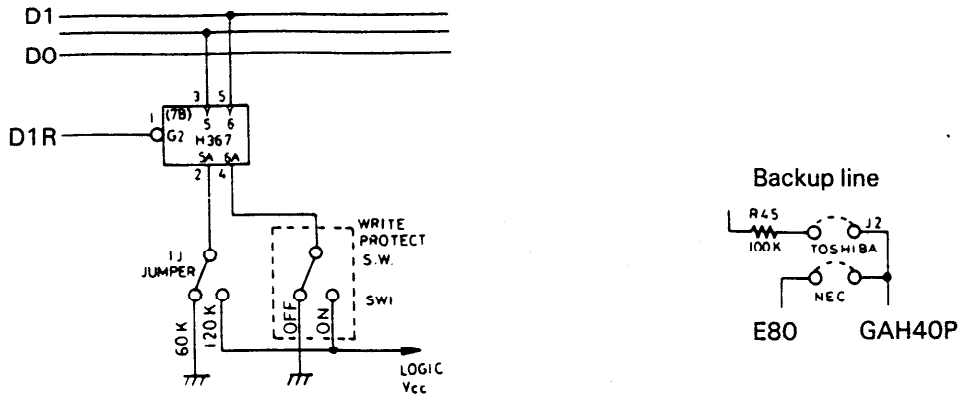
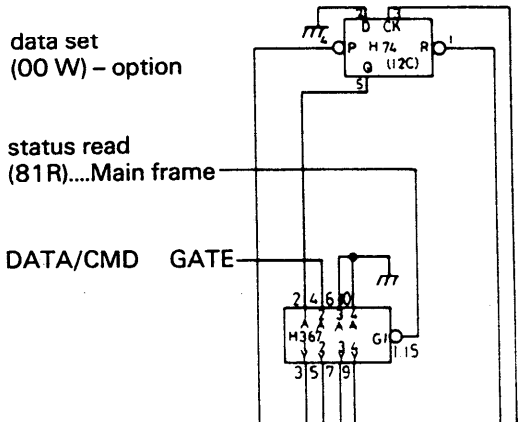
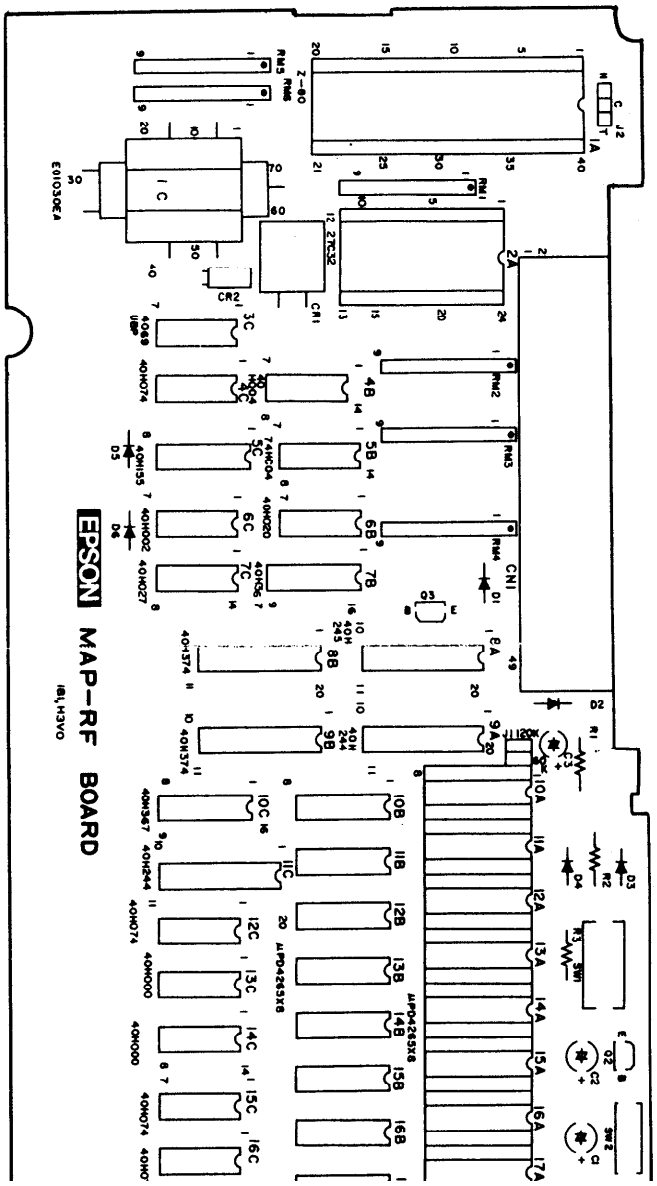


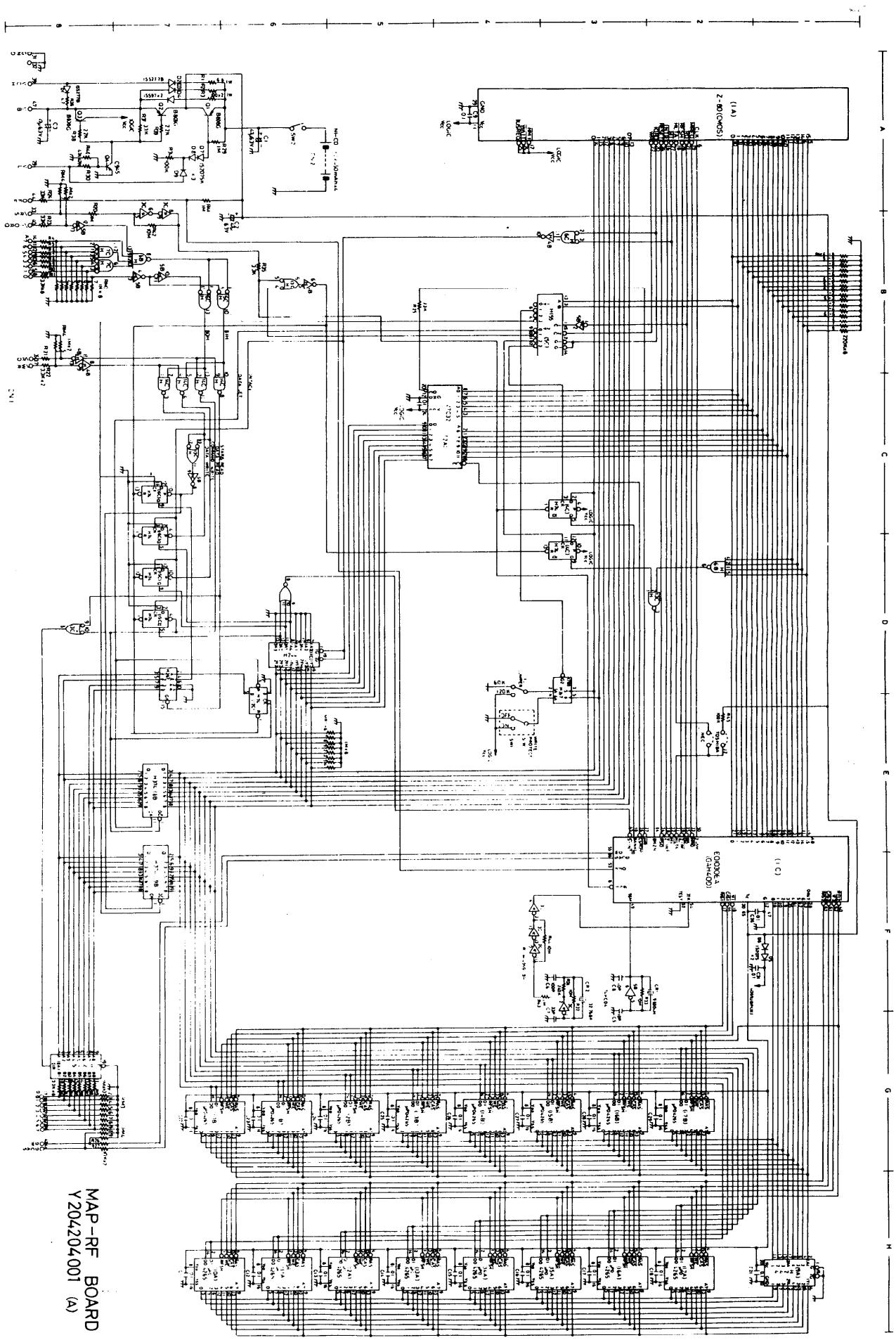
Fig. 3-44

3.2.13 Status Register

The Main Frame CPU reads the RAM disk status from IC "10C" shown in fig. 3-45. Input terminals 6 and 10 are grounded to produce the ID code of the RAM disk unit. The Date/COM Write signal input to terminal 4 indicates whether a data or command received from Main Frame is being processed or not. The signal input to terminal 2 from D-type FF "12C" indicates whether a data is latched (buffered) to be sent to Main Frame or not.




EPSON MAP-RF BOARD
IBL, H3YO



MAP-RF BOARD
Y20420001 (A)

CHAPTER 4
DISASSEMBLY/ASSEMBLY AND ADJUSTMENT

Disassemble/Assemble

This section describes how to disassemble and assemble the machine. First, disassembling/assembling of the unit, next, disassembling of each unit are shown. To assemble each unit, follow in the reverse order of disassembling. Pay attention to the following cautions when disassembling and assembling the machine.

(1) Confirm that power of the machine is off.
(2) Disconnect options and cables that are connected to the machine.
(3) Save programs if any that are stored in the RAM of main memory and the option onto cassette tapes, etc.
(4) When repairing, storing, or shipping the MAPLE board, care must be used to prevent any shortcircuit on the board.
(5) Avoid placing boards that incorporate ICs (MAPLE board, LCD panel board, option board, etc.) directly on a work stand. If it is not practical, place it with the component side below (so that static electricity will not affect it).
(6) Pay attention so that cables may not be caught by case, fitting poles, etc.
(7) When fitting a screw, pay attention to the length of the screw.
(8) When fitting a component with screw lock being used, be sure to apply specified screw lock.
(9) As for boards such as MAPLE board with battery on it, power off the battery line to protect the board from short-circuit or remove the battery and keep it.
Should the board be left with the battery installed, it would be completely discharged, and the battery life might be shortened.

CHAPTER 5
TROUBLESHOOTING

5.1 An Introduction to Troubleshooting

Troubleshooting is usually to easy; vaned symptoms appear depending on points of failure. This section describes two procedures which may allow easier troubleshooting and subsequent repair:

1. Check-out procedure

   Objective: To guide the user through a problem isolation process when symptoms do not indicate a specific component malfunction.

   Fault isolation level: Repair by unit replacement, repair can be accomplished with a basic knowledge of computer hardware.

2. Unit repair flowchart

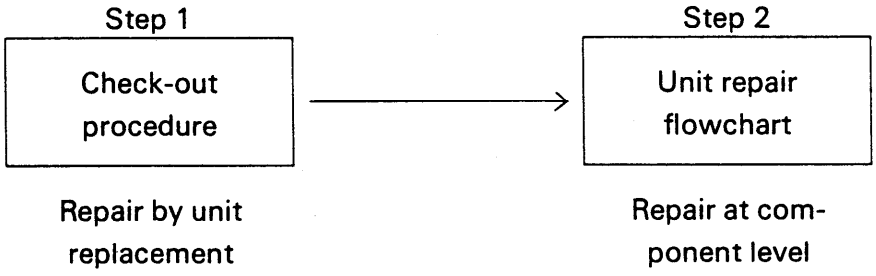
   Objective: To guide the user through a component level repair process.

   Allow a component-level repair of an individual faulty unit.

   Fault isolation level: Component level – Requires an advanced knowledge of computer hardware engineering, and electronics.

General troubleshooting procedure

- First, isolate and replace the faulty unit according to the check-out procedure faulty each time a unit is replaced, to make sure the new unit is not faulty. This process will prevent confusion with a problem caused by poor connector contacts.
- Second, isolate and replace the faulty component in the unit according to the appropriate unit flowchart or the trouble table.



Note 1) All checks indicated on the flowchart must be made.
Should any unit or component be replaced disregarding any check, the newly installed one might be damaged.

Note 2) Whenever you are lost in the repair procedure, return to the entry and restart the procedure.

Note 3) When no exit is found, during a diagnostic procedure (e.g., the test process has resulted in repeating a diagnostic loop), proceed with the repair according to the trouble table.

5.2 Test Program

A test program is supplied stored in an E-PROM with carrier which can be installed in the computer ROM capsule. The test program provides tests for the ten functions listed in Table 5.1. It allows either one of the following two execution modes

- AUTO Modo

  In this mode, the program automatically performs a six test cycle. If desired, the cycle may be repeated up to 99 times. The number of cycles may be selected after loading the program. This mode is suitable for an aging test after repair or a test on a problem of very low reproducibility.

CHAPTER 6
MAINTENANCE

6.1 Repair

Before starting the repair

1. Static electricity

- A human being's body is charged with the static electricity which is caused by the friction of his clothes. If his charged fingers contact the elements of the circuit, the static electricity may damage the elements. Therefore, before starting the repair work, touch the case cover with both hands to discharge any static electicity.
- When using a measuring instrument, such as an oscilloscope, which needs to be grounded, touch the conductive portion of the grounding terminal to the case of PX-8 and your fingers, then connect it to the GND terminal on the board.
- Before repairing the MAPLE board, remove the AC adaptor, the main and auxiliary batteries, and wait for approximately 30 second before beginning repair. This will allow residual power to dissipate. Handling before total power dissipation may result in damage to the board.

2. Circuit

- After removing the circuit board from the case for repair, rest it on insulative material, to prevent shortcircuits.
- After turning off the power switch, the RAM and a part of IC are backed up by the battery. Therefore it is necessary to observe the precautions listed above while replacing elements on the control board.
- Before examining the circuit, check to see if the signal lines are backed up.
- Flexible printed cable (FPC) is used in the mark. If the FPC is bent or scratched, it may result in circuit damage.
  Therefore, handle it very carefully.

4. Connectors

- All internal cable connectors in this device are of locking type. When disconnecting the cables, unlock the connectors.

5. Soldering

- When repairing the boards, refer to the section on soldering.

6. Storing or transporting circuit boards on which batteries are mounted.

- When storing or transporting circuit boards on which batteries are mounted, protect them from static hazards by using a static-proof insulator bag, etc. When storing them for a long time, remove the battery(s) to prevent battery deterioration or circuit damage due to possible battery leakage.

CHAPTER 7
APPENDIX

7.2 Slave CPU 6303

6303 is a 6800-series, 8-bit, C-MOS CPU. It incorporates a 4kB masked ROM which contains programs for controlling the microcassette tape drive, ROM capsule, V-RAM, LCD display unit, serial interface, and speaker. A mode six (Multiplexer Partial/Decode) is selected for the control operations. Stand-by and sleep modes, unique to 6303, are not used.

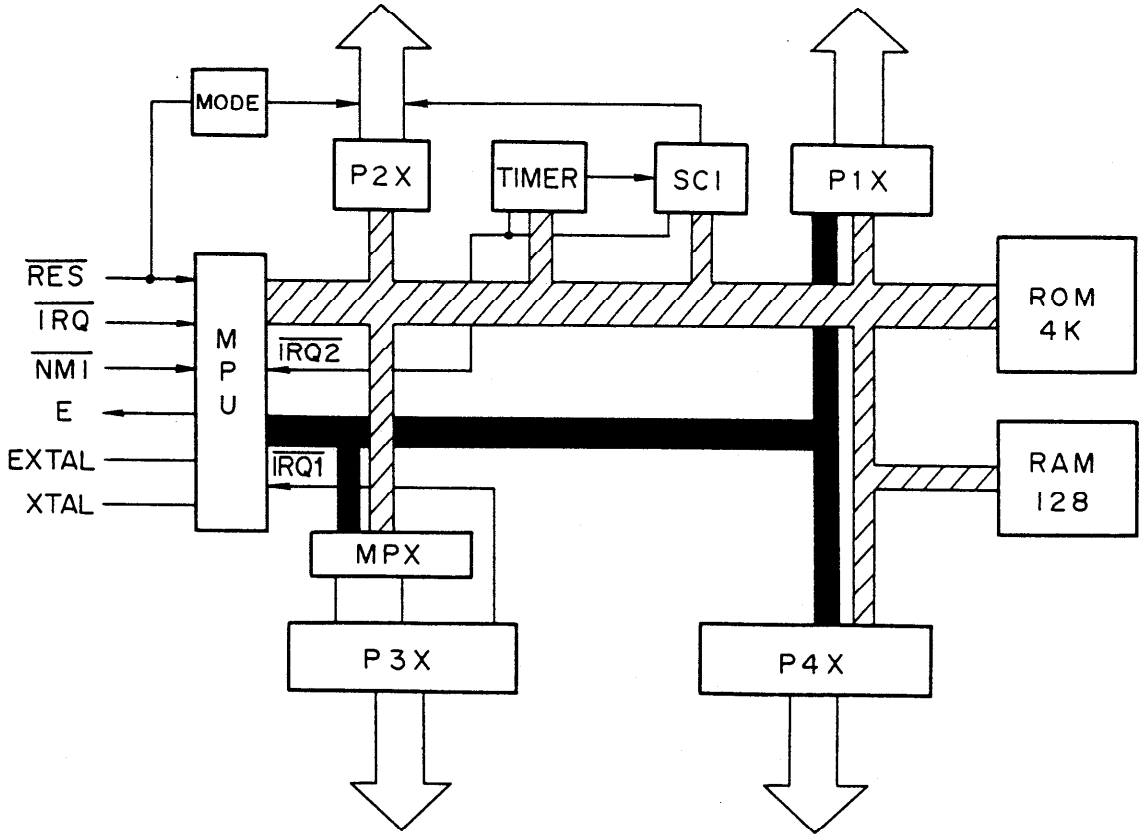


Fig. 7-2 6303 Slave CPU Functional Block Diagram

This computer uses a crystal oscillator for a 2.4576 MHz clock signal. The slave CPU operates with the 614.4 kHz system clock signal which is internally quartered from the primary frequency of 2.4576 MHz. The table opposite shows the port assignment.

Table 7-2

Port	Assignment
Port 1	Parallel I/O terminal
Port 2	Serial I/O terminal
Port 3	Address/data terminal
Port 4	Address terminal

REV.-A

Slave CPU 6303

1. Location: MAPLE Board, 130
2. Pin Assignment

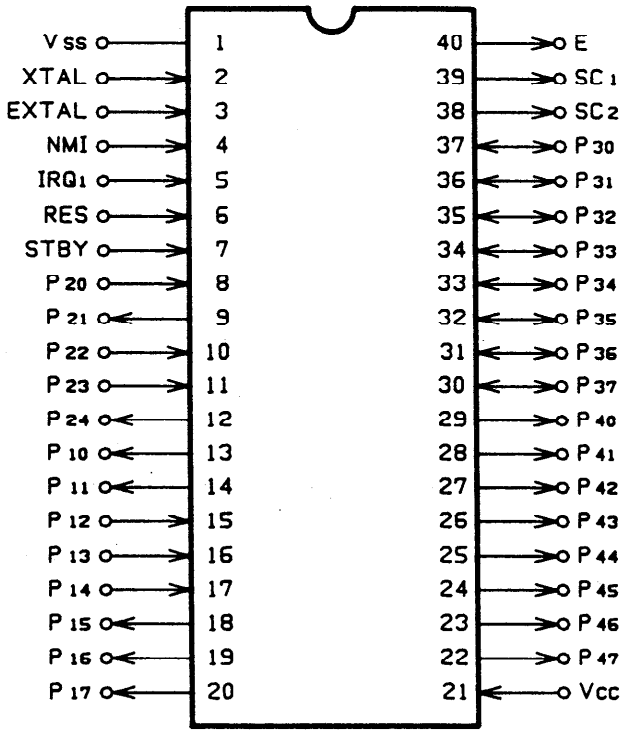


Table 7-3 6303 Slave CPU Pin Assignments

Pin No.	Signal Name	In/Out	Function
1	G	–	GND
2	X TAL	In	Unused – reserved for external clock signal input.
3	EX TAL	In	External clock signal input 2.4576 MHz
4	$\overline{NMI}$	In	Unused – reserved for non-maskable interrupt input.
5	$\overline{INTR}$	In	Interrupt request
6	$\overline{RS}$	In	Reset signal
7	$\overline{STB}$	In	Unused – reserved for Stand-by signal input.
8	P20	In	Microcassette tape read data (RDMC)
9	P21	Out	Microcassette tape write data (WD)
10	P22	In	Unused – reserved for operation mode setting.
11	P23	In	Serial interface receive data
12	P24	Out	Serial interface transmit data
13	P10	Out	Microcassette head pinch motor ON/OFF (HMT)

Pin No.	Signal Name	In/Out	Function
14	P11	Out	Microcassette tape erase (ERAH)
15	P12	In	Microcassette tape write enable (WE)
16	P13	In	Microcassette tape head load/unload switch
17	P14	In	Serial interface PIN signal
18	P15	Out	Serial interface POUT signal
19	P16	Out	Speaker output
20	P16	Out	Speaker power on/off
21	VC	In	+5V (Circuit voltage)
22	A15	Out	Address bus
23	A14	Out	Address bus
24	A13	Out	Address bus
25	A12	Out	Address bus
26	A11	Out	Address bus
27	A10	Out	Address bus
28	A9	Out	Address bus
29	A8	Out	Address bus

Pin No.	Signal Name	In/Out	Function
30	DA7	In Out	Data address bus
31	DA6	In Out	Data address bus
32	DA5	In Out	Data address bus
33	DA4	In Out	Data address bus
34	DA3	In Out	Data address bus
35	DA2	In Out	Data address bus

Pin No.	Signal Name	In/Out	Function
36	DA1	In Out	Data address bus
37	DA0	In Out	Data address bus
38	R/$\overline{W}$	Out	Read/Write
39	AS	Out	Address strobe
40	E	Out	ENABLE

7.3 Sub-CPU 7508

This is a 4-bit, C-MOS CPU which incorporates a masked ROM, timer, and serial interface, etc. This CPU is always backed up by the battery, regardless whether power is on or off, it provides the following control functions:

1. Power on/off (POWER switch and an associated program)
2. Keyboard scanning and auto-repeat
3. RESET switch
4. Temperature and battery voltage sensing
5. D-RAM refresh
6. Clock (calendar and alarm services)

The sub-CPU exchanges data with the main CPU in a bit-serial fashion via the gate array GAH40M. Fig. 7-3 is a functional block diagram of the sub-CPU. Table 7-4 lists the terminal signals and summarizes their functions.

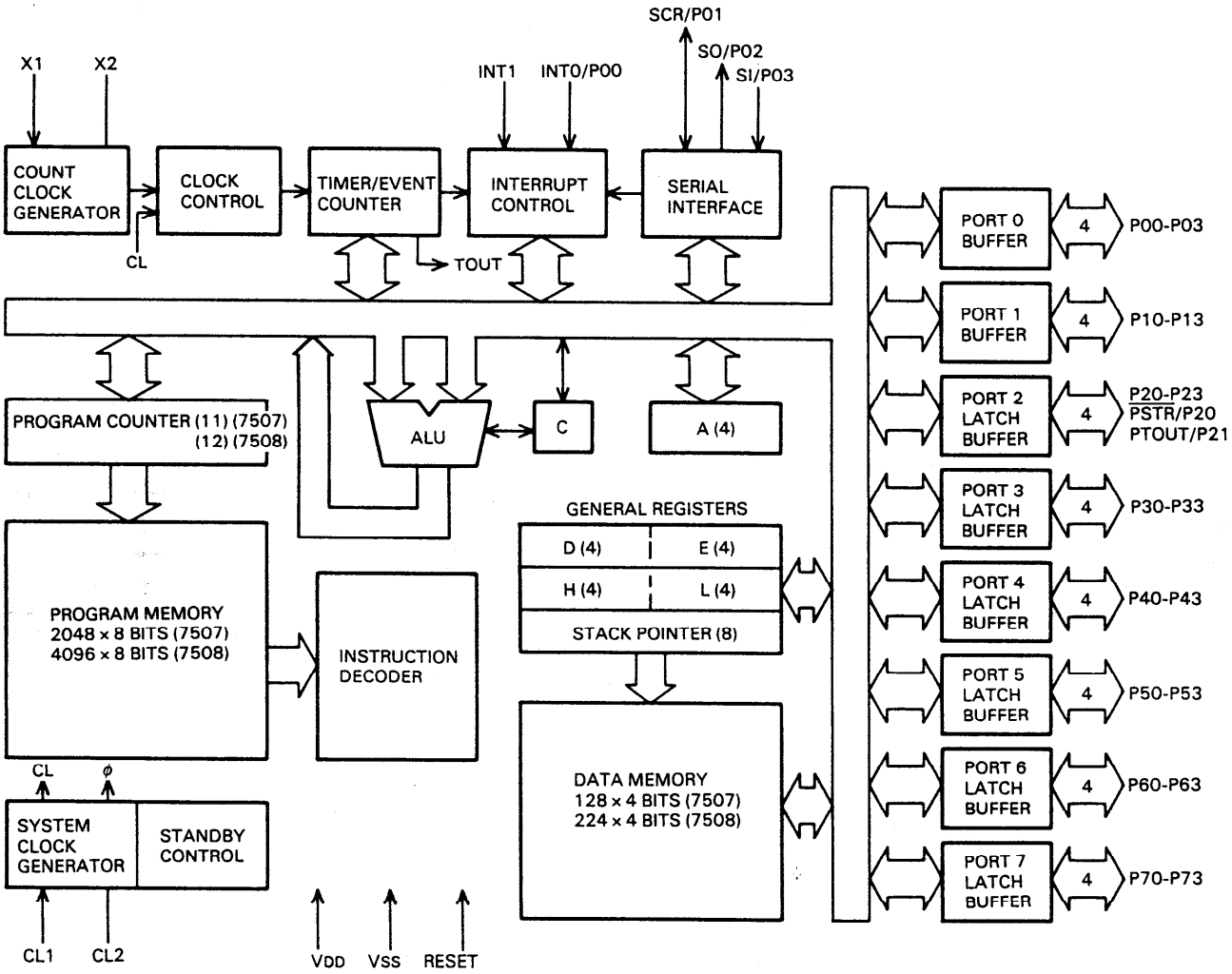


Fig. 7-3

7508 (Sub-CPU)

1. Location: MAPLE Board, 2E
2. Pin Assignments

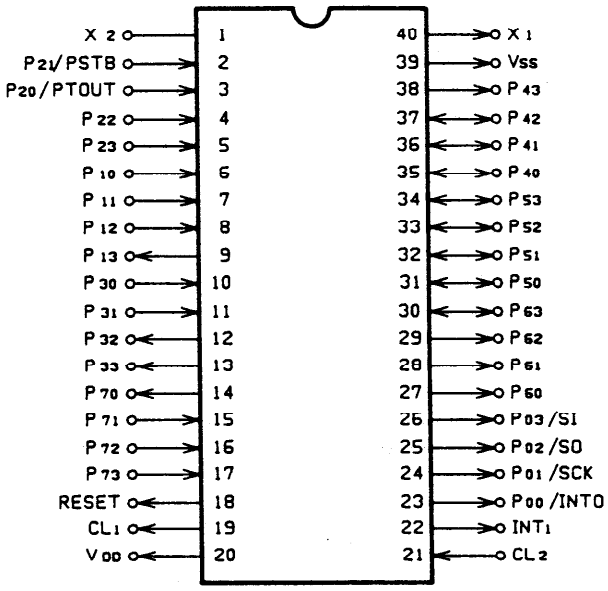


Table 7-4 7508 SUB-CPU Pin Assignments

Pin No.	Signal Name	In/Out	Function
1	x 2	In	Unused.
2	P20	Out	GAH40M SIOR access control – H: 7508, L: Main CPU
3	P21	Out	A-D converter 7001 Chip Select - mode switching between address data and A-D conversion.
4	P22	Out	Ready signal
5	P23	Out	A-D converter 7001 power on/off
6	P10	In	Key return 0
7	P11	In	Key return 1
8	P12	In	Key return 2
9	P13	In	Key return 3
10	P30	Out	Key scan control
11	P31	Out	Key scan control
12	P32	Out	Key scan control
13	P33	Out	Key scan control
14	P70	Out	Power ON/OFF

Pin No.	Signal Name	In/Out	Function
15	P71	Out	Data write – prevents FF latches in gate array at power off.
16	P72	Out	Data write – D-RAM refresh control signal during power off.
17	P73	Out	Data CAS
18	RS	In	Reset signal input
19	CL1	In	Clock signal input
20	VC	In	+5V (Battery voltage: VB) terminal
22	CL2	In	Clock signal input
23	P00/INT0	In	POWER switch
24	$\overline{SCK}$	Out	Shift clock signal output – used for A-D conversion data/main CPU command read.
25	SO	Out	Serial data output
26	SI	In	Serial data output
27	P60	In	RESET switch
28	P61	In	Charge start detection
29	P62	In	Analog interface trigger input
30	P63	In	Test point
31	P50	In	Key return 4
32	P51	In	Key return 5
33	P52	In	Key return 6
34	P53	In	Key return 7
35	P40	Out	Reset signal – initializes main CPU and slave CPU, etc. via GAH40.
36	P41	Out	Charge mode control – normal/trickle charge.
37	P42	Out	Auxiliary battery backup enable/disable control.
38	P43	Out	Interrupt to main CPU
39	G	In	Ground terminal
40	X1	In	External clock signal input – 1 kHz

7.4 Gate Array GAH40D

GAH40D is the gate array for D-RAM control. It controls memory access and memory refresh. It also incorporates a clock frequency divisor which divides 9.8 MHz input to 4.9 MHz, 2.45 MHz, 32 KHz and 1 KHz of clock frequency. Fig. 7-4 shows an internal block of diagram of the GAH40D.

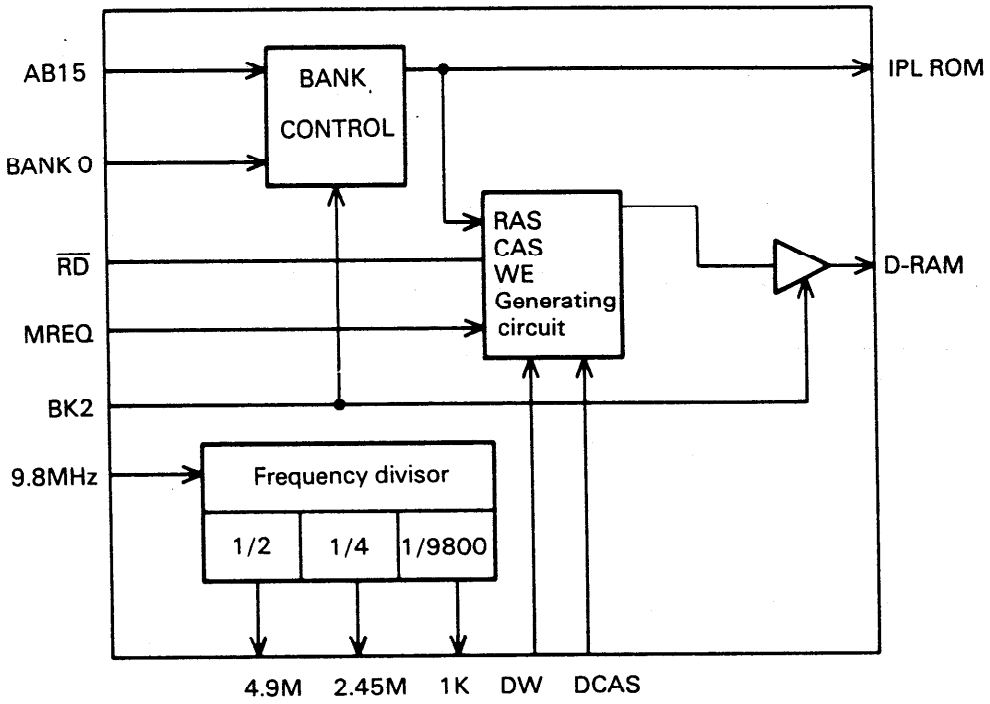


Fig. 7-4

The BANK 0/1 signal is provided from the gate array GAH40M. The main CPU sends this signal by writing bit 0 to I/O address 00. (0: bank 0, 1: bank 1)
BK2 signal is provided from the option unit.

GAH40D

1. Location: MAPLE Board, 6A
2. Pin Assignment

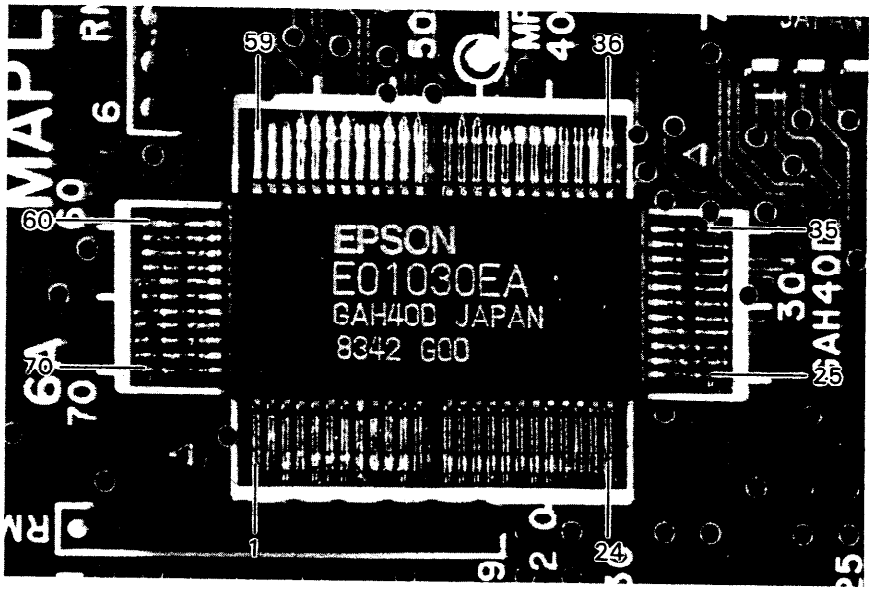


Table 7-5 GAH40D Pin Assignments

Pin No.	Signal Name	In/Out	Function
1	N/C	–	Not used.
2	N/C	–	Not used.
3	AB12	In	Address bus 12
4	N/C	–	Not used.
5	AB 6	In	Address bus 6
6	AB 13	In	Address bus 13
7	AB 5	In	Address bus 5
8	$\overline{RST}$	In	Reset input from sub-CPU 7508. Whole reset signal $\overline{RSQ}$ is generated from this signal.
9	DRA 2	Out	DRAM address 2 (10)
10	DRA 1	Out	DRAM address 1 (9)
11	AB 14	In	Address bus 14
12	G	–	Ground

Pin No.	Signal Name	In/Out	Function
13	AB 4	In	Address bus 4
14	AB 15	In	Address bus 15
15	AB 3	In	Address bus 3
16	DRA 0	Out	DRAM address 0(8)
17	$\overline{\text{RAS1}}$	Out	Low address stroke: RAS signal to RAS.
18	W1	Out	Write enable: WE signal to DRAM.
19	AB 2	In	Address bus 2
20	AB 1	In	Address bus 1
21	AB 0	In	Address bus 0
22	N/C	–	Not used
23	N/C	–	Not used
24	N/C	–	Not used
25	$\overline{\text{RD}}$	In	Read signal
26	$\overline{\text{CSROM}}$	Out	IPL ROM chip select signal
27	$\overline{\text{MR}}$	Out	Memory read signal
28	$\overline{\text{Z-INT}}$	Out	Interrupt request signal to main CPU
29	$\overline{\text{Z-RF}}$	In	Refresh signal from main CPU
30	VC	–	Circuit voltage (+5V)
31	$\overline{\text{HLTA}}$	In	Halt signal
32	$\overline{\text{M1}}$	In	Indicates that main CPU is in machine cycle 1 (opcode fetch)
33	$\overline{\text{MRQ}}$	In	Memory request signal
34	$\overline{\text{RSO}}$	Out	System reset signal resets the whole machine.
35	DRA 3	Out	DRAM address 3 (11)
36	N/C	–	Not used
37	N/C	–	Not used
38	DRA 7	Out	DRAM address 7 (15)
39	N/C	–	Not used

Pin No.	Signal Name	In/Out	Function
40	$\overline{RF}$	Out	Refresh signal for DRAM
41	DRA 4	Out	DRAM address 4 (12)
42	DRA 5	Out	DRAM address 5 (13)
43	DRA 6	Out	DRAM address 6 (14)
44	$\overline{CAS1}$	Out	Column address strobe: CAS signal to DRAM
45	$\overline{S\text{-}INT}$	In	Interrupt signal from gate array GAH40M. Generates $\overline{Z\text{-}INT}$ signal and causes an interrupt to main CPU.
46	BANK 1/0	In	Bank 0: Bank select signal from gate array GAH40M. Bank 0 at low level and IPL ROM is selected at $\overline{AB15}$.
47	G	–	Ground
48	4.9 M	Out	Clock output gained by dividing 9.8 MHz clock. Supplied to SED1320.
49	9.8 M	In	Clock input of 9.8404 MHz
50	$\overline{2.45\ M}$	Out	Clock output by dividing 9.8 MHz clock into four. Clock for main CPU.
51	1KC	Out	Clock output by dividing 32 KHz clock to 32. Clock for sub-CPU 7508.
52	TEST	In	Test terminal. Normally kept low.
53	OFF	In	Initializes signal for the whole internal circuit. At high level, initializes all FFs. Hold 4.9 M, 2.45 M, $\overline{CS\ ROM}$, $\overline{RD}$ and $\overline{Z\text{-}INT}$ at high level and others inactive. Outputs $\overline{RSO}$.
54	32K	In	Basic clock input of 32.768 KHz. Generates 1 KC (Clock).
55	DW	In	Data write signal. W1 (write enable) control data supplied from sub-CPU 7508 when main CPU is on standby.
56	DCAS	In	Data CAS. CAS 1 control data supplied from sub-CPU 7508 when main CPU is standby.
57	N/C	–	Not used
58	N/C	–	Not used

Pin No.	Signal Name	In/Out	Function
59	N/C	–	Not used
60	N/C	–	Not used
61	N/C	–	Not used
62	N/C	–	Not used
63	N/C	–	Not used
64	$\overline{BK2}$	In	DRAM select signal from option unit.
65	VC	–	Circuit voltage (+5V)
66	AB 10	In	Address bus 10
67	AB 9	In	Address bus 9
68	AB 8	In	Address bus 8
69	AB 11	In	Address bus 11
70	AB 7	In	Address bus 7

7.5 Gate Array GAH40M (E01031AA)

This gate array incorporates the following functional blocks; the operation is controlled by the Z80 main CPU.

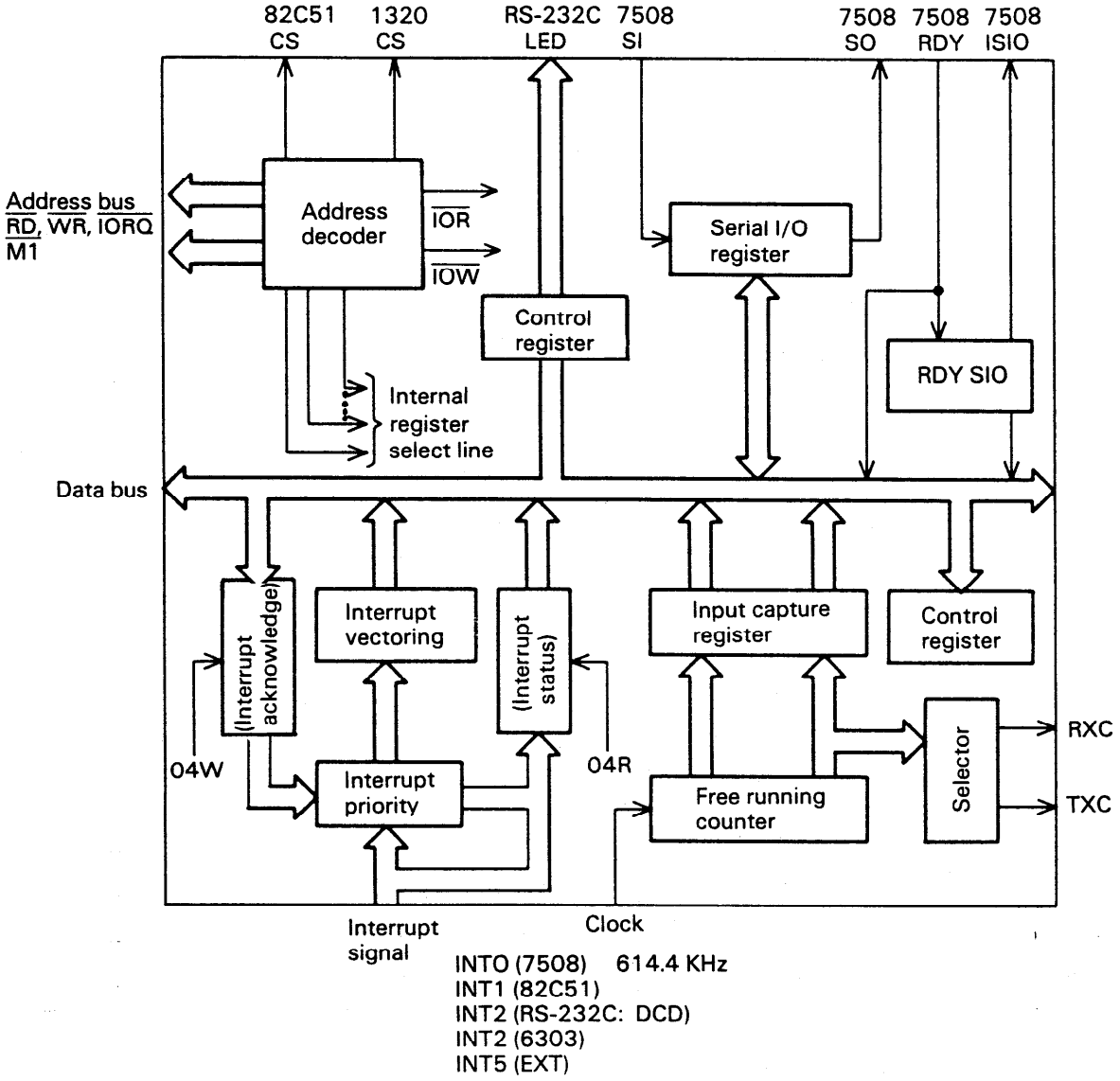


Fig. 7-5

As shown in Fig. 7-5, this gate array includes the address decoder, the 7508 interface, an interrupt controller, a timer and baud rate generator, and I/O ports for the RS-232C and the LED display.

Table 7-6

Write			Read	
00 CTLR1			00 ICLR · C	
7	BRG 3	Baud rate generator select 3 timer	7	ICR7
6	BRG 2	Baud rate generator select 2 timer	6	ICR6
5	BRG 1	Baud rate generator select 1 timer	5	ICR5
4	BRG 0	Baud rate generator select 0 timer	4	ICR4
③	SWBCD	Barcode reader switch timer	3	ICR3
2	BCD1 (μp)	Barcode mode select 1 timer	2	ICR2
1	BCK0 (down)	Barcode mode select 0 timer	1	ICR1
⓪	$\overline{\text{BANK0}}$	Bank switching	0	ICR0
01 CMDR			01 ICRH · C	
7			7	ICR15
6			6	ICR14
5			5	ICR13
4			4	ICR12
3			3	ICR11
2	1: reset OVF(Pulse)	timer	2	ICR10
1	1: reset RDYSIOFF(Pulse)	SIO	1	ICR9
0	1: set RDYSIOFF (Pulse)	SIO	0	ICR8
02 CTLR2			02 ICRL · B	
7			7	ICR7
6			6	ICR6
⑤	AUX	External auxiliary output	5	ICR5
④	INHRS Inhibit RS-232C	RS232	4	ICR4
③	SWRS RS-232C switch	RS232	3	ICR3
②	LED2	LED	2	ICR2
①	LED1	LED	1	ICR1
⓪	LED0	LED	0	ICR0
03			03 ICRH · B	
			7	ICR15
			6	ICR14
			5	ICR13
			4	ICR12
			3	ICR11
			2	ICR10
			1	ICR9
			0	ICR8

REV.-A

Write	
04 IER	
7	
6	
5	IER5 (INTEXT enable)
4	IER4 (INTOVF enable)
3	IER3 (INTICF enable)
2	IER2 (INT 6303 enable)
1	IER1 (INT 82C51 enable)
0	IER0 (INT 7508 enable)
05	
06 SIOR	
7	SIO 7
6	SIO 6
5	SIO 5
4	SIO 4
3	SIO 3
2	SIO 2
1	SIO 1
0	SIO 0
07	

Read			
04 ISR			
7	0		
6	0		
⑤	INT 5 (INTEXT)	External interrupt	
4	INT 4 (OVF)	Overflow flag timer	
3	INT 3 (ICF)	Input capture flag timer	
②	INT 2 (INT 6303)	6303 interrupt	
①	INT 1 (INT 82C51)	82C51 interrupt	
⓪	INT0 (INT7508)		7508 interrupt
05 STR			
7			
6			
5			
4			
3	RDYSIO	SIO ready	SIO
②	RDY	ready	SIO
①	BRDT	Barcode reader data timer	
0	$\overline{\text{BANK0}}$	$\overline{\text{BANK0}}$	
06 SIOR			
7	SIO 7		
6	SIO 6		
5	SIO 5		
4	SIO 4		
3	SIO 3		
2	SIO 2		
1	SIO 1		
0	SIO 0		

07	During interrupt
	1
	1
	1
	1
Interrupt vectoring	Vect 2
	Vect 1
	Vect

(1) Address Decoder

The address decoder performs each register specification, chip select signal output control of 82C51 (2C) and SED1320 (7C), decoding of I/O read/write signals, etc.

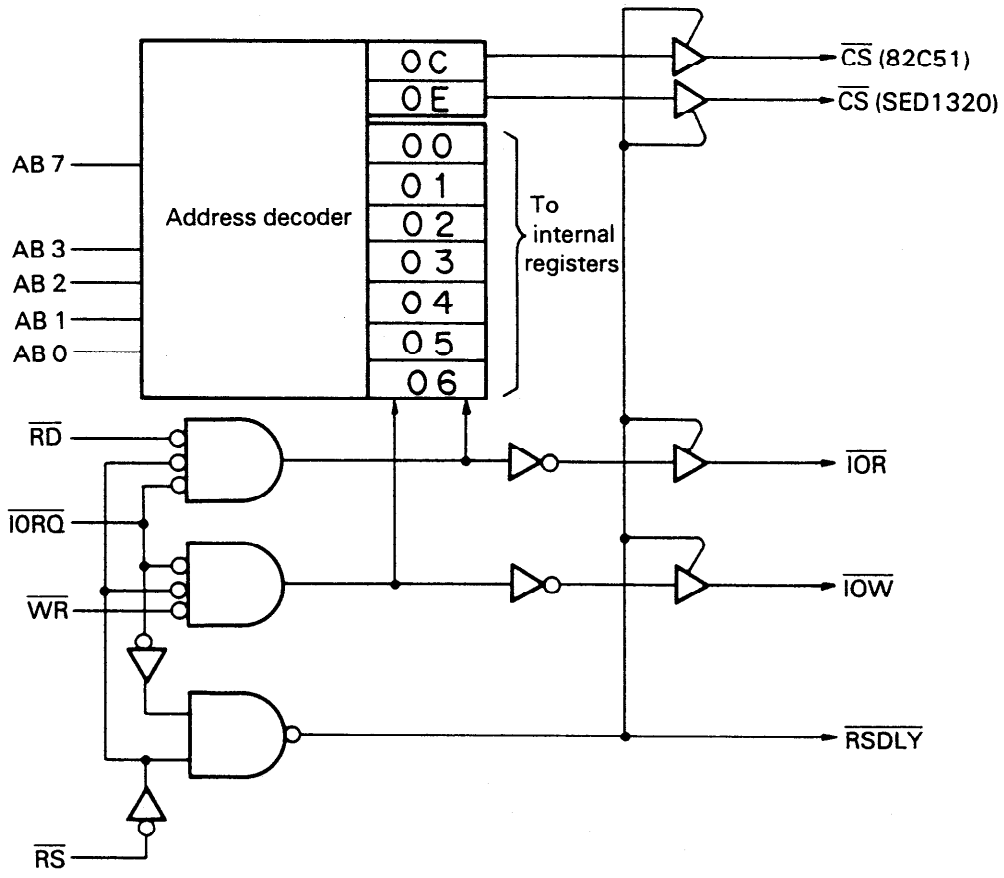


Fig. 7-6

As shown in Figure 7-6, the main CPU can directly select internal registers via four address lines. The CS signals of the 82C51 and SED1320 are also controlled by the I/O address decoder via this registers.

(2) Interrupt Controller

Fig. 7-7 shows six kinds of interrupt input, two of which are used for internal timer interrupt. Priority and vector addresses are assigned to each interrupt signal as shown in the table below.

Table 7-7 Priority and Vector Addresses

Priority	Signal Name	Description	Interrupt vector D7 6 5 4 3 2 1 0	Corresponding mask IER (04)	Corresponding status ISR (04)
Low	$\overline{INT5}$	($\overline{INTEXT}$) External pin: request from external expansion board	1 1 1 1 1 0 1 0	IER5	ISR5
	INT4	(OVF) Inside: FRC overflow	1 1 1 1 1 0 0 0	IER4	ISR4
	INT3	(ICF) Inside: ICR bar code trigger	1 1 1 1 0 1 1 0	IER3	ISR3
	$\overline{INT2}$	($\overline{INT6303}$) External pin: request from 6303	1 1 1 1 0 1 0 0	IER2	ISR2
	$\overline{INT1}$	($\overline{INT82C51}$) External pin: request from 82C51	1 1 1 1 0 0 1 0	IER1	ISR1
High	$\overline{INT0}$	($\overline{INT7508}$) External pin: request from 7508	1 1 1 1 0 0 0 0	IER0	ISR0

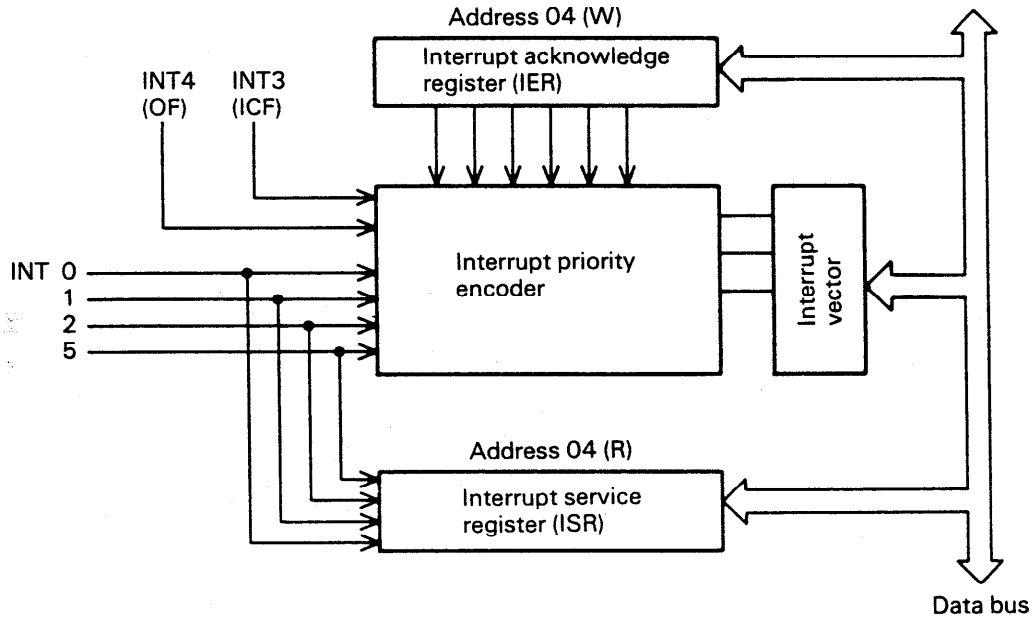


Fig. 7-7

This interrupt controller controls each interrupt acknowledge and mask operation at bit setting for IER. When an interrupt occurs, a vector address is output on the data bus.

(3) Timer and baud rate generator

An 2.4576 MHz clock supplied from the outside is divided into a basic clock of 614.4 KHz (1.6276 μsec) which operates the free running counter (FRC). FRC is a counter of 16 bits; the low-order, 8 bit output of the FRC Cover is also used for the RS-232C transmit/ receive clock.

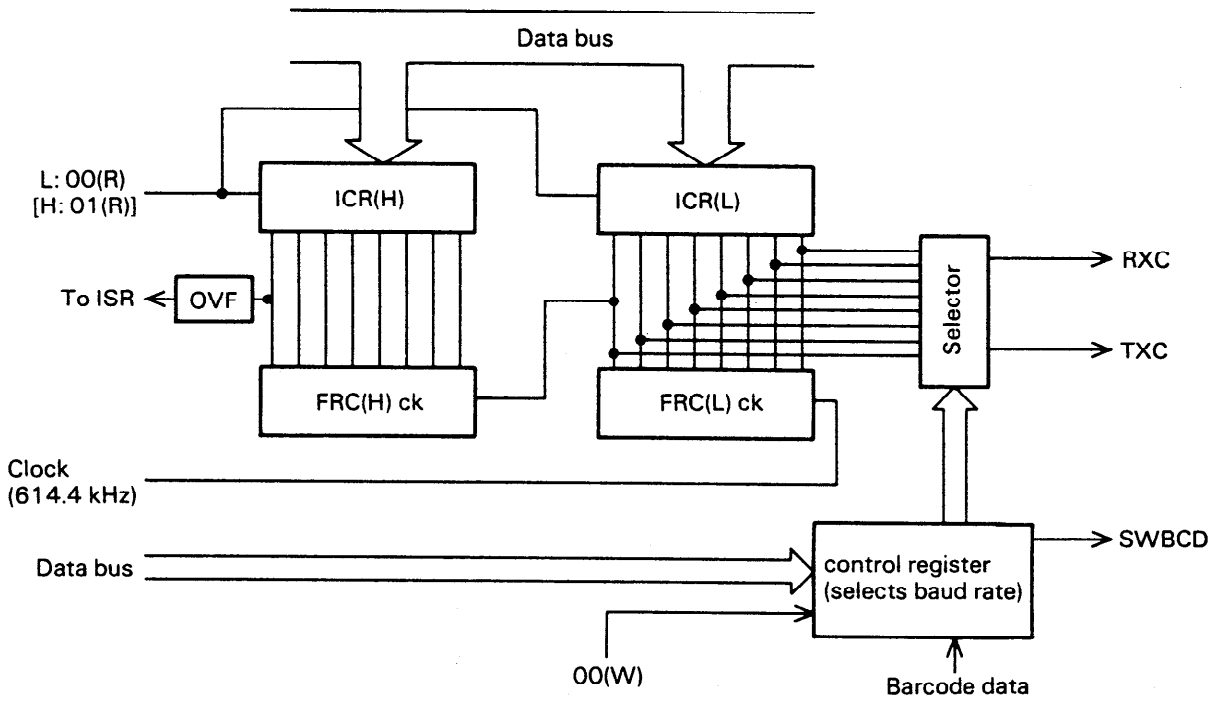


Fig. 7-8

When reading the content of FRC, it is necessary to latch the content to ICR (Input Capture Register) by reading address 00H. Because the counter consists of 16 bits, address 00H (low-order 8 bits) and 01H (high-order 8 bits) must be read separately.

Bits 1 and 2, set to the control register, combined with input data cause a trigger signal from BRDT; this signal allows data going to ICR from FRC to be latched.

(4) 7508 interface

The 7508 interface contains the circuitry for handshaking between the parallel-serial converting register on the main CPU and 7508.

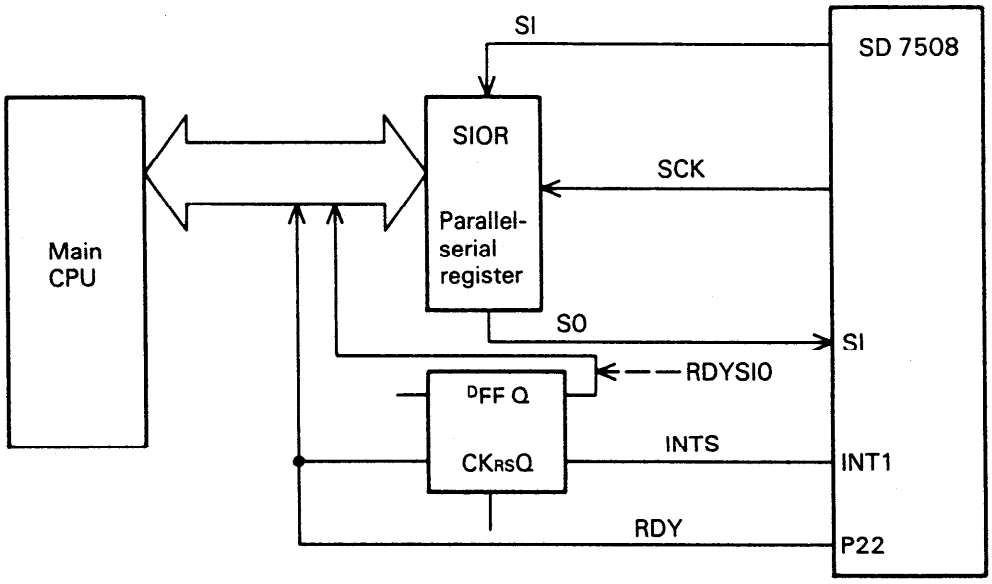


Fig. 7-9

Handshaking is performed in the internal flip-flop. When it is set, it means that the main CPU can access SIOR. When it is reset, it means that an interrupt signal is sent to the 7508 and the command set at SIOR is read by the 7508. The internal flip-flop is controlled by bits 0 and 1 of address 0IH.

After the R/W operation to/from SIOR is completed, the set status must be changed by writing to address 0IH.

Table 7-8

Address 0IH Bit 1	Reset RDYSIO	The main CPU sets a command to SIOR and requests processing to 7508.
Address 0IH Bit 0	Set RDYSIO	The power is turned on and access to 7508 is completed.

(5) I/O port

Power supply for the RS-232C, memory bank switching, and LED display on keyboard are controlled through the I/O port.

(RS-232C)

Fig. 7-10 controls power increases

The bits 3 and 4 of I/O address 02H.

±8V output is controled by the INHRS signal, and is performed in order to inhibit output voltage on the line during saturation time.

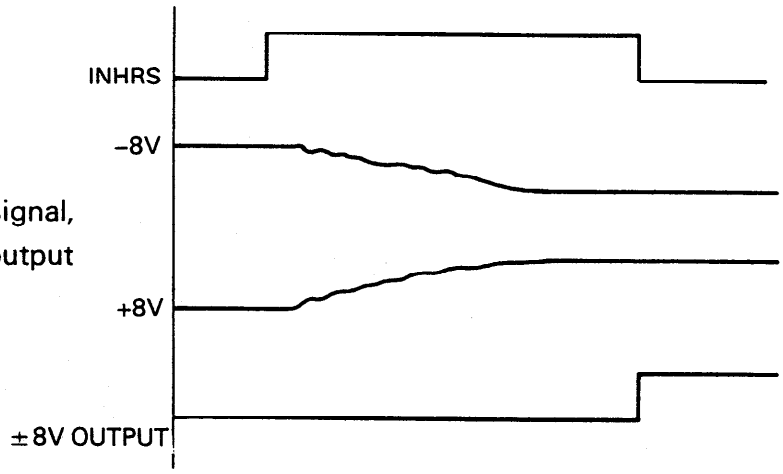


Fig. 7-10

(Bank switch)

The address space of the main CPU can be changed using bit 0 of I/O address 00H as shown below.

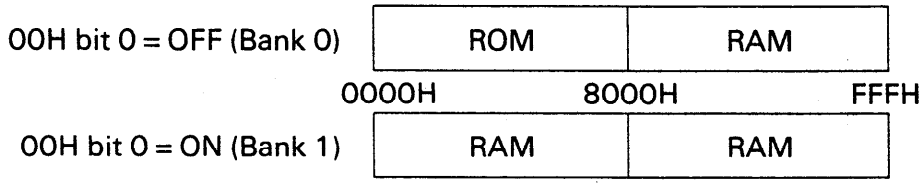


Fig. 7-11

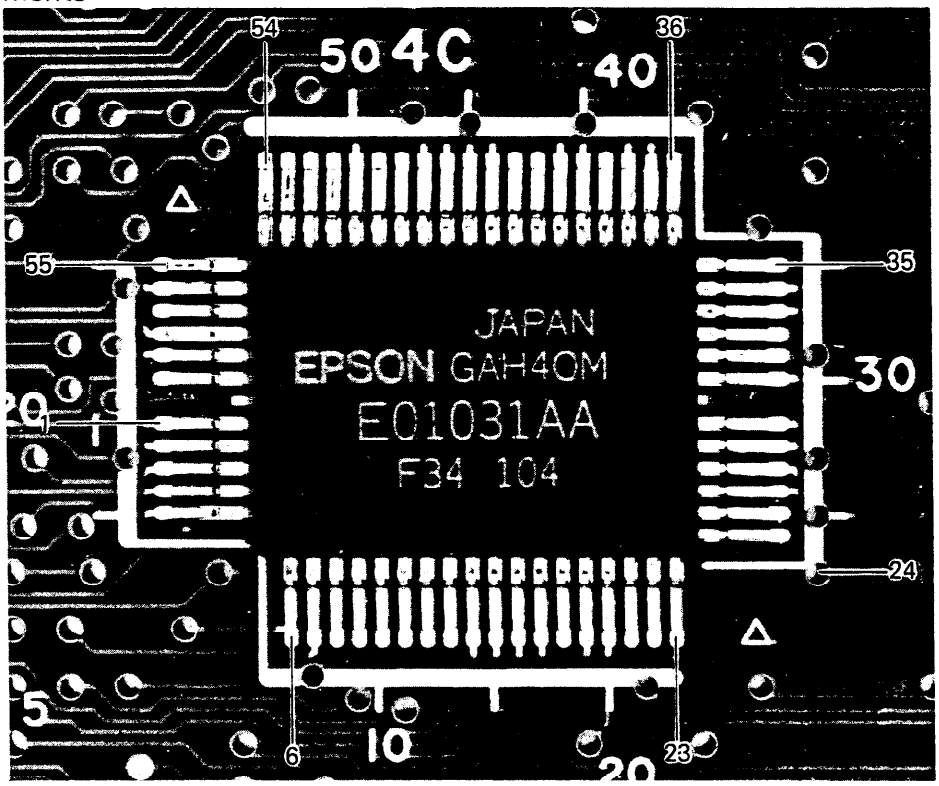
(LED display)

ON/OFF operation of shift mode LED on the keyboard is controlled using bits 0 to 2 of address 02H. (Bit ON drives the corresponding LED.)

REV.-A

GAH40M

1. Location: MAPLE Board, 4C
2. Pin assignments



Note: Pins 25 and 59 are cut.

Table 7-9 GAH40M Pin Assignments

Pin No.	Signal Name	In/Out	Function
1	DB6	In/Out	Data bus 6
2	DB1	In/Out	Data bus 1
3	$\overline{IR}$	Out	Indicates that data is being output according to main CPU instruction (RS-232C → main CPU).
4	DB 0	In/Out	Data bus 0
5	DB 2	In/Out	Data bus 2
6	$\overline{CSOE}$	Out	SED1320 chip select signal
7	$\overline{RS}$	In	Reset input: Supplied from GAH40D.
8	$\overline{IW}$	Out	Indicates that data is being input according to main CPU instruction (main CPU → RS-232C).
9	N/C	–	Not used.
10	TXC	Out	Baud rate control clock (for RS-232C).

Pin No.	Signal Name	In/Out	Function
11	$\overline{\text{INT0}}$	In	Sub-CPU 7508 interrupt signal
12	SWBCD	Out	Barcode power supply (+5V) switching signal
13	RXC	Out	Clock which controls receive character synchronization (RS-232C).
14	BCD	In	Bar code read data
15	CSIO	In	HIGH: Indicates that sub-CPU 7508 can access SIOR. LOW: Indicates that main CPU can read/write.
16	SI	In	Serial data input from sub-CPU 7508.
17	SO	Out	Serial data output to sub-CPU 7508.
18	$\overline{\text{S-INT}}$	Out	Interrupt signal to main CPU. Gives an interrupt via GAH40D ($\overline{\text{Z-INT}}$ signal).
19	DB 5	In/Out	Data bus 5
20	DB 3	In/Out	Data bus 3
21	N/C	–	Not used.
22	N/C	–	Not used.
23	N/C	–	Not used.
24	N/C	–	Not used.
25	N/C	–	Not used.
26	SWRS	Out	Switching signal for RS-232C power supply
27	INHRS	Out	Controls output voltage during power saturation time of RS-232C.
28	OFF	In	Power off. To prevent latch-up by isolating output in high impedance.
29	G	–	Ground
30	TEST	In	Test terminal. Normally kept low level.
31	N/C	–	Not used.
32	AUX	Out	RS-232C transmit/receive line control

Pin No.	Signal Name	In/Out	Function
33	$\overline{\text{INT 1}}$	In	Serial controller 82C51 interrupt signal
34	$\overline{\text{INT 5}}$	In	Interrupt signal from option unit
35	N/C	–	Not used.
36	SCK	In	Data transmit/receive shift clock against SIOR register. Provided from sub-CPU 7508.
37	$\overline{\text{INT 2}}$	In	RS-232C CD signal interrupt signal
38	$\overline{\text{RD}}$	In	Read signal: Synchronized to AND of IORQ. Outputs data on data bus.
39	AB 1	In	Address bus 1
40	$\overline{\text{WR}}$	In	Write signal: Synchronized to AND of IORQ. Outputs data on data bus.
41	INTS	Out	Interrupt signal to sub-CPU 7508
42	AB 0	In	Address bus 0
43	RDY	In	Ready signal of sub-CPU
44	LED 2	Out	Lamp control signal of LED on keyboard (lowest of the three)
45	AB 7	In	Address bus 7
46	LED 1	Out	Lamp control signal of LED on keyboard (highest of the three)
47	LED 0	Out	Lamp control signal of LED on keyboard (center of the three)
48	$\overline{\text{IORQ}}$	In	Main CPU in MI cycle: Request to output interrupt response vector on data bus.
49	AB 2	In	Address bus 2
50	$\overline{\text{CSOC}}$	Out	Serial controller 82C51 chip select signal.
51	$\overline{\text{BANK0/1}}$	Out	Bank select signal
52	$\overline{\text{M1}}$	In	Main CPU in machine cycle 1: Interrupt response vector is read to main CPU by AND operation with IORQ.
53	N/C	–	Not used.

Pin No.	Signal Name	In/Out	Function
54	N/C	–	Not used.
55	N/C	–	Not used.
56	DB 4	In/Out	Data bus 4
57	AB 7	In	Address bus 27
58	DB 7	In/Out	Data bus.
59	2.45	In	2.45 MHz clock on which timer and baud rate generator are based.
60	VC	–	Circuit voltage (+5V)

7.6 Gate Array GAH40S

Gate array GAH40S, which is controlled by the 6303 slave CPU, in turn controls the microcassette tape drive, LCD controller, and ROM capsule. It consists of three segments: an address decoder, a microcassette tape drive interface, and a P-ROM interface. Figs. 7-12 through 7-14 are functional block diagrams of these blocks.

(1) Address decoder block

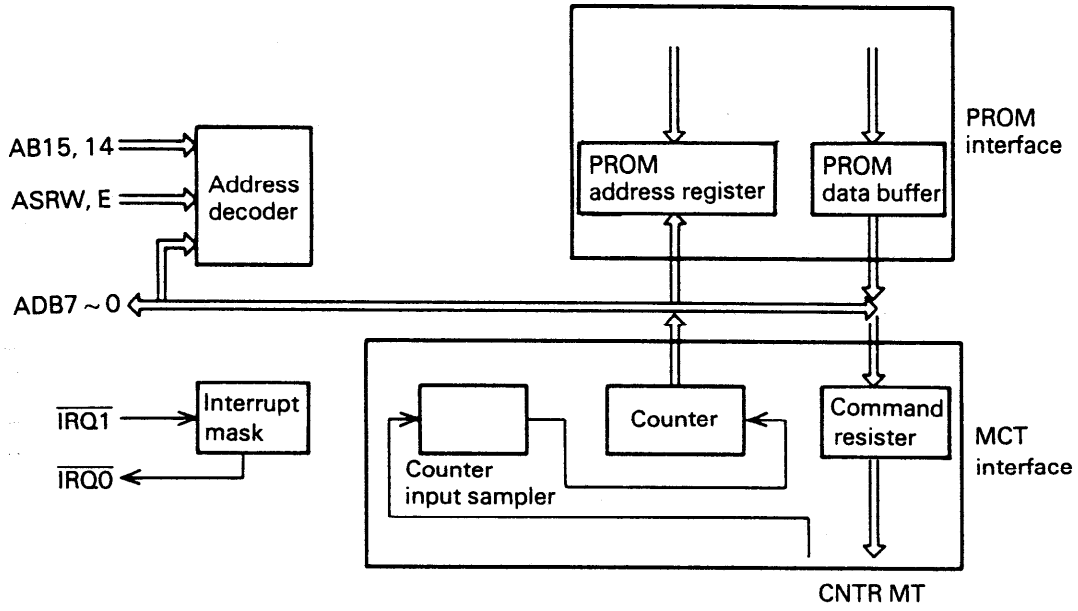


Fig. 7-12 Address decoder block diagram

(2) P-ROM interface block

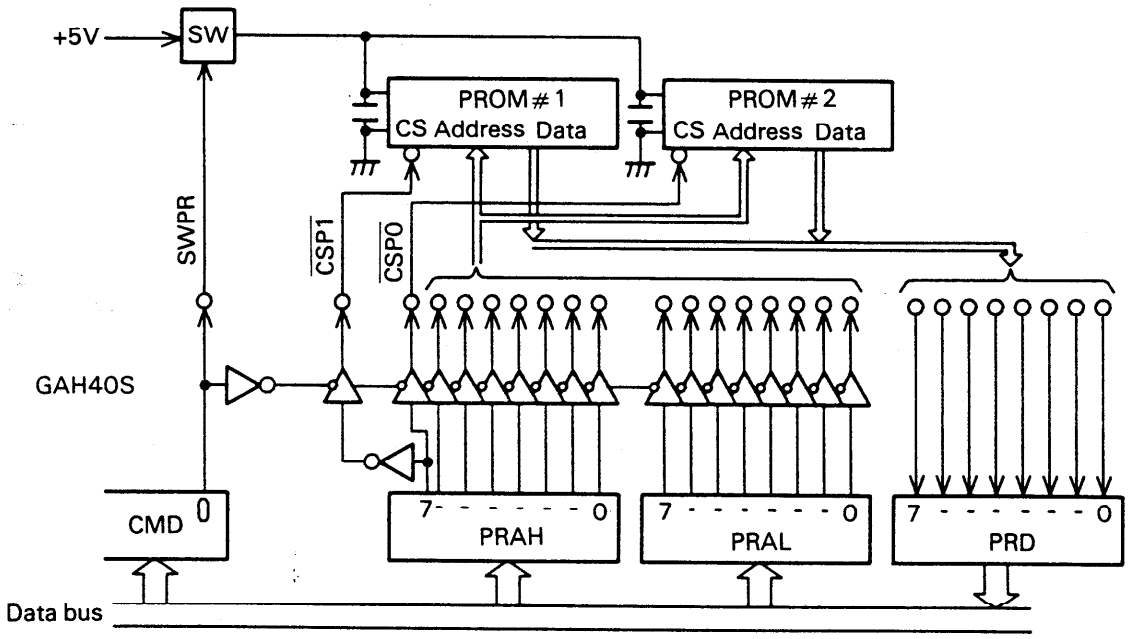


Fig. 7-13 P-ROM Interface Block Diagram

(3) Microcassette tape drive interface block

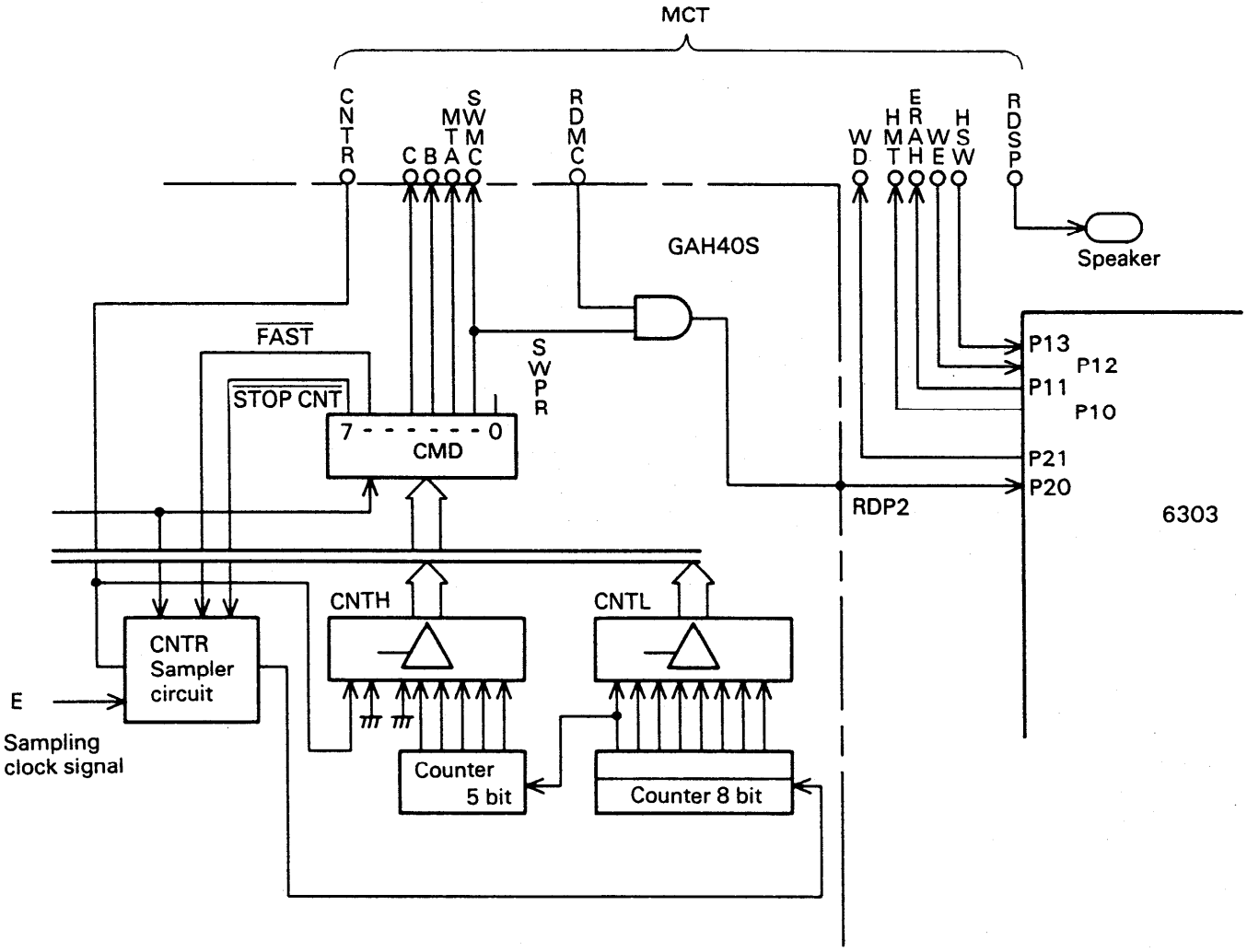
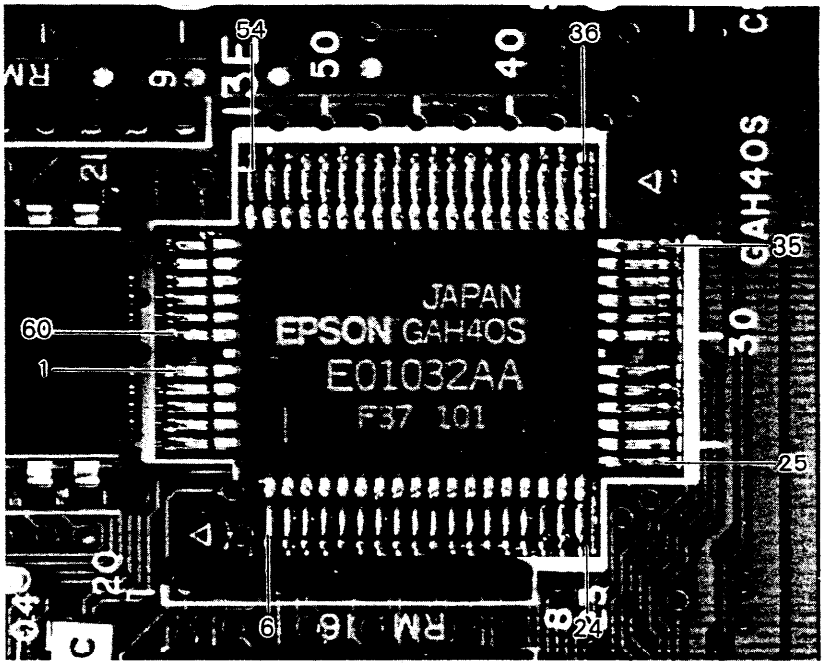


Fig. 7-14 Microcassette Tape Drive Interface Block Diagram

GAH40S

1. Location: MAPLE Board, 13E
2. Pin assignments



Note: Pins 25, 27 are cut.

Table 7-10 GAH40S Pin Assignments

Pin No.	Signal Name	In/Out	Function
1	PRA 12	Out	PROM address 12
2	PRA 14	Out	PROM address 14
3	PRA 7	Out	PROM address 7
4	PRA 13	Out	PROM address 13
5	PRA 6	Out	PROM address 6
6	PRA 8	Out	PROM address 8
7	PRA 11	Out	PROM address 11
8	PRA 4	Out	PROM address 4
9	PRA 9	Out	PROM address 9
10	PRA 5	Out	PROM address 5
11	PRA 10	Out	PROM address 10
12	PRA 3	Out	PROM address 3
13	PRA 2	Out	PROM address 2

Pin No.	Signal Name	In/Out	Function
14	$\overline{\text{CSP 1}}$	Out	PROM chip select.
15	PRD 0	In	PROM data 0
16	$\overline{\text{CSP 0}}$	Out	Chip select
17	PRD 7	In	PROM data 7
18	PRA 1	Out	PROM address 1
19	PRA 0	Out	PROM address 0
20	PRD 6	In	PROM data 6
21	PRD 1	In	PROM data 1
22	PRD 4	In	PROM data 4
23	PRD 3	In	PROM data 3
24	PRD 2	In	PROM data 2
25	PRD 5	In	PRD data 5
26	MTDA	Out	Microcassette drive motor control signal A
27	MTDB	Out	Microcassette drive motor control signal B
28	MTDC	Out	Microcassette drive motor control signal C
29	G	–	Ground
30	N/C	–	Not used
31	SWMCT	Out	Microcassette power switch
32	CNTR	In	Counter signal from microcassette
33	RDMC	In	Microcassette read data
34	$\overline{\text{CSLV}}$	Out	SED1320 VRAM chip select signal. Low level when addresses 8000 to BFFF are specified.
35	N/C	–	Not used.
36	$\overline{\text{CSLC}}$	Out	SED1320 internal register select signal. Low level when addresses 0024 to 0027 are specified.
37	AB15	In	Slave CPU address 15
38	AB14	In	Slave CPU address 15
39	N/C	–	Not used.

Pin No.	Signal Name	In/Out	Function
40	N/C	–	Not used.
41	DA 0	In/Out	Slave CPU address data bus 0
42	DA 4	In/Out	Slave CPU address data bus 4
43	DA 5	In/Out	Slave CPU address data bus 5
44	DA 6	In/Out	Slave CPU address data bus 6
45	DA 1	In/Out	Slave CPU address data bus 1
46	DA 7	In/Out	Slave CPU address data bus 7
47	DA 3	In/Out	Slave CPU address data bus 3
48	DA 2	In/Out	Slave CPU address data bus 2
49	E	In	Enable signal from slave CPU 6303
50	N/C	–	Not used.
51	SWPR	Out	PROM power switch
52	TEST	–	Test terminal. Normally kept low.
53	R/$\overline{W}$	In	Read/write signal from slave CPU 6303
54	$\overline{SINT}$	In	Interrupt signal from SED 1320
55	AS	Out	Address strobe signal from slave CPU 6303
56	PRD	Out	AND output from RDMC input and SMMC. Outputs RDMC input to terminal when SWMC is high.
57	N/C	–	Not used.
58	RS	In	Reset signal
59	$\overline{IRQ0}$	Out	Interrupt request signal to slave CPU
60	VC	–	Circuit voltage (+5V)

7.7 A-D Converter μPD7001

The μPD7001 is an 8-bit, C-MOS serial output, analog-to-digital converter which incorporates a 4-channel analog input multiplexer. In this computer, the reference voltage is set to +2.0V, providing an effective resolution of the upper six bits. The LSB corresponds to approximately 0.03V. It employs a sequential comparison A-D conversion method, and requires a conversion time of 140μs.

The computer assigns the analog input channels for battery voltage sensing, temperature sensing, barcode data input, and external analog signal input. Fig. 7-15 is a functional block diagram and Fig. 7-16 outlines the timing relationships among the operating signals.

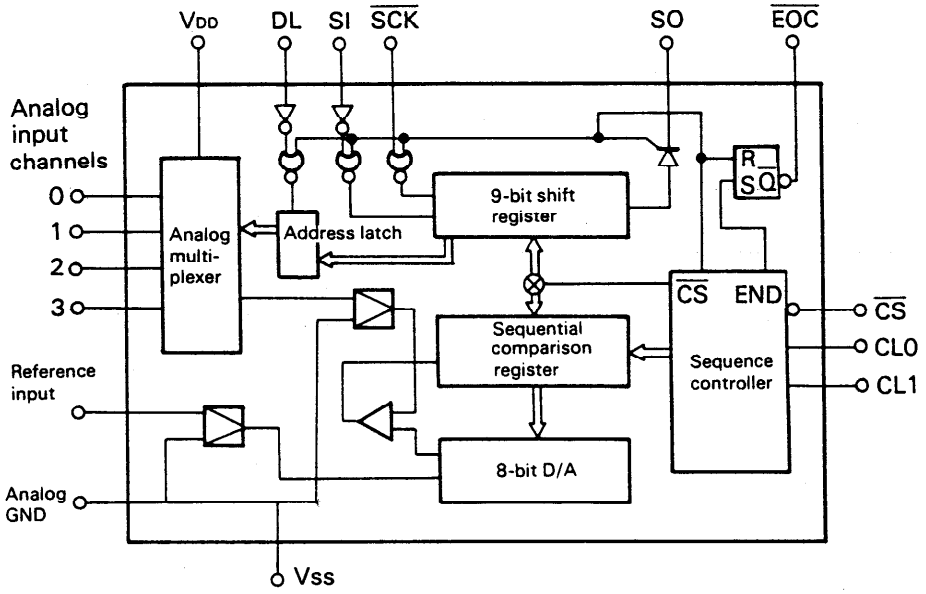


Fig. 7-15 A-D Converter μPD7001 Block Diagram

Timing chart

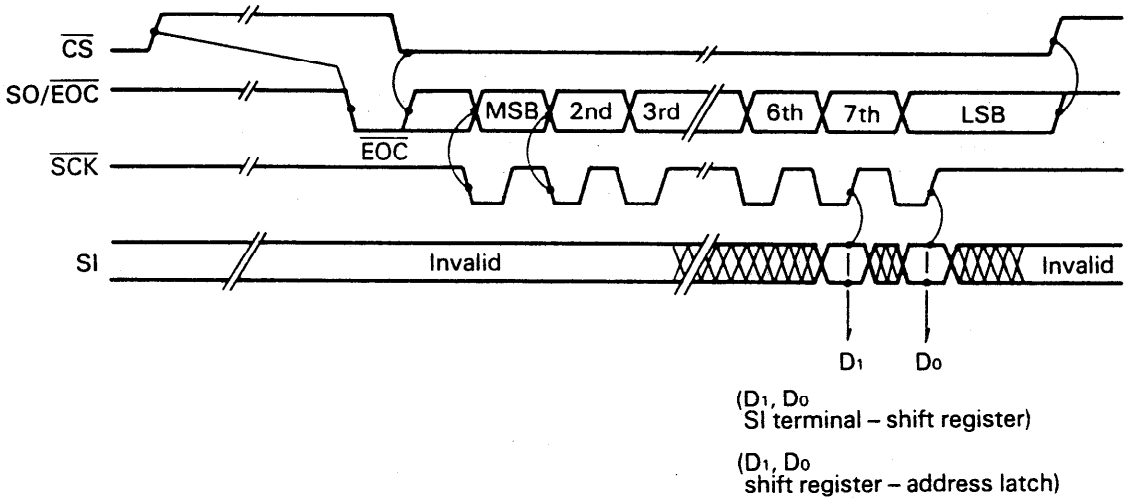


Fig. 7-16 A-D Converter Operation Timing Chart

REV.-A

μPD7001

1. Location: MAPLE Board, 1D
2. Pin Assignments

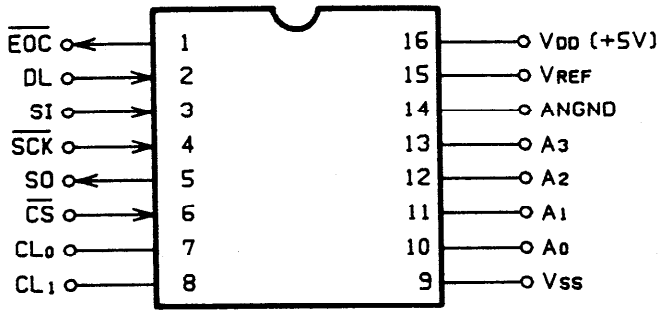
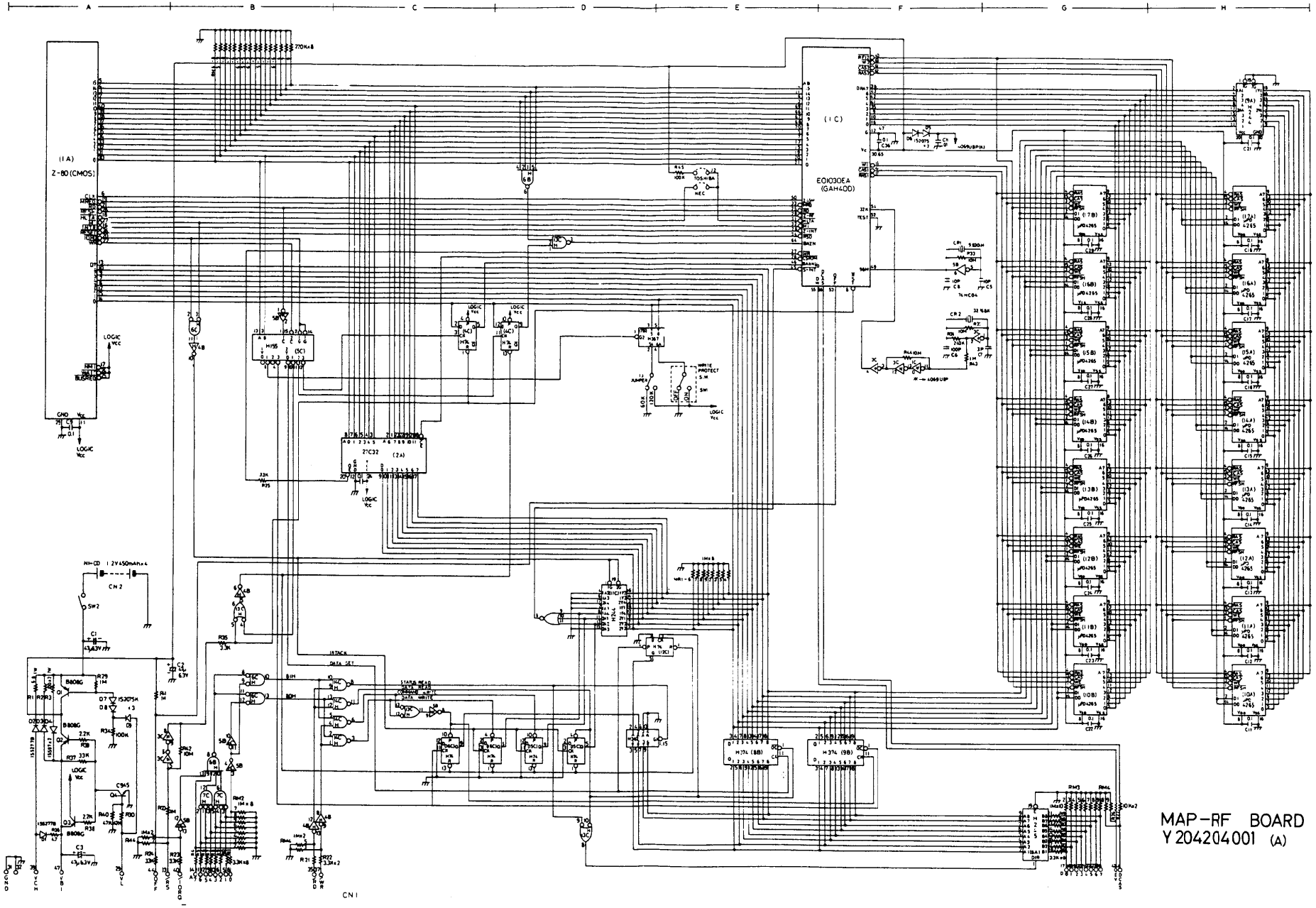
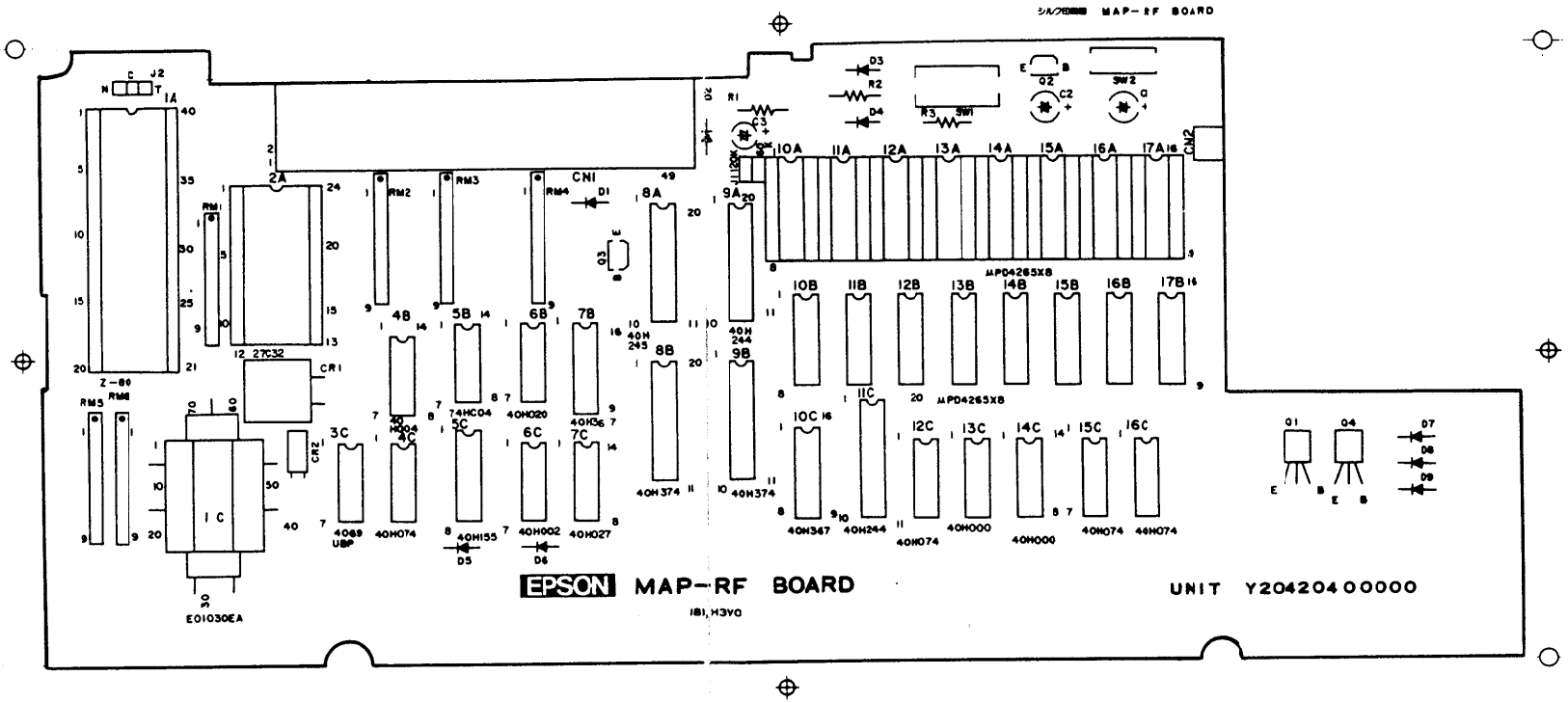


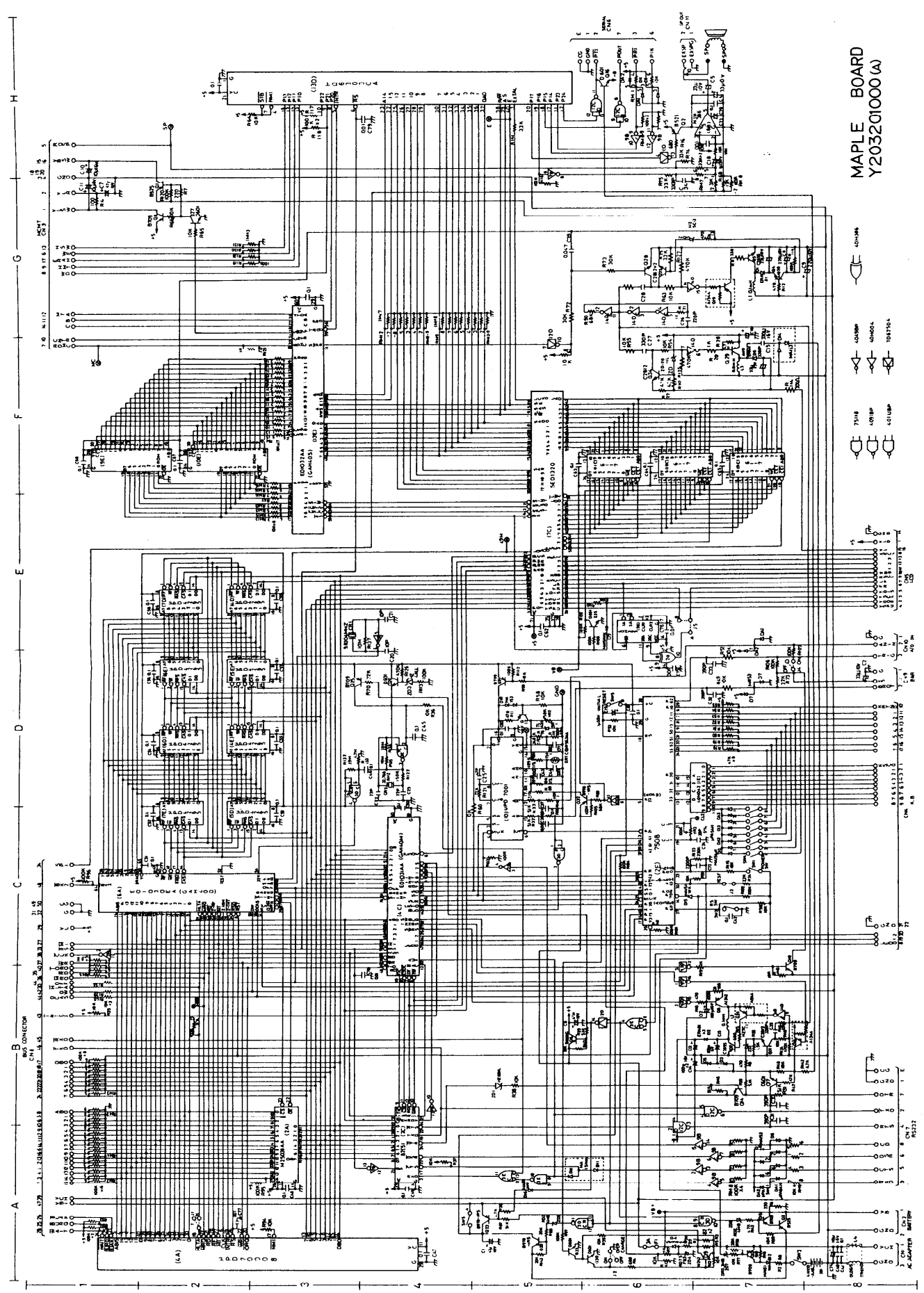
Table 7-11 μPD 7001 Pin Assignments

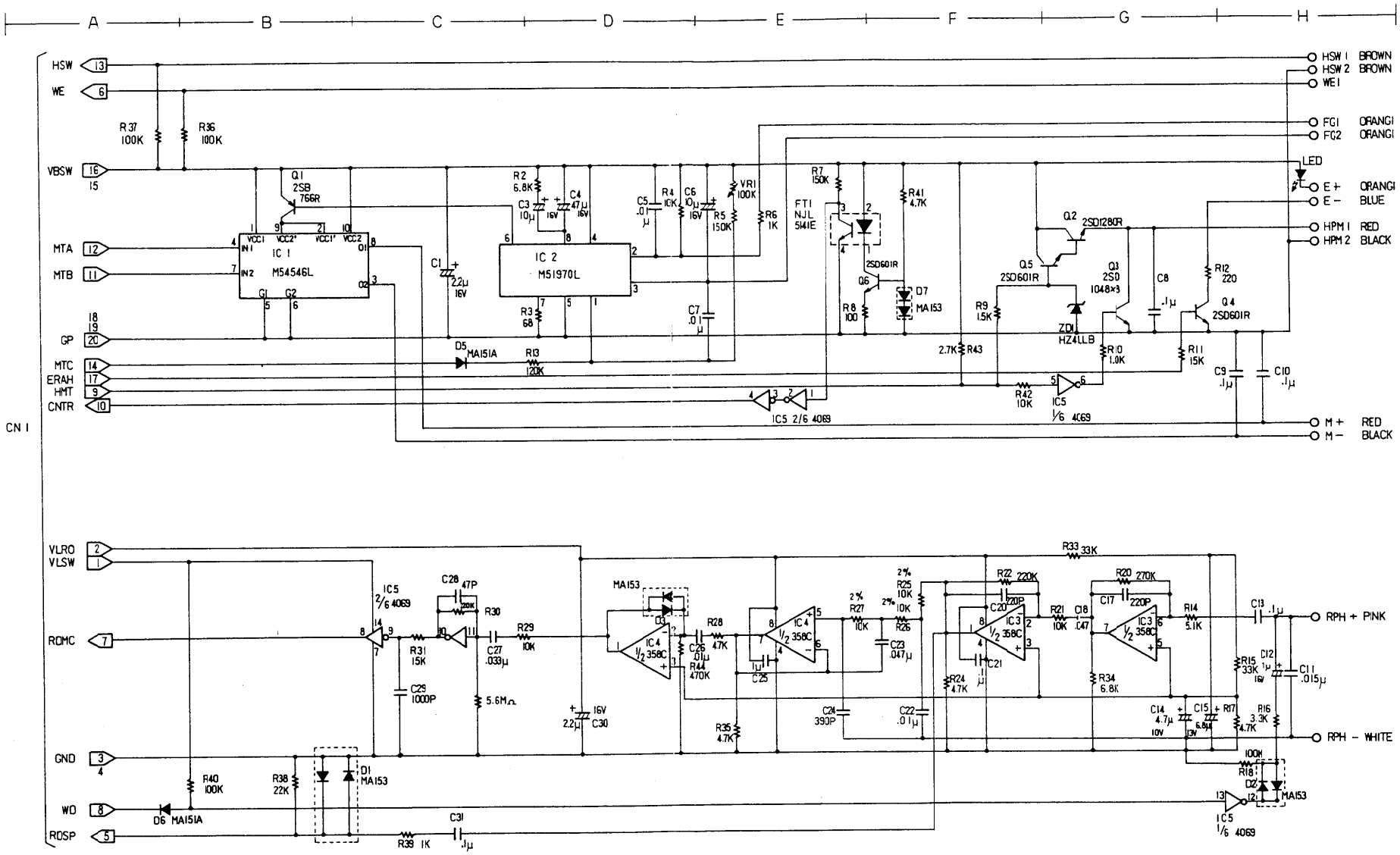
Pin No.	Signal Name	In/Out	Function
1	End of Conversion ($\overline{EOC}$)	Open drain – output	High impedance while $\overline{CS}$ is low, returns low when A – D conversion ends.
2	Data Latch (DL)	In	Latches the multiplexer address in the shift register at its falling edge.
3	Serial Input (SI)	In	Terminal which provides multiplexer address to be read to the shift register. The serial input data is read at the rising edge of the $\overline{SCK}$ signal.
4	Serial Clock ($\overline{SCK}$)	In	Controls the shift operation of the 9-bit interface shift register.
6	Chip Select ($\overline{CS}$)	In	Controls μPD7001's internal modes. When $\overline{CS}$ is high: A-D conversion mode When $\overline{CS}$ is low : Interface mode – DL, SI, $\overline{SCK}$, and SO, etc. have been strobed with $\overline{CS}$. All the terminals are disabled while $\overline{CS}$ is high.
7	Clock (CL_0)	For connection of clock oscillation CR	
8	Clock (CL_1)	For connection of clock oscillation CR	
9	— (Vss)	Externally connect to the GND and analogue GND terminals	
10 ~ 13	Analogue input ($A_0 \sim A_3$)	Analogue input pin	
14	Analogue (GND)	Ground pin for analogue input and reference input	
15	Reference input (V_{REF})	Used for full scale voltage setting. Supply voltage of about +2.5V.	
16	Power supply (Vcc)	Power supply pin (+5V)	

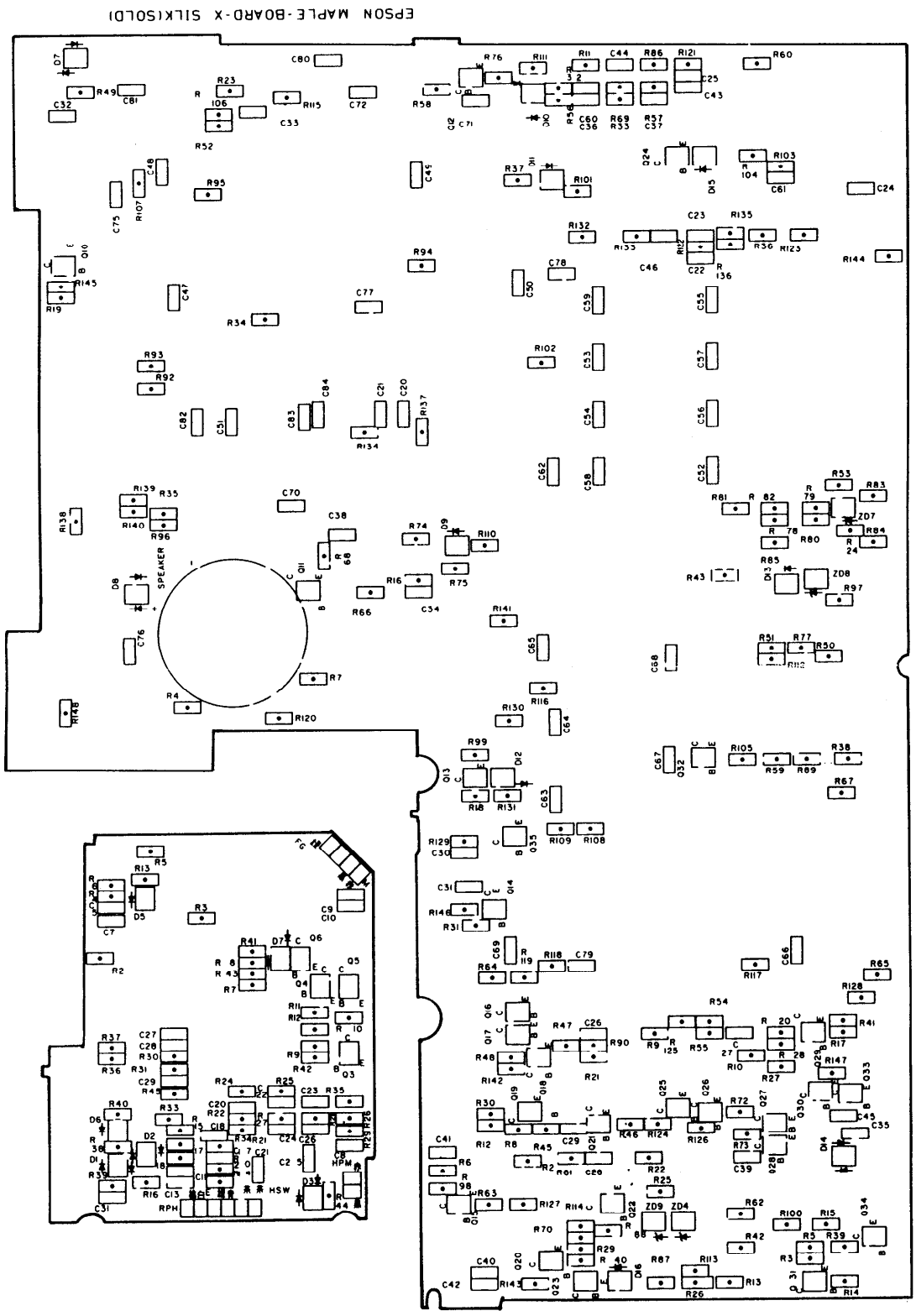


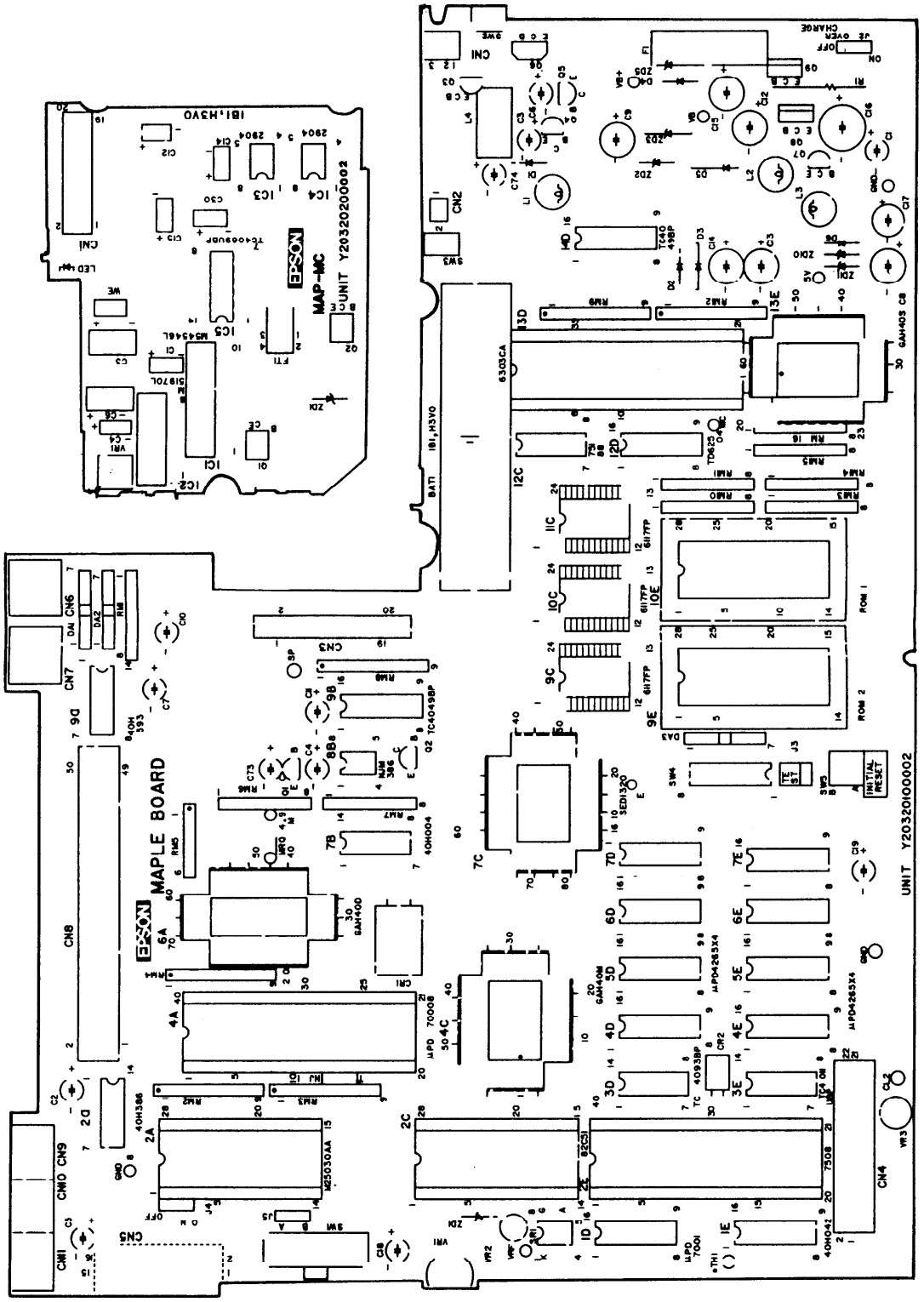
MAP-RF BOARD
Y 204204001 (A)


MAP-RF BOARD
EPSON MAP-RF BOARD
UNIT Y204204 00000
181, H3V0
CN1
CN2
Z-80
27C32
74HC04
40H020
40H374
40H244
40H074
40H000
40H002
40H027
40H155
40H347
40H245
40H244
4069 UBP
MPD4265X8
E01030EA

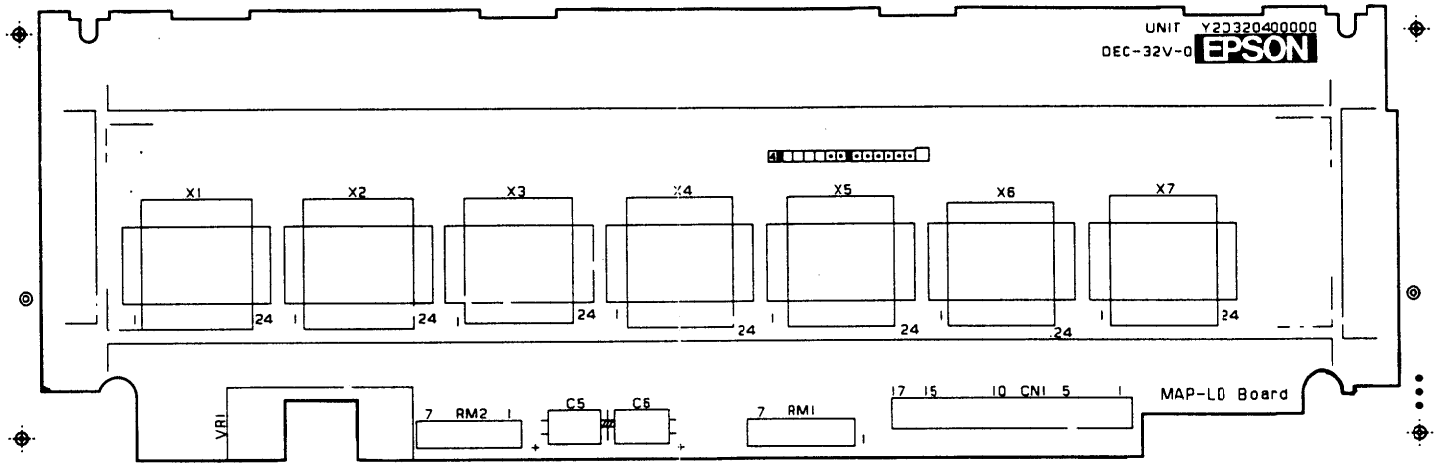

MAPLE BOARD
Y203201000(a)

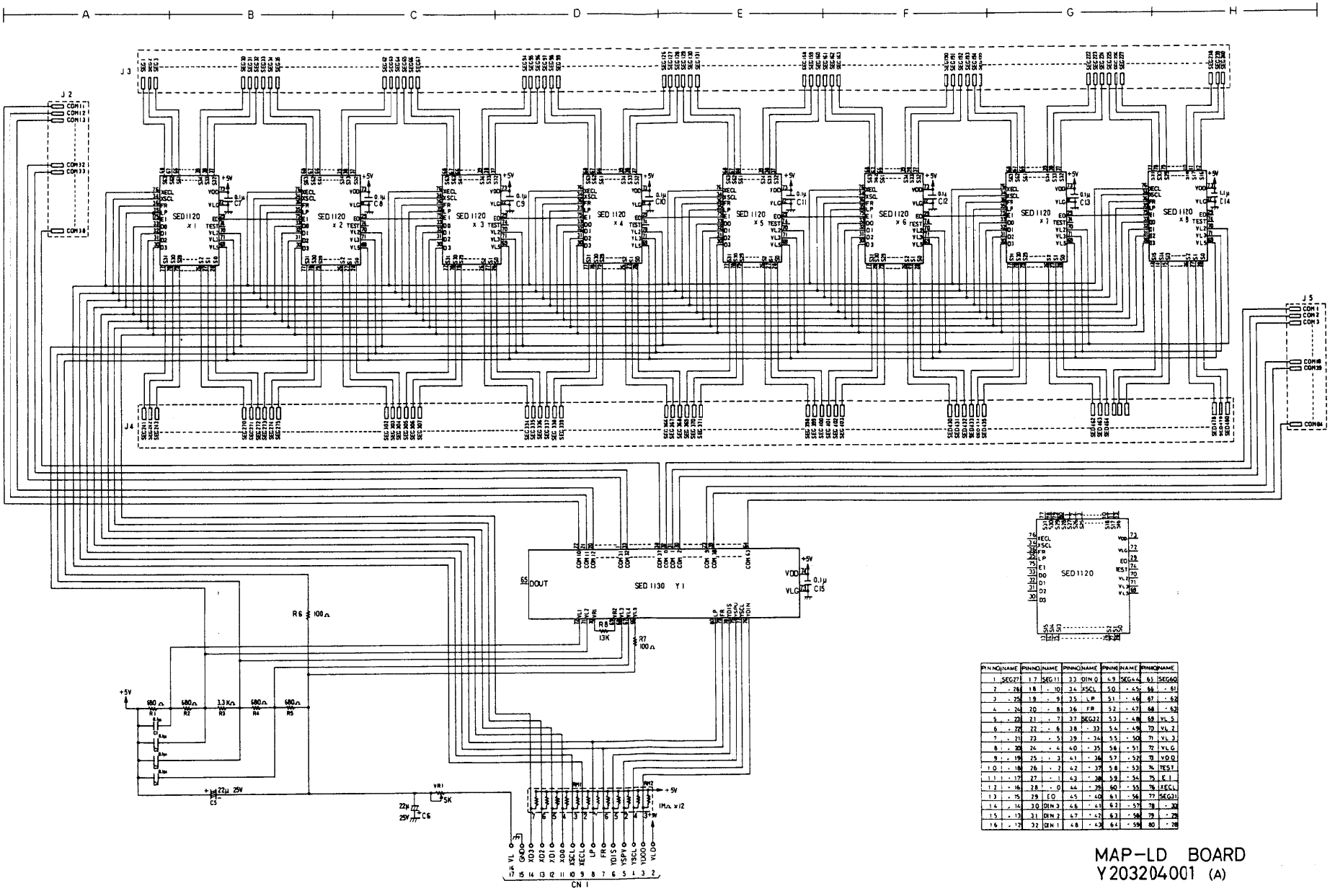

A
B
C
D
E
F
G
H
1
2
3
4
5
6
7
8
CN 1
HSW
WE
VBSW
MTA
MTB
GP
MTC
ERAH
HMT
CNTR
VLRO
VLSW
RDMC
GND
WD
RDSP
HSW 1 BROWN
HSW 2 BROWN
WE 1
FG 1 ORANGE
FG 2 ORANGE
LED
E + ORANGE
E − BLUE
HPM 1 RED
HPM 2 BLACK
M + RED
M − BLACK
RPH + PINK
RPH − WHITE
IC 1
M54546L
IC 2
M51970L
IC5 2/6 4069
IC5 1/6 4069
Q1 2SB 766R
Q2 2SD1280R
Q3 2SD 1048×3
Q4 2SD601R
Q5 2SD601R
Q6 2SD601R
FT1 NJL 5141E
D1 MA153
D2 MA153
D5 MA151A
D6 MA151A
D7 MA153
ZD1 HZ4LLB
R37 100K
R36 100K
R2 6.8K
R3 68
R4 10K
R5 150K
R6 1K
R7 150K
R8 100
R9 1.5K
R10 1.0K
R11 15K
R12 220
R13 120K
R31 15K
R33 33K
R34 6.8K
R35 4.7K
R38 22K
R39 1K
R40 100K
R41 4.7K
R42 10K
R43 2.7K
R44 470K
C1 2.2μ 16V
C2 10μ 16V
C3 10μ 16V
C4 47μ 16V
C5 .01μ
C6 10μ 16V
C7 .01μ
C8 .1μ
C9 .1μ
C10 .1μ
C11 .015μ
C12 1μ 16V
C13 .1μ
C14 4.7μ 10V
C15 6.8μ 10V
C16 .047
C17 220P
C18 .047
C20 220P
C21 .1μ
C22 .01μ
C23 .047μ
C24 390P
C25 1μ
C26 .01μ
C27 .033μ
C28 47P
C29 1000P
C30 2.2μ 16V
C31 .1μ
R14 5.1K
R15 33K
R16 3.3K
R17 4.7K
R18 100K
R20 270K
R21 10K
R22 220K
R24 4.7K
R25 10K
R26 10K
R27 10K
R28 47K
R29 10K
R30 5.6MΩ
VR1 100K
ZD1 HZ4LLB
MAP-MC BOARD
Y203202001 (A)


EPSON MAPLE-BOARD-X SILK(SOLD)
SPEAKER
HSW
HPM
RPH

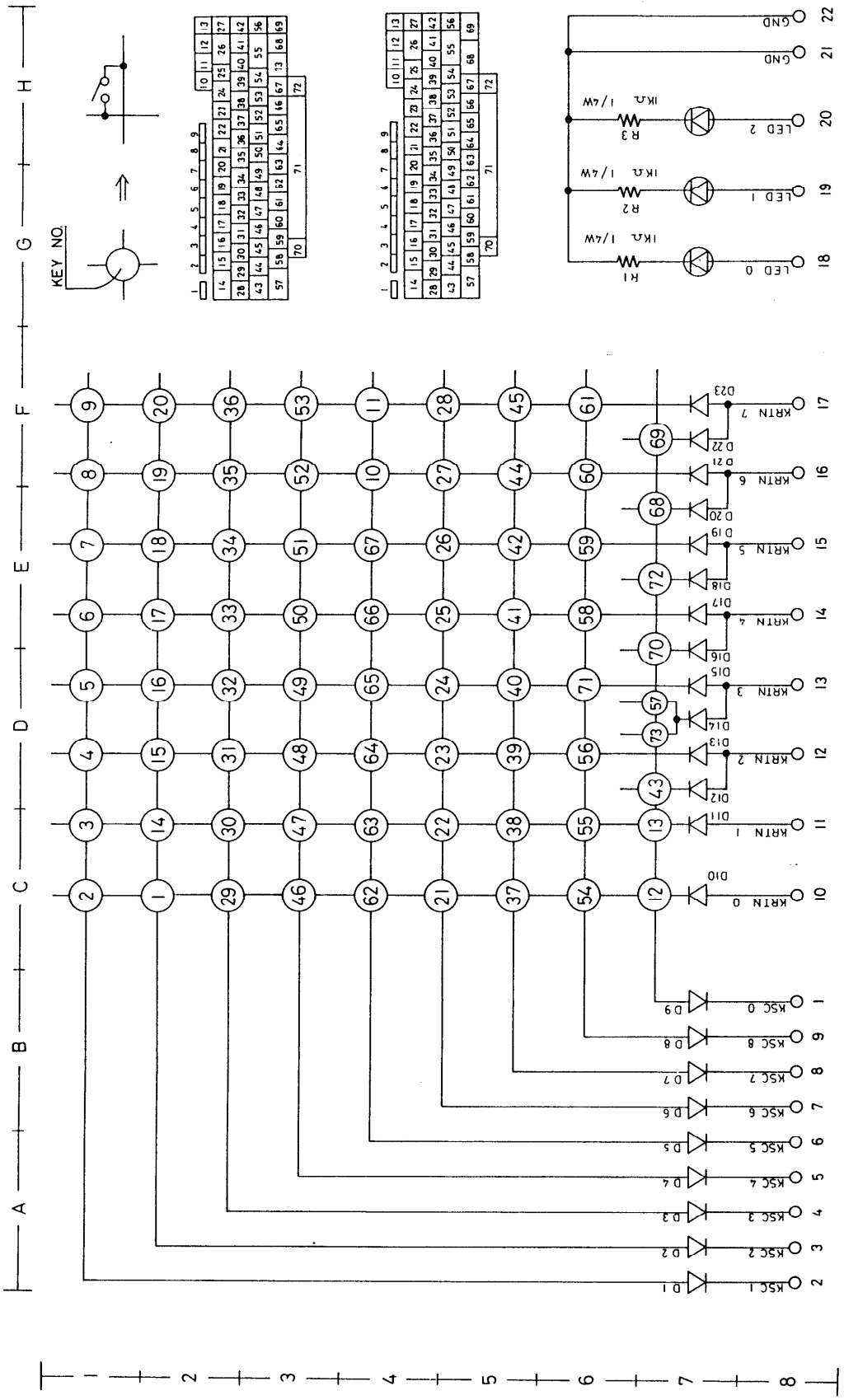


EPSON MAPLE-BOARD-X SILK(COMP)


UNIT Y20320400000
DEC-32V-0
EPSON
X1
X2
X3
X4
X5
X6
X7
24
VR1
7 RM2 1
C5
C6
7 RM1 1
17 15 10 CN1 5 1
MAP-L0 Board



PIN NO	NAME	PIN NO	NAME	PIN NO	NAME	PIN NO	NAME	PIN NO	NAME
1	SEG27	17	SEG11	33	DIN 0	49	SEG44	65	SEG60
2	26	18	10	34	XSCL	50	45	66	61
3	25	19	9	35	LP	51	46	67	62
4	24	20	8	36	FR	52	47	68	63
5	23	21	7	37	SEG32	53	48	69	VL 5
6	22	22	6	38	33	54	49	70	VL 2
7	21	23	5	39	34	55	50	71	VL 3
8	20	24	4	40	35	56	51	72	VL 6
9	19	25	3	41	36	57	52	73	VDD
10	18	26	2	42	37	58	53	74	TEST
11	17	27	1	43	38	59	54	75	E 1
12	16	28	0	44	39	60	55	76	XECL
13	15	29	EO	45	40	61	56	77	SEG31
14	14	30	DIN 3	46	41	62	57	78	30
15	13	31	DIN 2	47	42	63	58	79	29
16	12	32	DIN 1	48	43	64	59	80	28


KEY NO.
LED 0
LED 1
LED 2
GND
GND
1KΩ 1/4W
R1
R2
R3
KRTN 0
KRTN 1
KRTN 2
KRTN 3
KRTN 4
KRTN 5
KRTN 6
KRTN 7
KSC 0
KSC 1
KSC 2
KSC 3
KSC 4
KSC 5
KSC 6
KSC 7
KSC 8
A
B
C
D
E
F
G
H