

# IMS INTERNATIONAL

## MODEL 740

### I/O PROCESSOR BOARD

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#### GENERAL DESCRIPTION

The Model 740 I/O PROCESSOR is a single board computer with a Z-80A processor, 64K bytes of Dynamic RAM with Parity, 2K bytes of IPL PROM, Two programmable Synchronous/Asynchronous communication channels with MODEM control, Ten programmable parallel I/O lines compatible with Bell 801 Automatic Calling Unit, Four interval timers ( two used for baud rates), Z-80 internally-prioritized vectored interrupt structure, and Parallel interface to the S-100 BUS Host processor.

The Z-80A SIO interfaces the Z-80A CPU to Two asynchronous or synchronous Serial Data Channels. The SIO converts input serial data from the RS-232C port to parallel data to be acted upon by the system. Output data is converted from parallel to serial data to be placed on the RS-232C port.

The 8255A Programmable Peripheral Interface circuit interfaces the S-100 BUS to the slave Z-80A CPU bus.

The MODEL 740 I/O Processor consists of a single printed circuit board that occupies one slot in the Series 5000 or 8000 Computer Systems. Each serial RS-232C port is brought out to a 3M 26-pin header. The RS-232C ports are designed as Data Terminal Equipment (DTE) to connect directly to a MODEM. To connect a terminal directly to the RS-232C port (DTE to DTE) the RS-232C cable wires must be interchanged for proper operation of terminal.

#### S-100 BUS TO I/O PROCESSOR INTERFACE

##### 8255A Mode 2 S-100 BUS to Slave Z-80A CPU Interface

Due to the drastic reduction of hardware costs, system designs which utilize multiple CPU modules are becoming more common. A Model 451 Z-80A CPU is configured as the master S-100 CPU and used to control multiple Z-80A slave modules which act as intelligent I/O controllers. When multiple CPUs are utilized, a method of processor intercommunication must be supported. The IMS 740 Z-80A module is implemented as a master/slave interface through the use of the 8255A Mode 2 bidirectional bus.

The S-100 BUS interface is supported by an 8255A which is configured in Mode 2. The 8255A is selected through the use of a standard S-100 I/O Address decode select scheme and the S-100 vector interrupt structure. The Z-80A slave logic is implemented to allow the slave Z-80A CPU to generate the ACK- and STB- signals required to READ from and WRITE to the 8255A bidirectional bus.

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## S-100 Configuring and Programming

### I/O DEVICE ADDRESS SELECTION (JE)

JE			
A7	1	—	12
A6	2	. .	11
A5	3	—	10
A4	4	—	9
A3	5	—	8
A2	6	—	7

SHUNT OFF = 1

SHUNT ON = 0

Example shown places 740 board at I/O address 40H - 43H

### 8255A BASIC OPERATION

I/O DEVICE	ADDRESS	OPERATION
IN	X0	PORT A -> S-100 BUS
IN	X2	PORT C -> S-100 BUS
OUT	X0	S-100 BUS -> PORT A
OUT	X2	S-100 BUS -> PORT C
OUT	X3	S-100 BUS -> CONTROL
OUT	X3	C0H -> CONTROL (Mode 2)
OUT	X3	00H 0 -> PC0 Control/Data Flag
OUT	X3	01H 1 -> PC0
OUT	X3	02H 0 -> PC1 Reset Slave
OUT	X3	03H 1 -> PC1
OUT	X3	08H 0 -> PC4 INTE2 (INTE for IBF)
OUT	X3	09H 1 -> PC4
OUT	X3	0AH 0 -> PC5 IBF
OUT	X3	0BH 1 -> PC5
OUT	X3	0CH 0 -> PC6 INTE1 (INTE for OBF)
OUT	X3	0DH 1 -> PC6
OUT	X3	0EH 0 -> PC7 OBF
OUT	X3	0FH 1 -> PC7

## 8255A Bidirectional Bus I/O Control Signal Definition

**INTR+** (Interrupt Request) Used to interrupt the S-100 BUS Master for both input or output operations.

**OBF-** (Output buffer Full) Used to indicate that the S-100 BUS has written data out to PORT A.

**ACK-** (Acknowledge) Enables the tri-state output buffer of PORT A.

**INTE1** (The INTE Flip-Flop Associated with OBF) Controlled by bit set/reset of PC6.

**STB-** (Strobe Input) Used to load data into the input latch of PORT A.

**IBF+** (Input Buffer Full) Indicates that data has been loaded into the input latch of PORT A.

**INTE2** (The INTE Flip-Flop Associated with IBF) Controlled by bit set/reset of PC4.

## 8255A Definition Summary

PA0-PA7	I/O DATA
PB0-PB7	UNUSED
PC0	CONTROL/DATA FLAG
PC1	RESET SLAVE
PC2	UNUSED
PC3	INTR+
PC4	STB-/INTE2
PC5	IBF+
PC6	ACK-/INTE1
PC7	OBF-

## INTERRUPT SELECTION OPTION (JF)

		JF	
VI0	1	.	16
VI1	2	.	15
VI2	3	.	14
VI3	4	.	13
VI4	5	.	12
VI5	6	.	11
VI6	7	.	10
VI7	8	.	9

The installing of a SHUNT will attach the selected Vix Interrupt Level to Parallel Port A Interrupt (PC3 INTR).

**Note:** For more detail regarding the programming of the 8255A see the Intel Peripheral Design Handbook.

## **I/O Processor Configuring and Programming**

### **Z-80A SIO PORT A Receive and Transmit Baud Clock Selection (JA)**

#### **JA**

1. .8 RxCA- from Z-80A CTC T0 (this connection is etched)
2. .7 RxCA- from RS-232 Interface PIN 17 Signal DD
3. 6 TxCA- from Z-80A CTC T0 (requires a shunt)
4. .5 TxCA- from RS-232 Interface PIN 15 Signal DB

### **Z-80A SIO PORT B Receive and Transmit Baud Clock Selections (JB)**

#### **JB**

1. .6 RxTxCB- from Z-80A CTC T1 (this connection is etched)
2. .5 RxTxCB- from RS-232 Interface PIN 17 Signal DD
3. .4 RxTxCB- from RS-232 Interface PIN 15 Signal DB

### **S-100 RESET DISABLE SHUNT (JD)**

#### **JD**

- 1.
- 2.

SHUNT OFF = Normal mode

SHUNT ON = Local 740 Test mode

**MODEL 740**

**SERIAL PORT TO RS-232C CONNECTOR CABLE**

<b>Signal Name</b>	<b>RS-232C Circuit</b>	<b>Pin</b>	<b>Controller Pin</b>
Protective Ground	AA	1	1
Signal Ground	AB	7	13
Transmit Data (Data to MODEM)	BA	2	3
Receive Data (Data from MODEM)	BB	3	5
Request To Send	CA	4	7
Clear To Send	CB	5	9
Data Set Ready	CC	6	11
Data Terminal Ready	CD	20	14
Ring Indicator	CE	22	18
Data Carrier Detect	CF	8	15
Transmit Clock (Clock From MODEM)	DB	15	4
Receive Clock (Clock From MODEM)	DD	17	8

## Z-80A PIO Definition Summary

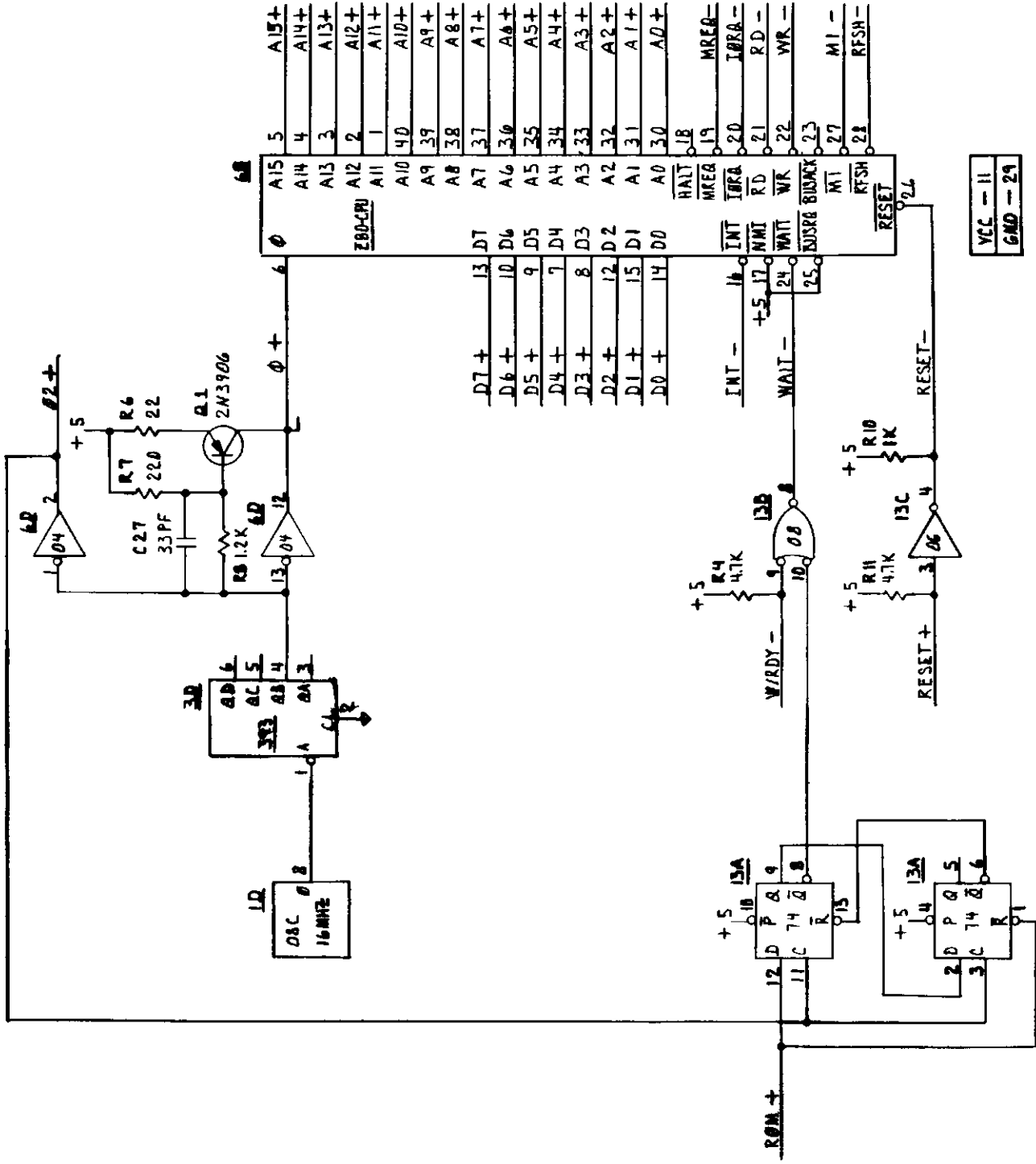
### PORT A INPUT BITS

A0		
A2	DSS-	BELL 801 DATA SET STATUS
A3	DLO-	BELL 801 DATA LINE OCCUPIED
A4	C/D+	8255A PC0 CONTROL/DATA FLAG
A5	IBF+	8255A PC5 INPUT BUFFER FULL
A6	OBF-	8255A PC7 OUTPUT BUFFER FULL
A7	PER+	RAM PARITY ERROR

### PORT B OUTPUT BITS

B0	NB1+	BELL 801 NUMBER BIT 1
B1	NB2+	BELL 801 NUMBER BIT 2
B2	NB4+	BELL 801 NUMBER BIT 4
B3	NB8+	BELL 801 NUMBER BIT 8
B4	DPR-	BELL 801 DIGIT PRESENT
B5	CRQ-	BELL 801 CALL REQUEST
B6	ROMEN+	ROM ENABLE
B7	PERR+	RAM PARITY RESET

**NOTE:** For more detail regarding the programming of the Z-80A Microcomputer Components see Zilog Data Book or Technical Manuals.



5	A15+
4	A14+
3	A13+
2	A12+
1	A11+
40	A10+
39	A9+
38	A8+
37	A7+
36	A6+
35	A5+
34	A4+
33	A3+
32	A2+
31	A1+
30	A0+
18	HALT
19	MREQ-
20	IOEA-
21	RD-
22	WR-
23	BUSRQ BUSACK
27	M1-
28	RFSH-
13	D7+
10	D6+
9	D5+
7	D4+
8	D3+
12	D2+
15	D1+
14	D0+
16	INT-
17	NMI-
24	WAIT-
25	BUSRQ BUSACK
26	RESET-

VCC - 11
GND - 29

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I/O PROCESSOR BOARD

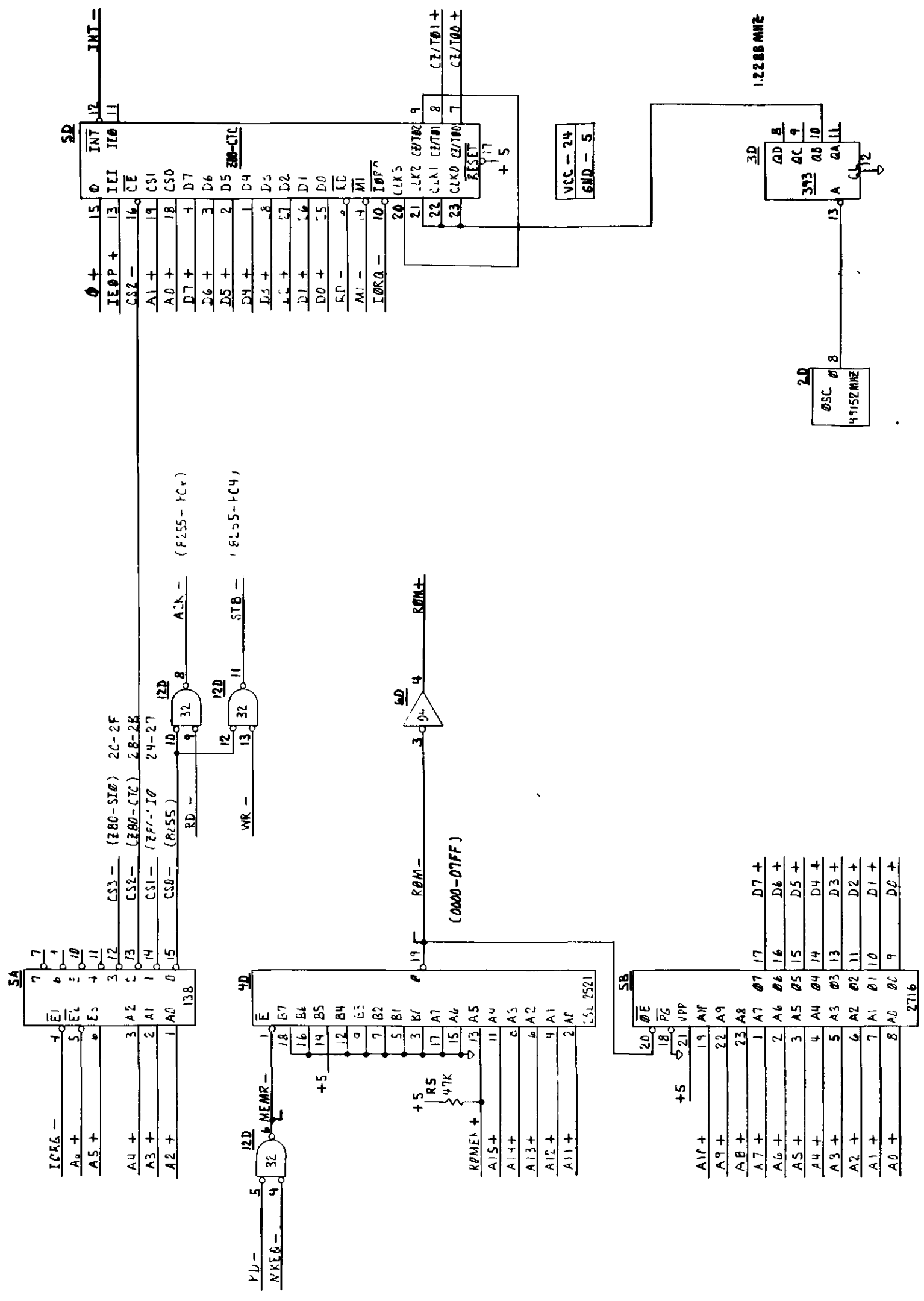
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**MODEL 740 P1 SIGNAL LIST**

PIN	SIGNAL	PIN	SIGNAL
1	+8V	51	+8V
2	+16V	52	-16V
3		53	
4	VI0-	54	
5	VI1-	55	
6	VI2-	56	
7	VI3-	57	
8	VI4-	58	
9	VI5-	59	
10	VI6-	60	
11	VI7-	61	
12		62	
13		63	
14		64	
15		65	
16		66	
17		67	
18		68	
19		69	
20	GND	70	GND
21		71	
22		72	
23		73	
24		74	
25		75	
26		76	
27		77	pWR-
28		78	pDBIN+
29	A5+	79	A0+
30	A4+	80	A1+
31	A3+	81	A2+
32		82	A6+
33		83	A7+
34		84	
35	DO1+	85	
36	DO0+	86	
37		87	
38	DO4+	88	DO2+
39	DO5+	89	DO3+
40	DO6+	90	DO7+
41	DI2+	91	DI4+
42	DI3+	92	DI5+
43	DI7+	93	DI6+
44		94	DI1+
45	sOUT+	95	DI0+
46	sINP+	96	
47		97	
48		98	
49		99	POC-
50	GND	100	GND

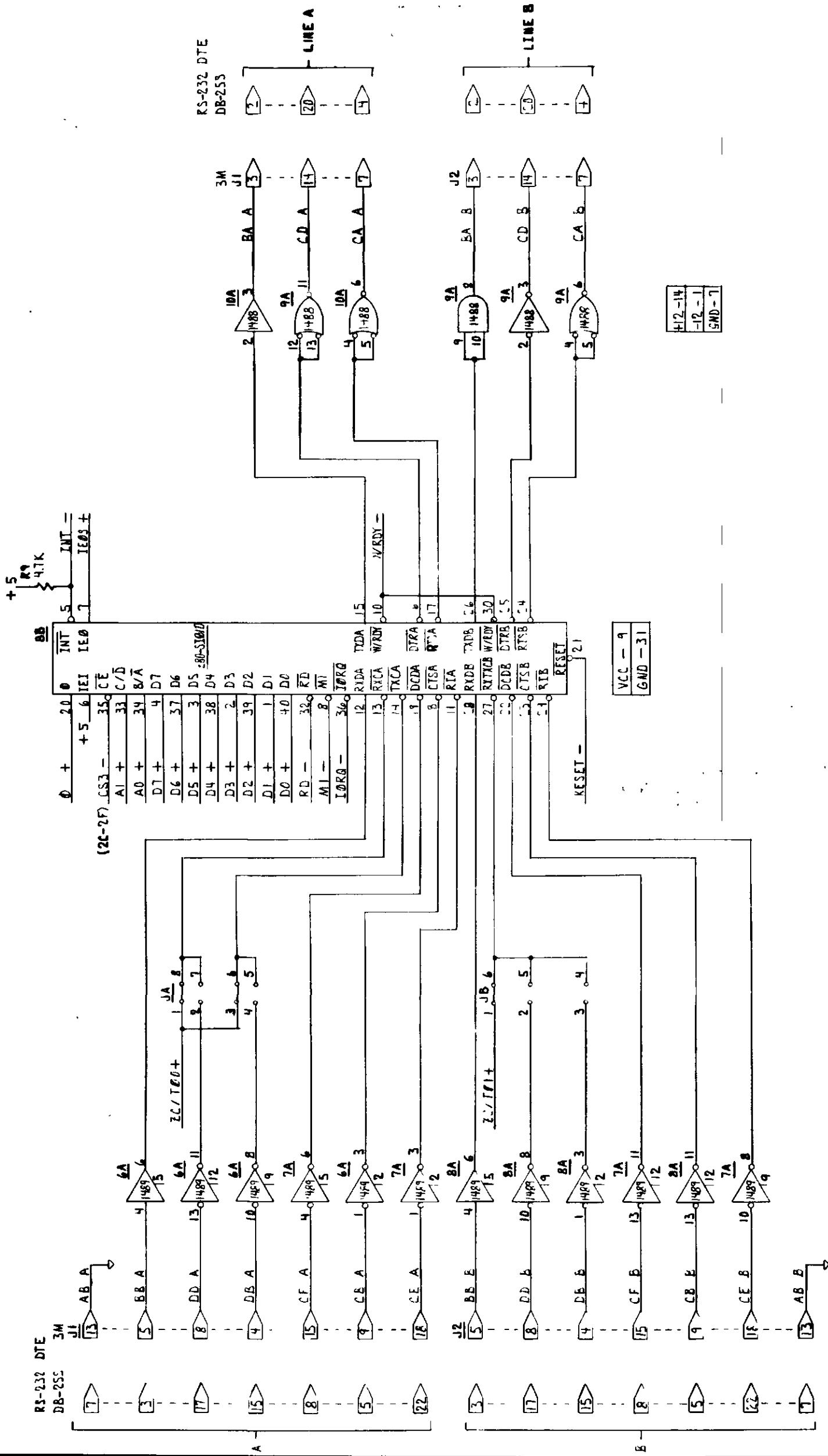




**MODEL 740**

**BELL 801 ACU PARALLEL PORT TO RS-232C CONNECTOR CABLE**

<b>Signal Name</b>	<b>ACU Circuit</b>	<b>Connector Pin</b>	<b>Controller Pin</b>
Frame Ground	FGD	1	1
Signal Ground	SGD	7	13
Digit Present	DPR	2	3
Abandon Call-Retry	ACR	3	5
Call Request	CRQ	4	7
Present Next Digit	PND	5	9
Power Indication	PWI	6	11
Data Set Status	DSS	13	25
Number Bit 1	NB1	14	2
Number Bit 2	NB2	15	4
Number Bit 4	NB4	16	6
Number Bit 8	NB8	17	8
Data Line Occupied	DLO	22	18



+12-14
-12-1
GND-7

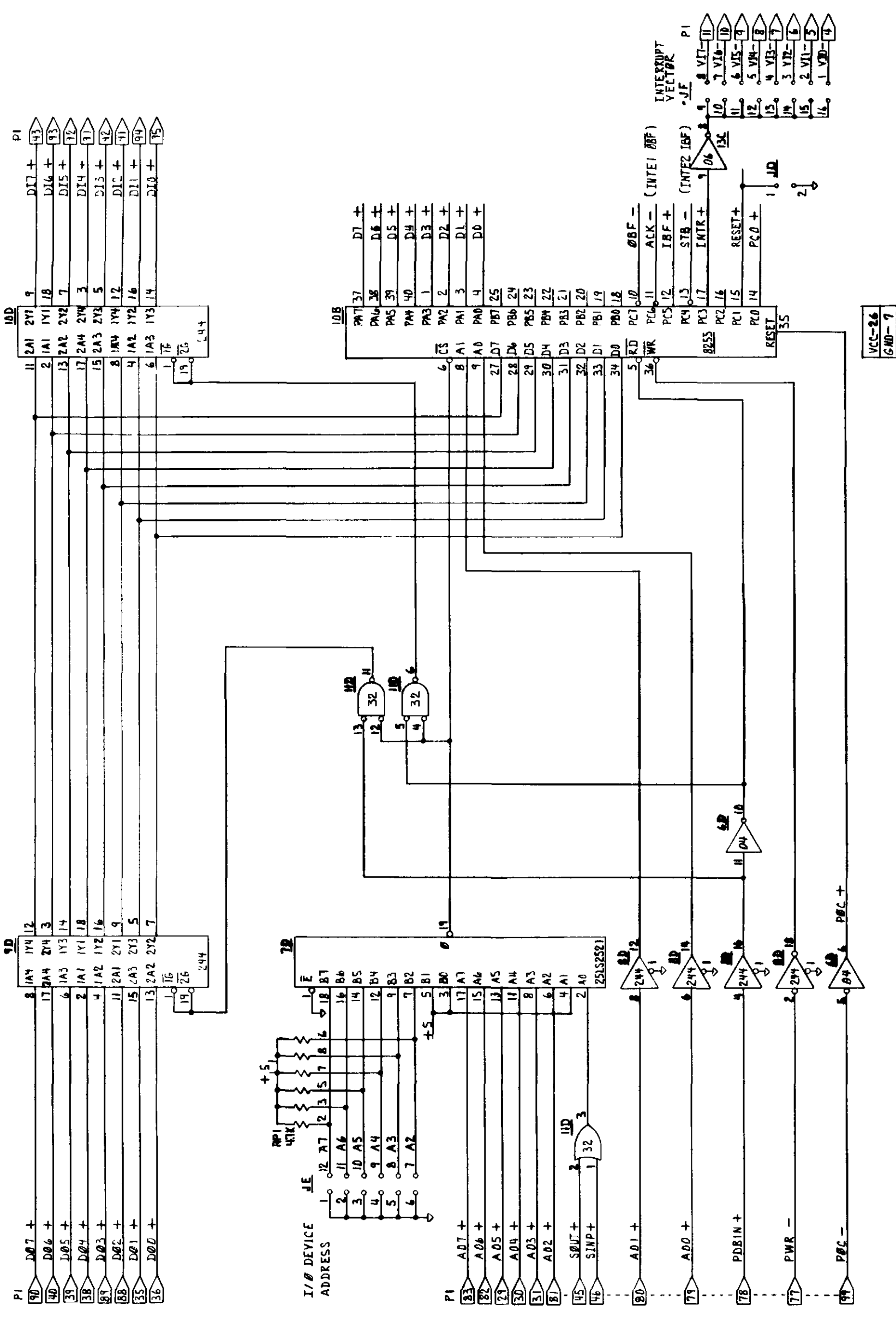
VCC - 9
GND - 31

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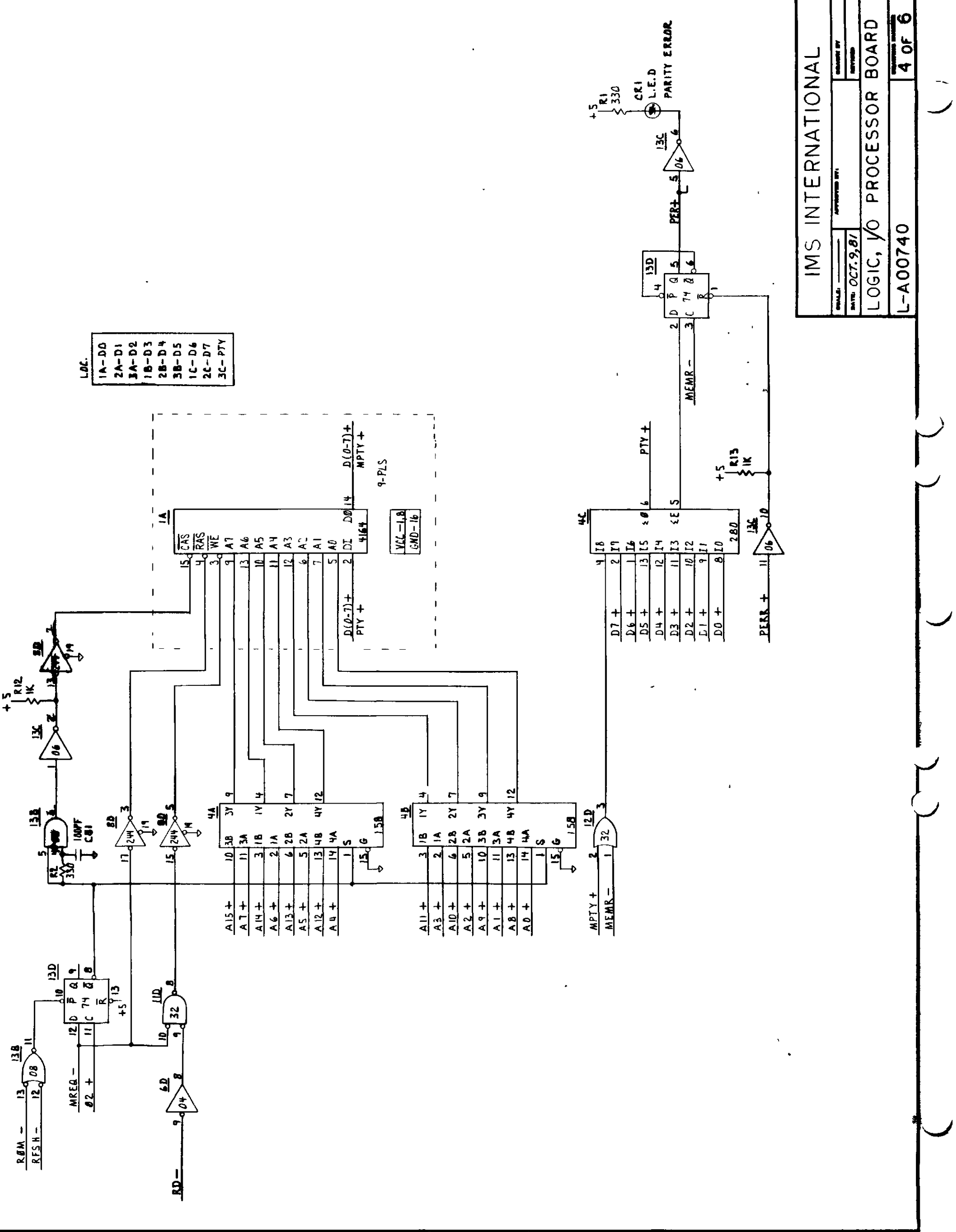
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- LOC.
- 1A-DD
  - 2A-D1
  - 3A-D2
  - 1B-D3
  - 2B-D4
  - 3B-D5
  - 1C-D6
  - 2C-D7
  - 3C-PTY

VCC-1,8  
GND-16

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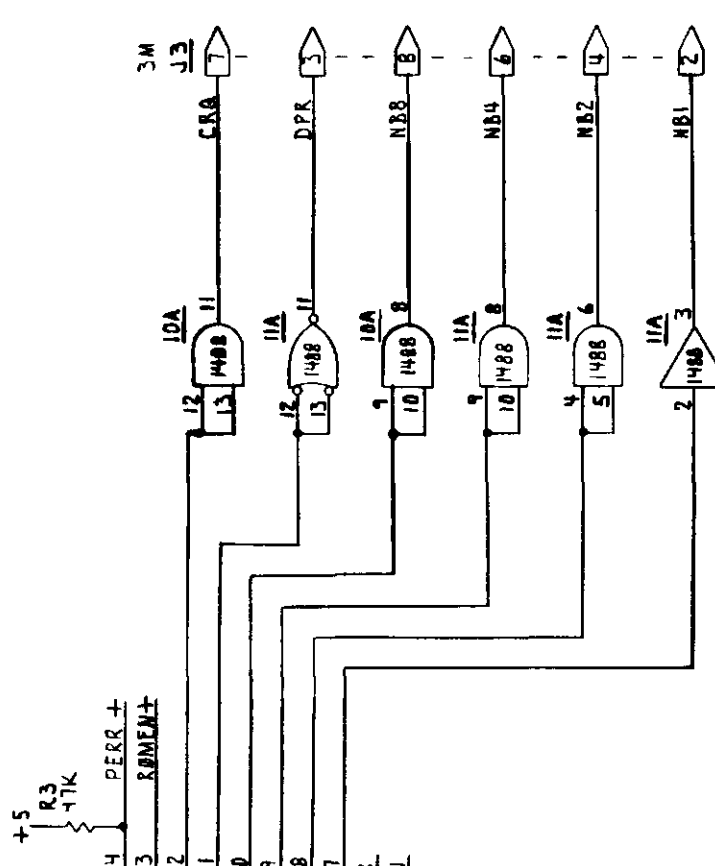
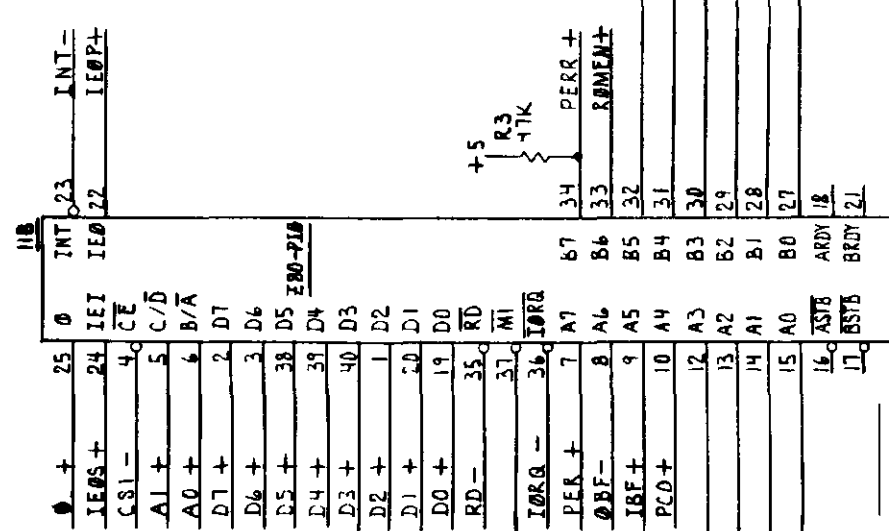
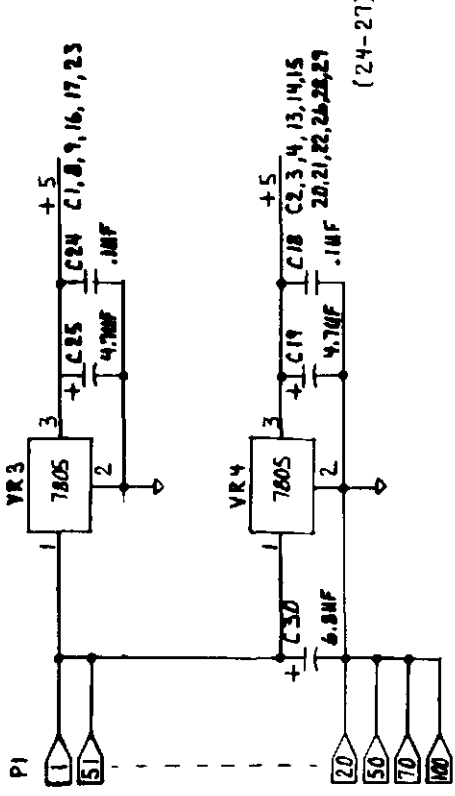
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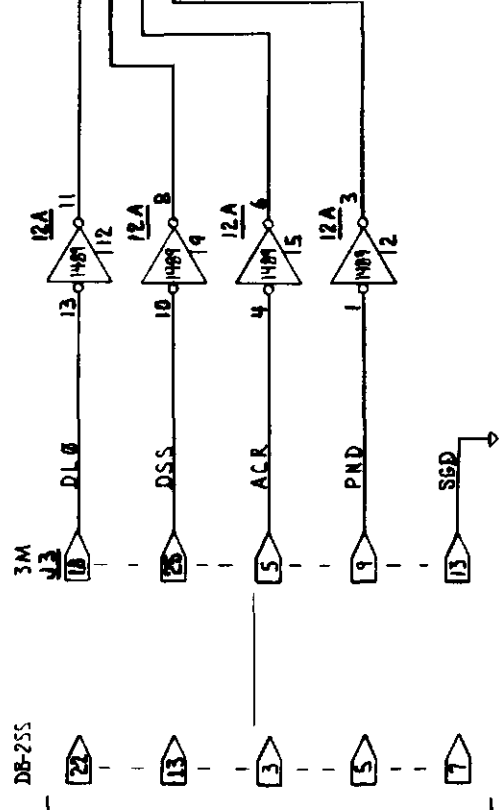
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+12-14
-12-1
GND-7

VCC-26
GND-11



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