Rev. 1

National Semiconductor

400093 Rev. 1

Series 32000 Microprocessors Databook

- *Series 32000 Family*
- *NSC800 Family*

Series 32000 Microprocessors Databook National Semiconductor

MICROPROCESSOR
DATABOOK

- Series 32000
- NSC800

1988 Edition

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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TWX (910) 339-9240

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Product Status Definitions

Definition of Terms

Data Sheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This data sheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This data sheet contains preliminary data, and supplementary data will be published at a later date. National Semiconductor Corporation reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
No Identification Noted	Full Production	This data sheet contains final specifications. National Semiconductor Corporation reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

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Alpha-Numeric Index (Continued)

Section 1

Series 32000 Overview

Section 1 Contents

Introduction

Series 32000 offers the most complete solution to your 32-bit microprocessor needs via CPUs, slave processors, system peripherals, evaluation/development tools and software.

We at National Semiconductor firmly believe that it takes a total family of microprocessors to effectively meet the needs of a system designer.

This Series 32000 Databook presents technical descriptions of Series 32000 8-, 16- and 32-bit microprocessors, slave processors, peripherals, software and development tools. It is designed to be updated frequently so that our customers can have the latest technical information on the Series 32000.

Series 32000 leads the way in state-of-the-art microprocessor designs because of its advanced architecture, which includes:

- 32-Bit Architecture
- Demand Paged Virtual Memory
- Fast Floating-Point Capability
- High-Level Language Support
- Symmetrical Architecture

When we at National Semiconductor began the design of the Series 32000 microprocessor family, we decided to take a radical departure from popular trends in architectural design that dated back more than a decade. We chose to take the time to design it properly.

Working from the top down, we analyzed the issues and anticipated the computing needs of the 80's and 90's. The result is an advanced and efficient family of microprocessor hardware and software products.

Clearly, software productivity has become a major issue in computer-related product development. In microprocessor-based systems this issue centers around the capability of the microprocessor to maximize the utility of software relative to shorter development cycles, improved software reliability and extended software life cycles.

In short, the degree to which the microprocessor can maximize software utility directly affects the cost of a product, its reliability, and time to market. It also affects future software modification for product enhancement or rapid advances in hardware technology.

Our approach has been to define an architecture addressing these software issues most effectively. Series 32000 combines 32-bit performance with efficient management of large address space. It facilitates high-level language program development and efficient instruction execution. Floating-point is integrated into the architecture.

This combination gives the user large system computing power at two orders of magnitude less cost.

But we didn't stop there. Advanced architecture isn't enough. Our top-down approach includes the hardware, software, and development support products necessary for your design. The evaluation board, in-system emulator, software development tools, including a VAX-11 cross-software package, and third party software are also available now for your evaluation and development.

The Series 32000 is a solid foundation from which National Semiconductor can build solutions for your future designs while satisfying your needs today.

For further information please contact your local sales office.

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Key Features of Series 32000®

Some of the features that set the Series 32000 family apart as the best choice for 32-bit designs are as follows:

FAMILY OF MICROPROCESSOR CHIP SETS

Series 32000 is more than just a single chip set, it is a family of chip sets. By mixing and matching Series 32000 CPUs with compatible slave processors and support chips, a system designer has an unprecedented degree of flexibility in matching price/performance to the end product.

CLEANEST 32-BIT SUPER MINI COMPUTER ARCHITECTURE

Series 32000 was designed around a 32-bit architecture from the beginning. It has a fully symmetrical instruction set so that all addressing modes and all data types can be operated on by all instructions. This makes it easy to learn the architecture, easy to program in assembly language, and easy to write code-efficient, high-level language compilers.

DEMAND-PAGED VIRTUAL MEMORY MANAGEMENT

Series 32000 provides hardware support for Demand-Paged Virtual Memory Management. This allows use of low-cost disk storage to increase the apparent size of main memory, and is an efficient method of managing very large address spaces. It is also the same popular memory management method used by DEC and IBM in their minicomputers and mainframes.

APPLICATION-SPECIFIC SLAVE PROCESSORS

Series 32000 architecture allows users to design their own application-specific slave processors to interface with the existing chip set. These processors can be used to increase the overall system performance by accelerating customized CPU instructions that would otherwise be implemented in software. At the same time, software compatibility is maintained, i.e., it is always possible to substitute lower-cost software modules in place of the slave processor.

FLOATING-POINT SUPPORT

The Series 32000 offers a complete set of floating-point solutions. This includes the NS32081 Floating-Point Unit, the NS32381 Floating-Point Unit and the NS32580 Floating-Point Controller. The NS32081 provides high-speed arithmetic computation with high precision and accuracy at low cost. The NS32381 provides low power consumption and even greater performance than the NS32081 while maintaining high-precision and accuracy.

The NS32580 is a floating-point controller that provides a direct interface between the Weitek WTL 3164 Floating-Point Data Path and the NS32532 CPU. This two chip combination, NS32580/WTL3164, provides optimum performance for speed critical floating-point applications.

OPERATING SYSTEM SUPPORT

Series 32000 features such as hardware support for Demand-Paged Virtual memory management, user software protection and modular programming make it much easier to implement powerful, reliable and efficient operating systems. These features along with its symmetrical architecture and powerful instruction set make the Series 32000 the most efficient and highest performance UNIX engine.

HIGH-LEVEL LANGUAGE SUPPORT

Series 32000 has special features that support high-level languages, thus improving software productivity and reducing development costs. For example, there are special instructions that help the compiler deal with structured data types such as Arrays, Strings, Records, and Stacks. Also, modular programming is supported by special hardware registers, software instructions, an external addressing mode, and architecturally supported link tables.

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Series 32000® Component Descriptions

Device	Description	Bus Width			Process	Package Type
		Internal	External			
			Address	Data		
CENTRAL PROCESSING UNITS (CPU's)						
NS32532	High-Performance 32-Bit Microprocessor	32	32	32	M²CMOS	175-pin PGA
NS32332	32-Bit Advanced Microprocessor	32	32	32	XMOS (NMOS)	84-pin PGA
NS32C032	High-Performance Microprocessor	32	24	32	CMOS	68-pin LCC Leadless Chip Carrier
NS32032	High-Performance Microprocessor	32	24	32	XMOS (NMOS)	68-pin LCC Leadless Chip Carrier
NS32C016	High-Performance Microprocessor	32	24	16	CMOS	48-pin DIP Dual-In-Line Package
NS32016	High-Performance Microprocessor	32	24	16	XMOS (NMOS)	48-pin DIP Dual-In-Line Package
NS32008	High Performance 8-Bit Microprocessor	32	24	8	XMOS (NMOS)	48-pin DIP Dual-In-Line Package
NS32CG16	High Performance Printer/Display Processor	32	24	16	CMOS	68-pin PCC
SLAVE PROCESSORS						
NS32382	Memory Management Unit	32	32	32	XMOS (NMOS)	PGA
NS32082	Memory Management Unit	32	24	16	XMOS (NMOS)	48-pin DIP Package
NS32081	Floating-Point Unit	64	—	16	XMOS	24-pin DIP Dual-In-Line Package
NS32381	Floating-Point Unit	64	—	16	CMOS	68-pin PGA
NS32580	Floating-Point Controller	64	—	16 or 32	CMOS	172-pin PGA
PERIPHERALS						
NS32C201	CMOS Timing Control Unit	—	—	—	CMOS	24-pin DIP Dual-In-Line Package
NS32202	Interrupt Control Unit	32	—	16	XMOS (NMOS)	40-pin DIP Dual-In-Line Package
NS32203	Direct Memory Access Controller	—	—	16	XMOS (NMOS)	48-pin DIP Dual-In-Line Package

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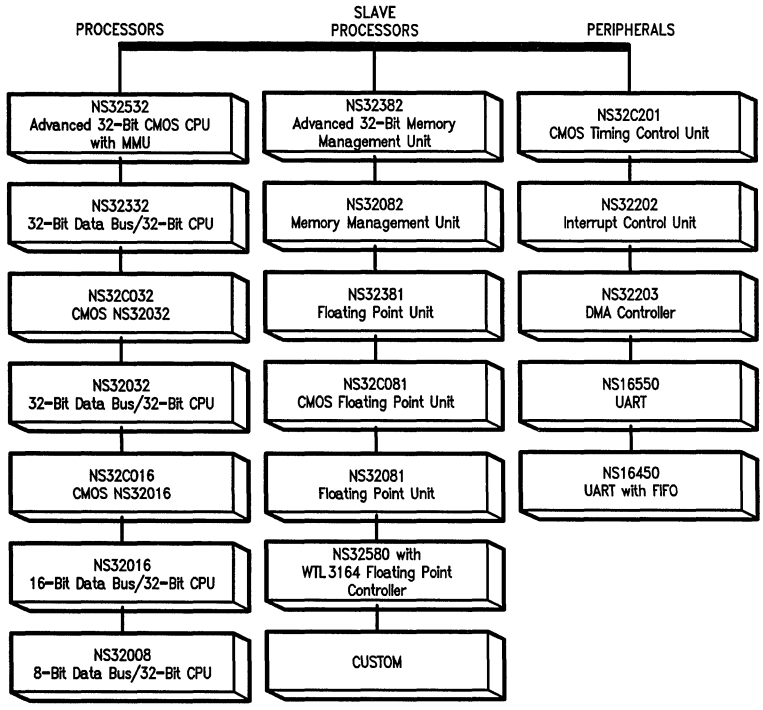
Hardware Chart



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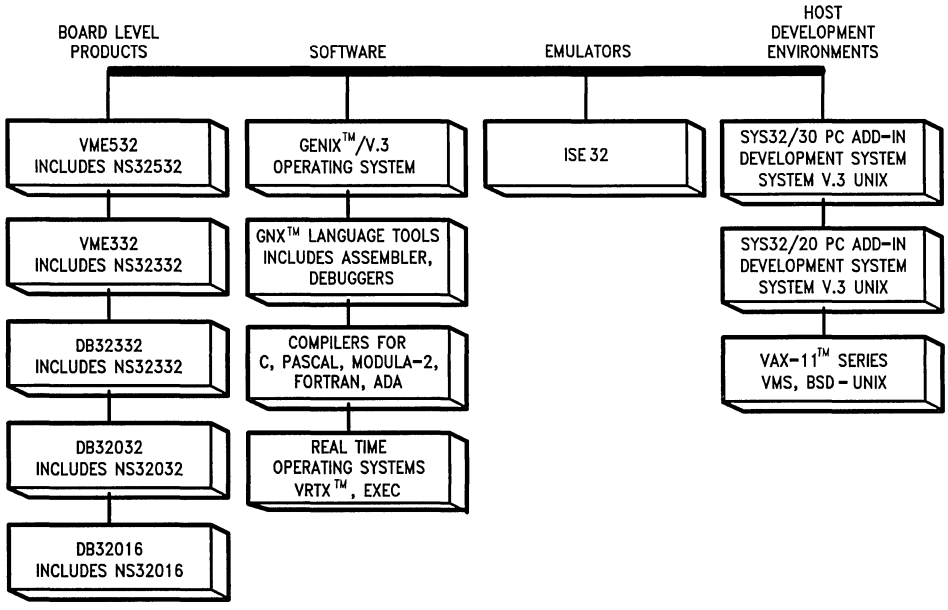
Systems and Software Chart



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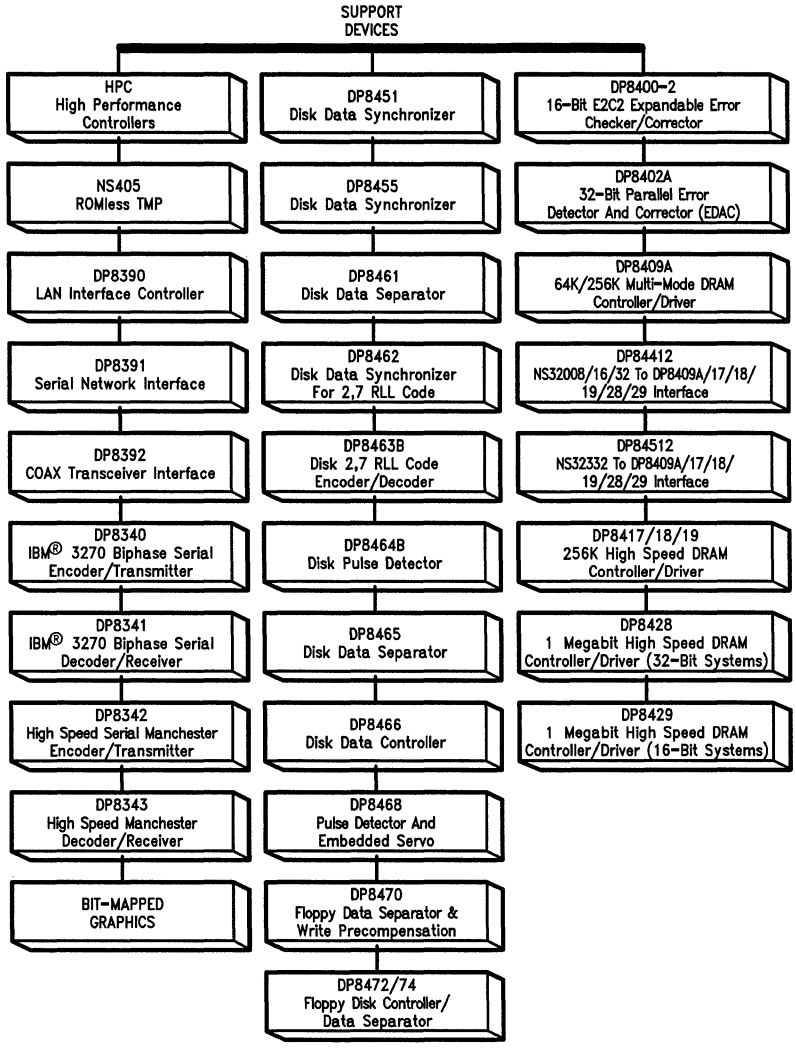
Support Devices Chart



TL/XX/0111–1

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Military/Aerospace Programs from National Semiconductor

This section is intended to provide a brief overview of military products available from National Semiconductor. For further information, refer to our 1986 Reliability Handbook which is expected to be available by mid 1986.

MIL-M-38510

The MIL-M-38510 Program, which is sometimes called the JAN IC Program, is administered by the Defense Electronics Supply Center (DESC). The purpose of this program is to provide the military community with standardized products that have been manufactured and screened to government-controlled specifications in government certified facilities. All 38510 manufacturers must be formally qualified and their products listed on DESC's Qualified Products List (QPL) before devices can be marked and shipped as JAN products.

There are two processing levels specified within MIL-M-38510: Classes S and B. Class S is typically specified for space flight applications, while Class B is used for aircraft and ground systems. National is a major supplier of both classes of devices. Screening requirements are outlined in Table III.

Tables I and II explain the JAN device marking system.

Copies of MIL-M-38510, the QPL, and other related documents may be obtained from:

Naval Publications and Forms Center
5801 Tabor Avenue
Philadelphia, PA 19120
(212) 697-2179

DESC Specifications

DESC specifications are issued to provide standardized versions of devices which are not yet available as JAN product. MIL-STD-883 Class B screening is coupled with tightly controlled electrical specifications which have been written to allow a manufacturer to use his standard electrical tests. A current listing of National's DESC specification offerings can be obtained from our franchised distributors, sales representatives, or DESC. DESC is located in Dayton, Ohio.

MIL-STD-883

Although originally intended to establish uniform test methods and procedures, MIL-STD-883 has also become the general specification for non-JAN military product. Revision C of this document defines minimum requirements for a device to be marked and advertised as 883-compliant. Included are design and construction criteria, documentation controls, electrical and mechanical screening requirements, and quality control procedures. Details can be found in paragraph 1.2.1 of MIL-STD-883.

National offers both 883 Class B and 883 Class S product. The screening requirements for both classes of product are outlined in Table III.

As with DESC specifications, a manufacturer is allowed to use his standard electrical tests provided that all critical parameters are tested. Also, the electrical test parameters, test conditions, test limits, and test temperatures must be clearly documented. At National Semiconductor, this information is available via our RETS (Reliability Electrical Test Specification) program. The RETS document is a complete description of the electrical tests performed and is controlled by our QA department. Individual copies are available upon request.

Some of National's older products are not completely compliant with MIL-STD-883, but are still required for use in military systems. These devices are screened to the same stringent requirements as 883 product but are marked "-Mil".

Military Screening Program (MSP)

National's Military Screening Program was developed to make screened versions of advanced products such as gate arrays and microprocessors available more quickly than is possible for JAN and 883 devices. Through this program, screened product is made available for prototypes and brassboards prior to or during the JAN or 883 qualification activities. MSP products receive the 100% screening of Table III, but are not subjected to group C and D quality conformance testing. Other criteria such as electrical testing and temperature range will vary depending upon individual device status and capability.

TABLE I. The MIL-M-38510 Part Marking

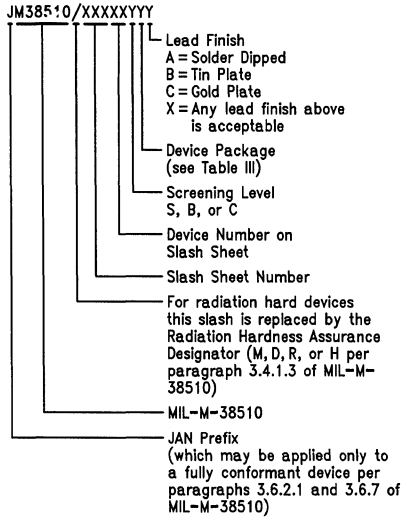


TABLE II. JAN Package Codes

38510 Package Designation	Microcircuit Industry Description
A	14-pin 1/4″ x 1/4″ (metal) flat pack
B	14-pin 3/16″ x 1/4″ flat pack
C	14-pin 1/4″ x 3/4″ dual-in-line
D	14-pin 1/4″ x 3/8″ (ceramic) flat pack
E	16-pin 1/4″ x 7/8″ dual-in-line
F	16-pin 1/4″ x 3/8″ (metal or ceramic) flat pack
G	8-pin TO-99 can or header
H	10-pin 1/4″ x 1/4″ (metal) flat pack
I	10-pin TO-100 can or header
J	24-pin 1/2″ x 1-1/4″ dual-in-line
K	24-pin 3/8″ x 5/8″ flat pack
L	24-pin 1/4″ x 1-1/4″ dual-in-line
M	12-pin TO-101 can or header
N	(Note 1)
P	8-pin 1/4″ x 3/8″ dual-in-line
Q	40-pin 3/16″ x 2-1/16″ dual-in-line
R	20-pin 1/4″ x 1-1/16″ dual-in-line
S	20-pin 1/4″ x 1/2″ flat pack
T	(Note 1)
U	(Note 1)
V	18-pin 3/8″ x 15/16″ dual-in-line
W	22-pin 3/8″ x 1-1/8″ dual-in-line
X	(Note 1)
Y	(Note 1)
Z	(Note 1)
2	20-terminal 0.350″ x 0.350″ chip carrier
3	28-terminal 0.450″ x 0.450″ chip carrier

Note 1: These letters are assigned to packages by individual detail specifications and may be assigned to different packages in different specifications.

TABLE III. 100% Screening Requirements

Screen	Class S		Class B	
	Method	Reqmt	Method	Reqmt
1. Wafer Lot Acceptance	5007	All Lots		
2. Nondestructive Bond Pull	2023	100%		
3. Internal Visual (Note 1)	2010, Condition A	100%	2010, Condition B	100%
4. Stabilization Bake	1008, Condition C, Min, 24 Hrs. Min	100%	1008, Condition C, Min, 24 Hrs. Min	100%
5. Temp. Cycling (Note 2)	1010, Condition C	100%	1010, Condition C	100%
6. Constant Acceleration	2001, Condition E (Min) Y_1 Orientation Only	100%	2001, Condition E (Min) Y_1 Orientation Only	100%
7. Visual Inspection (Note 3)		100%		100%
8. Particle Impact Noise Detection (PIND)	2020, Condition A (Note 4)	100%		
9. Serialization	(Note 5)	100%		
10. Interim (Pre-Burn-In) Electrical Parameters	Per Applicable Device Specification (Note 13)	100%	Per Applicable Device Specification (Note 6)	
11. Burn-In Test	1015 240 Hrs. at 125°C Min (Cond. F Not Allowed)	100%	1015, 160 Hrs. at 125°C Min	100%

TABLE III. 100% Screening Requirements (Continued)

Screen	Class S		Class B	
	Method	Reqmt	Method	Reqmt
12. Interim (Post-Burn-In) Electrical Parameters	Per Applicable Device Specification (Note 13)	100%		
13. Reverse Bias Burn-In (Note 7)	1015; Test Condition A, C, 72 Hrs. at 150°C Min (Cond. F Not Allowed)	100%		
14. Interim (Post-Burn-In) Electrical Parameters	Per Applicable Device Specification (Note 13)	100%	Per Applicable Device Specification	100%
15. PDA Calculation	5% Parametric (Note 14) 3% Functional — 25°C	All Lots	5% Parametric (Note 14)	All Lots
16. Final Electrical Test a) Static Tests 1) 25°C (Subgroup 1, Table I, 5005) 2) Max & Min Rated Operating Temp (Subgroups 2, 3, Table I, 5005) b) Dynamic Tests & Switching Tests, 25°C (Subgroups 4, 9, Table I, 5005) c) Functional Test, 25°C (Subgroup 7, Table I, 5005)	Per Applicable Device Specification	 100% 100% 100% 100%	Per Applicable Device Specification	 100% 100% 100% 100%
17. Seal Fine, Gross	1014	100% (Note 8)	1014	100% (Note 9)
18. Radiographic (Note 10)	2012 Two Views	100%		
19. Qualification or Quality Conformance Inspection Test Sample Selection	(Note 11)	Samp.	(Note 11)	Samp.
20. External Visual (Note 12)	2009	100%		100%

Note 1: Unless otherwise specified, at the manufacturer's option, test samples for Group B, bond strength (Method 5005) may be randomly selected prior to or following internal visual (Method 5004), prior to sealing provided all other specification requirements are satisfied (e.g. bond strength requirements shall apply to each inspection lot, bond failures shall be counted even if the bond would have failed internal visual).

Note 2: For Class B devices, this test may be replaced with thermal shock method 1011, test condition A, minimum.

Note 3: At the manufacturer's option, visual inspection for castastrophic failures may be conducted after each of the thermal/mechanical screens, after the sequence or after seal test. Catastrophic failures are defined as missing leads, broken packages or lids off.

Note 4: The PIND test may be performed in any sequence after step 9 and prior to step 16. See MIL-M-38510, paragraph 4.6.3.

Note 5: Class S devices shall be serialized prior to interim electrical parameter measurements.

Note 6: When specified, all devices shall be tested for those parameters requiring delta calculations.

Note 7: Reverse bias burn-in is a requirement only when specified in the applicable device specification. The order of performing burn-in and reverse bias burn-in may be inverted.

Note 8: For Class S devices, the seal test may be performed in any sequence between step 16 and step 19, but it shall be performed after all shearing and forming operations on the terminals.

Note 9: For Class B devices, the fine and gross seal tests shall be performed separate or together in any sequence and order between step 6 and step 20 except that they shall be performed after all shearing and forming operations on the terminals. When 100% seal screen cannot be performed after shearing and forming (e.g. flatpacks and chip carriers) the seal screen shall be done 100% prior to those operations and a sample test (LTPD = 5) shall be performed on each inspection lot following these operations. If the sample fails, 100% rescreening shall be required.

Note 10: The radiographic screen may be performed in any sequence after step 9.

Note 11: Samples shall be selected for testing in accordance with the specific device class and lot requirements of Method 5005.

Note 12: External visual shall be performed on the lot any time after step 19 and prior to shipment.

Note 13: Read and Record when post burn-in data measurements are specified.

Note 14: PDA shall apply to all static, dynamic, functional and switching measurements at either 25°C or maximum rated operating temperature.

National Semiconductor

Series 32000 Programs and Services

Technical Support Engineering Center (TSEC)

National Semiconductors Technical Support Engineering Center offers full aftersales service support. The Technical Support Staff is available to answer technical questions, and has the ability to utilize all of the resources within the company to resolve issues or problems. Extended maintenance contracts are available extending the warranty period of the product one full year, allowing full technical support, software and/or hardware maintenance.

HIGHLIGHTS OF THE EXTENDED MAINTENANCE PROGRAM

1. Unlimited Technical Assistance—access to 24 hour Hot Line and factory engineering staff.
2. Automatic Software Updates allowing customers to receive all software enhancements or bug fixes free of charge whenever they become available for the products covered.
3. Software Bulletin—Informative newsletter showing current software revisions, bug listings, work arounds, and new product information.
4. Equipment repairs—Factory repair for all products covered, including equipment on loan.

OBTAINING A MAINTENANCE CONTRACT

1. Determine which product(s) are to be placed under maintenance (refer to the Service Products Guide).
2. Fill out the Maintenance Contract and return to the Service Center along with a purchase order, or call any of the TSEC 800 numbers and a completed contract will be sent to your attention for signature. Return the contract along with a purchase order to us.

TOLL-FREE NUMBERS

(800) 538-1866 (Outside of California)
(800) 672-1811 (Inside California)
(800) 223-3248 (Canada)
(408) 749-7306 (Rest of World)
49-08141-103-0 (Europe)

FACTORY REPAIRS

The Service Center provides highly trained technicians and a complete range of Depot Services to meet your service needs. For more information on depot services and pricing, call one of the Service Center phone numbers listed above.

EVALUATION PROGRAM

The Series 32000 Development hardware and software products are available for a free 30 day evaluation. For full details and qualifications on the evaluation program, please call one of the Service Center phone numbers listed above or your local sales office.

The University Program

Begun as merely a concept several years ago, National Semiconductor's University Program has now emerged as one of the company's most successful programs. The University Program was originally created to establish a relationship between National and the academic community that would foster the exchange of information and keep students abreast of modern advancements in technology.

The University Program catalog provides a complete, up-to-date list of all student/university services as well as program application forms and course materials to guide instructors in introducing students to advanced microprocessors.

Because tomorrow's technology is dependent upon today's nurturing of up-and-coming scientists and engineers, National is committed to supporting universities, particularly in the area of microprocessor technology. National hopes that more universities will share in this commitment by becoming a part of the University Program.

For more information on any of these programs, contact the Series 32000 University Program Manager, National Semiconductor Corporation, P.O. Box 58090, M/S D3-667, Santa Clara, California 95052-8090, 408-721-7295.

Microcomputer Systems Division

The Microcomputer Systems Division's goal is to become a leading force in the microcomputer systems marketplace.

To achieve this goal, a total systems approach has been taken on the Series 32000 program to provide the customer with the necessary hardware and software support, evaluation and development tools, training, service and technical literature.

The focus is on upward migration paths, system integration at all levels and the preservation of the user's software investment.

Three groups (Microprocessor, Software Products and Development Systems) offer a broad capability to solve customer needs at various levels of performance and integration.

Section 2

CPU—Central Processing Units

Section 2 Contents

National Semiconductor

PRELIMINARY

NS32532-20/NS32532-25/NS32532-30 High-Performance 32-Bit Microprocessor

General Description

The NS32532 is a high-performance 32-bit microprocessor in the Series 32000® family. It is software compatible with the previous microprocessors in the family but with a greatly enhanced internal implementation.

The high-performance specifications are the result of a four-stage instruction pipeline, on-chip instruction and data caches, on-chip memory management unit and a significantly increased clock frequency. In addition, the system interface provides optimal support for applications spanning a wide range, from low-cost, real-time controllers to highly sophisticated, general purpose multiprocessor systems.

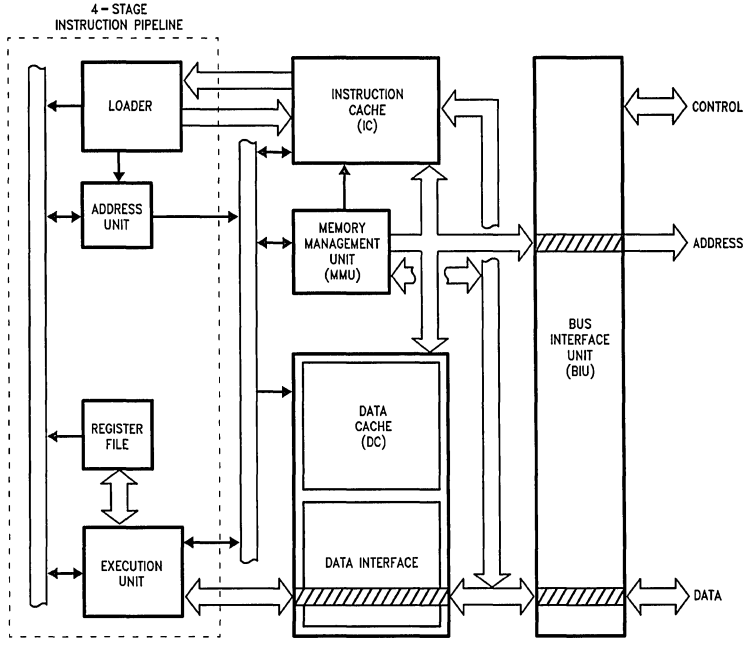
The NS32532 integrates more than 370,000 transistors fabricated in a 1.25 μm double-metal CMOS technology. The advanced technology and mainframe-like design of the device enable it to achieve more than 10 times the throughput of the NS32032 in typical applications.

In addition to generally improved performance, the NS32532 offers much faster interrupt service and task switching for real-time applications.

Features

- Software compatible with the Series 32000 family
- 32-bit architecture and implementation
- 4-GByte uniform addressing space
- On-chip memory management unit with 64-entry translation look-aside buffer
- 4-Stage instruction pipeline
- 512-Byte on-chip instruction cache
- 1024-Byte on-chip data cache
- High-performance bus
  - — Separate 32-bit address and data lines
  - — Burst mode memory accessing
  - — Dynamic bus sizing
- Extensive multiprocessing support
- Floating-point support via the NS32381 or NS32580
- 1.25 μm double-metal CMOS technology
- 175-pin PGA package

Block Diagram



TL/EE/9354–1

FIGURE 1

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1.0 Product Introduction

The NS32532 is an extremely sophisticated microprocessor in the Series 32000 family with a full 32-bit architecture and implementation optimized for high-performance applications.

By employing a number of mainframe-like features, the device can deliver 15 MIPS peaks performance with no wait states at a frequency of 30 MHz.

The NS32532 is fully software compatible will all the other Series 32000 CPUs. The architectural features of the Series 32000 family and particularly the NS32532 CPU, are described briefly below.

Powerful Addressing Modes. Nine addressing modes available to all instructions are included to access data structures efficiently.

Data Types. The architecture provides for numerous data types, such as byte, word, doubleword, and BCD, which may be arranged into a wide variety of data structures.

Symmetric Instruction Set. While avoiding special case instructions that compilers can't use, the Series 32000 architecture incorporates powerful instructions for control operations, such as array indexing and external procedure calls, which save considerable space and time for compiled code.

Memory-to-Memory Operations. The Series 32000 CPUs represent two-address machines. This means that each operand can be referenced by any one of the addressing modes provided.

This powerful memory-to-memory architecture permits memory locations to be treated as registers for all usefull operations. This is important for temporary operands as well as for context switching.

Memory Management. The NS32532 on-chip memory management unit provides advanced operating system support functions, including dynamic address translation, virtual memory management, and memory protection.

Large, Uniform Addressing. The NS32532 has 32-bit address pointers that can address up to 4 gigabytes without requiring any segmentation; this addressing scheme provides flexible memory management without added-on expense.

Modular Software Support. Any software package for the Series 32000 family can be developed independent of all other packages, without regard to individual addressing. In addition, ROM code is totally relocatable and easy to access, which allows a significant reduction in hardware and software costs.

Software Processor Concept. The Series 32000 architecture allows future expansions of the instruction set that can be executed by special slave processors, acting as extensions to the CPU. This concept of slave processors is unique to the Series 32000 family. It allows software compatibility even for future components because the slave hardware is transparent to the software. With future advances in semiconductor technology, the slaves can be physically integrated on the CPU chip itself.

To summarize, the architectural features cited above provide three primary performance advantages and characteristics:

- High-level language support
- Easy future growth path
- Application flexibility

2.0 Architectural Description

2.1 REGISTER SET

The NS32532 CPU has 28 internal registers grouped according to functions as follows: 8 general purpose, 7 address, 1 processor status, 1 configuration, 7 memory management and 4 debug. All registers are 32 bits wide except for the module and processor status, which are each 16 bits wide. *Figure 2-1* shows the NS32532 internal registers.

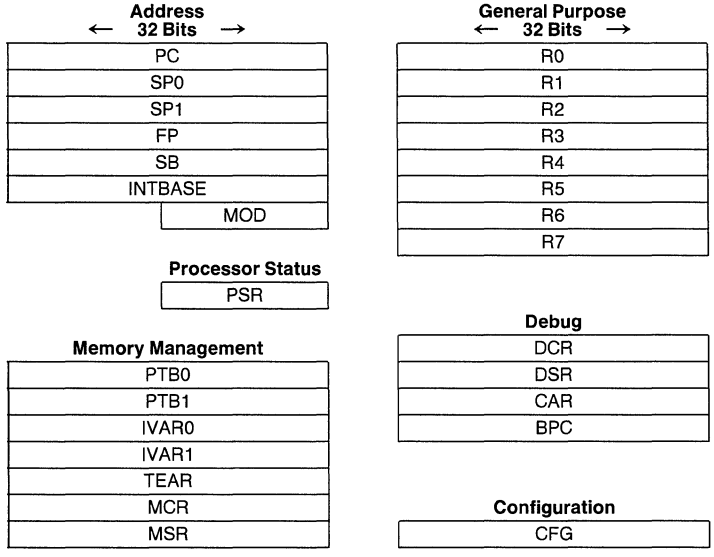


FIGURE 2-1. NS32532 Internal Registers

2.0 Architectural Description (Continued)

2.1.1 General Purpose Registers

There are eight registers (R0–R7) used for satisfying the high speed general storage requirements, such as holding temporary variables and addresses. The general purpose registers are free for any use by the programmer. They are 32 bits in length. If a general purpose register is specified for an operand that is eight or 16 bits long, only the low part of the register is used; the high part is not referenced or modified.

2.1.2 Address Registers

The seven address registers are used by the processor to implement specific address functions. A description of them follows.

PC—Program Counter. The PC register is a pointer to the first byte of the instruction currently being executed. The PC is used to reference memory in the program section.

SP0, SP1—Stack Pointers. The SP0 register points to the lowest address of the last item stored on the INTERRUPT STACK. This stack is normally used only by the operating system. It is used primarily for storing temporary data, and holding return information for operating system subroutines and interrupt and trap service routines. The SP1 register points to the lowest address of the last item stored on the USER STACK. This stack is used by normal user programs to hold temporary data and subroutine return information.

When a reference is made to the selected Stack Pointer (see PSR S-bit), the terms 'SP Register' or 'SP' are used. SP refers to either SP0 or SP1, depending on the setting of the S bit in the PSR register. If the S bit in the PSR is 0, SP refers to SP0. If the S bit in the PSR is 1 then SP refers to SP1.

The NS32532 also allows the SP1 register to be directly loaded and stored using privileged forms of the LPRi and SPRi instructions, regardless of the setting of the PSR S-bit. When SP1 is accessed in this manner, it is referred to as 'USP Register' or simply 'USP'.

Stacks in the Series 32000 family grow downward in memory. A Push operation pre-decrements the Stack Pointer by the operand length. A Pop operation post-increments the Stack Pointer by the operand length.

FP—Frame Pointer. The FP register is used by a procedure to access parameters and local variables on the stack. The FP register is set up on procedure entry with the ENTER instruction and restored on procedure termination with the EXIT instruction.

The frame pointer holds the address in memory occupied by the old contents of the frame pointer.

SB—Static Base. The SB register points to the global variables of a software module. This register is used to support relocatable global variables for software modules. The SB register holds the lowest address in memory occupied by the global variables of a module.

INTBASE—Interrupt Base. The INTBASE register holds the address of the dispatch table for interrupts and traps (Section 3.2.1).

MOD—Module. The MOD register holds the address of the module descriptor of the currently executing software module. The MOD register is 16 bits long, therefore the module table must be contained within the first 64 kbytes of memory.

2.1.3 Processor Status Register

The Processor Status Register (PSR) holds status information for the microprocessor.

The PSR is sixteen bits long, divided into two eight-bit halves. The low order eight bits are accessible to all programs, but the high order eight bits are accessible only to programs executing in Supervisor Mode.

C The C bit indicates that a carry or borrow occurred after an addition or subtraction instruction. It can be used with the ADDC and SUBC instructions to perform multiple-precision integer arithmetic calculations. It may have a setting of 0 (no carry or borrow) or 1 (carry or borrow).

T The T bit causes program tracing. If this bit is set to 1, a TRC trap is executed after every instruction (Section 3.3.1).

L The L bit is altered by comparison instructions. In a comparison instruction the L bit is set to "1" if the second operand is less than the first operand, when both operands are interpreted as unsigned integers. Otherwise, it is set to "0". In Floating-Point comparisons, this bit is always cleared.

V The V-bit enables generation of a trap (OVF) when an integer arithmetic operation overflows.

F The F bit is a general condition flag, which is altered by many instructions (e.g., integer arithmetic instructions use it to indicate overflow).

Z The Z bit is altered by comparison instructions. In a comparison instruction the Z bit is set to "1" if the second operand is equal to the first operand; otherwise it is set to "0".

N The N bit is altered by comparison instructions. In a comparison instruction the N bit is set to "1" if the second operand is less than the first operand, when both operands are interpreted as signed integers. Otherwise, it is set to "0".

U If the U bit is "1" no privileged instructions may be executed. If the U bit is "0" then all instructions may be executed. When U = 0 the processor is said to be in Supervisor Mode; when U = 1 the processor is said to

15							8	7							0
				I	P	S	U	N	Z	F	V		L	T	C

FIGURE 2-2. Processor Status Register (PSR)

2.0 Architectural Description (Continued)

be in User Mode. A User Mode program is restricted from executing certain instructions and accessing certain registers which could interfere with the operating system. For example, a User Mode program is prevented from changing the setting of the flag used to indicate its own privilege mode. A Supervisor Mode program is assumed to be a trusted part of the operating system, hence it has no such restrictions.

S The S bit specifies whether the SP0 register or SP1 register is used as the Stack Pointer. The bit is automatically cleared on interrupts and traps. It may have a setting of 0 (use the SP0 register) or 1 (use the SP1 register).

P The P bit prevents a TRC trap from occuring more than once for an instruction (Section 3.3.1). It may have a setting of 0 (no trace pending) or 1 (trace pending).

I If I = 1, then all interrupts will be accepted. If I = 0, only the NMI interrupt is accepted. Trap enables are not affected by this bit.

2.1.4 Configuration Register

The Configuration Register (CFG) is 32 bits wide, of which nine bits are implemented. The implemented bits enable various operating modes for the CPU, including vectoring of interrupts, execution of slave instructions, and control of the on-chip caches. In the NS32332 bits 4 through 7 of the CFG register selected between the 16-bit and 32-bit slave protocols and between 512-byte and 4-Kbyte page sizes. The NS32532 supports only the 32-bit slave protocol and 4-Kbyte page size: consequently these bits are forced to 1.

When the CFG register is loaded using the LPRi instruction, bits 13 through 31 should be set to 0. Bits 4 through 7 are ignored during loading, and are always returned as 1's when CFG is stored via the SPRi instruction. When the SETCFG instruction is executed, the contents of the CFG register bits 0 through 3 are loaded from the instruction's short field, bits 4 through 7 are ignored and bits 8 through 12 are forced to 0.

The format of the CFG register is shown in *Figure 2-3*. The various control bits are described below.

I Interrupt vectoring. This bit controls whether maskable interrupts are handled in nonvectored (I=0) or vectored (I=1) mode. Refer to Section 3.2.3 for more information.

F Floating-point instruction set. This bit indicates whether a floating-point unit (FPU) is present to execute floating-point instructions. If this bit is 0 when the CPU executes a floating-point instruction, a Trap (UND) occurs. If this bit is 1, then the CPU transfers the instruction and any necessary operands to the FPU using the slave-processor protocol described in Section 3.1.4.1.

M Memory management instruction set. This bit enables the execution of memory management instructions. If this bit is 0 when the CPU executes an LMR, SMR, RDVAL, or WRVAL instruction, a Trap (UND) occurs. If this bit is 1, the CPU executes LMR, SMR, RDVAL, and WRVAL instructions using the on-chip MMU.

C Custom instruction set. This bit indicates whether a custom slave processor is present to execute custom instructions. If this bit is 0 when the CPU executes a custom instruction, a Trap (UND) occurs. If this bit is 1, the CPU transfers the instruction and any necessary operands to the custom slave processor using the slave-processor protocol described in Section 3.1.4.1.

DE Direct-Exception mode enable. This bit enables the Direct-Exception mode for processing exceptions. When this mode is selected, the CPU response time to interrupts and other exceptions is significantly improved. Refer to Section 3.2.1 for more information.

DC Data Cache enable. This bit enables the on-chip Data Cache to be accessed for data reads and writes. Refer to Section 3.4.2 for more information.

LDC Lock Data Cache. This bit controls whether the contents of the on-chip Data Cache are locked to fixed memory locations (LDC=1), or updated when a data read is missing from the cache (LDC=0).

IC Instruction Cache enable. This bit enables the on-chip Instruction Cache to be accessed for instruction fetches. Refer to Section 3.4.1 for more information.

LIC Lock Instruction Cache. This bit controls whether the contents of the on-chip Instruction Cache are locked to fixed memory locations (LIC=1), or updated when an instruction fetch is missing from the cache (LIC=0).

PF Pipelined Floating-point execution. This bit indicates whether the floating-point unit uses the pipelined slave protocol. When PF is 1 the pipelined protocol is selected. PF is ignored if the F bit is 0. Refer to Section 3.1.4.2 for more information.

31 14	13					8	7							0
Reserved	PF	LIC	IC	LDC	DC	DE	1	1	1	1	C	M	F	I

FIGURE 2-3. Configuration Register (CFG) Bits 13 to 31 are Reserved; Bits 4 to 7 are Forced to 1.

2.0 Architectural Description (Continued)

2.1.5 Memory Management Registers

The NS32532 provides 7 registers to support memory management functions. They are accessed by means of the LMR and SMR instructions. All of them can be read and written except IVAR0 and IVAR1 that are write-only. A description of the memory management registers is given in the following sections.

PTB0, PTB1—Page Table Base Pointers. The PTBn registers hold the physical addresses of the level-1 page tables used in address translation. The least significant 12 bits are permanently zero, so that each register always points to a 4-Kbyte boundary in memory.

When either PTB0 or PTB1 is loaded by executing an LMR instruction, the MMU automatically invalidates all entries in the TLB that had been translated using the old value in the selected PTBn register.

The format of the PTBn registers is shown in *Figure 2-4*.

31 12	11 0
Base Address	000000000000

FIGURE 2-4. Page Table Base Registers (PTBn)

IVAR0, IVAR1—Invalidate Virtual Address. The Invalidate Virtual Address registers are write-only registers. When a virtual address is written to IVAR0 or IVAR1 using the LMR instruction, the translation for that virtual address is purged, if present, from the TLB. This must be done whenever a Page Table Entry has been changed in memory, since the TLB might otherwise contain an incorrect translation value.

Another technique for purging TLB entries is to load a PTBn register. Turning off translation (clearing the MCR TU and/or TS bits) does not purge any entries from the TLB.

TEAR—Translation Exception Address Register. The TEAR register is laoded by the on-chip MMU when a translation exception occurs. It contains the 32-bit virtual address that caused the translation exception.

TEAR is not updated if a page fault is detected while prefetching an instruction that is not executed because the previous instruction caused a trap.

MCR—Memory Management Control. The MCR register controls the operation of the MMU. Only four bits are implemented. Bits 4 to 31 are reserved for future use and must be loaded with zeroes.

When MCR is read as a 32-bit word, bits 4 to 31 are returned as zeroes. The format of MCR is shown in *Figure 2-5*. Details on the control bits are given below.

TU Translate User. While this bit is 1, address translation is enabled for User-Mode memory references. While this bit is 0, address translations is disabled for User-Mode memory references.

TS Translate Supervisor. While this bit is 1, address translation is enabled for Supervisor Mode memory references. While this bit is 0, address translation is disabled for Supervisor-Mode memory references.

DS Dual Space. While this bit is 1, then PTB1 contains the level-1 page table base address of all addresses specified in User-Mode, and PTB0 contains the level-1 page table base address of all addresses specified in Supervisor Mode. While this bit is 0, then PTB0 contains the level-1 page table base address of all addresses specified in both User and Supervisor Modes.

AO Access Level Override. When this bit is set to 1, User-Mode accesses are given Supervisor Mode privilege.

31 4	3			0
Reserved	AO	DS	TS	TU

FIGURE 2-5. Memory Management Control Register (MCR)

MSR—Memory Management Status. The MSR register provides status information related to the occurrence of a translation exception. Only eight bits are implemented. Bits 8 to 31 are ignored when MSR is loaded and are returned as zeroes when it is read as a 32-bit word. MSR is only updated by the MMU when a protection violation or page fault is detected while translating an address for a reference required to execute an instruction. It is not updated if a page fault is detected during either an operand or an instruction prefetch, if the data being prefetched is not needed due to a change in the instruction execution sequence. The format of MSR is shown in *Figure 2-6*. Details on the function of each bit are given below.

TEX Translation Exception. This two-bit field specifies the cause of the current address translation exception. (Trap(ABT)). Combinations appearing in this field are summarized below.

00 No Translation Exception

01 First Level PTE Invalid

10 Second Level PTE Invalid

11 Protection Violation

During address translation, if a protection violation and an invalid PTE are detected at the same time, the TEX field is set to indicate a protection violation.

DDT Data Direction. This bit indicates the direction of the transfer that the CPU was attempting when the translation exception occurred.

DDT = 0 => Read Cycle

DDT = 1 => Write Cycle

UST User/Supervisor. This bit indicates whether the Translation Exception was caused by a User-Mode or Supervisor Mode reference. If UST is 1, then the exception was caused by a User-Mode reference; otherwise it was caused by a Supervisor Mode reference.

2.0 Architectural Description (Continued)

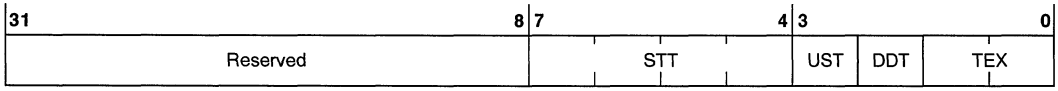


FIGURE 2-6. Memory Management Status Register (MSR)

STT CPU Status. This four bit field is set on an address translation exception according to the following encodings.

1000 Sequential Instruction Fetch
1001 Non-Sequential Instruction Fetch
1010 Data Transfer
1011 Read Read-Modify-Write Operand
1100 Read for Effective Address

If a reference for an Interrupt-Acknowledge or End-of-Interrupt bus cycle (either Master of Cascaded) causes a Translation Exception, then the value of the STT-field is undefined.

2.1.6 Debug Registers

The NS32532 contains 4 registers dedicated for debugging functions.

These registers are accessed using privileged forms of the LPRi and SPRi instructions.

DCR—Debug Condition Register. The DCR Register enables detection of debug conditions. The format of the DCR is shown in *Figure 2-7;* the various bits are described below. A debug condition is enabled when the related bit is set to 1.

CBE0 Compare Byte Enable 0; when set, BYTE0 of an aligned double-word is included in the address comparison

CBE1 Compare Byte Enable 1; when set, BYTE1 of an aligned double-word is included in the address comparison

CBE2 Compare Byte Enable 2; when set, BYTE2 of an aligned double-word is included in the address comparison

CBE3 Compare Byte Enable 3; when set, BYTE3 of an aligned double-word is included in the address comparison

VNP Compare virtual address (VNP = 1) or physical address (VNP = 0)

CWR Address-compare enable for write references

CRD Address-compare enable for read references

CAE Address-compare enable

TR Enable Trap (DBG) when a debug condition is detected

PCE PC-match enable

UD Enable debug conditions in User-Mode

SD Enable debug conditions in Supervisor Mode

DEN Enable debug conditions

The following 3 bits control testing features that can be used during initial system debugging. These features are unique to the NS32532 implementation of the Series 32000 architecture; as such, they may not be supported in future implementations. For normal operation these 3 bits should be set to 0.

BF Bus interface unit FIFO disable. When this bit is 1, all data references, including Data Cache hits, appear on the system interface.

SI Single-Instruction mode enable. This bit, when set to 1, inhibits the overlapping of instruction's execution.

BCP Branch Condition Prediction disable. When this bit is 1, the branch prediction mechanism is disabled. See Section 3.1.3.1.

DSR—Debug Status Register. The DSR Register indicates debug conditions that have been detected. When the CPU detects an enabled debug condition, it sets the corresponding bit (BC, BEX, BCA) in the DSR to 1. When an address-compare condition is detected, then the RD-bit is loaded to indicate whether a read or write reference was performed. Software must clear all the bits in the DSR when appropriate. The format of the DSR is shown in *Figure 2-8;* the various fields are described below.

RD Indicates whether the last address-compare condition was for a read (RD = 1) or write (RD = 0) reference

BPC PC-match condition detected

BEX External condition detected

BCA Address-compare condition detected

CAR—Compare Address Register. The CAR Register contains the address that is compared to operand reference addresses to detect an address-compare condition. The address must be double-word aligned; that is, the two least-significant bits must be 0. The CAR is 32 bits wide.

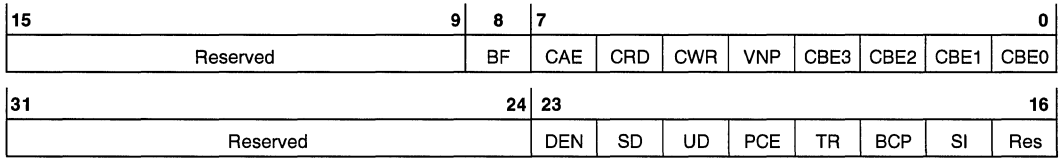


FIGURE 2-7. Debug Condition Register (DCR)

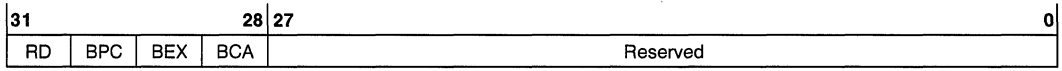


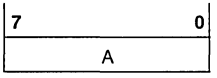
FIGURE 2-8. Debug Status Register (DSR)

2.0 Architectural Description (Continued)

BPC—Breakpoint Program Counter. The BPC Register contains the address that is compared with the PC contents to detect a PC-match condition. The BPC Register is 32 bits wide.

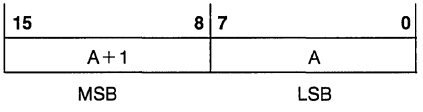
2.2 MEMORY ORGANIZATION

The NS32532 implements full 32-bit virtual addresses. This allows the CPU to access up to 4 Gbytes of virtual memory. The memory is a uniform linear address space. Memory locations are numbered sequentially starting at zero and ending at $2^{32}-1$. The number specifying a memory location is called an address. The contents of each memory location is a byte consisting of eight bits. Unless otherwise noted, diagrams in this document show data stored in memory with the lowest address on the right and the highest address on the left. Also, when data is shown vertically, the lowest address is at the top of a diagram and the highest address at the bottom of the diagram. When bits are numbered in a diagram, the least significant bit is given the number zero, and is shown at the right of the diagram. Bits are numbered in increasing significance and toward the left.



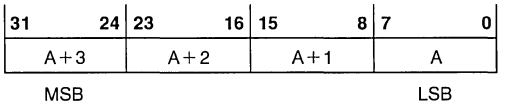
Byte at Address A

Two contiguous bytes are called a word. Except where noted, the least significant byte of a word is stored at the lower address, and the most significant byte of the word is stored at the next higher address. In memory, the address of a word is the address of its least significant byte, and a word may start at any address.



Word at Address A

Two contiguous words are called a double-word. Except where noted, the least significant word of a double-word is stored at the lowest address and the most significant word of the double-word is stored at the address two higher. In memory, the address of a double-word is the address of its least significant byte, and a double-word may start at any address.



Double-Word at Address A

Although memory is addressed as bytes, it is actually organized as double-words. Note that access time to a word or a double-word depends upon its address, e.g. double-words that are aligned to start at addresses that are multiples of four will be accessed more quickly than those not so aligned. This also applies to words that cross a double-word boundary.

2.2.1 Address Mapping

Figure 2-9 shows the NS32532 address mapping.

The NS32532 supports the use of memory-mapped peripheral devices and coprocessors. Such memory-mapped devices can be located at arbitrary locations in the address space except for the upper 8 Mbytes of virtual memory (addresses between FF800000 (hex) and FFFFFFFF (hex), inclusive), which are reserved by National Semiconductor Corporation. Nevertheless, it is recommended that high-performance peripheral devices and coprocessors be located in a specific 8 Mbyte region of virtual memory (addresses between FF000000 (hex) and FF7FFFFF (hex), inclusive), that is dedicated for memory-mapped I/O. This is because the NS32532 detects references to the dedicated locations and serializes reads and writes. See Section 3.1.3.3. When making I/O references to addresses outside the dedicated region, external hardware must indicate to the NS32532 that special handling is required.

In this case a small performance degradation will also result. Refer to Section 3.1.3.2 for more information on memory-mapped I/O.

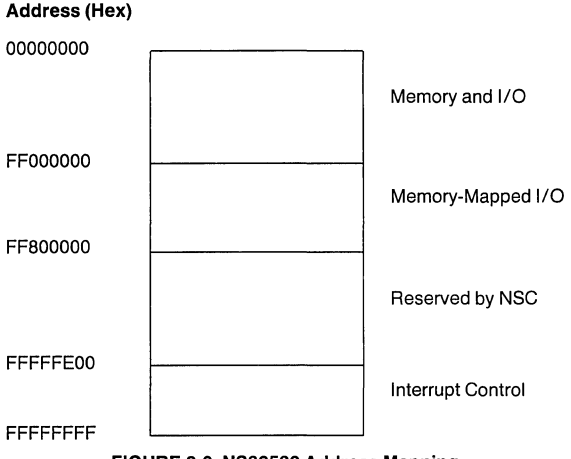


FIGURE 2-9. NS32532 Address Mapping

2.0 Architectural Description (Continued)

2.3 MODULAR SOFTWARE SUPPORT

The NS32532 provides special support for software modules and modular programs.

Each module in a NS32532 software environment consists of three components:

1. Program Code Segment.

   This segment contains the module's code and constant data.

2. Static Data Segment.

   Used to store variables and data that may be accessed by all procedures within the module.

3. Link Table.

   This component contains two types of entries: Absolute Addresses and Procedure Descriptors.

   An Absolute Address is used in the external addressing mode, in conjunction with a displacement and the current MOD Register contents to compute the effective address of an external variable belonging to another module.

   The Procedure Descriptor is used in the call external procedure (CXP) instruction to compute the address of an external procedure.

Normally, the linker program specifies the locations of the three components. The Static Data and Link Table typically reside in RAM; the code component can be either in RAM or in ROM. The three components can be mapped into non-contiguous locations in memory, and each can be independently relocated. Since the Link Table contains the absolute addresses of external variables, the linker need not assign absolute memory addresses for these in the module itself; they may be assigned at load time.

To handle the transfer of control from one module to another, the NS32532 uses a module table in memory and two registers in the CPU.

The Module Table is located within the first 64 kbytes of virtual memory. This table contains a Module Descriptor (also called a Module Table Entry) for each module in the address space of the program. A Module Descriptor has four 32-bit entries corresponding to each component of a module:

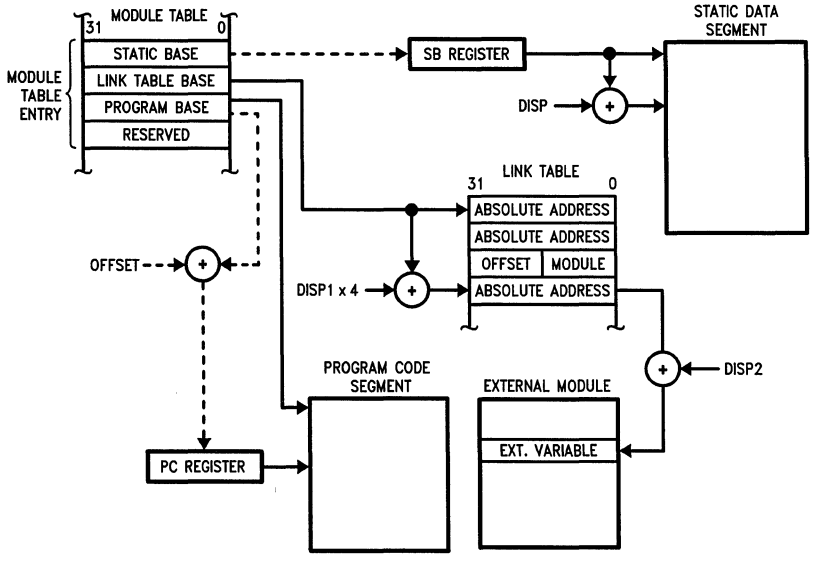
- The Static Base entry contains the address of the beginning of the module's static data segment.
- The Link Table Base points to the beginning of the module's Link Table.
- The Program Base is the address of the beginning of the code and constant data for the module.
- A fourth entry is currently unused but reserved.

The MOD Register in the CPU contains the address of the Module Descriptor for the currently executing module.

The Static Base Register (SB) contains a copy of the Static Base entry in the Module Descriptor of the currently executing module, i.e., it points to the beginning of the current module's static data area.

This register is implemented in the CPU for efficiency purposes. By having a copy of the static base entry or chip, the CPU can avoid reading it from memory each time a data item in the static data segment is accessed.

In an NS32532 software environment modules need not be linked together prior to loading. As modules are loaded, a linking loader simply updates the Module Table and fills the Link Table entries with the appropriate values. No modification of a module's code is required. Thus, modules may be stored in read-only memory and may be added to a system independently of each other, without regard to their individual addressing. *Figure 2-10* shows a typical NS32532 run-time environment.



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Note: Dashed lines indicate information copied to registers during transfer of control between modules.

FIGURE 2-10. NS32532 Run-Time Environment

2.0 Architectural Description (Continued)

2.4 MEMORY MANAGEMENT

The Memory Mangement Unit of the NS32532 provides support for demand-paged virtual memory. The MMU translates 32-bit virtual addresses into 32-bit physical addresses. The page size is 4096 bytes.

The mapping from virtual to physical addresses is defined by means of sets of tables in physical memory. These tables are found by the MMU using one of its two Page Table Base registers: PTB0 or PTB1. Which register is used depends on the currently selected address space. See Section 2.4.2.

Translation efficiency is improved by means of an on-chip 64-entry translation look-aside buffer (TLB). Refer to Section 3.4.4 for details.

If the MMU detects a protection violation or page fault while translating an address for a reference required to execute an instruction, a translation exception (Trap (ABT)) will result.

2.4.1 Page Tables Structure

The page tables are arranged in a two-level structure, as shown in *Figure 2-11*. Each of the MMU's PTBn registers may point to a Level-1 page table. Each entry of the Level-1 page table may in turn point to a Level-2 page table. Each Level-2 page table entry contains translation information for one page of the virtual space.

The Level-1 page table must remain in physical memory while the PTBn register contains its address and translation is enabled. Level-2 Page Tables need not reside in physical memory permanently, but may be swapped into physical memory on demand as is done with the pages of the virtual space.

The Level-1 Page Table contains 1024 32-bit Page Table Entries (PTE's) and therefore occupies 4 Kbytes. Each entry of the Level-1 Page Table contains a field used to construct the physical base address of a Level-2 Page Table. This field is a 20-bit PFN field, providing bits 12–31 of the physical address. The remaining bits (0–11) are assumed zero, placing a Level-2 Page Table always on a 4-Kbyte (page) boundary.

Level-2 Page Tables contain 1024 32-bit Page Table entries, and so occupy 4 Kbytes (1 page). Each Level-2 Page Table Entry points to a final 4-Kbyte physical page frame. In other words, its PFN provides the Page Frame Number portion (bits 12–31) of the translated address (*Figure 2-13*). The OFFSET field of the translated address is taken directly from the corresponding field of the virtual address.

2.4.2 Virtual Address Spaces

When the Dual Space option is selected for address translation in the MCR (Section 2.1.5) the on-chip MMU uses two maps: one for translating addresses presented to it in Supervisor Mode and another for User Mode addresses. Each map is referenced by the MMU using one of the two Page Table Base registers: PTB0 or PTB1. The MMU determines the map to be used by applying the following rules.

1) While the CPU is in Supervisor Mode (U/$\overline{S}$ pin = 0), the CPU is said to be generating virtual addresses belonging to Address Space 0, and the MMU uses the PTB0 register as its reference for looking up translations from memory.
2) While the CPU is in User Mode (U/$\overline{S}$ pin = 1), and the MCR DS bit is set to enable Dual Space translation, the CPU is said to be generating virtual addresses belonging to Address Space 1, and the MMU uses the PTB1 register to look up translations.
3) If Dual Space translation is not selected in the MCR, there is no Adress Space 1, and all virtual addresses generated in both Supervisor and User modes are considered by the MMU to be in Address Space 0. The privilege level of the CPU is used then only for access level checking.

Note: When the CPU executes a Dual-Space Move instruction (MOVUSi or MOVSUi), it temporarily enters User Mode by switching the state of the U/$\overline{S}$ pin. Accesses made by the CPU during this time are treated by the MMU as User-Mode accesses for both mapping and access level checking. It is possible, however, to force the MMU to assume Supervisor Mode privilege on such accesses by setting the Access Override (AO) bit in the MCR (Section 2.1.5).

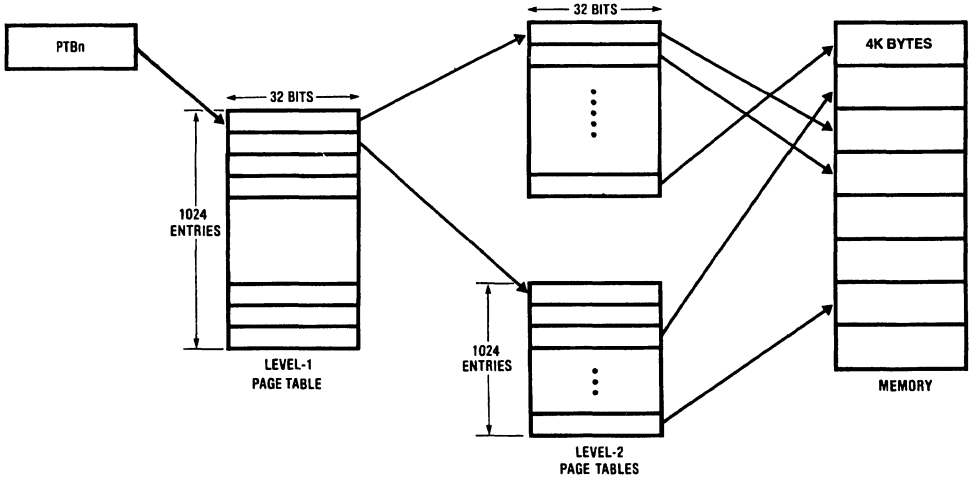

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FIGURE 2-11. Two-Level Page Tables

2.0 Architectural Description (Continued)

2.4.3 Page Table Entry Formats

Figure 2-12 shows the formats of Level-1 and Level-2 Page Table Entries (PTE's).

The bits are defined as follows:

V Valid. The V bit is set and cleared only by software.

V = 1 => The PTE is valid and may be used for translation by the MMU.

V = 0 => The PTE does not represent a valid translation. Any attempt to use this PTE to translate and address will cause the MMU to generate an Abort trap.

PL Protection Level. This two-bit field establishes the types of accesses permitted for the page in both User Mode and Supervisor Mode, as shown in Table 2-1.

The PL field is modified only by software. In a Level-1 PTE, it limits the maximum access level allowed for all pages mapped through that PTE.

TABLE 2-1. Access Protection Levels

Mode	U/$\overline{S}$	Protection Level Bits (PL)			
		00	01	10	11
User	1	no access	no access	read only	full access
Supervisor	0	read only	full access	full access	full access

NU Not Used. These bits are reserved by National for future enhancements. Their values should be set to zero.

CI Cache Inhibit. This bit appears only in Level-2 PTE's. It is used to specify non-cacheable pages.

R Referenced. This is a status bit, set by the MMU and cleared by the operating system, that indicates whether the page mapped by this PTE has been referenced within a period of time determined by the operating system. It is intended to assist in implementing memory allocation strategies. In a Level-1 PTE, the R bit indicates only that the Level-2 Page Table has been referenced for a translation, without necessarily implying that the translation was successful. In a Level-2 PTE, it indicates that the page mapped by the PTE has been sucessfully referenced.

R = 1 => The page has been referenced since the R bit was last cleared.

R = 0 => The page has not been referenced since the R bit was last cleared.

M Modified. This is a status bit, set by the MMU whenever a write cycle is successfully performed to the page mapped by this PTE. It is initialized to zero by the operating system when the page is brought into physical memory.

M = 1 => The page has been modified since it was last brought into physical memory.

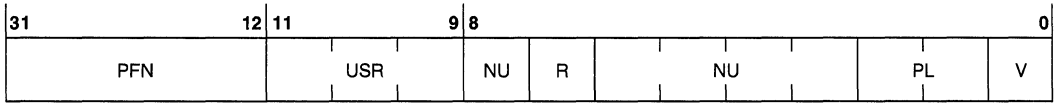
M = 0 => The page has not been modified since it was last brought into physical memory.

In Level-1 Page Table Entries, this bit position is undefined, and is unaltered.

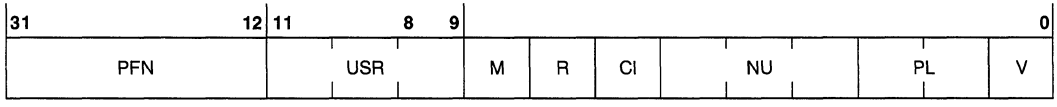
USR User bits. These bits are ignored by the MMU and their values are not changed.

They can be used by the user software.

PFN Page Frame Number. This 20-bit field provides bits 12–31 of the physical address. See *Figure 2-13*.



First Level PTE



Second Level PTE

FIGURE 2-12. Page Table Entries (PTE's)

2.0 Architectural Description (Continued)

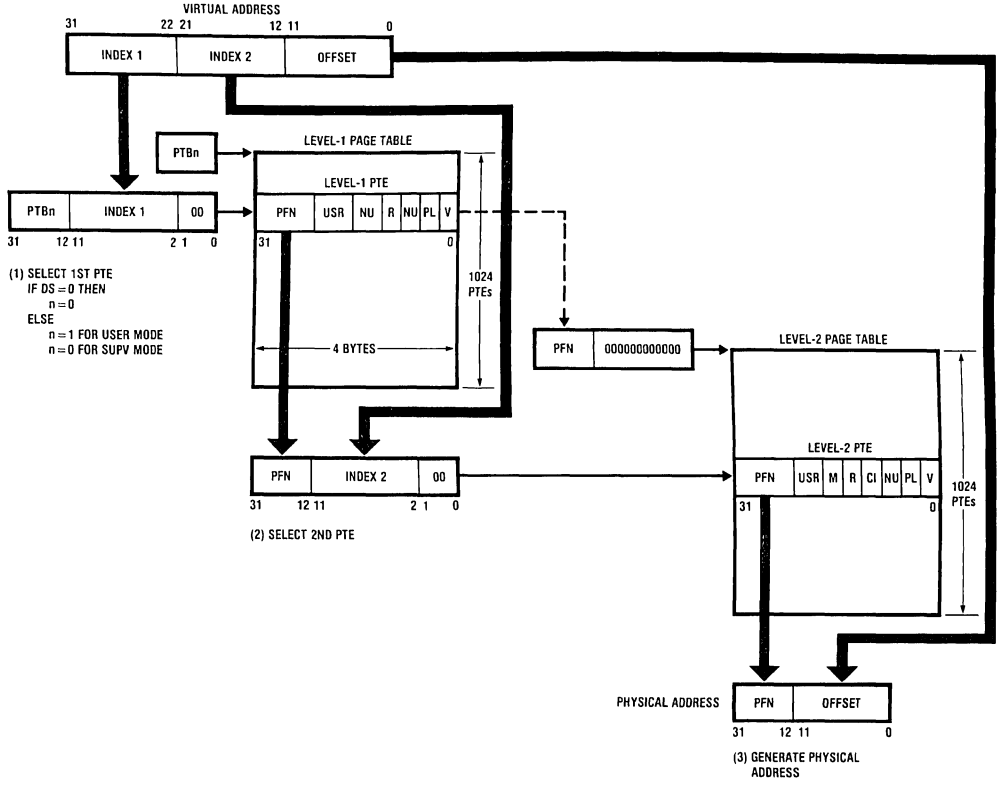


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FIGURE 2-13. Virtual to Physical Address Translation

2.4.4 Physical Address Generation

When a virtual address is presented to the MMU and the translation information is not in the TLB, the MMU performs a page table lookup in order to generate the physical address.

The Page Table structure is traversed by the MMU using fields taken from the virtual address. This sequence is diagrammed in *Figure 2-13*.

Bits 12–31 of the virtual address hold the 20-bit Page Number, which in the course of the translation is replaced with the 20-bit Page Frame Number of the physical address. The virtual Page Number field is further divided into two fields, INDEX 1 and INDEX 2.

Bits 0–11 constitute the OFFSET field, which identifies a byte's position within the accessed page. Since the byte position within a page does not change with translation, this value is not used, and is simply echoed by the MMU as bits 0–11 of the final physical address.

The 10-bit INDEX 1 field of the virtual address is used as an index into the Level-1 Page Table, selecting one of its 1024 entries. The address of the entry is computed by adding INDEX 1 (scaled by 4) to the contents of the current Page Table Base register. The PFN field of that entry gives the base address of the selected Level-2 Page Table.

The INDEX 2 field of the virtual address (10 bits) is used as the index into the Level-2 Page Table, by adding it (scaled by 4) to the base address taken from the Level-1 Page Table Entry. The PFN field of the selected entry provides the entire Page Frame Number of the translated address.

The offset field of the virtual address is then appended to this frame number to generate the final physical address.

2.4.5. Address Translation Algorithm

The MMU either translates the 32-bit virtual address to a 32-bit physical address or generates an abort trap to report a translation error. The algorithm used by the MMU to perform the translation is compatible with that of the NS32382. Refer to Appendix C for differences between the two MMUs.

In the description that follows, the symbol 'U' takes the value 1 for a User-Mode memory reference. A reference is a User-Mode reference in the following cases:

1. The reference is performed while executing in User-Mode.
2. The reference is for the source operand of a MOVUS instruction.
3. The reference is for the destination operand of a MOVSU instruction.

The following notations are used in the algorithm.

- A||B → A concatenated with B
- A.B → B is a field inside register A
- (A) → object pointed to by address A
- (A).B → B field of the object pointed to by address A

2.0 Architectural Description (Continued)

Each access is associated with one of two Address Spaces (AS), defined as follows:

AS = U AND MCR.DS

If AS = 1, Page Table Base Register 1 (PTB1) is used to select the first-level page table. If AS = 0, PTB0 is used to select the first-level page table.

The access-level is a 2-bit value used to specify the privilege level of an access. It is determined as follows:

- BIT1 = U AND (NOT(MCR.A0))
- BIT0 = 1 for write, or read with 'RMW' status
  0 otherwise

START TRANSLATION:

If (U = 0 AND MCR.TS = 0 OR U = 1 AND MCR.TU = 0) **then**

/* address translation disabled */

(physical address ← virtual address; CIOUT pin = 0);

/* Note: CIOUT = 0 in all MMU generated accesses */

else BEGIN /* (see also *Figure 2-13*) */

1. Select PTB:
- **If** (MCR.DS = 1 AND U = 1) **then**
— PTB = PTB1,
— AS = 1;
- **else** (PTB = PTB0, AS = 0);

2. Fetch first level PTE:
- PTE Pointer = PTB.BASE ADDRESS||INDEX1||00;
- PTE ← (PTE Pointer); /* Fetch PTE1 */
- Effective PL ← PTE.PL

3. Validate First Level PTE:
- **If** (PTE.PL < access level) **then**
- /* Protection Exception */
— TEAR ← virtual address,
— clock MSR with MSR.TEX = 11,
— terminate translation;
- **If** (PTE.V = 0) **then**
- /* PTE1 Invalid */
— TEAR ← virtual address,
— clock MSR with MSR.TEX = 01,
— terminate translation;
- **If** (PTE.R = 0) **then**
— Write a Byte (PTE Pointer) .R = 1;
- Effective PL ← PTE.PL

4. Fetch second level PTE:
- PTE Pointer = PTE.PFN||INDEX2||00;
- PTE ← (PTE Pointer); /* Fetch PTE2 */
- **If** (PTE.PL < effective PL) **then**
— Effective PL ← PTE.PL;

5. Validate Second Level PTE:
- **If** (PTE.PL < access level) **then**
- /* Protection Exception */
— TEAR ← virtual address,
— clock MSR with MSR.TEX = 11,
— terminate translation;
- **If** (PTE.V = 0) **then**
- /* PTE2 Invalid */
— TEAR ← virtual address,
— clock MSR with MSR.TEX = 10,
— terminate translation;
- **If** ((read AND NOT interlocked) AND PTE.R = 0) **then** Read-Modify-Write a double-word interlocked (PTE Pointer).R = 1;
- **If** ((write OR interlocked read) AND (PTE.R = 0 OR PTE.M = 0) **then** Read-Modify-Write a double-word interlocked (PTE Pointer).R = 1, (PTE Pointer).M = 1;

6. Generate Physical address:
- physical address ← PTE.PFN||OFFSET
- CIOUT pin ← PTE.CI

7. Update Translation Buffer:
- Select entry for replacement;
- TLB. Virtual Page Number ← INDEX1|| INDEX2;
- TLB.AS ← AS;
- TLB. Physical Frame Number ← PTE.PFN
- TLB.PL ← Effective PL
- TLB.CI ← PTE.CI
- TLB.M ← (PTE Pointer) .M
- Enable entry

END

Note 1: The TEAR and MSR are only updated when a Trap (ABT) occurs. It is possible that the MMU detects a page fault or protection violation on a reference for an instruction that is not executed, for example on a prefetch. In that event, Trap (ABT) does not occur, and the TEAR and MSR are not updated.

Note 2: If the MMU is translating a virtual address to check protection while executing a RDVAL or WRVAL instruction, then Trap (ABT) occurs only if the level-1 PTE is invalid and the access is permitted by the PL-field.

2.5 INSTRUCTION SET

2.5.1 General Instruction Format

Figure 2-14 shows the general format of a Series 32000 instruction. The Basic Instruction is one to three bytes long and contains the Opcode and up to two 5-bit General Addressing Mode ("Gen") fields. Following the Basic Instruction field is a set of optional extensions, which may appear depending on the instruction and the addressing modes selected.

Index Bytes appear when either or both Gen fields specify Scaled Index. In this case, the Gen field specifies only the Scale Factor (1, 2, 4 or 8), and the Index Byte specifies which General Purpose Register to use as the index, and which addressing mode calculation to perform before indexing. See *Figure 2-15.*

2.0 Architectural Description (Continued)

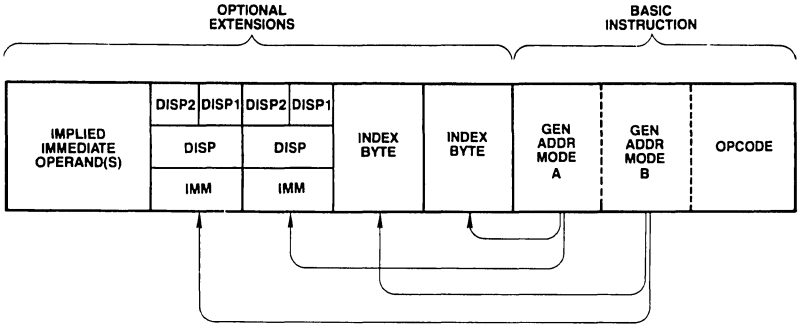

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FIGURE 2-14. General Instruction Format

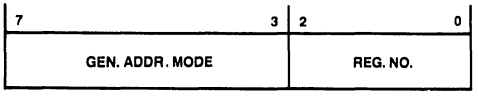

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FIGURE 2-15. Index Byte Format

Following Index Bytes come any displacements (addressing constants) or immediate values associated with the selected addressing modes. Each Disp/Imm field may contain one or two displacements, or one immediate value. The size of a Displacement field is encoded with the top bits of that field, as shown in *Figure 2-16*, with the remaining bits interpreted as a signed (two's complement) value. The size of an immediate value is determined from the Opcode field. Both Displacement and Immediate fields are stored most significant byte first. Note that this is different from the memory representation of data (Section 2.2).

Some instructions require additional, 'implied" immediates and/or displacements, apart from those associated with addressing modes. Any such extensions appear at the end of the instruction, in the order that they appear within the list of operands in the instruction definition (Section 2.5.3).

2.5.2 Addressing Modes

The CPU generally accesses an operand by calculating its Effective Address based on information available when the operand is to be accessed. The method to be used in performing this calculation is specified by the programmer as an "addressing mode."

Addressing modes are designed to optimally support high-level language accesses to variables. In nearly all cases, a variable access requires only one addressing mode, within the instruction that acts upon that variable. Extraneous data movement is therefore minimized.

Addressing Modes fall into nine basic types:

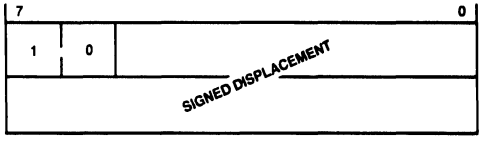
Register: The operand is available in one of the eight General Purpose Registers. In certain Slave Processor instructions, an auxiliary set of eight registers may be referenced instead.

Register Relative: A General Purpose Register contains an address to which is added a displacement value from the instruction, yielding the Effective Address of the operand in memory.

Memory Space: Identical to Register Relative above, except that the register used is one of the dedicated registers PC, SP, SB or FP. These registers point to data areas generally needed by high-level languages.

Byte Displacement: Range −64 to +63

Word Displacement: Range −8192 to +8191



Double Word Displacement: Range $-(2^{29} - 2^{24})$ to $+ (2^{29} - 1)$*

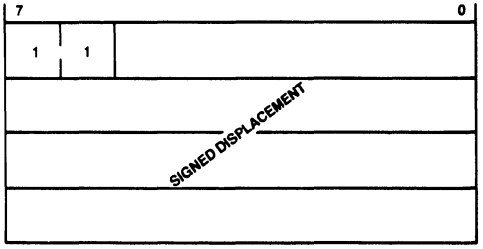


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FIGURE 2-16. Displacement Encodings

***Note:** The pattern "11100000" for the most significant byte of the displacement is reserved by National for future enhancements. Therefore, it should never be used by the user program. This causes the lower limit of the displacement range to be $-(2^{29}-2^{24})$ instead of -2^{29}.

2.0 Architectural Description (Continued)

Memory Relative: A pointer variable is found within the memory space pointed to by the SP, SB or FP register. A displacement is added to that pointer to generate the Effective Address of the operand.

Immediate: The operand is encoded within the instruction. This addressing mode is not allowed if the operand is to be written.

Absolute: The address of the operand is specified by a displacement field in the instruction.

External: A pointer value is read from a specified entry of the current Link Table. To this pointer value is added a displacement, yielding the Effective Address of the operand.

Top of Stack: The currently-selected Stack Pointer (SP0 or SP1) specifies the location of the operand. The operand is pushed or popped, depending on whether it is written or read.

Scaled Index: Although encoded as an addressing mode, Scaled Indexing is an option on any addressing mode except Immediate or another Scaled Index. It has the effect of calculating an Effective Address, then multiplying any General Purpose Register by 1, 2, 4 or 8 and adding it into the total, yielding the final Effective Address of the operand.

Table 2-2 is a brief summary of the addressing modes. For a complete description of their actions, see the Instruction Set Reference Manual.

2.5.3 Instruction Set Summary

Table 2-3 presents a brief description of the NS32532 instruction set. The Format column refers to the Instruction Format tables (Appendix A). The Instruction column gives the instruction as coded in assembly language, and the Description column provides a short description of the function provided by that instruction. Further details of the exact operations performed by each instruction may be found in the Instruction Set Reference Manual.

Notations:

i = Integer length suffix: B = Byte
W = Word
D = Double Word

f = Floating Point length suffix: F = Standard Floating
L = Long Floating

gen = General operand. Any addressing mode can be specified.

short = A 4-bit value encoded within the Basic Instruction (see Appendix A for encodings).

imm = Implied immediate operand. An 8-bit value appended after any addressing extensions.

disp = Displacement (addressing constant): 8, 16 or 32 bits. All three lengths legal.

reg = Any General Purpose Register: R0–R7.

areg = Any Processor Register: Address, Debug, Status, Configuration.

mreg = Any Memory Management Register.

creg = A Custom Slave Processor Register (Implementation Dependent).

cond = Any condition code, encoded as a 4-bit field within the Basic Instruction (see Appendix A for encodings).

2.0 Architectural Description (Continued)

TABLE 2-2. NS32532 Addressing Modes

ENCODING	MODE	ASSEMBLER SYNTAX	EFFECTIVE ADDRESS
Register			
00000	Register 0	R0 or F0	None: Operand is in the specified register.
00001	Register 1	R1 or F1	
00010	Register 2	R2 or F2	
00011	Register 3	R3 or F3	
00100	Register 4	R4 or F4	
00101	Register 5	R5 or F5	
00110	Register 6	R6 or F6	
00111	Register 7	R7 or F7	
Register Relative			
01000	Register 0 relative	disp(R0)	Disp + Register.
01001	Register 1 relative	disp(R1)	
01010	Register 2 relative	disp(R2)	
01011	Register 3 relative	disp(R3)	
01100	Register 4 relative	disp(R4)	
01101	Register 5 relative	disp(R5)	
01110	Register 6 relative	disp(R6)	
01111	Register 7 relative	disp(R7)	
Memory Relative			
10000	Frame memory relative	disp2(disp1(FP))	Disp2 + Pointer; Pointer found at address Disp1 + Register. "SP" is either SP0 or SP1, as selected in PSR.
10001	Stack memory relative	disp2(disp1(SP))	
10010	Static memory relative	disp2(disp1(SB))	
Reserved			
10011	(Reserved for Future Use)		
Immediate			
10100	Immediate	value	None. Operand is input from instruction queue.
Absolute			
10101	Absolute	@disp	Disp.
External			
10110	External	EXT(disp1) + disp2	Disp2 + Pointer; Pointer is found at Link Table Entry number Disp1.
Top of Stack			
10111	Top of stack	TOS	Top of current stack, using either User or Interrupt Stack Pointer, as selected in PSR. Automatic Push/Pop included.
Memory Space			
11000	Frame memory	disp(FP)	Disp + Register; "SP" is either SP0 or SP1, as selected in PSR.
11001	Stack memory	disp(SP)	
11010	Static memory	disp(SB)	
11011	Program memory	* + disp	
Scaled Index			
11100	Index, bytes	mode[Rn:B]	EA (mode) + Rn.
11101	Index, words	mode[Rn:W]	EA (mode) + 2 × Rn.
11110	Index, double words	mode[Rn:D]	EA (mode) + 4 × Rn.
11111	Index, quad words	mode[Rn:Q]	EA (mode) + 8 × Rn. "Mode' and 'n' are contained within the Index Byte. EA (mode) denotes the effective address generated using mode.

2.0 Architectural Description (Continued)

TABLE 2-3. NS32532 Instruction Set Summary

MOVES

Format	Operation	Operands	Description
4	MOVi	gen,gen	Move a value.
2	MOVQi	short,gen	Extend and move a signed 4-bit constant.
7	MOVMi	gen,gen,disp	Move Multiple: disp bytes (1 to 16).
7	MOVZBW	gen,gen	Move with zero extension.
7	MOVZiD	gen,gen	Move with zero extension.
7	MOVXBW	gen,gen	Move with sign extension.
7	MOVXiD	gen,gen	Move with sign extension.
4	ADDR	gen,gen	Move Effective Address.

INTEGER ARITHMETIC

Format	Operation	Operands	Description
4	ADDI	gen,gen	Add.
2	ADDQi	short,gen	Add signed 4-bit constant.
4	ADDCi	gen,gen	Add with carry.
4	SUBi	gen,gen	Subtract.
4	SUBCi	gen,gen	Subtract with carry (borrow).
6	NEGi	gen,gen	Negate (2's complement).
6	ABSi	gen,gen	Take absolute value.
7	MULi	gen,gen	Multiply.
7	QUOi	gen,gen	Divide, rounding toward zero.
7	REMi	gen,gen	Remainder from QUO.
7	DIVi	gen,gen	Divide, rounding down.
7	MODi	gen,gen	Remainder from DIV (Modulus).
7	MEIi	gen,gen	Multiply to Extended Integer.
7	DEIi	gen,gen	Divide Extended Integer.

PACKED DECIMAL (BCD) ARITHMETIC

Format	Operation	Operands	Description
6	ADDPi	gen,gen	Add Packed.
6	SUBPi	gen,gen	Subtract Packed.

INTEGER COMPARISON

Format	Operation	Operands	Description
4	CMPi	gen,gen	Compare.
2	CMPQi	short,gen	Compare to signed 4-bit constant.
7	CMPMi	gen,gen,disp	Compare Multiple: disp bytes (1 to 16).

LOGICAL AND BOOLEAN

Format	Operation	Operands	Description
4	ANDi	gen,gen	Logical AND.
4	ORi	gen,gen	Logical OR.
4	BICi	gen,gen	Clear selected bits.
4	XORi	gen,gen	Logical Exclusive OR.
6	COMi	gen,gen	Complement all bits.
6	NOTi	gen,gen	Boolean complement: LSB only.
2	Scondi	gen	Save condition code (cond) as a Boolean variable of size i.

SHIFTS

Format	Operation	Operands	Description
6	LSHi	gen,gen	Logical Shift, left or right.
6	ASHi	gen,gen	Arithmetic Shift, left or right.
6	ROTi	gen,gen	Rotate, left or right.

2.0 Architectural Description (Continued)

TABLE 2-3. NS32532 Instruction Set Summary (Continued)

BITS

Format	Operation	Operands	Description
4	TBITi	gen,gen	Test bit.
6	SBITi	gen,gen	Test and set bit.
6	SBITIi	gen,gen	Test and set bit, interlocked.
6	CBITi	gen,gen	Test and clear bit.
6	CBITIi	gen,gen	Test and clear bit, interlocked.
6	IBITi	gen,gen	Test and invert bit.
8	FFSi	gen,gen	Find first set bit.

BIT FIELDS

Bit fields are values in memory that are not aligned to byte boundaries. Examples are PACKED arrays and records used in Pascal. "Extract" instructions read and align a bit field. "Insert" instructions write a bit field from an aligned source.

Format	Operation	Operands	Description
8	EXTi	reg,gen,gen,disp	Extract bit field (array oriented).
8	INSi	reg,gen,gen,disp	Insert bit field (array oriented).
7	EXTSi	gen,gen,imm,imm	Extract bit field (short form).
7	INSSi	gen,gen,imm,imm	Insert bit field (short form).
8	CVTP	reg,gen,gen	Convert to Bit Field Pointer.

ARRAYS

Format	Operation	Operands	Description
8	CHECKi	reg,gen,gen	Index bounds check.
8	INDEXi	reg,gen,gen	Recursive indexing step for multiple-dimensional arrays.

STRINGS

String instructions assign specific functions to the General Purpose Registers:
R4 - Comparison Value
R3 - Translation Table Pointer
R2 - String 2 Pointer
R1 - String 1 Pointer
R0 - Limit Count

Options on all string instructions are:

B (Backward): Decrement string pointers after each step rather than incrementing.

U (Until match): End instruction if String 1 entry matches R4.

W (While match): End instruction if String 1 entry does not match R4.

All string instructions end when R0 decrements to zero.

Format	Operation	Operands	Description
5	MOVSi	options	Move String 1 to String 2.
	MOVST	options	Move string, translating bytes.
5	CMPSi	options	Compare String 1 to String 2.
	CMPST	options	Compare translating, String 1 bytes.
5	SKPSi	options	Skip over String 1 entries.
	SKPST	options	Skip, translating bytes for Until/While.

2.0 Architectural Description (Continued)

TABLE 2-3. NS32532 Instruction Set Summary (Continued)

JUMPS AND LINKAGE

Format	Operation	Operands	Description
3	JUMP	gen	Jump.
0	BR	disp	Branch (PC Relative).
0	Bcond	disp	Conditional branch.
3	CASEi	gen	Multiway branch.
2	ACBi	short,gen,disp	Add 4-bit constant and branch if non-zero.
3	JSR	gen	Jump to subroutine.
1	BSR	disp	Branch to subroutine.
1	CXP	disp	Call external procedure.
3	CXPD	gen	Call external procedure using descriptor.
1	SVC		Supervisor Call.
1	FLAG		Flag Trap.
1	BPT		Breakpoint Trap.
1	ENTER	[reg list],disp	Save registers and allocate stack frame (Enter Procedure).
1	EXIT	[reg list]	Restore registers and reclaim stack frame (Exit Procedure).
1	RET	disp	Return from subroutine.
1	RXP	disp	Return from external procedure call.
1	RETT	disp	Return from trap. (Privileged)
1	RETI		Return from interrupt. (Privileged)

CPU REGISTER MANIPULATION

Format	Operation	Operands	Description
1	SAVE	[reg list]	Save General Purpose Registers.
1	RESTORE	[reg list]	Restore General Purpose Registers.
2	LPRi	areg,gen	Load Processor Register. (Privileged if PSR, INTBASE, USP, CFG or Debug Registers).
2	SPRi	areg,gen	Store Processor Register. (Privileged if PSR, INTBASE, USP, CFG or Debug Registers).
3	ADJSPi	gen	Adjust Stack Pointer.
3	BISPSRi	gen	Set selected bits in PSR. (Privileged if not Byte length)
3	BICPSRi	gen	Clear selected bits in PSR. (Privileged if not Byte length)
5	SETCFG	[option list]	Set Configuration Register. (Privileged)

FLOATING POINT

Format	Operation	Operands	Description
11	MOVf	gen,gen	Move a Floating Point value.
9	MOVLF	gen,gen	Move and shorten a Long value to Standard.
9	MOVFL	gen,gen	Move and lengthen a Standard value to Long.
9	MOVfi	gen,gen	Convert any integer to Standard or Long Floating.
9	ROUNDfi	gen,gen	Convert to integer by rounding.
9	TRUNCfi	gen,gen	Convert to integer by truncating, toward zero.
9	FLOORfi	gen,gen	Convert to largest integer less than or equal to value.
11	ADDf	gen,gen	Add.
11	SUBf	gen,gen	Subtract.
11	MULf	gen,gen	Multiply.
11	DIVf	gen,gen	Divide.
11	CMPf	gen,gen	Compare.
11	NEGf	gen,gen	Negate.
11	ABSf	gen,gen	Take absolute value.
9	LFSR	gen	Load FSR.
9	SFSR	gen	Store FSR.

2.0 Architectural Description (Continued)

TABLE 2-3. NS32532 Instruction Set Summary (Continued)

MEMORY MANAGEMENT

Format	Operation	Operands	Description
14	LMR	mreg,gen	Load Memory Management Register. (Privileged)
14	SMR	mreg,gen	Store Memory Management Register. (Privileged)
14	RDVAL	gen	Validate address for reading. (Privileged)
14	WRVAL	gen	Validate address for writing. (Privileged)
8	MOVSUi	gen,gen	Move a value from Supervisor Space to User Space. (Privileged)
8	MOVUSi	gen,gen	Move a value from User Space to Supervisor Space. (Privileged)

MISCELLANEOUS

Format	Operation	Operands	Description
1	NOP		No Operation.
1	WAIT		Wait for interrupt.
1	DIA		Diagnose. Single-byte "Branch to Self" for hardware breakpointing. Not for use in programming.
14	CINV	options,gen	Cache Invalidate. (Privileged)

CUSTOM SLAVE

Format	Operation	Operands	Description
15.5	CCAL0c	gen,gen	Custom Calculate.
15.5	CCAL1c	gen,gen	
15.5	CCAL2c	gen,gen	
15.5	CCAL3c	gen,gen	
15.5	CMOV0c	gen,gen	Custom Move.
15.5	CMOV1c	gen,gen	
15.5	CMOV2c	gen,gen	
15.5	CMOV3c	gen,gen	
15.5	CCMP0c	gen,gen	Custom Compare.
15.5	CCMP1c	gen,gen	
15.1	CCV0ci	gen,gen	Custom Convert.
15.1	CCV1ci	gen,gen	
15.1	CCV2ci	gen,gen	
15.1	CCV3ic	gen,gen	
15.1	CCV4DQ	gen,gen	
15.1	CCV5QD	gen,gen	
15.1	LCSR	gen	Load Custom Status Register.
15.1	SCSR	gen	Store Custom Status Register.
15.0	LCR	creg,gen	Load Custom Register. (Privileged)
15.0	SCR	creg,gen	Store Custom Register. (Privileged)

3.0 Functional Description

This chapter provides details on the functional characteristics of the NS32532 microprocessor.

The chapter is divided into five main sections:

Instruction Execution, Exception Processing, Debugging, On-Chip Caches and System Interface.

3.1 INSTRUCTION EXECUTION

To execute an instruction, the NS32532 performs the following operations:

- Fetch the instruction
- Read source operands, if any (1)
- Calculate results
- Write result operands, if any
- Modify flags, if necessary
- Update the program counter

Under most circumstances, the CPU can be conceived to execute instructions by completing the operations above in strict sequence for one instruction and then beginning the sequence of operations for the next instruction. However, due to the internal instruction pipelining, as well as the occurrence of exceptions, the sequence of operations performed during the execution of an instruction may be altered. Furthermore, exceptions also break the sequentiality of the instructions executed by the CPU.

Details on the effects of the internal pipelining, as well as the occurrence of exceptions on the instruction execution, are provided in the following sections.

Note: 1 In this and following sections, memory locations read by the CPU to calculate effective addresses for Memory-Relative and External addressing modes are considered like source operands, even if the effective address is being calculated for an operand with access class of write.

3.1.1 Operating States

The CPU has five operating states regarding the execution of instructions and the processing of exceptions: Reset, Executing Instructions, Processing An Exception, Waiting-For-An-Interrupt, and Halted. The various states and transitions between them are shown in *Figure 3-1*.

Whenever the $\overline{RST}$ signal is asserted, the CPU enters the reset state. The CPU remains in the reset state until the $\overline{RST}$ signal is driven inactive, at which time it enters the Executing-Instructions state. In the Reset state the contents of certain registers are initialized. Refer to Section 3.5.3 for details.

In the Executing-Instructions state, the CPU executes instructions. It will exit this state when an exception is recognized or a WAIT instruction is encountered. At which time it enters the Processing-An-Exception state or the Waiting-For-An-Interrupt state respectively.

While in the Processing-An-Exception state, the CPU saves the PC, PSR and MOD register contents on the stack and reads the new PC and module linkage information to begin execution of the exception service procedure (see note).

Following the completion of all data references required to process an exception, the CPU enters the Executing-Instructions state.

In the Waiting-For-An-Interrupt state, the CPU is idle. A special status identifying this state is presented on the system interface (Section 3.5). When an interrupt or a debug condition is detected, the CPU enters the Processing-An-Exception state.

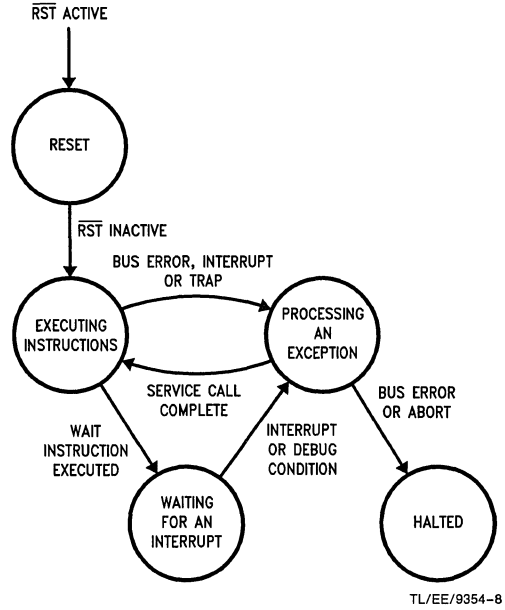

FIGURE 3-1. Operating States

The CPU enters the Halted state when a bus error or abort is detected while the CPU is processing an exception, thereby preventing the transfer of control to an appropriate exception service procedure. The CPU remains in the Halted state until reset occurs. A special status identifying this state is presented on the system interface.

Note: When the Direct-Exception mode is enabled, the CPU does not save the MOD Register contents nor does it read the module linkage information for the exception service procedure. Refer to Section 3.2 for details.

3.1.2 Instruction Endings

The NS32532 checks for exceptions at various points while executing instructions. Certain exceptions, like interrupts, are in most cases recognized between instructions. Other exceptions, like Divide-By-Zero Trap, are recognized during execution of an instruction. When an exception is recognized during execution of an instruction, the instruction ends in one of four possible ways: completed, suspended, terminated, or partially completed. Each type of exception causes a particular ending, as specified in Section 3.2.

3.1.2.1 Completed Instructions

When an exception is recognized after an instruction is completed, the CPU has performed all of the operations for that instruction and for all other instructions executed since the last exception occurred. Result operands have been written, flags have been modified, and the PC saved on the Interrupt Stack contains the address of the next instruction to execute. The exception service procedure can, at its conclusion, execute the RETT instruction (or the RETI instruction for vectored interrupts), and the CPU will begin executing the instruction following the completed instruction.

3.0 Functional Description (Continued)

3.1.2.2 Suspended Instructions

An instruction is suspended when one of several trap conditions or a restartable bus error is detected during execution of the instruction. A suspended instruction has not been completed, but all other instructions executed since the last exception occurred have been completed. Result operands and flags due to be affected by the instruction may have been modified, but only modifications that allow the instruction to be executed again and completed can occur. For certain exceptions (Trap (ABT), Trap (UND), Trap (ILL), and bus errors) the CPU clears the P-flag in the PSR before saving the copy that is pushed on the Interrupt Stack. The PC saved on the Interrupt Stack contains the address of the suspended instruction.

For example, the RESTORE instruction pops up to 8 general-purpose registers from the stack. If an invalid page table entry is detected on one of the references to the stack, then the instruction is suspended. The general-purpose registers due to be loaded by the instruction may have been modified, but the stack pointer still holds the same value that it did when the instruction began.

To complete a suspended instruction, the exception service procedure takes either of two actions:

1. The service procedure can simulate the suspended instruction's execution. After calculating and writing the instruction's results, the flags in the PSR copy saved on the Interrupt Stack should be modified, and the PC saved on the Interrupt Stack should be updated to point to the next instruction to execute. The service procedure can then execute the RETT instruction, and the CPU begins executing the instruction following the suspended instruction. This is the action taken when floating-point instructions are simulated by software in systems without a hardware floating-point unit.
2. The suspended instruction can be executed again after the service procedure has eliminated the trap condition that caused the instruction to be suspended. The service procedure should execute the RETT instruction at its conclusion; then the CPU begins executing the suspended instruction again. This is the action taken by a debugger when it encounters a BPT instruction that was temporarily placed in another instruction's location in order to set a breakpoint.

Note 1: Although the NS32532 allows a suspended instruction to be executed again and completed, the CPU may have read a source operand for the instruction from a memory-mapped peripheral port before the exception was recognized. In such a case, the characteristics of the peripheral device may prevent correct reexecution of the instruction.

Note 2: It may be necessary for the exception service procedure to alter the P-flag in the PSR copy saved on the Interrupt Stack: If the exception service procedure simulates the suspended instruction and the P-flag was cleared by the CPU before saving the PSR copy, then the saved T-flag must be copied to the saved P-flag (like the floating-point instruction simulation described above). Or if the exception service procedure executes the suspended instruction again and the P-flag was not cleared by the CPU before saving the PSR copy, then the saved P-flag must be cleared (like the breakpoint trap described above). Otherwise, no alteration to the saved P-flag is necessary.

3.1.2.3 Terminated Instructions

An instruction being executed is terminated when reset or a nonrestartable bus error occurs. Any result operands and flags due to be affected by the instruction are undefined, as is the contents of the PC. The result operands of other instructions executed since the last serializing operation may not have been written to memory. A terminated instruction cannot be completed.

3.1.2.4 Partially Completed Instructions

When a restartable bus error, interrupt, abort, or debug condition is recognized during execution of a string instruction, the instruction is said to be partially completed. A partially completed instruction has not completed, but all other instructions executed since the last exception occurred have been completed. Result operands and flags due to be affected by the instruction may have been modified, but the values stored in the string pointers and other general-purpose registers used during the instruction's execution allow the instruction to be executed again and completed.

The CPU clears the P-flag in the PSR before saving the copy that is pushed on the Interrupt Stack. The PC saved on the Interrupt Stack contains the address of the partially completed instruction. The exception service procedure can, at its conclusion, simply execute the RETT instruction (or the RETI instruction for vectored interrupts), and the CPU will resume executing the partially completed instruction.

3.1.3 Instruction Pipeline

The NS32532 executes instructions in a heavily pipelined fashion. This allows a significant performance enhancement since the operations of several instructions are performed simultaneously rather than in a strictly sequential manner.

The CPU provides a four-stage internal instruction pipeline. As shown in *Figure 3-2*, a write buffer, that can hold up to two operands, is also provided to allow write operations to be performed off-line.

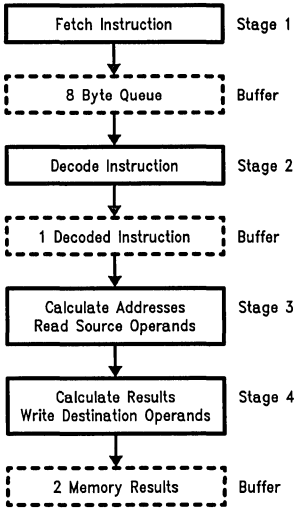

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FIGURE 3-2. NS32532 Internal Instruction Pipeline

Due to the pipelining, operations like fetching one instruction, reading the source operands of a second instruction, calculating the results of a third instruction and storing the results of a fourth instruction, can all occur in parallel.

3.0 Functional Description (Continued)

The order of memory references performed by the CPU may also differ from that related to a strictly sequential instruction execution. In fact, when an instruction is being executed, some of the source operands may be read from memory before the instruction is completely fetched. For example, the CPU may read the first source operand for an instruction before it has fetched a displacement used in calculating the address of the second source operand. The CPU, however, always completes fetching an instruction and reading its source operands before writing its results. When more than one source operand must be read from memory to execute an instruction, the operands may be read in any order. Similarly, when more than one result operand is written to memory to execute an instruction, the operands may be written in any order.

An instruction is fetched only after all previous instructions have been completely fetched. However, the CPU may begin fetching an instruction before all of the source operands have been read and results written for previous instructions.

The source operands for an instruction are read only after all previous instructions have been fetched and their source operands read. A source operand for an instruction may be read before all results of previous instructions have been written, except when the source operand's value depends on a result not yet written. The CPU compares the physical address and length of a source operand with those of any results not yet written, and delays reading the source operand until after writing all results on which the source operand depends. Also, the CPU ensures that the interlocked read and write references to execute an SBITIi or CBITIi instruction occur after writing all results of previous instructions and before reading any source operands for subsequent instructions.

The result operands for an instruction are written after all results of previous instructions have been written.

The description above is summarized in *Figure 3-3*, which shows the precedence of memory references for two consecutive instructions.

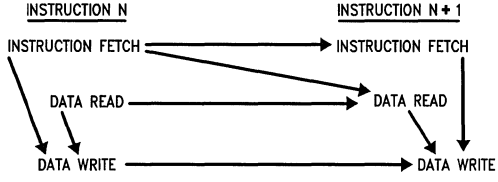

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FIGURE 3-3. Memory References for Consecutive Instructions (An arrow from one reference to another indicates that the first reference always precedes the second.)

Another consequence of overlapping the operations for several instructions, is that the CPU may fetch an instruction and read its source operands, even though the instruction is not executed (e.g., due to the occurrence of an exception). In such a case, the MMU may update the R-bit in Page Table Entries used in referring to the fetched instruction and its source operands.

Special care is needed in the handling of memory-mapped I/O devices. The CPU provides special mechanisms to ensure that the references to these devices are always performed in the order implied by the program. Refer to Section 3.1.3.2 for details.

It is also to be noted that the CPU does not check for dependencies between the fetching of an instruction and the writing of previous instructions' results. Therefore, special care is required when executing self-modifying code.

3.1.3.1 Branch Prediction

One problem inherent to all pipelined machines is what is called "Pipeline Breakage".

This occurs every time the sequentiality of the instructions is broken, due to the execution of certain instructions or the occurrence of exceptions.

The result of a pipeline breakage is a performance degradation, due to the fact that a certain portion of the pipeline must be flushed and new data must be brought in.

The NS32532 provides a special mechanism, called branch prediction, that helps minimize this performance penalty.

When a conditional branch instruction is decoded in the early stages of the pipeline, a prediction on the execution of the instruction is performed.

More precisely, the prediction mechanism predicts backward branches as taken and forward branches as not taken, except for the branch instructions BLE and BNE that are always predicted as taken.

Thus, the resulting probability of correct prediction is fairly high, especially for branch instructions placed at the end of loops.

The sequence of operations performed by the loader and execution units in the CPU is given below:

- Loader detects branches and calculates destination addresses
- Loader uses branch opcode and direction to select between sequential and non-sequential streams
- Loader saves address for alternate stream
- Execution unit resolves branch decision

Due to the branch predicition, some special care is required when writing self-modifying code. Refer to the appropriate section in Appendix B for more information on this subject.

3.1.3.2 Memory-Mapped I/O

The characteristics of certain peripheral devices and the overlapping of instruction execution in the pipeline of the NS32532 require that special handling be applied to memory-mapped I/O references. I/O references differ from memory references in two significant ways, imposing the following requirements:

1. Reading from a peripheral port can alter the value read on the next reference to the same port or another port in the same device. (A characteristic called here "destructive-reading".) Serial communication controllers and FIFO buffers commonly operate in this manner. As explained in "Instruction Pipeline" above, the NS32532 can read the source operands for one instruction while the previous instruction is executing. Because the previous instruction may cause a trap, an interrupt may be recognized, or the flow of control may be otherwise altered, it is a requirement that destructive-reading of source operands before the execution of an instruction be avoided.

3.0 Functional Description (Continued)

2. Writing to a peripheral port can alter the value read from another port of the same device. (A characteristic called here "side-effects of writing"). For example, before reading the counter's value from the NS32202 Interrupt Control Unit it is first necessary to freeze the value by writing to another control register.

However, as mentioned above, the NS32532 can read the source operands for one instruction before writing the results of previous instructions unless the addresses indicate a dependency between the read and write references. Consequently, it is a requirement that read and write references to peripheral that exhibit side-effects of writing must occur in the order dictated by the instructions.

The NS32532 supports 2 methods for handling memory-mapped I/O. The first method is more general; it satisfies both requirements listed above and places no restriction on the location of memory-mapped peripheral devices. The second method satisfies only the requirement for side effects of writing, and it restricts the location of memory-mapped I/O devices, but it is more efficient for devices that do not have destructive-read ports.

The first method for handling memory-mapped I/O uses two signals: $\overline{\text{IOINH}}$ and $\overline{\text{IODEC}}$. When the NS32532 generates a read bus cycle, it asserts the output signal $\overline{\text{IOINH}}$ if either of the I/O requirements listed above is not satisfied. That is, $\overline{\text{IOINH}}$ is asserted during a read bus cycle when (1) the read reference is for an instruction that may not be executed or (2) the read reference occurs while a write reference is pending for a previous instruction. When the read reference is to a peripheral device that implements ports with destructive-reading or side-effects of writing, the input signal $\overline{\text{IODEC}}$ must be asserted; in addition, the device must not be selected if $\overline{\text{IOINH}}$ is active. When the CPU detects that the $\overline{\text{IODEC}}$ input signal is active while the $\overline{\text{IOINH}}$ output signal is also active, it discards the data read during the bus cycle and serializes instruction execution. See the next section for details on serializing operations. The CPU then generates the read bus cycle again, this time satisfying the requirements for I/O and driving $\overline{\text{IOINH}}$ inactive.

The second method for handling memory-mapped I/O uses a dedicated region of virtual memory. The NS32532 treats all references to the memory range from address FF000000 to address FFFFFFFF inclusive in a special manner.

While a write to a location in this range is pending, reads from locations in the same range are delayed. However, reads from locations with addresses lower than FF000000 may occur. Similarly, reads from locations in the above range may occur while writes to locations outside of the range are pending.

It is to be noted that the CPU may assert $\overline{\text{IOINH}}$ even when the reference is within the dedicated region. Refer to Section 3.5.8 for more information on the handling of I/O devices.

3.1.3.3 Serializing Operations

After executing certain instructions or processing an exception, the CPU serializes instruction execution. Serializing instruction execution means that the CPU completes writing all previous instructions' results to memory, then begins fetching and executing the next instruction.

For example, when a new value is loaded into the PSR by executing an LPRW instruction, the pipeline is flushed and a serializing operation takes place. This is necessary since the privilege level might have changed and the instructions following the LPRW instruction must be fetched again with the new privilege level and possibly with a different MMU mapping. See Section 2.4.2.

The CPU serializes instruction execution after executing one of the following instructions: BICPSRW, BISPSRW, BPT, CINV, DIA, FLAG (trap taken), LMR, LPR (CFG, INTBASE, PSR, UPSR, DCR, BPC, DSR, and CAR only), RETT, RETI, and SVC. *Figure 3-4* shows the memory references after serialization.

Note 1: LPRB UPSR can be executed in User Mode to serialize instruction execution.

Note 2: After an instruction that writes a result to memory is executed, the updating of the result's memory location may be delayed until the next serializing operation.

Note 3: When reset or a nonrestartable bus error exception occurs, the CPU discards any results that have not yet been written to memory.

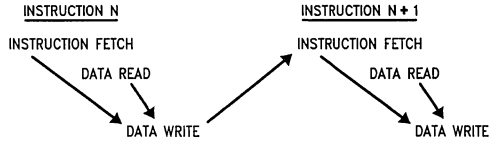

FIGURE 3-4. Memory References after Serialization

3.1.4 Slave Processor Instructions

The NS32532 recognizes two groups of instructions being executable by external slave processors:

- Floating Point Instructions
- Custom Slave Instructions

Each Slave Instruction Set is enabled by a bit in the Configuration Register (Section 2.1.4). Any Slave Instruction which does not have its corresponding Configuration Register bit set will trap as undefined, without any Slave Processor communication attempted by the CPU. This allows software simulation of a non-existent Slave Processor.

Note that the Memory Management Instructions, like Floating Point and Custom Slave Instructions, have to be enabled through an appropriate bit in the configuration register in order to be executable.

However, they are not considered here as Slave Instructions, since the NS32532 integrates the MMU on-chip and the execution of them does not follow the protocol of the Slave Instructions.

3.1.4.1 Regular Slave Instruction Protocol

Slave Processor instructions have a three-byte Basic Instruction field, consisting of an ID Byte followed by an Operation Word. The ID Byte has three functions:

1) It identifies the instruction as being a Slave Processor instruction.
2) It specifies which Slave Processor will execute it.
3) It determines the format of the following Operation Word of the instruction.

Upon receiving a Slave Processor instruction, the CPU initiates the sequence outlined in *Figure 3-5*. While applying Status code 11111 (Broadcast ID Section 3.5.4.1), the CPU transfers the ID Byte on bits AD24–AD31, the operation

3.0 Functional Description (Continued)

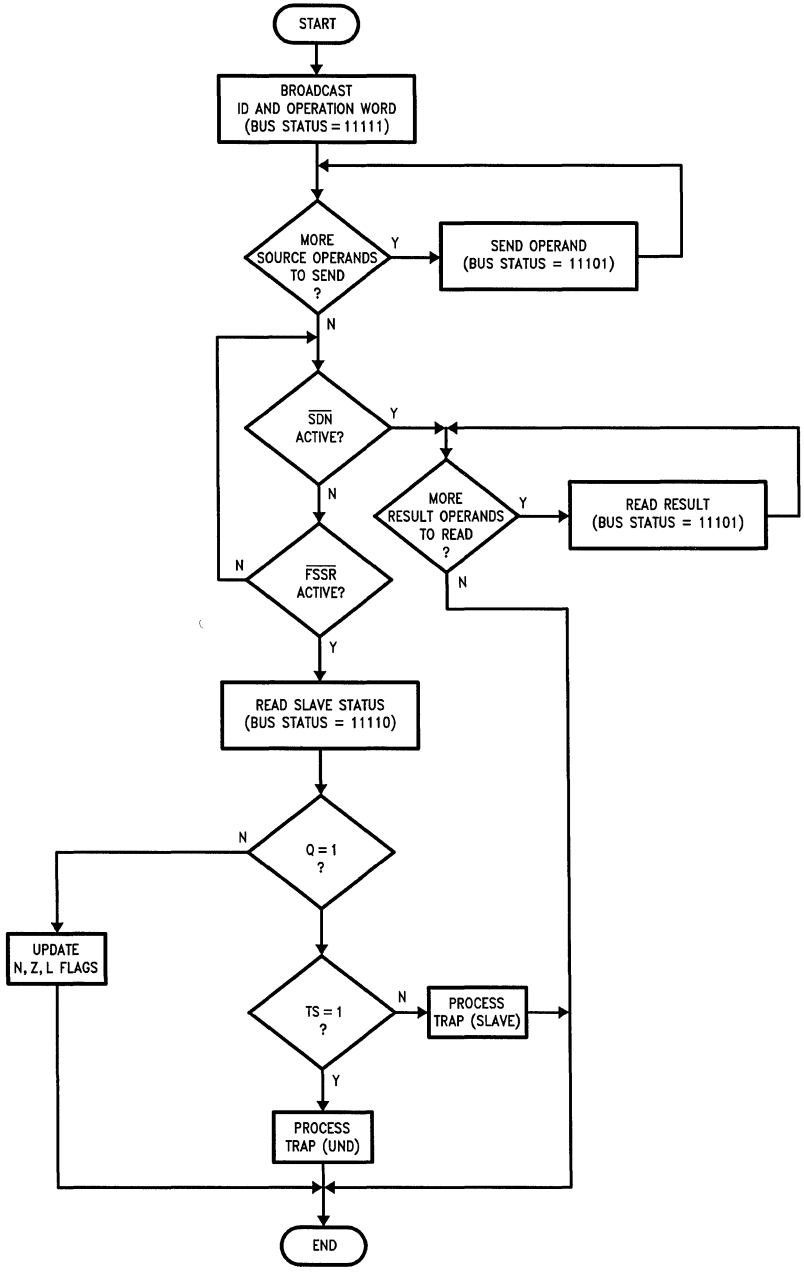

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FIGURE 3-5. Regular Slave Instruction Protocol: CPU Actions

3.0 Functional Description (Continued)

31			0
ID BYTE	OPCODE (LOW)	OPCODE (HIGH)	XXXXXXXX

FIGURE 3-6. ID and Operation Word

31		15		7							0
I	ZERO	TS	ZERO	N	Z	0	0	0	L	0	Q

FIGURE 3-7. Slave Processor Status Word

word on bits AD8–AD23 in a swapped order of bytes and a non-used byte XXXXXXXX (X = don't care) on bits AD0–AD7 (*Figure 3-6*).

All slave processors observe the bus cycle and inspect the identification code. The slave selected by the identification code continues with the protocol; other slaves wait for the next slave instruction to be broadcast.

After transferring the slave instruction, the CPU sends to the slave any source operands that are located in memory or the General-Purpose registers. The CPU then waits for the slave to assert $\overline{SDN}$ or $\overline{FSSR}$. While the CPU is waiting, it can perform bus cycles to fetch instructions and read source operands for instructions that follow the slave instruction being executed. If there are no bus cycles to perform, the CPU is idle with a special Status indicating that it is waiting for a slave processor. After the slave asserts $\overline{SDN}$ or $\overline{FSSR}$, the CPU follows one of the two sequences described below.

If the slave asserts $\overline{SDN}$, then the CPU checks whether the instruction stores any results to memory or the General-Purpose registers. The CPU reads any such results from the slave by means of 1 or 2 bus cycles and updates the destination.

If the slave asserts $\overline{FSSR}$, then the NS32532 reads a 32-bit status word from the slave. The CPU checks bit 0 in the slave's status word to determine whether to update the PSR flags or to process an exception. *Figure 3-7* shows the format of the slave's status word.

If the Q bit in the status word is 0, the CPU updates the N, Z and L flags in the PSR.

If the Q bit in the status word is set to 1, the CPU processes either a Trap (UND) if TS is 1 or a Trap (SLAVE) if TS is 0.

Note 1: Only the floating-point and custom compare instructions are allowed to return a value of 0 for the Q bit when the $\overline{FSSR}$ signal is activated. All other instructions must always set the Q bit to 1 (to signal a Trap), when activating $\overline{FSSR}$.

Note 2: While executing an LMR or CINV instruction, the CPU displays the operation code and source operand using slave processor write bus cycles, as described in the protocol above. Nevertheless, the CPU does not wait for $\overline{SDN}$ or $\overline{FSSR}$ to be asserted while executing these instructions. This information can be used to monitor the contents of the on-chip TLB, Instruction Cache, and Data Cache.

Note 3: The slave processor must be ready to accept new slave instruction at any time, even while the slave is executing another instruction or waiting for the CPU to read results. For example, the CPU may terminate an instruction being executed by a slave because a non-restartable bus error is detected while the MMU is updating a Page Table Entry for an instruction being prefetched.

Note 4: If a slave instruction stores a result to memory, the CPU checks whether Trap (ABT) would occur on the store operation before reading the result from the slave. For quad-word destination operands, the CPU checks that both double-words of the destination can be stored without an abort before reading either double-word of the result from the slave.

3.1.4.2 Pipelined Slave Instruction Protocol

In order to increase performance of floating-point instructions while maintaining full software compatibility with the Series 32000 architecture, the NS32532 incorporates a pipelined floating-point protocol. This protocol is designed to operate in conjunction with the NS32580 FPC, or any other floating-point slave which conforms to the protocol and the Series 32000 architecture. The protocol is enabled by the PF bit in the CFG register.

The basic methods of transferring data and control information between the CPU and the FPC, are the same as in the regular slave protocol.

However, in pipelined mode, the CPU may send a new floating-point instruction to the FPC before the previous instruction has been completed.

Although the CPU can advance as many as four floating-point instructions before receiving a completion pulse on $\overline{SDN}$ for the first instruction, full exception recovery is assured. This is accomplished through a FIFO mechanism which maintains the addresses of all the floating-point instructions sent to the FPC for execution.

Pipelined execution can occur only for instructions which do not require a result to be read from the FPC.

In cases where a result is to be read back, the CPU will wait for instruction completion before issuing the next instruction. Instructions can be divided into three groups, depending on the amount of pipelining permitted.

Group A. Fully-Pipelined Instructions

Instructions in this group can be sent to the FPC before previous group A instructions are completed. No instruction completion indication from the FPC is required in order to continue to another group A or group B instruction.

Group A contains floating-point instructions satisfying all of the following conditions.

1. The destination operand is in a floating-point register.
2. The source operand is not of type TOS or IMM.
3. The instruction format is either 11 or 12.

Group B. Half-Pipelined Instructions

Group B instructions can begin execution before previous group A instructions are completed. However, they cannot complete before the FPC signals completion of all the previous floating-point instructions.

Group B contains floating-point instructions satisfying at least one of the following conditions.

1. The destination operand is either in memory or in a CPU register (this includes the CMPf instruction which modifies the PSR register).
2. The source operand is of type TOS or IMM.
3. The instruction format is 9.

3.0 Functional Description (Continued)

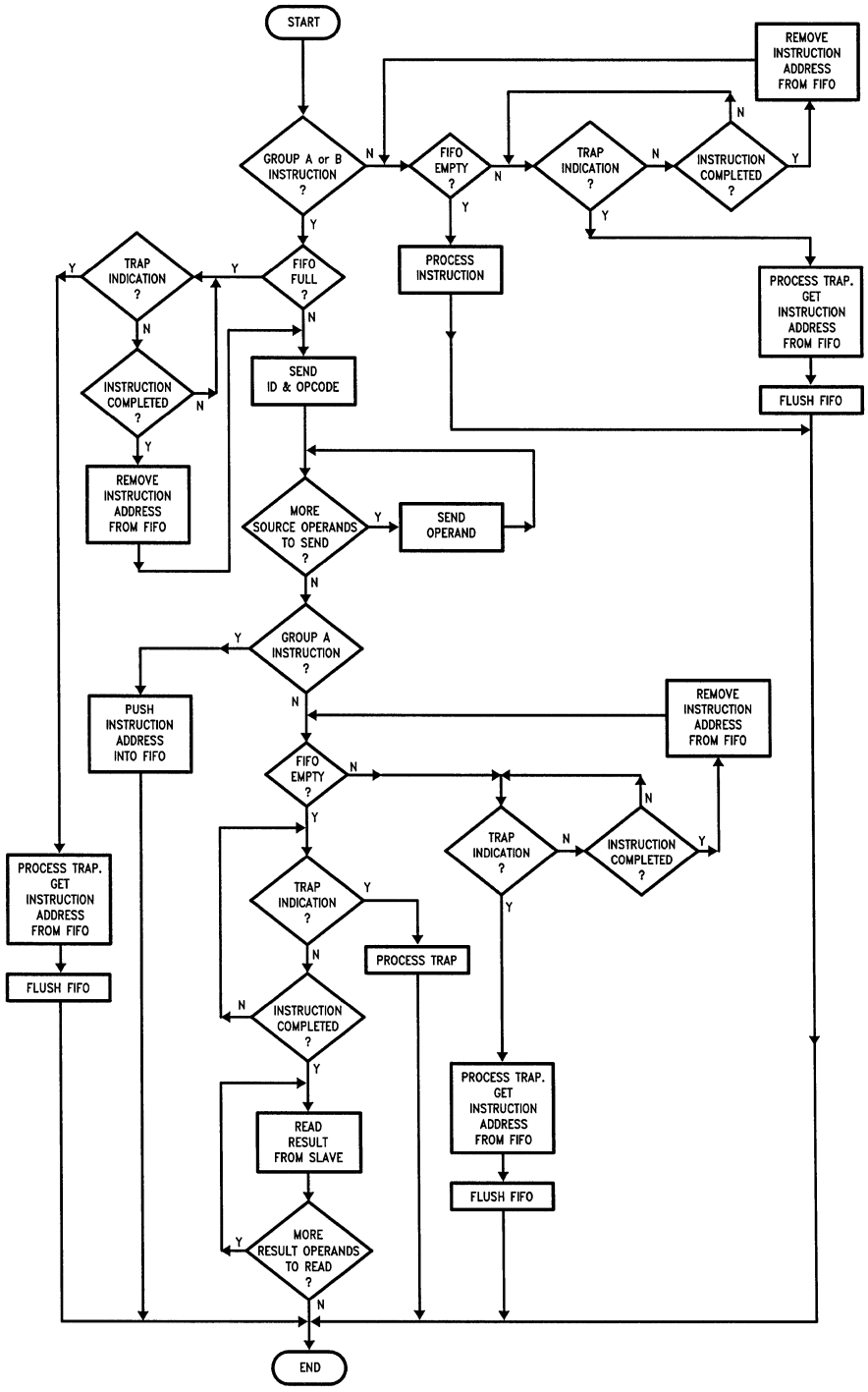

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FIGURE 3-8. Instruction Flow in Pipelined Floating-Point Mode

3.0 Functional Description (Continued)

Group C. Non-Pipelined Instructions

Group C instructions can begin execution only after all other instructions have been completed. The CPU cannot proceed to other instructions before their execution is completed.

Group C contains all the floating-point/integer conversion instructions.

3.1.4.3 Instruction Flow and Exceptions

When operating in pipelined mode, the CPU will push the address of group A instructions into a five-entry FIFO after the ID, opcode and source operands have been sent to the FPC. The address will be pushed into the FIFO only if no exception is detected during the transfer of the source operands needed for the execution of the instruction.

Group A instructions are only stalled when the FIFO is full, in which case the CPU will wait before sending the next instruction. Group B instructions can begin execution while some entries are still in the FIFO, but cannot complete before the FIFO is empty (i.e., before all previous instructions are completed). Group C instructions cannot begin execution until the FIFO is empty. When a normal completion indication is received, the instruction address at the bottom of the FIFO is dropped. If a trap indication is received and the FIFO is not empty, the instruction address at the bottom of the FIFO is copied to the PC register and the floating-point exception is serviced. The remaining entries in the FIFO are discarded.

A floating-point exception may be received and serviced at any time after the CPU has sent the ID and opcode for the first instruction and until the FPC has signalled completion for the last instruction.

Other exceptions may occur while the FIFO is not empty. This may be the case when an interrupt is received or a translation exception is detected in the access of an operand needed for the execution of the next floating-point instruction. These exceptions will be processed as soon as the FIFO becomes empty, and after any floating-point exception has been acknowledged.

In the event of a non-restartable bus error, the acknowledge will occur immediately. The CPU will flush the internal FIFO and will reset the FPC by performing a dummy read of the slave status word. This operation is performed for both the regular and pipelined floating-point protocol and regardless of whether any floating-point instruction is pending in the FPC instruction queue.

The CPU may cancel the last instruction sent to the FPC by sending another ID and opcode, before the last source operand for that instruction has been sent. *Figure 3-8* shows the instruction flow in pipelined floating-point mode.

3.1.4.4 Floating Point Instructions

Table 3-1 gives the protocols followed for each Floating Point instruction. The instructions are referenced by their mnemonics. For the bit encodings of each instruction, see Appendix A.

The Operand class columns give the Access Class for each general operand, defining how the addressing modes are interpreted (see Instruction Set Reference Manual).

The Operand Issued columns show the sizes of the operands issued to the Floating Point Unit by the CPU. "D" indicates a 32-bit Double Word. "i" indicates that the instruction specifies an integer size for the operand (B = Byte, W = Word, D = Double Word). "f" indicates that the instruction specifies a Floating Point size for the operand (F = 32-bit Standard Floating, L = 64-bit Long Floating).

The Returned Value Type and Destination column gives the size of any returned value and where the CPU places it. The PSR-Bits-Affected column indicates which PSR bits, if any, are updated from the Slave Processor Status Word *(Figure 3-7)*.

Any operand indicated as being of type "f" will not cause a transfer if the Register addressing mode is specified. This is because the Floating Point Registers are physically on the Floating Point Unit and are therefore available without CPU assistance.

3.1.4.5 Custom Slave Instructions

Provided in the NS32532 is the capability of communicating with a user-defined, "Custom" Slave Processor. The instruction set provided for a Custom Slave Processor defines the instruction formats, the operand classes and the communication protocol. Left to the user are the interpretations of the Op Code fields, the programming model of the Custom Slave and the actual types of data transferred. The protocol specifies only the size of an operand, not its data type.

Table 3-2 lists the relevant information for the Custom Slave instruction set. The designation "c" is used to represent an operand which can be a 32-bit ("D") or 64-bit ("Q") quantity in any format; the size is determined by the suffix on the mnemonic. Similarly, an "i" indicates an integer size (Byte, Word, Double Word) selected by the corresponding mnemonic suffix.

Any operand indicated as being of type "c" will not cause a transfer if the register addressing mode is specified. It is assumed in this case that the slave processor is already holding the operand internally.

For the instruction encodings, see Appendix A.

3.2 EXCEPTION PROCESSING

Exceptions are special events that alter the sequence of instruction execution. The CPU recognizes three basic types of exceptions: interrupts, traps and bus errors.

An interrupt occurs in response to an event signalled by activating the $\overline{\text{NMI}}$ or $\overline{\text{INT}}$ input signals. Interrupts are typically requested by peripheral devices that require the CPU's attention.

Traps occur as a result either of exceptional conditions (e.g., attempted division by zero) or of specific instructions whose purpose is to cause a trap to occur (e.g., supervisor call instruction).

A bus error exception occurs when the $\overline{\text{BER}}$ signal is activated during an instruction fetch or data transfer required by the CPU to execute an instruction.

When an exception is recognized, the CPU saves the PC, PSR and optionally the MOD register contents on the interrupt stack and then it transfers control to an exception service procedure.

Details on the operations performed in the various cases by the CPU to enter and exit the exception service procedure are given in the following sections.

It is to be noted that the reset operation is not treated here as an exception. Even though, like any exception, it alters the instruction execution sequence.

The reason being that the CPU handles reset in a significantly different way than it does for exceptions.

Refer to Section 3.5.3 for details on the reset operation.

3.0 Functional Description (Continued)

TABLE 3-1. Floating Point Instruction Protocols

Mnemonic	Operand 1 Class	Operand 2 Class	Operand 1 Issued	Operand 2 Issued	Returned Value Type and Dest.	PSR Bits Affected
ADDf	read.f	rmw.f	f	f	f to Op.2	none
SUBf	read.f	rmw.f	f	f	f to Op.2	none
MULf	read.f	rmw.f	f	f	f to Op.2	none
DIVf	read.f	rmw.f	f	f	f to Op.2	none
MOVf	read.f	write.f	f	N/A	f to Op.2	none
ABSf	read.f	write.f	f	N/A	f to Op.2	none
NEGf	read.f	write.f	f	N/A	f to Op.2	none
CMPf	read.f	read.f	f	f	N/A	N, Z, L
FLOORfi	read.f	write.i	f	N/A	i to Op.2	none
TRUNCfi	read.f	write.i	f	N/A	i to Op.2	none
ROUNDfi	read.f	write.i	f	N/A	i to Op.2	none
MOVFL	read.F	write.L	F	N/A	L to Op.2	none
MOVLF	read.L	write.F	L	N/A	F to Op.2	none
MOVif	read.i	write.f	i	N/A	f to Op.2	none
LFSR	read.D	N/A	D	N/A	N/A	none
SFSR	N/A	write.D	N/A	N/A	D to Op.2	none

TABLE 3-2. Custom Slave Instruction Protocols

Mnemonic	Operand 1 Class	Operand 2 Class	Operand 1 Issued	Operand 2 Issued	Returned Value Type and Dest.	PSR Bits Affected
CCAL0c	read.c	rmw.c	c	c	c to Op.2	none
CCAL1c	read.c	rmw.c	c	c	c to Op.2	none
CCAL2c	read.c	rmw.c	c	c	c to Op.2	none
CCAL3c	read.c	rmw.c	c	c	c to Op.2	none
CMOV0c	read.c	write.c	c	N/A	c to Op.2	none
CMOV1c	read.c	write.c	c	N/A	c to Op.2	none
CMOV2c	read.c	write.c	c	N/A	c to Op.2	none
CMOV3c	read.c	write.c	c	N/A	c to Op.2	none
CCMP0c	read.c	read.c	c	c	N/A	N,Z,L
CCMP1c	read.c	read.c	c	c	N/A	N,Z,L
CCV0ci	read.c	write.i	c	N/A	i to Op.2	none
CCV1ci	read.c	write.i	c	N/A	i to Op.2	none
CCV2ci	read.c	write.i	c	N/A	i to Op.2	none
CCV3ic	read.i	write.c	i	N/A	c to Op.2	none
CCV4DQ	read.D	write.Q	D	N/A	Q to Op.2	none
CCV5QD	read.Q	write.D	Q	N/A	D to Op.2	none
LCSR	read.D	N/A	D	N/A	N/A	none
SCSR	N/A	write.D	N/A	N/A	D to Op.2	none
LCR*	read.D	N/A	D	N/A	N/A	none
SCR*	write.D	N/A	N/A	N/A	D to Op.1	none

Note:
D = Double Word
i = Integer size (B,W,D) specified in mnemonic.
c = Custom size (D:32 bits or Q:64 bits) specified in mnemonic.
* = Privileged instruction: will trap if CPU is in User Mode.
N/A = Not Applicable to this instruction.

3.0 Functional Description (Continued)

3.2.1 Exception Acknowledge Sequence

When an exception is recognized, the CPU goes through three major steps:

1) Adjustment of Registers. Depending on the source of the exception, the CPU may restore and/or adjust the contents of the Program Counter (PC), the Processor Status Register (PSR) and the currently-selected Stack Pointer (SP). A copy of the PSR is made, and the PSR is then set to reflect Supervisor Mode and selection of the Interrupt Stack. Trap (TRC) and Trap (OVF) are always disabled. Maskable interrupts are also disabled if the exception is caused by an interrupt, Trap (DBG), Trap (ABT) or bus error.
2) Vector Acquisition. A vector is either obtained from the data bus or is supplied internally by default.
3) Service Call. The CPU performs one of two sequences common to all exceptions to complete the acknowledge process and enter the appropriate service procedure. The selection between the two sequences depends on whether the Direct-Exception mode is disabled or enabled.

Direct-Exception Mode Disabled

The Direct-Exception mode is disabled while the DE bit in the CFG register is 0 (Section 2.1.4). In this case the CPU first pushes the saved PSR copy along with the contents of the MOD and PC registers on the interrupt stack. Then it reads the double-word entry from the Interrupt Dispatch table at address 'INTBASE + vector × 4'. See *Figures 3-9* and *3-10*. The CPU uses this entry to call the exception service procedure, interpreting the entry as an external procedure descriptor.

A new module number is loaded into the MOD register from the least-significant word of the descriptor, and the static-base pointer for the new module is read from memory and loaded into the SB register. Then the program-base pointer for the new module is read from memory and added to the most-significant word of the module descriptor, which is interpreted as an unsigned value. Finally, the result is loaded into the PC register.

Direct-Exception Mode Enabled

The Direct-Exception mode is enabled when the DE bit in the CFG register is set to 1. In this case the CPU first pushes the saved PSR copy along with the contents of the PC register on the Interrupt Stack. The word stored on the Interrupt Stack between the saved PSR and PC register is reserved for future use; its contents are undefined. The CPU then reads the double-word entry from the Interrupt Dispatch Table at address 'INTBASE + vector × 4'. The CPU uses this entry to call the exception service procedure, interpreting the entry as an absolute address that is simply loaded into the PC register. *Figure 3-11* provides a pictorial of the acknowledge sequence. It is to be noted that while the

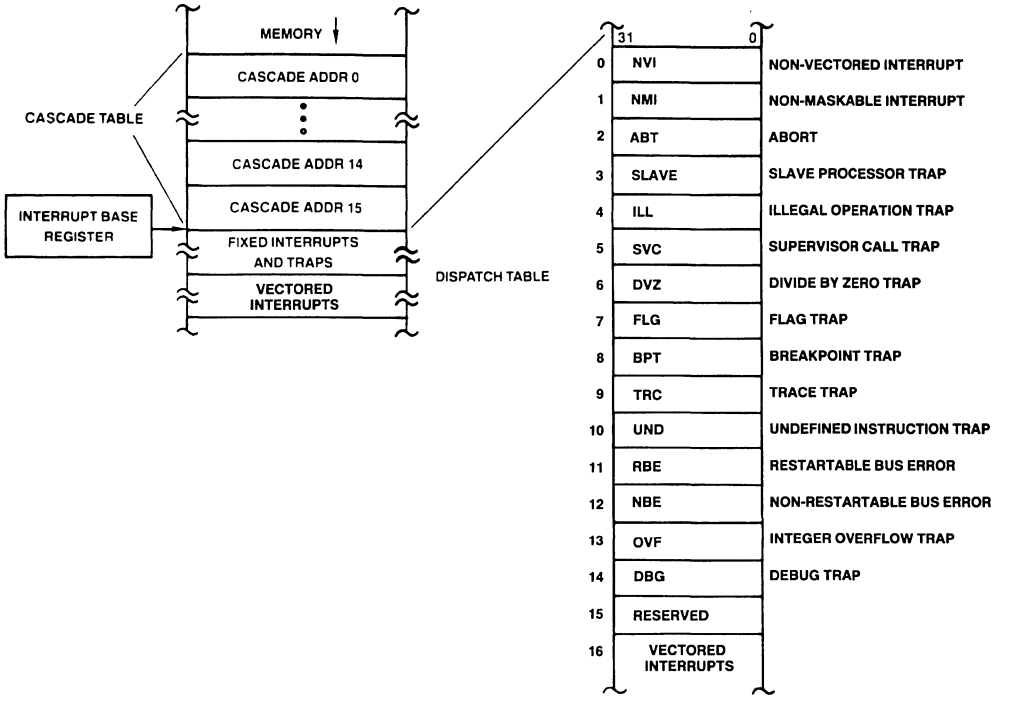

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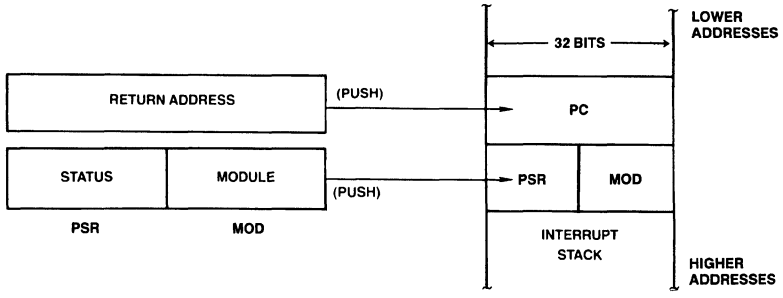
FIGURE 3-9. Interrupt Dispatch Table

3.0 Functional Description (Continued)



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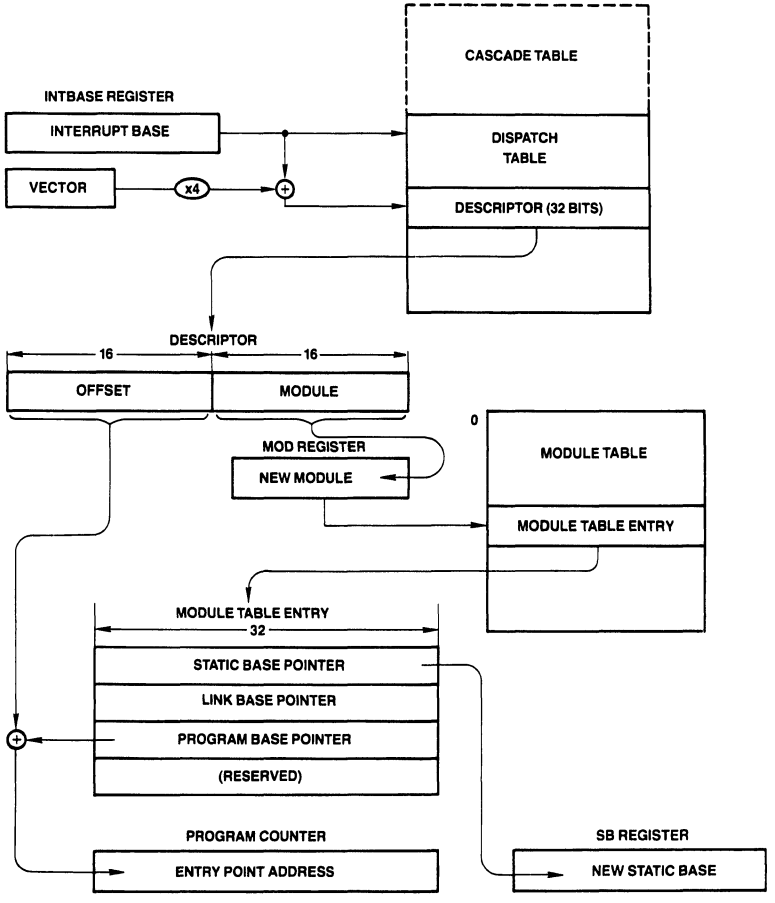

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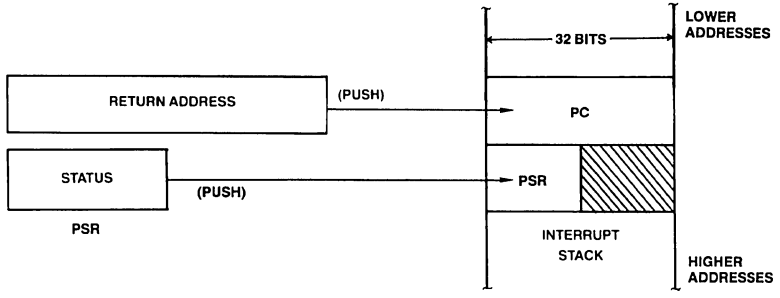
FIGURE 3-10. Exception Acknowledge Sequence. Direct-Exception Mode Disabled.

3.0 Functional Description (Continued)



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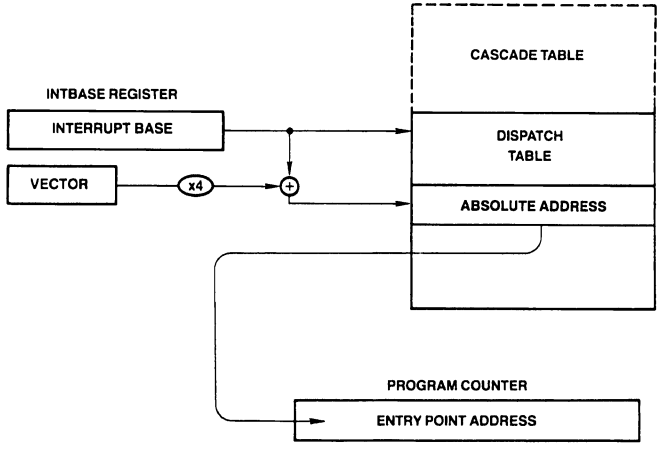

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FIGURE 3-11. Exception Acknowledge Sequence. Direct-Exception Mode Enabled.

direct-exception mode is enabled, the CPU can respond more quickly to interrupts and other exceptions because fewer memory references are required to process an exception. The MOD and SB registers, however, are not initialized before the CPU transfers control to the service procedure. Consequently, the service procedure is restricted from executing any instructions, such as CXP, that use the contents of the MOD or SB registers in effective address calculations.

3.2.2 Returning from an Exception Service Procedure

To return control to an interrupted program, one of two instructions can be used: RETT (Return from Trap) and RETI (Return from Interrupt).

RETT is used to return from any trap, non-maskable interrupt or bus error service procedure. Since some traps are often used deliberately as a call mechanism for supervisor mode procedures, RETT can also adjust the Stack Pointer (SP) to discard a specified number of bytes from the original stack as surplus parameter space.

RETI is used to return from a maskable interrupt service procedure. A difference of RETT, RETI also informs any external interrupt control units that interrupt service has completed. Since interrupts are generally asynchronous external events, RETI does not discard parameters from the stack.

Both of the above instructions always restore the Program Counter (PC) and the Processor Status Register from the interrupt stack. If the Direct-Exception mode is disabled, they also restore the MOD and SB register contents. *Figures 3-12* and *3-13* show the RETT and RETI instruction flows when the Direct-Exception mode is disabled.

3.0 Functional Description (Continued)

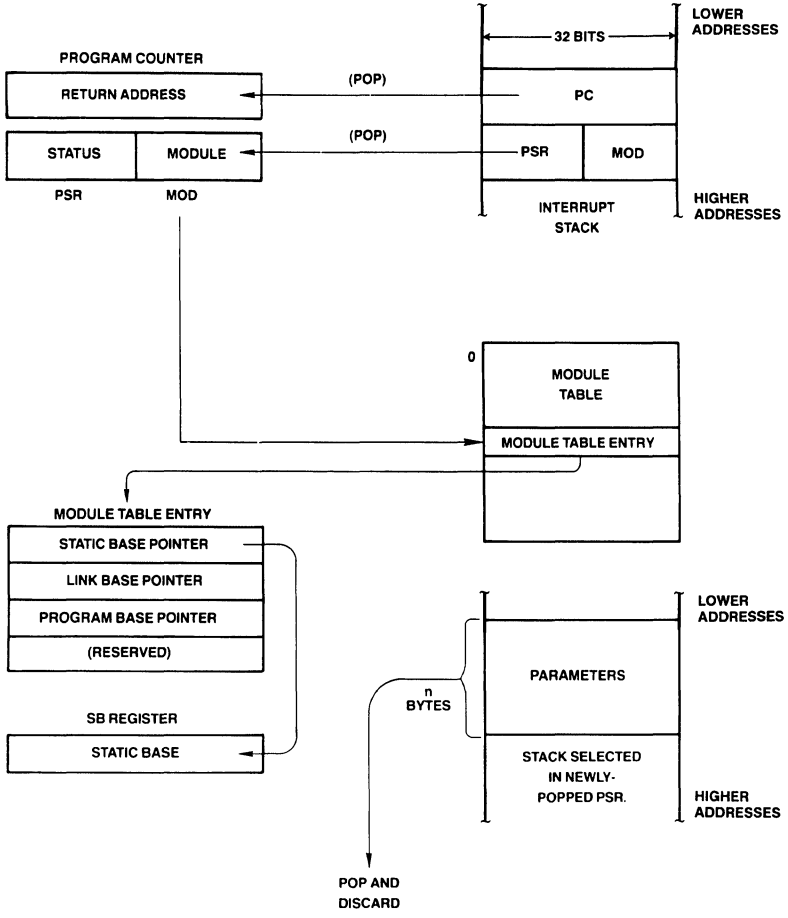

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FIGURE 3-12. Return from Trap (RETT n) Instruction Flow. Direct-Exception Mode Disabled.

3.2.3 Maskable Interrupts

The $\overline{INT}$ pin is a level-sensitive input. A continuous low level is allowed for generating multiple interrupt requests. The input is maskable, and is therefore enabled to generate interrupt requests only while the Processor Status Register I bit is set. The I bit is automatically cleared during service of an $\overline{INT}$, $\overline{NMI}$, Trap (DBG), Trap (ABT) or Bus Error request, and is restored to its original setting upon return from the interrupt service routine via the RETT or RETI instruction.

The $\overline{INT}$ pin may be configured via the SETCFG instruction as either Non-Vectored (CFG Register bit I = 0) or Vectored (bit I = 1).

3.2.3.1 Non-Vectored Mode

In the Non-Vectored mode, an interrupt request on the $\overline{INT}$ pin will cause an Interrupt Acknowledge bus cycle, but the CPU will ignore any value read from the bus and use instead a default vector of zero. This mode is useful for small systems in which hardware interrupt prioritization is unnecessary.

3.2.3.2 Vectored Mode: Non-Cascaded Case

In the Vectored mode, the CPU uses an Interrupt Control Unit (ICU) to prioritize many interrupt requests. Upon receipt of an interrupt request on the $\overline{INT}$ pin, the CPU performs an "Interrupt Acknowledge, Master" bus cycle (Section 3.5.4.6) reading a vector value from the low-order byte of the Data Bus. This vector is then used as an index into the Dispatch Table in order to find the External Procedure Descriptor for the proper interrupt service procedure. The service procedure eventually returns via the Return from Interrupt (RETI) instruction, which performs an End of Interrupt bus cycle, informing the ICU that it may re-prioritize any interrupt requests still pending. The ICU provides the vector number again, which the CPU uses to determine whether it needs also to inform a Cascaded ICU (see below).

In a system with only one ICU (16 levels of interrupt), the vectors provided must be in the range of 0 through 127; that is, they must be positive numbers in eight bits. By providing

3.0 Functional Description (Continued)

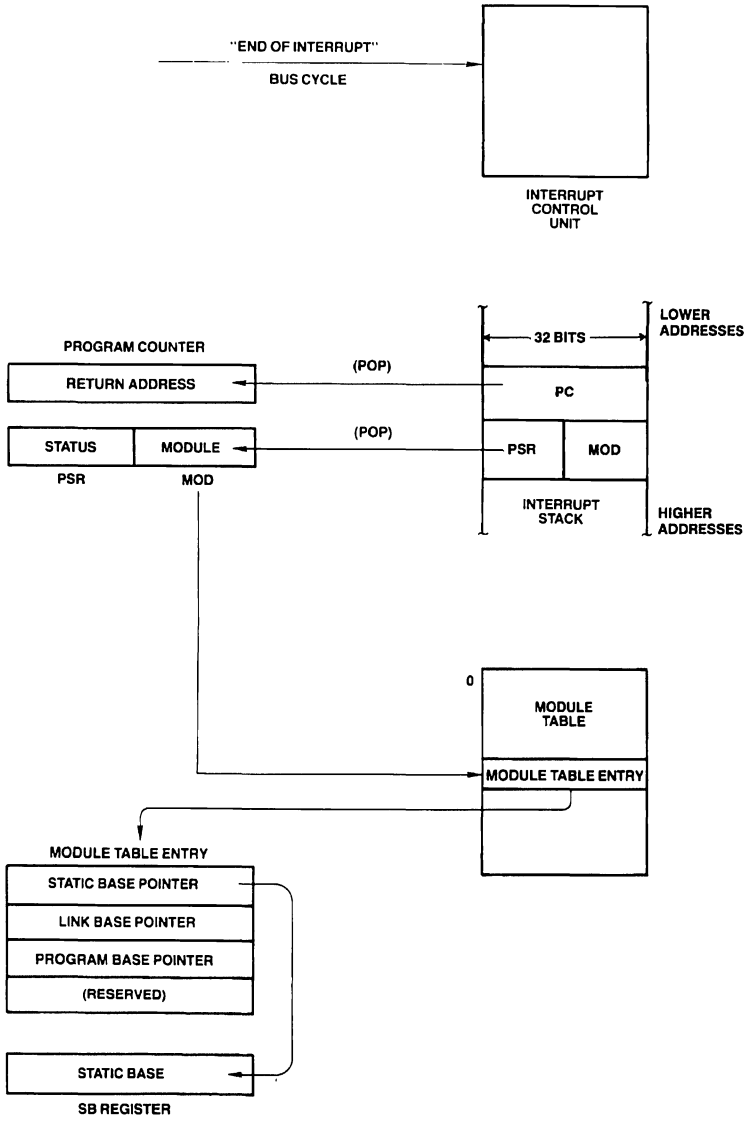

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FIGURE 3-13. Return from Interrupt (RETI) Instruction Flow. Direct-Exception Mode Disabled.

3.0 Functional Description (Continued)

a negative vector number, an ICU flags the interrupt source as being a Cascaded ICU (see below).

3.2.3.3 Vectored Mode: Cascaded Case

In order to allow more levels of interrupt, provision is made in the CPU to transparently support cascading. Note that the Interrupt output from a Cascaded ICU goes to an Interrupt Request input of the Master ICU, which is the only ICU which drives the CPU $\overline{INT}$ pin. Refer to the ICU data sheet for details.

In a system which uses cascading, two tasks must be performed upon initialization:

1) For each Cascaded ICU in the system, the Master ICU must be informed of the line number on which it receives the cascaded requests.
2) A Cascade Table must be established in memory. The Cascade Table is located in a NEGATIVE direction from the location indicated by the CPU Interrupt Base (INTBASE) Register. Its entries are 32-bit addresses, pointing to the Vector Registers of each of up to 16 Cascaded ICUs.

Figure 3-9 illustrates the position of the Cascade Table. To find the Cascade Table entry for a Cascaded ICU, take its Master ICU line number (0 to 15) and subtract 16 from it, giving an index in the range -16 to -1. Multiply this value by 4, and add the resulting negative number to the contents of the INTBASE Register. The 32-bit entry at this address must be set to the address of the Hardware Vector Register of the Cascaded ICU. This is referred to as the "Cascade Address."

Upon receipt of an interrupt request from a Cascaded ICU, the Master ICU interrupts the CPU and provides the negative Cascade Table index instead of a (positive) vector number. The CPU, seeing the negative value, uses it as an index into the Cascade Table and reads the Cascade Address from the referenced entry. Applying this address, the CPU performs an "Interrupt Acknowledge, Cascaded" bus cycle, reading the final vector value. This vector is interpreted by the CPU as an unsigned byte, and can therefore be in the range of 0 through 255.

In returning from a Cascaded interrupt, the service procedure executes the Return from Interrupt (RETI) instruction, as it would for any Maskable Interrupt. The CPU performs an "End of Interrupt, Master" bus cycle, whereupon the Master ICU again provides the negative Cascade Table index. The CPU, seeing a negative value, uses it to find the corresponding Cascade Address from the Cascade Table. Applying this address, it performs an "End of Interrupt, Cascaded" bus cycle, informing the Cascaded ICU of the completion of the service routine. The byte read from the Cascaded ICU is discarded.

Note: If an interrupt must be masked off, the CPU can do so by setting the corresponding bit in the interrupt mask register of the interrupt controller.

However, if an interrupt is set pending during the CPU instruction that masks off that interrupt, the CPU may still perform an interrupt acknowledge cycle following that instruction since it might have sampled the $\overline{INT}$ line before the ICU deasserted it. This could cause the ICU to provide an invalid vector. To avoid this problem the above operation should be performed with the CPU interrupt disabled.

3.2.4 Non-Maskable Interrupt

The Non-Maskable Interrupt is triggered whenever a falling edge is detected on the $\overline{NMI}$ pin. The CPU performs an "Interrupt Acknowledge, Master" bus cycle (Section 3.5.4.6) when processing of this interrupt actually begins. The Interrupt Acknowledge cycle differs from that provided for Maskable Interrupts in that the address presented is $FFFFFF00_{16}$. The vector value used for the Non-Maskable Interrupt is taken as 1, regardless of the value read from the bus.

The service procedure returns from the Non-Maskable Interrupt using the Return from Trap (RETT) instruction. No special bus cycles occur on return.

3.2.5 Traps

Traps are processing exceptions that are generated as direct results of the execution of an instruction.

The return address saved on the stack by any trap except Trap (TRC) and Trap (DBG) is the address of the first bye of the instruction during which the trap occurred.

When a trap is recognized, maskable interrupts are not disabled except for the case of Trap (ABT) and Trap (DBG).

There are 11 trap conditions recognized by the NS32532 as described below.

Trap (ABT): An abort trap occurs when an invalid page table entry or a protection level violation is detected for any of the memory references required to execute an instruction.

Trap (SLAVE): An exceptional condition was detected by the Floating Point Unit or another Slave Processor during the execution of a Slave Instruction. This trap is requested via the Status Word returned as part of the Slave Processor Protocol (Section 3.1.4.1).

Trap (ILL): Illegal operation. A privileged operation was attempted while the CPU was in User Mode (PSR bit U = 1).

Trap (SVC): The Supervisor Call (SVC) instruction was executed.

Trap (DVZ): An attempt was made to divide an integer by zero. (The FPU trap is used for Floating Point division by zero.)

Trap (FLG): The FLAG instruction detected a "1" in the PSR F bit.

Trap (BPT): The Breakpoint (BPT) instruction was executed.

Trap (TRC): The instruction just completed is being traced.

Refer to Section 3.3.1 for details.

Trap (UND): An Undefined-Instruction trap occurs when an attempt to execute an instruction is made and one or more of the following conditions is detected:

1. The instruction is undefined. Refer to Appendix A for a description of the codes that the CPU recognizes to be undefined.
2. The instruction is a floating point instruction and the F-bit in the CFG register is 0.
3. The instruction is a custom slave instruction and the C-bit in the CFG register is 0.
4. The instruction is a memory-management instruction and the M-bit in the CFG register is 0.
5. An LMR or SMR instruction is executed while the U-flag in the PSR is 0 and the most significant bit of the instruction's short field is 0.
6. The reserved general adressing mode encoding (10011) is used.
7. Immediate addressing mode is used for an operand that has access class different from read.

3.0 Functional Description (Continued)

8. Scaled Indexing is used and the basemode is also Scaled Indexing.
9. The instruction is a floating-point or custom slave instruction that the FPU or custom slave detects to be undefined. Refer to Section 3.1.4.1 for more information.

Trap (OVF): An Integer-Overflow trap occurs when the V-bit in the PSR register is set to 1 and an Integer-Overflow condition is detected during the execution of an instruction. An Integer-Overflow condition is detected in the following cases:

1. The F-flag is 1 following execution of an ADDi, ADDQi, ADDCi, SUBi, SUBCi, NEGi, ABSi, or CHECKi instruction.
2. The product resulting from a MULi instruction cannot be represented exactly in the destination operand's location.
3. The quotient resulting from a DEIi, DIVi, or QUOi instruction cannot be represented exactly in the destination operand's location.
4. The result of an ASHi instruction cannot be represented exactly in the destination operand's location.
5. The sum of the 'INC' value and the 'INDEX' operand for an ACBi instruction cannot be represented exactly in the index operand's location.

Trap (DBG): A debug trap occurs when one or more of the conditions selected by the settings of the bits in the DCR register is detected. This trap can also be requested by activating the input signal $\overline{DBG}$. Refer to Section 3.3.2 for more information.

Note 1: Following execution of the WAIT instruction, then a Trap (DBG) can be pending for a PC-match condition. In such an event, the Trap (DBG) is processed immediately.

Note 2: If an attempt is made to execute a memory-management instruction while in User-Mode and the M-bit in the CFG register is 0, then Trap (UND) occurs.

Note 3: If an attempt is made to execute a privileged custom instruction while in User-Mode and the C-bit in the CFG register is 0, then Trap (UND) occurs.

Note 4: While operating in User-Mode, if an attempt is made to execute a privileged instruction with an undefined use of a general addressing mode (either the reserved encoding is used or else scaled-index or immediate modes are incorrectly used), the Trap (UND) occurs.

Note 5: If an undefined instruction or illegal operation is detected, then no data references are performed for the instruction.

Note 6: For certain instructions that are relatively long to execute, such as DEID, the CPU checks for pending interrupts during execution of the instruction. In order to reduce interrupt latency, the NS2532 can suspend executing the instruction and process the interrupt. Refer to Section B.5 in Appendix B for more information about recognizing interrupts in this manner.

3.2.6 Bus Errors

A bus error exception occurs when the $\overline{BER}$ signal is asserted in response to an instruction fetch or data transfer that is required to execute an instruction.

Two types of bus errors are recognized: Restartable and Non-Restartable. Restartable bus errors are recognized during read bus cycles, except for MMU read cycles (from Page Tables) needed to translate the address of a result being stored into memory. All other bus errors are non-restartable.

The CPU responds to restartable bus errors by suspending the instruction that it was executing. When a non-restartable bus error is detected, the CPU responds immediately and the instruction being executed is terminated.

In this case, any results that have not yet been written to memory are discarded, and any pending traps other than Trap (DBG) for external condition, are eliminated. The PC value saved on the stack is undefined.

The NS32532 does not respond to bus errors indicated for instructions that are not executed. For example, no bus error exception occurs in response to asserting the $\overline{BER}$ signal during a bus cycle to prefetch an instruction that is not executed because the previous instruction caused a trap.

An exception to this rule occurs if the bus error is detected during an MMU write cycle to update the R-bit in a page table entry.

In this case the CPU recognizes the bus error and considers it as non-restartable even though the bus cycle that caused it belongs to a non-executed instruction.

If a bus error is detected during a data transfer required for the processing of another exception or during the ICU read cycle of a RETI instruction, then the CPU considers it as a fatal bus error and enters the 'HALTED' state.

Note 1: If the address and control signals associated with the last bus cycle that caused a bus error are latched by external hardware, then the information they provide can be used by the service procedure for restartable bus errors to analyze and resolve the exception recognized by the CPU. This can be accomplished because upon detecting a restartable bus error, the NS32532 stops making memory references for subsequent instructions until it determines whether the instruction that caused the bus error is executed and the exception is processed.

Note 2: When a non-restartable bus error is recognized, the service procedure must execute the CINV and LMR instructions to invalidate the on-chip caches and TLB. This is necessary to maintain coherence between them and external memory.

3.2.7 Priority Among Exceptions

The CPU checks for specific exceptions at various points while executing an instruction. It is possible that several exceptions occur simultaneously. In that event, the CPU responds to the exception with highest priority.

Figure 3-14 shows an exception processing flowchart. A non-restartable bus error is assigned highest priority and is serviced immediately regardless of the execution state of the CPU.

Before executing an instruction, the CPU checks for pending Trap (DBG), interrupts, and Trap (TRC), in that order. If a Trap (DBG) is pending, then the CPU processes that exception, otherwise the CPU checks for pending interrupts. At this point, the CPU responds to any pending interrupt requests; nonmaskable interrupts are recongized with higher priority than maskable interrupts. If no interrupts are pending, then the CPU checks the P-flag in the PSR to determine whether a Trap (TRC) is pending. If the P-flag is 1, a Trap (TRC) is processed. If no Trap (DBG), interrupt or Trap (TRC) is pending, the CPU begins executing the instruction.

While executing an instruction, the CPU may recognize up to four exceptions:

1. trap (ABT)
2. restartable bus error
3. trap (DBG) or interrupt, if the instruction is interruptible
4. one of 7 mutually exclusive traps: SLAVE, ILL, SVC, DVZ, FLG, BPT, UND

Trap (ABT) and restartable bus error have equal priority; the CPU responds to the first one detected.

If no exception is detected while the instruction is executing, then the instruction is completed and the PC is updated to point to the next instruction. If a Trap (OVF) is detected, then it is processed at this time.

3.0 Functional Description (Continued)

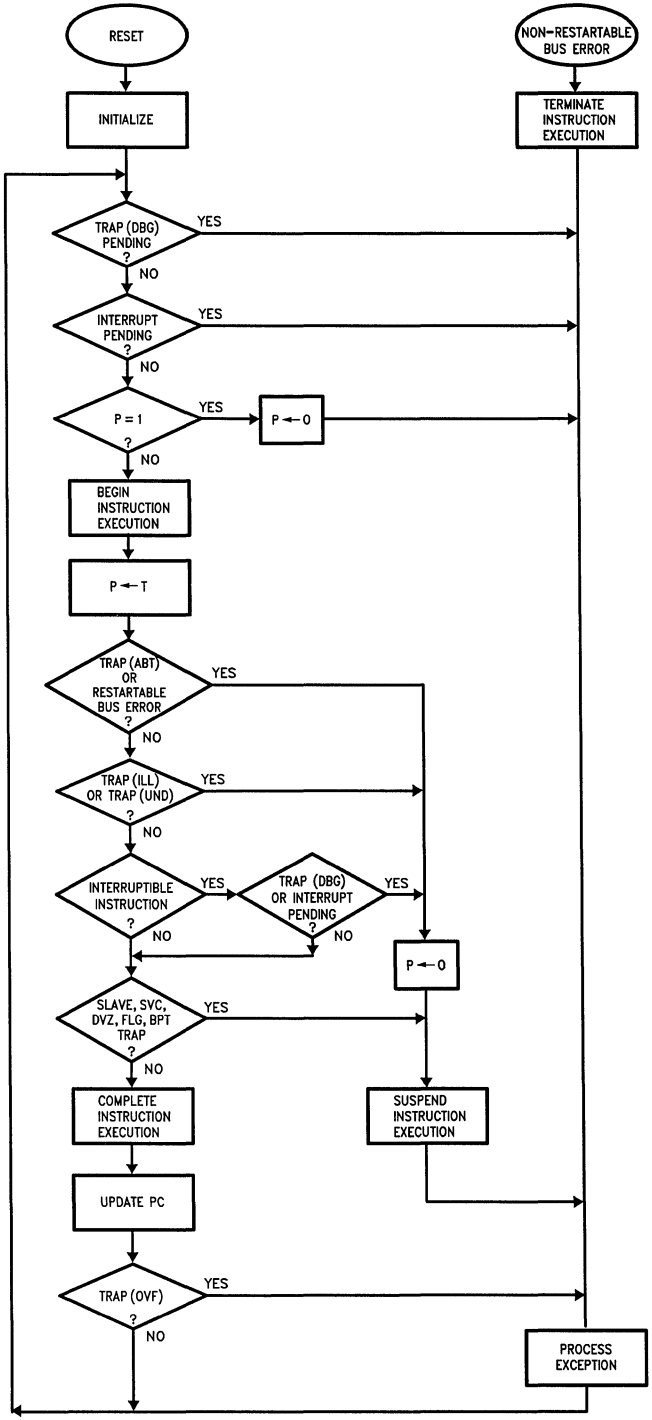

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FIGURE 3-14. Exception Processing Flowchart

3.0 Functional Description (Continued)

While executing the instruction, the CPU checks for enabled debug conditions. If an enabled debug condition is met, a Trap (DBG) is held pending until after the instruction is completed (see Note 3). If another exception is detected before the instruction is completed, the pending Trap (DBG) is removed and the DSR register is not updated.

Note 1: Trap (DBG) can be detected simultaneously with Trap (OVF). In this event, the Trap (OVF) is processed before the Trap (DBG).

Note 2: An address-compare debug condition can be detected while processing a bus error, interrupt, or trap. In this event, the Trap (DBG) is held pending until after the CPU has processed the first exception.

Note 3: Between operations of a string instruction, the CPU responds to pending operand address compare and external debug conditions as well as interrupts. If a PC-match debug condition is detected while executing a string instruction, then Trap (DBG) is held pending until the instruction has completed.

3.2.8 Exception Acknowledge Sequences: Detailed Flow

For purposes of the following detailed discussion of exception acknowledge sequences, a single sequence called "service" is defined in *Figure 3-15*.

Upon detecting any interrupt request, trap or bus error condition, the CPU first performs a sequence dependent upon the type of exception. This sequence will include saving a copy of the Processor Status Register and establishing a vector and a return address. The CPU then performs the service sequence.

3.2.8.1 Maskable/Non-Maskable Interrupt Sequence

This sequence is performed by the CPU when the $\overline{NMI}$ pin receives a falling edge, or the $\overline{INT}$ pin becomes active with the PSR I bit set. The interrupt sequence begins either at the next instruction boundary or, in the case of an interruptible instruction (e.g., string instruction), at the next interruptible point during its execution.

1. If an interruptible instruction was interrupted and not yet completed:
   a. Clear the Processor Status Register P bit.
   b. Set "Return Address" to the address of the first byte of the interrupted instruction.

   Otherwise, set "Return Address" to the address of the next instruction.
2. Copy the Processor Status Register (PSR) into a temporary register, then clear PSR bits T, V, U, S, P and I.
3. If the interrupt is Non-Maskable:
   a. Read a byte from address $FFFFFF00_{16}$, applying Status Code 00100 (Interrupt Acknowledge, Master). Discard the byte read.
   b. Set "Vector" to 1.
   c. Go to Step 8.
4. If the interrupt is Non-Vectored:
   a. Read a byte from address $FFFFFE00_{16}$, applying Status Code 00100 (Interrupt Acknowledge, Master). Discard the byte read.
   b. Set "Vector" to 0.
   c. Go to Step 8.
5. Here the interrupt is Vectored. Read "Byte" from address $FFFFFE00_{16}$, applying Status Code 00100 (Interrupt Acknowledge, Master).
6. If "Byte" ≥ 0, then set "Vector" to "Byte" and go to Step 8.
7. If "Byte" is in the range -16 through -1, then the interrupt source is Cascaded. (More negative values are reserved for future use.) Perform the following:
   a. Read the 32-bit Cascade Address from memory. The address is calculated as INTBASE + 4* Byte.
   b. Read "Vector," applying the Cascade Address just read and Status Code 00101 (Interrupt Acknowledge, Cascaded).
8. Perform Service (Vector, Return Address), *Figure 3-15*.

3.2.8.2 Abort/Restartable Bus Error Sequence

1. Suspend instruction and restore the currently selected Stack Pointer to its original contents at the beginning of the instruction.
2. Clear the PSR P bit.
3. Copy the PSR into a temmporary register, then clear PSR bits T, V, U, S and I.
4. Set "Vector" to the value corresponding to the exception type:

   Abort: Vector = 2

   Restartable Bus Error: Vector = 11
5. Set "Return Address" to the address of the first byte of the suspended instruction.
6. Perform Service (Vector, Return Address), *Figure 3-15*.

3.2.8.3 SLAVE/ILL/SVC/DVZ/FLG/BPT/UND Trap Sequence

1. Restore the currently selected Stack Pointer and the Processor Status Register to their original values at the start of the trapped instruction.
2. Set "Vector" to the value corresponding to the trap type.

   SLAVE: Vector = 3.
   ILL: Vector = 4.
   SVC: Vector = 5.
   DVZ: Vector = 6.
   FLG: Vector = 7.
   BPT: Vector = 8.
   UND: Vector = 10.
3. If Trap (ILL) or Trap (UND)
   a. Clear the Processor Status Register P bit.
4. Copy the Processor Status Register (PSR) into a temporary register, then clear PSR bits T, V, U, S and P.
5. Set "Return Address" to the address of the first byte of the trapped instruction.
6. Perform Service (Vector, Return Address), *Figure 3-15*.

3.2.8.4 Trace Trap Sequence

1. In the Processor Status Register (PSR), clear the P bit.
2. Copy the PSR into a temporary register, then clear PSR bits T, V, U and S.
3. Set "Vector" to 9.
4. Set "Return Address" to the address of the next instruction.
5. Perform Service (Vector, Return Address), *Figure 3-15*.

3.2.8.5 Integer-Overflow Trap Sequence

1. Copy the PSR into a temporary register, then clear PSR bits T, V, U, S and P.
2. Set "Vector" to 13.

3.0 Functional Description (Continued)

3. Set "Return Address" to the address of the next instruction.
4. Perform Service (Vector, Return Address), *Figure 3-15*.

3.2.8.6 Debug Trap Sequence

A debug condition can be recognized either at the next instruction boundary or, in the case of the String instructions, at the next interruptible point during its execution.

1. If PC-match condition, then go to Step 3.
2. If a String instruction was interrupted and not yet completed:
   a. Clear the Processor Status Register P bit.
   b. Set "Return Address" to the address of the first byte of the instruction.
   c. Go to Step 4.
3. Set "Return Address" to the address of the next instruction.
4. Set "Vector" to 14.
5. Copy the Processor Status Register (PSR) into a temporary register, then clear PSR bits T, V, U, S, P and I.
6. Perform Service (Vector, Return Address), *Figure 3-15*.

3.2.8.7 Non-Restartable Bus Error Sequence

1. Set "Vector" to 12.
2. Set "Return Address" to "Undefined".
3. Copy the Processor Status Register (PSR) into a temporary register, then clear PSR bits T, V, U, S, P and I.
4. Perform a dummy read of the Slave Status Word to reset the Slave Processor.
5. Perform Service (Vector, Return Address), *Figure 3-15*.

3.3 DEBUGGING SUPPORT

The NS32532 provides serveral features to assist in program debugging.

Besides the Breakpoint (BPT) instruction that can be used to generate soft breaks, the CPU also provides instruction tracing as well as debug trap (or hardware breakpoints) capabilities. Details on these features are provided in the following sub-sections.

3.3.1 Instruction Tracing

Instruction tracing is a very useful feature that can be used during debugging to single-step through selected portions of a program. Tracing is enabled by setting the T-bit in the PSR Register. When enabled, the CPU generates a Trace Trap (TRC) after the execution of each instruction.

At the beginning of each instruction, the T bit is copied into the PSR P (Trace "Pending") bit. If the P bit is set at the end of an instruction, then the Trace Trap is activated. If any other trap or interrupt request is made during a traced instruction, its entire service procedure is allowed to complete before the Trace Trap occurs. Each interrupt and trap sequence handles the P bit for proper tracing, guaranteeing only one Trace Trap per instruction, and guaranteeing that the Return Address pushed during a Trace Trap is always the address of the next instruction to be traced.

Due to the fact that some instructions can clear the T and P bits in the PSR, in some cases a Trace Trap may not occur at the end of the instruction. This happens when one of the privileged instructions BICPSRW or LPRW PSR is executed.

TABLE 3-3. Summary of Exception Processing

Exception	Instruction Ending	Cleared Before Saving PSR	Cleared After Saving PSR
Restartable Bus Error	Suspended	P	TVUSI
Nonrestartable Bus Error	Terminated	Undefined	TVUSPI
Interrupt	Before Instruction	None/P*	TVUSPI
ABT	Suspended	P	TVUSI
ILL, UND	Suspended	P	TVUS
SLAVE, SVC, DVZ, FLG, BPT	Suspended	None	TVUSP
OVF	Completed	None	TVUSP
TRC	Before Instruction	P	TVUS
DBG	Before Instruction	None/P*	TVUSPI

***Note:** The P bit of the saved PSR is cleared in case the exception is acknowledged before the instruction is completed (e.g., interrupted string instruction). This is to avoid a mid-instruction trace trap upon return from the Exception Service Routine.

Service (Vector, Return Address):

1) Push the PSR copy onto the Interrupt Stack as a 16-bit value.

2) If Direct-Exception mode is selected, then go to step 4.

3) Push MOD Register into the Interrupt Stack as a 16-bit value.

4) Read 32-bit Interrupt Dispatch Table (IDT) entry at address 'INTBASE + vector × 4'.

5) If Direct-Exception mode is selected, then go to Step 10.

6) Move the L.S. word of the IDT entry (Module Field) into the MOD register.

7) Read the Program Base pointer from memory address 'MOD + 8', and add to it the M.S. word of the IDT entry (Offset Field), placing the result in the Program Counter.

8) Read the new Static Base pointer from the memory address contained in MOD, placing it into the SB Register.

9) Go to Step 11.

10) Place IDT entry in the Program Counter.

11) Push the Return Address onto the Interrupt Stack as a 32-bit quantity.

12) Serialize: Non-sequentially fetch first instruction of Exception Service Routine.

Note: Some of the Memory Accesses indicated in the service sequence may be performed in an order different from the one shown.

FIGURE 3-15. Service Sequence

3.0 Functional Description (Continued)

In other cases, it is still possible to guarantee that a Trace Trap occurs at the end of the instruction, provided that special care is taken before returning from the Trace Trap Service Procedure. In case a BICPSRB instruction has been executed, the service procedure should make sure that the T bit in the PSR copy saved on the Interrupt Stack is set before executing the RETT instruction to return to the program begin traced. If the RETT or RETI instructions have to be traced, the Trace Trap Service Procedure should set the P and T bits in the PSR copy on the Interrupt Stack that is going to be restored in the execution of such instructions.

Note: If instruction tracing is enabled while the WAIT instruction is executed, the Trap (TRC) occurs after the next interrupt, when the interrupt service procedure has returned.

3.3.2 Debug Trap Capability

The CPU recognizes three different conditions to generate a Debug Trap:

1) Address Compare

2) PC Match

3) External

These conditions can be enabled and monitored through the CPU Debug Registers.

An address-compare condition is detected when certain memory locations are either read or written. The double-word address used for the comparison is specified in the CAR Register. The address-compare condition can be separately enabled for each of the bytes in the specified double-word, under control of the CBE bits of the DCR Register. The VNP bit in the DCR controls whether virtual or physical addresses are compared. The CRD and CWR bits in the DCR separately enable the address compare condition for read and write references; the CAE bit in the DCR can be used to disable the compare-address condition independently from the other control bits. The CPU examines the address compare condition for all data reads and writes, reads of memory locations for effective address calculations, Interrupt-Acknowledge and End-of-Interrupt bus cycles, and memory references for exception processing. An address-compare condition is not detected for MMU references to Page Table Entries.

The PC-match condition is detected when the address of the instruction equals the value specified in the BPC register. The PC-match condition is enabled by the PCE bit in the DCR.

Detection of address-compare and PC-match conditions is enabled for User and Supervisor Modes by the UD and SD bits in the DCR. The DEN-bit can be used to disable detection of these two conditions independently from the other control bits.

An external condition is recognized whenever the $\overline{DBG}$ signal is activated.

When the CPU detects an address-compare or PC-match condition while executing an instruction or processing an exception, then Trap (DBG) occurs if the TR bit in the DCR is 1. When an external debug condition is detected, Trap (DBG) occurs regardless of the TR bit. The cause of the Trap (DBG) is indicated in the DSR Register.

When an address-compare or PC-match condition is detected while executing an instruction, the CPU asserts the $\overline{BP}$ signal at the beginning of the next instruction, synchronously with $\overline{PFS}$. If the instruction is not completed because a higher priority trap (i.e., ABORT) is detected, the $\overline{BP}$ signal may or may not be asserted.

Note 1: While executing the MOVUS and MOVSU instructions, the compare-address condition is enabled for the User space memory reference under control of the UD-bit in the DCR.

Note 2: When the LPRi instruction is executed to load a new value into the BPC, CAR or DCR, it is undefined whether the address-compare and PC-match conditions, in effect while executing the instruction, are detected under control of the old or new contents of the loaded register. Therefore, any LPRi instruction that alters the control of the address-compare or PC-match conditions should use register or immediate addressing mode for the source operand.

3.4 ON-CHIP CACHES

The NS32532 provides three on-chip caches: the Instruction Cache (IC), the Data Cache (DC) and the Translation Look-aside Buffer (TLB).

The first two are used to hold the contents of frequently used memory locations, while the TLB holds address-translation information.

The IC and DC can be individually enabled by setting appropriate bits in the CFG Register (See Section 2.1.4); the TLB is automatically enabled when address-translation is enabled.

The CPU also provides a locking feature that allows the contents of the IC and DC to be locked to specific memory locations. This is accomplished by setting the LIC and LDC bits in the CFG register.

Cache locking can be successfully used in real-time applications to guarantee fast access to critical instruction and data areas.

Details on the organization and function of each of the caches are provided in the following sections.

Note: The size and organization of the on-chip caches may change in future Series 32000 microprocessors. This however, will not affect software compatibility.

3.4.1 Instruction Cache (IC)

The basic structure of the instruction cache (IC) is shown in *Figure 3-16*.

The IC stores 512 bytes of code in a direct-mapped organization with 32 sets. Direct-mapped means that each set contains only one block, thus each memory location can be loaded into the IC in only one place.

Each block contains a 23-bit tag, which holds the most-significant bits of the physical address for the locations stored in the block, along with 4 double-words and 4 validity bits (one for each double-word).

A 4-double-word instruction buffer is also provided, which is loaded either from a selected cache block or from external memory. Instructions are read from this buffer by the loader unit and transferred to an 8-byte instruction queue.

The IC may or may not be enabled to cache an instruction being fetched by the CPU. It is enabled when the IC bit in the CFG Register is set to 1 and either the address translation is disabled or the CI bit in the Level-2 PTE used to translate the virtual address of the instruction is set to 0.

If the IC is disabled, the CPU bypasses it during the instruction fetch and its contents are not affected. The instruction is read directly from external memory into the instruction buffer.

3.0 Functional Description (Continued)

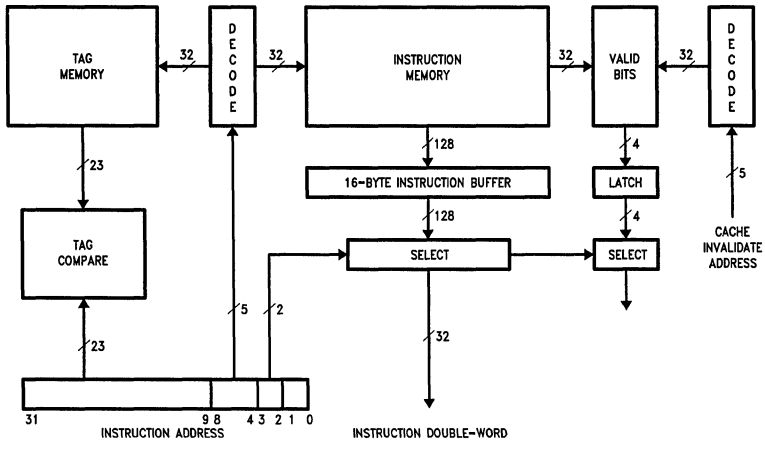

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FIGURE 3-16. Instruction Cache Structure

When the IC is enabled, the instruction address bits 4 to 8 are used to select the IC set where the instruction may be stored. The tag corresponding to the single block in the set is compared with the 23 most-significant bits of the instruction's physical address. The 4 double-words in this block are loaded into the instruction buffer and the 4 validity bits are also retrieved. Bits 2 and 3 of the instruction's physical address select one of these double-words and the associated validity bit.

If the tag matches and the selected double-word is valid, a cache 'hit' occurs and the double-word is directly transferred to the instruction queue for decoding; otherwise a cache 'miss' will result.

In the latter case, if the cache is not locked, the CPU will take the following actions.

First, if the tag of the selected block does not match, the tag is loaded with the 23 most-significant bits of the instruction address and all the validity bits are cleared. Then, the instruction is read from external memory into the instruction buffer.

If the CIIN input signal is not active during the fetching of the missing instruction, then the IC is updated and the instruction double-words fetched from memory are stored into it with the validity bits set.

If the cache is locked, its contents are not affected, as the CPU reads the missing instruction from external memory.

Whenever the CPU accesses external memory, whether or not the IC is enabled, it always fetches instruction double-words in a non-wrap-around fashion. Refer to Sections 3.5.4.3 and 3.5.6 for more information.

The contents of the instruction cache can be invalidated by software through the CINV instruction or by hardware through the appropriate cache invalidation input signals. Clearing the IC bit in the CFG Register also invalidates the instruction cache. Refer to Sections 3.5.10 and C.3 for details.

Note: If the IC is enabled for a certain instruction and a 'miss' occurs due to a tag mismatch, the CPU will update the tag and clear all the validity bits before fetching the instruction from external memory. If the CIIN input signal is activated during the fetching of that instruction, the validity bits are not set and the IC is not updated.

3.4.2 Data Cache (DC)

The Data Cache (DC) stores 1,024 bytes of data in a two-way set associative organization as shown in *Figure 3-17*.

Each of the 32 sets has 2 cache blocks. Each block contains a 23-bit tag, which holds the most-significant bits of the physical address for the locations stored in the block, along with 4 double-words and 4 validity bits (one for each double-word).

The DC is enabled for a data read when all of the following conditions are satisfied.

- The DC bit in the CFG Register is set to 1.
- Either the address translation is disabled or the CI bit in the Level-2 PTE used to translate the virtual address of the data reference is set to 0.
- The reference is not an interlocked read resulting from executing a CBITI or SBITI instruction.

If the DC is disabled, the CPU bypasses it during the data read and its contents are not affected. The data is read directly from external memory. The DC is also bypassed for MMU reads from Page Table entries during address translation and for Interrupt-Acknowledge and End-of-Interrupt bus cycles.

When the DC is enabled for a data read, the address bits 4 to 8 are used to select the DC set where the data may be stored.

The tags corresponding to the two blocks in the set are compared to the 23 most-significant bits of the physical address. Bits 2 and 3 of the address select one double-word in each block and the associated validity bit.

If one of the tag matches and the selected double-word in the corresponding block is valid, a cache 'hit' occurs and the data is used to execute the instruction; otherwise a cache 'miss' will result. In the latter case, if the cache is not locked, the CPU will take the following actions.

3.0 Functional Description (Continued)

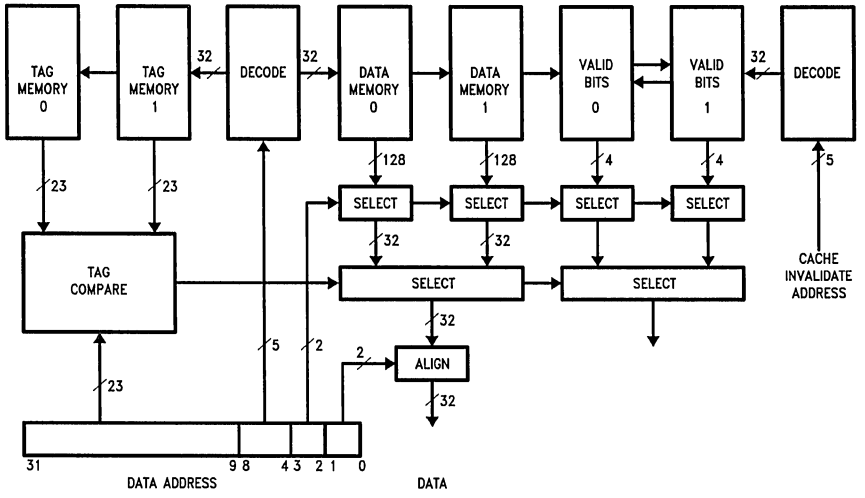

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FIGURE 3-17. Data Cache Structure

First, if the tag of either block in the set matches the data address, that block is selected for updating. Otherwise, if neither tag matches, then the least recently used block is selected; its tag is loaded with the 23 most-significant bits of the data address, and all the validity bits are cleared.

Then, the data is read from external memory; up to 4 double-word bits are read into the cache in a wrap-around fashion. Refer to Sections 3.5.4.3 and 3.5.6 for more information.

If the CIIN and $\overline{\text{IODEC}}$ input signals are both inactive during the bus cycles performed to read the missing data, then the DC is updated, as each double-word is read from memory, and the corresponding validity bit is set. If the cache is locked, its contents are not affected, as the CPU reads the missing data from external memory.

The DC is enabled for a data write whenever the DC bit in the CFG Register is set to 1, including interlocked writes resulting from executing the CBITI and SBITI instructions, and MMU writes to Page Table entries during address translation.

The DC does not use write allocation. This means that, during a write, if a cache 'hit' occurs, the DC is updated, otherwise it is unaffected. The data is always written through to external memory.

The contents of the data cache can be invalidated by software through the CINV instruction or by hardware through the appropriate cache invalidation input signals. Clearing the DC bit in the CFG Register also invalidates the data cache. Refer to Sections 3.5.10 and C.3 for details.

Note: If the DC is enabled for a certain data reference and a "miss" occurs due to tag mismatch, the CPU will update the tag of the least recently used block and clear all the validity bits before reading the data from external memory. If either CIIN or $\overline{\text{IODEC}}$ are activated during the data read bus cycles, the validity bits are not set and the DC is not updated.

3.4.3 Cache Coherence Support

The NS32532 provides several mechanisms for maintaining coherence between the on-chip caches and external memory. In software, the use of caches can be inhibited for individual pages using the CI-bit in the level-2 Page Table Entries. The CINV instruction can be executed to invalidate entriely the Instruction Cache and/or Data Cache; the CINV instruction can also be executed to invalidate a single 16-byte block in either or both caches.

In hardware, the use of the caches can be inhibited for individual locations using the CIIN input signal. A cache invalidation request can cause the entire Instruction Cache and/or Data Cache to be invalidated; a cache invalidation request can also cause invalidation of a single set in either or both caches. Refer to Section 3.5.7 for more information.

An external "Bus Watcher" circuit can also be used to help maintain cache coherence. The Bus Watcher observes the CPU's bus cycles to maintain a copy of the on-chip cache tags while also monitoring writes to main memory by DMA controllers and other microprocessors in the system. When the Bus Watcher detects that a location in one of the on-chip caches has been modified in main memory, it issues an invalidation request to the CPU. The CPU provides the necessary information on the system interface to help maintain an external copy of the on-chip tags.

The status codes differentiate between instruction fetches and data reads.

The set, affected during the bus access (if CIOUT is low), as well as the tag can be determined from the address bits A4 through A8 and A9 through A31 respectively.

During a data read the CPU also indicates, by means of the CASEC signal, which block in the set is being updated.

Whenever a CINV instruction is executed, the operation code and operand appear on the system interface using slave processor bus cycles. Thus, invalidations of the on-chip caches by software can be monitored externally.

Note, however, that the software is responsible for communicating to the external circuitry the values of the cache enable and lock bits in the CFG Register, since the CPU does not generate any special cycle (e.g., Slave Cycle) when the CFG Register is loaded.

3.0 Functional Description (Continued)

3.4.4 Translation Look-aside Buffer (TLB)

The Translation Look-aside Buffer is an on-chip fully associative memory. It provides direct virtual to physical mapping for 64 pages, thus minimizing the time needed to perform the address translation.

The efficiency of the on-chip MMU is greatly increased by the TLB, which bypasses the much longer Page Table lookup in over 99% of the accesses made by the CPU.

Entries in the TLB are allocated and replaced automatically; the operating system is not involved. The TLB entries cannot be read or written by software; however, they can be purged from it under program control.

Figure 3-18 shows a model of the TLB. Information is placed into the TLB whenever a Page Table lookup is performed. If the retrieved mapping is valid (V = 1 in both levels of the Page Tables), and the access attempted is permitted by the protection level, an entry of the TLB is loaded from the information retrieved from memory.

The on-chip MMU places the Virtual Page Number (VPN) and the Address Space qualifier (AS) into the tag portion of the TLB entry.

The value portion of the entry is loaded from the Page Tables as follows:

- The PFN field (20 bits) as well as the CI and M bits are loaded from the Level-2 Page Table Entry (PTE2).
- The PL field (2 bits) is loaded to reflect the most restrictive of the protection levels imposed by the PL fields of the Level-1 and Level-2 Page Table Entries (PTE1 and PTE2).

Not shown in the figure is an additional bit associated with each TLB entry which indicates whether the entry is valid.

Address translation can be either enabled or disabled for a memory reference. If translation is disabled, then the TLB is bypassed and the physical address is identical to the virtual address.

When translation is enabled and a virtual address needs to be translated, the high-order 20 bits (VPN) and the Address Space qualifier are compared associatively to the corresponding fields in all entries of the TLB.

For a read reference, if the tag portion of a valid TLB entry, completely matches the input values, then the value portion of the entry is used to complete the address translation and protection checking.

For a write reference, if a valid entry with a matching tag is present in the TLB, then the M bit is examined. If the M bit is 1, the value portion of the entry is used to complete the address translation and protection checking. If the M bit is 0, the entry is invalidated.

In either case, if a protection level violation is detected, a translation exception (Trap (ABT)) is generated. When no matching entry is found or a matching entry is invalidated because the M bit is 0 in a write reference, a Page Table lookup is performed. The virtual address is translated according to the algorithm given in Section 2.4.5 and the translation information is loaded into the TLB.

The recipient entry is selected by an on-chip circuit that implements a First-In-First-Out (FIFO) algorithm.

Note that for a translation to be loaded into the TLB it is necessary that the Level-1 and Level-2 Page Table Entries be valid (V bit = 1). Also, it is guaranteed that in the process of loading a TLB entry (during a Page Table lookup) the Level-1 and Level-2 R bits will be set in memory if they were not already set. For these reasons, there is no need to replicate either the V bit or the R bit in the TLB entries.

Whenever a Page Table Entry in memory is altered by software, it is necessary to purge any matching entry from the TLB, otherwise the corresponding addresses would be translated according to obsolete information. TLB entries may be selectively purged by writing a virtual address to one of the IVARn registers using the LMR instruction. The TLB entry (if any) that matches that virtual address is then purged, and its space is made available for another translation. Purging is also performed whenever an address space is remapped by altering the contents of the PTB0 or PTB1 register. When this is done, all the TLB entries corresponding to the address space mapped by that register are purged. Turning translation on or off (via the MCR TU and TS bits) does not affect the contents of the TLB.

It is possible to maintain an external copy of the valid contents of the on-chip TLB by observing the CPU's system interface during the replacement and invalidation of TLB entries. Whenever the CPU replaces a TLB entry, the page tables are accessed in external memory using bus cycles with a special Status. Because a FIFO replacement algorithm is used, it is possible to determine which entry is being replaced by using a 6-bit counter that is incremented whenever a Level-1 PTE is accessed. The contents of the new entry can be found as follows:

- VPN appears on A2 through A11 during the PTE1 and PTE2 accesses. The most-significant 10 bits appear during the PTE1 access, and the least-significant 10 bits appear during the PTE2 access.
- AS can be determined from the U/$\overline{S}$ signal during the PTE1 access.
- PFN, M and CI can be determined from the PTE2 value read on the Data Bus. PL can be determined from the most restrictive of the PTE1 and PTE2 values read on the Data Bus.

Whenever a LMR instruction is executed, the operation code and operand appear on the system interface using slave processor bus cycles. Thus, the information is available externally to determine the translation modes controlled by the MCR and to identify that a TLB entry has been invalidated.

When the PTB0 register is loaded by executing the 'LMR PTB0 src' instruction, the internal FIFO pointer is also reset to point to the first TLB entry.

Note that the contents of the TLB maintained externally include copies of all valid entries in the on-chip TLB, but the external copy may include some entries that are invalid in the on-chip TLB. For example, when the TLB is searched for a write reference and a matching entry is found with the M bit clear, then the on-chip entry is invalidated and a miss is processed. It is not possible to detect externally that the old matching entry on-chip has been invalidated.

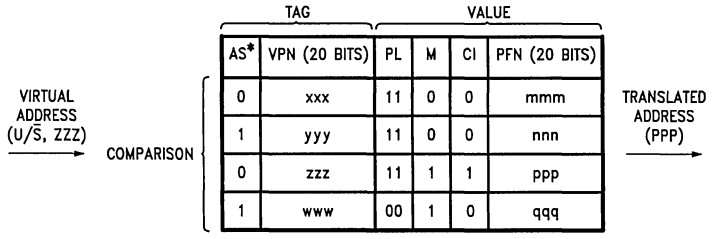
3.5 SYSTEM INTERFACE

This section provides general information on the NS32532 interface to the external world. Descriptions of the CPU requirements as well as the various bus characteristics are provided here. Details on other device characteristics including timing are given in Chapter 4.

3.5.1 Power and Grounding

The NS32532 requires a single 5-volt power supply, applied on 21 pins. The logic voltage pins (VCCL1 to VCCL6) supply

3.0 Functional Description (Continued)



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*AS represents the virtual address space qualifier.

FIGURE 3-18. TLB Model

the power to the on-chip logic. The buffer voltage pins (VCCB1 to VCCB14) supply the power to the output drivers of the chip. The bus clock power pin (VCCCLK) is the power supply for the on-chip clock drivers. All the voltage pins should be connected together by a power (VCC) plane on the printed circuit board.

The NS32532 grounding connections are made on 20 pins. The logic ground pins (GNDL1 to GNDL6) are the ground pins for the on-chip logic. The buffer ground pins (GNDB1 to GNDB13) are the ground pins for the output drivers of the chip. The bus clock ground pin (GNDCLK) is the ground connection for the on-chip clock drivers. All the ground pins should be connected together by a ground plane on the printed circuit board.

Both power and ground connections are shown in *Figure 3-19.*

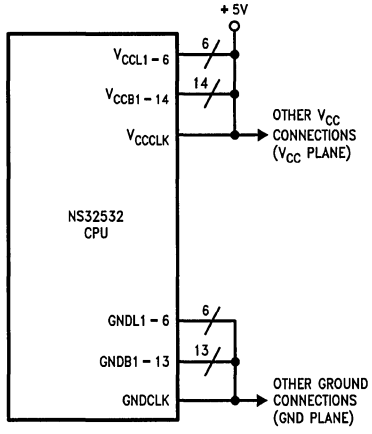

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FIGURE 3-19. Power and Ground Connections

3.5.2 Clocking

The NS32532 requires a single-phase input clock signal (CLK) with frequency twice the CPU's operating frequency.

This clock signal is internally divided by two to generate two non-overlapping phases PHI1 and PHI2. One single-phase clock signal BCLK in phase with PHI1 and its complement $\overline{BCLK}$, are also generated and output by the CPU for timing reference.

Following power-on, the phase relationship between BCLK and CLK is undefined. Nevertheless, in some systems it may be necessary to synchronize the CPU bus timing to an external reference. The $\overline{SYNC}$ input signal can be used to initialize the phase relationship between CLK and BCLK. $\overline{SYNC}$ can also be used to stretch BCLK (Low) while CLK is toggling.

$\overline{SYNC}$ is sampled on each rising edge of CLK. As shown in *Figure 3-20*, whenever $\overline{SYNC}$ is sampled low, BCLK stops toggling and stays low. On the first rising edge that $\overline{SYNC}$ is sampled high, BCLK is driven high and then toggles on each subsequent rising edge of CLK.

Every rising edge of BCLK defines a transition in the timing state ("T-State") of the CPU.

One T-State represents the execution of one microinstruction within the CPU and/or one step of an external bus transfer.

Note: The CPU requirement on the maximum period of BCLK must be satisfied when $\overline{SYNC}$ is asserted at times other than reset.

3.5.3 Resetting

The $\overline{RST}$ input pin is used to reset the NS32532. The CPU samples $\overline{RST}$ synchronously on the rising edge of BCLK. Whenever a low level is detected, the CPU responds immediately. Any instruction being executed is terminated; any results that have not yet been written to memory are discarded; and any pending bus errors, interrupts, and traps are eliminated. The internal latches for the edge-sensitive $\overline{NMI}$ and $\overline{DBG}$ signals are cleared.

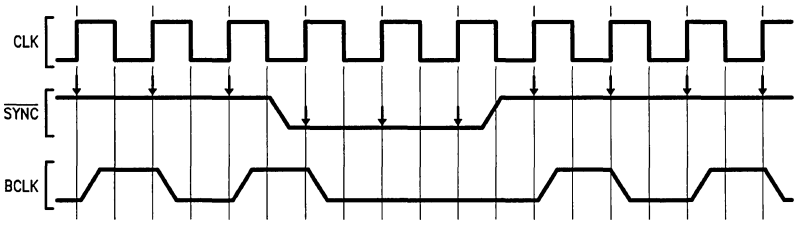

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FIGURE 3-20. Bus Clock Synchronization

3.0 Functional Description (Continued)

The CPU stores the PC contents in the R0 Register and the PSR contents in the least-significant word of R1, leaving the most-significant word undefined. The PC is then cleared to 0 and so are all the implemented bits in the PSR, MSR, MCR and CFG registers. The DEN-bit in the DCR Register is also cleared to 0. After reset, the remaining implemented bits in DCR and the contents of all other registers are undefined. The CPU begins executing the instruction at Address 0.

On application of power, $\overline{RST}$ must be held low for at least 50 μs after V_{CC} is stable. This is to ensure that all on-chip voltages are completely stable before operation. Whenever a Reset is applied, it must also remain active for not less than 64 BCLK cycles. See *Figures 3-21* and *3-22*.

While in the Reset state, the CPU drives the signals $\overline{ADS}$, $\overline{BE0}$–3, $\overline{BMT}$, $\overline{CONF}$ and $\overline{HLDA}$ inactive. The data bus is floated and the state of all other output signals is undefined.

Note: If $\overline{SYNC}$ is asserted while the CPU is being reset, then BCLK does not toggle. Consequently, $\overline{SYNC}$ must be high for at least 200 CLK cycles while $\overline{RST}$ is low.

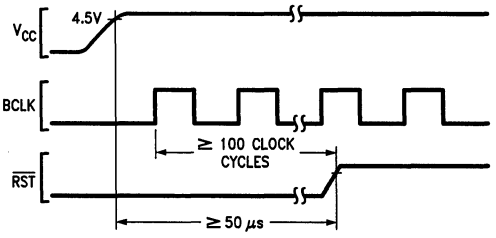

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FIGURE 3-21. Power-On Reset Requirements

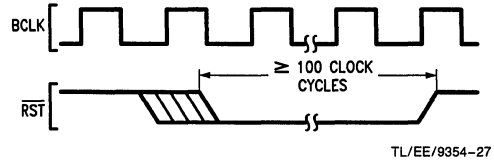

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FIGURE 3-22. General Reset Timing

3.5.4 Bus Cycles

The NS32532 CPU will perform bus cycles for one of the following reasons:

1. To fetch instructions from memory.
2. To write or read data to or from memory or peripheral devices. Peripheral input and output are memory mapped in the Series 32000 family.
3. To read and update Page Table Entries in memory to perform memory management functions.
4. To acknowledge an interrupt and allow external circuitry to provide a vector number, or to acknowledge completion of an interrupt service routine.
5. To transfer information to or from a Slave Processor.

In terms of bus timing, cases 1 through 4 above are identical. For timing specifications, see Section 4. The only external difference between them is the 5-bit code placed on the Bus Status pins (ST0–ST4). Slave Processor cycles differ in that separate control signals are applied (Section 3.5.4.7).

3.5.4.1 Bus Status

The CPU presents five bits of Bus Status information on pins ST0–ST4. The various combinations on these pins indicate why the CPU is performing a bus cycle, or, if it is idle on the bus, then why is it idle.

The Bus Status pins are interpreted as a five-bit value, with ST0 the least significant bit. Their values decode as follows:

00000 The bus is idle because the CPU does not yet need to access the bus.

00001 The bus is idle because the CPU is waiting for an interrupt following execution of the WAIT instruction.

00010 The bus is idle because the CPU has halted after detecting an abort or bus error while processing an exception.

00011 The bus is idle because the CPU is waiting for a Slave Processor to complete executing an instruction.

00100 Interrupt Acknowledge, Master.

The CPU is reading an interrupt vector to acknowledge an interrupt request.

00101 Interrupt Acknowledge, Cascaded.

The CPU is reading an interrupt vector to acknowledge a maskable interrupt request from a Cascaded Interrupt Control Unit.

00110 End of Interrupt, Master.

The CPU is performing a read cycle to indicate that it is executing a Return from Interrupt (RETI) instruction at the completion of an interrupt's service procedure.

00111 End of Interrupt, Cascaded.

The CPU is performing a read cycle from a Cascaded Interrupt Control Unit to indicate that it is executing a Return from Interrupt (RETI) instruction at the completion of an interrupt's service procedure.

01000 Sequential Instruction Fetch.

The CPU is fetching the next double-word in sequence from the instruction stream.

01001 Non-Sequential Instruction Fetch.

The CPU is fetching the first double-word of a new sequence of instruction. This will occur as a result of any JUMP or BRANCH, any exception, or after the execution of certain instructions.

01010 Data Transfer.

The CPU is reading or writing an operand for an instruction, or it is referring to memory while processing an exception.

01011 Read RMW Class Operand.

The CPU is reading an operand with access class of read-modify-write.

01100 Read for Effective Address Calculation.

The CPU is reading a pointer from memory in order to calculate an effective address for Memory Relative or External addressing modes.

01101 Access PTE1 by MMU.

The CPU is reading or writing a Level-1 Page Table Entry while the on-chip MMU is translating virtual address.

3.0 Functional Description (Continued)

01110 Access PTE2 by MMU.

The CPU is reading or writing a Level-2 Page Table Entry while the on-chip MMU is translating a virtual address.

11101 Transfer Slave Processor Operand.

The CPU is transferring an operand to or from a Slave Processor.

11110 Read Slave Processor Status.

The CPU is reading a status word from a slave processor after the slave processor has activated the $\overline{FSSR}$ signal.

11111 Broadcast Slave Processor ID + OPCODE.

The CPU is initiating the execution of a Slave Instruction by transferring the first 3 bytes of the instruction, which specify the Slave Processor identification and operation.

3.5.4.2 Basic Read and Write Cycles

The sequence of events occurring during a basic CPU access to either memory or peripheral device is shown in *Figure 3-23* for a read cycle, and *Figure 3-24* for a write cycle.

The cases shown assume that the selected memory or peripheral device is capable of communicating with the CPU at full speed. If not, then cycle extension may be requested through the $\overline{RDY}$ line. See Section 3.5.4.4.

A full speed bus cycle is performed in two cycles of the BCLK clock, labeled T1 and T2. For both read and write bus cycles the CPU asserts $\overline{ADS}$ during the first half of T1 indicating the beginning of the bus cycle. From the beginning of T1 until the completion of the bus cycle the CPU drives the Address Bus and other relevant control signals as indicated in the timing diagrams. For cacheable data read cycles the CPU also drives the CASEC signal to indicate the block in the DC set where the data will be stored. If the bus cycle is not cancelled (e.g., state T2 is entered in the next clock cycle), the confirm signal ($\overline{CONF}$) is asserted in the middle of T1. Note that due to a bus cycle cancellation, the $\overline{BMT}$ signal may be asserted at the beginning of T1, and then deasserted before the time in which it is guaranteed valid (see Section 4.4.2).

A confirmed bus cycle is completed at the end of T2, unless a cycle extension is requested. Following state T2 is either state T1 of the next bus cycle, or an idle T-state, if the CPU has no bus cycle to perform.

In case of a read cycle the CPU samples the data bus at the end of state T2.

If a bus exception is detected, the data is ignored.

For write bus cycles, valid data is output from the middle of T1 until the end of the cycle. When a write bus cycle is immediately followed by another write cycle, the CPU keeps driving the bus with the data related to the previous cycle until the middle of state T1 of the second bus cycle.

The CPU always inserts an idle state before a write cycle when the write immediately follows a read cycle.

Note: The CPU can initiate a bus cycle with a T1-state and then cancel the cycle, such as when a TLB miss or a Cache hit occurs. In such a case, the $\overline{CONF}$ signal remains High and the $\overline{BMT}$ signal is driven High; the T1-state is followed by another T1-state or an idle T-state.

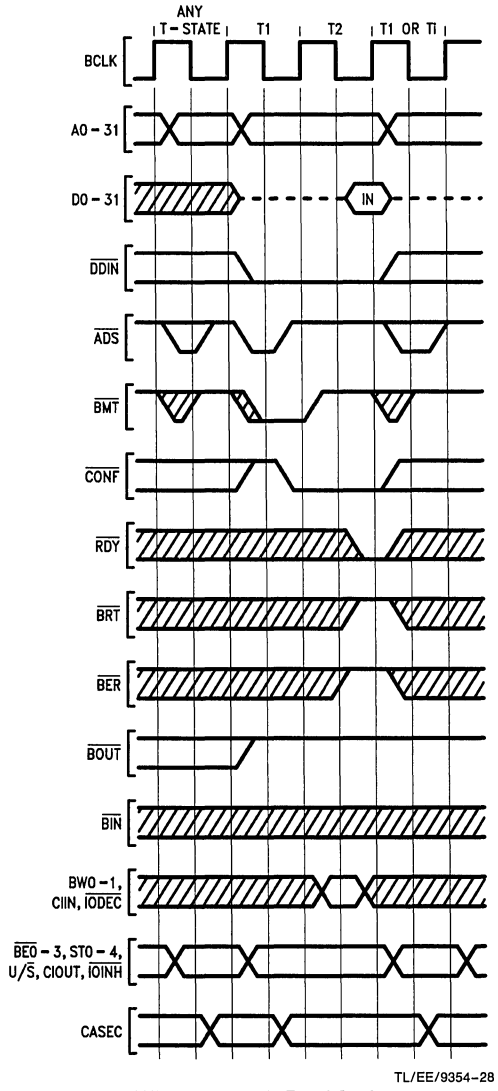

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FIGURE 3-23. Basic Read Cycle

3.0 Functional Description (Continued)

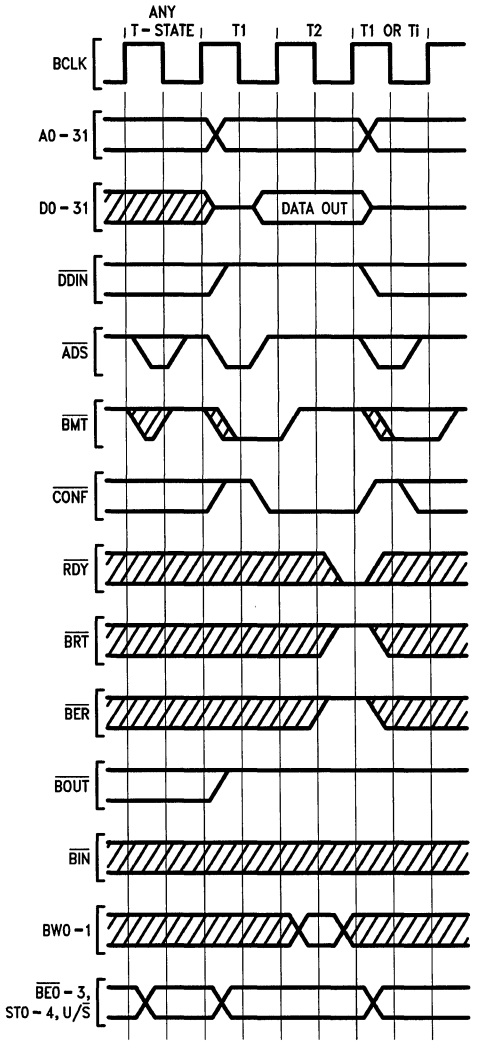

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FIGURE 3-24. Write Cycle

3.5.4.3 Burst Cycles

The NS32532 is capable of performing burst cycles in order to increase the bus transfer rate. Burst is only available in instruction fetch cycles and data read cycle from 32-bit wide memories. Burst is not supported in operand write cycles or slave cycles.

The sequence of events for burst cycles is shown in *Figure 3-25*. The case shown assumes that the selected memory is capable of communicating with the CPU at full speed. If not, then cycle extension can be requested through the $\overline{RDY}$ line. See Section 3.5.4.4.

A Burst cycle is composed of two parts. The first part is a regular cycle (opening cycle), in which the CPU outputs the new status and asserts all the other relevant control signals. In addition, the Burst Out Signal ($\overline{BOUT}$) is activated by the CPU indicating that the CPU can perform Burst cycles. If the selected memory allows Burst cycles, it will notify the CPU by activating the burst in signal ($\overline{BIN}$). $\overline{BIN}$ is sampled by the CPU in the middle of T2 on the falling edge of BCLK. If the memory does not allow burst ($\overline{BIN}$ high), the cycle will terminate at the end of T2 and $\overline{BOUT}$ will go inactive immediately. If the memory allows burst ($\overline{BIN}$ low), and the CPU has not deasserted $\overline{BOUT}$, the second part of the Burst cycle will be performed and $\overline{BOUT}$ will remain active until termination of the Burst.

The second part consists of up to 3 nibbles, labeled T2B. In each of them a data item is read by the CPU. For each nibble in the burst sequence the CPU forces the 2 least-significant bits of the address to 0 and increments address bits 2 and 3 to select the next double-word; all the byte enable signals ($\overline{BE}$0–3) are activated.

As shown in *Figures 3-25* and *4-8* (in Section 4), the CPU samples $\overline{RDY}$ at the end of each nibble and extends the access time for the burst transfer if $\overline{RDY}$ is inactive.

The CPU initiates burst read cycles in the following cases.

1. An instruction must be fetched (Status = 01000 or 01001), and the instruction address does not fall within the last double-word in an aligned 16-byte block (e.g., address bits 2 and 3 are not both equal to 1).
2. A data item must be read (Status = 01010, 01011 or 01100), and all of the following conditions are met.
   - The data cache is enabled and not locked. (DC = 1 and LDC = 0 in the CFG register.)
   - The addressed page is cacheable as indicated in the Level-2 Page Table Entry.
   - The bus cycle is not an interlocked data access performed while executing a CBITI or SBITI instruction.

The Burst sequence will be terminated when one of the following events occurs.

1. The last instruction double-word in an aligned 16-byte block has been fetched.
2. The CPU detects that the instructions being prefetched are no longer needed due to an alteration of the flow of control. This happens, for example, when a Branch instruction is executed or an exception occurs.
3. 4 double-words of data have been read by the CPU. The double-words are transferred within an aligned 16-byte block in a wrap-around order. For example, if a source operand is located at address 104, then the burst read cycle transfers the double-words at 104, 108, 112, and 100, in that order.

3.0 Functional Description (Continued)

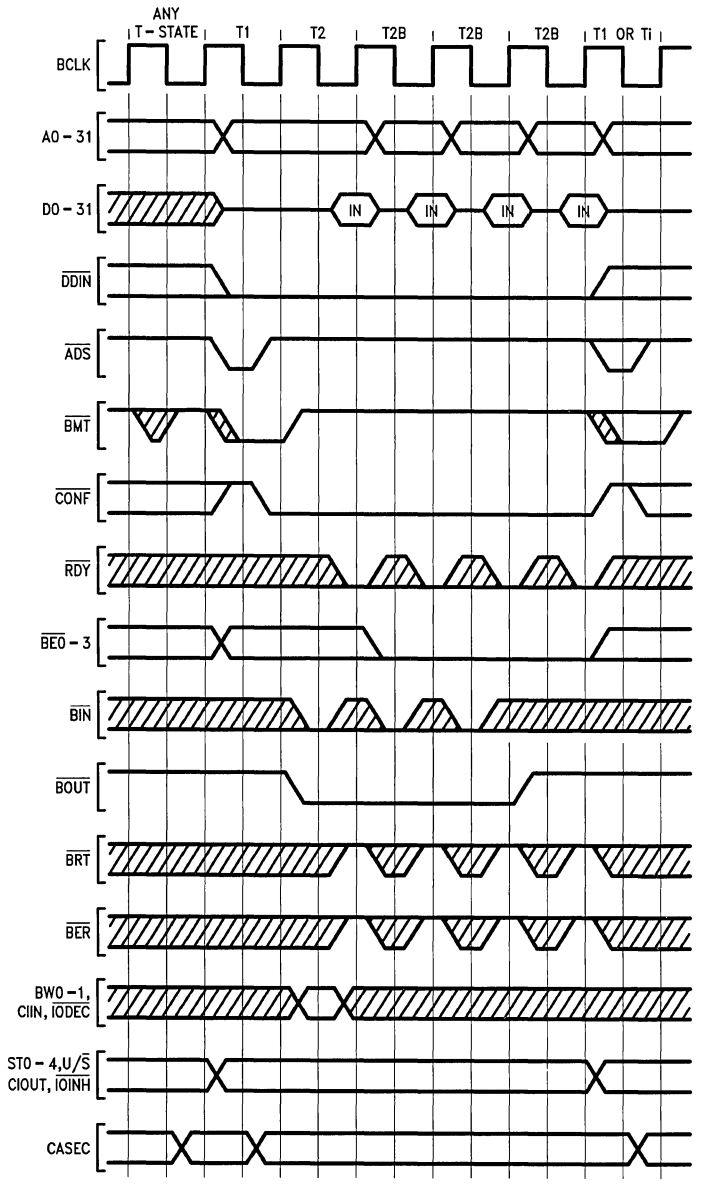

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FIGURE 3-25. Burst Read Cycles

3.0 Functional Description (Continued)

4. The $\overline{BIN}$ signal is deasserted.
5. $\overline{BRT}$ is asserted to signal a bus retry.
6. $\overline{IODEC}$ is asserted or the BW0–1 signals indicate a bus width other than 32-bits. The CPU samples these signals during state T2 of the opening cycle. During T2B-states BW0–1 are ignored and $\overline{IODEC}$ must be kept HIGH.

The CPU uses only the values of the above signals sampled during the last state of the transfer when the cycle is extended. See Section 3.5.4.4.

Note: A burst sequence is not stopped by the assertion of $\overline{BER}$. See Note 3 in Section 3.5.5.

3.5.4.4 Cycle Extension

To allow sufficient access time for any speed of memory or peripheral device, the NS32532 provides for extension of a bus cycle. Any type of bus cycle except a slave processor cycle can be extended.

A bus cycle can be extended by causing state T2 for a normal cycle or state T2B for a Burst cycle to be repeated.

At the end of each T2 or T2B state, on the rising edge of BCLK, the $\overline{RDY}$ line is sampled by the CPU. If $\overline{RDY}$ is active, then the transfer cycle will be completed. If $\overline{RDY}$ is inactive, then the bus cycle is extended by repeating the T-state for another clock cycle. These additional T-states inserted by the CPU in this manner are called 'WAIT' states.

During a transfer the CPU samples the input control signals $\overline{BIN}$, $\overline{BER}$, $\overline{BRT}$, BW0–1, CIIN and $\overline{IODEC}$.

When wait states are inserted, only the values of these signals sampled during the last wait state are significant.

Figures 3-26 and *4-8* (in Section 4) illustrate both a normal read cycle and a Burst cycle with wait states added through the $\overline{RDY}$ pin.

Note: If $\overline{RST}$ is asserted during a bus cycle, then the cycle is terminated without regard of $\overline{RDY}$.

3.5.4.5 Interlocked Bus Cycles

The NS32532 supports indivisible read-modify-write transactions by asserting the $\overline{ILO}$ signal during consecutive read and write operations. See *Figure 4-7* in Section 4.

Interlocked transactions are always preceded and followed by one or more idle T-states.

The $\overline{ILO}$ signal is asserted in the middle of the idle T-state preceding state T1 of the read operation, and is deasserted in the middle of one of the idle T-states following completion of the write operation, including any retried bus cycles.

No other bus operations (e.g., instruction fetches) will occur while an interlocked transaction is taking place.

Interlocked transactions are required in multiprocessor systems to handle shared resources. The CPU uses them to reference data while executing a CBITIi or SBITIi instruction, during which a single byte of data is read and written. They are also used when the on-chip MMU is updating a Level-2 Page Table Entry during a Page Table Lookup.

In this case a double-word is read and written. If the Level-2 Page Tables are located in a memory area whose width is other than 32 bits, multiple interlocked reads followed by multiple interlocked writes will result. The $\overline{ILO}$ signal is always released for one or more clock cycles in the middle of two consecutive interlocked transactions.

Note 1: If a bus error is detected during an interlocked read cycle, the subsequent interlocked write cycle will not be performed, and $\overline{ILO}$ is deasserted before the next bus cycle begins.

Note 2: The CPU may assert $\overline{ILO}$ before a read cycle that is cancelled (for example, due to a TLB miss). In such a case, the CPU deasserts $\overline{ILO}$ before performing any additional bus cycles.

3.5.4.6 Interrupt Control Cycles

The CPU generates Interrupt-Acknowledge bus cycles in response to non-maskable interrupt and enabled maskable interrupt requests.

The CPU also generates one or two End-of-Interrupt bus cycles during execution of the Return-from-Interrupt (RETI) instruction.

The timing for the interrupt control cycles is the same as for the basic memory read cycle shown in *Figure 3-23*; only the status presented on pins ST0–4 is different. These cycles are single-byte read cycles, and they always bypass the data cache.

Table 3-4 shows the interrupt control sequences associated with each interrupt and with the return from its service procedure.

3.5.4.7 Slave Processor Bus Cycles

The NS32532 performs bus cycles to transfer information to or from slave processors while executing floating-point or custom-slave instructions.

The CPU uses slave write bus cycles to broadcast the identification and operation codes of a slave instruction as well as to transfer operands from memory or general purpose registers to a slave.

Figure 3-27 shows the timing for a slave write bus cycle. The CPU asserts $\overline{SPC}$ during T1; the status is valid during T1 and T2. The operation code or operand is output on the data bus from the middle of T1 until the end of T2. The address line A9 is used during the transfer of the operation code to communicate to the slave the value of the I bit in the PSR register. A9 is high when the I bit is 1.

The CPU uses a slave read bus cycle to transfer a result operand from a slave to either memory or a general purpose register. A slave read cycle is also used to read a status word when the $\overline{FSSR}$ signal is asserted. *Figure 3-28* shows the timing for a slave read bus cycle.

During T1 and T2 the CPU drives the status lines and asserts $\overline{SPC}$. The data from the slave is sampled at the end of T2.

The CPU will never perform another slave cycle immediately following a slave read cycle. In fact, the T-state following state T2 of a slave read cycle is either an idle T-state or the T1 state of a memory cycle.

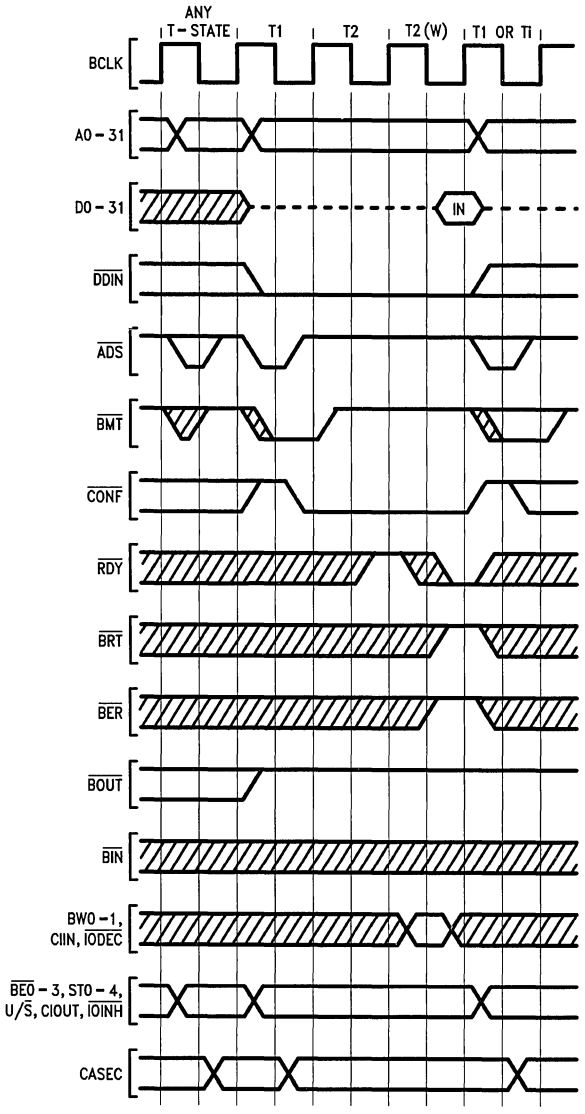
Slave processor data transfers are always 32 bits wide. If the operand is a single byte, then it is transferred on D0 through D7. If it is a word, then it is transferred on D0 through D15.

When two operands are transferred, operand 1 is transferred before operand 2. For double-precision operands, the least-significant double-word is transferred before the most-significant double-word.

During a slave bus cycle the output signals $\overline{BE}$0–3 are undefined while the input signals BW0–1 and $\overline{RDY}$ are ignored.

$\overline{BER}$ and $\overline{BRT}$ must be kept high.

3.0 Functional Description (Continued)



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3-26. Cycle Extension of a Basic Read Cycle

3.0 Functional Description (Continued)

TABLE 3-4. Interrupt Sequences

Cycle	Status	Address	$\overline{DDIN}$	$\overline{BE3}$	$\overline{BE2}$	$\overline{BE1}$	$\overline{BE0}$	Data Bus Byte 3	Byte 2	Byte 1	Byte 0
A. Non-Maskable Interrupt Control Sequences											
Interrupt Acknowledge											
1	00100	$FFFFFF00_{16}$	0	1	1	1	0	X	X	X	X
Interrupt Return											
None: Performed through Return from Trap (RETT) instruction.											
B. Non-Vectored Interrupt Control Sequences											
Interrupt Acknowledge											
1	00100	$FFFFFE00_{16}$	0	1	1	1	0	X	X	X	X
Interrupt Return											
1	00110	$FFFFFE00_{16}$	0	1	1	1	0	X	X	X	X
C. Vectored Interrupt Sequences: Non-Cascaded											
Interrupt Acknowledge											
1	00100	$FFFFFE00_{16}$	0	1	1	1	0	X	X	X	Vector: Range: 0–127
Interrupt Return											
1	00110	$FFFFFE00_{16}$	0	1	1	1	0	X	X	X	Vector: Same as in Previous Int. Ack. Cycle
D. Vectored Interrupt Sequences: Cascaded											
Interrupt Acknowledge											
1	00100	$FFFFFE00_{16}$	0	1	1	1	0	X	X	X	Cascade Index: range −16 to −1
(The CPU here uses the Cascade Index to find the Cascade Address)											
2	001101	Cascade Address	0	See Note				Vector, range 16–255; on appropriate byte of data bus.			
Interrupt Return											
1	00110	$FFFFFE00_{16}$	0	1	1	1	0	X	X	X	Cascade Index: Same as in previous Int. Ack. Cycle
(The CPU here uses the Cascade Index to find the Cascade Address)											
2	00111	Cascade Address	0	See Note				X	X	X	X

X = Don't Care

Note: $\overline{BE0}$–$\overline{BE3}$ signals will be activated according to the cascaded ICU address

3.0 Functional Description (Continued)

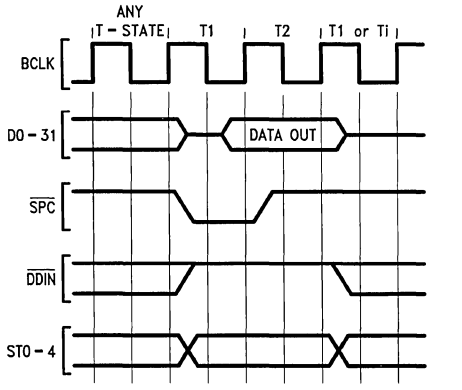

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FIGURE 3-27. Slave Processor Write Cycle

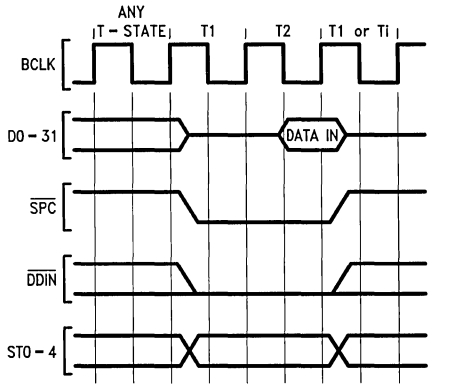

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FIGURE 3-28. Slave Processor Read Cycle

3.5.5 Bus Exceptions

The NS32532 has the capability of handling errors occurring during the execution of a bus cycle. These errors can be either correctable or incorrectable, and the CPU can be notified of their occurrence through the input signals $\overline{BRT}$ and/or $\overline{BER}$.

Bus Retry

If a bus error can be corrected, the CPU may be requested to repeat the erroneous bus cycle. The request is done by asserting the $\overline{BRT}$ signal. $\overline{BRT}$ is sampled at the end of state T2 or T2B.

When the CPU detects that $\overline{BRT}$ is active, it completes the bus cycle normally, but ignores the data read in case of a read cycle, and maintains a copy of the data to be written in case of a write cycle. Then, after a delay of two clock cycles, it will start executing the bus cycle again.

If the transfer cycle is multiple (e.g., for non-aligned data), only the problematic part will be repeated.

For instance, if a non-aligned double-word is being transferred and the second half of the transfer fails, only the second part will be repeated.

The same applies for a retry during a burst sequence. The repeated cycle will begin where the read operation failed (rather than the first address of the burst) and will finish the original burst.

Figures 3-29 and *4-10* (in Section 4) show the $\overline{BRT}$ timing for a basic access cycle and for burst cycles respectively.

The CPU always waits for $\overline{BRT}$ to be HIGH before repeating the bus cycle. While $\overline{BRT}$ is LOW, the CPU places all the output signals shown in *Figure 4-11* in a TRI-STATE® condition.

Bus Error

If a bus error is incorrectable the CPU may be requested to interrupt the current process and branch to an appropriate procedure to handle the error. The request is performed by activating the $\overline{BER}$ signal. $\overline{BER}$ is sampled by the CPU at the end of state T2 or T2B on the rising edge of BCLK. When $\overline{BER}$ is sampled active, the CPU completes the bus cycle normally. If a bus error occurs during a bus cycle for a reference required to execute an instruction, then a bus error exception is recognized. However, if an error occurs during an acknowledge cycle of another exception or during the ICU read cycle of a RETI instruction, the CPU interprets the event as a fatal bus error and enters the 'halted' state.

In this state the CPU floats its address and data buses and places a special status code on the ST0–4 lines. The CPU can exit this condition only through a hardware reset. Refer to Section 3.2.6 for more details on bus error.

Note 1: If the erroneous bus cycle is extended by means of wait states, then the CPU uses the values of $\overline{BRT}$ and/or $\overline{BER}$ sampled during the last wait state.

Note 2: If the CPU samples both $\overline{BRT}$ and $\overline{BER}$ active, $\overline{BRT}$ has higher priority. The bus error indication is ignored, and the bus cycle is repeated.

Note 3: If $\overline{BER}$ is asserted during a bus cycle of a multi-cycle data transfer, the CPU completes the entire transfer normally, but the data will be ignored. The CPU also ignores any subsequent assertion of $\overline{BER}$ during the same data transfer.

Note 4: Neither $\overline{BRT}$ nor $\overline{BER}$ should be asserted during the T2 state of a slave processor bus cycle.

3.5.6 Dynamic Bus Configuration

The NS32532 is tuned to operate with 32-bit wide memory and peripheral devices. The bus also supports 8-bit and 16-bit data widths, but at reduced efficiency. The CPU can switch from one bus width to another dynamically; the only restriction is that the bus width cannot change for locations within an aligned 16-byte block.

The CPU determines the bus width in effect for a bus cycle by using the values of the BW0 and BW1 signals sampled during the last T2 state. Values of BW0 and BW1 sampled before the last T2 state or during T2B states are ignored. Whenever a bus width other than 32-bit is sampled by the CPU, the bus remains idle for 2 clock cycles before the next bus cycle can be initiated.

3.0 Functional Description (Continued)

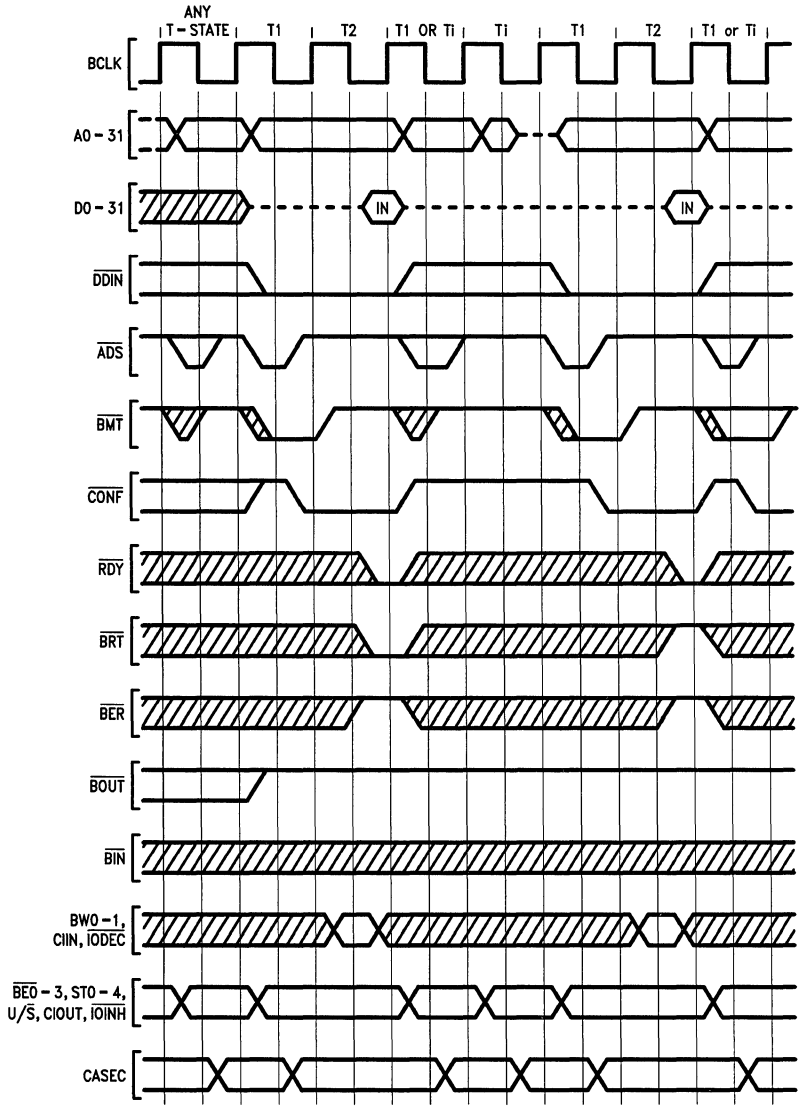

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FIGURE 3-29. Bus Retry During a Basic Read Cycle

3.0 Functional Description (Continued)

The various combinations for BW0 and BW1 are shown below.

BW1	BW0	
0	0	Reserved
0	1	8-Bit Bus
1	0	16-Bit Bus
1	1	32-Bit Bus

The bus width must always be 32 bits during slave cycles. An important feature of the NS32532 is that it does not impose any restrictions on the data alignment, regardless of the bus width.

Bus accesses are performed in double-word units. Accesses of data operands that cross double-word boundaries are decomposed into two or more aligned double-word accesses.

The CPU provides four byte enable signals ($\overline{BE}0-3$) which facilitate individual byte accessing on either a 32-bit or a 16-bit bus.

Figures 3-30 and *3-31* show the basic interfaces for 32-bit and 16-bit memories. An 8-bit memory interface (not shown) is even simpler since it does not use any of the $\overline{BE}0-3$ signals and its single bank is always enabled whenever the memory is selected. Each byte location in this case is selected by address bits A0–31.

The NS32532 does not keep track of the bus width used in previous instruction fetches or data accesses. At the beginning of every memory transaction, the CPU always assumes that the bus is 32-bit wide and the $\overline{BE}0-3$ signals are activated accordingly.

The $\overline{BOUT}$ signal is also asserted during instruction fetches or data reads if the conditions for bursting are satisfied. If the bus is other than 32-bit wide, the $\overline{BIN}$ signal is ignored and $\overline{BOUT}$ is deasserted at the beginning of the T state following T2, since burst cycles are not allowed for 8-bit or 16-bit buses.

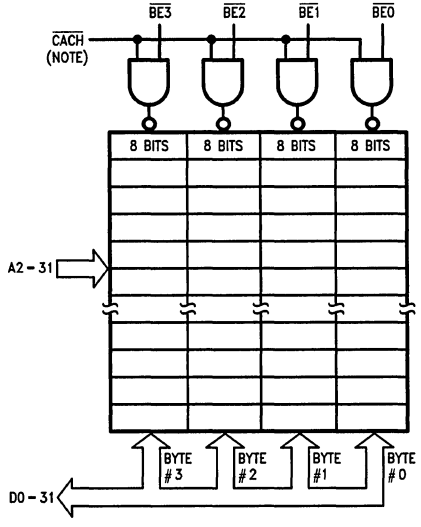

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FIGURE 3-30. Basic Interface for 32-Bit Memories

Note: The $\overline{CACH}$ signal must be asserted during cacheable read accesses.

The following subsections provide detailed descriptions of the access sequences performed in the various cases.

Note: Although the NS32532 ignores the $\overline{BIN}$ signal for 8-bit and 16-bit bus widths, it is recommended that $\overline{BIN}$ be asserted only if the system supports burst transfers. This is to ensure compatibility with future versions of the CPU that might support burst transfers for 8-bit and 16-bit buses.

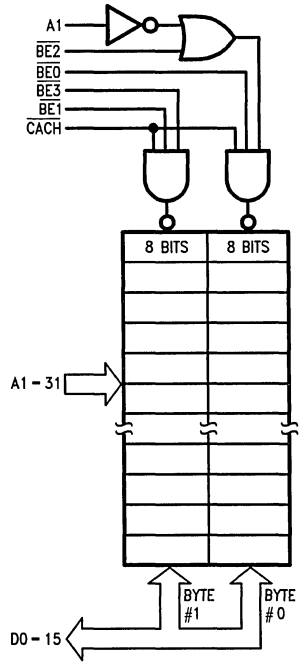

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FIGURE 3-31. Basic Interface for 16-Bit Memories

3.5.6.1 Instruction Fetch Sequences

The CPU performs two types of instruction fetch cycles: sequential and non-sequential. These can be distinguished from each other by the differing status combinations on pins ST0–4. For non-sequential instruction fetches the CPU presents on the address bus the exact byte address of the first instruction in the instruction stream that is about to begin; for sequential instruction fetches, the address of the next aligned instruction double-word is presented on the address bus. The CPU always activates all byte enable signals ($\overline{BE}0-3$) for both sequential and non-sequential fetches. $\overline{BOUT}$ is also asserted during T2 if the addressed double-word is not the last in an aligned 16-byte block. Tables 3-5 to 3-7 show the fetch sequence for the various bus widths.

32-Bit Bus Width

The CPU reads the entire double-word present on the data bus into its internal instruction buffer.

If $\overline{BOUT}$ and $\overline{BIN}$ are both active, the CPU reads up to 3 consecutive double-words using burst cycles. Burst cycles are used for instruction fetches regardless of whether the accesses are cacheable.

3.0 Functional Description (Continued)

Example: JUMP @5

- The CPU performs a fetch cycle at address 5 with $\overline{BE0}$–3 all active.
- Two burst cycles are then performed and addresses 8 and 12 are output while $\overline{BE0}$–3 are kept active.

16-Bit Bus Width

The word on the least-significant half of the data bus is read by the CPU. This is either the even or the odd word within the required instruction double-word, as determined by address bit 1.

The CPU then complements address bit 1, clears address bit 0 and initiates a bus cycle to read the other word, while keeping all the $\overline{BE0}$–3 signals active.

These two words are then assembled into a double-word and transferred into the instruction buffer.

In case of a non-sequential fetch, if the access is not cacheable and the instruction address selects the odd word within the instruction double-word, the even word is not fetched.

Example JUMP @6

- A fetch cycle is performed at address 6 with $\overline{BE0}$–3 all active.
- The word at address 4 is then fetched if the access is cacheable.

8-Bit Bus Width

The instruction byte on the bus lines D0–7 is fetched. The CPU performs three consecutive cycles to read the remaining bytes within the required double-word, while keeping $\overline{BE0}$–3 all active. The 4 bytes are then assembled into a double-word and transferred into the instruction buffer. For a non-sequential fetch, if the access is not cacheable, the CPU will only read the upper bytes within the instruction double-word starting with the byte at the instruction address.

Example: JUMP @7

- The CPU performs a fetch cycle at address 7 with $\overline{BE0}$–3 all active.
- Bytes at addresses 4, 5 and 6 are then fetched consecutively if the access is cacheable.

TABLE 3-5. Cacheable/Non-Cacheable Instruction Fetches from a 32-Bit Bus

1. In a burst access four bytes are fetched with the L.S. bits of the address set to 00.
2. A 'C' on the data bus refers to cacheable fetches and indicates that the byte is placed in the instruction cache. An 'I' refers to non-cacheable fetches and indicates that the byte is ignored.

Number of Bytes	Address LSB	Bytes to be Fetched				Address Bus	$\overline{BE0}$–3	Data Bus			
1	11	B0	—	—	—	A	LLLL	B0	C/I	C/I	C/I
2	10	B1	B0	—	—	A	LLLL	B1	B0	C/I	C/I
3	01	B2	B1	B0	—	A	LLLL	B2	B1	B0	C/I
4	00	B3	B2	B1	B0	A	LLLL	B3	B2	B1	B0

TABLE 3-6. Cacheable/Non-Cacheable Instruction Fetches from a 16-Bit Bus

1. A bus access marked with '*' in the 'Address Bus' column is performed only if the fetch is cacheable.

Number of Bytes	Address LSB	Bytes to be Fetched				Address Bus	$\overline{BE0}$–3	Data Bus			
1	11	B0	—	—	—	A *A − 3	LLLL LLLL	— —	— —	B0 C	C/I C
2	10	B1	B0	—	—	A *A − 2	LLLL LLLL	— —	— —	B1 C	B0 C
3	01	B2	B1	B0	—	A A + 1	LLLL LLLL	— —	— —	B0 B2	C/I B1
4	00	B3	B2	B1	B0	A A + 2	LLLL LLLL	— —	— —	B1 B3	B0 B2

3.0 Functional Description (Continued)

TABLE 3-7. Cacheable/Non-Cacheable Instruction Fetches from an 8-Bit Bus

Number of Bytes	Address LSB	Bytes to be Fetched				Address Bus	$\overline{BE}$0–3	Data Bus			
1	11	B0	—	—	—	A	LLLL	—	—	—	B0
						*A − 3	LLLL	—	—	—	C
						*A − 2	LLLL	—	—	—	C
						*A − 1	LLLL	—	—	—	C
2	10	B1	B0	—	—	A	LLLL	—	—	—	B0
						A + 1	LLLL	—	—	—	B1
						*A − 2	LLLL	—	—	—	C
						*A − 1	LLLL	—	—	—	C
3	01	B2	B1	B0	—	A	LLLL	—	—	—	B0
						A + 1	LLLL	—	—	—	B1
						A + 2	LLLL	—	—	—	B2
						*A − 1	LLLL	—	—	—	C
4	00	B3	B2	B1	B0	A	LLLL	—	—	—	B0
						A + 1	LLLL	—	—	—	B1
						A + 2	LLLL	—	—	—	B2
						A + 3	LLLL	—	—	—	B3

3.5.6.2 Data Read Sequences

The CPU starts a data read access by placing the exact address of the operand on the address bus. The byte enable lines are activated to select only the bytes required by the instruction being executed. This prevents spurious accesses to peripheral devices that might be sensitive to read accesses, such as those which exhibit the characteristic of destructive reading. If the on-chip data cache is internally enabled for the read access, the $\overline{BOUT}$ signal is asserted at the beginning of state T2. $\overline{BOUT}$ will be deasserted if the data cache is externally inhibited (through CIIN or $\overline{IODEC}$), or the bus width is other than 32 bits. During cacheable accesses the CPU always reads all the bytes in the double-word, whether or not they are needed to execute the instruction, and stores them into the data cache. The external memory, in this case, must place the data on the bus regardless of the state of the byte enable signals.

If the data cache is either internally or externally inhibited during the access, the CPU ignores the bytes not selected by the $\overline{BE}$0–3 signals. Data read sequences for the various bus widths are shown in tables 3-8 to 3-10.

32-Bit Bus Width

The entire double-word present on the bus is read by the CPU. If the access is cacheable and the memory allows burst accesses, the CPU reads up to 3 additional double-words within the aligned 16-byte block containing the first byte of the operand. These burst accesses are performed in a wrap-around fashion within the 16-byte block.

Example: MOVW @5, R0

- The CPU reads a double-word at address 5 while keeping $\overline{BE}$1 and $\overline{BE}$2 active.
- If the access is not-cacheable, $\overline{BOUT}$ is deasserted and the data bytes 0 and 3 are ignored.
- If the access is cacheable, the CPU performs burst cycles with $\overline{BE}$0–3 all active, to read the double-words at addresses 8, 12, and 0.

16-Bit Bus Width

The word on the least-significant half of the data bus is read by the CPU. The CPU can then perform another access cycle with address bit 1 complemented and address bit 0 cleared to read the other word within the addressed double-word.

If the access is cacheable, the entire double-word is read and stored into the cache.

If the access is not cacheable, the CPU ignores the bytes in the double-word not selected by $\overline{BE}$0–3. In this case, the second access cycle is not performed, unless selected bytes are contained in the second word.

Example: MOVB @5, R0

- The CPU reads a word at address 5 while keeping $\overline{BE}$1 active.
- If the access is not cacheable, the CPU ignores byte 0.
- If the access is cacheable, the CPU performs another access cycle, with $\overline{BE}$0–3 all active, to read the word at address 6.

8-Bit Bus Width

The data byte on the bus lines D0–7 is read by the CPU. The CPU can then perform up to 3 access cycles to read the remaining bytes in the double-word.

If the access is cacheable, the entire double-word is read and stored into the cache.

If the access is not cacheable, the CPU will only perform those access cycles needed to read the selected bytes.

Example: MOVW @5, R0

- The CPU reads the byte at address 5 while keeping $\overline{BE}$1 and $\overline{BE}$2 active.
- If the access is not cacheable, the CPU activates $\overline{BE}$2 and reads the byte at address 6.
- If the access is cacheable, the CPU performs three bus cycles with $\overline{BE}$0–3 all active, to read the bytes at addresses 6, 7 and 4.

3.0 Functional Description (Continued)

TABLE 3-8. Cacheable/Non-Cacheable Data Reads from a 32-Bit Bus

1. In a burst access four bytes are read with the L.S. bits of the address set to 00.
2. A 'C' on the data bus refers to cacheable reads and indicates that the byte is placed in the data cache. An 'I' refers to non-cacheable reads and indicates that the byte is ignored.

Number of Bytes	Address LSB	Bytes to be Read				Address Bus	$\overline{BE}$0–3	Data Bus			
1	00	—	—	—	B0	A	HHHL	C/I	C/I	C/I	B0
1	01	—	—	B0	—	A	HHLH	C/I	C/I	B0	C/I
1	10	—	B0	—	—	A	HLHH	C/I	B0	C/I	C/I
1	11	BO	—	—	—	A	LHHH	B0	C/I	C/I	C/I
2	00	—	—	B1	B0	A	HHLL	C/I	C/I	B1	B0
2	01	—	B1	B0	—	A	HLLH	C/I	B1	B0	C/I
2	10	B1	B0	—	—	A	LLHH	B1	B0	C/I	C/I
3	00	—	B2	B1	B0	A	HLLL	C/I	B2	B1	B0
3	01	B2	B1	B0	—	A	LLLH	B2	B1	B0	C/I
4	00	B3	B2	B1	B0	A	LLLL	B3	B2	B1	B0

TABLE 3-9. Cacheable/Non-Cacheable Data Reads from a 16-Bit Bus

1. A bus access marked with '*' in the 'Address Bus' column is performed only if the read is cacheable.

Number of Bytes	Address LSB	Data to be Read				Address Bus	$\overline{BE}$0–3		Data Bus			
							Cach.	Non Cach.				
1	00	—	—	—	B0	A *A + 2	HHHL LLLL	HHHL	— —	— —	C/I C	B0 C
1	01	—	—	B0	—	A *A + 1	HHLH LLLL	HHLH	— —	— —	B0 C	C/I C
1	10	—	B0	—	—	A *A − 2	HLHH LLLL	HLHH	— —	— —	C/I C	B0 C
1	11	B0	—	—	—	A *A − 3	LHHH LLLL	LHHH	— —	— —	B0 C	C/I C
2	00	—	—	B1	B0	A *A + 2	HHLL LLLL	HHLL	— —	— —	B1 C	B0 C
2	01	—	B1	B0	—	A A + 1	HLLH LLLL	HLLH HLHH	— —	— —	B0 C/I	C/I B1
2	10	B1	B0	—	—	A *A − 2	LLHH LLLL	LLHH	— —	— —	B1 C	B0 C
3	00	—	B2	B1	B0	A A + 2	HLLL LLLL	HLLL HLHH	— —	— —	B1 C/I	B0 B2
3	01	B2	B1	B0	—	A A + 1	LLLH LLLL	LLLH LLHH	— —	— —	B0 B2	C/I B1
4	00	B3	B2	B1	B0	A A + 2	LLLL LLLL	LLLL LLHH	— —	— —	B1 B3	B0 B2

3.0 Functional Description (Continued)

TABLE 3-10. Cacheable/Non-Cacheable Data Reads from an 8-Bit Bus D8–12

Number of Bytes	Address LSB	Data to be Read				Address Bus	$\overline{BE}$0–3		Data Bus			
							Cach.	Non Cach.				
1	00	—	—	—	B0	A	HHHL	HHHL	—	—	—	B0
						*A + 1	LLLL		—	—	—	C
						*A + 2	LLLL		—	—	—	C
						*A + 3	LLLL		—	—	—	C
1	01	—	—	B0	—	A	HHLH	HHLH	—	—	—	B0
						*A + 1	LLLL		—	—	—	C
						*A + 2	LLLL		—	—	—	C
						*A − 1	LLLL		—	—	—	C
1	10	—	B0	—	—	A	HLHH	HLHH	—	—	—	B0
						*A + 1	LLLL		—	—	—	C
						*A − 2	LLLL		—	—	—	C
						*A − 1	LLLL		—	—	—	C
1	11	B0	—	—	—	A	LHHH	LHHH	—	—	—	B0
						*A − 3	LLLL		—	—	—	C
						*A − 2	LLLL		—	—	—	C
						*A − 1	LLLL		—	—	—	C
2	00	—	—	B1	B0	A	HHLL	HHLL	—	—	—	B0
						A + 1	LLLL	HHLH	—	—	—	B1
						*A + 2	LLLL		—	—	—	C
						*A + 3	LLLL		—	—	—	C
2	01	—	B1	B0	—	A	HLLH	HLLH	—	—	—	B0
						A + 1	LLLL	HLHH	—	—	—	B1
						*A + 2	LLLL		—	—	—	C
						*A − 1	LLLL		—	—	—	C
2	10	B1	B0	—	—	A	LLHH	LLHH	—	—	—	B0
						A + 1	LLLL	LHHH	—	—	—	B1
						*A − 2	LLLL		—	—	—	C
						*A − 1	LLLL		—	—	—	C
3	00	—	B2	B1	B0	A	HLLL	HLLL	—	—	—	B0
						A + 1	LLLL	HLLH	—	—	—	B1
						A + 2	LLLL	HLHH	—	—	—	B2
						*A + 3	LLLL		—	—	—	C
3	01	B2	B1	B0	—	A	LLLH	LLLH	—	—	—	B0
						A + 1	LLLL	LLHH	—	—	—	B1
						A + 2	LLLL	LHHH	—	—	—	B2
						*A − 1	LLLL		—	—	—	C
4	00	B3	B2	B1	B0	A	LLLL	LLLL	—	—	—	B0
						A + 1	LLLL	LLLH	—	—	—	B1
						A + 2	LLLL	LLHH	—	—	—	B2
						A + 3	LLLL	LHHH	—	—	—	B3

3.5.6.3 Data Write Sequences

In a write access the CPU outputs the operand address and asserts only the byte enable lines needed to select the specific bytes to be written.

In addition, the CPU duplicates the data to be written on the appropriate bytes of the data bus in order to handle 8-bit and 16-bit buses.

The various access sequences as well as the duplication of data are summarized in tables 3-11 to 3-13.

32-Bit Bus Width

The CPU performs only one access cycle to write the selected bytes within the addressed double-word.

Example: MOVB R0, @6

- The CPU duplicates byte 2 of the data bus into byte 0 and performs a write cycle at address 6 with $\overline{BE}$2 active.

16-Bit Bus Width

Up to two access cycles are needed to complete the write operation.

3.0 Functional Description (Continued)

Example: MOVW R0, @5

- The CPU duplicates byte 1 of the data bus into byte 0 and performs a write cycle at address 5 with $\overline{BE}1$ and $\overline{BE}2$ active.
- A write at address 6 is then performed with $\overline{BE}2$ active and the original byte 2 of the data bus placed on byte 0.

8-Bit Bus Width

Up to 4 access cycles are needed in this case to complete the write operation.

Example: MOVB R0, @7

- The CPU duplicates byte 3 of the data bus into bytes 0 and 1, and then performs a write cycle at address 7 with $\overline{BE}3$ active.

3.5.7 Bus Access Control

The NS32532 has the capability of relinquishing its control of the bus upon request from a DMA device or another CPU. This capability is implemented with the $\overline{HOLD}$ and $\overline{HLDA}$ signals. By asserting $\overline{HOLD}$, an external device requests access to the bus. On receipt of $\overline{HLDA}$ from the CPU, the device may perform bus cycles, as the CPU at this point has placed all the output signals shown in *Figure 3-32* into the TRI-STATE condition.

To return control of the bus to the CPU, the external device sets $\overline{HOLD}$ inactive, and the CPU acknowledges return of the bus by setting $\overline{HLDA}$ inactive.

The CPU samples $\overline{HOLD}$ in the middle of each T-state on the falling edge of BCLK. If $\overline{HOLD}$ is asserted when the bus is idle between access sequences, then the bus is granted immediately (see *Figure 3-31*). If $\overline{HOLD}$ is asserted during an access sequence, then the bus is granted immediately after the access sequence, including any retried bus cycles, has completed (see *Figure 4-13*). Note that an access sequence can be composed of several bus cycles if the bus width is 8 or 16 bits.

TABLE 3-11. Data Writes to a 32-Bit Bus

1. Bytes on the data bus marked with '•' are undefined.

Number of Bytes	Address LSB	Data to be Written				Address Bus	$\overline{BE}$0–3	Data Bus			
1	00	—	—	—	B0	A	HHHL	•	•	•	B0
1	01	—	—	B0	—	A	HHLH	•	•	B0	B0
1	10	—	B0	—	—	A	HLHH	•	B0	•	B0
1	11	B0	—	—	—	A	LHHH	B0	•	B0	B0
2	00	—	—	B1	B0	A	HHLL	•	•	B1	B0
2	01	—	B1	B0	—	A	HLLH	•	B1	B0	B0
2	10	B1	B0	—	—	A	LLHH	B1	B0	B1	B0
3	00	—	B2	B1	B0	A	HLLL	•	B2	B1	B0
3	01	B2	B1	B0	—	A	LLLH	B2	B1	B0	B0
4	00	B3	B2	B1	B0	A	LLLL	B3	B2	B1	B0

TABLE 3-12. Data Writes to a 16-Bit Bus

Number of Bytes	Address LSB	Data to be Written				Address Bus	$\overline{BE}$0–3	Data Bus			
1	00	—	—	—	B0	A	HHHL	•	•	•	B0
1	01	—	—	B0	—	A	HHLH	•	•	B0	B0
1	10	—	B0	—	—	A	HLHH	•	B0	•	B0
1	11	B0	—	—	—	A	LHHH	B0	•	B0	B0
2	00	—	—	B1	B0	A	HHLL	•	•	B1	B0
2	01	—	B1	B0	—	A A + 1	HLLH HLHH	• •	B1 •	B0 •	B0 B1
2	10	B1	B0	—	—	A	LLHH	B1	B0	B1	B0
3	00	—	B2	B1	B0	A A + 2	HLLL HLHH	• •	B2 •	B1 •	B0 B2
3	01	B2	B1	B0	—	A A + 1	LLLH LLHH	B2 •	B1 •	B0 B2	B0 B1
4	00	B3	B2	B1	B0	A A + 2	LLLL LLHH	B3 •	B2 •	B1 B3	B0 B2

3.0 Functional Description (Continued)

TABLE 3-13. Data Writes to an 8-Bit Bus

Number of Bytes	Address LSB	Data to be Written				Address Bus	$\overline{BE}0-3$	Data Bus			
1	00	—	—	—	B0	A	HHHL	•	•	•	B0
1	01	—	—	B0	—	A	HHLH	•	•	B0	B0
1	10	—	B0	—	—	A	HLHH	•	B0	•	B0
1	11	B0	—	—	—	A	LHHH	B0	•	B0	B0
2	00	—	—	B1	B0	A A + 1	HHLL HHLH	• •	• •	B1 •	B0 B1
2	01	—	B1	B0	—	A A + 1	HLLH HLHH	• •	B1 •	B0 •	B0 B1
2	10	B1	B0	—	—	A A + 1	LLHH LHHH	B1 •	B0 •	B1 •	B0 B1
3	00	—	B2	B1	B0	A A + 1 A + 2	HLLL HLLH HLHH	• • •	B2 • •	B1 • •	B0 B1 B2
3	01	B2	B1	B0	—	A A + 1 A + 2	LLLH LLHH LHHH	B2 • •	B1 • •	B0 • •	B0 B1 B2
4	00	B3	B2	B1	B0	A A + 1 A + 2 A + 3	LLLL LLLH LLHH LHHH	B3 • • •	B2 • • •	B1 • • •	B0 B1 B2 B3

2

3.0 Functional Description (Continued)

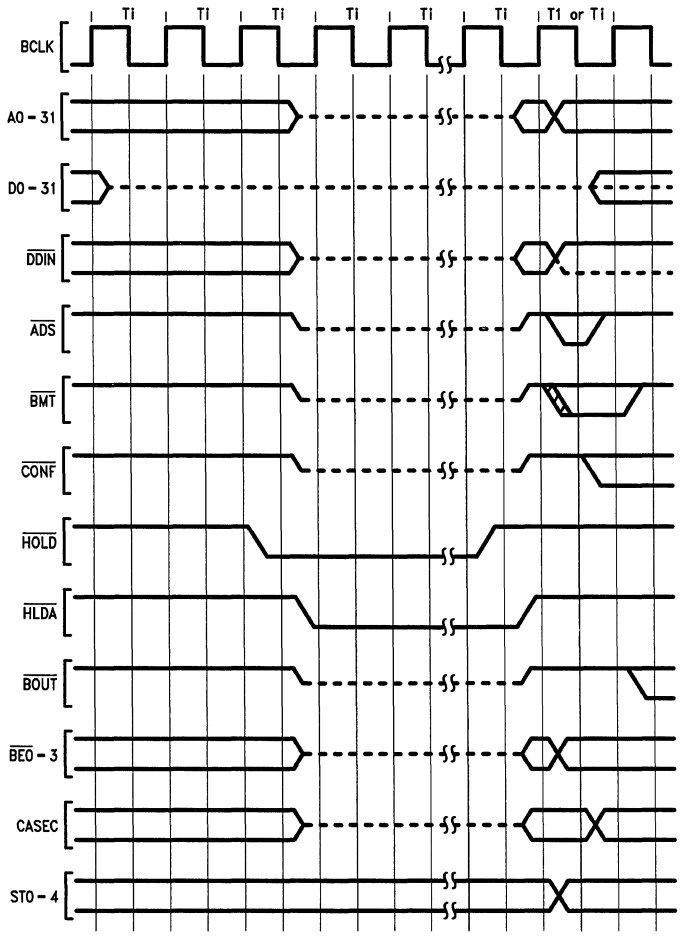

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FIGURE 3-32. Hold Acknowledge. (Bus Initially Idle.)

Note: The status indicates 'IDLE' while the bus is granted. If the cause of the IDLE changes (e.g., CPU starts waiting for an interrupt), the status also changes.

The CPU will never grant the bus between interlocked read and write bus cycles.

Note: If an external device requires a very short latency to get control of the bus, the bus retry signal ($\overline{BRT}$) can be used instead of hold. See Section 3.5.5.

3.5.8 Interfacing Memory-Mapped I/O Devices

In Section 3.1.3.2 it was mentioned that some special precautions are needed when interfacing I/O devices to the NS32532 due to its internal pipelined implementation. Two special signals are provided for this purpose: $\overline{IOINH}$ and $\overline{IODEC}$. The CPU asserts $\overline{IOINH}$ during a read bus cycle to indicate that the bus cycle should be ignored if an I/O device is selected. The system responds by asserting $\overline{IODEC}$ to indicate to the CPU that an I/O device has been selected. $\overline{IODEC}$ is sampled by the CPU in the middle of state T2. If the cycle is extended, then the CPU uses the $\overline{IODEC}$ value sampled during the last wait state. If a bus error or a bus retry occurs, the sampled $\overline{IODEC}$ value is ignored. $\overline{IODEC}$ must be kept high during burst transfer cycles.

When $\overline{IODEC}$ is active during a bus cycle for which $\overline{IOINH}$ is asserted, the CPU discards the data and applies the special handling required for I/O devices. *Figure 3-33* shows a possible implementation of an I/O device interface where the address mapping of the I/O devices is fixed.

In an open system configuration, $\overline{IODEC}$ could be generated by the decoding logic of each I/O device subsystem.

When the on-chip MMU is enabled, the CIOUT signal could also be used for this purpose, since I/O devices are located in noncacheable areas. In this case however, a small performance degradation could result, due to the fact that the special I/O handling is also applied on references to noncacheable program and/or data areas.

Note 1: When $\overline{IODEC}$ is active in response to a read bus cycle, the CPU treats the reference as noncacheable.

Note 2: $\overline{IOINH}$ is kept inactive during write cycles.

3.0 Functional Description (Continued)

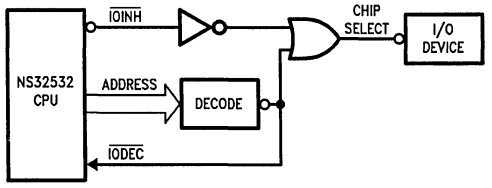

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FIGURE 3-33. Typical I/O Device Interface

3.5.9 Interrupt and Debug Trap Requests

Three signals are provided by the CPU to externally request interrupts and/or a debug trap. $\overline{INT}$ and $\overline{NMI}$ are for maskable and non-maskable interrupts respectively. $\overline{DBG}$ is used for requesting an external debug trap.

The CPU samples $\overline{INT}$ and $\overline{NMI}$ on every other rising edge of BCLK, starting with the second rising edge of BCLK after $\overline{RST}$ goes high.

$\overline{NMI}$ is edge-sensitive; a high-to-low transition on it is detected by the CPU and stored in an internal latch, so that there is no need to keep it asserted until it is acknowledged.

$\overline{INT}$ is level-sensitive and, as such, once asserted, it must be kept asserted until it is acknowledged.

The $\overline{DBG}$ signal, like $\overline{NMI}$, is edge-sensitive; it differs from $\overline{NMI}$ in that the CPU samples it on each rising edge of BCLK. $\overline{DBG}$ can be asserted asynchronously to the CPU clock, but it should be at least 1.5 clock cycles wide in order to be recognized.

If $\overline{DBG}$ meets the specified setup and hold times, it will be recognized on the rising edge of BCLK deterministically.

Refer to *Figures 4-19* and *4-20* for more details on the timing of the above signals.

Note: If the $\overline{NMI}$ signal is pulsed to request a non-maskable interrupt, it may be necessary to keep it asserted for a minimum of two clock cycles to guarantee its detection, unless extra logic ensures that the pulse occurs around the BCLK sampling edge.

3.5.10 Cache Invalidation Requests

The contents of the on-chip Instruction and Data Caches can be invalidated by external requests from the system. It is possible to invalidate a single set or all sets in the Instruction Cache, Data Cache or both. The input signals $\overline{INVIC}$ and $\overline{INVDC}$ request invalidation of the Instruction Cache and Data Cache respectively. The input signal $\overline{INVSET}$ indicates whether the invalidation applies to a single set (16 bytes for the Instruction Cache and 32 bytes for the Data Cache) or to the entire cache. When only a single set is invalidated, the set number is specified on CIA0–CIA6.

$\overline{INVIC}$, $\overline{INVDC}$, $\overline{INVSET}$ and CIA0–CIA6 are all sampled synchronously by the CPU on the rising edge of BCLK. The CPU can respond to cache invalidation requests at a rate of one per BCLK cycle.

As shown in *Figures 3-16* and *3-17*, the validity bits of the on-chip caches are dual-ported. One port is used for accessing and updating the caches, while the other port is used independently for invalidation requests. Consequently, invalidation of the on-chip caches occurs with no interference to on-going cache accesses or bus cycles.

A cache invalidation request can occur during a read bus cycle for a location affected by the invalidation. In such a case, the data will be invalid in the cache if the invalidation request occurs during or after the T2- or T2B-state of the bus cycle.

Refer to *Figure 4-18* in Section 4 for timing details.

3.5.11 Internal Status

The NS32532 provides information on the system interface concerning its internal activity.

The U/$\overline{S}$ signal indicates the Address Space for a memory reference (See Section 2.4.2).

Note that U/$\overline{S}$ does not necessarily reflect the value of the U bit in the PSR register. For example, U/$\overline{S}$ is high during the memory access used to store the destination operand of a MOVSU instruction.

The $\overline{PFS}$ signal is asserted for one BCLK cycle when the CPU begins executing a new instruction. The $\overline{ISF}$ signal is driven High along with $\overline{PFS}$ if the new instruction does not follow the previous instruction in sequence. More specifically, $\overline{ISF}$ is High along with $\overline{PFS}$ after processing an exception or after executing one of the following instructions: ACB (branch taken), Bcond (branch taken), BR, BSR, CASE, CXP, CXPD, DIA, JSR, JUMP, RET, RETT, RETI, and RXP.

The $\overline{BP}$ signal is asserted for one BCLK cycle when an address-compare or PC-match condition is detected. If the $\overline{BP}$ signal is asserted one BCLK cycle after $\overline{PFS}$, it indicates that an address-compare debug condition has been detected. If $\overline{BP}$ is asserted at any other time, it indicates that a PC-Match debug condition has been detected.

While executing an LMR or CINV instruction, the CPU displays the operation code and source operand using slave processor write bus cycles. This information can be used to monitor the contents of the on-chip TLB, Instruction Cache and Data Cache.

During idle bus cycles, the signals ST0–ST4 indicate whether the CPU is waiting for an interrupt, waiting for a Slave Processor to complete executing an instruction or halted.

4.0 Device Specifications

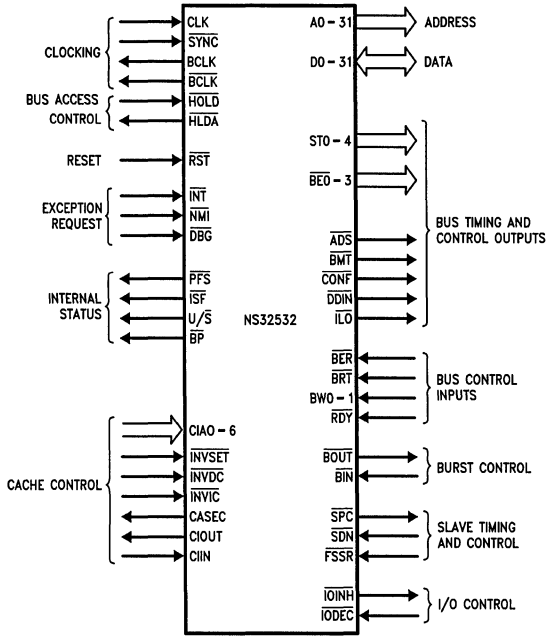

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FIGURE 4-1. NS32532 Interface Signals

4.1 NS32532 PIN DESCRIPTIONS

Descriptions of the NS32532 pins are given in the following sections.

Included are also references to portions of the functional description, Section 3.

Figure 4-1 shows the NS32532 interface signals grouped according to related functions.

Note: An asterisk next to the signal name indicates a TRI-STATE condition for that signal when HOLD is acknowledged or during an extended retry.

4.1.1 Supplies

VCCL1-6 **Logic Power.**
+5V positive supplies for on-chip logic.

VCCB1-14 **Buffers Power.**
+5V positive supplies for on-chip output buffers.

VCCCLK **Bus Clock Power.**
+5V positive supply for on-chip clock drivers.

GNDL1-6 **Logic Ground.**
Ground references for on-chip logic.

GNDB1-13 **Buffers Ground.**
Ground references for on-chip output buffers.

GNDCLK **Bus Clock Ground.**
Ground reference for on-chip clock drivers.

4.1.2 Input Signals

CLK **Clock.**
Input Clock used to derive all CPU Timing.

SYNC **Synchronize.**
When SYNC is active, BCLK will stop toggling. This signal can be used to synchronize two or more CPUs (Section 3.5.2).

HOLD **Hold Request.**
When active, causes the CPU to release the bus for DMA or multiprocessing purposes (Section 3.5.7).

Note:
If the HOLD signal is generated asynchronously, its set up and hold times may be violated. In this case it is recommended to synchronize it with CLK to minimize the possibility of metastable states.

The CPU provides only one synchronization stage to minimize the HLDA latency. This is to avoid speed degradations in cases of heavy HOLD activity (i.e. DMA controller cycles interleaved with CPU cycles).

RST **Reset.**
When RST is active, the CPU is initialized to a known state (Section 3.5.3).

INT **Interrupt.**
A low level on this signal requests a maskable interrupt (Section 3.5.9).

NMI **Nonmaskable Interrupt.**
A High-to-Low transition of this signal requests a nonmaskable interrupt (Section 3.5.9).

4.0 Device Specifications (Continued)

$\overline{DBG}$ **Debug Trap Request.**

A High-to-Low transition of this signal requests a debug trap (Section 3.5.9).

CIA0–6 **Cache Invalidation Address Bus.**

Bits 0 through 4 specify the set address to invalidate in the on-chip caches. CIA0 is the least significant. Bits 5 and 6 are reserved (Section 3.5.10).

$\overline{INVSET}$ **Invalidate Set.**

When Low, only a set in the on-chip cache(s) is invalidated; when High, the entire cache(s) is (are) invalidated.

$\overline{INVDC}$ **Invalidate Data Cache.**

When Low, the Data Cache contents are invalidated. $\overline{INVSET}$ determines whether a single set or the entire Data Cache is invalidated.

$\overline{INVIC}$ **Invalidate Instruction Cache.**

When Low, the Instruction Cache contents are invalidated. $\overline{INVSET}$ determines whether a single set or the entire Instruction Cache is invalidated.

CIIN **Cache Inhibit In.**

When active, indicates that the location referenced in the current bus cycle is not cacheable. CIIN must not change within an aligned 16-byte block.

$\overline{IODEC}$ **I/O Decode.**

Indicates to the CPU that a peripheral device is addressed by the current bus cycle. The value of $\overline{IODEC}$ must not change within an aligned 16-byte block (Section 3.5.8).

$\overline{FSSR}$ **Force Slave Status Read.**

When asserted, indicates that the slave status word should be read by the CPU (Section 3.1.4.1). An external 10 kΩ resistor should be connected between $\overline{FSSR}$ and V_{CC}.

$\overline{SDN}$ **Slave Done.**

Used by a slave processor to signal the completion of a slave instruction (Section 3.1.4.1). An external 10 kΩ resistor should be connected between $\overline{SDN}$ and V_{CC}.

$\overline{BIN}$ **Burst In.**

When active, indicates to the CPU that the memory supports burst cycles (Section 3.5.4.3).

$\overline{RDY}$ **Ready.**

While this signal is not active, the CPU extends the current bus cycle to support a slow memory or peripheral device.

BW0–1 **Bus Width.**

These lines define the bus width (8, 16 or 32 bits) for each data transfer; BW0 is the least significant bit. The bus width must not change within an aligned 16-byte block—encodings are:

00—Reserved

01—8 Bits

10—16 Bits

11—32 Bits

$\overline{BRT}$ **Bus Retry.**

When active, the CPU will reexecute the last bus cycle (Section 3.5.5).

$\overline{BER}$ **Bus Error.**

When active, indicates that an error occurred during a bus cycle. It is treated by the CPU as the highest priority exception after reset.

4.1.3 Output Signals

BCLK **Bus Clock.**

Output clock for bus timing (Section 3.5.2).

$\overline{BCLK}$ **Bus Clock Inverse.**

Inverted output clock.

$\overline{HLDA}$ **Hold Acknowledge.**

Activated by the CPU in response to the $\overline{HOLD}$ input to indicate that the CPU has released the bus.

$\overline{PFS}$ **Program Flow Status.**

A pulse on this signal indicates the beginning of execution for each instruction (Section 3.5.11).

$\overline{ISF}$ **Internal Sequential Fetch.**

Indicates along with $\overline{PFS}$ that the instruction beginning execution is sequential ($\overline{ISF}$ Low) or non-sequential ($\overline{ISF}$ High).

U/$\overline{S}$ **User/Supervisor.**

User or supervisor mode status.

$\overline{BP}$ **Break Point.**

This signal is activated when the CPU detects a PC or operand-address match debug condition (Section 3.3.2).

CASEC ***Cache Section.**

For cacheable data read bus cycles indicates the Section of the on-chip Data Cache where the data will be placed; undefined for other bus cycles. This signal can be used for external monitoring of the data cache contents.

CIOUT **Cache Inhibit Out.**

This signal reflects the state of the CI bit in the second level page table entry (PTE). It is used to specify non-cacheable pages. It is held low while address translation is disabled and for MMU references to page table entries.

$\overline{IOINH}$ **I/O Inhibit.**

Indicates that the current bus cycle should be ignored if a peripheral device is addressed.

$\overline{SPC}$ **Slave Processor Control.**

Data strobe for slave processor transfers.

$\overline{BOUT}$ ***Burst Out.**

When active, indicates that the CPU is requesting to perform burst cycles.

$\overline{ILO}$ **Interlocked Operation.**

When active, indicates that interlocked cycles are being performed (Section 3.5.4.5).

4.0 Device Specifications (Continued)

$\overline{DDIN}$ ***Data Direction.**

Indicates the direction of a data transfer. It is low for reads and high for writes.

$\overline{CONF}$ ***Confirm Bus Cycle.**

When active, indicates that a bus cycle initiated by $\overline{ADS}$ is valid; that is, the bus cycle has not been cancelled (Section 3.5.4.2).

$\overline{BMT}$ ***Begin Memory Transaction.**

When Stable Low indicates that the current bus cycle is valid; that is, the bus cycle has not been cancelled (Section 3.5.4.2).

$\overline{ADS}$ ***Address Strobe.**

When active, indicates that a bus cycle has begun and a valid address is on the address bus.

$\overline{BE}$0-3 ***Byte Enables.**

Used to selectively enable data transfers on bytes 0–3 of the data bus.

ST0-4 **Status.**

Bus cycle status code; ST0 is the least significant. Encodings are:

00000—Idle: CPU Inactive on Bus.

00001—Idle: WAIT Instruction.

00010—Idle: Halted.

00011—Idle: The bus is idle while the slave processor is executing an instruction.

00100—Interrupt Acknowledge, Master.

00101—Interrupt Acknowledge, Cascaded.

00110—End of Interrupt, Master.

00111—End of Interrupt, Cascaded.

01000—Sequential Instruction Fetch.

01001—Non-Sequential Instruction Fetch.

01010—Data Transfer.

01011—Read Read-Modify-Write Operand.

01100—Read for Effective Address.

01101—Access PTE1 by MMU.

01110—Access PTE2 by MMU.

01111 • • • 11100 } Reserved.

11101—Transfer Slave Operand.

11110—Read Slave Status Word.

11111—Broadcast Slave ID.

A0-31 ***Address Bus.**

Used by the CPU to output a 32-bit address at the beginning of a bus cycle. A0 is the least significant.

4.1.4 Input/Output Signals

D0-31 ***Data Bus.**

Used by the CPU to input or output data during a read or write cycle respectively.

4.2 ABSOLUTE MAXIMUM RATINGS

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Temperature Under Bias	0°C to +70°C
Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to GND	−0.5V to +7V
Power Dissipation	4 W

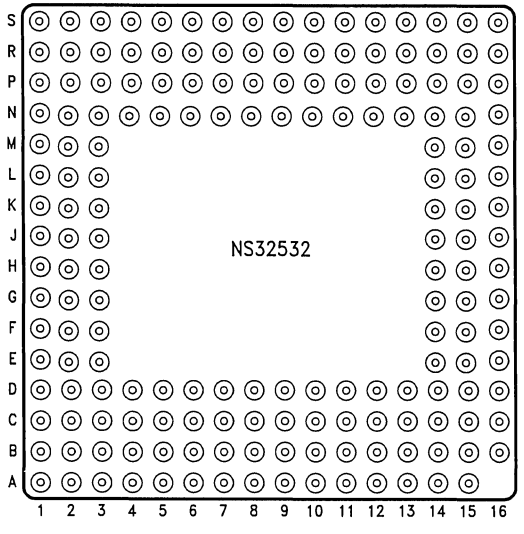
Note: *Absolute maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended; operation should be limited to those conditions specified under Electrical Characteristics.*

4.3 ELECTRICAL CHARACTERISTICS T_A = 0° to +70°C, V_{CC} = 5V ±5%, GND = 0V

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High Level Input Voltage		2.0		V_{CC} + 0.5	V
V_{IL}	Low Level Input Voltage		−0.5		0.8	V
V_{OH}	High Level Output Voltage	I_{OH} = −400 μA	2.4			V
V_{OL}	Low Level Output Voltage					
	A0–11, D0–31, $\overline{DDIN}$	I_{OL} = 4 mA			0.4	V
	$\overline{CONF}$, $\overline{BMT}$	I_{OL} = 6 mA			0.4	V
	BCLK, $\overline{BCLK}$	I_{OL} = 16 mA			0.4	V
	All Other Outputs	I_{OL} = 2 mA			0.4	V
I_L	Input Load Current	0 ≤ V_{IN} ≤ V_{CC}	−20		20	μA
I_L	Leakage Current (Output and I/O pins in TRI-STATE/Input Mode)	0.4 ≤ V_{IN} ≤ V_{CC}	−20		20	μA
I_{CC}	Active Supply Current	I_{OUT} = 0, T_A = 25°C			750	mA

4.0 Device Specifications (Continued)

Connection Diagram



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Bottom View

FIGURE 4-2. 175-Pin PGA Package

NS32532 Pinout Descriptions

Desc	Pin	Desc	Pin	Desc	Pin
Reserved	A1	D26	B16	GNDB13	D14
Reserved	A2	Reserved	C1	VCCB14	D15
Reserved	A3	Reserved	C2	D23	D16
$\overline{BP}$	A4	VCCL2	C3	$\overline{IOINH}$	E1
$\overline{ISF}$	A5	Reserved	C4	$\overline{ILO}$	E2
$\overline{RST}$	A6	$\overline{PFS}$	C5	GNDB3	E3
$\overline{NMI}$	A7	$\overline{SDN}$	C6	D24	E14
GNDB1	A8	Reserved	C7	D22	E15
Reserved	A9	$\overline{BCLK}$	C8	D20	E16
VCCB2	A10	VCCCLK	C9	A30	F1
$\overline{INVIC}$	A11	$\overline{SYNC}$	C10	$\overline{CASEC}$	F2
Reserved (1)	A12	CIA0	C11	Reserved	F3
CIA1	A13	CIA6	C12	D21	F14
CIA4	A14	VCCL6	C13	D19	F15
VCCB1	A15	D29	C14	D18	F16
Reserved	B1	D27	C15	A29	G1
VCCB4	B2	D25	C16	A31	G2
Reserved	B3	U/$\overline{S}$	D1	VCCB5	G3
Reserved	B4	Reserved	D2	GNDB12	G14
VCCB3	B5	Reserved	D3	D17	G15
$\overline{FSSR}$	B6	GNDL3	D4	D16	G16
$\overline{INT}$	B7	GNDB2	D5	A27	H1
VCCL1	B8	$\overline{DBG}$	D6	A28	H2
GNDL2	B9	Reserved	D7	GNDB4	H3
$\overline{INVSET}$	B10	BCLK	D8	VCCB13	H14
$\overline{INVDC}$	B11	GNDCLK	D9	D15	H15
CIA3	B12	CLK	D10	D14	H16
CIA5	B13	CIA2	D11	A26	J1
D30	B14	D31	D12	A25	J2
D28	B15	GNDL1	D13	A24	J3

Desc	Pin	Desc	Pin	Desc	Pin
GNDL6	J14	GNDL5	N9	A0	R6
VCCL5	J15	$\overline{CONF}$	N10	VCCB9	R7
D13	J16	$\overline{RDY}$	N11	CIOUT	R8
VCCB6	K1	$\overline{HOLD}$	N12	$\overline{SPC}$	R9
A23	K2	VCCB11	N13	$\overline{BE3}$	R10
GNDL4	K3	GNDB10	N14	VCCB10	R11
GNDB11	K14	D4	N15	$\overline{ADS}$	R12
D11	K15	D6	N16	BW1	R13
D12	K16	A16	P1	$\overline{BER}$	R14
A22	L1	VCCB7	P2	CIIN	R15
A21	L2	GNDB6	P3	D2	R16
VCCL3	L3	A10	P4	A13	S1
D8	L14	A6	P5	A8	S2
D9	L15	A2	P6	A5	S3
D10	L16	ST3	P7	A3	S4
A20	M1	GNDB8	P8	A1	S5
GNDB5	M2	VCCL4	P9	ST2	S6
A17	M3	$\overline{BE1}$	P10	ST1	S7
D5	M14	GNDB9	P11	ST0	S8
D7	M15	BW0	P12	$\overline{BOUT}$	S9
VCCB12	M16	$\overline{BIN}$	P13	$\overline{DDIN}$	S10
A19	N1	Reserved	P14	$\overline{BE2}$	S11
A18	N2	D0	P15	$\overline{BE0}$	S12
A14	N3	D3	P16	$\overline{BMT}$	S13
A11	N4	A15	R1	$\overline{BRT}$	S14
VCCB8	N5	A12	R2	$\overline{IODEC}$	S15
GNDB7	N6	A9	R3	D1	S16
ST4	N7	A7	R4		
$\overline{HLDA}$	N8	A4	R5		

Note 1: This pin should be grounded.
All other reserved pins should be left open.

4.0 Device Specifications (Continued)

4.4 SWITCHING CHARACTERISTICS

4.4.1 Definitions

All the timing specifications given in this section refer to 0.8V or 2.0V on all the signals as illustrated below, unless specifically stated otherwise.

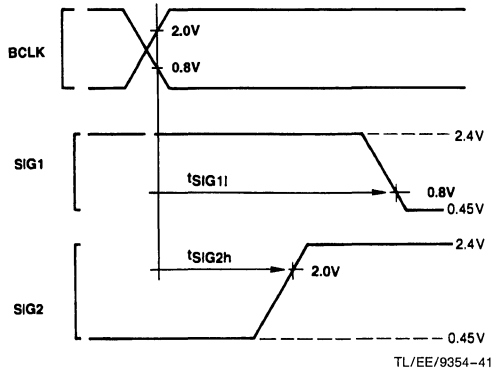

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FIGURE 4-3. Timing Specification Standard (Signal Valid after Clock Edge)

ABBREVIATIONS:

L.E.—leading edge R.E.—rising edge

T.E.—training edge F.E.—falling edge

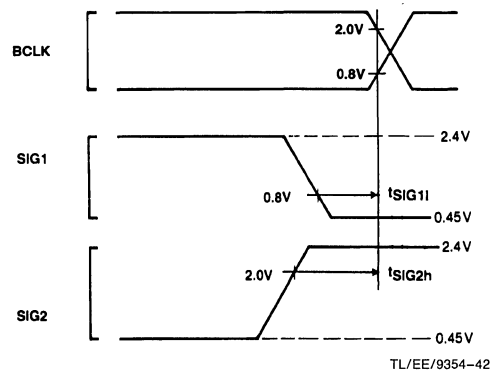

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FIGURE 4-4. Timing Specification Standard (Signal Valid before Clock Edge)

4.4.2 Timing Tables

4.4.2.1 Output Signals: Internal Propagation Delays, NS32532-20, NS32532-25, NS32532-30

Maximum times assume capacitive loading of 100 pF on the clock signals and 50 pF on all the other signals. A minimum capacitance load of 50 pF on BCLK and $\overline{BCLK}$ is also assumed.

Name	Figure	Description	Reference/Conditions	NS32532-20		NS32532-25		NS32532-30		Units
				Min	Max	Min	Max	Min	Max	
t_{BC_p}	4-24	Bus Clock Period	R.E., BCLK to Next R.E., BCLK	50	100	40	100	33.3	100	ns
t_{BC_h}	4-24	BCLK High Time	At 2.0V on BCLK (Both Edges)	0.5 t_{BC_p} −5 ns		0.5 t_{BC_p} −4 ns		0.5 t_{BC_p} −3 ns		
t_{BC_l}	4-24	BCLK Low Time	At 0.8V on BCLK (Both Edges)	0.5 t_{BC_p} −5 ns		0.5 t_{BC_p} −4 ns		0.5 t_{BC_p} −3 ns		
t_{BC_r}	4-24	BCLK Rise Time	0.8V to 2.0V on R.E., BCLK		5		4		3	ns
t_{BC_f}	4-24	BCLK Fall Time	2.0V to 0.8V on F.E., BCLK		5		4		3	ns
t_{NBC_h}	4-24	$\overline{BCLK}$ High Time	At 2.0V on $\overline{BCLK}$ (Both Edges)	0.5 t_{NBC_p} −5 ns		0.5 t_{NBC_p} −4 ns		0.5 t_{NBC_p} −3 ns		
t_{NBC_l}	4-24	$\overline{BCLK}$ Low Time	At 0.8V on $\overline{BCLK}$ (Both Edges)	0.5 t_{NBC_p} −5 ns		0.5 t_{NBC_p} −4 ns		0.5 t_{NBC_p} −3 ns		
t_{NBC_r}	4-24	$\overline{BCLK}$ Rise Time	0.8V to 2.0V on R.E., $\overline{BCLK}$		5		4		3	ns
t_{NBC_f}	4-24	$\overline{BCLK}$ Fall Time	2.0V to 0.8V on F.E., $\overline{BCLK}$		5		4		3	ns
$t_{CBC_{dr}}$	4-24	CLK to BCLK R.E. Delay	2.0V on R.E., CLK to 2.0V on R.E., BCLK		17		14		12	ns
$t_{CBC_{df}}$	4-24	CLK to BCLK F.E. Delay	2.0V on R.E., CLK to 0.8V on F.E., BCLK		17		14		12	ns
$t_{CNBC_{dr}}$	4-24	CLK to $\overline{BCLK}$ R.E. Delay	2.0V on R.E., CLK to 0.8V on R.E., $\overline{BCLK}$		17		14		12	ns

4.0 Device Specifications (Continued)

4.4.2.1 Output Signals: Internal Propagation Delays, NS32532-20, NS32532-25, NS32532-30 (Continued)

Name	Figure	Description	Reference/Conditions	NS32532-20		NS32532-25		NS32532-30		Units
				Min	Max	Min	Max	Min	Max	
$t_{CNBC_{df}}$	4–24	CLK to $\overline{BCLK}$ F.E. Delay	2.0V on R.E., CLK to 0.8V on F.E., $\overline{BCLK}$		17		14		12	ns
$t_{BCNBC_{rf}}$	4–24	Bus Clocks Skew	2.0V on R.E., BCLK to 0.8V on F.E., $\overline{BCLK}$	−2	+2	−2	+2	−1	+1	ns
$t_{BCNBC_{fr}}$	4–24	Bus Clocks Skew	0.8V on F.E., BCLK to 2.0V on R.E., $\overline{BCLK}$	−2	+2	−2	+2	−1	+1	ns
t_{A_v}	4–5, 4–6	Address Bits 0–31 Valid	After R.E., BCLK T1		11		8		7	ns
t_{A_h}	4–5, 4–6	Address Bits 0–31 Hold	After R.E., BCLK T1 or Ti	0		0		0		ns
t_{A_f}	4–11, 4–12	Address Bits 0–31 Floating	After F.E., BCLK Ti		21		17		13	ns
t_{An_f}	4–11, 4–12	Address Bits 0–31 Not Floating	After F.E., BCLK Ti	0		0		0		ns
t_{AB_v}	4–8	Address Bits A2, A3 Valid (Burst Cycle)	After R.E., BCLK T2B		11		8		7	ns
t_{AB_h}	4–8	Address Bits A2, A3 Hold (Burst Cycle)	After R.E., BCLK T2B	0		0		0		ns
t_{DO_v}	4–6, 4–15	Data Out Valid	After F.E., BCLK T1		13		12		11	ns
t_{DO_h}	4–6, 4–15	Data Out Hold	After R.E., BCLK T1 or Ti	0		0		0		ns
$t_{DO_{spc}}$	4–15	Data Out Setup (Slave Write)	Before $\overline{SPC}$ T.E.	8		6		5		ns
t_{DO_f}	4–7	Data Bus Floating	After R.E., BCLK T1 or Ti		21		17		13	ns
$t_{DO_{nf}}$	4–7	Data Bus Not Floating	After F.E., BCLK T1	0		0		0		ns
t_{BMT_v}	4–5, 4–7	$\overline{BMT}$ Signal Valid	After R.E., BCLK T1		32		27		23	ns
t_{BMT_h}	4–5, 4–7	$\overline{BMT}$ Signal Hold	After R.E., BCLK T2	0		0		0		ns
t_{BMT_f}	4–11, 4–12	$\overline{BMT}$ Signal Floating	After F.E., BCLK Ti		21		17		13	ns
$t_{BMT_{hf}}$	4–11, 4–12	$\overline{BMT}$ Signal Not Floating	After F.E., BCLK Ti	0		0		0		ns
t_{CONF_a}	4–5, 4–8	$\overline{CONF}$ Signal Active	After F.E., BCLK T1		11		9		8	ns
$t_{CONF_{ia}}$	4–5, 4–8	$\overline{CONF}$ Signal Inactive	After R.E., BCLK T1 or Ti		11		9		8	ns
t_{CONF_f}	4–11, 4–12	$\overline{CONF}$ Signal Floating	After F.E., BCLK Ti		21		17		13	ns
$t_{CONF_{nf}}$	4–11, 4–12	$\overline{CONF}$ Signal Not Floating	After F.E., BCLK Ti	0		0		0		ns
t_{ADS_a}	4–5, 4–8	$\overline{ADS}$ Signal Active	After R.E., BCLK T1		11		8		7	ns
$t_{ADS_{ia}}$	4–5, 4–8	$\overline{ADS}$ Signal Inactive	After F.E., BCLK T1		11		8		7	ns
t_{ADS_w}	4–6	$\overline{ADS}$ Pulse Width	At 0.8V (Both Edges)	15		12		10		ns
t_{ADS_f}	4–11, 4–12	$\overline{ADS}$ Signal Floating	After F.E., BCLK Ti		21		17		13	ns

4.0 Device Specifications (Continued)

4.4.2.1 Output Signals: Internal Propagation Delays, NS32532-20, NS32532-25, NS32532-30 (Continued)

Name	Figure	Description	Reference/Conditions	NS32532-20		NS32532-25		NS32532-30		Units
				Min	Max	Min	Max	Min	Max	
$t_{ADS_{nf}}$	4-11, 4-12	$\overline{ADS}$ Signal Not Floating	After F.E., BCLK Ti	0		0		0		ns
t_{BE_v}	4-6, 4-8	$\overline{BE}_n$ Signals Valid	After R.E., BCLK T1		11		9		8	ns
t_{BE_h}	4-6, 4-8	$\overline{BE}_n$ Signals Hold	After R.E., BCLK T1, Ti or T2B	0		0		0		ns
t_{BE_f}	4-11, 4-12	$\overline{BE}_n$ Signals Floating	After F.E., BCLK Ti		21		17		13	ns
$t_{BE_{nf}}$	4-11, 4-12	$\overline{BE}_n$ Signals Not Floating	After F.E., BCLK Ti	0		0		0		ns
t_{DDIN_v}	4-5, 4-6	$\overline{DDIN}$ Signal Valid	After R.E., BCLK T1		11		8		7	ns
t_{DDIN_h}	4-5, 4-6	$\overline{DDIN}$ Signal Hold	After R.E., BCLK T1 or Ti	0		0		0		ns
t_{DDIN_f}	4-11, 4-12	$\overline{DDIN}$ Signal Floating	After F.E., BCLK Ti		21		17		13	ns
$t_{DDIN_{nf}}$	4-11, 4-12	$\overline{DDIN}$ Signal Not Floating	After F.E., BCLK Ti	0		0		0		ns
t_{SPC_a}	4-14, 4-15	$\overline{SPC}$ Signal Active	After R.E., BCLK T1		19		15		12	ns
$t_{SPC_{ia}}$	4-14, 4-15	$\overline{SPC}$ Signal Inactive	After R.E., BCLK Ti, T1 or T2		19		15		12	ns
t_{DDSPC}	4-14	$\overline{DDIN}$ Valid to $\overline{SPC}$ Active	Before $\overline{SPC}$ L.E.	0		0		0		ns
t_{HLDA_a}	4-12, 4-13	$\overline{HLDA}$ Signal Active	After F.E., BCLK Ti		15		11		10	ns
$t_{HLD_{Aia}}$	4-12	$\overline{HLDA}$ Signal Inactive	After F.E., BCLK Ti		15		11		10	ns
t_{ST_v}	4-5, 4-14	Status (ST0-4) Valid	After R.E., BCLK T1		11		8		7	ns
t_{ST_h}	4-5, 4-14	Status (ST0-4) Hold	After R.E., BCLK T1 or Ti	0		0		0		ns
t_{BOUT_a}	4-8, 4-9	$\overline{BOUT}$ Signal Active	After R.E., BCLK T2		15		12		11	ns
$t_{BOUT_{ia}}$	4-8, 4-9	$\overline{BOUT}$ Signal Inactive	After R.E., BCLK Last T2B, T1 or Ti		15		12		11	ns
t_{BOUT_f}	4-11, 4-12	$\overline{BOUT}$ Signal Floating	After F.E., BCLK Ti		21		17		13	ns
$t_{BOUT_{nf}}$	4-11, 4-12	$\overline{BOUT}$ Signal Not Floating	After F.E., BCLK Ti	0		0		0		ns
t_{ILO_a}	4-7	Interlock Signal Active	After F.E., BCLK Ti		11		9		8	ns
$t_{ILO_{ia}}$	4-7	Interlock Signal Inactive	After F.E., BCLK Ti		11		9		8	ns
t_{PFS_a}	4-21	$\overline{PFS}$ Signal Active	After F.E., BCLK		15		11		10	ns
$t_{PFS_{ia}}$	4-21	$\overline{PFS}$ Signal Inactive	After F.E., Next BCLK		15		11		10	ns
t_{ISF_a}	4-22	$\overline{ISF}$ Signal Active	After F.E., BCLK		15		11		10	ns
$t_{ISF_{ia}}$	4-22	$\overline{ISF}$ Signal Inactive	After F.E., Next BCLK		15		11		10	ns
t_{BP_a}	4-23	$\overline{BP}$ Signal Active	After F.E., BCLK		15		11		10	ns
$t_{BP_{ia}}$	4-23	$\overline{BP}$ Signal Inactive	After F.E., Next BCLK		15		11		10	ns
t_{US_v}	4-5	U/$\overline{S}$ Signal Valid	After R.E., BCLK T1		11		9		8	ns
t_{US_h}	4-5	U/$\overline{S}$ Signal Hold	After R.E., BCLK T1 or Ti	0		0		0		ns

4.0 Device Specifications (Continued)

4.4.2.1 Output Signals: Internal Propagation Delays, NS32532-20, NS32532-25, NS32532-30 (Continued)

Name	Figure	Description	Reference/Conditions	NS32532-20		NS32532-25		NS32532-30		Units
				Min	Max	Min	Max	Min	Max	
t_{CAS_v}	4–5	$\overline{CASEC}$ Signal Valid	After F.E., BCLK T1		15		11		10	ns
t_{CAS_h}	4–5	$\overline{CASEC}$ Signal Hold	After F.E., BLCK T1 or Ti	0		0		0		ns
t_{CAS_f}	4–11, 4–12	$\overline{CASEC}$ Signal Floating	After F.E., BLCK Ti		21		17		13	ns
$t_{CAS_{nf}}$	4–11, 4–12	$\overline{CASEC}$ Signal Not Floating	After F.E., BLCK Ti	0		0		0		ns
t_{CIO_v}	4–5	CIOUT Signal Valid	After R.E., BLCK T1		15		11		10	ns
t_{CIO_h}	4–5	CIOUT Signal Hold	After R.E., BLCK T1 or Ti	0		0		0		ns
t_{IOI_v}	4–5	$\overline{IOINH}$ Signal Valid	After R.E., BLCK T1		15		11		10	ns
t_{IOI_h}	4–5	$\overline{IOINH}$ Signal Hold	After R.E., BLCK T1 or Ti	0		0		0		ns

4.4.2.2 Input Signal Requirements: NS32532-20, NS32532-25, NS32532-30

Name	Figure	Description	Reference/Conditions	NS32532-20		NS32532-25		NS32532-30		Units
				Min	Max	Min	Max	Min	Max	
t_{C_p}	4–24	Input Clock Period	R.E., CLK to Next R.E., CLK	25	100	20	100	16.6	100	ns
t_{C_h}	4–24	CLK High Time	At 2.0V on CLK (Both Edges)	0.5 t_{C_p} −5 ns		0.5 t_{C_p} −5 ns		0.5 t_{C_p} −4 ns		
t_{C_l}	4–24	CLK Low Time	At 0.8V on CLK (Both Edges)	0.5 t_{C_p} −5 ns		0.5 t_{C_p} −5 ns		0.5 t_{C_p} −4 ns		
t_{C_r}	4–24	CLK Rise Time	0.8V to 2.0V on R.E., CLK		5		4		3	ns
t_{C_f}	4–24	CLK Fall Time	2.0V to 0.8V on F.E., CLK		5		4		3	ns
t_{DI_s}	4–5, 4–14	Data In Setup	Before R.E., BLCK T1 or Ti	13		11		9		ns
t_{DI_h}	4–5, 4–14	Data In Hold	After R.E., BCLK T1 or Ti	1		1		1		ns
t_{RDY_s}	4–5	$\overline{RDY}$ Setup Time	Before R.E., BCLK T2(W), T1 or Ti	22		18		15		ns
t_{RDY_h}	4–5	$\overline{RDY}$ Hold Time	Ater R.E., BCLK T2(W), T1 or Ti	1		1		1		ns
t_{BW_s}	4–5	BW0–1 Setup Time	Before F.E., BCLK T2 or T2(W)	21		17		14		ns
t_{BW_h}	4–5	BW0–1 Hold Time	After F.E., BCLK T2 or T2(W)	1		1		1		ns
t_{HOLD_s}	4–12, 4–13	$\overline{HOLD}$ Setup Time	Before F.E., BCLK	21		17		14		ns
t_{HOLD_h}	4–12	$\overline{HOLD}$ Hold Time	After F.E., BCLK	1		1		1		ns
t_{BIN_s}	4–8	$\overline{BIN}$ Setup Time	Before F.E., BCLK T2 or T2(W)	21		17		14		ns
t_{BIN_h}	4–8	$\overline{BIN}$ Hold Time	After F.E., BCLK T2 or T2(W)	1		1		1		ns

4.0 Device Specifications (Continued)

4.4.2.2 Input Signal Requirements: NS32532-20, NS32532-25, NS32532-30 (Continued)

Name	Figure	Description	Reference/Conditions	NS32532-20		NS32532-25		NS32532-30		Units
				Min	Max	Min	Max	Min	Max	
t_{BER_s}	4–6, 4–8	$\overline{BER}$ Setup Time	Before R.E., BCLK T1 or Ti	21		17		14		ns
t_{BER_h}	4–6, 4–8	$\overline{BER}$ Hold Time	After R.E., BCLK T1 or Ti	1		1		1		ns
t_{BRT_s}	4–6, 4–8	$\overline{BRT}$ Setup Time	Before R.E., BCLK T1 or Ti	21		17		14		ns
t_{BRT_h}	4–6, 4–8	$\overline{BRT}$ Hold Time	After R.E., BCLK T1 or Ti	1		1		1		ns
t_{IOD_s}	4–5	$\overline{IODEC}$ Setup Time	Before F.E., BCLK T2 or T2(W)	21		17		14		ns
t_{IOD_h}	4–5	$\overline{IODEC}$ Hold Time	After F.E., BCLK T2 or T2(W)	1		1		1		ns
t_{PWR}	4–26	Power Stable to R.E. of $\overline{RST}$	After VCC Reaches 4.5V	50		40		30		μs
t_{RST_s}	4–27	$\overline{RST}$ Setup Time	Before R.E., BCLK	14		12		11		ns
t_{RST_w}	4–27	$\overline{RST}$ Pulse Width	At 0.8V (Both Edges)	64		64		64		t_{BC_p}
t_{CII_s}	4–5	$\overline{CIIN}$ Setup Time	Before F.E., BCLK T2	21		17		14		ns
t_{CII_h}	4–5	$\overline{CIIN}$ Hold Time	After F.E., BCLK T2	1		1		1		ns
t_{INT_s}	4–19	$\overline{INT}$ Setup Time	Before R.E., BCLK	14		12		11		ns
t_{INT_h}	4–19	$\overline{INT}$ Hold Time	After R.E., BCLK	1		1		1		ns
t_{NMI_s}	4–19	$\overline{NMI}$ Setup Time	Before R.E., BCLK	20		17		16		ns
t_{NMI_h}	4–19	$\overline{NMI}$ Hold Time	After R.E., BCLK	1		1		1		ns
t_{SD_s}	4–16	$\overline{SDN}$ Setup Time	Before R.E., BCLK	14		12		11		ns
t_{SD_h}	4–16	$\overline{SDN}$ Hold Time	After R.E., BCLK	1		1		1		ns
t_{FSSR_s}	4–17	$\overline{FSSR}$ Setup Time	Before R.E., BCLK	14		12		11		ns
t_{FSSR_h}	4–17	$\overline{FSSR}$ Hold Time	After R.E., BCLK	1		1		1		ns
t_{SYNC_s}	4–25	$\overline{SYNC}$ Setup Time	Before R.E., CLK	10		8		7		ns
t_{SYNC_h}	4–25	$\overline{SYNC}$ Hold Time	After R.E., CLK	1		1		1		ns
t_{CIA_s}	4–18	CIA0–6 Setup Time	Before R.E., BCLK	16		13		11		ns
t_{CIA_h}	4–18	CIA0–6 Hold Time	After R.E., BCLK	1		1		1		ns
t_{INVS_s}	4–18	$\overline{INVSET}$ Setup Time	Before R.E., BCLK	16		13		11		ns
t_{INVS_h}	4–18	$\overline{INVSET}$ Hold Time	After R.E., BCLK	1		1		1		ns
t_{INVI_s}	4–18	$\overline{INVIC}$ Setup Time	Before R.E., BCLK	14		12		11		ns
t_{INVI_h}	4–18	$\overline{INVIC}$ Hold Time	After R.E., BCLK	1		1		1		ns
t_{INVD_s}	4–18	$\overline{INVDC}$ Setup Time	Before R.E., BCLK	16		13		11		ns
t_{INVD_h}	4–18	$\overline{INVDC}$ Hold Time	After R.E., BCLK	1		1		1		ns
t_{DBG_s}	4–20	$\overline{DBG}$ Setup Time	Before R.E., BCLK	14		12		11		ns
t_{DBG_h}	4–20	$\overline{DBG}$ Hold Time	After R.E., BCLK	1		1		1		ns

4.0 Device Specifications (Continued)

4.4.3 Timing Diagrams

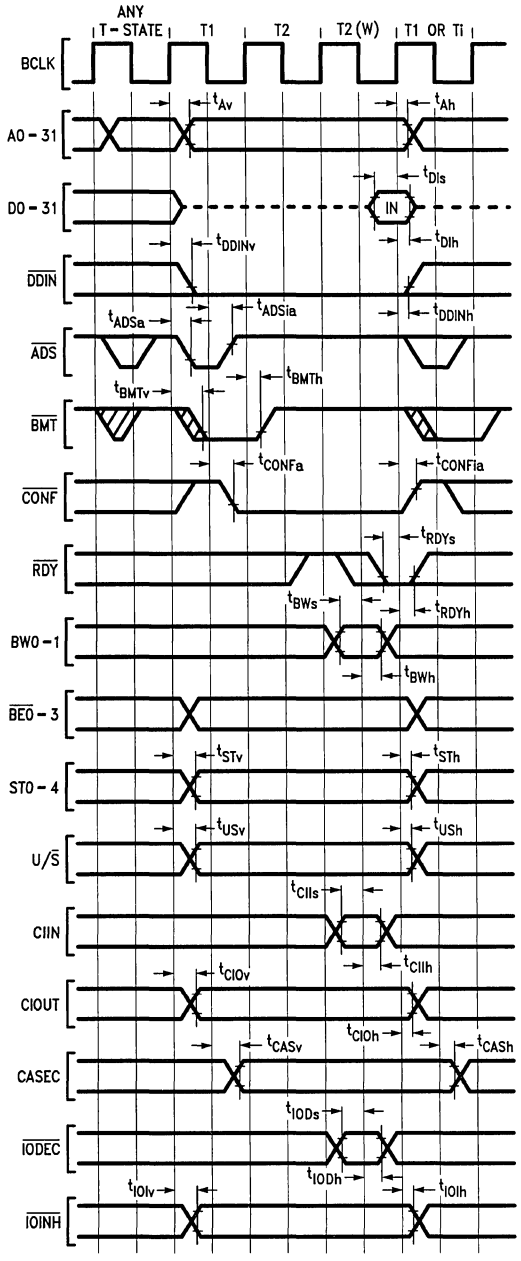

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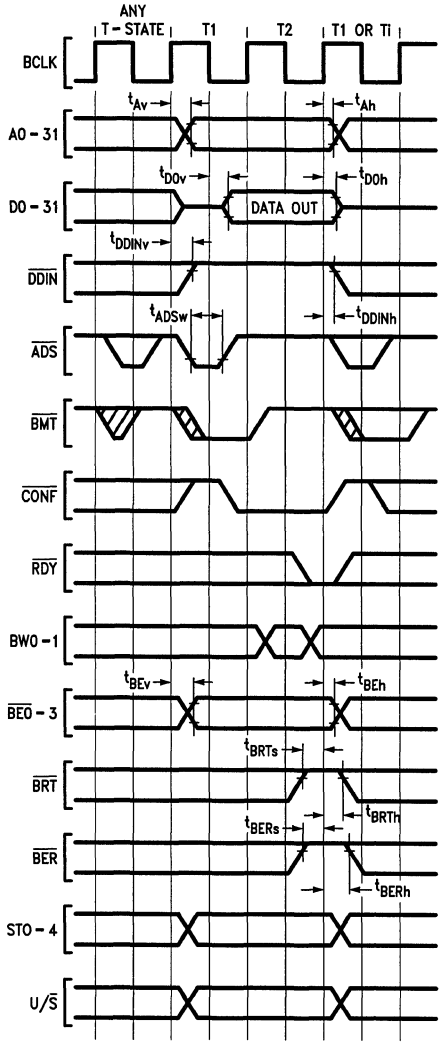
FIGURE 4-5. Basic Read Cycle Timing

4.0 Device Specifications (Continued)



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Note: An Idle State is always inserted before a Write Cycle when the Write immediately follows a Read Cycle.

FIGURE 4-6. Write Cycle Timing

4.0 Device Specifications (Continued)

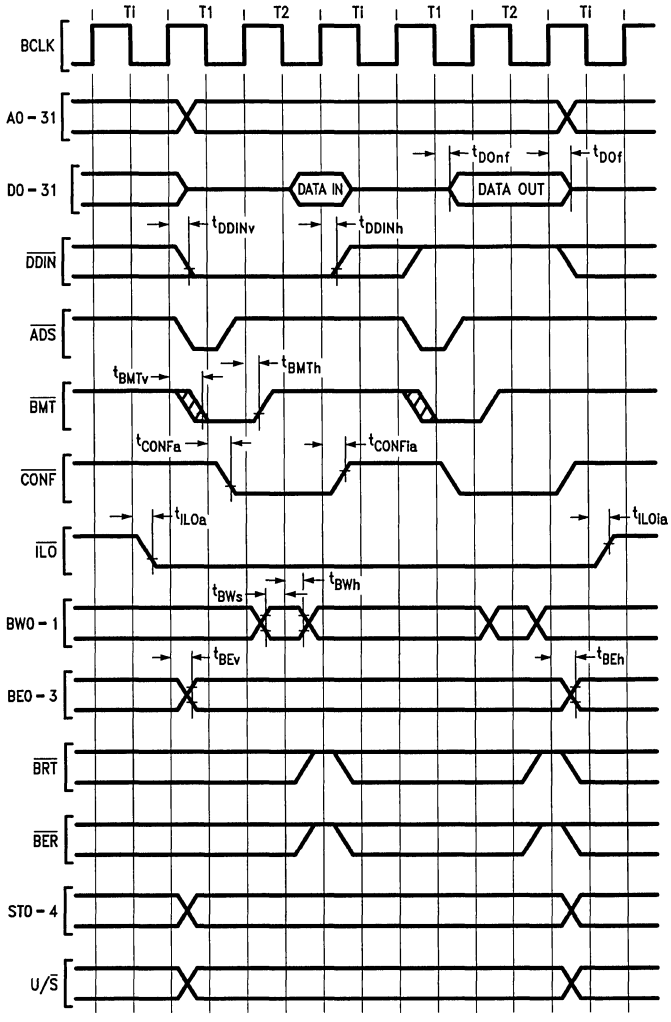

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FIGURE 4-7. Interlocked Read and Write Cycles

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4.0 Device Specifications (Continued)

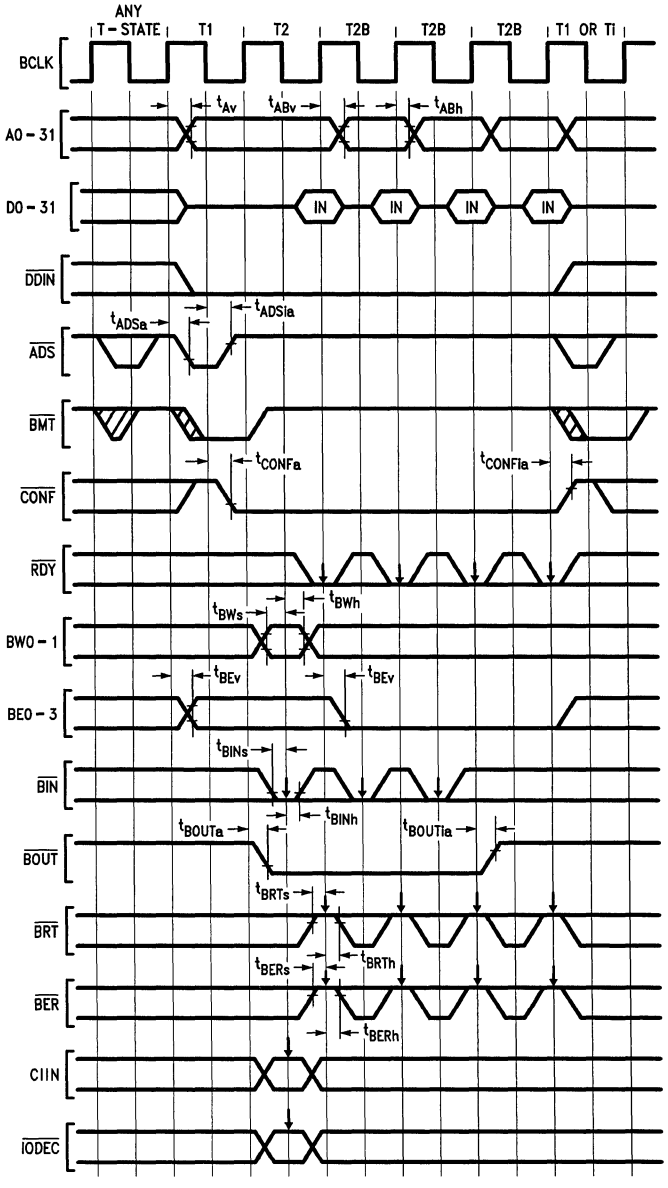

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FIGURE 4-8. Burst Read Cycles

4.0 Device Specifications (Continued)

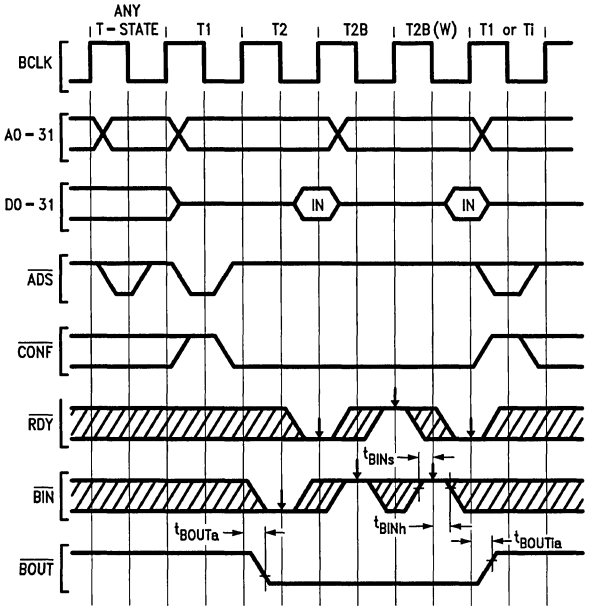

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FIGURE 4-9. External Termination of Burst Cycles

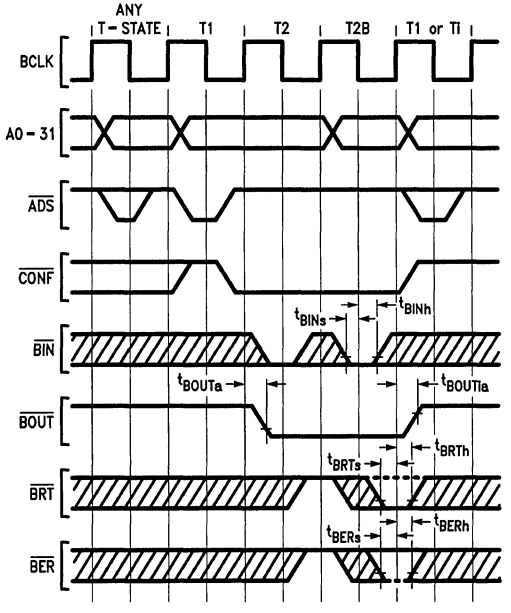

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FIGURE 4-10. Bus Error or Retry During Burst Cycles

Note: Two idle state are always inserted by the CPU following the assertion of $\overline{BRT}$.

4.0 Device Specifications (Continued)

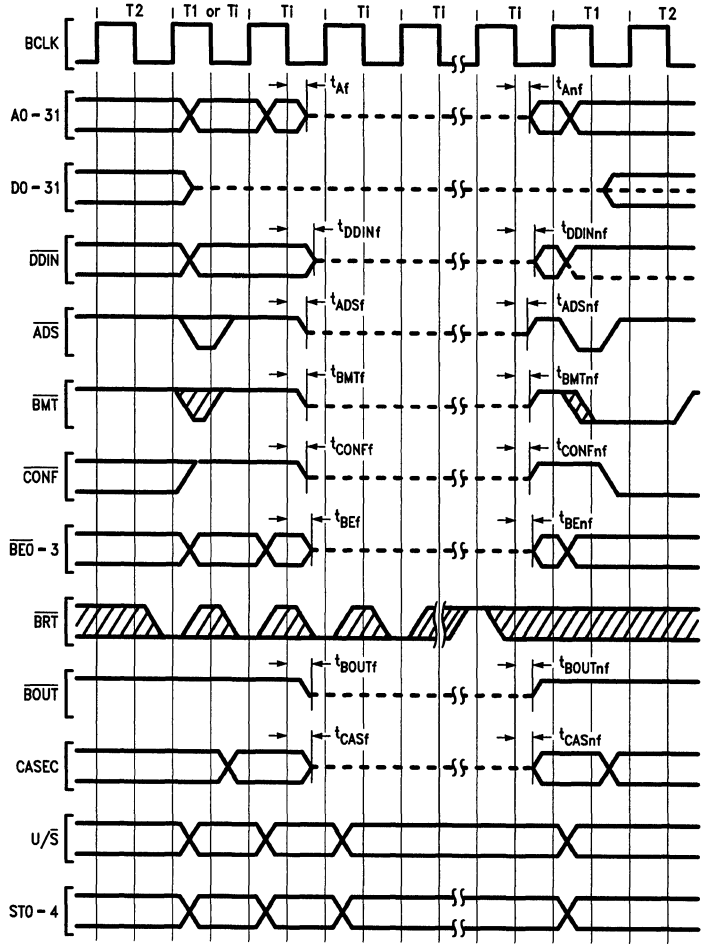

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FIGURE 4-11. Extended Retry Timing

4.0 Device Specifications (Continued)

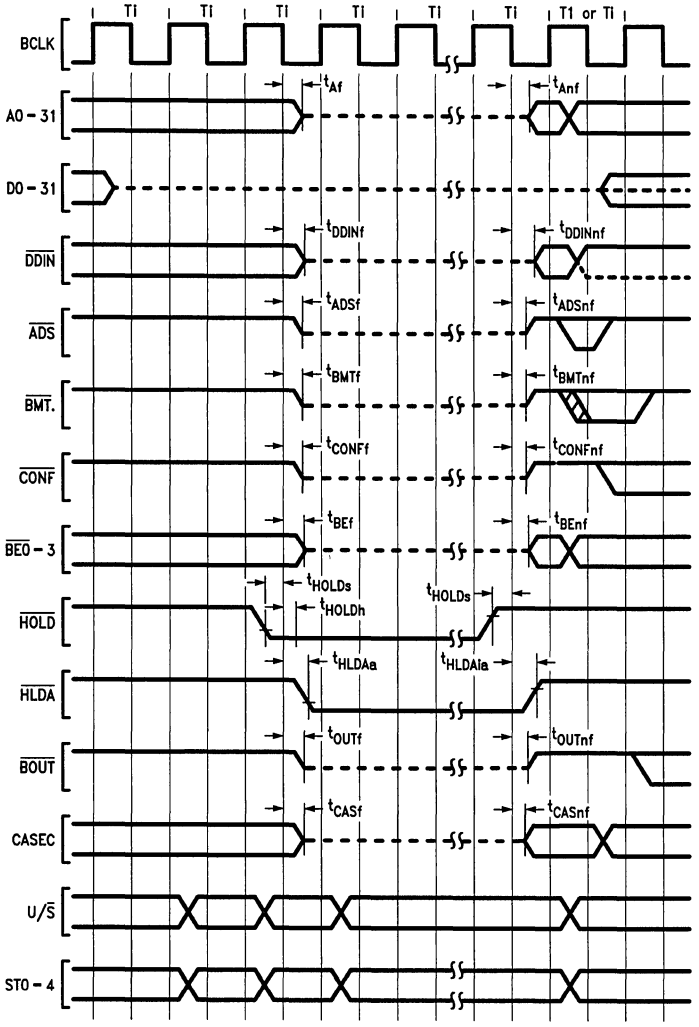

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FIGURE 4-12. Hold Timing (Bus Initially Idle)

4.0 Device Specifications (Continued)

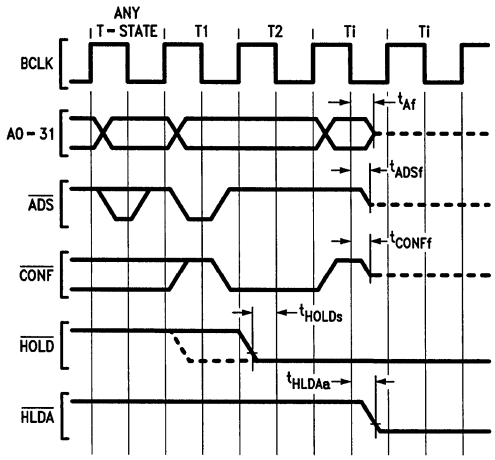

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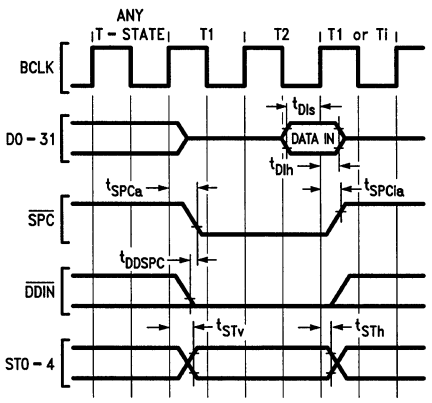
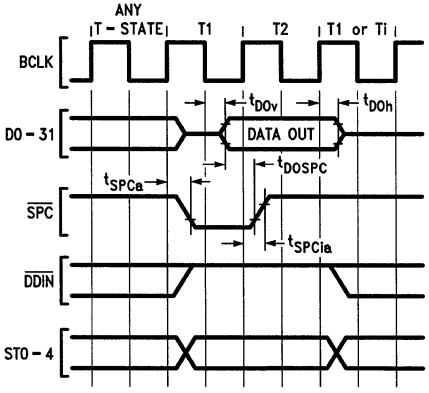
FIGURE 4-13. $\overline{\text{HOLD}}$ Acknowledge Timing (Bus Initially Not Idle)



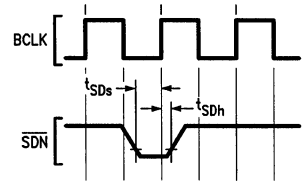
TL/EE/9354-52

FIGURE 4-14. Slave Processor Read Timing



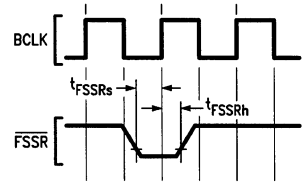
TL/EE/9354-53

FIGURE 4-15. Slave Processor Write Timing



TL/EE/9354-54

FIGURE 4-16. Slave Processor Done



TL/EE/9354-55

FIGURE 4-17. $\overline{\text{FSSR}}$ Signal Timing

4.0 Device Specifications (Continued)

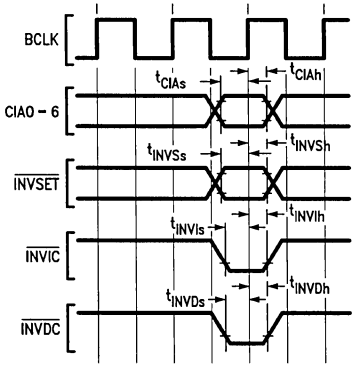


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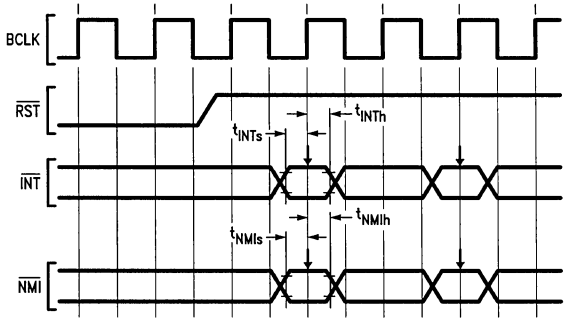
FIGURE 4-18. Cache Invalidation Request

Note 1: CIA0–6 and $\overline{\text{INVSET}}$ are only relevant when $\overline{\text{INVIC}}$ and/or $\overline{\text{INVDC}}$ are asserted.

Note 2: If a memory location is being read at the same time an invalidation request for that location occurs, the data will be invalid in the cache if the invalidation request occurs during or after state T2 or T2B of the read cycle.



TL/EE/9354–57

FIGURE 4-19. $\overline{\text{INT}}$ and $\overline{\text{NMI}}$ Signals Sampling

Note 1: $\overline{\text{INT}}$ and $\overline{\text{NMI}}$ are sampled on every other rising edge of BCLK, starting with the second rising edge of BCLK after $\overline{\text{RST}}$ goes high.

Note 2: $\overline{\text{INT}}$ is level sensitive, and once asserted, it should not be deasserted until it is acknowledged.

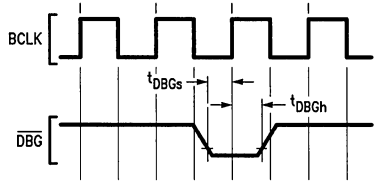


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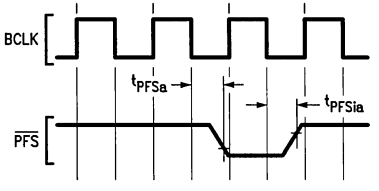
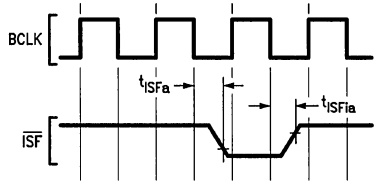
FIGURE 4-20. Debug Trap Request



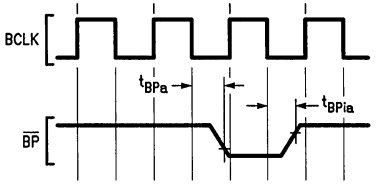
TL/EE/9354–59

FIGURE 4-21. $\overline{\text{PFS}}$ Signal Timing



TL/EE/9354–60

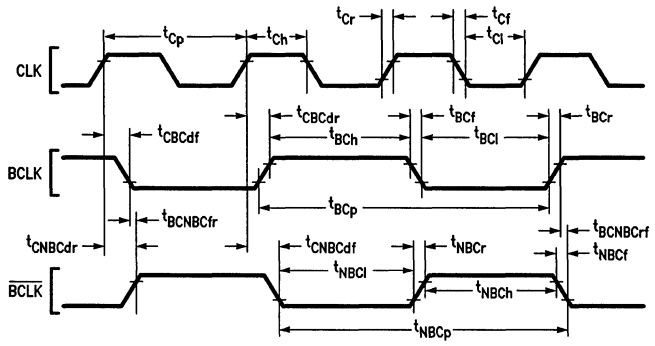
FIGURE 4-22. $\overline{\text{ISF}}$ Signal Timing



TL/EE/9354–61

FIGURE 4-23. Break Point Signal Timing

4.0 Device Specifications (Continued)



TL/EE/9354–62

FIGURE 4-24. Clock Waveforms

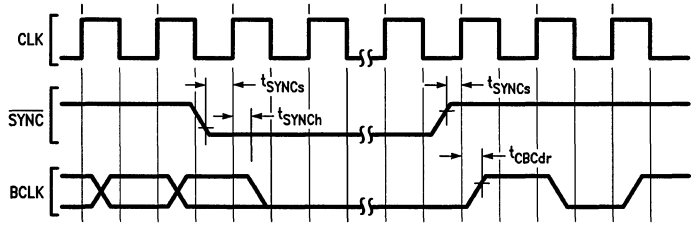


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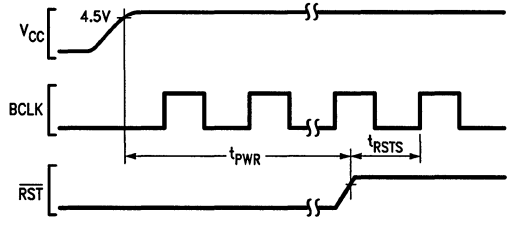
FIGURE 4-25. Bus Clock Synchronization



TL/EE/9354–64

FIGURE 4-26. Power-On Reset

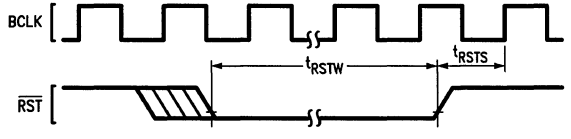


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FIGURE 4-27. Non-Power-On Reset

Appendix A: Instruction Formats

NOTATIONS:

i = Integer Type Field
B = 00 (Byte)
W = 01 (Word)
D = 11 (Double Word)

f = Floating Point Type Field
F = 1 (Std. Floating: 32 bits)
L = 0 (Long Floating: 64 bits)

c = Custom Type Field
D = 1 (Double Word)
Q = 0 (Quad Word)

op = Operation Code
Valid encodings shown with each format.

gen, gen 1, gen 2 = General Addressing Mode Field
See Section 2.2 for encodings.

reg = General Purpose Register Number

cond = Condition Code Field
0000 = EQual: Z = 1
0001 = Not Equal: Z = 0
0010 = Carry Set: C = 1
0011 = Carry Clear: C = 0
0100 = Higher: L = 1
0101 = Lower or Same: L = 0
0110 = Greater Than: N = 1
0111 = Less or Equal: N = 0
1000 = Flag Set: F = 1
1001 = Flag Clear: F = 0
1010 = LOwer: L = 0 and Z = 0
1011 = Higher or Same: L = 1 or Z = 1
1100 = Less Than: N = 0 and Z = 0
1101 = Greater or Equal: N = 1 or Z = 1
1110 = (Unconditionally True)
1111 = (Unconditionally False)

short = Short Immediate value. May contain:
quick: Signed 4-bit value, in MOVQ, ADDQ, CMPQ, ACB.
cond: Condition Code (above), in Scond.
areg: CPU Dedicated Register, in LPR, SPR.
0000 = US
0001 = DCR
0010 = BPC
0011 = DSR
0100 = CAR
0101–0111 = (Reserved)
1000 = FP
1001 = SP
1010 = SB
1011 = USP
1100 = CFG
1101 = PSR
1110 = INTBASE
1111 = MOD

Options: in String Instructions

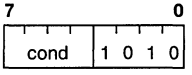
U/W	B	T

T = Translated
B = Backward
U/W = 00: None
01: While Match
11: Until Match

Configuration bits, in SETCFG Instruction:

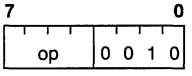
1	1	1	1	C	M	F	I

mreg: MMU Register number, in LMR, SMR.
0000 = } Trap (UND)
•
•
•
0111 = }
1000 = Reserved
1001 = MCR
1010 = MSR
1011 = TEAR
1100 = PTB0
1101 = PTB1
1110 = IVAR0
1111 = IVAR1



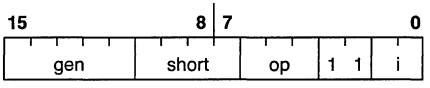
Format 0

Bcond (BR)



Format 1

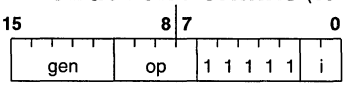
BSR	-0000	ENTER	-1000
RET	-0001	EXIT	-1001
CXP	-0010	NOP	-1010
RXP	-0011	WAIT	-1011
RETT	-0100	DIA	-1100
RETI	-0101	FLAG	-1101
SAVE	-0110	SVC	-1110
RESTORE	-0111	BPT	-1111



Format 2

ADDQ	-000	ACB	-100
CMPQ	-001	MOVQ	-101
SPR	-010	LPR	-110
Scond	-011		

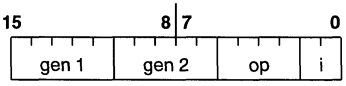
Appendix A: Instruction Formats (Continued)



Format 3

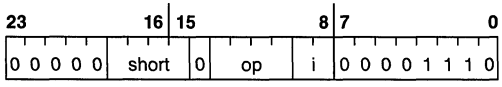
CXPD	-0000	ADJSP	-1010
BICPSR	-0010	JSR	-1100
JUMP	-0100	CASE	-1110
BISPSR	-0110		

Trap (UND) on XXX1, 1000



Format 4

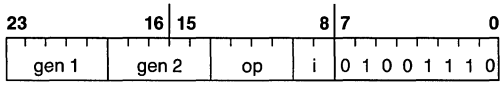
ADD	-0000	SUB	-1000
CMP	-0001	ADDR	-1001
BIC	-0010	AND	-1010
ADDC	-0100	SUBC	-1100
MOV	-0101	TBIT	-1101
OR	-0110	XOR	-1110



Format 5

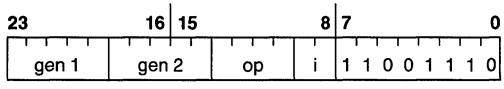
MOVS	-0000	SETCFG	-0010
CMPS	-0001	SKPS	-0011

Trap (UND) on 1XXX, 01XX



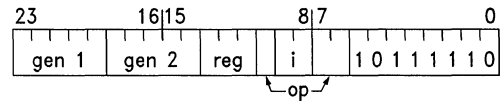
Format 6

ROT	-0000	NEG	-1000
ASH	-0001	NOT	-1001
CBIT	-0010	Trap (UND)	-1010
CBITI	-0011	SUBP	-1011
Trap (UND)	-0100	ABS	-1100
LSH	-0101	COM	-1101
SBIT	-0110	IBIT	-1110
SBITI	-0111	ADDP	-1111



Format 7

MOVM	-0000	MUL	-1000
CMPM	-0001	MEI	-1001
INSS	-0010	Trap (UND)	-1010
EXTS	-0011	DEI	-1011
MOVXBW	-0100	QUO	-1100
MOVZBW	-0101	REM	-1101
MOVZiD	-0110	MOD	-1110
MOVXiD	-0111	DIV	-1111



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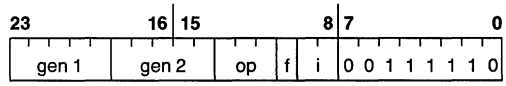
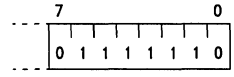
Format 8

EXT	-0 00	INDEX	-1 00
CVTP	-0 01	FFS	-1 01
INS	-0 10		
CHECK	-0 11		
MOVSU	-110, reg = 001		
MOVUS	-110, reg = 011		



Format 9

MOVif	-000	ROUND	-100
LFSR	-001	TRUNC	-101
MOVLF	-010	SFSR	-110
MOVFL	-011	FLOOR	-111



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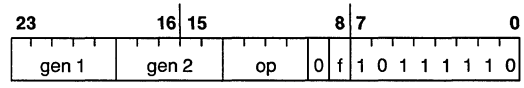
Format 10

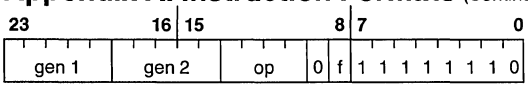
Trap (UND) Always



Format 11

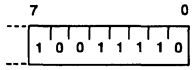
ADDf	-0000	DIVf	-1000
MOVf	-0001	Note 1	-1001
CMPf	-0010	Note 3	-1010
Note 3	-0011	Note 1	-1011
SUBf	-0100	MULf	-1100
NEGf	-0101	ABSf	-1101
Note 2	-0110	Note 2	-1110
Note 1	-0111	Note 1	-1111

Appendix A: Instruction Formats (Continued)



Format 12

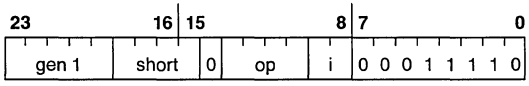
Note 2	-0000	Note 2	-1000
Note 1	-0001	Note 1	-1001
Note 3	-0010	Note 3	-1010
Note 3	-0011	Note 1	-1011
Note 2	-0100	Note 2	-1100
Note 1	-0101	Note 1	-1101
Note 2	-0110	Note 2	-1110
Note 1	-0111	Note 1	-1111



TL/EE/9354-68

Format 13

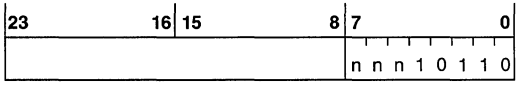
Trap (UND) Always



Format 14

RDVAL	-0000	LMR	-0010
WRVAL	-0001	SMR	-0011
		CINV	-1001

Trap (UND) on 01XX, 1000, 101X, 11XX

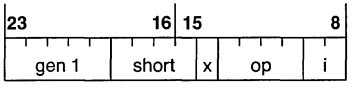


Format 15

(Custom Slave)

nnn **Operation Word Format**

000

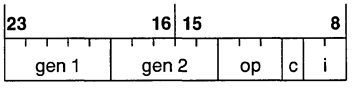


Format 15.0

LCR	-0010
SCR	-0011

Trap (UND) on all others

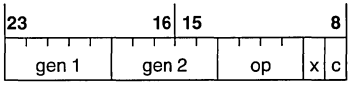
001



Format 15.1

CCV3	-000	CCV2	-100
LCSR	-001	CCV1	-101
CCV5	-010	SCSR	-110
CCV4	-011	CCV0	-111

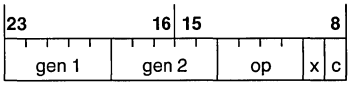
101



Format 15.5

CCAL0	-0000	CCAL3	-1000
CMOV0	-0001	CMOV3	-1001
CCMP0	-0010	Note 3	-1010
CCMP1	-0011	Note 1	-1011
CCAL1	-0100	CCAL2	-1100
CMOV2	-0101	CMOV1	-1101
Note 2	-0110	Note 2	-1110
Note 1	-0111	Note 1	-1111

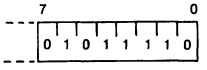
111



Format 15.7

Note 2	-0000	Note 2	-1000
Note 1	-0001	Note 1	-1001
Note 3	-0010	Note 3	-1010
Note 3	-0011	Note 1	-1011
Note 2	-0100	Note 2	-1100
Note 1	-0101	Note 1	-1101
Note 2	-0110	Note 2	-1110
Note 1	-0111	Note 1	-1111

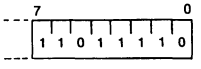
If nnn = 010, 011, 100, 110 then Trap (UND) Always.



TL/EE/9354-69

Format 16

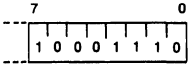
Trap (UND) Always



TL/EE/9354-70

Format 17

Trap (UND) Always



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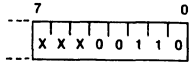
2

Appendix A: Instruction Formats (Continued)

Format 18

Trap (UND) Always



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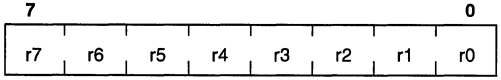
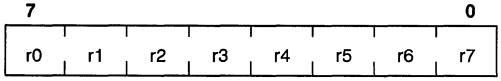
Format 19

Trap (UND) Always

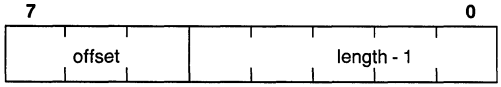
Implied Immediate Encodings:



Register Mark, Appended to SAVE, ENTER



Register Mark, Appended to RESTORE, EXIT



Offset/Length Modifier Appended to INSS, EXTS

Note 1: Opcode not defined; CPU treats like MOV_f or $CMOV_c$. First operand has access class of read; second operand has access class of write; f or c field selects 32- or 64-bit data.

Note 2: Opcode not defined; CPU treats like ADD_f or $CCAL_c$. First operand has access class of read;, second operand has access class of read-modify-write; f or c field selects 32- or 64-bit data.

Note 3: Opcode not defined; CPU treats like CMP_f or $CCMP_c$. First operand has access class of read;, second operand has access class of read; f or c field selects 32- or 64-bit data.

Appendix B. Compatibility Issues

The NS32532 is compatible with the Series 32000 architecture implemented by the NS32032, NS32332, and previous microprocessors in the family. Compatibility means that within certain limited constraints, programs that execute on one of the earlier Series 32000 microprocessors will produce identical results when executed on the NS32532. Compatibility applies to privileged operating systems programs, as well as to non-privileged applications programs. This appendix explains both the restrictions on compatibility with previous Series 32000 microprocessors and the extensions to the architecture that are implemented by the NS32532.

B.1 RESTRICTIONS ON COMPATIBILITY

If the following restrictions are observed, then a program that executes on an earlier Series 32000 microprocessor will produce identical results when executed on the NS32532 in an appropriately configured system:

1. The program is not time-dependent. For example, the program should not use instruction loops to control real-time delays.
2. The program does not use any encodings of instructions, operands, addresses, or control fields identified to be reserved or undefined. For example, if the count operand's value for an LSHi instruction is not within the range specified by the *Series 32000 Instruction Set Reference Manual,* then the results produced by the NS32532 may differ from those of the NS32032.
3. Either the program does not depend on the use of a Memory Management Unit (MMU), or it is written for operation with the NS32382 MMU and does not use the bus-error or debugging features of the NS32382.
4. The program does not depend on the detection of bus errors according to the implementation of the NS32332. For example, the NS32532 distinguishes between restartable and nonrestartable bus errors by transferring control to the appropriate bus-error exception service procedure through one of two distinct entries in the Interrupt Dispatch Table. In contrast, the NS32332 uses a single entry in the Interrupt Dispatch Table for all bus errors.
5. The program does not modify itself. Refer to Section B.4 for more information.
6. The program does not depend on the execution of certain complex instructions to be non-interruptible. Refer to Section B.5 on. "Memory-Mapped I/O" for more information.
7. The program does not use the custom slave instructions CATSTO and CATST1, as they are not supported by the NS32532 and will result in a Trap (UND) when their execution is attempted.

B.2 ARCHITECTURE EXTENSIONS

The NS32532 implements the following extensions of the Series 32000 architecture using previously reserved control bits, instruction encodings, and memory locations. Extensions implemented earlier in the NS32332, such as 32-bit addressing, are not listed.

1. The DC, LDC, IC, and LIC bits in the CFG register have been defined to control the on-chip Instruction and Data Caches. The DE-bit in the CFG register has been defined to enable Direct-Exception Mode.
2. The V-flag in the PSR register has been defined to enable the Integer-Overflow Trap.
3. The DCR, BPC, DSR, and CAR registers have been defined to control debugging features. Access to these registers has been added to the definition of the LPR and SPR instructions.
4. Access to the CFG and SP1 registers has been added to the definition of the LPR and SPR instructions.
5. The CINV instruction has been defined to invalidate control of the on-chip Instruction and Data Caches.
6. Direct-Exception Mode has been added to support faster interrupt service time and systems without module tables.
7. A new entry has been added to the Interrupt Dispatch Table for supporting vectors to distinguish between restartable and nonrestartable bus errors. Two additional entries support Trap (OVF) and Trap (DBG).
8. Restrictions have been eliminated for recovery from Trap (ABT) for operands with access class of write that cross page boundaries. Restrictions still exist however, for the operands of the MOVMi instruction.

B.3 INTEGER OVERFLOW TRAP

A new trap condition is recognized for integer arithmetic overflow. Trap (OVF) is enabled by the V-flag in the PSR. This new trap is important because detection of integer overflow conditions is required for certain programming languages, such as ADA, and the PSR flags do not indicate the occurrence of overflow for ASHi, DIVi and MULi instructions.

Appendix B. Compatibility Issues (Continued)

More details on integer overflow are given in Section 3.2.5, where a description of all the cases in which an overflow condition is detected is also provided.

INTEGER ARITHMETIC

The V-flag in the PSR enables Trap (OVF) to occur following execution of an integer arithmetic instruction whose result cannot be represented exactly in the destination operand's location.

If the number of bits required to represent the resulting quotient of a DEI instruction exceeds half the number of bits of the destination, then the contents of both the quotient and remainder stored in the destination are undefined.

The ADDR instruction can be used in place of integer arithmetic instructions to perform certain calculations. In this case however, integer overflow is not detected by the CPU.

LOGICAL INSTRUCTIONS

The V-flag in the PSR enables Trap (OVF) to occur following execution of an ASHi instruction whose result cannot be represented exactly in the destination operand's location.

ARRAY INSTRUCTIONS

The V-flag in the PSR enables Trap (OVF) to occur following execution of a CHECKi instruction whose source operand is out of bounds.

PROCESSOR CONTROL INSTRUCTIONS

The V-flag in the PSR enables Trap (OVF) to occur following execution of an ACBi instruction if the sum of the "inc" value and the "index" operand cannot be represented exactly in the "index" operand's location.

B.4 SELF-MODIFYING CODE

The Series 32000 architecture does not have special provisions to optimally support self-modifying programs. Nevertheless, on the NS32332 and previous Series 32000 microprocessors it is possible to execute self-modifying code according to the following sequence:

1. Modify the appropriate instruction.
2. Execute a JUMP instruction or other instruction that causes the microprocessor's instruction queue to be flushed.
3. Execute the modified instruction.

For example, an interactive debugger may follow the sequence above after reaching a breakpoint in a program being monitored.

The same program may not produce identical results when executed on the NS32532 due to effects of the Instruction Cache and branch prediction. In order to execute self-modifying code on the NS32532 it is necessary to do the following:

1. Modify the appropriate instruction.
2. If the modified instruction is on a cacheable page, execute CINV to invalidate the contents of the Instruction Cache.
3. Execute an instruction that causes a serializing operation. See Section 3.1.3.3.
4. Execute the modified instruction.

B.5 MEMORY-MAPPED I/O

As was mentioned in Section 3.1.3.2, certain peripheral devices exhibit characteristics identified as "destructive-reading" and "side-effects of writing" that impose requirements for special handling of memory-mapped I/O references. The NS32532 supports two methods to use on references to memory-mapped peripheral devices that exhibit either or both of these characteristics.

For peripheral devices that exhibit only side-effects of writing, correct operation can be ensured either by locating the device between addresses FF000000 (hex) and FF7FFFFF (hex) in the virtual address space or by observing the first 2 restrictions listed below. For peripheral devices that exhibit destructive-reading, all the following restrictions must be observed to ensure correct operation:

1. References to the device must be inhibited while the CPU asserts the output signal $\overline{\text{IOINH}}$.
2. The input signal $\overline{\text{IODEC}}$ must be asserted by the system on references to the device.
3. The device cannot be used for instruction fetches, reads of effective addresses, or Page Table Entries.
4. If an instruction that reads a source operand from the device crosses a page boundary, then no Trap (ABT) or restartable bus error can occur during fetches from the page with higher addresses.
5. No Trap (ABT) for a data reference or other exception can occur during execution of an instruction that reads a source operand from the device. (Exceptions that are recognized after completion of an instruction, like Trap (OVF) and Trap (DBG), cause no problem.)
6. The device can be used as a source operand only for instructions in the list below.

ABSi	CBITi	MOVMi	SBITIi
ADDi	CBITIi	MOVXi	SUBi
ADDCi	CMPi	MOVZi	SUBCi
ADDPi	CMPQi	NEGi	SUBPi
ADDQi	COMi	NOTi	TBITi
ANDi	IBITi	ORi	XORi
ASHi	LSHi	ROTi	
BICi	MOVi	SBITi	

This restriction arises because the CPU can respond to interrupt requests during the execution of complex instruction in order to reduce interrupt latency. Thus, the CPU may read the source operands for a DEID instruction (extended-precision divide), begin calculating the instruction's results, and then respond to an interrupt request before completing the instruction. In such an event, the instruction can be executed again and completed correctly after the interrupt service procedure returns unless one of the source operands was altered by destructive-reading.

Appendix C. Instruction Set Extensions

The following sections describe the differences and extensions to the Series 32000 instruction set (as presented in the "Series 32000 Instruction Set Reference Manual") implemented by the NS32352.

No changes or additions have been made to the user-mode instruction set, and only a few privileged instructions have been added.

Appendix C. Instruction Set Extensions (Continued)

C.1 PROCESSOR SERVICE INSTRUCTIONS

The CFG register, User Stack Pointer (SP1), and Debug Registers can be loaded and stored using privileged forms of the LPRi and SPRi instructions.

When the SETCFG instruction is executed, the CFG register bits 0 through 3 are loaded from the instruction's short field, bits 4 through 7 are forced to 1, and bits 8 through 12 are forced to 0.

The contents of the on-chip Instruction Cache and Data Cache can be invalidated by executing the privileged instruction CINV. While executing the CINV instruction, the CPU generates 2 slave bus cycles on the system interface to display the first 3 bytes of the instruction and the source operand. External circuitry can thereby detect the execution of the CINV instruction for use in monitoring the contents of the on-chip caches.

C.2 MEMORY MANAGEMENT INSTRUCTIONS

The NS32532 on-chip MMU does not implement the BAR, BDR, BEAR, and BMR registers of the NS32382. These registers are used in the NS32382 to support bus error and debugging features. When an attempt is made to access one of these 4 registers by executing an LMR or SMR instruction, a Trap (UND) occurs. More generally, a Trap (UND) occurs whenever an attempt is made to execute an LMR or SMR instruction and the most-significant bit of the short-field is 0.

While executing an LMR instruction, the CPU generates 2 slave bus cycles on the system interface to display the first 3 bytes of the instruction and the source operand. External circuitry can thereby detect the execution of an LMR instruction for use in monitoring the contents of the on-chip Translation Lookaside Buffer.

Like the NS32382 MMU, the F-flag in the PSR is set and no Trap (ABT) occurs when a RDVAL or WRVAL instruction is executed and the Protection Level in the Level-1 Page Table Entry indicates that the access is not allowed. In the NS32082 MMU, an abort occurs when the Level-1 PTE is invalid, regardless of the Protection Level.

C.3 INSTRUCTION DEFINITIONS

This section provides a description of the operations and encodings of the new NS32532 privileged instructions.

Load and Store Processor Registers

Syntax:	**LPRi**	**procreg,**	**src**
		short	gen
			read.i
	SPRi	**procreg**	**dest**
		short	gen
			write.i

The LPRi and SPRi instructions can be used to load and store the User Stack Pointer (USP or SP1), the Configuration Register (CFG) and the Debug Registers in addition to the Processor Registers supported by the previous Series 32000 CPUs. Access to these registers is privileged.

Figure C-1 and Table C-1 show the instruction formats and the new 'short' field encodings for LPRi and SPRi.

Flags Affected: No flags affected by loading or storing the USP, CFG, or Debug Registers.

Traps: Illegal Instruction Trap (ILL) occurs if an attempt is made to load or store the USP, CFG or Debug Registers while the U-flag is 1.

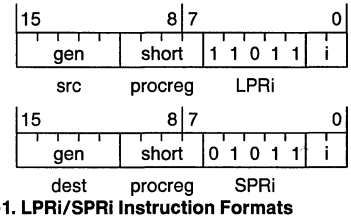


FIGURE C-1. LPRi/SPRi Instruction Formats

TABLE C-1. LPRi/SPRi New 'Short' Field Encodings

Register	procreg	short field
Debug Condition Register	DCR	0001
Breakpoint Program Counter	BPC	0010
Debug Status Register	DSR	0011
Compare Address Register	CAR	0100
User Stack Pointer	USP	1011
Configuration Register	CFG	1100

Cache Invalidate

Syntax:	**CINV**	**options, src**	
		gen	
		read. D	

The CINV instruction invalidates the contents of locations in the on-chip Instruction Cache and Data Cache. The instruction can be used to invalidate either the entire contents of the on-chip caches or only a 16-byte block. In the latter case, the 28 most-significant bits of the source operand specify the physical address of the aligned 16-byte block; the 4 least-significant bits of the source operand are ignored. If the specified block is not located in the on-chip caches, then the instruction has no effect. If the entire cache contents is to be invalidated, then the source operand is read, but its value is ignored.

Options are specified by listing the letters A (invalidate All), I (Instruction Cache), and D (Data Cache). If neither the I nor D option is specified, the instruction has no effect.

In the instruction encoding, the options are represented in the A, I, and D fields as follows:

A: 0—invalidate only a 16-byte block
1—invalidate the entire cache

I: 0—do not affect the Instruction Cache
1—invalidate the Instruction Cache

D: 0—do not affect the Data Cache
1—invalidate the Data Cache

Flags Affected: None

Traps: Illegal Operation Trap (ILL) occurs if an attempt is made to execute this instruction while the U-flag is 1.

Examples:

1. CINV A, D, I, R3 1E A7 1B

2. CINV I, R3 1E 27 19

Example 1 invalidates the entire Instruction Cache and Data Cache.

Example 2 invalidates the 16-byte block whose physical address in the Instruction Cache is contained in R3.

Appendix C. Instruction Set Extensions (Continued)

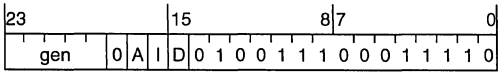


FIGURE C-2. CINV Instruction Format

Load and Store Memory Management Register

Syntax:

LMR	**mmreg,**	**src**
	short	gen
		read.D
SMR	**mmureg,**	**dest**
	short	gen
		write.D

The LMR and SMR instruction load and store the on-chip MMU registers as 32-bit quantities to and from any general operand. For reasons of system security, these instructions are privileged. In order to be executable, they must also be enabled by setting the M bit in the CFG register.

The instruction formats as well as the 'short' field encodings are shown in *Figure C-3* and Table C-2 respectively.

It is to be noted that the IVAR0 and IVAR1 registers are write-only, and as such, they can only be loaded by the LMR instruction.

Flags Affected: none

Traps: Undefined Instruction Trap (UND) occurs if an attempt is made to execute this instruction while either of the following conditions is true:

1. The M-bit in the CFG register is 0.
2. The U-Flag in the PSR is 0 and the most-significant bit of the short field is 0.

Illegal Instruction Trap (ILL) occurs if an attempt is made to execute this instruction while the M-bit in the CFG register and the U-flag in the PSR are both 1.

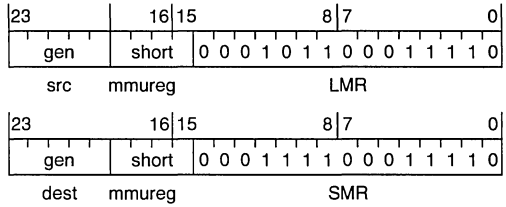


FIGURE C-3. LMR/SMR Instruction Formats

TABLE C-2. LMR/SMR 'Short' Field Encodings

Register	mmureg	short field
Memory Management Control Reg	MCR	1001
Memory Management Status Reg	MSR	1010
Translation Exception Address Reg	TEAR	1011
Page Table Base Register 0	PTB0	1100
Page Table Base Register 1	PTB1	1101
Invalidate Virtual Address 0	IVAR0	1110
Invalidate Virtual Address 1	IVAR1	1111

National Semiconductor

PRELIMINARY

NS32332-10/NS32332-15
32-Bit Advanced Microprocessors

General Description

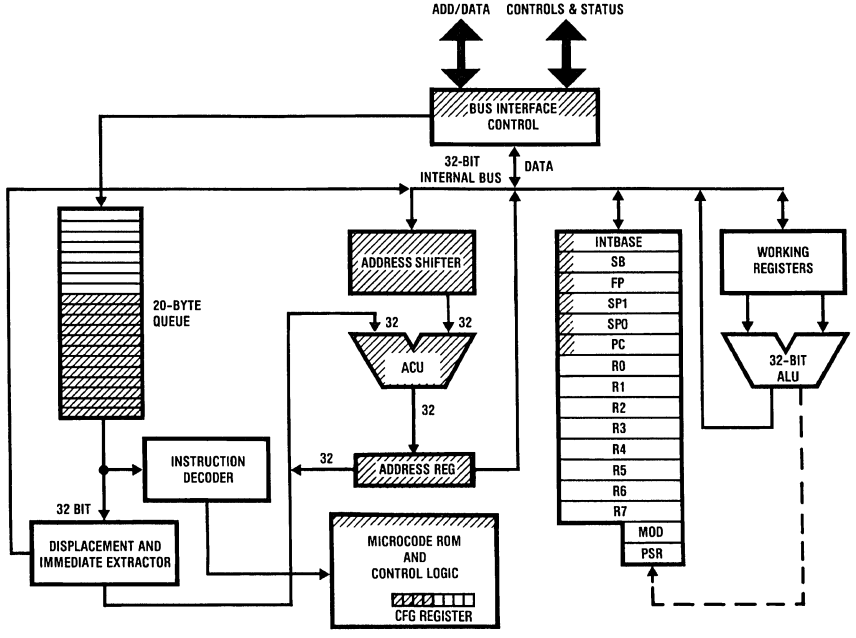
The NS32332 is a 32-bit, virtual memory microprocessor with 4 GByte addressing and an enhanced internal implementation. It is fully object code compatible with other Series 32000® microprocessors, and it has the added features of 32-bit addressing, higher instruction execution throughput, cache support, and expanded bus handling capabilities. The new bus features include bus error and retry support, dynamic bus sizing, burst mode memory accessing, and enhanced slave processor communication protocol. The higher clock frequency and added features of the NS32332 enable it to deliver 2 to 3 times the performance of the NS32032.

The NS32332 microprocessor is designed to work with both the 16- and 32-bit slave processors of the Series 32000 family.

Features

- 32-bit architecture and implementation
- 4 Gbyte uniform addressing space
- Software compatible with the Series 32000 Family
- Powerful instruction set
  - — General 2-address capability
  - — Very high degree of symmetry
  - — Address modes optimized for high level languages
- Supports both 16- and 32-bit Slave Processor Protocol
  - — Memory management support via NS32082 or NS32382
  - — Floating point support via NS32081 or NS32381
- Extensive bus feature
  - — Burst mode memory accessing
  - — Cache memory support
  - — Dynamic bus configuration (8-, 16-, 32-bits)
  - — Fast bus protocol
- High speed XMOS™ technology
- 84 Pin grid array package

Block Diagram



TL/EE/8673–1

FIGURE 1

*Shaded areas indicate enhancements from the NS32032.

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List of Tables

1.0 Product Introduction

The Series 32000 Microprocessor family is a new generation of devices using National's XMOS and CMOS technologies. By combining state-of-the-art MOS technology with a very advanced architectural design philosophy, this family brings mainframe computer processing power to VLSI processors.

The Series 32000 family supports a variety of system configurations, extending from a minimum low-cost system to a powerful 4 gigabyte system. The architecture provides complete upward compatibility from one family member to another. The family consists of a selection of CPUs supported by a set of peripherals and slave processors that provide sophisticated interrupt and memory management facilities as well as high-speed floating-point operations. The architectural features of the Series 32000 family are described briefly below:

Powerful Addressing Modes. Nine addressing modes available to all instructions are included to access data structures efficiently.

Data Types. The architecture provides for numerous data types, such as byte, word, doubleword, and BCD, which may be arranged into a wide variety of data structures.

Symmetric Instruction Set. While avoiding special case instructions that compilers can't use, the Series 32000 family incorporates powerful instructions for control operations, such as array indexing and external procedure calls, which save considerable space and time for compiled code.

Memory-to-Memory Operations. The Series 32000 CPUs represent two-address machines. This means that each operand can be referenced by any one of the addressing modes provided. This powerful memory-to-memory architecture permits memory locations to be treated as registers for all useful operations. This is important for temporary operands as well as for context switching.

Memory Management. Either the NS32382 or the NS32082 Memory Management Unit may be added to the system to provide advanced operating system support functions, including dynamic address translation, virtual memory management, and memory protection.

Large, Uniform Addressing. The NS32332 has 32-bit address pointers that can address up to 4 gigabytes without requiring any segmentation; this addressing scheme provides flexible memory management without added-on expense.

Modular Software Support. Any software package for the Series 32000 family can be developed independent of all other packages, without regard to individual addressing. In addition, ROM code is totally relocatable and easy to access, which allows a significant reduction in hardware and software cost.

Software Processor Concept. The Series 32000 architecture allows future expansions of the instruction set that can be executed by special slave processors, acting as extensions to the CPU. This concept of slave processors is unique to the Series 32000 family. It allows software compatibility even for future components because the slave hardware is transparent to the software. With future advances in semiconductor technology, the slaves can be physically integrated on the CPU chip itself.

To summarize, the architectural features cited above provide three primary performance advantages and characteristics:

- High-Level Language Support
- Easy Future Growth Path
- Application Flexibility

1.1 NS32332 KEY FEATURES

The NS32332 is a 32-bit CPU in the Series 32000 family. It is totally software compatible with the NS32032, NS32016, and NS32008 CPUs but with an enhanced internal implementation.

The NS32332 design goals were to achieve two to three times the throughput of the NS32032 and to provide the full 32-bit addressing inherent in the architecture.

The basic approaches to higher throughput were: fewer clock cycles per instruction, better bus use, and higher clock frequency.

An examination of the block diagram of the NS32332 shows it to be identical to that of the NS32032, except for enhanced bus interface control, a 20-byte (rather than 8-byte) instruction prefetch queue, and special hardware in the address unit. The new addressing hardware consists of a high-speed ALU, a barrel shifter on one of its inputs, and an address register. Of the throughput improvement not due to increased clock frequency, about 15% is derived from the new address unit hardware, 15% from the bus enhancements, 10% from the larger prefetch queue, and 60% from microcode improvements.

Other important aspects of the enhanced bus interface circuitry of the NS32332 are a burst access mode, designed to work with nibble and static column RAMs, read and write timing designed to support caches, and support for bus error processing.

An enhanced slave processor communication protocol is designed to achieve improved performance with the NS32382 MMU and NS32381 FPU, while still working directly with the previous NS32082 MMU and NS32081 FPU.

2.0 Architectural Description

2.1 PROGRAMMING MODEL

The Series 32000 architecture has 8 general purpose and 8 dedicated registers. All registers are 32 bits wide except the STATUS and MODULE register. These two registers are each 16 bits wide.

2.1.1 General Purpose Registers

There are eight registers for meeting high speed general storage requirements, such as holding temporary variables and addresses. The general purpose registers are free for any use by the programmer. They are thirty-two bits in length. If a general register is specified for an operand that is eight or sixteen bits long, only the low part of the register is used; the high part is not referenced or modified.

2.1.2 Dedicated Registers

The eight dedicated registers of the processor are assigned specific functions.

PC: The PROGRAM COUNTER register is a pointer to the first byte of the instruction currently being executed. The PC is used to reference memory in the program section.

SP0, SP1: The SP0 register points to the lowest address of the last item stored on the INTERRUPT STACK. This stack is normally used only by the operating system. It is used

2.0 Architectural Description (Continued)

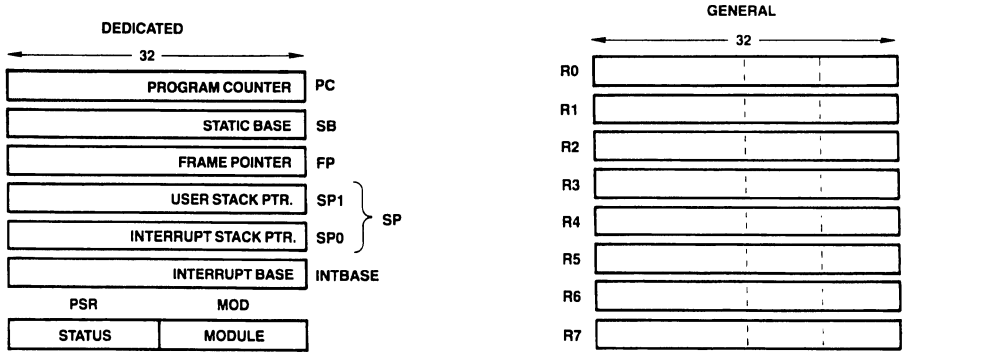

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FIGURE 2-1. The General and Dedicated Registers

primarily for storing temporary data, and holding return information for operating system subroutines and interrupt and trap service routines. The SP1 register points to the lowest address of the last item stored on the USER STACK. This stack is used by normal user programs to hold temporary data and subroutine return information.

In this document, reference is made to the SP register. The terms "SP register" or "SP" refer to either SP0 or SP1, depending on the setting of the S bit in the PSR register. If the S bit in the PSR is 0 the SP refers to SP0. If the S bit in the PSR is 1 then SP refers to SP1.

Stacks in the Series 32000 family grow downward in memory. A Push operation pre-decrements the Stack Pointer by the operand length. A Pop operation post-increments the Stack Pointer by the operand length.

FP: The FRAME POINTER register is used by a procedure to access parameters and local variables on the stack. The FP register is set up on procedure entry with the ENTER instruction and restored on procedure termination with the EXIT instruction.

The frame pointer holds the address in memory occupied by the old contents of the frame pointer.

SB: The STATIC BASE register points to the global variables of a software module. This register is used to support relocatable global variables for software modules. The SB register holds the lowest address in memory occupied by the global variables of a module.

INTBASE: The INTERRUPT BASE register holds the address of the dispatch table for interrupts and traps (Sec. 3.8). The INTBASE register holds the lowest address in memory occupied by the dispatch table.

MOD: The MODULE register holds the address of the module descriptor of the currently executing software module. The MOD register is sixteen bits long, therefore the module table must be contained within the first 64K bytes of memory.

PSR: The PROCESSOR STATUS REGISTER (PSR) holds the status codes for the microprocessor.

The PSR is sixteen bits long, divided into two eight-bit halves. The low order eight bits are accessible to all programs, but the high order eight bits are accessible only to programs executing in Supervisor Mode.

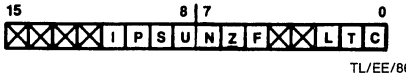

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FIGURE 2-2. Processor Status Register

C: The C bit indicates that a carry or borrow occurred after an addition or subtraction instruction. It can be used with the ADDC and SUBC instructions to perform multiple-precision integer arithmetic calculations. It may have a setting of 0 (no carry or borrow) or 1 (carry or borrow).

T: The T bit causes program tracing. If this bit is a 1, a TRC trap is executed after every instruction (Sec. 3.8.5).

L: The L bit is altered by comparison instructions. In a comparison instruction the L bit is set to "1" if the second operand is less than the first operand, when both operands are interpreted as unsigned integers. Otherwise, it is set to "0". In Floating Point comparisons, this bit is always cleared.

F: The F bit is a general condition flag, which is altered by many instructions (e.g., integer arithmetic instructions use it to indicate overflow).

Z: The Z bit is altered by comparison instructions. In a comparison instruction the Z bit is set to "1" if the second operand is equal to the first operand; otherwise it is set to "0".

N: The N bit is altered by comparison instructions. In a comparison instruction the N bit is set to "1" if the second operand is less than the first operand, when both operands are interpreted as signed integers. Otherwise, it is set to "0".

U: If the U bit is "1" no privileged instructions may be executed. If the U bit is "0" then all instructions may be executed. When U = 0 the processor is said to be in Supervisor Mode; when U = 1 the processor is said to be in User Mode. A User Mode program is restricted from executing certain instructions and accessing certain registers which could interfere with the operating system. For example, a User Mode program is prevented from changing the setting of the flag used to indicate its own privilege mode. A Supervisor Mode program is assumed to be a trusted part of the operating system, hence it has no such restrictions.

S: The S bit specifies whether the SP0 register or SP1 register is used as the stack pointer. The bit is automatically cleared on interrupts and traps. It may have a setting of 0 (use the SP0 register) or 1 (use the SP1 register).

2.0 Architectural Description (Continued)

P: The P bit prevents a TRC trap from occurring more than once for an instruction (Sec. 3.8.5.). It may have a setting of 0 (no trace pending) or 1 (trace pending).

I: If I = 1, then all interrupts will be accepted (Sec. 3.8.). If I = 0, only the NMI interrupt is accepted. Trap enables are not affected by this bit.

2.1.3 The Configuration Register (CFG)*

Within the Control section of the CPU is the CFG Register, which declares the presence and type of external devices. It is referenced by only one instruction, SETCFG, which is intended to be executed only as part of system initialization after reset. The format of the CFG Register is shown in *Figure 2-3*.

*The NS32332 CPU has four new bits in the CFG Register, namely P, FC, FM and FF.

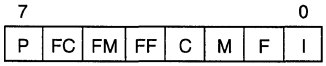


FIGURE 2-3. CFG Register

The CFG I bit declares the presence of external interrupt vectoring circuitry (specifically, the Interrupt Control Unit). If the CFG I bit is set, interrupts requested through the $\overline{INT}$ pin are "Vectored." If it is clear, these interrupts are "Non-Vectored." See Sec. 3.8.

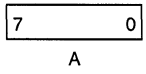
The F, M and C bits declare the presence of the FPU, MMU and Custom Slave Processors. If these bits are not set, the corresponding instructions are trapped as being undefined.

The FF, FM, FC bits define the Slave Communication Protocol to be used in FPU, MMU and Custom Slave instructions (Sec. 3.4.9). If these bits are not set, the corresponding instructions will use the 16-bit protocol (32032 compatible). If these bits are set, the corresponding instructions will use the new (fast) 32-bit protocol.

The P bit improves the efficiency of the Write Validation Buffer in the CPU. It is set if the Virtual Memory has page size(s) larger than or equal to 4 Kbytes. It is reset otherwise. In Systems where the MMU is not present, the P bit is not used.

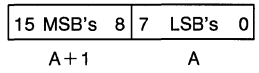
2.1.4 Memory Organization

The main memory is a uniform linear address space. Memory locations are numbered sequentially starting at zero and ending at $2^{32} - 1$. The number specifying a memory location is called an address. The contents of each memory location is a byte consisting of eight bits. Unless otherwise noted, diagrams in this document show data stored in memory with the lowest address on the right and the highest address on the left. Also, when data is shown vertically, the lowest address is at the top of a diagram and the highest address at the bottom of the diagram. When bits are numbered in a diagram, the least significant bit is given the number zero, and is shown at the right of the diagram. Bits are numbered in increasing significance and toward the left.



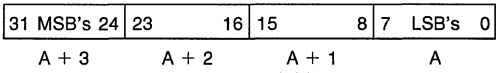
Byte at Address A

Two contiguous bytes are called a word. Except where noted (Sec. 2.2.1), the least significant byte of a word is stored at the lower address, and the most significant byte of the word is stored at the next higher address. In memory, the address of a word is the address of its least significant byte, and a word may start at any address.



Word at Address A

Two contiguous words are called a double word. Except where noted (Sec. 2.2.1), the least significant word of a double word is stored at the lowest address and the most significant word of the double word is stored at the address two greater. In memory, the address of a double word is the address of its least significant byte, and a double word may start at any address.



Double Word at Address A

Although memory is addressed as bytes, it is actually organized as double-words. Note that access time to a word or a double-word depends upon its address, e.g. double-words that are aligned to start at addresses that are multiples of four will be accessed more quickly than those not so aligned. This also applies to words that cross a double-word boundary.

2.1.5 Dedicated Tables

Two of the dedicated registers (MOD and INTBASE) serve as pointers to dedicated tables in memory.

The INTBASE register points to the Interrupt Dispatch and Cascade tables.

The MOD register contains a pointer into the Module Table, whose entries are called Module Descriptors. A Module Descriptor contains four pointers. The MOD register contains the address of the Module Descriptor for the currently running module. It is automatically up-dated by the Call External Procedure instructions (CXP and CXPD).

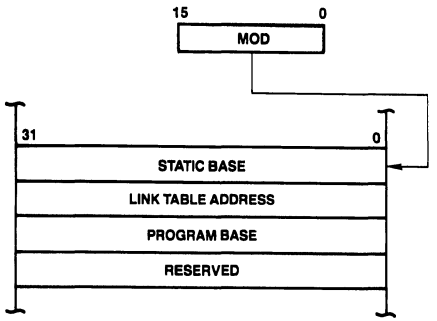


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FIGURE 2-4. Module Descriptor Format

The format of a Module Descriptor is shown in *Figure 2-4*. The Static Base entry contains the address of static data assigned to the running module. It is loaded into the CPU Static Base register by the CXP and CXPD instructions. The Program Base entry contains the address of the first byte of instruction code in the module. Since a module may have multiple entry points, the Program Base pointer serves only as a reference to find them.

2.0 Architectural Description (Continued)

The Link Table Address points to the Link Table for the currently running module. The Link Table provides the information needed for:

1) Sharing variables between modules. Such variables are accessed through the Link Table via the External addressing mode.
2) Transferring control from one module to another. This is done via the Call External Procedure (CXP) instruction.

The format of a Link Table is given in *Figure 2-5*. A Link Table Entry for an external variable contains the 32-bit address of that variable. An entry for an external procedure contains two 16-bit fields: Module and Offset. The Module field contains the new MOD register contents for the module being entered. The Offset field is an unsigned number giving the position of the entry point relative to the new module's Program Base pointer.

For further details of the functions of these tables, see the Series 32000 Instruction Set Reference Manual.

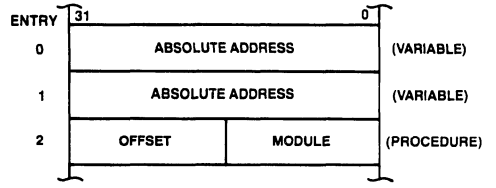

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FIGURE 2-5. A Sample Link Table

2.2 INSTRUCTION SET

2.2.1 General Instruction Format

Figure 2-6 shows the general format of a Series 32000 instruction. The Basic Instruction is one to three bytes long and contains the Opcode and up to two 5-bit General Addressing Mode ("Gen") fields. Following the Basic Instruction field is a set of optional extensions, which may appear depending on the instruction and the addressing modes selected.

Index Bytes appear when either or both Gen fields specify Scaled Index. In this case, the Gen field specifies only the Scale Factor (1, 2, 4 or 8), and the Index Byte specifies which General Purpose Register to use as the index, and which addressing mode calculation to perform before indexing. See *Figure 2-7*.

Following Index Bytes come any displacements (addressing constants) or immediate values associated with the selected address modes. Each Disp/Imm field may contain one or two displacements, or one immediate value. The size of a Displacement field is encoded with the top bits of that field, as shown in *Figure 2-8*, with the remaining bits interpreted as a signed (two's complement) value. The size of an immediate value is determined from the Opcode field. Both Displacement and Immediate fields are stored most significant byte first. Note that this is different from the memory representation of data (Sec. 2.1.4).

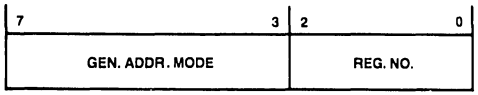

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FIGURE 2-7. Index Byte Format

Some instructions require additional, "implied" immediates and/or displacements, apart from those associated with addressing modes. Any such extensions appear at the end of the instruction, in the order that they appear within the list of operands in the instruction definition (Sec. 2.2.3).

2.2.2 Addressing Modes

The CPU generally accesses an operand by calculating its Effective Address based on information available when the operand is to be accessed. The method to be used in performing this calculation is specified by the programmer as an "addressing mode."

Addressing modes are designed to optimally support high-level language accesses to variables. In nearly all cases, a variable access requires only one addressing mode, within the instruction that acts upon that variable. Extraneous data movement is therefore minimized.

Addressing Modes fall into nine basic types:

Register: The operand is available in one of the eight General Purpose Registers. In certain Slave Processor instructions, an auxiliary set of eight registers may be referenced instead.

Register Relative: A General Purpose Register contains an address to which is added a displacement value from the instruction, yielding the Effective Address of the operand in memory.

Memory Space. Identical to Register Relative above, except that the register used is one of the dedicated registers PC, SP, SB or FP. These registers point to data areas generally needed by high-level languages.

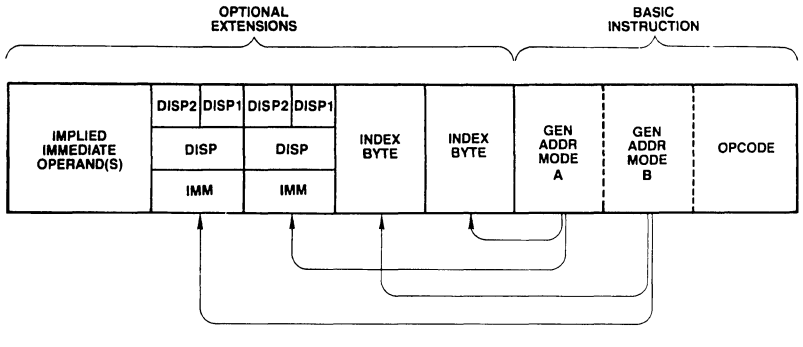

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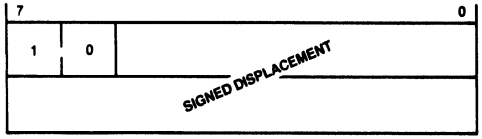
FIGURE 2-6. General Instruction Format

2.0 Architectural Description (Continued)

BYTE DISPLACEMENT: RANGE −64 TO +63

WORD DISPLACEMENT: RANGE −8192 TO +8191



DOUBLE WORD DISPLACEMENT: RANGE $-(2^{29}-2^{24})$ to $+(2^{29}-1)$*

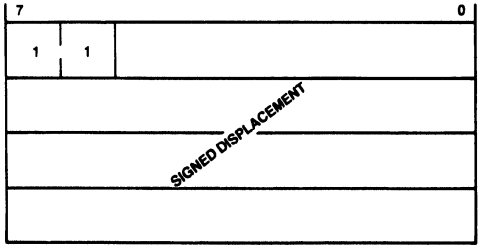


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FIGURE 2-8. Displacement Encodings

***Note: The pattern "11100000" for the most significant byte of the displacement is reserved by National for future enhancements. Therefore, it should never be used by the user program. This causes the lower limit of the displacement range to be $-(2^{29}-2^{24})$ instead of -2^{29}.**

Memory Relative: A pointer variable is found within the memory space pointed to by the SP, SB or FP register. A displacement is added to that pointer to generate the Effective Address of the operand.

Immediate: The operand is encoded within the instruction. This addressing mode is not allowed if the operand is to be written.

Absolute: The address of the operand is specified by a displacement field in the instruction.

External: A pointer value is read from a specified entry of the current Link Table. To this pointer value is added a displacement, yielding the Effective Address of the operand.

Top of Stack: The currently-selected Stack Pointer (SP0 or SP1) specifies the location of the operand. The operand is pushed or popped, depending on whether it is written or read.

Scaled Index: Although encoded as an addressing mode. Scaled Indexing is an option on any addressing mode except Immediate or another Scaled Index. It has the effect of calculating an Effective Address, then multiplying any General Purpose Register by 1, 2, 4 or 8 and adding it into the total, yielding the final Effective Address of the operand.

Table 2-1 is a brief summary of the addressing modes. For a complete description of their actions, see the Instruction Set Reference Manual.

2.2.3 Instruction Set Summary

Table 2-2 presents a brief description of the Series 32000 instruction set. The Format column refers to the Instruction Format tables (Appendix A). The Instruction column gives the instruction as coded in assembly language, and the Description column provides a short description of the function provided by that instruction. Further details of the exact operations performed by each instruction may be found in the Instruction Set Reference Manual.

Notations:

i = Integer length suffix: B = Byte
W = Word
D = Double Word

f = Floating Point length suffix: F = Standard Floating
L = Long Floating

gen = General operand. Any addressing mode can be specified.

short = A 4-bit value encoded within the Basic Instruction (see Appendix A for encodings).

imm = Implied immediate operand. An 8-bit value appended after any addressing extensions.

disp = Displacement (addressing constant): 8, 16 or 32 bits. All three lengths legal.

reg = Any General Purpose Register: R0–R7.

areg = Any Dedicated/Address Register: SP, SB, FP, MOD, INTBASE, PSR, US (bottom 8 PSR bits).

mreg = Any Memory Management Status/Control Register.

creg = A Custom Slave Processor Register (Implementation Dependent).

cond = Any condition code, encoded as a 4-bit field within the Basic Instruction (see Appendix A for encodings).

2.0 Architectural Description (Continued)

TABLE 2-1
NS32332 Addressing Modes

ENCODING	MODE	ASSEMBLER SYNTAX	EFFECTIVE ADDRESS
Register			
00000	Register 0	R0 or F0	None: Operand is in the specified register
00001	Register 1	R1 or F1	
00010	Register 2	R2 or F2	
00011	Register 3	R3 or F3	
00100	Register 4	R4 or F4	
00101	Register 5	R5 or F5	
00110	Register 6	R6 or F6	
00111	Register 7	R7 or F7	
Register Relative			
01000	Register 0 relative	disp(R0)	Disp + Register.
01001	Register 1 relative	disp(R1)	
01010	Register 2 relative	disp(R2)	
01011	Register 3 relative	disp(R3)	
01100	Register 4 relative	disp(R4)	
01101	Register 5 relative	disp(R5)	
01110	Register 6 relative	disp(R6)	
01111	Register 7 relative	disp(R7)	
Memory Relative			
10000	Frame memory relative	disp2(disp1(FP))	Disp2 + Pointer; Pointer found at address Disp1 + Register. "SP" is either SP0 or SP1, as selected in PSR.
10001	Stack memory relative	disp2(disp1(SP))	
10010	Static memory relative	disp2(disp1(SB))	
Reserved			
10011	(Reserved for Future Use)		
Immediate			
10100	Immediate	value	None: Operand is input from instruction queue.
Absolute			
10101	Absolute	@disp	Disp.
External			
10110	External	EXT (disp1) + disp2	Disp2 + Pointer; Pointer is found at Link Table Entry number Disp1.
Top of Stack			
10111	Top of stack	TOS	Top of current stack, using either User or Interrupt Stack Pointer, as selected in PSR. Automatic Push/Pop included.
Memory Space			
11000	Frame memory	disp(FP)	Disp + Register; "SP" is either SP0 or SP1, as selected in PSR.
11001	Stack memory	disp(SP)	
11010	Static memory	disp(SB)	
11011	Program memory	*+disp	
Scaled Index			
11100	Index, bytes	mode[Rn:B]	EA (mode) + Rn.
11101	Index, words	mode[Rn:W]	EA (mode) + 2× Rn.
11110	Index, double words	mode[Rn:D]	EA (mode) + 4× Rn.
11111	Index, quad words	mode[Rn:Q]	EA (mode) + 8 × Rn. 'Mode' and 'n' are contained within the Index Byte. EA (mode) denotes the effective address generated using mode.

2.0 Architectural Description (Continued)

TABLE 2-2
Series 32000 Instruction Set Summary

MOVES

Format	Operation	Operands	Description
4	MOVi	gen,gen	Move a value.
2	MOVQi	short,gen	Extend and move a signed 4-bit constant.
7	MOVMi	gen,gen,disp	Move Multiple: disp bytes (1 to 16).
7	MOVZBW	gen,gen	Move with zero extension.
7	MOVZiD	gen,gen	Move with zero extension.
7	MOVXBW	gen,gen	Move with sign extension.
7	MOVXiD	gen,gen	Move with sign extension.
4	ADDR	gen,gen	Move Effective Address.

INTEGER ARITHMETIC

Format	Operation	Operands	Description
4	ADDI	gen,gen	Add.
2	ADDQi	short,gen	Add signed 4-bit constant.
4	ADDCi	gen,gen	Add with carry.
4	SUBi	gen,gen	Subtract.
4	SUBCi	gen,gen	Subtract with carry (borrow).
6	NEGi	gen,gen	Negate (2's complement).
6	ABSi	gen,gen	Take absolute value.
7	MULi	gen,gen	Multiply
7	QUOi	gen,gen	Divide, rounding toward zero.
7	REMi	gen,gen	Remainder from QUO.
7	DIVi	gen,gen	Divide, rounding down.
7	MODi	gen,gen	Remainder from DIV (Modulus).
7	MEIi	gen,gen	Multiply to Extended Integer.
7	DEIi	gen,gen	Divide Extended Integer.

PACKED DECIMAL (BCD) ARITHMETIC

Format	Operation	Operands	Description
6	ADDPi	gen,gen	Add Packed.
6	SUBPi	gen,gen	Subtract Packed.

INTEGER COMPARISON

Format	Operation	Operands	Description
4	CMPi	gen,gen	Compare.
2	CMPQi	short,gen	Compare to signed 4-bit constant.
7	CMPMi	gen,gen,disp	Compare Multiple: disp bytes (1 to 16).

LOGICAL AND BOOLEAN

Format	Operation	Operands	Description
4	ANDi	gen,gen	Logical AND.
4	ORi	gen,gen	Logical OR.
4	BICi	gen,gen	Clear selected bits.
4	XORi	gen,gen	Logical Exclusive OR.
6	COMi	gen,gen	Complement all bits.
6	NOTi	gen,gen	Boolean complement: LSB only.
2	Scondi	gen	Save condition code (cond) as a Boolean variable of size i.

2.0 Architectural Description (Continued)

SHIFTS

Format	Operation	Operands	Description
6	LSHi	gen,gen	Logical Shift, left or right.
6	ASHi	gen,gen	Arithmetic Shift, left or right.
6	ROTi	gen,gen	Rotate, left or right.

BITS

Format	Operation	Operands	Description
4	TBITi	gen,gen	Test bit.
6	SBITi	gen,gen	Test and set bit.
6	SBITIi	gen,gen	Test and set bit, interlocked
6	CBITi	gen,gen	Test and clear bit.
6	CBITIi	gen,gen	Test and clear bit, interlocked.
6	IBITi	gen,gen	Test and invert bit.
8	FFSi	gen,gen	Find first set bit

BIT FIELDS

Bit fields are values in memory that are not aligned to byte boundaries. Examples are PACKED arrays and records used in Pascal. "Extract" instructions read and align a bit field. "Insert" instructions write a bit field from an aligned source.

Format	Operation	Operands	Description
8	EXTi	reg,gen,gen,disp	Extract bit field (array oriented).
8	INSi	reg,gen,gen,disp	Insert bit field (array oriented).
7	EXTSi	gen,gen,imm,imm	Extract bit field (short form).
7	INSSi	gen,gen,imm,imm	Insert bit field (short form).
8	CVTP	reg,gen,gen	Convert to Bit Field Pointer.

ARRAYS

Format	Operation	Operands	Description
8	CHECKi	reg,gen,gen	Index bounds check.
8	INDEXi	reg,gen,gen	Recursive indexing step for multiple-dimensional arrays.

STRINGS

String instructions assign specific functions to the General Purpose Registers:

R4 - Comparison Value

R3 - Translation Table Pointer

R2 - String 2 Pointer

R1 - String 1 Pointer

R0 - Limit Count

Options on all string instructions are:

B (Backward): Decrement string pointers after each step rather than incrementing.

U (Until match): End instruction if String 1 entry matches R4.

W (While match): End instruction if String 1 entry does not match R4.

All string instructions end when R0 decrements to zero.

Format	Operation	Operands	Descriptions
5	MOVSi	options	Move String 1 to String 2.
	MOVST	options	Move string, translating bytes.
5	CMPSi	options	Compare String 1 to String 2.
	CMPST	options	Compare translating, String 1 bytes.
5	SKPSi	options	Skip over String 1 entries
	SKPST	options	Skip, translating bytes for Until/While.

2.0 Architectural Description (Continued)

JUMPS AND LINKAGE

Format	Operation	Operands	Description
3	JUMP	gen	Jump.
0	BR	disp	Branch (PC Relative).
0	Bcond	disp	Conditional branch.
3	CASEi	gen	Multiway branch.
2	ACBi	short,gen,disp	Add 4-bit constant and branch if non-zero.
3	JSR	gen	Jump to subroutine.
1	BSR	disp	Branch to subroutine.
1	CXP	disp	Call external procedure.
3	CXPD	gen	Call external procedure using descriptor.
1	SVC		Supervisor Call.
1	FLAG		Flag Trap.
1	BPT		Breakpoint Trap.
1	ENTER	[reg list],disp	Save registers and allocate stack frame (Enter Procedure).
1	EXIT	[reg list]	Restore registers and reclaim stack frame (Exit Procedure).
1	RET	disp	Return from subroutine.
1	RXP	disp	Return from external procedure call.
1	RETT	disp	Return from trap. (Privileged)
1	RETI		Return from interrupt. (Privileged)

CPU REGISTER MANIPULATION

Format	Operation	Operands	Description
1	SAVE	[reg list]	Save General Purpose Registers.
1	RESTORE	[reg list]	Restore General Purpose Registers.
2	LPRi	areg,gen	Load Dedicated Register. (Privileged if PSR or INTBASE)
2	SPRi	areg,gen	Store Dedicated Register. (Privileged if PSR or INTBASE)
3	ADJSPi	gen	Adjust Stack Pointer.
3	BISPSRi	gen	Set selected bits in PSR. (Privileged if not Byte length)
3	BICPSRi	gen	Clear selected bits in PSR. (Privileged if not Byte length)
5	SETCFG	[option list]	Set Configuration Register. (Privileged)

FLOATING POINT

Format	Operation	Operands	Description
11	MOVf	gen,gen	Move a Floating Point value.
9	MOVLF	gen,gen	Move and shorten a Long value to Standard.
9	MOVFL	gen,gen	Move and lengthen a Standard value to Long.
9	MOVif	gen,gen	Convert any integer to Standard or Long Floating.
9	ROUNDfi	gen,gen	Convert to integer by rounding.
9	TRUNCfi	gen,gen	Convert to integer by truncating, toward zero.
9	FLOORfi	gen,gen	Convert to largest integer less than or equal to value.
11	ADDf	gen,gen	Add.
11	SUBf	gen,gen	Subtract.
11	MULf	gen,gen	Multiply.
11	DIVf	gen,gen	Divide.
11	CMPf	gen,gen	Compare.
11	NEGf	gen,gen	Negate.
11	ABSf	gen,gen	Take absolute value.
12	POLYf	gen,gen	Polynomial Step.
12	DOTf	gen,gen	Dot Product.
12	SCALBf	gen,gen	Binary Scale.
12	LOGBf	gen,gen	Binary Log.
9	LFSR	gen	Load FSR.
9	SFSR	gen	Store FSR.

2.0 Architectural Description (Continued)

MEMORY MANAGEMENT

Format	Operation	Operands	Description
14	LMR	mreg,gen	Load Memory Management Register. (Privileged)
14	SMR	mreg,gen	Store Memory Management Register. (Privileged)
14	RDVAL	gen	Validate address for reading. (Privileged)
14	WRVAL	gen	Validate address for writing. (Privileged)
8	MOVSUi	gen,gen	Move a value from Supervisor Space to User Space. (Privileged)
8	MOVUSi	gen,gen	Move a value from User Space to Supervisor Space. (Privileged)

MISCELLANEOUS

Format	Operation	Operands	Description
1	NOP		No Operation.
1	WAIT		Wait for interrupt.
1	DIA		Diagnose. Single-byte "Branch to Self" for hardware breakpointing. Not for use in programming.

CUSTOM SLAVE

Format	Operation	Operands	Description
15.5	CCAL0c	gen,gen	Custom Calculate.
15.5	CCAL1c	gen,gen	
15.5	CCAL2c	gen,gen	
15.5	CCAL3c	gen,gen	
15.5	CMOV0c	gen,gen	Custom Move.
15.5	CMOV1c	gen,gen	
15.5	CMOV2c	gen,gen	
15.5	CMOV3c	gen,gen	
15.5	CCMP0c	gen,gen	Custom Compare.
15.5	CCMP1c	gen,gen	
15.1	CCV0ci	gen,gen	Custom Convert.
15.1	CCV1ci	gen,gen	
15.1	CCV2ci	gen,gen	
15.1	CCV3ic	gen,gen	
15.1	CCV4DQ	gen,gen	
15.1	CCV5QD	gen,gen	
15.1	LCSR	gen	Load Custom Status Register.
15.1	SCSR	gen	Store Custom Status Register.
15.0	CATST0	gen	Custom Address/Test. (Privileged)
15.0	CATST1	gen	(Privileged)
15.0	LCR	creg,gen	Load Custom Register. (Privileged)
15.0	SCR	creg,gen	Store Custom Register. (Privileged)

3.0 Functional Description

The following is a functional description of the NS32332 CPU.

3.1 POWER AND GROUNDING

The NS32332 requires a single 5-volt power supply, applied on 7 pins. The Logic Voltage pins ($V_{CC}L1$ and $V_{CC}L2$) supply the power to the on-chip logic. The Buffer Voltage pins (V_{CCB1} to V_{CCB5}) supply the power to the output drivers of the chip. The Logic Voltage pins and the Buffer Voltage pins should be connected together by a power (V_{CC}) plane on the printed circuit board.

The NS32332 grounding connections are made on 8 pins. The Logic Ground pins (GNDL1 and GNDL2) are the ground pins for the on-chip logic. The Buffer Ground pins (GNDB1 to GNDB6) are the ground pins for the output drivers of the chip. The Logic Ground pins and the Buffer Ground pins should be connected together by a ground plane on the printed circuit board.

In addition to V_{CC} and Ground, the NS32332 CPU uses an internally-generated negative voltage. It is necessary to filter this voltage externally by attaching a pair of capacitors (*Figure 3.1*) from the BBG pin to Ground.

Recommended values for these are:

C1: 1 μF, Tantalum

C2: 1000 pF, Low inductance. This should be either a disc or monolithic capacitor.

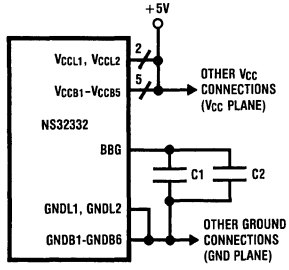

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FIGURE 3-1. Recommended Supply Connections

3.2 CLOCKING

The NS32332 inputs clocking signals from the Timing Control Unit (TCU), which presents two non-overlapping phases of a single clock frequency. These phases are called PHI1 (pin A7) and PHI2 (pin B8). Their relationship to each other is shown in *Figure 3-2*.

Each rising edge of PHI1 defines a transition in the timing state ("T-State") of the CPU. One T-State represents the execution of one microinstruction within the CPU, and/or one step of an external bus transfer. See Sec. 4 for complete specifications of PHI1 and PHI2.

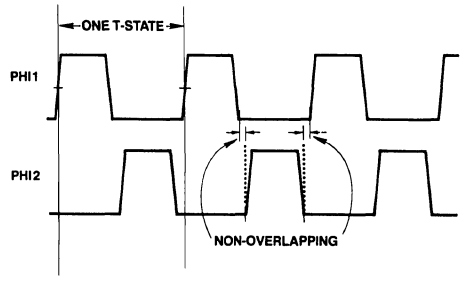

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FIGURE 3-2. Clock Timing Relationships

As the TCU presents signals with very fast transitions, it is recommended that the conductors carrying PHI1 and PHI2 be kept as short as possible, and that they not be connected anywhere except from the TCU to the CPU and, if present, the MMU. A TTL Clock signal (CTTL) is provided by the TCU for all other clocking.

3.3 RESETTING

The $\overline{RST}/\overline{ABT}$ pin serves both as a Reset for on-chip logic and as the Abort input for Memory-Managed systems. For its use as the Abort Command, see Sec. 3.5.2.

The $\overline{DT}/\overline{SDONE}$ pin is sampled on the rising edge of PHI1, one cycle before the reset signal is deasserted to select the data timing during write cycles. If $\overline{DT}/\overline{SDONE}$ is sampled high, AD0–AD31 are floated during state T2 and the data is output during state T3. This mode must be selected if an MMU is used (Section 3.5). If $\overline{DT}/\overline{SDONE}$ is sampled low, the data is output during state T2. See *Figure 3-7*.

The CPU may be reset at any time by pulling the $\overline{RST}/\overline{ABT}$ pin low for at least 64 clock cycles. Upon detecting a reset, the CPU terminates instruction processing, resets its internal logic, and clears the Program Counter (PC) and Processor Status Register (PSR) to all zeroes.

On application of power, $\overline{RST}/\overline{ABT}$ must be held low for at least 50 μsec after V_{CC} is stable. This is to ensure that all

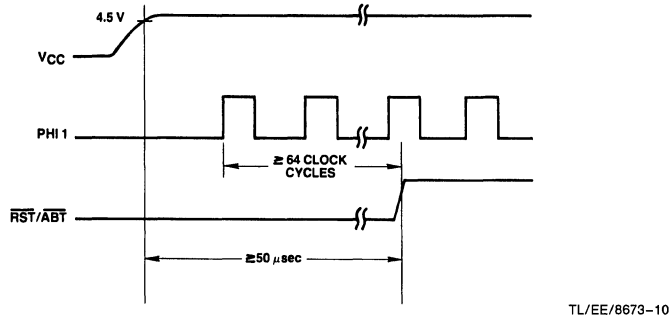

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FIGURE 3-3. Power-on Reset Requirements

3.0 Functional Description (Continued)

on-chip voltages are completely stable before operation. Whenever a Reset is applied, it must also remain active for not less than 64 clock cycles. See *Figures 3-3* and *3-4*.

The Timing Control Unit (TCU) provides circuitry to meet the Reset requirements of the NS32332 CPU. *Figure 3-5a* shows the recommended connections for a non-Memory-Managed system. *Figure 3-5b* shows the connections for a Memory-Managed system.

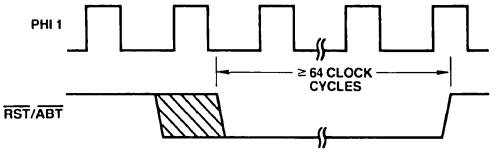

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FIGURE 3-4. General Reset Timing

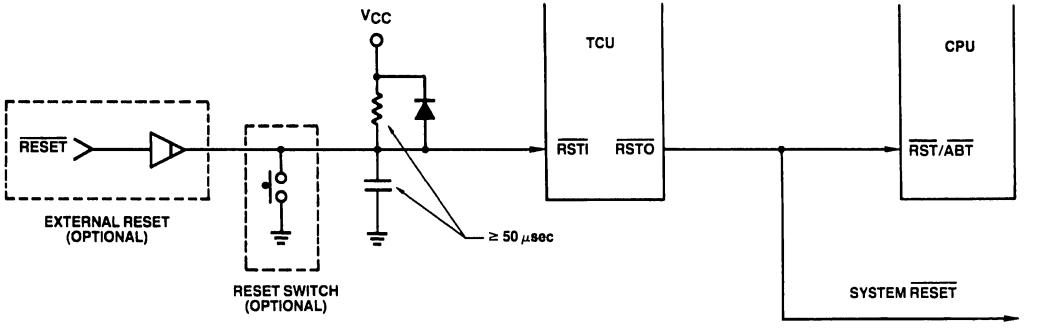

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FIGURE 3-5a. Recommended Reset Connections, Non-Memory-Managed System

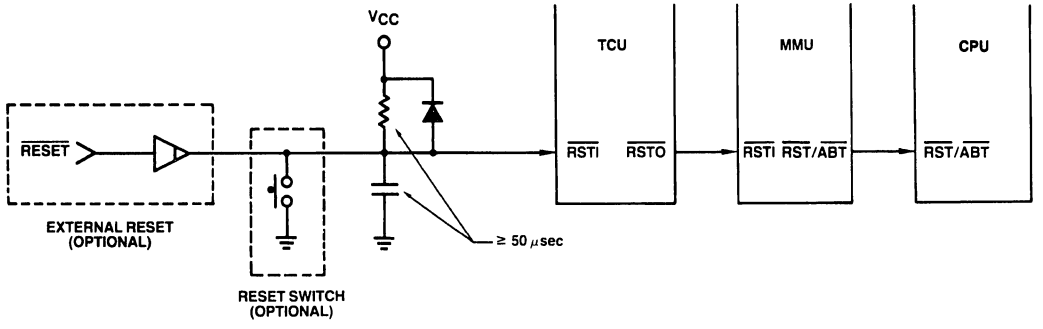

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FIGURE 3-5b. Recommended Reset Connections, Memory-Managed System

3.4 BUS CYCLES

The NS32332 CPU will perform Bus cycles for one of the following reasons:

1) To write or read data to or from memory or peripheral interface device. Peripheral input and output are memory mapped in the Series 32000 family.
2) To fetch instructions into the 20-byte instruction queue. This happens whenever the bus would otherwise be idle and the queue is not already full.
3) To acknowledge an interrupt and allow external circuitry to provide a vector number, or to acknowledge completion of an interrupt service routine.
4) To transfer information to or from a Slave Processor.

In terms of bus timing, cases 1 through 3 above are identical. For timing specifications, see Sec. 4. The only external difference between them is the 4-bit code placed on the Bus Status pins (ST0–ST3). Slave Processor cycles differ in that separate control signals are applied (Sec. 3.4.6).

For case 1 (only Read) and case 2, the NS32332 supports Burst cycles which are suitable for memories that can handle "nibble mode" accesses. (Sec. 3.4.2).

The sequence of events in a non-Slave, non-Burst Bus cycle is shown in *Figure 3-6* for a Read cycle, and *Figure 3-7* for a Write cycle. The cases shown assume that the selected memory or interface device is capable of communicating with the CPU at full speed. If it is not, then cycle extension may be requested through the RDY line (Sec. 3.4.1).

A full speed Bus cycle is performed in four cycles of the PHI1 clock, labeled T1 through T4. Clock cycles not associated with a Bus cycle are designated Ti (for idle).

3.0 Functional Description (Continued)

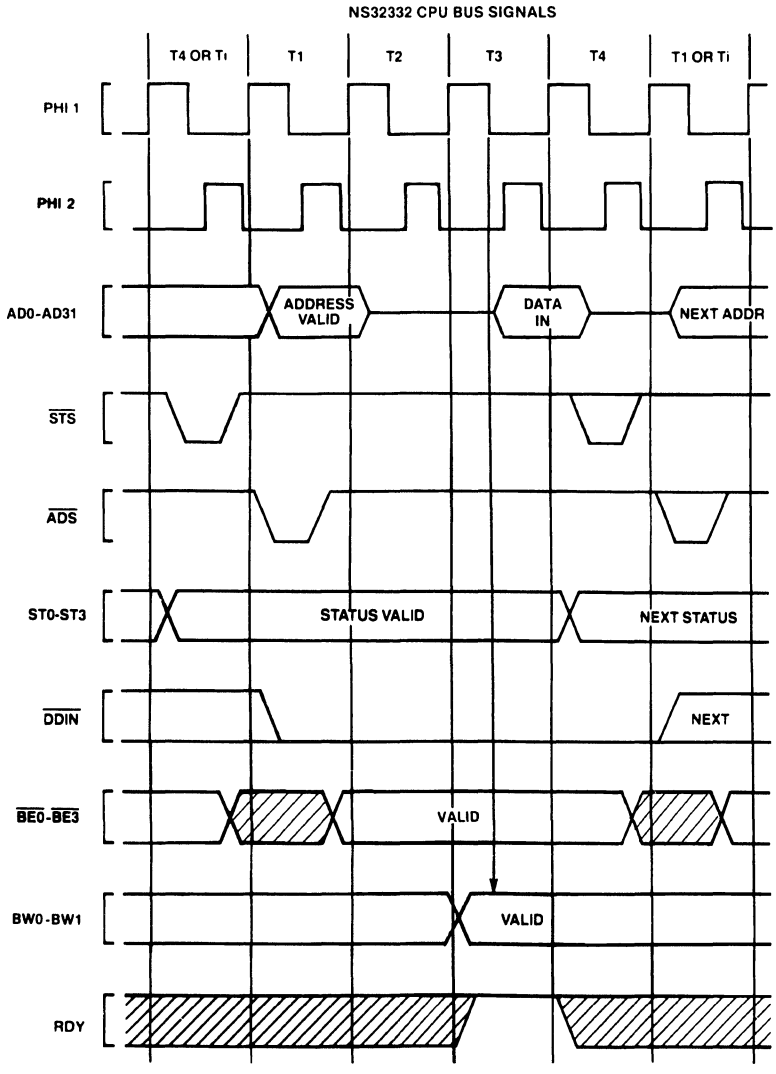

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FIGURE 3-6. Read Cycle Timing

3.0 Functional Description (Continued)

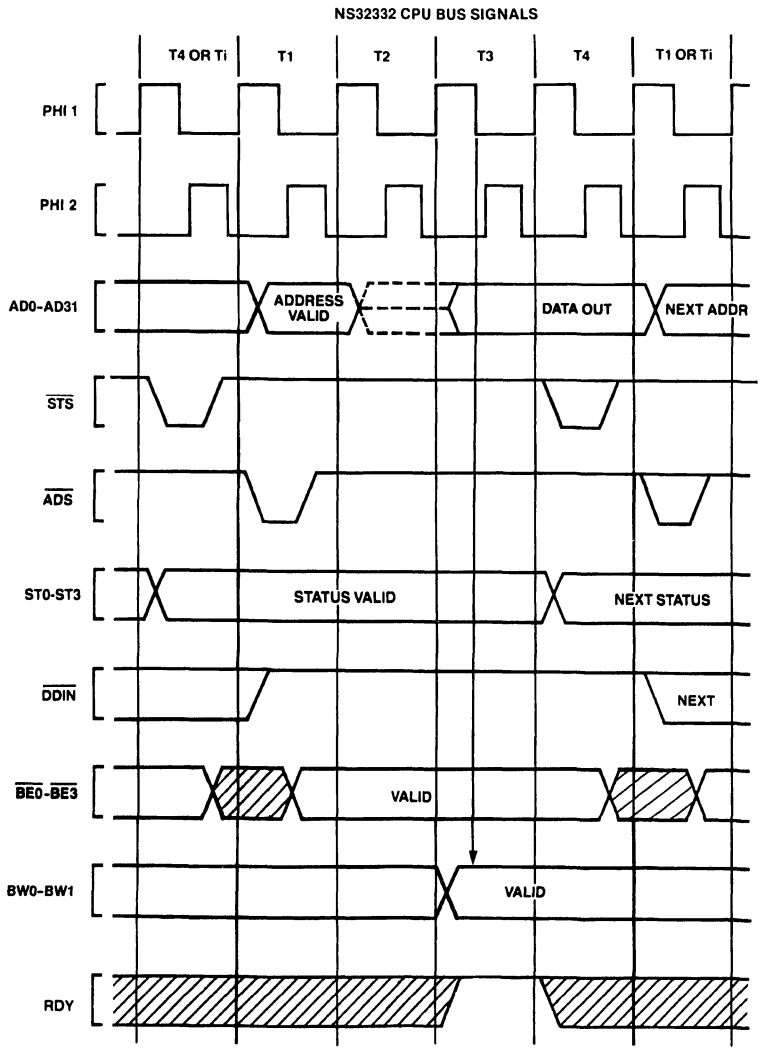

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FIGURE 3-7. Write Cycle Timing

3.0 Functional Description (Continued)

During T4 or Ti which preceed T1 of the current Bus cycle, the CPU applies a Status Code on pins ST0-ST3. It also provides a low-going pulse on the $\overline{STS}$ pin to indicate that the status code is valid.

The $\overline{ADS}$ signal has the dual purpose of informing the external circuitry that a Bus cycle is starting and of providing control to an external latch for demultiplexing address bits 0-31 from AD0-AD31 pins. (See *Figure 3-8.*)

During this time, the control signal $\overline{DDIN}$, which indicates the direction of the transfer, and $\overline{BE0}$-$\overline{BE3}$ which indicate which of the four bus bytes to be referenced, become valid. Note that during Instruction Fetch cycles $\overline{BE0}$-$\overline{BE3}$ are all active, but in operand Read or Write cycles they indicate the byte(s) to be referenced.

Note: If a burst cycle occurs during an operand read, all the memory banks should be enabled, during the burst cycle, regardless of $\overline{BE}$n. The CPU $\overline{BE}$n lines, in this case, are valid in the middle of T3 of the burst cycle—thus, there may not be enough time to selectively enable the different memory banks, unless a WAIT state is added. See *Figure 4-6.*

During T2 the CPU floats AD0-AD31 lines unless $\overline{DT/SDONE}$ is sampled low on the rising edge of reset and the bus cycle is a write cycle. T2 is a time window to be used for virtual to physical address translation by the Memory Management Unit, if virtual memory is used in the system.

The T3 state provides for access time requirements and it occurs at least once in a bus cycle. In the middle of T3 on the falling edge of PHI1, the RDY line is sampled to determine whether the bus cycle will be extended (Sec. 3.4.1).

If the CPU is performing a Read cycle, the Data Bus (AD0-AD31) is sampled on the falling edge of PHI2 of the last T3 state. See Sec. 4. Data must, however, be held at least until the beginning of T4. The T4 state finishes the Bus cycle. Data from the CPU during Write cycles remains valid throughout T4. Note that the Bus Status lines (ST0-ST3) change at the beginning of T4, anticipating the following bus cycle (if any).

3.4.1 Cycle Extension

To allow sufficient strobe widths and access times for any speed of memory or peripheral device, the NS32332 provides for extension of a bus cycle. Any type of bus cycle except a Slave Processor cycle can be extended.

In *Figures 3-7* and *3-8*, note that during T3 all bus control signals from the CPU and TCU are flat. Therefore, a bus cycle can be cleanly extended by causing the T3 state to be repeated. This is the purpose of the RDY (Ready) pin.

In the middle of T3 on the falling edge of PHI1, the RDY line is sampled by the CPU. If RDY is high, the next T-state will be T4, ending the bus cycle. If RDY is low, then another T3 state will be inserted and the RDY line will again be sampled on the falling edge of PHI1. Each additional T3 state after the first is referred to as a "WAIT STATE". See *Figure 3-9.*

Figure 3-10 illustrates a typical Read cycle, with two WAIT states requested through the RDY pin.

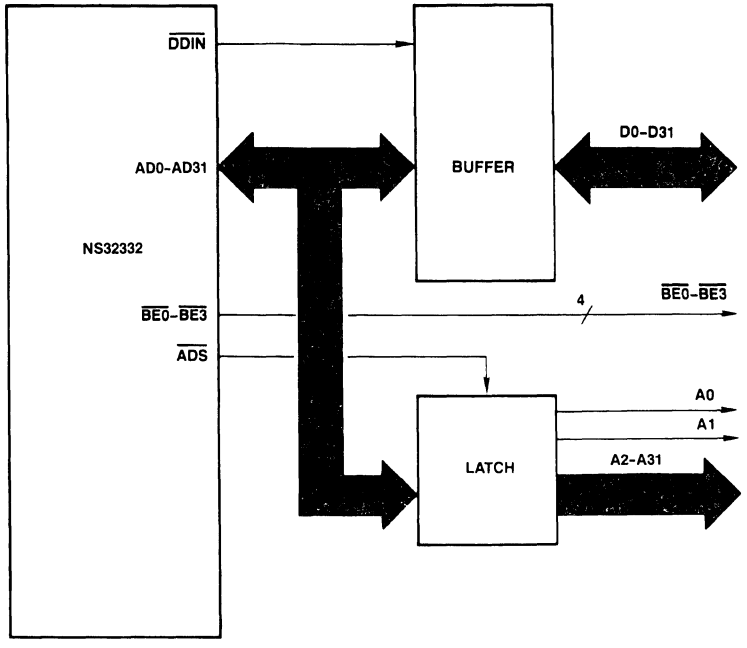

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FIGURE 3-8. Bus Connections

3.0 Functional Description (Continued)

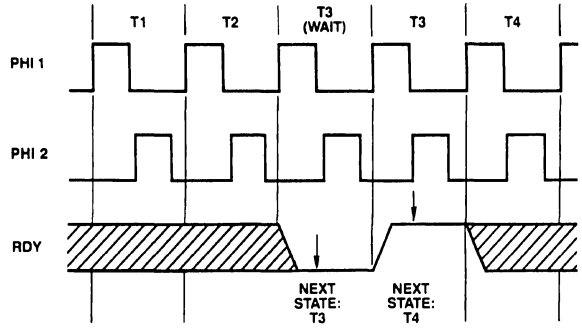

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FIGURE 3-9. RDY Pin Timing

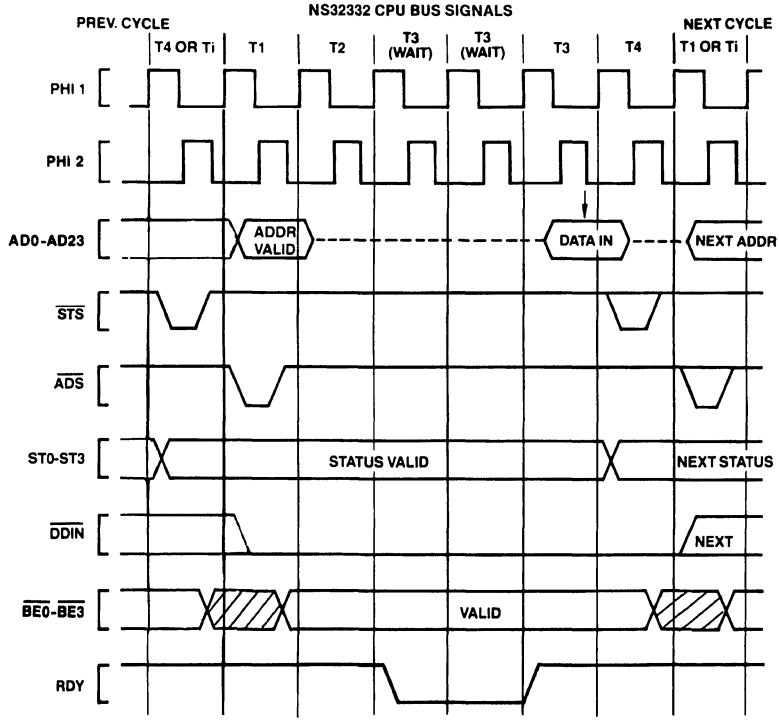

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FIGURE 3-10. Extended Cycle Example

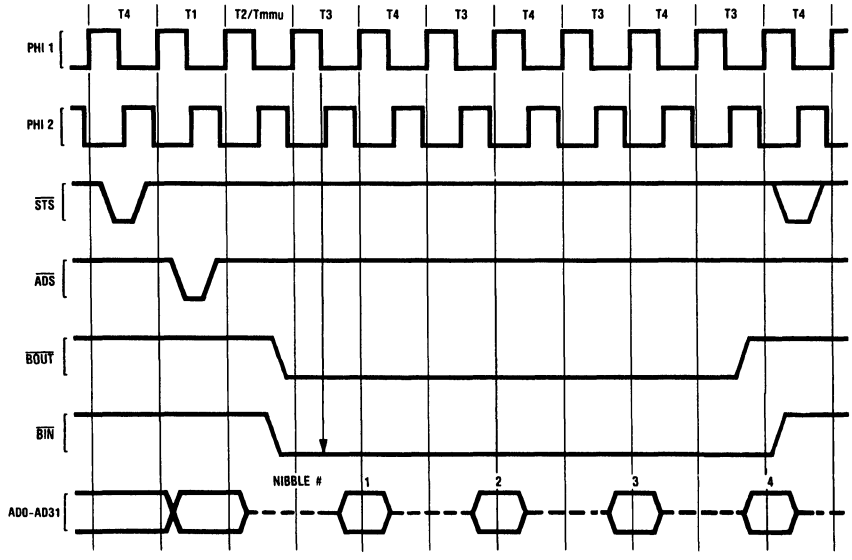
3.0 Functional Description (Continued)

3.4.2 Burst Cycles

The NS32332 is capable of performing Burst cycles in order to increase the bus throughput. Burst is available in instruction Fetch cycles and operand Read cycles only. Burst is not supported in operand Write cycles or Slave cycles.

The sequence of events for Burst cycles is shown in *Figure 3-11*. The cases shown assume that the selected memory is capable of communicating with the CPU at full speed. If it is not, then cycle extension may be requested through the RDY line (Sec. 3.4.1).

A Burst cycle is composed of two parts. The first part is a regular cycle (i.e. T1 through T4), in which the CPU outputs the new status and asserts all the other relevant control signals discussed in Sec. 3.4. In addition, the Burst Out Signal ($\overline{BOUT}$) is activated by the CPU indicating that the CPU can perform Burst cycles. If the selected memory allows



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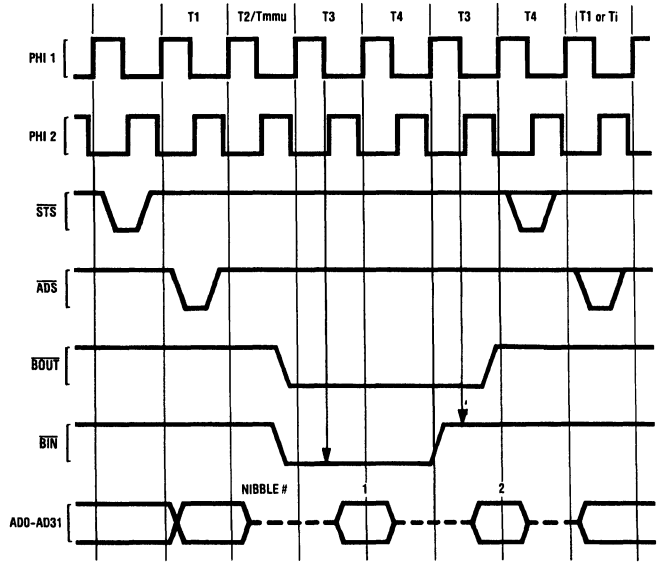
(a) Normal Termination of Burst



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(b) External Termination of Burst

FIGURE 3-11. Burst Cycles (For Read Only)

3.0 Functional Description (Continued)

Burst cycles, it will notify the CPU by activating the burst in signal ($\overline{BIN}$). $\overline{BIN}$ is sampled by the CPU in the middle of T3 on the falling edge of PHI1. If the memory does not allow burst ($\overline{BIN}$ high), the cycle will terminate through T4 and $\overline{BOUT}$ will go inactive immediately. If the memory allows burst ($\overline{BIN}$ low), and the CPU has not deasserted $\overline{BOUT}$, the second part of the Burst cycle will be performed (see *Figure 3-11*) and $\overline{BOUT}$ will remain active until termination of the Burst.

The second part consists of up to 3 nibbles. In each nibble, a data item is read by the CPU. The duration of each nibble is 2 clock cycles labeled T3 and T4.

The Burst chain will be terminated in the following cases:

1. The CPU has reached a 16 byte boundary i.e. the byte address of the current nibble is x...x1111 (binary).
2. The CPU detects that the instructions being prefetched (in Burst Mode) are no longer needed due to an alteration of the flow of control. This happens, for example, when a branch instruction is executed or an exception occurs.

Note: In 16-bit bus systems (see Sec. 3.4.7) the Burst chain will be terminated by the CPU on an 8-byte boundary i.e. address x..x111 (binary) and in 8-bit bus system on a 4-byte boundary i.e. address x...x11 (binary).

3. The data operand has been completely read. This applies to burst read cycles for non-aligned operands or when the bus width is either 8 or 16 bits.
4. $\overline{BIN}$, sampled in the current nibble's last T3, is not active any more. (See *Figure 3.11b*).
5. Bus Error or Bus Retry occurs (see Sec. 3.4.8).
6. A $\overline{HOLD}$ Request occurs.

Any nibble's T3 may be extended with WAIT states using the RDY line as described in Sec. 3.4.2.

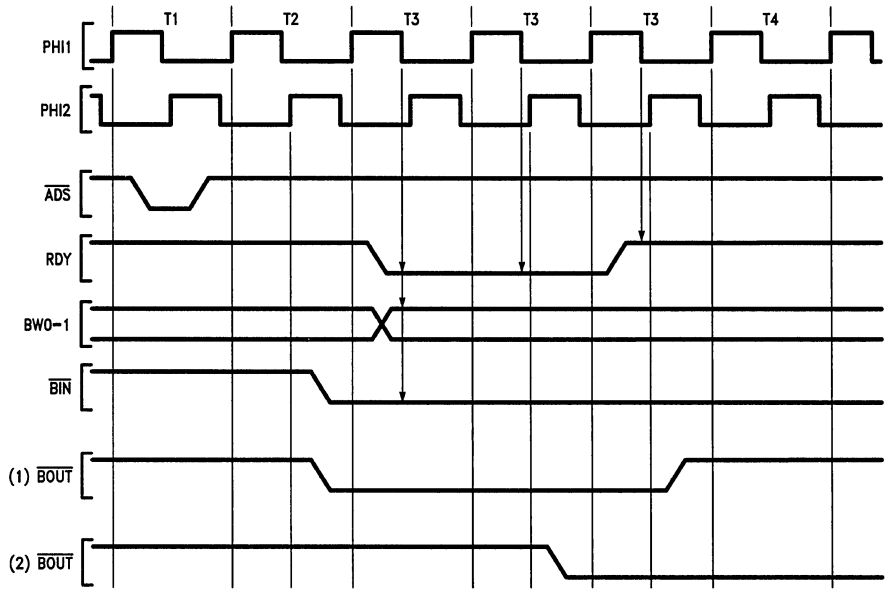
The control signals $\overline{BOUT}$, ST0–ST3, and $\overline{DDIN}$ remain stable during the Burst chain.

$\overline{BE0}$–$\overline{BE3}$ are adjusted for every nibble in operand cycles.

$\overline{BOUT}$ is initially set by the CPU according to the known bus width. Its state may change in a subsequent T3 as a result of a change in the bus width. *Figure 3-12* shows the resulting $\overline{BOUT}$ timing.

Note: If the selected memory is capable of handling burst transfers, it should activate $\overline{BIN}$ regardless of the state of $\overline{BOUT}$.

The reason is that $\overline{BOUT}$ may be activated by the CPU after the $\overline{BIN}$ sampling time. The $\overline{BOUT}$ signal indicates when the CPU is going to burst, and should not be interpreted as a 'Burst Request' signal.



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Note 1: CPU deasserts $\overline{BOUT}$.

Note 2: CPU asserts $\overline{BOUT}$.

FIGURE 3-12. $\overline{BOUT}$ Timing Resulting from a Bus Width Change

3.0 Functional Description (Continued)

3.4.3 Bus Status

The NS32332 CPU presents four bits of Bus Status information on pins ST0–ST3. The various combinations on these pins indicate why the CPU is performing a bus cycle, or, if it is idle on the bus, then why is it idle.

Referring to *Figures 3-6* and *3-7*, note that Bus Status leads the corresponding Bus Cycle, going valid one clock cycle before T1, and changing to the next state at T4. This allows the system designer to fully decode the Bus Status and, if desired, latch the decoded signals before $\overline{ADS}$ initiates the Bus Cycle.

The Bus Status pins are interpreted as a four-bit value, with ST0 the least significant bit. Their values decode as follows:

0000 – The bus is idle because the CPU does not yet need to perform a bus access.

0001 – The bus is idle because the CPU is executing the WAIT instruction.

0010 – (Reserved for future use.)

0011 – The bus is idle because the CPU is waiting for a Slave Processor to complete an instruction.

0100 – Interrupt Acknowledge, Master.

The CPU is performing a Read cycle. To acknowledge receipt of a Non-Maskable Interrupt (on $\overline{NMI}$) it will read from address $FFFFFF00_{16}$, but will ignore any data provided.

To acknowledge receipt of a Maskable Interrupt (on $\overline{INT}$) it will read from address $FFFFFE00_{16}$, expecting a vector number to be provided from the Master Interrupt Control Unit. If the vectoring mode selected by the last SETCFG instruction was Non-Vectored, then the CPU will ignore the value it has read and will use a default vector instead. See Sec. 3.4.5.

0101 – Interrupt Acknowledge, Cascaded.

The CPU is reading a vector number from a Cascaded Interrupt Control Unit. The address provided is the address of ICU's Hardware Vector register. See Sec. 3.4.6.

0110 – End of Interrupt, Master.

The CPU is performing a Read cycle to indicate that it is executing a Return from Interrupt (RETI) instruction. See Sec. 3.4.6.

0111 – End of Interrupt, Cascaded.

The CPU is reading from a Cascaded Interrupt Control Unit to indicate that it is returning (through RETI) from an interrupt service routine requested by that unit. See Sec. 3.4.6.

1000 – Sequential Instruction Fetch.

The CPU is reading the next sequential word from the instruction stream into the Instruction Queue. It will do so whenever the bus would otherwise be idle and the queue is not already full.

1001 – Non-Sequential Instruction Fetch.

The CPU is performing the first fetch of instruction code after the Instruction Queue is purged. This will occur as a result of any jump or branch, or any interrupt or trap, or execution of certain instructions.

1010 – Data Transfer.

The CPU is reading or writing an operand of an instruction.

1011 – Read RMW Operand.

The CPU is reading an operand which will subsequently be modified and rewritten. If memory protection circuitry would not allow the following Write cycle, it must abort this cycle.

1100 – Read for Effective Address Calculation.

The CPU is reading information from memory in order to determine the Effective Address of an operand. This will occur whenever an instruction uses the Memory Relative or External addressing mode.

1101 – Transfer Slave Processor Operand.

The CPU is either transferring an instruction operand to or from a Slave Processor, or it is issuing the Operation Word of a Slave Processor instruction. See Sec. 3.9.1.

1110 – Read Slave Processor Status.

The CPU is reading a Status Word from a Slave Processor. This occurs after the Slave Processor has signalled completion of an instruction. The transferred word tells the CPU whether a trap should be taken, and in some instructions it presents new values for the CPU Processor Status Register bits N, Z, L or F. See Sec. 3.9.1.

1111 – Broadcast Slave ID.

The CPU is initiating the execution of a Slave Processor instruction. The ID Byte (first byte of the instruction) is sent to all Slave Processors, one of which will recognize it. From this point the CPU is communicating with only one Slave Processor. See Sec. 3.9.1.

3.0 Functional Description (Continued)

3.4.4 Data Access Sequences

The 32-bit address provided by the NS32332 is a byte address; that is, it uniquely identifies one of up to 4 billion eight-bit memory locations. An important feature of the NS32332 is that the presence of a 32-bit data bus imposes no restrictions on data alignment; any data item, regardless of size, may be placed starting at any memory address. The NS32332 provides special control signals. Byte Enable ($\overline{BE0}$–$\overline{BE3}$) which facilitate individual byte accessing on a 32-bit bus.

Memory is organized as four eight-bit banks, each bank receiving the double-word address (A2–A31) in parallel. One bank, connected to Data Bus pins AD0–AD7 is enabled when $\overline{BE0}$ is low. The second bank, connected to data bus pins AD8–AD15 is enabled when $\overline{BE1}$ is low. The third and fourth banks are enabled by $\overline{BE2}$ and $\overline{BE3}$, respectively. See *Figure 3-13*.

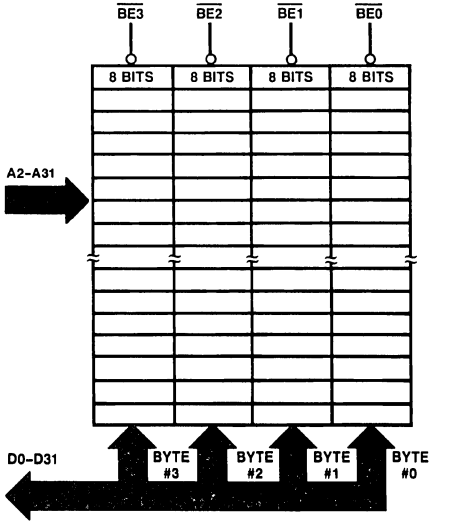

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FIGURE 3-13. Memory Interface

Since operands do not need to be aligned with respect to the double-word bus access performed by the CPU, a given double-word access can contain one, two, three, or four bytes of the operand being addressed, and these bytes can begin at various positions, as determined by A1, A0. Table 3-1 lists the 10 resulting access types.

TABLE 3-1
Bus Access Types

Type	Bytes Accessed	A1,A0	$\overline{BE3}$	$\overline{BE2}$	$\overline{BE1}$	$\overline{BE0}$
1	1	00	1	1	1	0
2	1	01	1	1	0	1
3	1	10	1	0	1	1
4	1	11	0	1	1	1
5	2	00	1	1	0	0
6	2	01	1	0	0	1
7	2	10	0	0	1	1
8	3	00	1	0	0	0
9	3	01	0	0	0	1
10	4	00	0	0	0	0

Accesses of operands requiring more than one bus cycle are performed sequentially, with no idle T-States separating them. The number of bus cycles required to transfer an operand depends on its size and its alignment. Table 3-2 lists the bus cycles performed for each situation.

3.4.4.1 Bit Accesses

The Bit Instructions perform byte accesses to the byte containing the designated bit. The Test and Set Bit instruction (SBIT), for example, reads a byte, alters it, and rewrites it, having changed the contents of one bit.

3.4.4.2 Bit Field Accesses

An access to a Bit Field in memory always generates a Double-Word transfer at the address containing the least significant bit of the field. The Double Word is read by an Extract instruction; an Insert instruction reads a Double Word, modifies it, and rewrites it.

3.4.4.3 Extending Multiple Accesses

The Extending Multiply Instruction (MEI) will return a result which is twice the size in bytes of the operand it reads. If the multiplicand is in memory, the most-significant half of the result is written first (at the higher address), then the least-significant half. This is done in order to support retry if this instruction is aborted.

3.4.5 Instruction Fetches

Instructions for the NS32332 CPU are "prefetched"; that is, they are input before being needed into the next available entry of the twenty-byte Instruction Queue. The CPU performs two types of Instruction Fetch cycles: Sequential and Non-Sequential. These can be distinguished from each other by their differing status combinations on pins ST0–ST3 (Sec. 3.4.3).

A Sequential Fetch will be performed by the CPU whenever the Data Bus would otherwise be idle and the Instruction Queue is not currently full. Sequential Fetches are always type 10 Read cycles (Table 3-1).

A Non-Sequential Fetch occurs as a result of any break in the normally sequential flow of a program. Any jump or branch instruction, a trap or an interrupt will cause the next Instruction Fetch cycle to be Non-Sequential. In addition, certain instructions flush the instruction queue, causing the next instruction fetch to display Non-Sequential status. Only the first bus cycle after a break displays Non-Sequential status, and that cycle depends on the destination address.

If a non-sequential fetch is followed by additional sequential fetches which are burst continuation of the non-sequential fetch, then the Status Bus (ST0–ST3) remains the same.

Note 1: During instruction fetch cycles, $\overline{BE0}$–$\overline{BE3}$ are all active regardless of the alignment.

Note 2: During Operand Access cycles $\overline{BE0}$–$\overline{BE3}$ are activated as if the bus is 32 bits wide, regardless of the real width.

3.4.6 Interrupt Control Cycles

Activating the $\overline{INT}$ or $\overline{NMI}$ pin on the CPU will initiate one or more bus cycles whose purpose is interrupt control rather than the transfer of instructions or data. Execution of the Return from Interrupt instruction (RETI) will also cause Interrupt Control bus cycles. These differ from instruction or data transfers only in the status presented on pins ST0–ST3. All Interrupt Control cycles are single-byte Read cycles.

This section describes only the Interrupt Control sequences associated with each interrupt and with the return from its service routine.

3.0 Functional Description (Continued)

TABLE 3-2
Access Sequences

Cycle	Type	Address	$\overline{BE3}$	$\overline{BE2}$	$\overline{BE1}$	$\overline{BE0}$	Data Bus Byte 3	Byte 2	Byte 1	Byte 0
A. ***Word at address ending with 11***									BYTE 1 | BYTE 0	← A
1.	4	A	0	1	1	1	Byte 0	X	X	X
2.	1	A + 1	1	1	1	0	X	X	X	Byte 1
B. ***Double word at address ending with 01***								BYTE 3 | BYTE 2 | BYTE 1 | BYTE 0		← A
1.	9	A	0	0	0	1	Byte 2	Byte 1	Byte 0	X
2.	1	A + 3	1	1	1	0	X	X	X	Byte 3
C. ***Double word at address ending with 10***								BYTE 3 | BYTE 2 | BYTE 1 | BYTE 0		← A
1.	7	A	0	0	1	1	Byte 1	Byte 0	X	X
2.	5	A + 2	1	1	0	0	X	X	Byte 3	Byte 2
D. ***Double word at address ending with 11***								BYTE 3 | BYTE 2 | BYTE 1 | BYTE 0		← A
1.	4	A	0	1	1	1	Byte 0	X	X	X
2.	8	A + 1	1	0	0	0	X	Byte 3	Byte 2	Byte 1
E. ***Quad word at address ending with 00***							BYTE 7 | BYTE 6 | BYTE 5 | BYTE 4 | BYTE 3 | BYTE 2 | BYTE 1 | BYTE 0			← A
1.	10	A	0	0	0	0	Byte 3	Byte 2	Byte 1	Byte 0
Other bus cycles (instruction prefetch or slave) can occur here.										
2.	10	A + 4	0	0	0	0	Byte 7	Byte 6	Byte 5	Byte 4
F. ***Quad word at address ending with 01***							BYTE 7 | BYTE 6 | BYTE 5 | BYTE 4 | BYTE 3 | BYTE 2 | BYTE 1 | BYTE 0			← A
1.	9	A	0	0	0	1	Byte 2	Byte 1	Byte 0	X
2.	1	A + 3	1	1	1	0	X	X	X	Byte 3
Other bus cycles (instruction prefetch or slave) can occur here.										
3.	9	A + 4	0	0	0	1	Byte 6	Byte 5	Byte 4	X
4.	1	A + 7	1	1	1	0	X	X	X	Byte 7
G. ***Quad word at address ending with 10***							BYTE 7 | BYTE 6 | BYTE 5 | BYTE 4 | BYTE 3 | BYTE 2 | BYTE 1 | BYTE 0			← A
1.	7	A	0	0	1	1	Byte 1	Byte 0	X	X
2.	5	A + 2	1	1	0	0	X	X	Byte 3	Byte 2
Other bus cycles (instruction prefetch or slave) can occur here.										
3.	7	A + 4	0	0	1	1	Byte 5	Byte 4	X	X
4.	5	A + 6	1	1	0	0	X	X	Byte 7	Byte 6
H. ***Quad word at address ending with 11***							BYTE 7 | BYTE 6 | BYTE 5 | BYTE 4 | BYTE 3 | BYTE 2 | BYTE 1 | BYTE 0			← A
1.	4	A	0	1	1	1	Byte 0	X	X	X
2.	8	A + 1	1	0	0	0	X	Byte 3	Byte 2	Byte 1
Other bus cycles (instruction prefetch or slave) can occur here.										
1.	4	A + 4	0	1	1	1	Byte 4	X	X	X
2.	8	A + 5	1	0	0	0	X	Byte 7	Byte 6	Byte 5

X = Don't Care

3.0 Functional Description (Continued)

TABLE 3-3
Interrupt Sequences

Cycle	Status	Address	$\overline{DDIN}$	$\overline{BE3}$	$\overline{BE2}$	$\overline{BE1}$	$\overline{BE0}$	Data Bus Byte 3	Byte 2	Byte 1	Byte 0
					A. Non-Maskable Interrupt Control Sequences						
Interrupt Acknowledge											
1	0100	$FFFFFF00_{16}$	0	1	1	1	0	X	X	X	X
Interrupt Return											
None: Performed through Return from Trap (RETT) instruction.											
					B. Non-Vectored Interrupt Control Sequences						
Interrupt Acknowledge											
1	0100	$FFFFFE00_{16}$	0	1	1	1	0	X	X	X	X
Interrupt Return											
1	0110	$FFFFFE00_{16}$	0	1	1	1	0	X	X	X	X
					C. Vectored Interrupt Sequences: Non-Cascaded.						
Interrupt Acknowledge											
1	0100	$FFFFFE00_{16}$	0	1	1	1	0	X	X	X	Vector: Range: 0-127
Interrupt Return											
1	0110	$FFFFFE00_{16}$	0	1	1	1	0	X	X	X	Vector: Same as in Previous Int. Ack. Cycle
					D. Vectored Interrupt Sequences: Cascaded						
Interrupt Acknowledge											
1	0100	$FFFFFE00_{16}$	0	1	1	1	0	X	X	X	Cascade Index: range -16 to -1
(The CPU here uses the Cascade Index to find the Cascade Address.)											
2	0101	Cascade Address	0			See Note		Vector, range 9–255; on appropriate byte of data bus.			
Interrupt Return											
1	0110	$FFFFFE00_{16}$	0	1	1	1	0	X	X	X	Cascade Index: Same as in previous Int. Ack. Cycle
(The CPU here uses the Cascade Index to find the Cascade Address)											
2	0111	Cascade Address	0			See Note		X	X	X	X

X = Don't Care

Note: $\overline{BE0}$-$\overline{BE3}$ signals will be activated according to the cascaded ICU address. The cycle type can be 1, 2, 3 or 4, when reading the interrupt vector. The vector value can be in the range 0–255.

3.0 Functional Description (Continued)

3.4.7 Dynamic Bus Configuration

The NS32332 interfaces to external data buses with 3 different widths: 8-bit, 16-bit and 32-bit. The NS32332 can switch from one bus width to another dynamically i.e. on a cycle by cycle basis.

This feature allows the user to include in his system different bus sizes for different purposes, like 8-bit bus for bootstrap ROM and 32-bit bus for cache memory, etc.

In each memory cycle, the bus width is determined by the inputs BW0 and BW1.

Four combinations exist:

BW1	BW0	
0	0	reserved
0	1	8-bit bus
1	0	16-bit bus
1	1	32-bit bus

The dynamic bus configuration is not applicable for slave cycles (see Sec. 3.4.1).

The BW0–BW1 lines are sampled by the CPU in T3 with the falling edge of PHI1 (see *Figure 3-14*).

If the bus width didn't change from the previous memory cycle, the CPU terminates the cycle normally.

If the bus width of the current cycle is different from the bus width of the previous cycle, then two WAIT states (see Sec. 3.4.1) must be inserted in order to let the CPU switch to the new width.

The additional 2 WAIT states count from the moment BW0 BW1 change. This can be overlapped with the wait states due to slow memories.

Note: BW0–BW1 can only be changed during the first T3 state of a memory access cycle. They should be externally latched and should not be changed at any other time.

In write cycles, the appropriate data will be present on the appropriate data lines. The CPU presents the data during T3 in a way that would fit any bus width.

If the operand being written is a byte, it will be duplicated on the 4 bytes AD0–AD31 depending on the operand address:

Address A0–1 =	00	XX	XX	XX	OP
	01	XX	XX	OP	OP
	10	XX	OP	XX	OP
	11	OP	XX	OP	OP

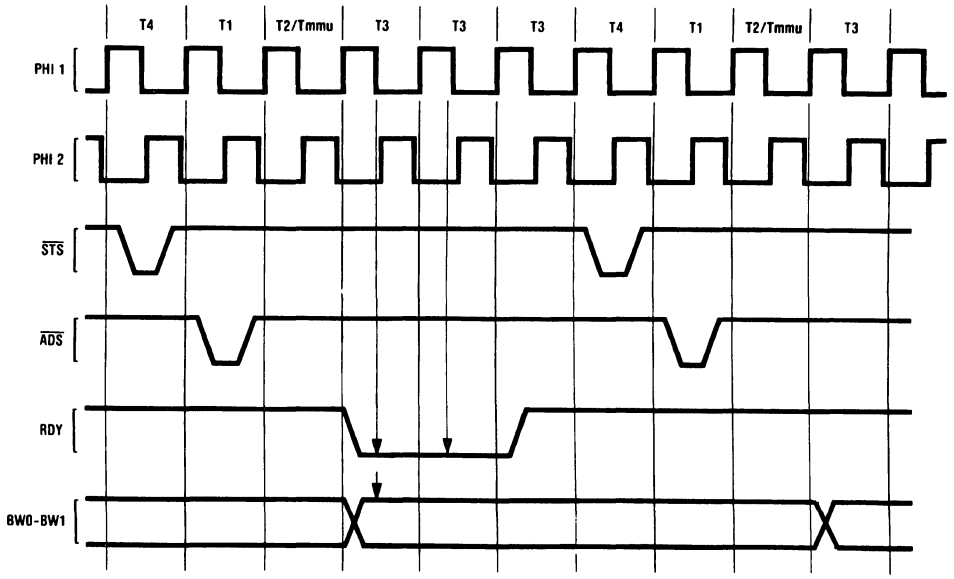

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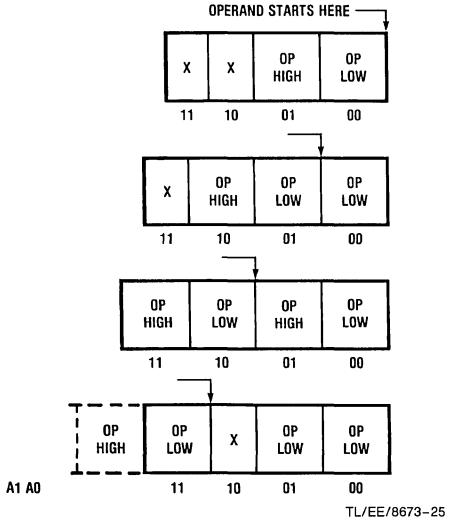
FIGURE 3-14. Bus width changes. Two wait states are required after the signals BW0–BW1 change.

3.0 Functional Description (Continued)

If the operand being written is a word, 4 cases exist. The operand address can be x...x00 (binary) or x...x01 (binary) or x...x10 or x...x11 (binary).

See the duplications for each case:



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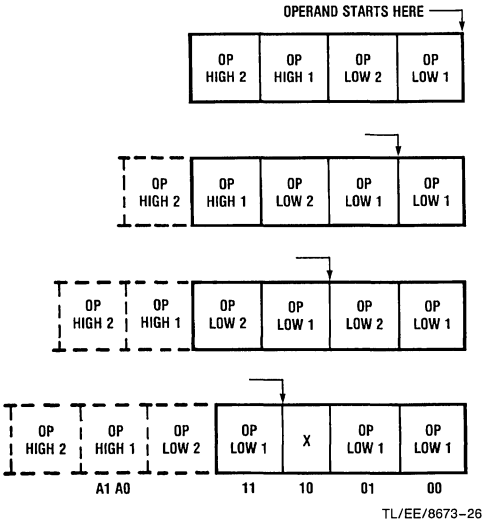

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If the operand being written is a double word 4 cases exist: The operand address can be x...x00 (binary) or x...x01 (binary) or x...x10 (binary) or x...x11 (binary).

See the duplications for each case:

Note that the organization of the operand described applies to the initial part of the operand cycle. For instance, if the CPU writes a double word operand to a 16-bit bus and the operand address is x...x11 (binary) it needs three memory cycles.

The description above applies to the first cycle. In the other 2 memory cycles belonging to the same operand, the data will be presented on the data bus lines to fit 16-bit bus width and take into account the operand length.

Example:

The CPU has to write a double word DDCCBBAA to address HEX 987653 which is in a 16-bit bus area. In the first cycle, the CPU does not know the width until T3 so it generates a cycle to address 987653 which activates the $\overline{BE3}$ line and puts on the data bus AA XX AA AA (X = don't care). After this cycle, the CPU knows it has a 16-bit bus and it generates a cycle to address 987654 which activates the BE0, BE1 and BE2 lines and puts on the data bus XX XX CC BB. The last cycle will address 987656, activate BE2, and put on the data bus XX XX XX DD. The BE0–BE3 lines are always activated as if the bus is 32-bit wide, regardless of BW0–BW1 state.

The CPU does not support a change of the bus width during a sequence of several memory references belonging to the same operand e.g. nonaligned double word. In other words, any operand should not be split between two memory spaces having different bus widths.

Instruction Fetches do not fall in this category and an Instruction Fetch can have its own bus width regardless of the bus width in the previous cycle.

3.4.8 Bus Exceptions

Any bus cycle may have a bus error during its execution. The error may be corrected during the current cycle or may be incorrectable. The NS32332 can handle both types of errors by means of BUS RETRY and BUS ERROR.

3.4.8.1 Bus Retry

If a bus error can be corrected, the CPU may be requested to repeat the erroneous bus cycle. The request is done by asserting the $\overline{BRT}$ (Bus Retry) signal.

The CPU response to Bus Retry depends on the cycle type:

Instruction Fetch Cycle—If the RETRY occurs during an instruction fetch, the fetch cycle will be retried as soon as possible. If the RETRY is requested during a burst chain, the burst is stopped and the fetch is retried. The only delay in retrying the instruction fetch may result from pending operand requests (and, of course, from hold or wait requests).

The fetch cycle will be retried only if there are no more than four bytes in the queue.

Operand Read Cycle—If the RETRY occurs on an operand read, the bus cycle is immediately repeated. If the data read is "multiple" e.g. non-aligned, only the problematic part will be repeated. For instance, if the cycle is a non-aligned double word and the second half failed, only the second part will be repeated. The same applies for a RETRY occurring during a burst chain. The repeated cycle will begin where the read operand failed (rather than the first address of the burst) and will finish the original burst.

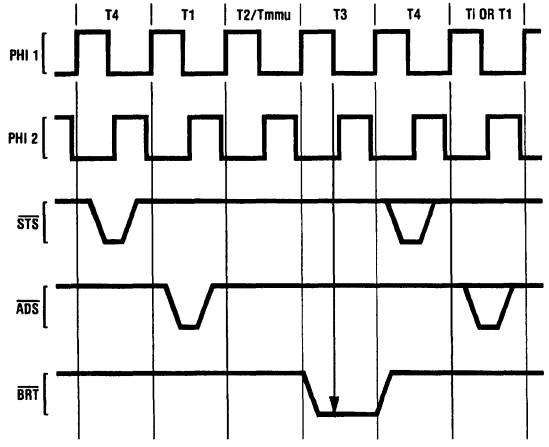
3.0 Functional Description (Continued)

Operand Write Cycle—If the RETRY occurs on a write, the bus cycle is immediately repeated. If the operand write is "multiple" e.g. non-aligned, only the problematic part will be repeated. For instance, if the cycle is a non-aligned double word and the second half failed, only the second part will be repeated.

A Bus Retry is requested by activating the $\overline{BRT}$ line (see *Figure 3-15*). $\overline{BRT}$ is sampled by the CPU during T3 on the falling edge of PHI1. If $\overline{BRT}$ is inactive, the cycle will be terminated in a regular way. In this case $\overline{BRT}$ must also be kept inactive during T4. If $\overline{BRT}$ is active, $\overline{BRT}$ will be sampled again during T4 on the falling edge of PHI1. If $\overline{BRT}$ is inactive, the cycle will be terminated in a regular way. If $\overline{BRT}$ is active, T4 will be followed by an idle state and the cycle will be repeated, i.e. a new T4 for setting the Status Bus and issuing $\overline{STS}$ and then T1 through T4 will be performed.

Although the decision about Retry is taken by the CPU on T4, $\overline{BRT}$ must have an early activation in T3 as described above in order to prevent the internal pipeline to advance. Holding the pipeline allows the repeated cycle to override the original one. If $\overline{BRT}$ is activated only in T3 and not in T4, there might be one cycle penalty in the performance of the execution unit in operand read cycles.

Retry is applicable for regular memory cycles and burst cycles, but not for Slave cycles.



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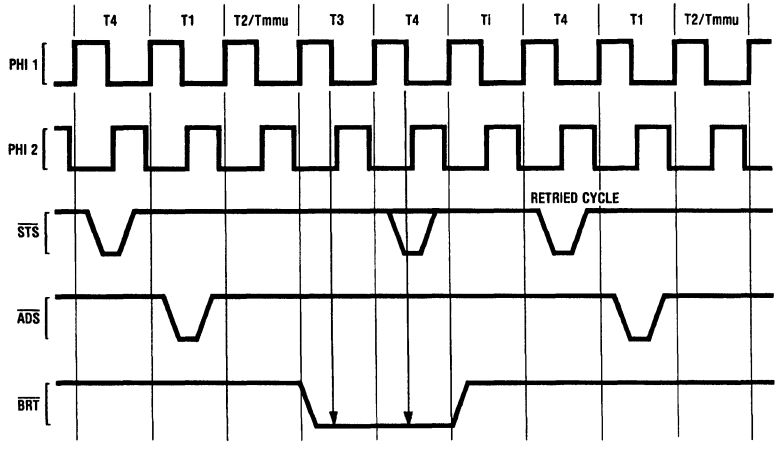
(a) Bus Cycle Not Retried



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(b) Bus Cycle Retried

FIGURE 3-15. Bus Cycle Retry

3.0 Functional Description (Continued)

3.4.8.2 Bus Error

If a Bus Error is incorrectable the CPU may be requested to abort the current process and branch to an appropriate routine to handle the error. The request is performed by activating the $\overline{BER}$ signal.

$\overline{BER}$ is sampled by the CPU during T4 on the falling edge of PHI1. If $\overline{BER}$ is active the bus will go to Tidle after T4 and the CPU will jump to the Bus Error handler (see Sec. 3.8).

The CPU response to Bus Error depends on the cycle type:

Instruction Fetch Cycles—If the bus error occurs on an instruction fetch, additional fetches are inhibited including the one which failed. If, after inhibiting instruction fetches, some operand cycles are still pending within the CPU, they are executed normally, delaying the access to the bus error exception. If and when the internal instruction queue becomes empty, the CPU will enter the BUS ERROR exception. This arrangement enables the CPU to ignore bus errors which belong to fetch ahead cycles if these fetches are not to be used as a result of a jump.

Operand Read Cycles—If the bus error occurs on an operand read, the bus error is immediately accepted, and the CPU enters the BUS ERROR exception.

Operand Write Cycles—If the bus error occurs on an operand write, the exception is immediately accepted.

Note 1: When a bus error occurs, the instruction that caused the error is generally not re-executable.

The process that was being executed should either be aborted or should be restarted from the last checkpoint.

Note 2: Bus error has top priority and is accepted even during the acknowledge sequence of another CPU exception (i.e. Abort, Interrupt, etc.).

It is the responsibility of the user software to detect such an occurence and to take the appropriate corrective actions.

3.4.8.3 Fatal Bus Error

As previously mentioned, the CPU response to a bus error is to interrupt the current activity and enter the error routine.

An exception to this rule occurs when a bus error is signalled to the CPU during the acknowledge of a previous bus error. In this case the second error is interpreted by the CPU as a fatal bus error.

The CPU will respond to this event by halting execution and floating $\overline{ADS}$, $\overline{BE0}$–$\overline{BE3}$, $\overline{DDIN}$, $\overline{STS}$ and AD0–AD31.

The Halt condition is indicated by the setting of ST0–ST3 to zero and by the assertion of $\overline{MC}/\overline{EXS}$ for more than one clock cycle (see Sec. 4.1.3).

The CPU can exit this condition only through a hardware reset.

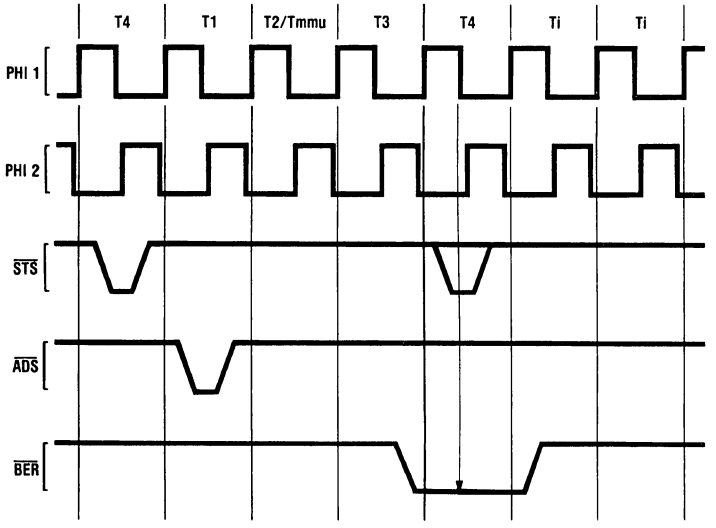

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FIGURE 3-16. Bus Error During Read or Write Cycle

3.0 Functional Description (Continued)

3.4.9 Slave Processor Communication

The $\overline{SPC}$ pin is used as the data strobe for Slave Processor transfers. In this role, it is referred to as Slave Processor Control ($\overline{SPC}$). In a Slave Processor bus cycle, data is transferred on the Data Bus and the status lines (ST0–ST3) are monitored by each Slave Processor in order to determine the type of transfer being performed. $\overline{SPC}$ is bidirectional, but is driven by the CPU during all Slave Processor bus cycles. See Sec. 3.9 for full protocol sequences.

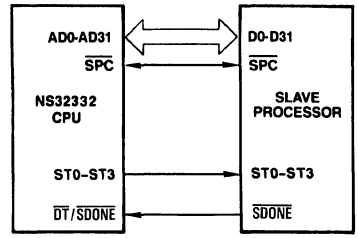

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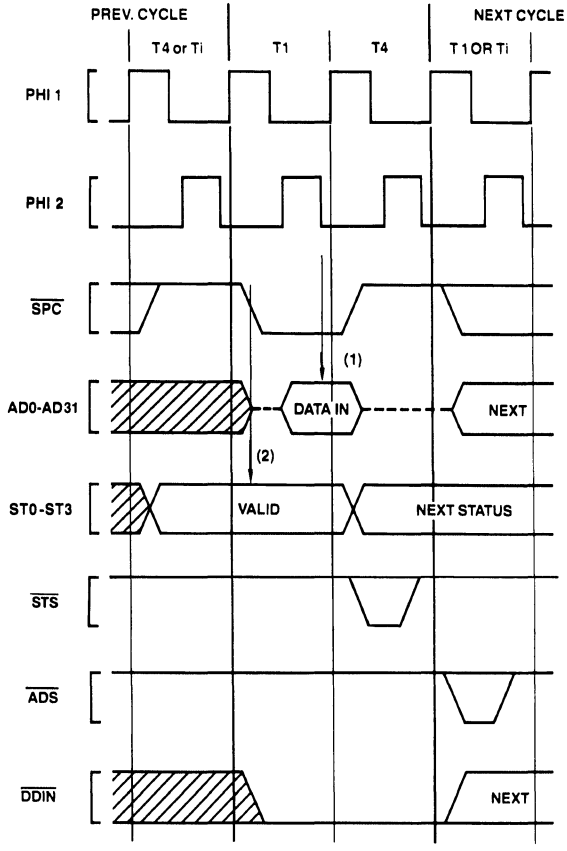
FIGURE 3-17. Slave Processor Connections



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Notes:

(1) CPU samples Data Bus here.

(2) Slave Processor samples CPU Status here.

FIGURE 3-18. CPU Read from Slave Processor

3.0 Functional Description (Continued)

3.4.9.1 Slave Processor Bus Cycles

A Slave Processor bus cycle always takes exactly two clock cycles, labeled T1 and T4 (see *Figures 3-18* and *3-19*). During a Read cycle, $\overline{SPC}$ is active from the beginning of T1 to the beginning of T4, and the data is sampled at the end of T1. The Cycle Status pins lead the cycle by one clock period, and are sampled at the leading edge of $\overline{SPC}$. During a Write cycle, the CPU applies data and activates $\overline{SPC}$ at T1, removing $\overline{SPC}$ at T4. The Slave Processor latches status on the leading edge of $\overline{SPC}$ and latches data on the trailing edge.

The CPU does not pulse the address ($\overline{ADS}$) and status ($\overline{STS}$) strobes during a slave protocol. The direction of a transfer is determined by the sequence ("protocol") established by the instruction under execution; but the CPU indicates the direction on the $\overline{DDIN}$ pin for hardware debugging purposes.

3.4.9.2 Slave Operand Transfer Sequences

A Slave Processor operand is transferred in one or more slave operand cycles. The NS32332 supports two slave protocols which can be selected by the configuration register (CFG).

1. The regular Slave protocol is fully compatible with NS32032, NS32016 and NS32008 slave protocols.

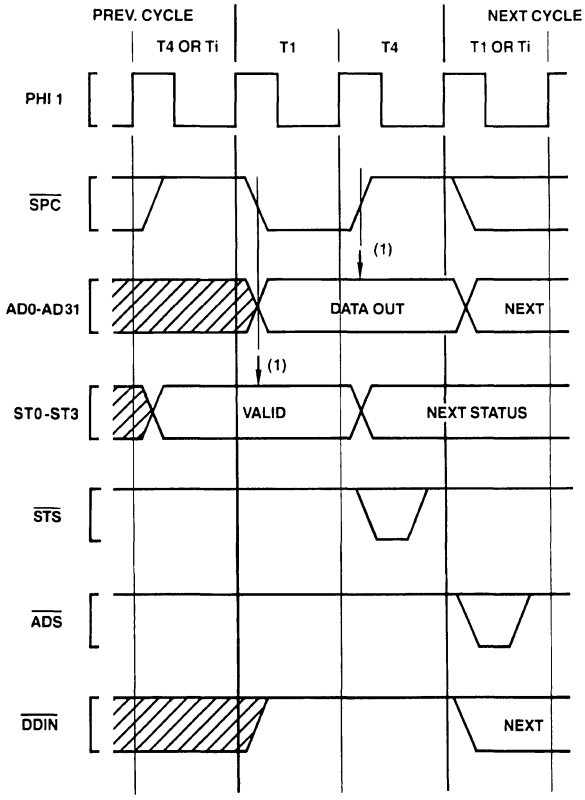
   In this protocol the NS32332 uses only the two least significant bytes of the data bus for slave cycles. This allows the NS32332 CPU to work with the current slaves (like NS32082, NS32081 etc.)

   A byte operand is transferred on the least significant byte of the data bus (AD0–AD15).

   A double word is transferred in a consecutive pair of bus cycles least significant word first. A quadword is transferred in two pairs of slave cycles.

2. The fast slave protocol is unique to the NS32332 CPU. In this protocol the NS32332 uses the full width of the data bus (AD0–AD31) for slave cycles.

   A byte operand is transferred on the least significant byte of the data bus (AD0–AD7), a word operand is transferred on bits AD0–AD15 and a double word operand is transferred on bits AD0–AD31. A quad word is transferred in two pairs of slave cycles with other bus cycles possibly occurring between them.



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Note:

(1) Arrows indicate points at which the Slave Processor samples.

FIGURE 3-19. CPU Write to Slave Processor

3.0 Functional Description (Continued)

3.5 MEMORY MANAGEMENT OPTION

The NS32332 CPU, in conjunction with the Memory Management Unit (MMU), provides full support for address translation, memory protection, and memory allocation techniques up to and including Virtual Memory.

When an MMU is used, the states T2 and TMMU are overlapped. During this time the CPU places AD0–AD31 into the TRI-STATE mode, allowing the MMU to assert the translated address and issue the physical address strobe $\overline{PAV}$. *Figure 3-20* shows the Bus Cycle timing with address translation.

Note 1: If an NS32382 MMU is used, the CPU can be selected to output data during write cycles in state T2, by forcing $\overline{DT}/\overline{SDONE}$ low during reset. This can be done because the NS32382 uses a separate physical address bus.

However, if a write cycle causes an MMU page table lookup, the CPU data will be valid in state T3. After $\overline{FLT}$ is deasserted, regardless of the data timing selected.

$DT/\overline{SDONE}$ must always be forced high during reset if an NS32082 MMU is used since, in this case, no separate physical address bus is provided.

Note 2: If an NS32082 MMU is used, in order for it to operate properly, it must be set to the 32-Bit mode by forcing a $A24/\overline{HBF}$ low during reset. In this mode the bus lines AD16–AD24 are floated after the MMU address has been latched, since they are used by the CPU to transfer data.

3.5.1 The $\overline{FLT}$ (Float) Pin

The $\overline{FLT}$ signal is used by the CPU for address translation support. Activating $\overline{FLT}$ during Tmmu causes the CPU to wait longer than Tmmu for address translation and validation. This feature is used occasionally by the MMU in order to update its Translation Lookaside Buffer (TLB) from page tables in memory, or to update certain status bits within them.

Figure 3-21 shows the effect of $\overline{FLT}$. Upon sampling $\overline{FLT}$ low, late in Tmmu, the CPU enters idle T-States (Tf) during which it:

1) Sets AD0–AD31, and $\overline{DDIN}$ to the TRI-STATE condition ("floating").
2) Suspends further internal processing of the current instruction. This ensures that the current instruction remains abortable with retry. (See $\overline{RST}/\overline{ABT}$ description.)

The above conditions remain in effect until $\overline{FLT}$ again goes high. See Sec. 4.

3.5.2 Aborting Bus Cycles

The $\overline{RST}/\overline{ABT}$ pin, apart from its Reset function (Sec. 3.3), also serves as the means to "abort", or cancel, a bus cycle and the instruction, if any, which initiated it. An Abort request is distinguished from a Reset in that the $\overline{RST}/\overline{ABT}$ pin is held active for only one clock cycle.

If $\overline{RST}/\overline{ABT}$ is pulled low during Tmmu or Tf, this signals that the cycle must be aborted. Since it is the MMU $\overline{PAV}$ signal which triggers a physical cycle, the rest of the system remains unaware that a cycle was started.

The MMU will abort a bus cycle for either of two reasons:

1) The CPU is attempting to access a virtual address which is not currently resident in physical memory. The referenced page must be brought into physical memory from mass storage to make it accessible to the CPU.
2) The CPU is attempting to perform an access which is not allowed by the protection level assigned to that page.

When a bus cycle is aborted by the MMU, the instruction that caused it to occur is also aborted in such a manner that it is guaranteed re-executable later.

Note: To guarantee correct instruction reexecution, Bit M in the CFG Register must be set.

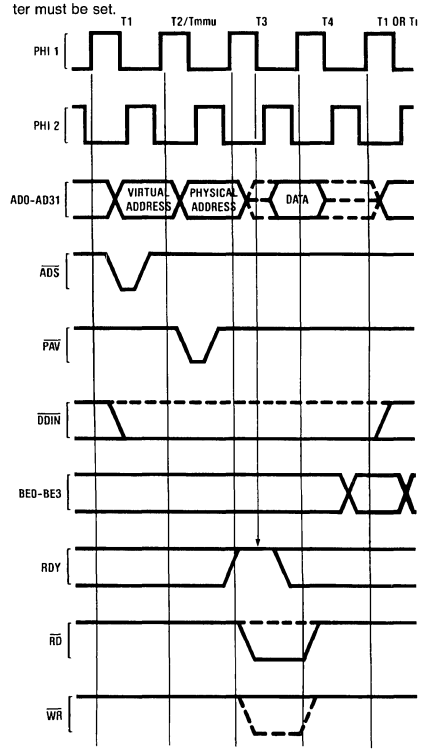

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FIGURE 3-20. Read (Write) Cycle with Address Translation

3.5.2.1 Instruction Abort

Upon aborting an instruction, the CPU immediately interrupts the instruction and performs an abort acknowledge using the ABT vector in the Interrupt Table (see Sec. 3.8). The Return Address pushed on the Interrupt Stack is the address of the aborted instruction, so that a Return from Trap (RETT) instruction will automatically retry it.

The one exception to this sequence occurs if the aborted bus cycle was an instruction prefetch. If so, it is not yet certain that the aborted prefetched code is to be executed. Instead of causing an interrupt, the CPU only aborts the bus cycle, and stops prefetching. If the information in the Instruction Queue runs out, meaning that the instruction will actually be executed, the Abort will occur, in effect aborting the instruction that was being fetched.

3.5.2.2 Hardware Considerations

In order to guarantee instruction retry, certain rules must be followed in applying an Abort to the CPU. These rules are followed by the Memory Management Unit.

1) If $\overline{FLT}$ has not been applied to the CPU, the Abort pulse must occur during Tmmu.

3.0 Functional Description (Continued)

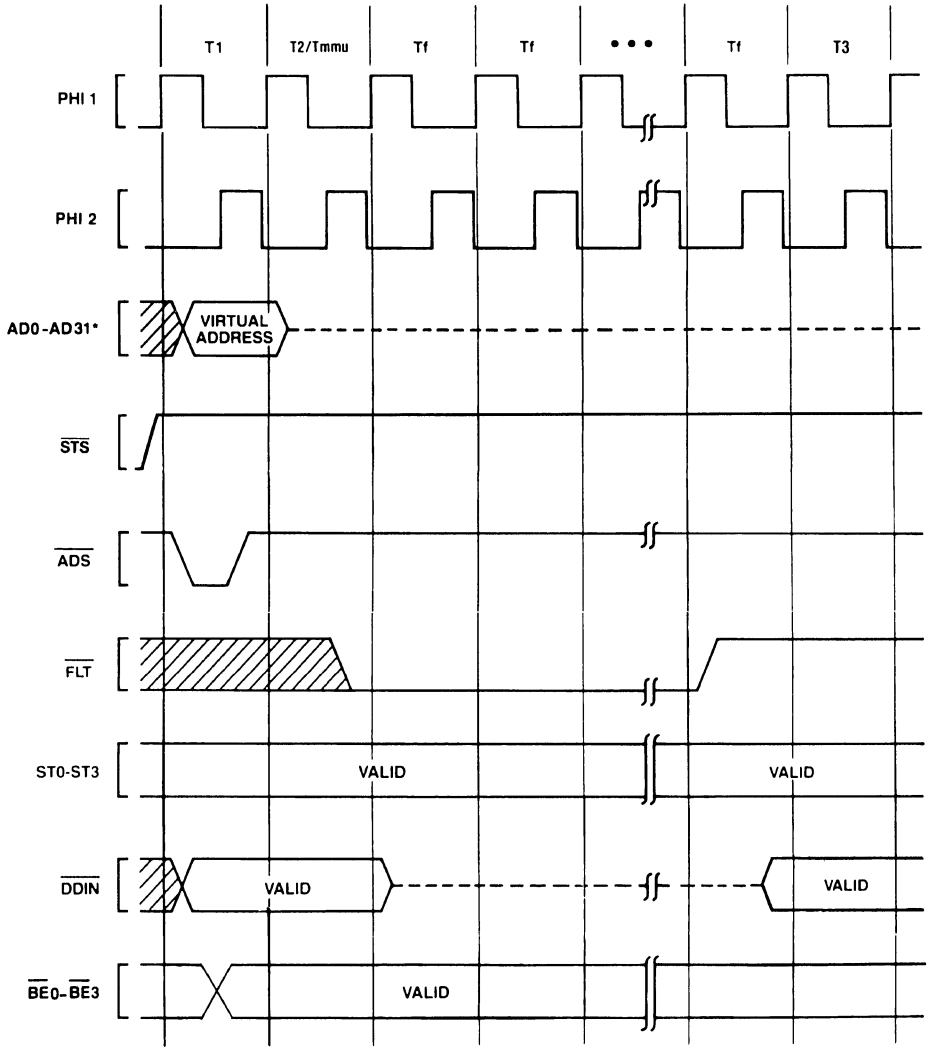
2) If $\overline{FLT}$ has been applied to the CPU, the Abort pulse must be applied before the T-State in which $\overline{FLT}$ goes inactive. The CPU will not actually respond to the Abort command until $\overline{FLT}$ is removed.

3) The Write half of a Read-Modify-Write operand access may not be aborted. The CPU guarantees that this will never be necessary for Memory Management functions by applying a special RMW status (Status Code 1011) during the Read half of the access. When the CPU presents RMW status, that cycle must be aborted if it would be illegal to write to any of the accessed addresses.

If $\overline{RST}/\overline{ABT}$ is pulsed at any time other than as indicated above, it will abort either the instruction currently under execution or the next instruction and will act as a very high-priority interrupt. However, the program that was running at the time is not guaranteed recoverable.

3.6 BUS ACCESS CONTROL

The NS32332 CPU has the capability of relinquishing its access to the bus upon request from a DMA device or another CPU. This capability is implemented on the $\overline{HOLD}$ (Hold Request) and $\overline{HLDA}$ (Hold Acknowledge) pins. By asserting HOLD low, an external device requests access to the bus. On receipt of $\overline{HLDA}$ from the CPU, the device may perform bus cycles, as the CPU at this point has set the



*See MMU data sheet for details on physical address timing and MMU initiated Bus cycles.

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FIGURE 3-21. $\overline{FLT}$ Timing

3.0 Functional Description (Continued)

AD0–AD31, $\overline{ADS}$, $\overline{STS}$, $\overline{DDIN}$ and $\overline{BE0}$–$\overline{BE3}$ pins to the TRI-STATE condition. To return control of the bus to the CPU, the device sets $\overline{HOLD}$ inactive, and the CPU acknowledges return of the bus by setting $\overline{HLDA}$ inactive.

How quickly the CPU releases the bus depends on whether it is idle on the bus at the time the $\overline{HOLD}$ request is made, as the CPU must always complete the current bus cycle. *Figure 3-22* shows the timing sequence when the CPU is idle. In this case, the CPU grants the bus during the immediately following clock cycle. *Figure 3-23* shows the sequence if the CPU is using the bus at the time that the $\overline{HOLD}$ request is made. If the request is made during or before the clock cycle shown (two clock cycles before T4), the CPU will release the bus during the clock cycle following T4. If the request occurs closer to T4, the CPU may already have decided to initiate another bus cycle. In that case it will not grant the bus until after the next T4 state. Note that this situation will also occur if the CPU is idle on the bus but has initiated a bus cycle internally.

In a Memory-Managed system, the $\overline{HLDA}$ signal is connected in a daisy-chain through the MMU, so that the MMU can release the bus if it is using it.

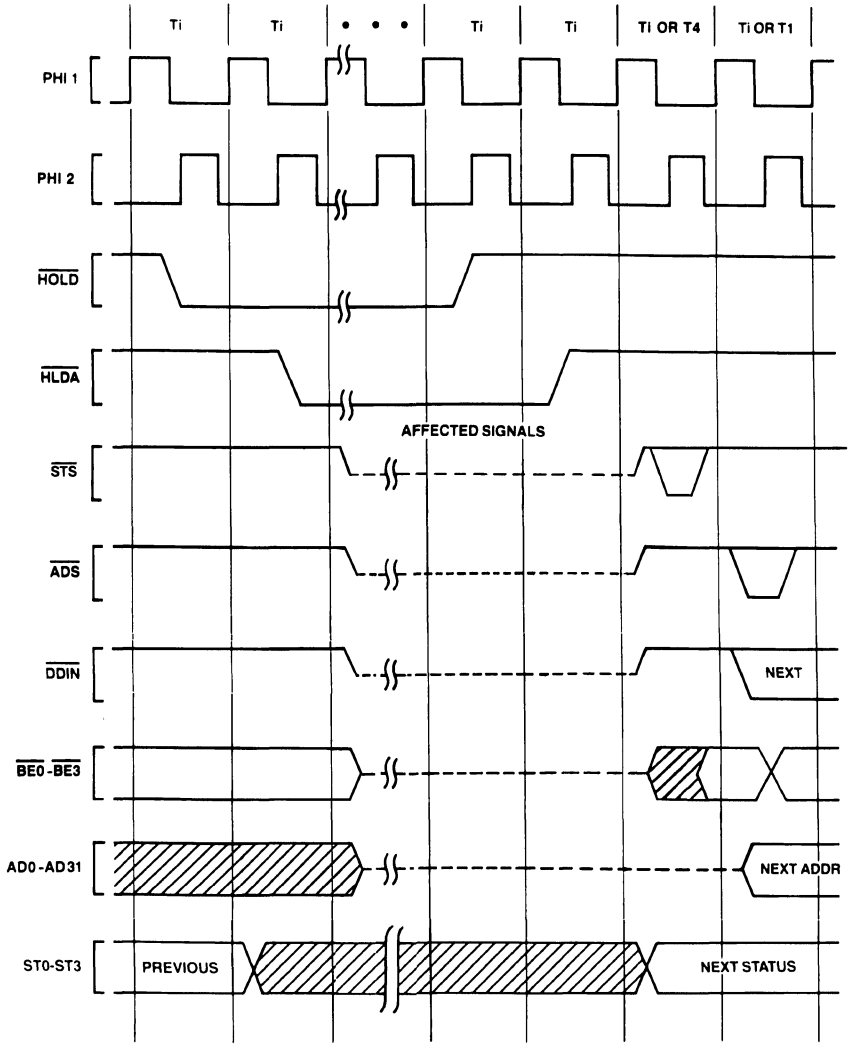

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FIGURE 3-22. $\overline{HOLD}$ Timing, Bus Initially Idle

3.0 Functional Description (Continued)

3.7 INSTRUCTION STATUS

In addition to the four bits of Bus Cycle status (ST0–ST3), the NS32332 CPU also presents Instruction Status information on four separate pins. These pins differ from ST0–ST3 in that they are synchronous to the CPU's internal instruction execution section rather than to its bus interface section.

$\overline{PFS}$ (Program Flow Status) is pulsed low as each instruction begins execution. It is intended for debugging purposes.

U/$\overline{S}$ originates from the U bit of the Processor Status Register, and indicates whether the CPU is currently running in User or Supervisor mode. It is sampled by the MMU for mapping, protection, and debugging purposes. U/$\overline{S}$ line is updated every T4.

$\overline{ILO}$ (Interlocked Operation) is activated during an SBITI (Set Bit, Interlocked) or CBITI (Clear Bit, Interlocked) instruction. It is made available to external bus arbitration circuitry in order to allow these instructions to implement the semaphore primitive operations for multi-processor communication and resource sharing.

While $\overline{ILO}$ is active, the CPU inhibits instruction fetches. In order to prevent MMU cycles during $\overline{ILO}$, the CPU executes a dummy Read cycle with status code 1011 (RMW) prior to activating $\overline{ILO}$. Thereafter, $\overline{ILO}$ is activated and the Read is performed again but with status code 1010 (operand transfer). Refer to *Figure 3-24*.

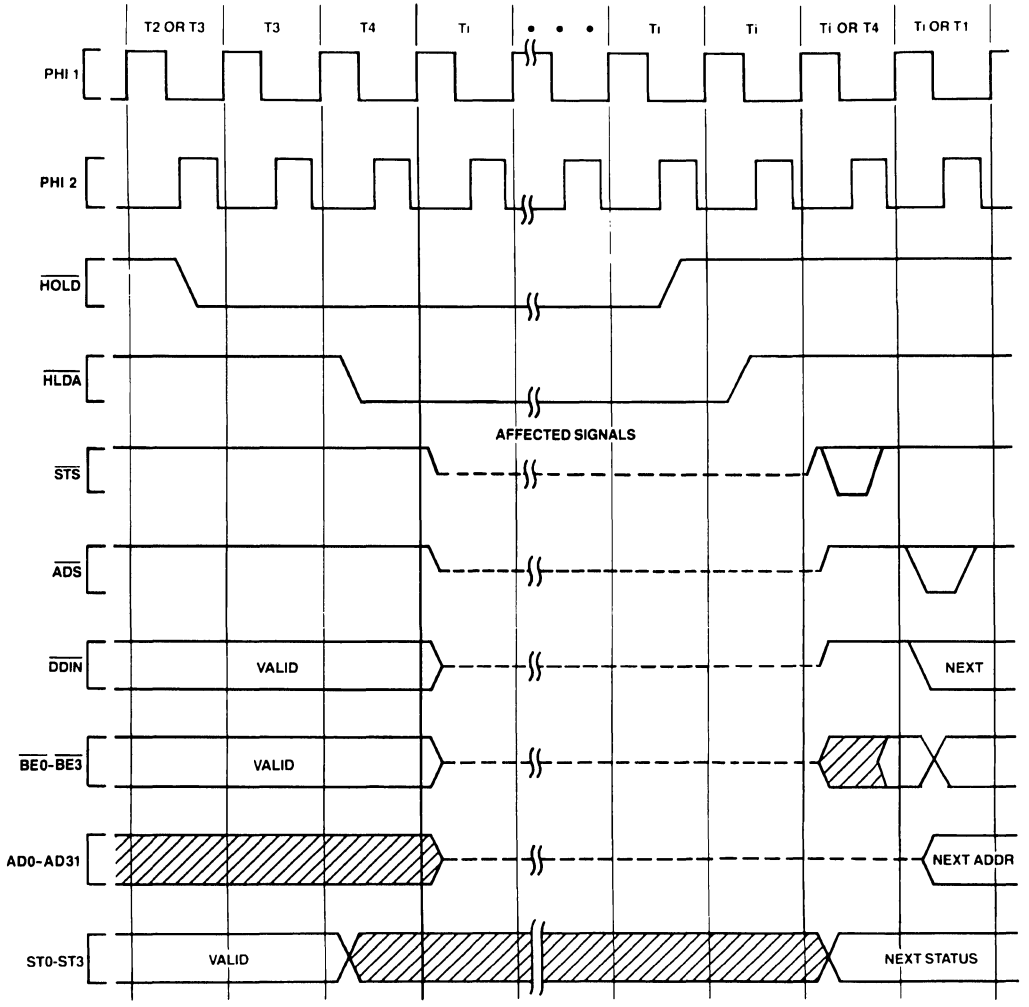

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FIGURE 3-23. $\overline{HOLD}$ Timing, Bus Initially Not Idle

3.0 Functional Description (Continued)

$\overline{MC}/\overline{EXS}$ (Multiple Cycle/Exception Status) is activated during the access of the first part of an operand that crosses a double-word address boundary. The activation of this signal is independent of the selected bus width. Its timing is shown in *Figure 3-25.* The MMU or other external circuitry can use it as an early indication of a CPU access to an operand that crosses a page boundary.

$\overline{MC}/\overline{EXS}$ is also activated during the first non-sequential instruction fetch (status code 1001) following an abort, and when the CPU enters the idle state (Status Code 0000) following a fatal bus error.

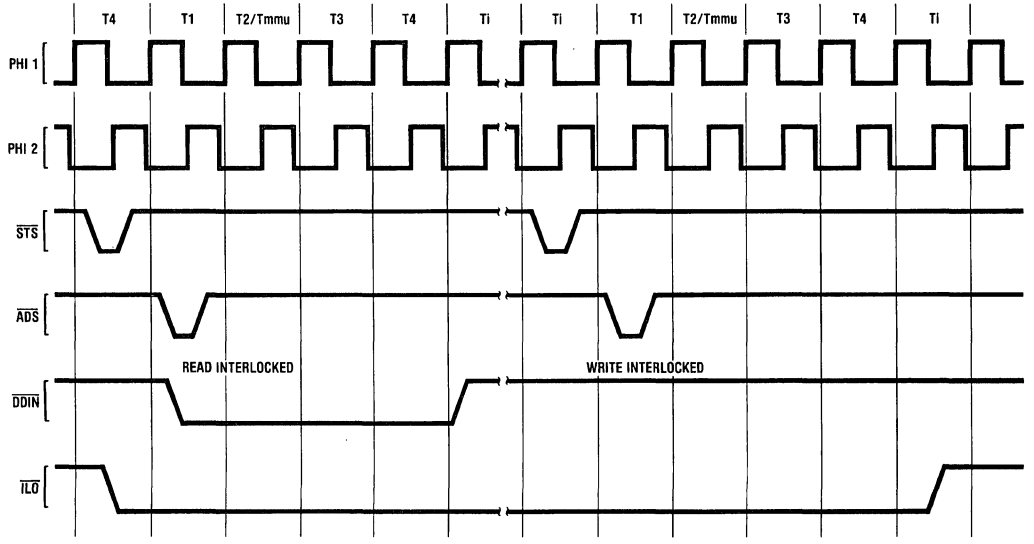

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FIGURE 3-24. $\overline{ILO}$ Timing

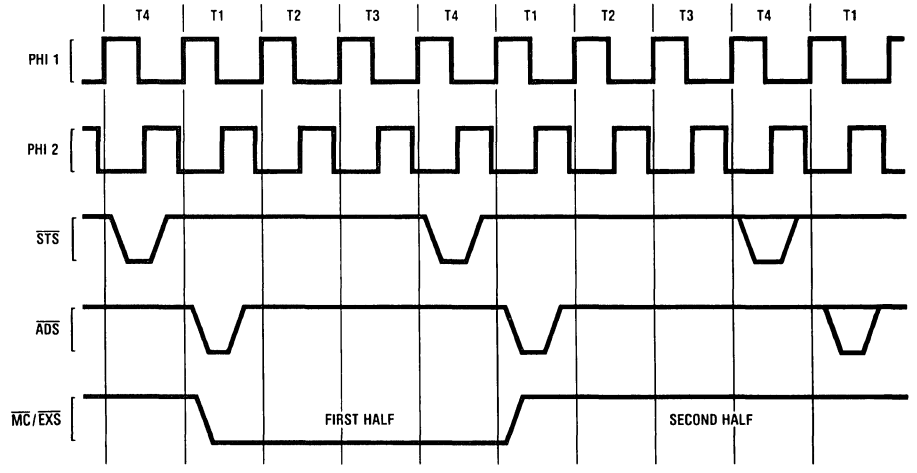

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FIGURE 3-25. Non-aligned Write Cycle—$\overline{MC}/\overline{EXS}$ Timing

3.0 Functional Description (Continued)

3.8 NS32332 INTERRUPT STRUCTURE

$\overline{INT}$, on which maskable interrupts may be requested,

$\overline{NMI}$, on which non-maskable interrupts may be requested, and

$\overline{RST}/\overline{ABT}$, which may be used to abort a bus cycle and any associated instruction. See Sec. 3.5.2.

In addition there is a set of internally-generated "traps" which cause interrupt service to be performed as a result either of exceptional conditions (e.g., attempted division by zero) or of specific instructions whose purpose is to cause a trap to occur (e.g., the Supervisor Call instruction).

3.8.1 General Interrupt/Trap Sequence

Upon receipt of an interrupt or trap request, the CPU goes through three major steps:

1) Adjustment of Registers.

Depending on the source of the interrupt or trap, the CPU may restore and/or adjust the contents of the Program Counter (PC), the Processor Status Register (PSR) and the currently-selected Stack Pointer (SP). A copy of the PSR is made, and the PSR is then set to reflect Supervisor Mode and selection of the Interrupt Stack.

2) Vector Acquisition.

A Vector is either obtained from the Data Bus or is supplied by default.

3) Service Call.

The Vector is used as an index into the Interrupt Dispatch Table, whose base address is taken from the CPU Interrupt Base (INTBASE) Register. See *Figure 3-26*. A 32-bit External Procedure Descriptor is read from the table entry, and an External Procedure Call is performed using it. The MOD Register (16 bits) and Program Counter (32 bits) are pushed on the Interrupt Stack.

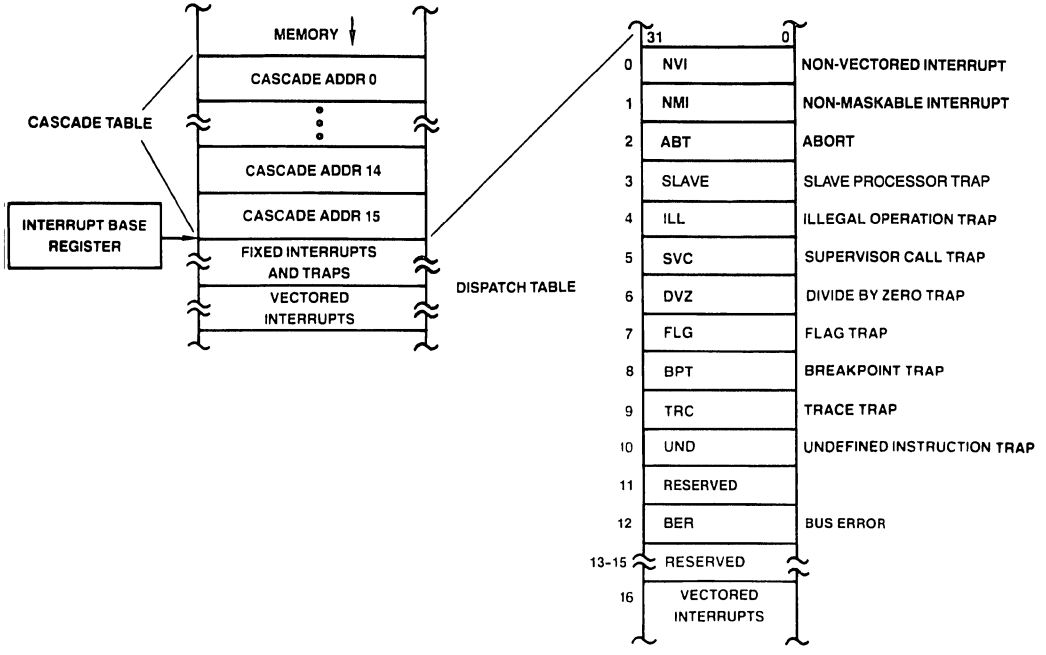

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FIGURE 3-26. Interrupt Dispatch Table

3.0 Functional Description (Continued)

This process is illustrated in *Figure 3-27*, from the viewpoint of the programmer.

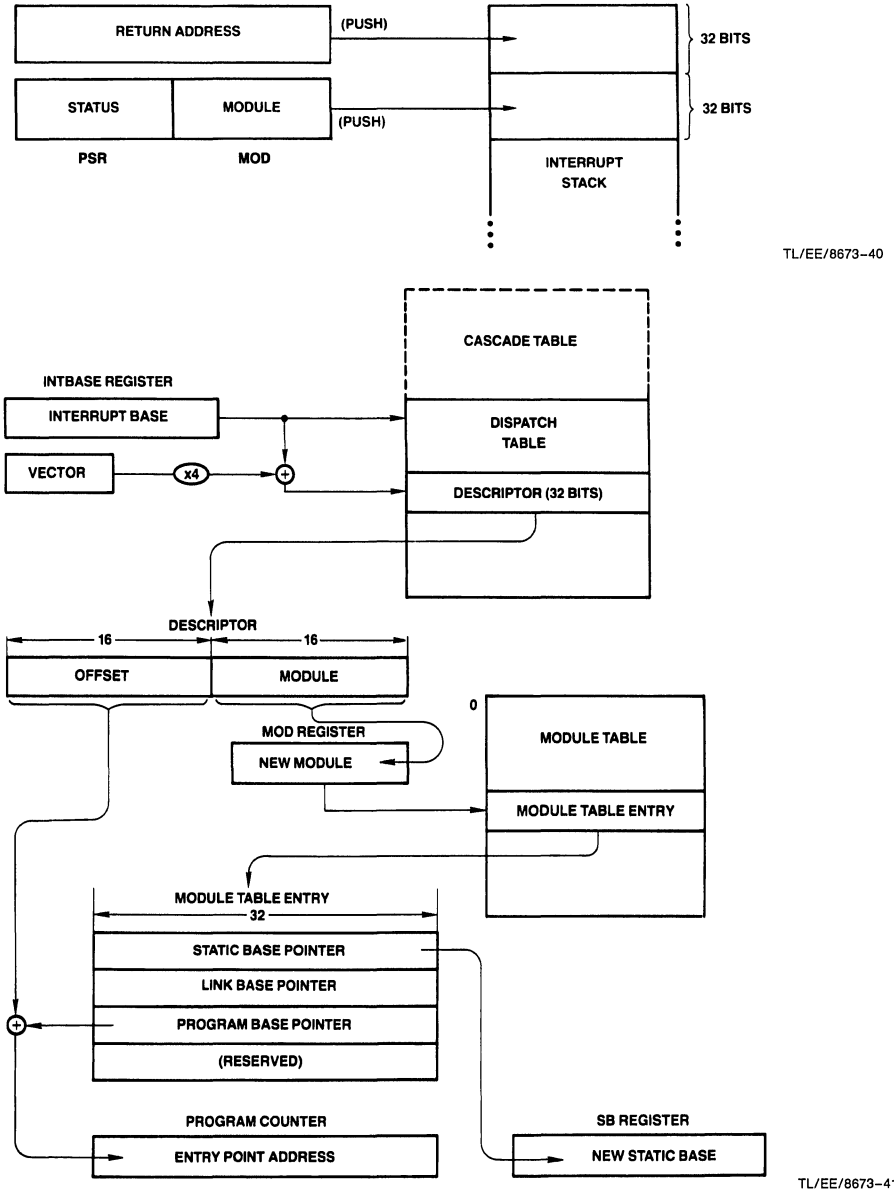

FIGURE 3-27. Interrupt/Trap Service Routine Calling Sequence

3.0 Functional Description (Continued)

3.8.2 Interrupt/Trap Return

To return control to an interrupted program, one of two instructions is used. The RETT (Return from Trap) instruction *(Figure 3-28)* restores the PSR, MOD, PC and SB registers to their previous contents and, since traps are often used deliberately as a call mechanism for Supervisor Mode procedures, it also discards a specified number of bytes from the original stack as surplus parameter space. RETT is used to return from any trap or interrupt except the Maskable Interrupt. For this, the RETI (Return from Interrupt) instruction is used, which also informs any external Interrupt Control Units that interrupt service has completed. Since interrupts are generally asynchronous external events, RETI does not pop parameters. See *Figure 3-29*.

3.8.3 Maskable Interrupts (The $\overline{\text{INT}}$ Pin)

The $\overline{\text{INT}}$ pin is a level-sensitive input. A continuous low level is allowed for generating multiple interrupt requests. The input is maskable, and is therefore enabled to generate interrupt requests only while the Processor Status Register I bit is set. The I bit is automatically cleared during service of an $\overline{\text{INT}}$, $\overline{\text{NMI}}$ or Abort request, and is restored to its original setting upon return from the interrupt service routine via the RETT or RETI instruction.

The $\overline{\text{INT}}$ pin may be configured via the SETCFG instruction as either Non-Vectored (CFG Register bit I = 0) or Vectored (bit I = 1).

3.8.3.1 Non-Vectored Mode

In the Non-Vectored mode, an interrupt request on the $\overline{\text{INT}}$ pin will cause an Interrupt Acknowledge bus cycle, but the CPU will ignore any value read from the bus and use instead a default vector of zero. This mode is useful for small systems in which hardware interrupt prioritization is unnecessary.

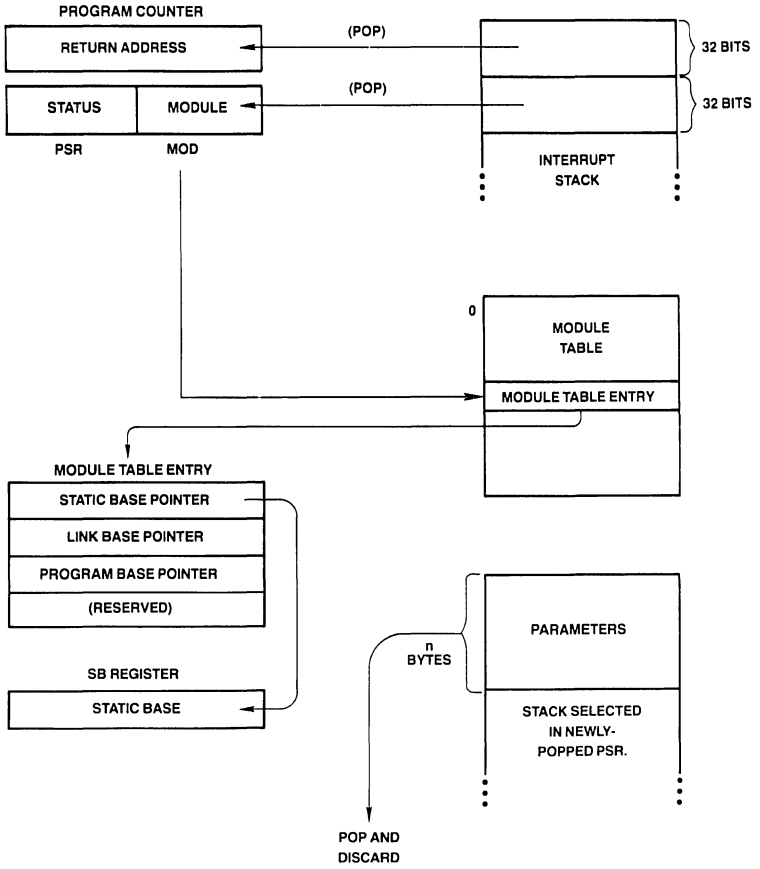

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FIGURE 3-28. Return from Trap (RETT n) Instruction Flow

3.0 Functional Description (Continued)

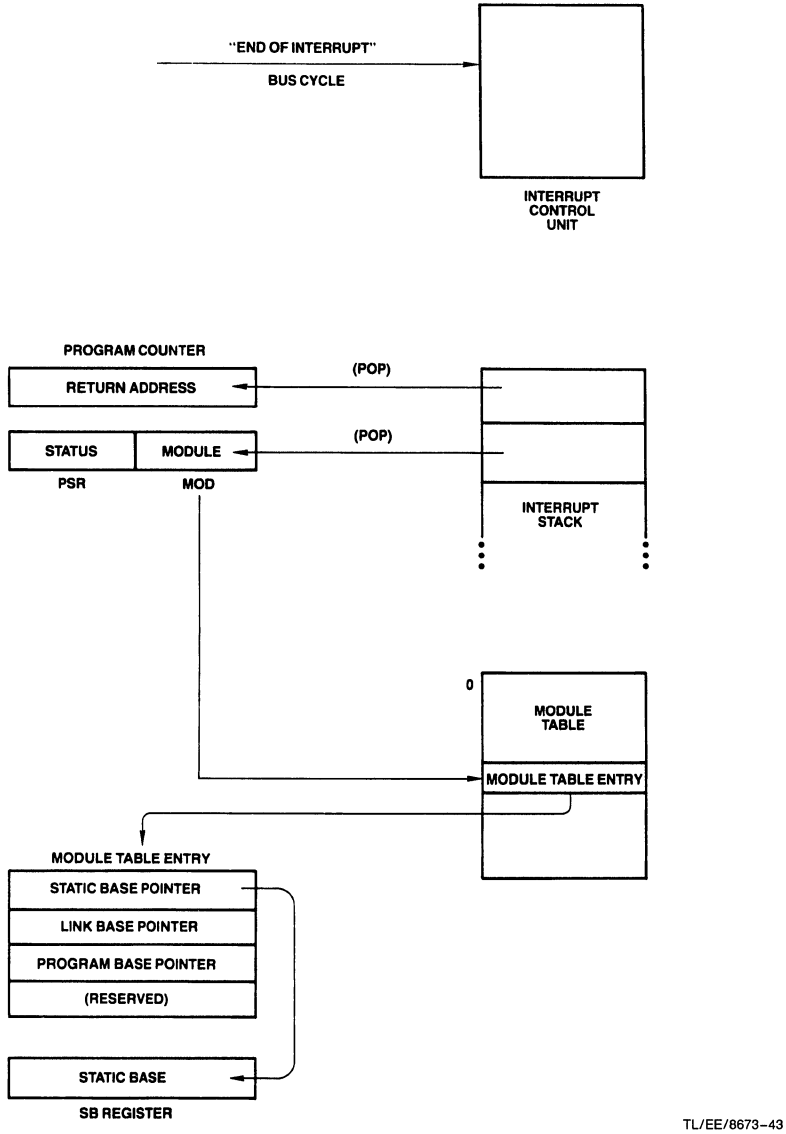

FIGURE 3-29. Return from Interrupt (RETI) Instruction Flow

3.0 Functional Description (Continued)

3.8.3.2 Vectored Mode: Non-Cascaded Case

In the Vectored mode, the CPU uses an Interrupt Control Unit (ICU) to prioritize many interrupt requests. Upon receipt of an interrupt request on the $\overline{INT}$ pin, the CPU performs an "Interrupt Acknowledge, Master" bus cycle (Sec. 3.4.3) reading a vector value from the low-order byte of the Data Bus. This vector is then used as an index into the Dispatch Table in order to find the External Procedure Descriptor for the proper interrupt service procedure. The service procedure eventually returns via the Return from Interrupt (RETI) instruction, which performs an End of Interrupt bus cycle, informing the ICU that it may re-prioritize any interrupt requests still pending. The ICU provides the vector number again, which the CPU uses to determine whether it needs also to inform a Cascaded ICU (see below).

In a system with only one ICU (16 levels of interrupt), the vectors provided must be in the range of 0 through 127; that is, they must be positive numbers in eight bits. By providing a negative vector number, an ICU flags the interrupt source as being a Cascaded ICU (see below).

3.8.3.3 Vectored Mode: Cascaded Case

In order to allow more levels of interrupt, provision is made in the CPU to transparently support cascading. Note that the Interrupt output from a Cascaded ICU goes to an Interrupt Request input of the Master ICU, which is the only ICU which drives the CPU $\overline{INT}$ pin. Refer to the ICU data sheet for details.

In a system which uses cascading, two tasks must be performed upon initialization:

1) For each Cascaded ICU in the system, the Master ICU must be informed of the line number on which it receives the cascaded requests.
2) A Cascade Table must be established in memory. The Cascade Table is located in a NEGATIVE direction from the location indicated by the CPU Interrupt Base (INTBASE) Register. Its entries are 32-bit addresses, pointing to the Vector Registers of each of up to 16 Cascaded ICUs.

Figure 3-26 illustrates the position of the Cascade Table. To find the Cascade Table entry for a Cascaded ICU, take its Master ICU line number (0 to 15) and subtract 16 from it, giving an index in the range -16 to -1. Multiply this value by 4, and add the resulting negative number to the contents of the INTBASE Register. The 32-bit entry at this address must be set to the address of the Hardware Vector Register of the Cascaded ICU. This is referred to as the "Cascade Address."

Upon receipt of an interrupt request from a Cascaded ICU, the Master ICU interrupts the CPU and provides the negative Cascade Table index instead of a (positive) vector number. The CPU, seeing the negative value, uses it as an index into the Cascade Table and reads the Cascade Address from the referenced entry. Applying this address, the CPU performs an "Interrupt Acknowledge, Cascaded" bus cycle (Sec. 3.4.3), reading the final vector value. This vector is interpreted by the CPU as an unsigned byte, and can therefore be in the range of 0 through 255.

In returning from a Cascaded interrupt, the service procedure executes the Return from Interrupt (RETI) instruction, as it would for any Maskable Interrupt. The CPU performs an "End of Interrupt, Master" bus cycle (Sec. 3.4.3), whereupon the Master ICU again provides the negative Cascade Table index. The CPU, seeing a negative value, uses it to find the corresponding Cascade Address from the Cascade Table. Applying this address, it performs an "End of Interrupt, Cascaded" bus cycle (Sec. 3.4.3), informing the Cascaded ICU of the completion of the service routine. The byte read from the Cascaded ICU is discarded.

Note: If an interrupt must be masked off, the CPU can do so by setting the corresponding bit in the interrupt mask register of the interrupt controller.

However, if an interrupt is set pending during the CPU instruction that masks off that interrupt, the CPU may still perform an interrupt acknowledge cycle following that instruction since it might have sampled the $\overline{INT}$ line before the ICU deasserted it. This could cause the ICU to provide an invalid vector. To avoid this problem the above operation should be performed with the CPU interrupt disabled.

3.8.4 Non-Maskable Interrupt (The $\overline{NMI}$ Pin)

The Non-Maskable Interrupt is triggered whenever a falling edge is detected on the $\overline{NMI}$ pin. The CPU performs an "Interrupt Acknowledge, Master" bus cycle (Sec. 3.4.3) when processing of this interrupt actually begins. The Interrupt Acknowledge cycle differs from that provided for Maskable Interrupts in that the address presented is $FFFFFF00_{16}$. The vector value used for the Non-Maskable Interrupt is taken as 1, regardless of the value read from the bus.

The service procedure returns from the Non-Maskable Interrupt using the Return from Trap (RETT) instruction. No special bus cycles occur on return.

For the full sequence of events in processing the Non-Maskable Interrupt, see Sec. 3.8.7.1.

3.8.5 Traps

A trap is an internally-generated interrupt request caused as a direct and immediate result of the execution of an instruction. The Return Address pushed by any trap except Trap (TRC) is the address of the first byte of the instruction during which the trap occurred. Traps do not disable interrupts, as they are not associated with external events. Traps recognized by the NS32332 CPU are:

Trap (SLAVE): An exceptional condition was detected by the Floating Point Unit or another Slave Processor during the execution of a Slave Instruction. This trap is requested via the Status Word returned as part of the Slave Processor Protocol (Sec. 3.9.1).

Trap (ILL): Illegal operation. A privileged operation was attempted while the CPU was in User Mode (PSR bit U = 1).

Trap (SVC): The Supervisor Call (SVC) instruction was executed.

Trap (DVZ): An attempt was made to divide an integer by zero. (The Slave trap is used for Floating Point division by zero.)

Trap (FLG): The FLAG instruction detected a "1" in the CPU PSR F bit.

Trap (BPT): The Breakpoint (BPT) instruction was executed.

Trap (TRC): The instruction just completed is being traced. See below.

Trap (UND): An undefined opcode was encountered by the CPU.

3.0 Functional Description (Continued)

A special case is the Trace Trap (TRC), which is enabled by setting the T bit in the Processor Status Register (PSR). At the beginning of each instruction, the T bit is copied into the PSR P (Trace "Pending") bit. If the P bit is set at the end of an instruction, then the Trace Trap is activated. If any other trap or interrupt request is made during a traced instruction, its entire service procedure is allowed to complete before the Trace Trap occurs. Each interrupt and trap sequence handles the P bit for proper tracing, guaranteeing one and only one Trace Trap per instruction, and guaranteeing that the Return Address pushed during a Trace Trap is always the address of the next instruction to be traced.

Note: A slight difference exists between the NS32332 and previous Series 32000 CPUs when tracing is enabled.

The NS32332 always clears the P bit in the PSR before pushing the PSR on the stack. Previous CPUs do not clear it when a trap (ILL) occurs.

The result is that an instruction that causes a trap (ILL) exception is traced by previous Series 32000 CPUs, but is never traced by the NS32332.

3.8.6 Prioritization

The NS32332 CPU internally prioritizes simultaneous interrupt and trap requests as follows:

1) Traps other than Trace (Highest priority)
2) Abort
3) Bus Error
4) Non-Maskable Interrupt
5) Maskable Interrupts
6) Trace Trap (Lowest priority)

3.8.7 Interrupt/Trap Sequences: Detailed Flow

For purposes of the following detailed discussion of interrupt and trap service sequences, a single sequence called "Service" is defined in *Figure 3-30*. Upon detecting any interrupt request or trap condition, the CPU first performs a sequence dependent upon the type of interrupt or trap. This sequence will include pushing the Processor Status Register and establishing a Vector and a Return Address. The CPU then performs the Service sequence.

For the sequence followed in processing either Maskable or Non-Maskable interrupts (on the $\overline{INT}$ or $\overline{NMI}$ pins, respectively), see Sec. 3.8.7.1 For Abort Interrupts, see Sec. 3.8.7.4. For the Trace Trap, see Sec. 3.8.7.3, and for all other traps see Sec. 3.8.7.2.

3.8.7.1 Maskable/Non-Maskable Interrupt Sequence

This sequence is performed by the CPU when the $\overline{NMI}$ pin receives a falling edge, or the $\overline{INT}$ pin becomes active with the PSR I bit set. The interrupt sequence begins either at the next instruction boundary or, in the case of the String instructions, at the next interruptible point during its execution.

1. If a String instruction was interrupted and not yet completed:
   a. Clear the Processor Status Register P bit.
   b. Set "Return Address" to the address of the first byte of the interrupted instruction.

   Otherwise, set "Return Address" to the address of the next instruction.
2. Copy the Processor Status Register (PSR) into a temporary register, then clear PSR bits S, U, T, P and I.
3. If the interrupt is Non-Maskable:
   a. Read a byte from address $FFFFFF00_{16}$, applying Status Code 0100 (Interrupt Acknowledge, Master, Sec. 3.4.3). Discard the byte read.
   b. Set "Vector" to 1.
   c. Go to Step 8.
4. If the interrupt is Non-Vectored:
   a. Read a byte from address $FFFFFE00_{16}$, applying Status Code 0100 (Interrupt Acknowledge, Master: Sec. 3.4.3). Discard the byte read.
   b. Set "Vector" to 0.
   c. Go to Step 8.
5. Here the interrupt is Vectored. Read "Byte" from address $FFFFFE00_{16}$, applying Status Code 0100 (Interrupt Acknowledge, Master: Sec. 3.4.3).
6. If "Byte" ≥ 0, then set "Vector" to "Byte" and go to Step 8.
7. If "Byte" is in the range -16 through -1, then the interrupt source is Cascaded. (More negative values are reserved for future use.) Perform the following:
   a. Read the 32-bit Cascade Address from memory. The address is calculated as INTBASE $+4*$ Byte.
   b. Read "Vector," applying the Cascade Address just read and Status Code 0101 (Interrupt Acknowledge, Cascaded: Sec. 3.4.3).
8. Perform Service (Vector, Return Address), *Figure 3-30*.

Service (Vector, Return Address):

1) Read the 32-bit External Procedure Descriptor from the Interrupt Dispatch Table: address is Vector* 4 + INTBASE Register contents.
2) Move the Module field of the Descriptor into the MOD Register.
3) Read the Program Base pointer from memory address MOD + 8, and add to it the Offset field from the Descriptor, placing the result in the Program Counter.
4) Read the new Static Base pointer from the memory address contained in MOD, placing it into the SB Register.
5) Flush queue: Non-sequentially fetch first instruction of Interrupt routine.
6) Push the PSR copy onto the Interrupt Stack as a 16-bit value.
7) Push MOD Register into the Interrupt Stack as a 16-bit value.
8) Push the Return Address onto the Interrupt Stack as a 32-bit quantity.

FIGURE 3-30. Service Sequence

Invoked during all interrupt/trap sequences.

3.8.7.2 Trap Sequence: Traps Other Than Trace

1) Restore the currently selected Stack Pointer and the Processor Status Register to their original values at the start of the trapped instruction.
2) Set "Vector" to the value corresponding to the trap type.

   SLAVE: Vector = 3.
   ILL: Vector = 4.
   SVC: Vector = 5.
   DVZ: Vector = 6.
   FLG: Vector = 7.
   BPT: Vector = 8.
   UND: Vector = 10.
3) Copy the Processor Status Register (PSR) into a temporary register, then clear PSR bits S, U, P and T.

3.0 Functional Description (Continued)

4) Set "Return Address" to the address of the first byte of the trapped instruction.

5) Perform Service (Vector, Return Address), *Figure 3-30.*

3.8.7.3 Trace Trap Sequence

1) In the Processor Status Register (PSR), clear the P bit.

2) Copy the PSR into a temporary register, then clear PSR bits S, U and T.

3) Set "Vector" to 9.

4) Set "Return Address" to the address of the next instruction.

5) Perform Service (Vector, Return Address), *Figure 3-30.*

3.8.7.4 Abort Sequence

1) Restore the currently selected Stack Pointer to its original contents at the beginning of the aborted instruction.

2) Clear the PSR P bit.

3) Copy the PSR into a temporary register, then clear PSR bits S, U, T and I.

4) Set "Vector" to 2.

5) Set "Return Address" to the address of the first byte of the aborted instruction.

6) Perform Service (Vector, Return Address), *Figure 3-30.*

3.8.7.5 Bus Error Sequence

1) The same as Abort sequence above, but set vector to 12.

3.9 SLAVE PROCESSOR INSTRUCTIONS

The NS32332 CPU recognizes three groups of instructions being executable by external Slave Processor:

Floating Point Instruction Set

Memory Management Instruction Set

Custom Instruction Set

Each Slave Instruction Set is validated by a bit in the Configuration Register (Sec. 2.1.3). Any Slave Instruction which does not have its corresponding Configuration Register bit set will trap as undefined, without any Slave Processor communication attempted by the CPU. This allows software simulation of a non-existent Slave Processor.

In addition, each slave instruction will be performed either through the regular (32032 compatible) slave protocol or through a fast slave protocol according to the relevent bit in the configuration register (Sec. 2.1.3).

A combination of one slave communicating with an old protocol and another with a new protocol is allowed, e.g. 16-bit FPU (32081) and 32-bit MMU (32382) or vice versa.

3.9.1 16-Bit Slave Processor Protocol (32032 Compatible)

Slave Processor instructions have a three-byte Basic Instruction field, consisting of an ID Byte followed by an Operation Word. The ID Byte has three functions:

1) It identifies the instruction as being a Slave Processor instruction.

2) It specifies which Slave Processor will execute it.

3) It determines the format of the following Operation Word of the instruction.

Upon receiving a Slave Processor instruction, the CPU initiates the sequence outlined in *Figure 3-31.* While applying Status Code 1111 (Broadcast ID, Sec. 3.4.3), the CPU transfers the ID Byte on bits AD0–AD7 and a non-used byte xxxxxxx1 (x = don't care) on bits AD24–AD31. All Slave Processors input this byte and decode it. The Slave Processor selected by the ID Byte is activated, and from this point the CPU is communicating only with it. If any other slave protocol was in progress (e.g., an aborted Slave instruction), this transfer cancels it.

The CPU next sends the Operation Word while applying Status Code 1101 (Transfer Slave Operand, Sec. 3.4.3). Upon receiving it, the Slave Processor decodes it, and at this point both the CPU and the Slave Processor are aware of the number of operands to be transferred and their sizes. The operation Word is swapped on the Data Bus, that is, bits 0–7 appear on pins AD8–AD15 and bits 8–15 appear on pins AD0–AD7.

Using the Address Mode fields within the Operation Word, the CPU starts fetching operand and issuing them to the Slave Processor. To do so, it references any Addressing Mode extensions which may be appended to the Slave Processor instruction. Since the CPU is solely responsible for memory accesses, these extensions are not sent to the Slave processor. The Status Code applied is 1101 (Transfer Slave Processor Operand, Sec. 3.4.3).

After the CPU has issued the last operand, the Slave Processor starts the actual execution of the instruction. Upon completion, it will signal the CPU by pulsing $\overline{SPC}$ low. To allow for this $\overline{SPC}$ is normally held high only by an internal pull-up device of approximately 5 kΩ.

While the Slave Processor is executing the instruction, the CPU is free to prefetch instructions into its queue. If it fills the queue before the Slave Processor finishes, the CPU will wait, applying Status Code 0011 (Waiting for Slave, Sec. 3.4.3).

Upon receiving the pulse on $\overline{SPC}$, the CPU uses $\overline{SPC}$ to read a Status Word from the Slave Processor, applying Status Code 1110 (Read Slave Status, Sec. 3.4.3). This word has the format shown in *Figure 3-34.* If the Q bit ("Quit", Bit 0) is set, this indicates that an error was detected by the Slave Processor. The CPU will not continue the protocol, but will immediately trap through the SLAVE vector in the Interrupt Table. Certain Slave Processor instructions cause CPU PSR bits to be loaded from the Status Word.

The last step in the protocol is for the CPU to read a result, if any, and transfer it to the destination. The Read cycles from the Slave Processor are performed by the CPU while applying Status Code 1101 (Transfer Slave Operand, Sec. 3.4.3).

An exception to the protocol above is the LMR (Load Memory Management Register) instruction, and a corresponding Custom Slave instruction (LCR: Load Custom Register). In executing these instructions, the protocol ends after the CPU has issued the last operand. The CPU does not wait for an acknowledgement from the Slave Processor, and it does not read status.

3.0 Functional Description (Continued)

Status Combinations:
Send ID (ID): Code 1111
Xfer Operand (OP): Code 1101
Read Status (ST): Code 1110

Step	Status	Action
1	ID	CPU Send ID Byte.
2	OP	CPU Sends Operaton Word.
3	OP	CPU Sends Required Operands
4	—	Slave Starts Execution. CPU Pre-fetches.
5	—	Slave Pulses $\overline{SPC}$ Low.
6	ST	CPU Reads Status Word. (Trap? Alter Flags?)
7	OP	CPU Reads Results (If Any).

FIGURE 3-31. 16-Bit Slave Processor Protocol

3.9.2 32-Bit Fast Slave Protocol

Upon receiving a Slave Processor instruction, the CPU initiates the sequence outlined in *Figure 3-32*. While applying Status code 1111 (Broadcast ID Sec. 3.4.2), the CPU transfers the ID Byte on bits AD24–AD31, the operation word on bits AD8–AD23 in a swapped order of bytes and a non-used byte XXXXXXX1 (X = don't care) on bits AD0–AD7 (*Figure 3-33*).

Using the addressing mode fields within the Operation word, the CPU fetches operands and sends them to the Slave Processor. Since the CPU is solely responsible for memory accesses, addressing mode extensions are not sent to the Slave Processor. The Status Code applied is 1101 (Transfer Slave Processor Operand Sec. 3.4.2). After the CPU has issued the last operand, the Slave Processor starts the actual execution of the instruction. Upon completion, it will signal the CPU by pulsing $\overline{SDONE}$ or $\overline{SPC}$ low for one clock cycle.

Unlike the old protocol, the SLAVE may request the CPU to read the status by activating the $\overline{SDONE}$ or $\overline{SPC}$ line for two clock cycles instead of one. The CPU will then read the slave status word and update the PSR Register, unless a trap is signalled. If this happens, the CPU will immediately abort the protocol and start a trap sequence using either the SLAVE or the UND vector in the interrupt table as specified in the Status Word.

Note: The PSR update is presently restricted to three instructions: CMPf, RDVAL, WRVAL and their custom slave equivalents.

While the Slave Processor is executing the instruction, the CPU is free to prefetch instructions into its queue. If it fills its queue before the Slave Processor finishes, the CPU will wait applying status code 0011 (waiting for Slave, Sec. 3.4.2).

Upon receiving the pulse on either $\overline{SDONE}$ or $\overline{SPC}$, the CPU uses $\overline{SPC}$ to read the result from the Slave Processor and transfer it to the destination. The Read cycles from the Slave Processor are performed by the CPU while applying Status Code 1101 (Transfer Slave Operand, Sec. 3.4.2).

Status Combinations:
Send ID (ID): Code 1111
Xfer Operand (OP): Code 1101
Read Status (ST): Code 1110

Step	Status	Action
1	ID	CPU sends ID and Operation Word.
2	OP	CPU sends required operands (if any).
3	—	Slave starts execution (CPU prefetches).*
4	—	Slave pulses $\overline{SDONE}$ or $\overline{SPC}$ low.
5	ST	CPU Reads Status word (only if $\overline{SDONE}$ or $\overline{SPC}$ pulse is two clock cycles wide).
6	OP	CPU Reads Results (if any).

FIGURE 3-32. 32-Bit Fast Slave Protocol

Certain Slave Processor instructions affect CPU PSR. For these instructions only the CPU will perform a Read Slave status cycle as described in 3.9.1.1 before reading the result. The relevent PSR bits will be loaded from the status word.

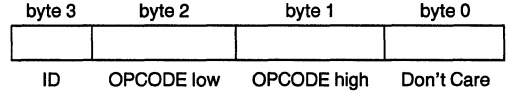

FIGURE 3-33. ID and Opcode Format for Fast Slave Protocol

3.9.3 Floating Point Instructions

Table 3-4 gives the protocols followed for each Floating Point instruction. The instructions are referenced by their mnemonics. For the bit encodings of each instruction, see Appendix A.

The Operand class columns give the Access Class for each general operand, defining how the addressing modes are interpreted (see Instruction Set Reference Manual).

The Operand Issued columns show the sizes of the operands issued to the Floating Point Unit by the CPU. "D" indicates a 32-bit Double Word. "i" indicates that the instruction specifies an integer size for the operand (B = Byte, W = Word, D = Double Word). "f" indicates that the instruction specifies a Floating Point size for the operand (F = 32-bit Standard Floating, L = 64-bit Long Floating).

The Returned Value Type and Destination column gives the size of any returned value and where the CPU places it. The PSR Bits Affected column indicates which PSR bits, if any, are updated from the Slave Processor Status Word (*Figure 3-34*).

3.0 Functional Description (Continued)

TABLE 3-4
Floating Point Instruction Protocols.

Mnemonic	Operand 1 Class	Operand 2 Class	Operand 1 Issued	Operand 2 Issued	Returned Value Type and Dest.	PSR Bits Affected
ADDf	read.f	rmw.f	f	f	f to Op. 2	none
SUBf	read.f	rmw.f	f	f	f to Op. 2	none
MULf	read.f	rmw.f	f	f	f to Op. 2	none
DIVf	read.f	rmw.f	f	f	f to Op. 2	none
MOVf	read.f	write.f	f	N/A	f to Op. 2	none
ABSf	read.f	write.f	f	N/A	f to Op. 2	none
NEGf	read.f	write.f	f	N/A	f to Op. 2	none
CMPf	read.f	read.f	f	f	N/A	N,Z,L
FLOORfi	read.f	write.i	f	N/A	i to Op. 2	none
TRUNCfi	read.f	write.i	f	N/A	i to Op. 2	none
ROUNDfi	read.f	write.i	f	N/A	i to Op. 2	none
MOVFL	read.F	write.L	F	N/A	L to Op. 2	none
MOVLF	read.L	write.F	L	N/A	F to Op. 2	none
MOVif	read.i	write.f	i	N/A	f to Op. 2	none
POLYf	read.f	read.f	f	f	f to F0	none
DOTf	read.f	read.f	f	f	f to F0	none
SCALBf	read.f	rmw.f	f	f	f to Op.2	none
LOGBf	read.f	write.f	f	N/A	f to Op.2	none
LFSR	read.D	N/A	D	N/A	N/A	none
SFSR	N/A	write.D	N/A	N/A	D to Op. 2	none

Note 1:

D = Double Word

i = Integer size (B,W,D) specified in mnemonic.

f = Floating Point type (F,L) specified in mnemonic.

N/A = Not Applicable to this instruction.

Any operand indicated as being of type "f" will not cause a transfer if the Register addressing mode is specified. This is because the Floating Point Registers are physically on the Floating Point Unit and are therefore available without CPU assistance.

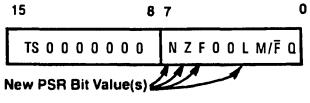

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FIGURE 3-34. Slave Processor Status Word Format

Note 1: Q is the Trap Bit. It is set to 1 by the Slave whenever a trap is requested.

Note 2: TS is the Trap Select Bit. When a trap is requested (Q = 1), TS tells the CPU whether a SLAVE or an UND trap is to be generated. TS is 0 for a slave trap and 1 for an UND trap.

Note 3: M/$\overline{F}$ should be set for a RDVAL, WRVAL, or Custom Slave Equivalent instruction. It should be cleared for CMPf and CCMP0c and CCMPc. When M/$\overline{F}$ is cleared, the F bit should also be cleared.

3.9.4 Memory Management Instructions

Table 3-5 gives the protocols for Memory Management instructions. Encodings for these instructions may be found in Appendix A.

In executing the RDVAL and WRVAL instructions, the CPU calculates and issues the 32-bit Effective Address of the single operand. The CPU then performs a single-byte Read cycle from that address, allowing the MMU to safely abort the instruction if the necessary information is not currently in physical memory. Upon seeing the memory cycle complete, the MMU continues the protocol, and returns the validation result in the F bit of the Slave Status Word.

The size of a Memory Management operand is always a 32-bit Double Word. For further details of the Memory Management Instruction set, see the Instruction Set Reference Manual and the MMU Data Sheet.

3.0 Functional Description (Continued)

TABLE 3-5
Memory Management Instruction Protocols.

Mnemonic	Operand 1 Class	Operand 2 Class	Operand 1 Issued	Operand 2 Issued	Returned Value Type and Dest.	PSR Bits Affected
RDVAL*	addr	N/A	D	N/A	N/A	F
WRVAL*	addr	N/A	D	N/A	N/A	F
LMR*	read.D	N/A	D	N/A	N/A	none
SMR*	write.D	N/A	N/A	N/A	D to Op. 1	none

Note:

In the RDVAL and WRVAL instructions, the CPU issues the address as a Double Word, and performs a single-byte Read cycle from that memory address. For details, see the Instruction Set Reference Manual and the Memory Management Unit Data Sheet.

D = Double Word

* = Privileged Instruction: will trap if CPU is in User Mode.

N/A = Not Applicable to this instruction.

3.9.5 Custom Slave Instructions

Provided in the NS32332 is the capability of communicating with a user-defined, "Custom" Slave Processor. The instruction set provided for a Custom Slave Processor defines the instruction formats, the operand classes and the communication protocol. Left to the user are the interpretations of the Op Code fields, the programming model of the Custom Slave and the actual types of data transferred. The protocol specifies only the size of an operand, not its data type.

Table 3-6 lists the relevant information for the Custom Slave instruction set. The designation "c" is used to represent an operand which can be a 32-bit ("D") or 64-bit ("Q") quantity in any format; the size is determined by the suffix on the mnemonic. Similarly, an "i" indicates an integer size (Byte, Word, Double Word) selected by the corresponding mnemonic suffix.

Any operand indicated as being of type "c" will not cause a transfer if the register addressing mode is specified. It is assumed in this case that the slave processor is already holding the operand internally.

For the instruction encodings, see Appendix A.

3.0 Functional Description (Continued)

TABLE 3-6
Custom Slave Instruction Protocols.

Mnemonic	Operand 1 Class	Operand 2 Class	Operand 1 Issued	Operand 2 Issued	Returned Value Type and Dest.	PSR Bits Affected
CCAL0c	read.c	rmw.c	c	c	c to Op. 2	none
CCAL1c	read.c	rmw.c	c	c	c to Op. 2	none
CCAL2c	read.c	rmw.c	c	c	c to Op. 2	none
CCAL3c	read.c	rmw.c	c	c	c to Op. 2	none
CMOV0c	read.c	write.c	c	N/A	c to Op. 2	none
CMOV1c	read.c	write.c	c	N/A	c to Op. 2	none
CMOV2c	read.c	write.c	c	N/A	c to Op. 2	none
CMOV3c	read.c	write.c	c	N/A	c to Op.2	none
CCMP0c	read.c	read.c	c	c	N/A	N,Z,L
CCMP1c	read.c	read.c	c	c	N/A	N,Z,L
CCV0ci	read.c	write.i	c	N/A	i to Op. 2	none
CCV1ci	read.c	write.i	c	N/A	i to Op. 2	none
CCV2ci	read.c	write.i	c	N/A	i to Op. 2	none
CCV3ic	read.i	write.c	i	N/A	c to Op. 2	none
CCV4DQ	read.D	write.Q	D	N/A	Q to Op. 2	none
CCV5QD	read.Q	write.D	Q	N/A	D to Op. 2	none
LCSR	read.D	N/A	D	N/A	N/A	none
SCSR	N/A	write.D	N/A	N/A	D to OP. 2	none
CATST0*	addr	N/A	D	N/A	N/A	F
CATST1*	addr	N/A	D	N/A	N/A	F
LCR*	read.D	N/A	D	N/A	N/A	none
SCR*	write.D	N/A	N/A	N/A	D to Op.1	none

Note:
D = Double Word
i = Integer size (B,W,D) specified in mnemonic.
c = Custom size (D:32 bits or Q:64 bits) specified in mnemonic.
* = Privileged instruction: will trap if CPU is in User Mode.
N/A = Not Applicable to this instruction.

4.0 Device Specifications

4.1 NS32332 PIN DESCRIPTIONS

The following is a brief description of all NS32332 pins. The descriptions reference portions of the Functional Description, Section 3.

Unless otherwise indicated, reserved pins should be left open.

4.1.1 Supplies

Logic Power ($V_{CCL1, 2}$): +5V positive supply.

Buffers Power ($V_{CCB1, 2, 3, 4, 5}$): +5V positive supply.

Logic Ground (GNDL1, GNDL2): Ground reference for on-chip logic.

Buffer Grounds (GNDB1, GNDB2, GNDB3, GNDB4, GNDB5, GNDB6): Ground references for on-chip drivers.

Back Bias Generator (BBG): Output of on-chip substrate voltage generator.

4.1.2 Input Signals

Clocks (PHI1, PHI2): Two-phase clocking signals.

Ready (RDY): Active high. While RDY is not active, the CPU adds wait cycles to the current bus cycle. Not applicable for slave cycles.

Hold Request ($\overline{\text{HOLD}}$): Active low. Causes the CPU to release the bus for DMA or multiprocessing purposes.

Note: If the $\overline{\text{HOLD}}$ signal is generated asynchronously, it's set up and hold times may be violated. In this case it is recommended to synchronize it with CTTL to minimize the possibility of metastable states.

The CPU provides only one synchronization stage to minimize the $\overline{\text{HLDA}}$ latency. This is to avoid speed degradations in cases of heavy $\overline{\text{HOLD}}$ activity (i.e. DMA controller cycles interleaved with CPU cycles.)

Interrupt ($\overline{\text{INT}}$): Active low. Maskable Interrupt request.

Non-Maskable Interrupt ($\overline{\text{NMI}}$): Active low. Non-Maskable Interrupt request.

Reset/Abort ($\overline{\text{RST}}/\overline{\text{ABT}}$): Active low. If held active for one clock cycle and released, this pin causes an ABORT. If held longer, it is interpreted as RESET.

Bus Error ($\overline{\text{BER}}$): Active low. When active, indicates that an error occurred during a bus cycle. It is treated by the CPU as the highest priority exception after RESET. Not applicable for slave cycles.

Bus Retry ($\overline{\text{BRT}}$): Active low. When active, the CPU will re-execute the last bus cycle. Not applicable for slave cycles.

Bus Width (BW1, BW0): Define the bus width (8, 16, 32) in every bus cycle. 01–8 bits, 10–16 bits, 11–32 bits. 00 is a reserved combination. Not applicable for slave cycles.

Burst in ($\overline{\text{BIN}}$): Active low. When active, the CPU may perform burst cycles.

Float ($\overline{\text{FLT}}$): Active low. Float command input. In non-memory managed systems, this pin should be tied to V_{CC} through a 10 kΩ resistor.

Data Timing/Slave Done ($\overline{\text{DT}}/\overline{\text{SDONE}}$): Active low. Used by a 32-bit slave processor to acknowledge the completion of an instruction and/or indicate that the slave status should be read (Section 3.9.2). Sampled during reset to select the data timing during write cycles (Section 3.3).

4.1.3 Output Signals

Address Strobe ($\overline{\text{ADS}}$): Active low. Controls address latches, indicates the start of a bus cycle.

Data Direction in ($\overline{\text{DDIN}}$): Active low. Indicates the directions of data transfers.

Byte Enables ($\overline{\text{BE0}}$–$\overline{\text{BE3}}$): Active low. Enable the access of bytes 0–3 in a 32 bit system.

Status (ST0–ST3): Bus cycle status code, ST0 least significant. Encodings are:

0000 — Idle: CPU Inactive on Bus.
0001 — Idle: WAIT Instruction.
0010 — (Reserved).
0011 — Idle: Waiting for Slave.
0100 — Interrupt Acknowledge, Master.
0101 — Interrupt Acknowledge, Cascaded.
0110 — End of Interrupt, Master.
0111 — End of Interrupt, Cascaded.
1000 — Sequential Instruction Fetch.
1001 — Non-Sequential Instruction Fetch.
1010 — Data Transfer.
1011 — Read Read-Modify-Write Operand.
1100 — Read for Effective Address.
1101 — Transfer Slave Operand.
1110 — Read Slave Status Word.
1111 — Broadcast Slave ID.

Status Strobe ($\overline{\text{STS}}$): Active low. Indicates that a new status (ST0–ST3) is valid. Not applicable for slave cycles.

Multiple Cycle/Exception Status ($\overline{\text{MC}}/\overline{\text{EXS}}$): Active low. This signal is activated during the access of the first part of an operand that crosses a double word address boundary.

It is also activated in conjunction with status codes 1001 and 0000 during Abort Acknowledge and when a fatal bus error occurs.

Note: $\overline{\text{MC}}/\overline{\text{EXS}}$ indicates a fatal bus error only when it has been active for more than one clock cycle.

Hold Acknowledge ($\overline{\text{HLDA}}$): Active low. Activated by the CPU in response to HOLD input. Indicates that the CPU has released the bus.

User/Supervisor (U/$\overline{\text{S}}$): User or Supervisor Mode status.

Interlocked Operation ($\overline{\text{ILO}}$): Active low. Indicates that an interlocked cycle is being performed.

Program Flow Status ($\overline{\text{PFS}}$): Active low. A pulse that indicates the beginning of an instruction execution.

Burst Out ($\overline{\text{BOUT}}$): Active low. When active, indicates that the CPU will perform burst cycles.

4.1.4 Input/Output Signals

Address/Data 0–31 (AD0–AD31): Multiplexed address and data lines.

Slave Processor Control ($\overline{\text{SPC}}$): Active low. Used by the CPU as a data strobe output for slave processor transfers. Used by a 16-bit slave processor to acknowledge the completion of an instruction.

4.0 Device Specifications (Continued)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

4.2 ABSOLUTE MAXIMUM RATINGS

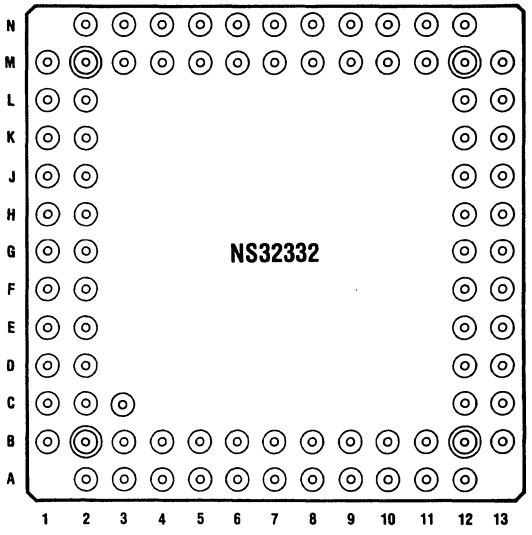
Temperature Under Bias	0°C to +70°C
Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to GND	−0.5V to +7V
Power Dissipation	3 Watt

Note: *Absolute maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended; operation should be limited to those conditions specified under Electrical Characteristics.*

4.3 ELECTRICAL CHARACTERISTICS $T_A = 0°$ to $+70°C$, $V_{CC} = 5V \pm 5\%$, GND = 0V

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High Level Input Voltage		2.0		V_{CC} +0.5	V
V_{IL}	Low Level Input Voltage		−0.5		0.8	V
V_{CH}	High Level Clock Voltage	PHI1, PHI2 pins only	V_{CC} −0.5		V_{CC} +0.5	V
V_{CL}	Low Level Clock Voltage	PHI1, PHI2 pins only	−0.5		0.3	V
V_{CRT}	Clock Input Ringing Tolerance	PHI1, PHI2 pins only	−0.5		0.5	V
V_{OH}	High Level Output Voltage	$I_{OH} = -400\ \mu A$	2.4			V
V_{OL}	Low Level Output Voltage	$I_{OL} = 2$ mA			0.45	V
I_{ILS}	$\overline{SPC}$ and $\overline{DT}/\overline{SDONE}$ Input Current (low)	$V_{IN} = 0.4V$, $\overline{SPC}$ in input mode	0.05		1.0	mA
I_I	Input Load Current	$0 \le V_{IN} \le V_{CC}$, Input Pins except PHI1, PHI2, $\overline{DT}/\overline{SDONE}$	−20		20	μA
I_L	Leakage Current (Output and I/O pins in TRI-STATE/Input Mode)	$0.4 \le V_{IN} \le V_{CC}$	−80		80	μA
I_{CC}	Active Supply Current	$I_{OUT} = 0$, $T_A = 25°C$		450	600	mA

Connection Diagram*



Bottom View

NS32332 Pinout Descriptions
84 Pin Grid Array

Desc	Pin	Desc	Pin	Desc	Pin
GNDB1	B1	AD29	N6	$\overline{BOUT}$	E12
AD6	B2	AD30	M6	$\overline{SPC}$	D13
AD7	C1	AD31	N7	$\overline{MC}/\overline{EXS}$	D12
AD8	C2	VCCL1	M7	VCCB5	C13
AD9	D1	VCCL2	N8	$\overline{ADS}$	C12
AD10	D2	$\overline{INT}$	M8	GNDB6	B13
AD11	E1	$\overline{NMI}$	N9	$\overline{DDIN}$	A12
GNDB2	E2	RESERVED	M9	$\overline{BE0}$	B12
AD12	F1	RESERVED	N10	$\overline{BE1}$	A11
AD13	F2	RESERVED	M10	$\overline{BE2}$	B11
AD14	G1	RESERVED	N11	$\overline{BE3}$	A10
AD15	G2	$\overline{ILO}$	M11	$\overline{HLDA}$	B10
VCCB2	H1	VCCB4	N12	$\overline{HOLD}$	A9
AD16	H2	ST3	M13	RDY	B9
AD17	J1	ST2	M12	$\overline{DT}/\overline{SDONE}$	A8
AD18	J2	ST1	L13	PHI 2	B8
AD19	K1	ST0	L12	PHI 1	A7
GNDB3	K2	$\overline{STS}$	K13	BBG	B7
AD20	L1	GNDB5	K12	GNDL2	A6
AD21	L2	$\overline{PFS}$	J13	GNDL1	B6
AD22	M1	U/$\overline{S}$	J12	VCCB1	A5
AD23	N2	BW1	H13	AD0	B5
VCCB3	M2	BW0	H12	AD1	A4
AD24	N3	$\overline{BIN}$	G13	AD2	B4
AD25	M3	$\overline{FLT}$	G12	AD3	A3
AD26	N4	$\overline{RST}/\overline{ABT}$	F13	AD4	B3
AD27	M4	$\overline{BRT}$	F12	AD5	A2
GNDB4	N5	$\overline{BER}$	E13	POSITION PIN	C3
AD28	M5				

Order Number NS32332U-10 or NS32332U-15
See NS Package Number U84C

FIGURE 4-1. Pin Grid Array Package

*AMP sockets are recommended for use with NS32332 CPU. AMP sockets are manufactured by AMP INCORPORATED, Harrisburg PA.

4.0 Device Specifications (Continued)

4.4 SWITCHING CHARACTERISTICS

4.4.1 Definitions

All the timing specifications given in this section refer to 2.0V on the rising or falling edges of the clock phases PHI1 and PHI2 and 0.8V or 2.0V on all other signals as illustrated below, unless specifically stated otherwise.

ABBREVIATIONS:

L.E. — leading edge
T.E. — trailing edge
R.E. — rising edge
F.E. — falling edge

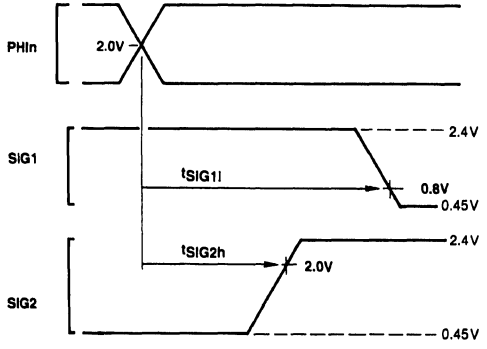


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FIGURE 4-2. Timing Specification Standard (Signal Valid After Clock Edge)

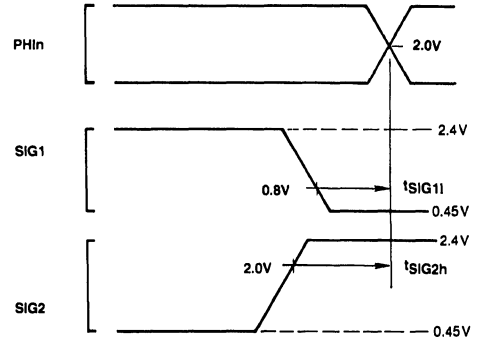

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FIGURE 4-3. Timing Specification Standard (Signal Valid Before Clock Edge)

4.4.2 Timing Tables

4.4.2.1 Output Signals: Internal Propagation Delays, NS32332-10, NS32332-15

Maximum times assume capacitive loading of 100 pF.

AD0–31, $\overline{ADS}$ and $\overline{BOUT}$ timings are defined with a capacitive loading of 75 pF.

Symbol	Figure	Description	Reference/ Conditions	NS32332-10		NS32332-15		Units
				Min	Max	Min	Max	
t_{ALv}	4-5	Address bits 0–31 valid	after R.E., PHI1 T1		30		20	ns
t_{ALh}	4-5	Address bits 0–31 hold	after R.E., PHI1 T2/Tmmu	10		6		ns
t_{Dv}	4-5	Data valid (write cycle)	after R.E., PHI1 T3 or T2		50		38	ns
t_{Dh}	4-5	Data hold (write cycle)	after R.E., PHI1 next T1 or Ti	0		0		ns
t_{ALADSs}	4-4	Address bits 0–31 setup	before $\overline{ADS}$ T.E.	25		20		ns
t_{ALADSh}	4-18	Address bits 0–31 hold	after $\overline{ADS}$ T.E.	10		10		ns
t_{ALf}	4-4	Address bits 0–31 floating (no MMU)	after R.E., PHI1 T2/Tmmu		25		24	ns
t_{ALMf}	4-18	Address bits 0–31 floating (by $\overline{FLT}$ line)	after R.E., PHI1 Tf		40		40	ns
t_{STSa}	4-3,4-5	$\overline{STS}$ signal active (low)	after R.E., PHI1 T4 of previous bus cycle or Ti		35		25	ns
t_{STSia}	4-3,4-5	$\overline{STS}$ signal inactive	after R.E., PHI2 T4 of previous bus cycle or Ti		45		30	ns
t_{STSw}	4-3	$\overline{STS}$ pulse width	at 0.8V (both edges)	35		24		ns
t_{BErv}	4-4,4-6	$\overline{BEn}$ signals valid (Operand Read Cycles Only)	after R.E., PHI2, T4 or Ti		140		95	ns
t_{BEv}	4-5,4-6	$\overline{BEn}$ signals valid	after R.E., PHI2, T4 or Ti		85		58	ns
t_{BEh}	4-4	$\overline{BEn}$ signals hold	after R.E., PHI2, T4	0		0		ns

4.0 Device Specifications (Continued)

4.4.2.1 Output Signals: Internal Propagation Delays, NS32332-10, NS32332-15 (Continued)

Symbol	Figure	Description	Reference/ Conditions	NS32332-10		NS32332-15		Units
				Min	Max	Min	Max	
t_{STv}	4-5	Status (ST0–ST3) valid	after R.E., PHI1 T4 (before T1, see note)		50		35	ns
t_{STSTSs}	4-5	Status Signals Setup	Before $\overline{STS}$ T.E.	10		6		ns
t_{STh}	4-5	Status (ST0–ST3) hold	after R.E., PHI1 T4 (after T1)	0		0		ns
t_{DDINv}	4-4	$\overline{DDIN}$ signal valid	after R.E., PHI1 T1		35		25	ns
t_{DDINh}	4-4	$\overline{DDIN}$ signal hold	after R.E., PHI1 next T1 or Ti	0		0		ns
t_{ADSa}	4-5	$\overline{ADS}$ signal active (low)	after R.E., PHI1 T1		25		17	ns
t_{ADSia}	4-5	$\overline{ADS}$ signal inactive	after R.E., PHI2 T1		45		29	ns
t_{ADSw}	4-5	$\overline{ADS}$ pulse width	at 0.8V (both edges)	35		24		ns
t_{MCa}	4-4,4-5	$\overline{MC}$ signal active (low)	after R.E., PHI1 T1		70		50	ns
t_{MCia}	4-4,4-5	$\overline{MC}$ signal inactive	after R.E., PHI1 T1 or T3 (burst)		70		50	ns
t_{ALf}	4-15	AD0–AD31 floating (caused by $\overline{HOLD}$)	after R.E., PHI1 T1		25		24	ns
t_{ADSf}	4-15, 4-17	$\overline{ADS}$ floating (caused by $\overline{HOLD}$)	after R.E., PHI1 Ti		55		40	ns
t_{BEf}	4-15, 4-17	$\overline{BEn}$ floating (caused by $\overline{HOLD}$)	after R.E., PHI1 Ti		55		40	ns
t_{DDINf}	4-15, 4-17	$\overline{DDIN}$ floating (caused by $\overline{HOLD}$)	after R.E., PHI1 Ti		55		45	ns
t_{HLDAa}	4-15, 4-16	$\overline{HLDA}$ signal active (low)	after R.E., PHI1 T4		60		45	ns
t_{HLDAia}	4-18	$\overline{HLDA}$ signal inactive	after R.E., PHI1 Ti		60		45	ns
t_{ADSr}	4-18	$\overline{ADS}$ signal returns from floating (caused by $\overline{HOLD}$)	after R.E., PHI1 Ti		55		40	ns
t_{BEr}	4-18	$\overline{BEn}$ signals return from floating (caused by $\overline{HOLD}$)	after R.E., PHI1 Ti		55		40	ns
t_{DDINr}	4-18	$\overline{DDIN}$ signal returns from floating (caused by $\overline{HOLD}$)	after R.E., PHI1 Ti		55		40	ns
t_{DDINf}	4-19	$\overline{DDIN}$ signal floating (caused by $\overline{FLT}$)	after $\overline{FLT}$ F.E.		50		45	ns
t_{DDINr}	4-20	$\overline{DDIN}$ signal returns from floating (caused by $\overline{FLT}$)	after $\overline{FLT}$ R.E.		40		28	ns
t_{SPCa}	4-21	$\overline{SPC}$ output active (low)	after R.E., PHI1 T1		30		21	ns
t_{SPCia}	4-21	$\overline{SPC}$ output inactive	after R.E., PHI1 T4	2	35	2	26	ns
t_{SPCnf}	4-24	$\overline{SPC}$ output nonforcing	after R.E., PHI2 T4		10		8	ns
t_{Dv}	4-21	Data valid (slave processor write)	after R.E., PHI1 T1		50		38	ns
t_{Dh}	4-21	Data hold (slave processor write)	after R.E., PHI1 next T1 or Ti	0		0		ns
t_{PFSw}	4-26	$\overline{PFS}$ pulse width	at 0.8V (both edges)	70		45		ns
t_{PFSa}	4-26	$\overline{PFS}$ pulse active (low)	after R.E., PHI2		50		38	ns
t_{PFSia}	4-26	$\overline{PFS}$ pulse inactive	after R.E., PHI2		50		38	ns
t_{USv}	4-33	U/$\overline{S}$ signal valid	after R.E., PHI1 T4		48		35	ns
t_{USh}	4-33	U/$\overline{S}$ signal hold	after R.E., PHI1 T4	10		6		ns
t_{NSPF}	4-28	Nonsequential fetch to next $\overline{PFS}$ clock cycle	after R.E., PHI1 T1	4		4		t_{Cp}

4.0 Device Specifications (Continued)

4.4.2.1 Output Signals: Internal Propagation Delays, NS32332-10, NS32332-15 (Continued)

Symbol	Figure	Description	Reference/ Conditions	NS32332-10		NS32332-15		Units
				Min	Max	Min	Max	
t_{PFNS}	4-27	$\overline{PFS}$ clock cycle to next non-sequential fetch	before R.E., PHI1 T1	4		4		t_{Cp}
t_{STSf}	4-15, 4-16	$\overline{STS}$ floating (HOLD)	after R.E., PHI1 Ti		55		44	ns
t_{STSr}	4-18	$\overline{STS}$ not floating (HOLD)	after R.E., PHI1 Ti, T4		55		40	ns
t_{BOUTa}	4-6, 4-10	$\overline{BOUT}$ output active	after R.E., PHI2 Tmmu		100		66	ns
t_{BOUTia}	4-6, 4-10	$\overline{BOUT}$ output inactive	after R.E., PHI2 T3 or T4		75		40	ns
t_{ILOa}	4-14	$\overline{ILO}$ signal active	after R.E., PHI1 T4		50		38	ns
t_{ILOia}	4-14	$\overline{ILO}$ signal inactive	after R.E., PHI1 Ti		50		38	ns

Note: Every memory cycle starts with T4, during which Cycle Status is applied. If the CPU was idling, the sequence will be: ". . . Ti, T4, T1 . . .". If the CPU was not idling, the sequence will be: ". . . T4, T1 . . .".

4.4.2.2 Input Signal Requirements: NS32332-10, NS32332-15

Symbol	Figure	Description	Reference/ Conditions	NS32332-10		NS32332-15		Units
				Min	Max	Min	Max	
t_{PWR}	4-31	Power stable to $\overline{RST}$ R.E.	after V_{CC} reaches 4.5V	50		33		μs
t_{DIs}	4-4	Data in setup (read cycle)	before F.E., PHI2 T3	12		10		ns
t_{DIh}	4-4	Data in hold (read cycle)	after R.E., PHI1 T4	3		3		ns
t_{HLDa}	4-15 4-16,	$\overline{HOLD}$ active setup time	before F.E., PHI2 T2/Tmmu or T3 or Ti	25		17		ns
t_{HLDia}	4-18	$\overline{HOLD}$ inactive setup time	before F.E., PHI2 Ti	25		17		ns
t_{HLDh}	4-15, 4-17, 4-18	$\overline{HOLD}$ hold time	after R.E., PHI1 Ti or T3	0		0		ns
t_{FLTa}	4-19	$\overline{FLT}$ active (low) setup time	before F.E., PHI2 Tmmu	25		17		ns
t_{FLTia}	4-20	$\overline{FLT}$ inactive setup time	before F.E., PHI2 T3	25		17		ns
t_{RDYs}	4-4, 4-5, 4-6	RDY setup time	before F.E., PHI1 T3	20		12		ns
t_{RDYh}	4-4, 4-5, 4-6	RDY hold time	after R.E., PHI2 T3	4		3		ns
t_{ABTs}	4-29	$\overline{ABT}$ setup time ($\overline{FLT}$ inactive)	before F.E., PHI2 T2/Tmmu	20		13		ns
t_{ABTs}	4-30	$\overline{ABT}$ setup time ($\overline{FLT}$ active)	before F.E., PHI2 Tf	20		13		ns
t_{ABTh}	4-29, 4-30	$\overline{ABT}$ hold time	after R.E., PHI1 T3	0		0		ns
t_{RSTs}	4-31, 4-32	$\overline{RST}$ setup time	before F.E., PHI1	20		13		ns
t_{RSTw}	4-31, 4-32	$\overline{RST}$ pulse width	at 0.8V (both edges)	64		64		t_{Cp}
t_{INTs}	4-34	$\overline{INT}$ setup time	before F.E., PHI2	20		13		ns
t_{NMIw}	4-35	$\overline{NMI}$ pulse width	at 0.8V (both edges)	40		27		ns

4.0 Device Specifications (Continued)

4.4.2.2 Input Signal Requirements: NS32332-10, NS32332-15 (Continued)

Symbol	Figure	Description	Reference/ Conditions	NS32332-10		NS32332-15		Units
				Min	Max	Min	Max	
t_{DIs}	4-24	Data setup (slave read cycle)	before F.E., PHI2 T1	12		10		ns
t_{DIh}	4-24	Data hold (slave read cycle)	after R.E., PHI1 T4	3		3		ns
t_{DTs}	4-31	$\overline{DT}$ setup time	before F.E., PHI1	0		0		ns
t_{DTh}	4-31	$\overline{DT}$ hold time	after R.E., PHI1	0		0		ns
t_{SPCd}	4-24	$\overline{SPC}$ pulse delay from slave	after R.E., PHI2 T4	10		8		ns
t_{SPCs}	4-24	$\overline{SPC}$ setup time	before F.E., PHI1	25		15		ns
t_{SPCw}	4-24	$\overline{SPC}$ pulse width	at 0.8V (both edges)	20	100	13	66	ns
t_{SDNd}	4-23	$\overline{SDONE}$ pulse delay from slave	after R.E., PHI2 T4	10		8		ns
t_{SDNs}	4-23	$\overline{SDONE}$ setup time	before F.E., PHI1	25		15		ns
t_{SDNw}	4-23	$\overline{SDONE}$ pulse width	at 0.8V (both edges)	20	100	13	66	ns
t_{SDNSTw}	4-23	$\overline{SDONE}$ pulse width (to force CPU to read slave status)	at 0.8V (both edges)	175	275	115	200	ns
t_{BWs}	4-4, 4-5 4-6	$\overline{BW}$ 0–1 setup time	before F.E., PHI1 T3	25		13		ns
t_{BWh}	4-6	$\overline{BW}$0-1 hold time	after R.E., PHI1 T3 of Next Memory Access Cycle	0		0		ns
t_{BINs}	4-6, 4-7	$\overline{BIN}$ setup time (for each cycle of the burst)	before F.E., PHI1 T3	25		12		ns
t_{BINh}	4-6, 4-7	$\overline{BIN}$ hold time	after R.E., PHI1 T4	0		0		ns
t_{BERs}	4-12, 4-13	$\overline{BER}$ setup time	before F.E., PHI1 T4	25		14		ns
t_{BERh}	4-12, 4-13	$\overline{BER}$ hold time (see note)	after R.E., PHI1 Ti	0		0		ns
t_{BRTs}	4-8, 4-9, 4-10, 4-11	$\overline{BRT}$ setup time	before F.E., PHI1 T3 and T4	25		14		ns
t_{BRTh}	4-8, 4-9, 4-10	$\overline{BRT}$ hold time	after R.E., PHI1 T4 or Ti	0		0		ns

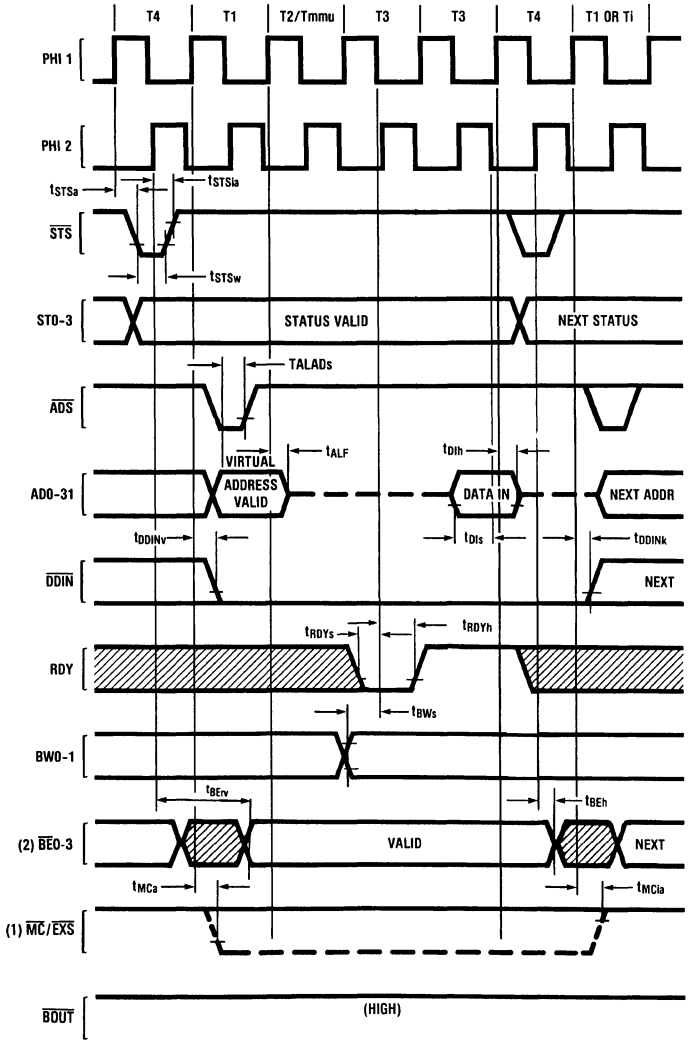
Note: A Ti state follows T4 when $\overline{BER}$ is asserted. $\overline{BER}$ should be deasserted at the latest in the beginning of the cycle following this Ti state.

4.4.2.3 Clocking Requirements: NS32332-10, NS32332-15

Symbol	Figure	Description	Reference/ Conditions	NS32332-10		NS32332-15		Units
				Min	Max	Min	Max	
t_{Cp}	4-25	Clock period	R.E., PHI1, PHI2 to next R.E., PHI1, PHI2	100	250	66	250	ns
$t_{CLw(1,2)}$	4-25	PHI1, PHI2 Pulse Width	At 2.0V on PHI1, PHI2 (Both Edges)	0.5 t_{cp} − 10 ns		0.5 t_{cp} − 6 ns		
$t_{CLh(1,2)}$	4-25	PHI1, PHI2 high time	At V_{CC}−0.9V on PHI1, PHI2 (Both Edges)	0.5 t_{cp} − 15 ns		0.5 t_{cp} − 10 ns		
t_{CLl}	4-25	PHI1, PHI2 low time	At 0.8V on PHI1, PHI2 (Both Edges)	0.5 t_{cp} −5 ns		0.5 t_{cp} −5 ns		
$t_{nOVL(1,2)}$	4-25	Non-overlap time	0.8V on F.E., PHI1, PHI2 to 0.8V on R.E., PHI2, PHI1	−2	2	−2	2	ns
t_{nOVLas}		Non-overlap asymmetry ($t_{nOVL(1)} - t_{nOVL(2)}$)	At 0.8V on PHI1, PHI2	−3	3	−3	3	ns
t_{CLhas}		PHI1, PHI2 asymmetry ($t_{CLh(1)} - t_{CLh(2)}$)	At V_{CC}−0.9V on PHI1, PHI2	−5	5	−3	3	ns

4.0 Device Specifications (Continued)

4.4.3 Timing Diagrams



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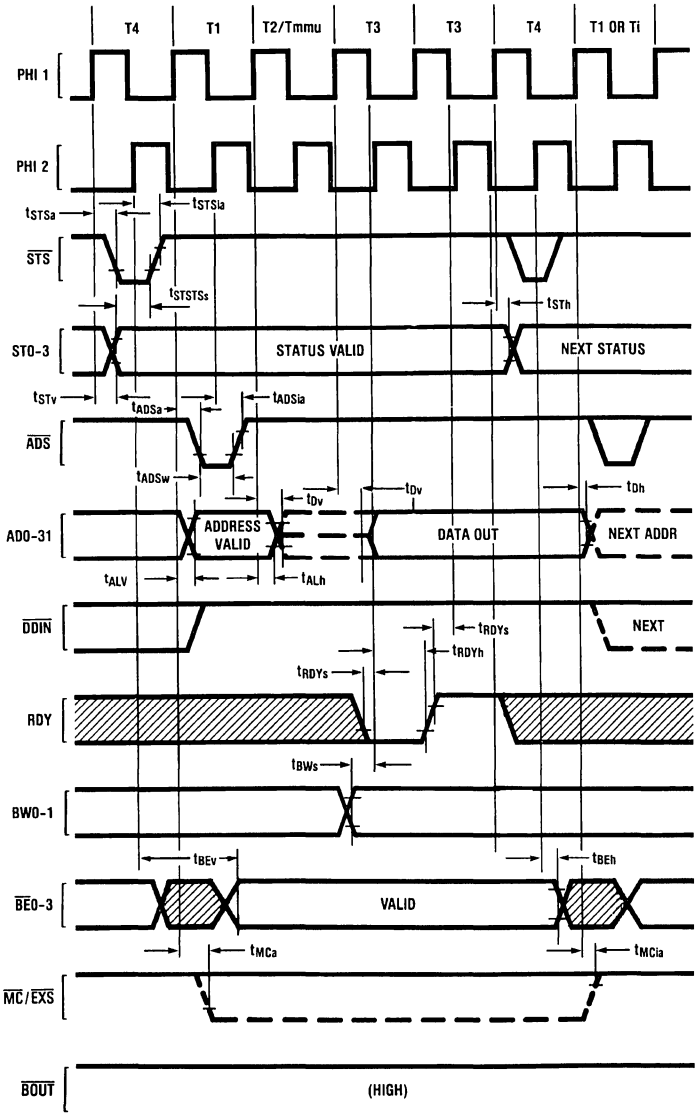
Note 1: Asserted (low) when the bus transaction crosses a double-word boundary (address bits A0–1 wrap around during the transaction).

Note 2: $\overline{BE0}$–$\overline{BE3}$ are all active during instruction fetch cycles.

FIGURE 4-4. NS32332 Read Cycle Timing

4.0 Device Specifications (Continued)



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Note: If $\overline{DT}/\overline{SDONE}$ is sampled low during reset, the CPU outputs the data during T2/TMMU (see Section 3.3).

FIGURE 4-5. NS32332 Write Cycle Timing

4.0 Device Specifications (Continued)

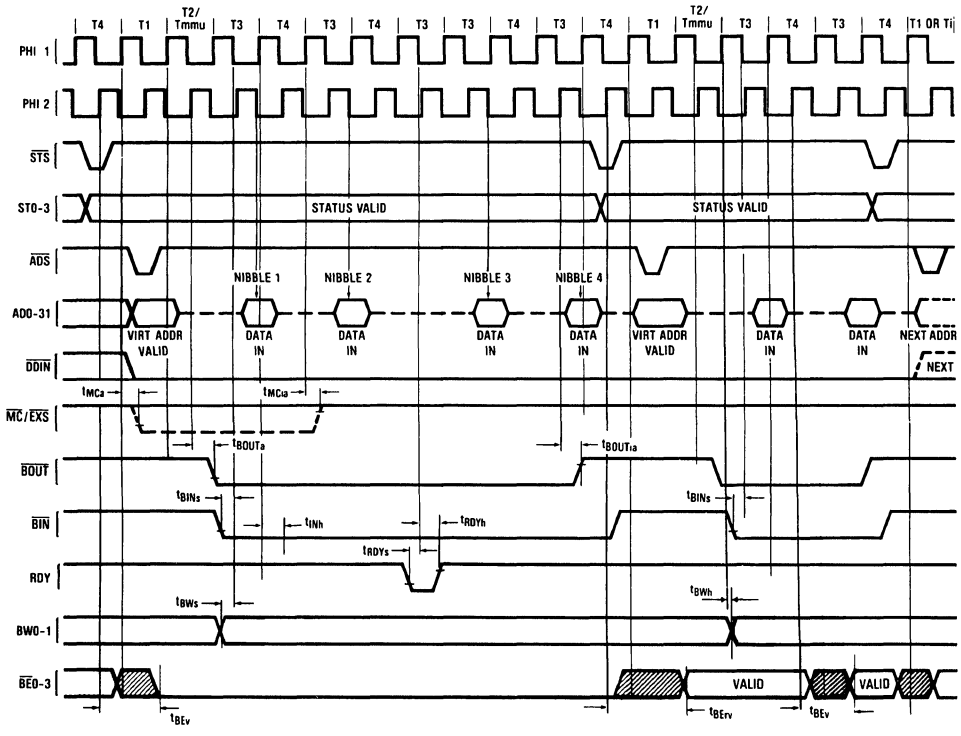

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FIGURE 4-6. NS32332 Burst Cycle Timing (Instruction fetches followed by Operand Reads)

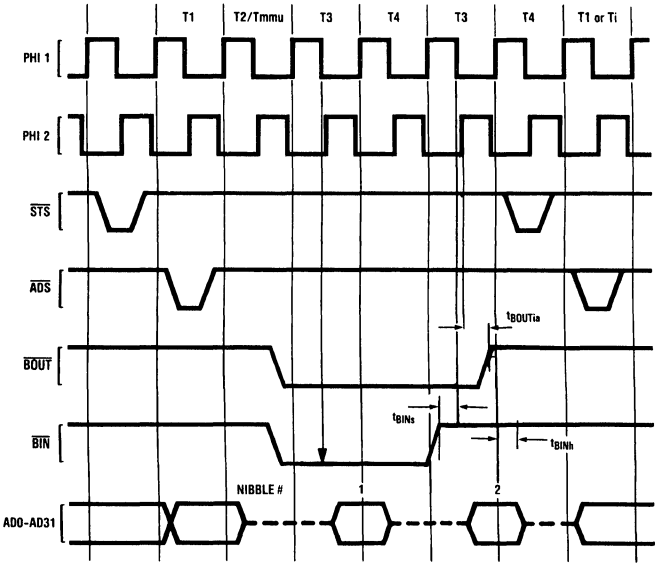

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FIGURE 4-7. External Termination of Burst Cycle

4.0 Device Specifications (Continued)

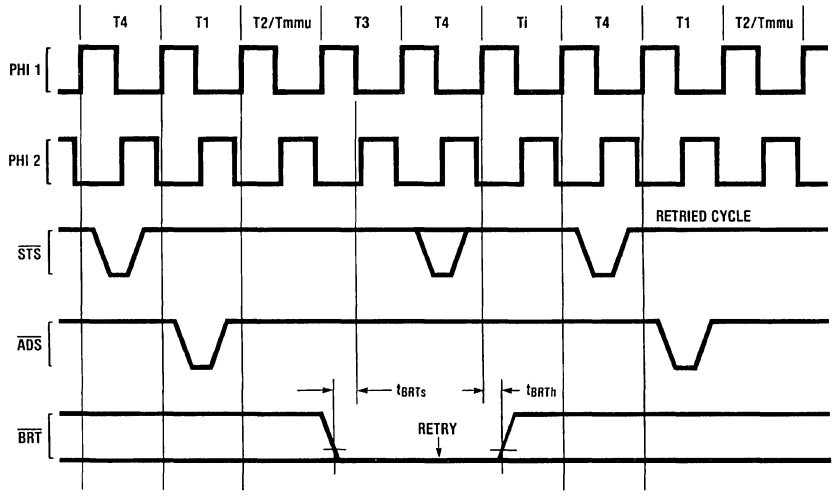

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FIGURE 4-8. Bus Retry During Normal Bus Cycle

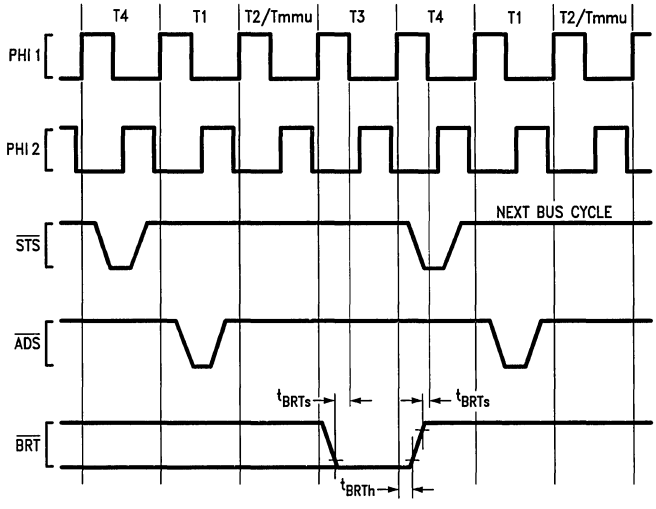

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FIGURE 4-9. $\overline{\text{BRT}}$ Activated, but no Bus Retry

4.0 Device Specifications (Continued)

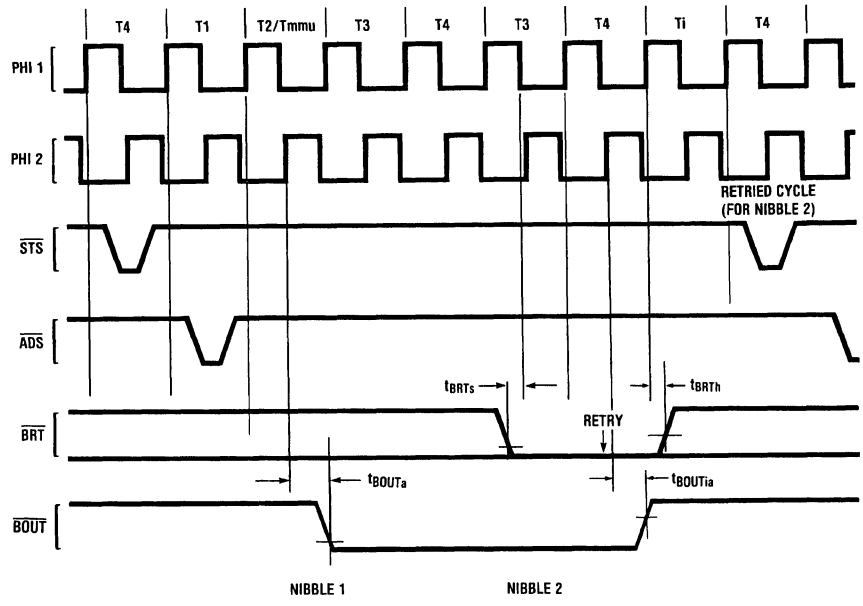

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FIGURE 4-10. Bus Retry During Burst Bus Cycle

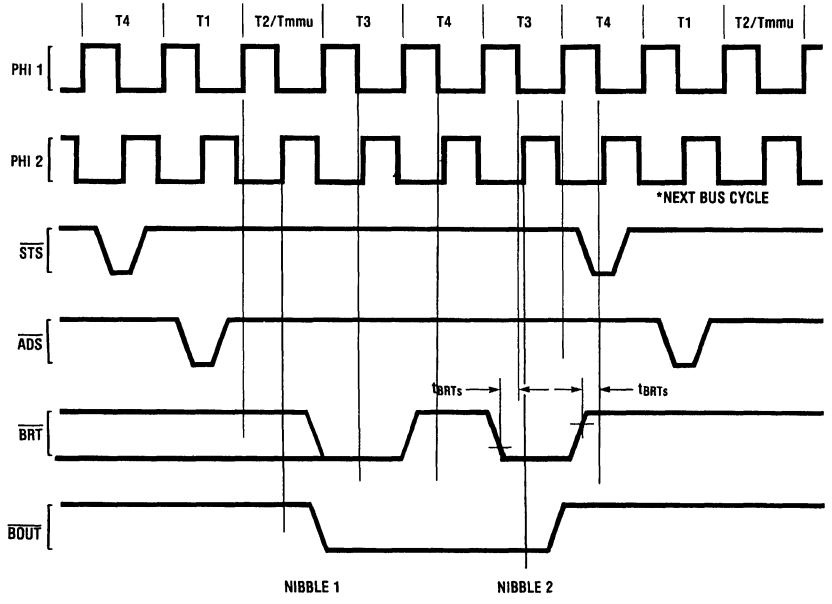

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FIGURE 4-11. $\overline{\text{BRT}}$ Activated During Burst Bus Cycle, but no Bus Retry

4.0 Device Specifications (Continued)

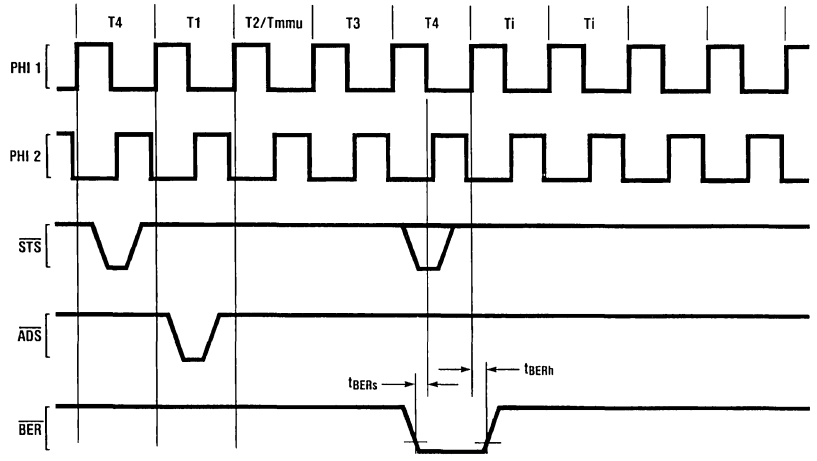

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FIGURE 4-12. Bus Error During Normal Bus Cycle

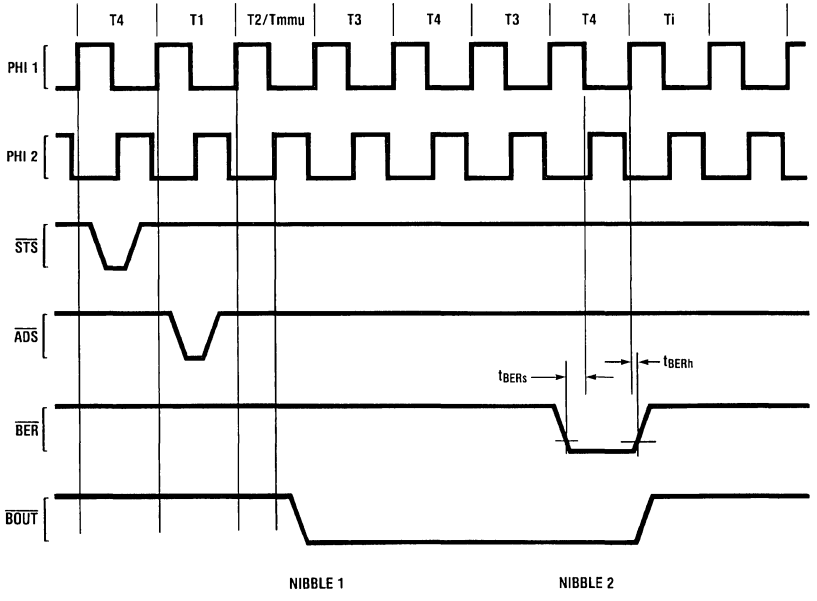

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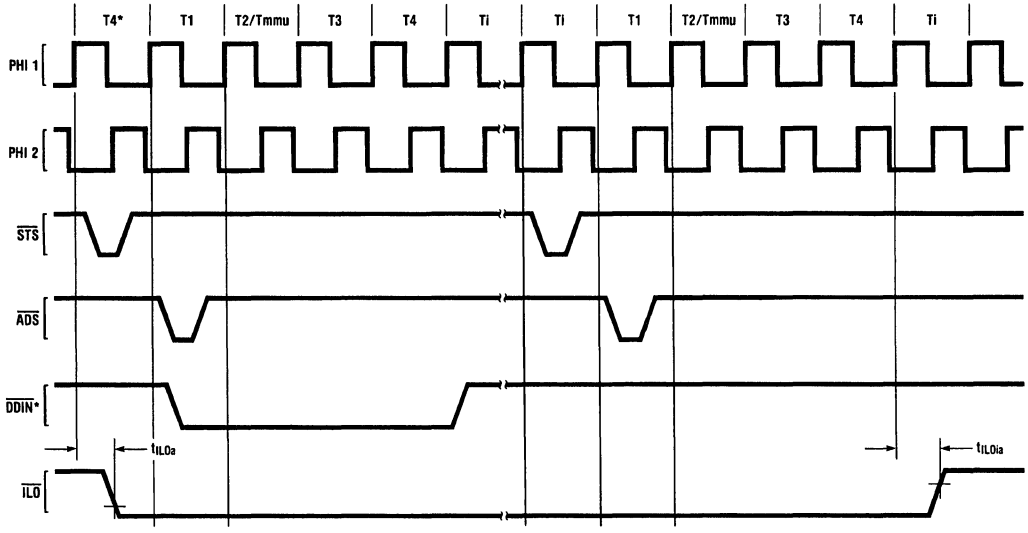
FIGURE 4-13. Bus Error During Burst Bus Cycle

4.0 Device Specifications (Continued)



*End of Dummy Read cycle with the address of the interlocked operand.

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FIGURE 4-14. Timing of Interlocked Bus Transactions

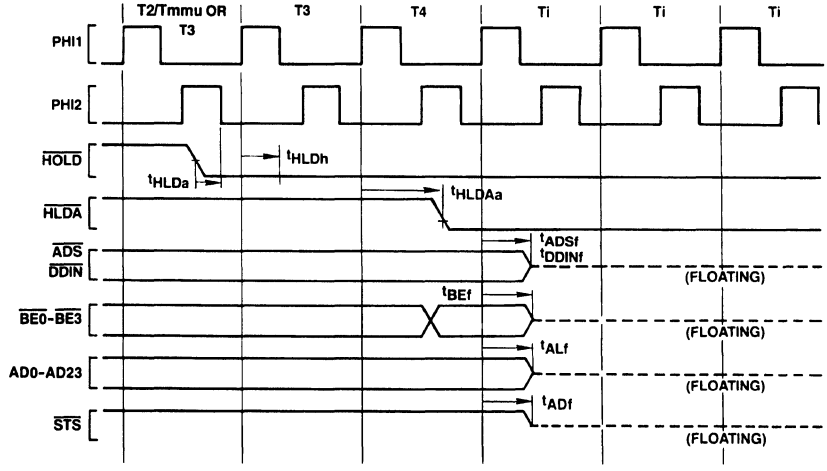

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FIGURE 4-15. Floating by $\overline{\text{HOLD}}$ Timing (CPU Not Idle Initially)

Note: Whenever the CPU is not idling (not in Ti), the $\overline{\text{HOLD}}$ signal must be active before the falling edge of PHI2 of the clock cycle that appears two clock cycles before T4 (TX1) and stay low until after the rising edge of PHI1 of the clock cycle that precedes T4 (TX2) for the request to be acknowledged.

4.0 Device Specifications (Continued)

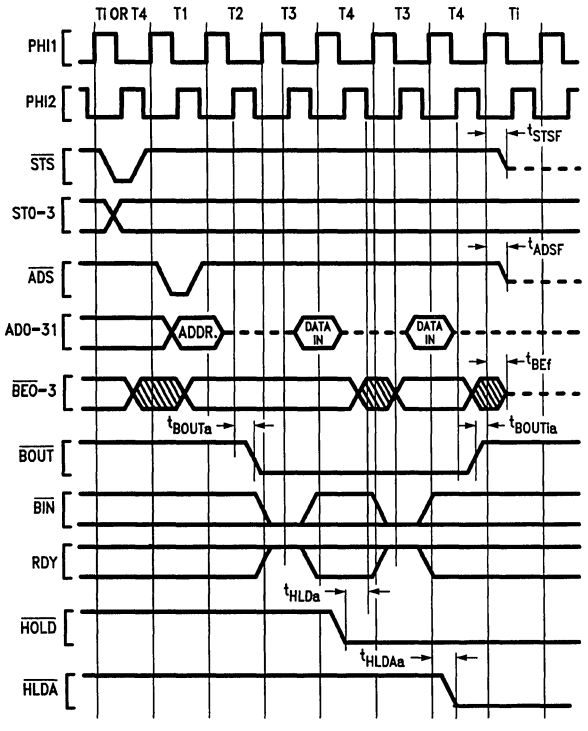

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FIGURE 4-16. Floating by $\overline{HOLD}$ Timing (Burst Cycle Ended by $\overline{HOLD}$ Assertion)

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4.0 Device Specifications (Continued)

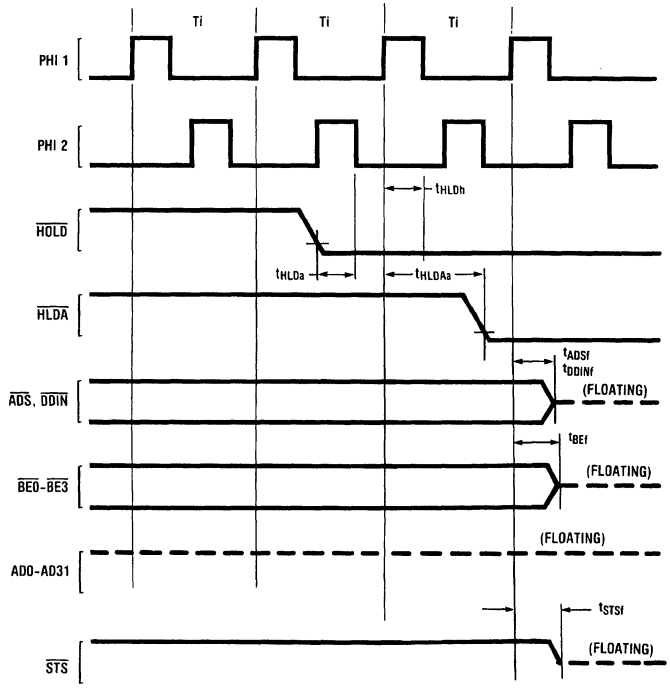

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FIGURE 4-17. Floating by $\overline{\text{HOLD}}$ Timing (CPU initially idle)

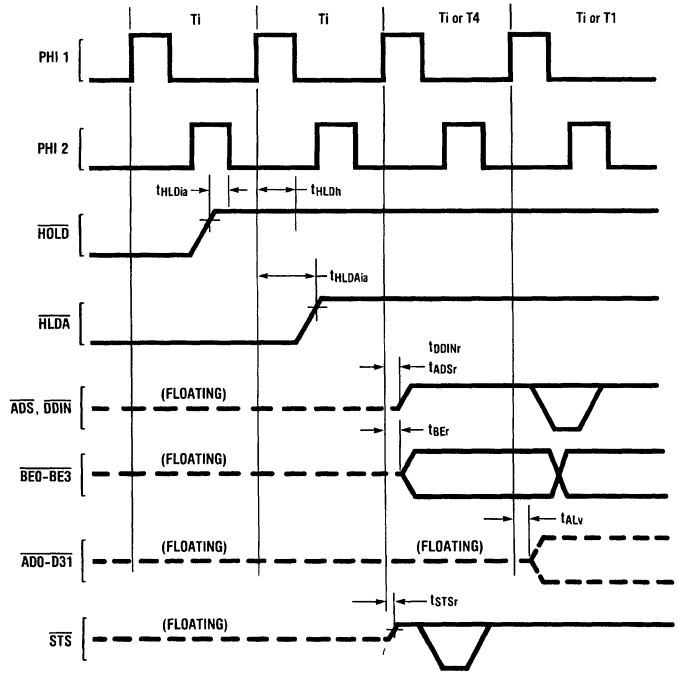

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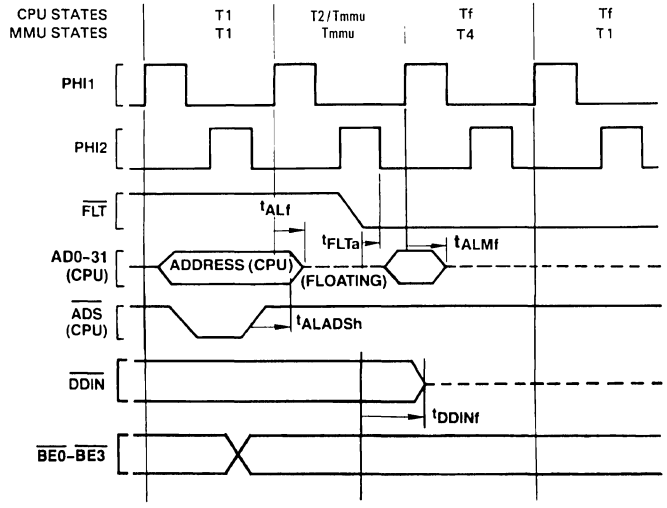
FIGURE 4-18. Release from $\overline{\text{HOLD}}$

4.0 Device Specifications (Continued)



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Note: The bus lines AD0–31 are temporarily driven in T2/TMMU and T_f when $\overline{FLT}$ is asserted only if $\overline{DT}/\overline{SDONE}$ is sampled low during reset (see Section 3.3).

FIGURE 4-19. $\overline{FLT}$ Initiated Cycle Timing

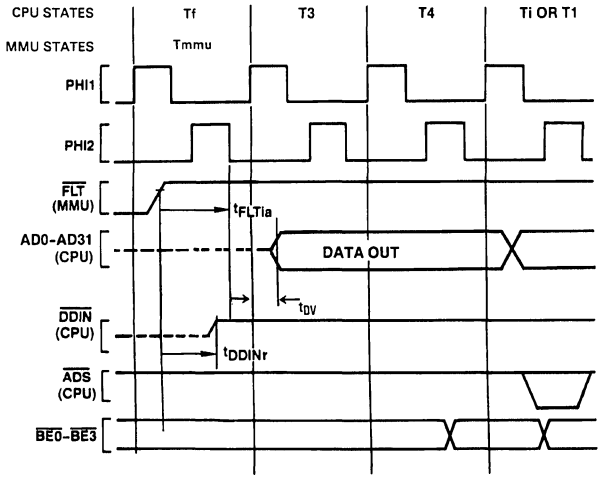

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FIGURE 4-20. Release from $\overline{FLT}$ Timing (CPU Write Cycle)

Note: When $\overline{FLT}$ is deasserted the CPU restarts driving $\overline{DDIN}$ before the MMU releases it. This, however, does not cause any conflict, since both CPU and MMU force $\overline{DDIN}$ to the same logic level.

4.0 Device Specifications (Continued)

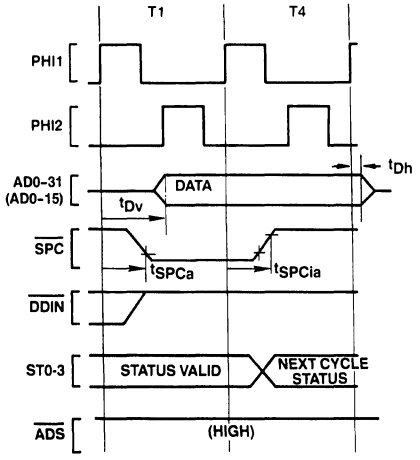

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FIGURE 4-21. Slave Processor Write Timing

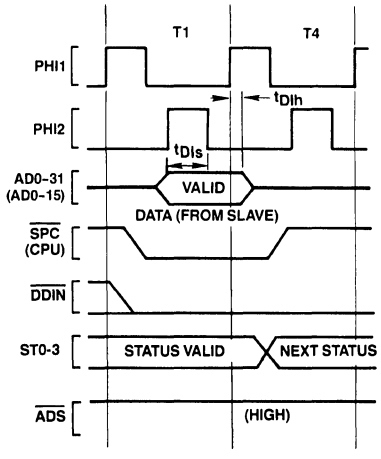

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FIGURE 4-22. Slave Processor Read Timing

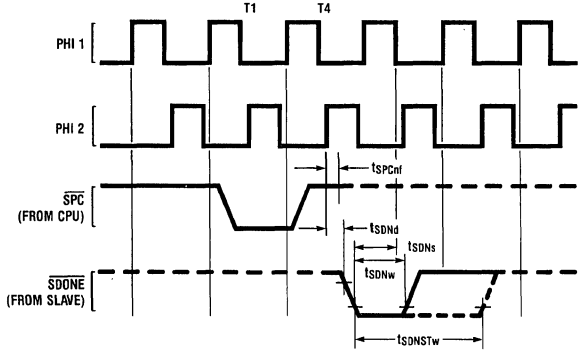

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FIGURE 4-23. $\overline{DT}/\overline{SDONE}$ Timing (32-Bit Slave Protocol)

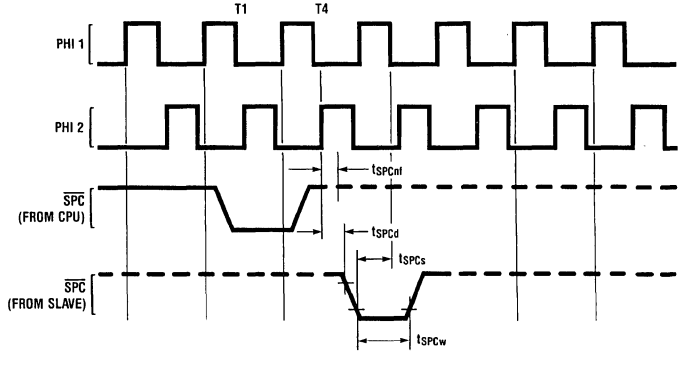

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FIGURE 4-24. $\overline{SPC}$ Timing (16-Bit Slave Protocol)

Note: After transferring last operand to a Slave Processor, CPU turns OFF driver and holds $\overline{SPC}$ high with internal 5 kΩ pullup.

4.0 Device Specifications (Continued)

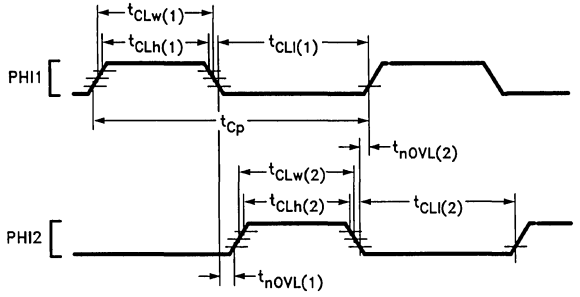

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FIGURE 4-25. Clock Waveforms

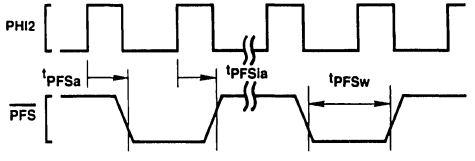

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FIGURE 4-26. Relationship of $\overline{PFS}$ to Clock Cycles

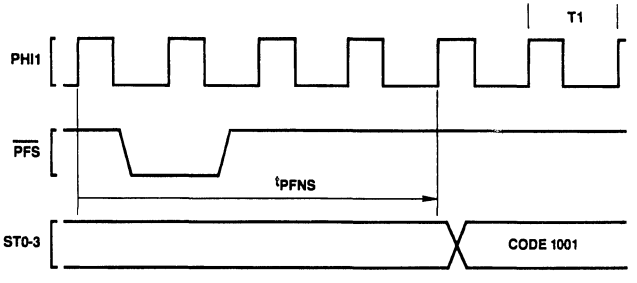

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FIGURE 4-27. Guaranteed Delay, $\overline{PFS}$ to Non-Sequential Fetch

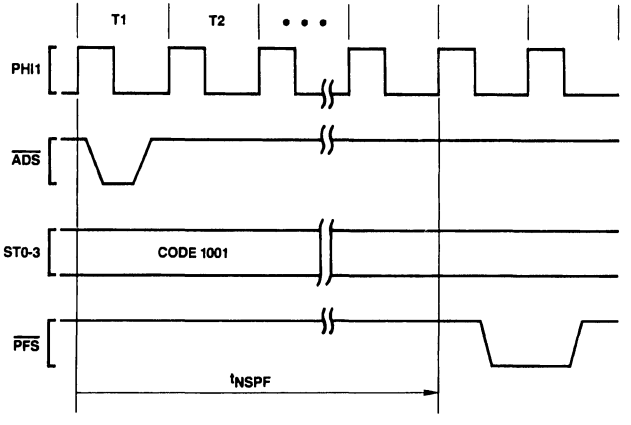

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FIGURE 4-28. Guaranteed Delay, Non-Sequential Fetch to $\overline{PFS}$

4.0 Device Specifications (Continued)

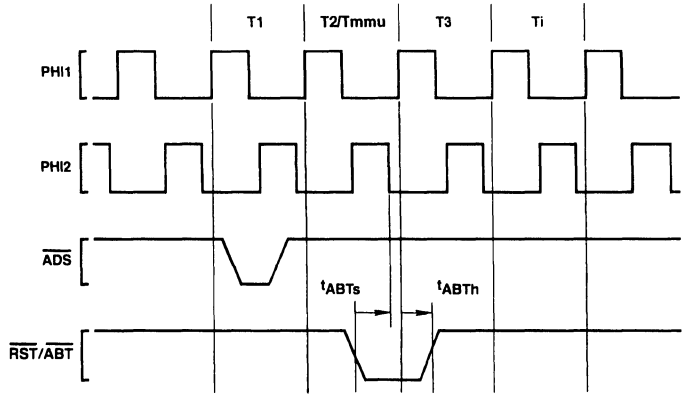

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FIGURE 4-29. Abort Timing, $\overline{FLT}$ Not Applied

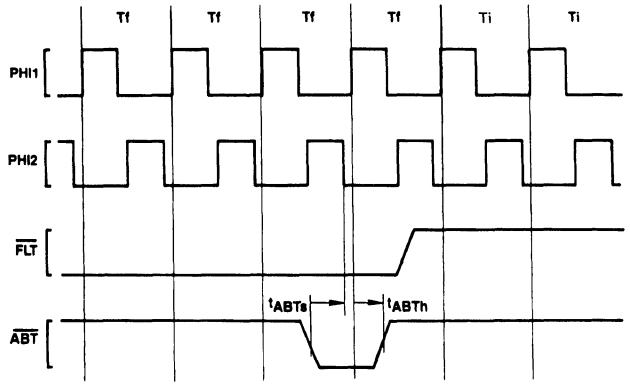

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FIGURE 4-30. Abort Timing, $\overline{FLT}$ Applied

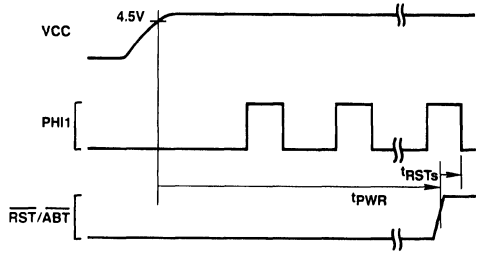

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FIGURE 4-31. Power-On Reset

4.0 Device Specifications (Continued)

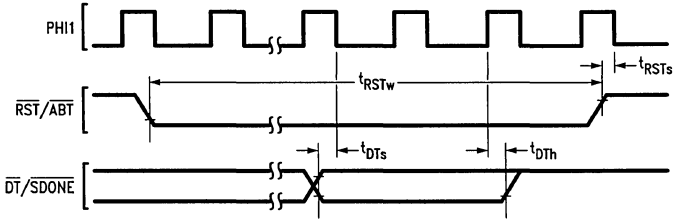

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FIGURE 4-32. Non-Power-On Reset

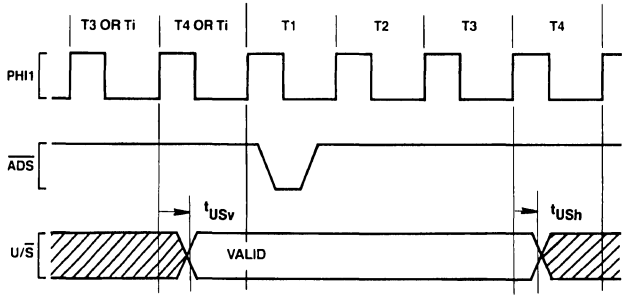

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FIGURE 4-33. U/$\overline{S}$ Relationship to Any Bus Cycle — Guaranteed Valid Interval

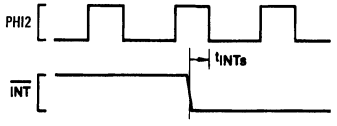

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FIGURE 4-34. $\overline{INT}$ Interrupt Signal Detection

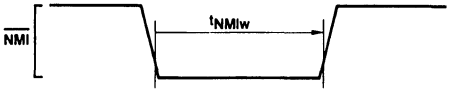

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FIGURE 4-35. $\overline{NMI}$ Interrupt Signal Timing

2

Appendix A: Instruction Formats

NOTATIONS

i= Integer Type Field
B = 00 (Byte)
W = 01 (Word)
D = 11 (Double Word)

f= Floating Point Type Field
F = 1 (Std. Floating: 32 bits)
L = 0 (Long Floating: 64 bits)

c= Custom Type Field
D = 1 (Double Word)
Q = 0 (Quad Word)

op= Operation Code
Valid encodings shown with each format.

gen, gen 1, gen 2= General Addressing Mode Field
See Sec. 2.2 for encodings.

reg= General Purpose Register Number

cond= Condition Code Field
0000 = EQual: Z = 1
0001 = Not Equal: Z = 0
0010 = Carry Set: C = 1
0011 = Carry Clear: C = 0
0100 = HIgher: L = 1
0101 = Lower or Same: L = 0
0110 = Greater Than: N = 1
0111 = Less or Equal: N = 0
1000 = Flag Set: F = 1
1001 = Flag Clear: F = 0
1010 = LOwer: L = 0 and Z = 0
1011 = Higher or Same: L = 1 or Z = 1
1100 = Less Than: N = 0 and Z = 0
1101 = Greater or Equal: N = 1 or Z = 1
1110 = (Unconditionally True)
1111 = (Unconditionally False)

short= Short Immediate value. May contain
quick: Signed 4-bit value, in MOVQ, ADDQ, CMPQ, ACB.
cond: Condition Code (above), in Scond.
areg: CPU Dedicated Register, in LPR, SPR.
0000 = US
0001 – 0111 = (Reserved)
1000 = FP
1001 = SP
1010 = SB
1011 = (Reserved)
1100 = (Reserved)
1101 = PSR
1110 = INTBASE
1111 = MOD
Options: in String Instructions

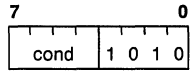
U/W	B	T

T = Translated
B = Backward
U/W = 00: None
01: While Match
11: Until Match

Configuration bits in SETCFG Instruction:

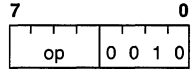
P	FC	FM	FF	C	M	F	I

mreg: NS32382 Register number, in LMR, SMR.
0000 = BAR
0001 = (Reserved)
0010 = BMR
0011 = BDR
0100 = (Reserved)
0101 = (Reserved)
0110 = BEAR
0111 = (Reserved)
1000 = (Reserved)
1001 = MCR
1010 = MSR
1011 = TEAR
1100 = PTB0
1101 = PTB1
1110 = IVAR0
1111 = IVAR1



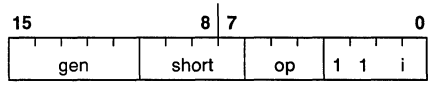
Format 0

Bcond (BR)



Format 1

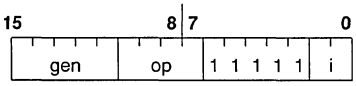
BSR	-0000	ENTER	-1000
RET	-0001	EXIT	-1001
CXP	-0010	NOP	-1010
RXP	-0011	WAIT	-1011
RETT	-0100	DIA	-1100
RETI	-0101	FLAG	-1101
SAVE	-0110	SVC	-1110
RESTORE	-0111	BPT	-1111



Format 2

ADDQ	-000	ACB	-100
CMPQ	-001	MOVQ	-101
SPR	-010	LPR	-110
Scond	-011		

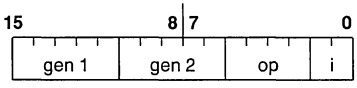
Appendix A: Instruction Formats (Continued)



Format 3

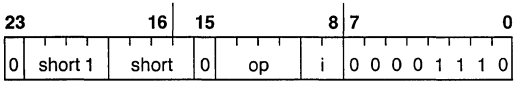
CXPD	-0000	ADJSP	-1010
BICPSR	-0010	JSR	-1100
JUMP	-0100	CASE	-1110
BISPSR	-0110		

Trap (UND) on XXX1, 1000



Format 4

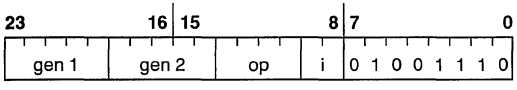
ADD	-0000	SUB	-1000
CMP	-0001	ADDR	-1001
BIC	-0010	AND	-1010
ADDC	-0100	SUBC	-1100
MOV	-0101	TBIT	-1101
OR	-0110	XOR	-1110



Format 5

MOVS	-0000	SETCFG*	-0010
CMPS	-0001	SKPS	-0011

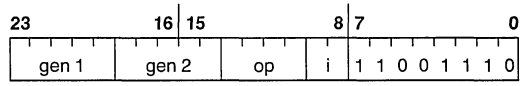
Trap (UND) on 1XXX, 01XX



Format 6

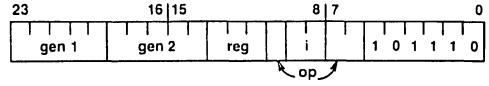
ROT	-0000	NEG	-1000
ASH	-0001	NOT	-1001
CBIT	-0010	Trap (UND)	-1010
CBITI	-0011	SUBP	-1011
Trap (UND)	-0100	ABS	-1100
LSH	-0101	COM	-1101
SBIT	-0110	IBIT	-1110
SBITI	-0111	ADDP	-1111

*Short 1 in format 5 applies only for SETCFG instruction. In other instructions this field is 0.



Format 7

MOVM	-0000	MUL	-1000
CMPM	-0001	MEI	-1001
INSS	-0010	Trap (UND)	-1010
EXTS	-0011	DEI	-1011
MOVXBW	-0100	QUO	-1100
MOVZBW	-0101	REM	-1101
MOVZiD	-0110	MOD	-1110
MOVXiD	-0111	DIV	-1111



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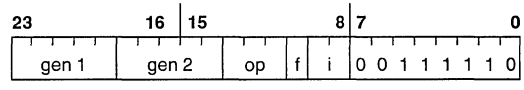
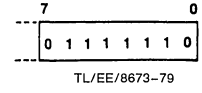
Format 8

EXT	-0 00	INDEX	-1 00
CVTP	-0 01	FFS	-1 01
INS	-0 10		
CHECK	-0 11		
MOVSU	-110, reg = 001		
MOVUS	-110, reg = 011		



Format 9

MOVif	-000	ROUND	-100
LFSR	-001	TRUNC	-101
MOVLF	-010	SFSR	-110
MOVFL	-011	FLOOR	-111



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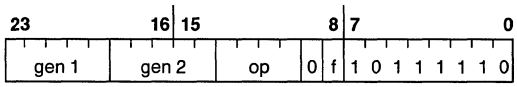
Format 10

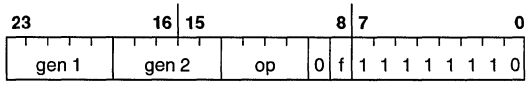
Trap (UND) Always

Appendix A: Instruction Formats (Continued)



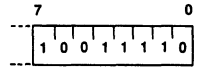
Format 11

ADDf	-0000	DIVf	-1000
MOVf	-0001	Note 1	-1001
CMPf	-0010	Trap (UND)	-1010
Note 3	-0011	Trap (UND)	-1011
SUBf	-0100	MULf	-1100
NEGf	-0101	ABSf	-1101
Trap (UND)	-0110	Trap (UND)	-1110
Trap (UND)	-0111	Trap (UND)	-1111



Format 12

Note 2	-0000	Note 2	-1000
Note 1	-0001	Note 1	-1001
POLYf	-0010	Trap (UND)	-1010
DOTf	-0011	Trap (UND)	-1011
SCALBf	-0100	Note 2	-1100
LOGBf	-0101	Note 1	-1101
Trap (UND)	-0110	Trap (UND)	-1110
Trap (UND)	-0111	Trap (UND)	-1111



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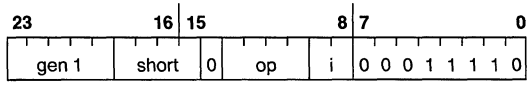
Format 13

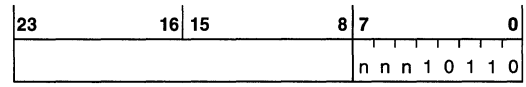
Trap (UND) Always



Format 14

RDVAL	-0000	LMR	-0010
WRVAL	-0001	SMR	-0011

Trap (UND) on 01XX, 1XXX

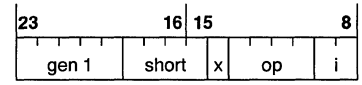


Operation Word ID Byte

Format 15

(Custom Slave)

nnn **Operation Word Format**

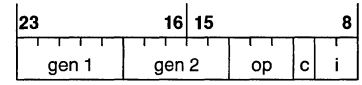


000

Format 15.0

CATST0	-0000	LCR	-0010
CATST1	-0001	SCR	-0011

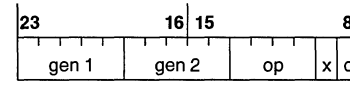
Trap (UND) on all others



001

Format 15.1

CCV3	-000	CCV2	-100
LCSR	-001	CCV1	-101
CCV5	-010	SCSR	-110
CCV4	-011	CCV0	-111

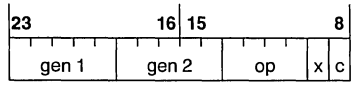


101

Format 15.5

CCAL0	-0000	CCAL3	-1000
CMOV0	-0001	CMOV3	-1001
CCMP0	-0010	Trap (UND)	-1010
CCMP1	-0011	Trap (UND)	-1011
CCAL1	-0100	CCAL2	-1100
CMOV2	-0101	CMOV1	-1101
Trap (UND)	-0110	Trap (UND)	-1110
Trap (UND)	-0111	Trap (UND)	-1111

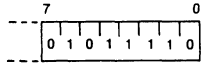
Appendix A: Instruction Formats (Continued)



Format 15.7

Note 2	-0000	Note 2	-1000
Note 1	-0001	Note 1	-1001
Note 3	-0010	Trap (UND)	-1010
Note 3	-0011	Trap (UND)	-1011
Note 2	-0100	Note 2	-1100
Note 1	-0101	Note 1	-1101
Trap (UND)	-0110	Trap (UND)	-1110
Trap (UND)	-0111	Trap (UND)	-1111

If nnn = 010, 011, 100, 110 then Trap (UND) Always.



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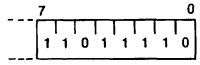
Format 16

Trap (UND) Always



TL/EE/8673-83

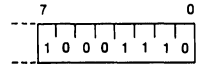
Note 1: Opcode not defined; CPU treats like MOV_f or $CMOV_c$. First operand has access class of read; second operand has access class of write; f or c field selects 32- or 64-bit data.

Note 2: Opcode not defined; CPU treats like ADD_f or $CCAL_c$. First operand has access class of read; second operand has access class of read-modify-write; f or c field selects 32- or 64-bit data.

Note 3: Opcode not defined; CPU treats like CMP_f or $CCMP_c$. First operand has access class of read; second operand has access class of read; f or c field selects 32- or 64-bit data.

Format 17

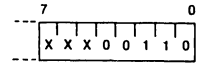
Trap (UND) Always



TL/EE/8673-84

Format 18

Trap (UND) Always

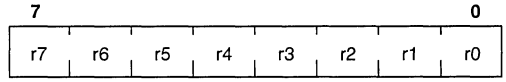


TL/EE/8673-85

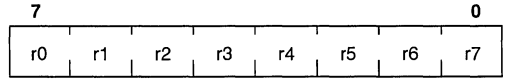
Format 19

Trap (UND) Always

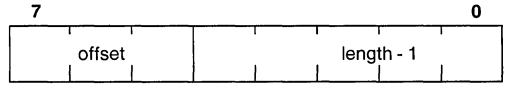
Implied Immediate Encodings:



Register Mark, appended to SAVE, ENTER



Register Mark, appended to RESTORE, EXIT



Offset/Length Modifier appended to INSS, EXTS

2

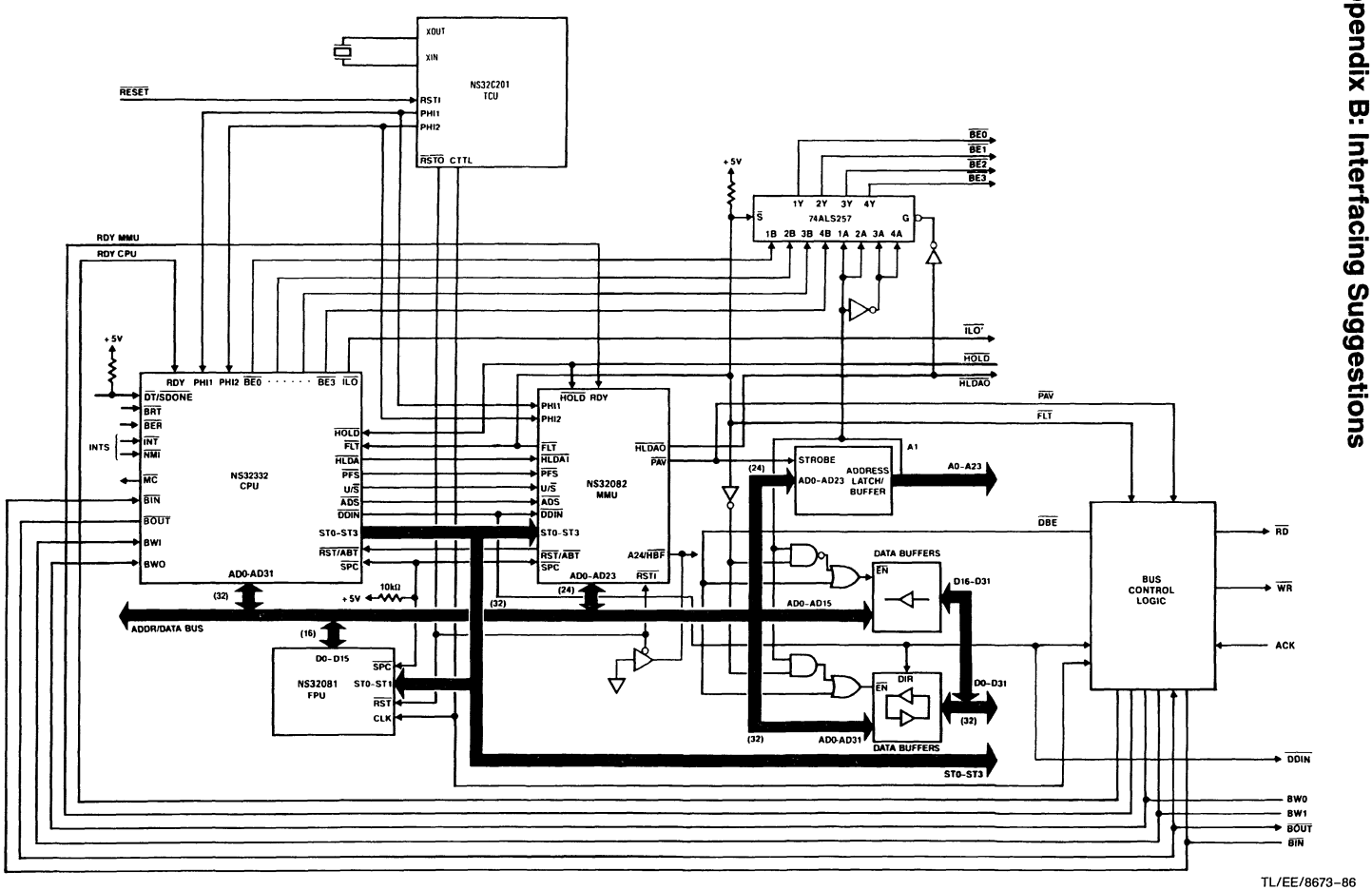


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FIGURE B-1. System Connection Diagram (32332, 32081 & 32082)

Appendix B: Interfacing Suggestions (Continued)

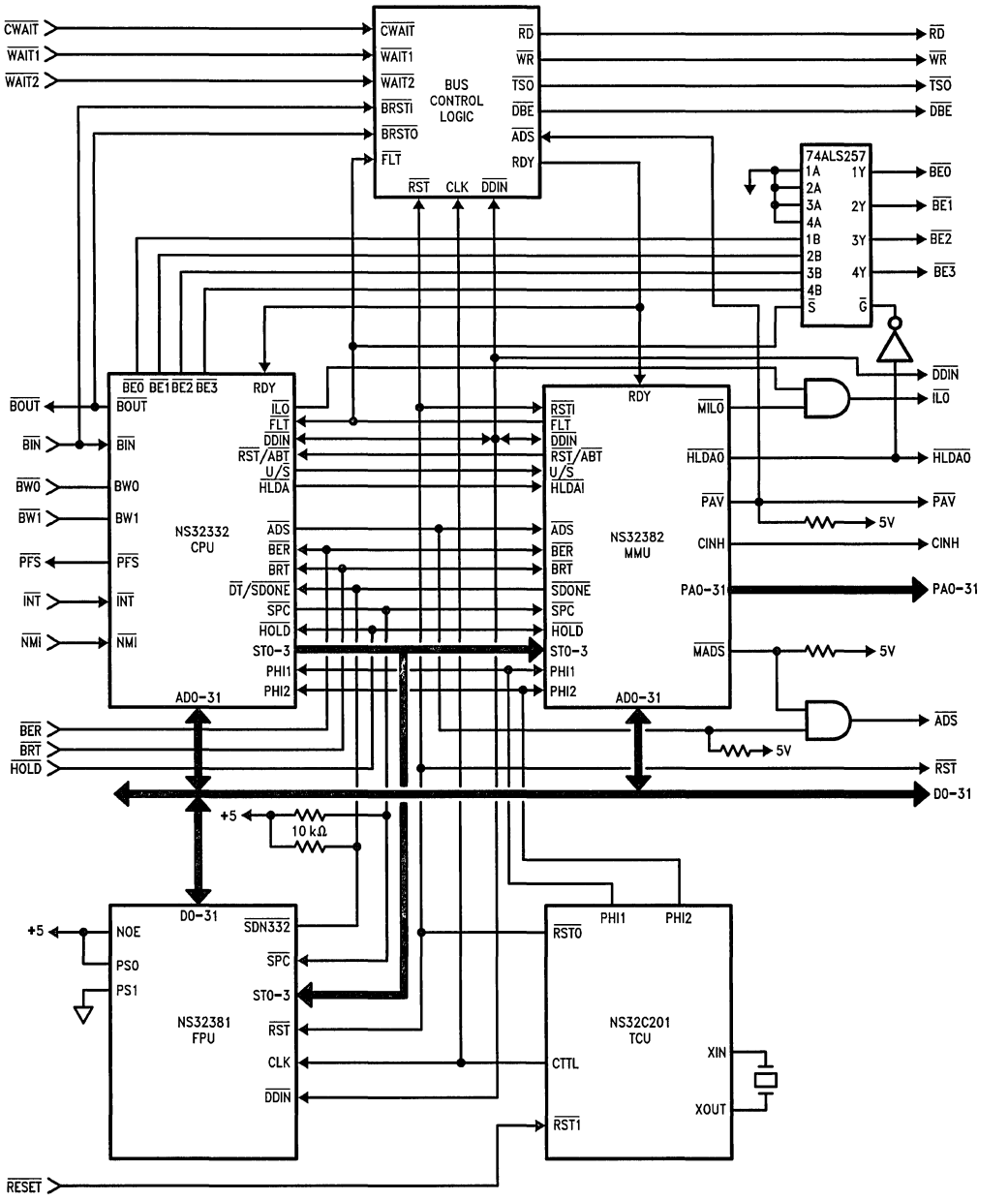

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FIGURE B-2. System Connection Diagram (32332, 32381 & 32382)

National Semiconductor

NS32C032-10/NS32C032-15 High-Performance Microprocessors

General Description

The NS32C032 is a 32-bit, virtual memory microprocessor with a 16-MByte linear address space and a 32-bit external data bus. It has a 32-bit ALU, eight 32-bit general purpose registers, an eight-byte prefetch queue, and a slave processor interface. The NS32C032 is fabricated with National Semiconductor's advanced CMOS process, and is fully object code compatible with other Series 32000® processors. The Series 32000 instruction set is optimized for modular, high-level languages (HLL). The set is very symmetric, it has a two address format, and it incorporates HLL oriented addressing modes. The capabilities of the NS32C032 can be expanded with the use of the NS32081 floating point unit (FPU), and the NS32082 demand-paged virtual memory management unit (MMU). Both devices interface to the NS32C032 as slave processors. The NS32C032 is a general purpose microprocessor that is ideal for a wide range of computational intensive applications.

Features

- 32-bit architecture and implementation
- Virtual memory support
- 16-MByte linear address space
- 32-bit data bus
- Powerful instruction set
  - — General 2-address capability
  - — Very high degree of symmetry
  - — Addressing modes optimized for high-level languages
- Series 32000 slave processor support
- High-speed CMOS technology
- 68-pin leadless chip carrier

Block Diagram

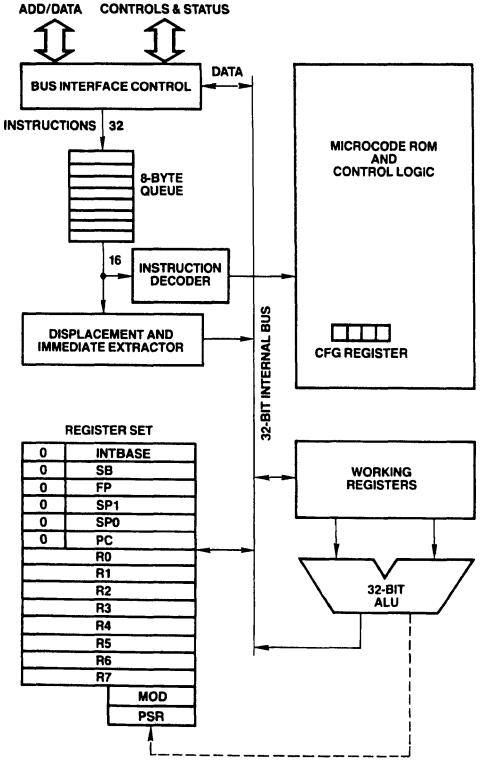

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FIGURE 1

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List of Illustrations

List of Illustrations (Continued)

List of Tables

1.0 Product Introduction

The Series 32000 microprocessor family is a new generation of devices using National's XMOS and CMOS technologies. By combining state-of-the-art MOS technology with a very advanced architectural design philosophy, this family brings mainframe computer processing power to VLSI processors.

The Series 32000 family supports a variety of system configurations, extending from a minimum low-cost system to a powerful 4 gigabyte system. The architecture provides complete upward compatibility from one family member to another. The family consists of a selection of CPUs supported by a set of peripherals and slave processors that provide sophisticated interrupt and memory management facilities as well as high-speed floating-point operations. The architectural features of the Series 32000 family are described briefly below:

Powerful Addressing Modes. Nine addressing modes available to all instructions are included to access data structures efficiently.

Data Types. The architecture provides for numerous data types, such as byte, word, doubleword, and BCD, which may be arranged into a wide variety of data structures.

Symmetric Instruction Set. While avoiding special case instructions that compilers can't use, the Series 32000 family incorporates powerful instructions for control operations, such as array indexing and external procedure calls, which save considerable space and time for compiled code.

Memory-to-Memory Operations. The Series 32000 CPUs represent two-address machines. This means that each operand can be referenced by any one of the addressing modes provided. This powerful memory-to-memory architecture permits memory locations to be treated as registers for all useful operations. This is important for temporary operands as well as for context switching.

Memory Management. Either the NS32382 or the NS32082 Memory Management Unit may be added to the system to provide advanced operating system support functions, including dynamic address translation, virtual memory management, and memory protection.

Large, Uniform Addressing. The NS32C032 has 24-bit address pointers that can address up to 16 megabytes without requiring any segmentation; this addressing scheme provides flexible memory management without added-on expense.

Modular Software Support. Any software package for the Series 32000 family can be developed independent of all other packages, without regard to individual addressing. In addition, ROM code is totally relocatable and easy to access, which allows a significant reduction in hardware and software cost.

Software Processor Concept. The Series 32000 architecture allows future expansions of the instruction set that can be executed by special slave processors, acting as extensions to the CPU. This concept of slave processors is unique to the Series 32000 family. It allows software compatibility even for future components because the slave hardware is transparent to the software. With future advances in semiconductor technology, the slaves can be physically integrated on the CPU chip itself.

To summarize, the architectural features cited above provide three primary performance advantages and characteristics:

- High-Level Language Support
- Easy Future Growth Path
- Application Flexibility

2.0 Architectural Description

2.1 PROGRAMMING MODEL

The Series 32000 architecture includes 16 registers on the NS32C032 CPU.

2.1.1 General Purpose Registers

There are eight registers for meeting high speed general storage requirements, such as holding temporary variables and addresses. The general purpose registers are free for any use by the programmer. They are thirty-two bits in length. If a general register is specified for an operand that is eight or sixteen bits long, only the low part of the register is used; the high part is not referenced or modified.

2.1.2 Dedicated Registers

The eight dedicated registers of the NS32C032 are assigned specific functions.

PC: The PROGRAM COUNTER register is a pointer to the first byte of the instruction currently being executed. The PC is used to reference memory in the program section. (In the NS32C032 the upper eight bits of this register are always zero.)

SP0, SP1: The SP0 register points to the lowest address of the last item stored on the INTERRUPT STACK. This stack is normally used only by the operating system. It is used primarily for storing temporary data, and holding return information for operating system subroutines and interrupt and trap service routines. The SP1 register points to the lowest address of the last item stored on the USER STACK. This stack is used by normal user programs to hold temporary data and subroutine return information.

In this document, reference is made to the SP register. The terms "SP register" or "SP" refer to either SP0 or SP1, depending on the setting of the S bit in the PSR register. If the S bit in the PSR is 0 the SP refers to SP0. If the S bit in the PSR is 1 then SP refers to SP1. (In the NS32C032 the upper eight bits of these registers are always zero).

Stacks in the Series 32000 family grow downward in memory. A Push operation pre-decrements the Stack Pointer by the operand length. A Pop operation post-increments the Stack Pointer by the operand length.

FP: The FRAME POINTER register is used by a procedure to access parameters and local variables on the stack. The FP register is set up on procedure entry with the ENTER instruction and restored on procedure termination with the EXIT instruction.

The frame pointer holds the address in memory occupied by the old contents of the frame pointer. (In the NS32C032 the upper eight bits of this register are always zero.)

SB: The STATIC BASE register points to the global variables of a software module. This register is used to support relocatable global variables for software modules.

2.0 Architectural Description (Continued)

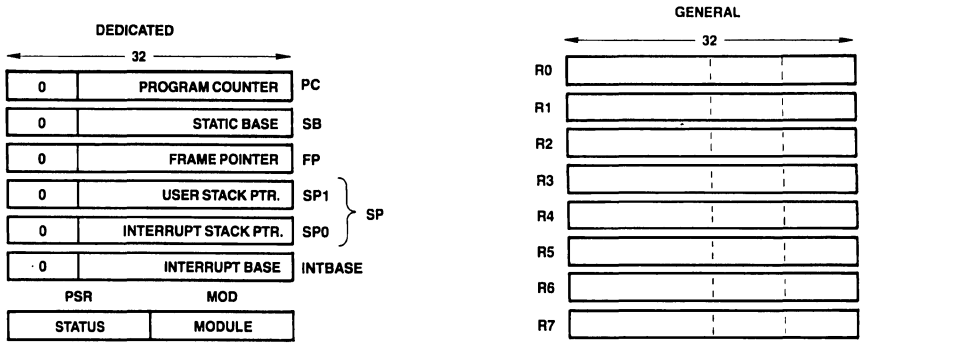

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FIGURE 2-1. The General and Dedicated Registers

The SB register holds the lowest address in memory occupied by the global variables of a module. (In the NS32C032 the upper eight bits of this register are always zero.)

INTBASE: The INTERRUPT BASE register holds the address of the dispatch table for interrupts and traps (Sec. 3.8). The INTBASE register holds the lowest address in memory occupied by the dispatch table. (In the NS32C032 the upper eight bits of this register are always zero.)

MOD: The MODULE register holds the address of the module descriptor of the currently executing software module. The MOD register is sixteen bits long, therefore the module table must be contained within the first 64K bytes of memory.

PSR: The PROCESSOR STATUS REGISTER (PSR) holds the status codes for the NS32C032 microprocessor.

The PSR is sixteen bits long, divided into two eight-bit halves. The low order eight bits are accessible to all programs, but the high order eight bits are accessible only to programs executing in Supervisor Mode.

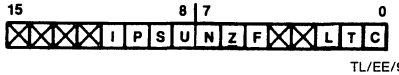

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FIGURE 2-2. Processor Status Register

C: The C bit indicates that a carry or borrow occurred after an addition or subtraction instruction. It can be used with the ADDC and SUBC instructions to perform multiple-precision integer arithmetic calculations. It may have a setting of 0 (no carry or borrow) or 1 (carry or borrow).

T: The T bit causes program tracing. If this bit is a 1, a TRC trap is executed after every instruction (Sec. 3.8.5).

L: The L bit is altered by comparison instructions. In a comparison instruction the L bit is set to "1" if the second operand is less than the first operand, when both operands are interpreted as unsigned integers. Otherwise, it is set to "0". In Floating Point comparisons, this bit is always cleared.

F: The F bit is a general condition flag, which is altered by many instructions (e.g., integer arithmetic instructions use it to indicate overflow).

Z: The Z bit is altered by comparison instructions. In a comparison instruction the Z bit is set to "1" if the second operand is equal to the first operand; otherwise it is set to "0".

N: The N bit is altered by comparison instructions. In a comparison instruction the N bit is set to "1" if the second operand is less than the first operand, when both operands are interpreted as signed integers. Otherwise, it is set to "0".

U: If the U bit is "1" no privileged instructions may be executed. If the U bit is "0" then all instructions may be executed. When U = 0 the NS32C032 is said to be in Supervisor Mode; when U = 1 the NS32C032 is said to be in User Mode. A User Mode program is restricted from executing certain instructions and accessing certain registers which could interfere with the operating system. For example, a User Mode program is prevented from changing the setting of the flag used to indicate its own privilege mode. A Supervisor Mode program is assumed to be a trusted part of the operating system, hence it has no such restrictions.

S: The S bit specifies whether the SP0 register or SP1 register is used as the stack pointer. The bit is automatically cleared on interrupts and traps. It may have a setting of 0 (use the SP0 register) or 1 (use the SP1 register).

P: The P bit prevents a TRC trap from occurring more than once for an instruction (Sec. 3.8.5.). It may have a setting of 0 (no trace pending) or 1 (trace pending).

I: If I = 1, then all interrupts will be accepted (Sec. 3.8.). If I = 0, only the NMI interrupt is accepted. Trap enables are not affected by this bit.

2.1.3 The Configuration Register (CFG)

Within the Control section of the NS32C032 CPU is the four-bit CFG Register, which declares the presence of certain external devices. It is referenced by only one instruction, SETCFG, which is intended to be executed only as part of system initialization after reset. The format of the CFG Register is shown in *Figure 2-3*.

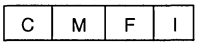


FIGURE 2-3. CFG Register

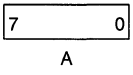
2.0 Architectural Description (Continued)

The CFG I bit declares the presence of external interrupt vectoring circuitry (specifically, the NS32202 Interrupt Control Unit). If the CFG I bit is set, interrupts requested through the $\overline{INT}$ pin are "Vectored." If it is clear, these interrupts are "Non-Vectored." See Sec. 3.8.

The F, M and C bits declare the presence of the FPU, MMU and Custom Slave Processors. If these bits are not set, the corresponding instructions are trapped as being undefined.

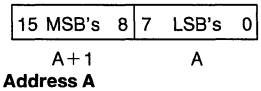
2.1.4 Memory Organization

The main memory of the NS32C032 is a uniform linear address space. Memory locations are numbered sequentially starting at zero and ending at $2^{24} - 1$. The number specifying a memory location is called an address. The contents of each memory location is a byte consisting of eight bits. Unless otherwise noted, diagrams in this document show data stored in memory with the lowest address on the right and the highest address on the left. Also, when data is shown vertically, the lowest address is at the top of a diagram and the highest address at the bottom of the diagram. When bits are numbered in a diagram, the least significant bit is given the number zero, and is shown at the right of the diagram. Bits are numbered in increasing significance and toward the left.



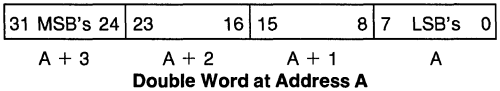
Byte at Address A

Two contiguous bytes are called a word. Except where noted (Sec. 2.2.1), the least significant byte of a word is stored at the lower address, and the most significant byte of the word is stored at the next higher address. In memory, the address of a word is the address of its least significant byte, and a word may start at any address.



Word at Address A

Two contiguous words are called a double word. Except where noted (Sec. 2.2.1), the least significant word of a double word is stored at the lowest address and the most significant word of the double word is stored at the address two greater. In memory, the address of a double word is the address of its least significant byte, and a double word may start at any address.



Double Word at Address A

Although memory is addressed as bytes, it is actually organized as double-words. Note that access time to a word or a double-word depends upon its address, e.g. double-words that are aligned to start at addresses that are multiples of four will be accessed more quickly than those not so aligned. This also applies to words that cross a double-word boundary.

2.1.5 Dedicated Tables

Two of the NS32C032 dedicated registers (MOD and INTBASE) serve as pointers to dedicated tables in memory.

The INTBASE register points to the Interrupt Dispatch and Cascade tables. These are described in Sec. 3.8.

The MOD register contains a pointer into the Module Table, whose entries are called Module Descriptors. A Module Descriptor contains four pointers, three of which are used by NS32C032. The MOD register contains the address of the Module Descriptor for the currently running module. It is automatically up-dated by the Call External Procedure instructions (CXP and CXPD).

The format of a Module Descriptor is shown in *Figure 2-4*. The Static Base entry contains the address of static data assigned to the running module. It is loaded into the CPU Static Base register by the CXP and CXPD instructions. The Program Base entry contains the address of the first byte of instruction code in the module. Since a module may have multiple entry points, the Program Base pointer serves only as a reference to find them.

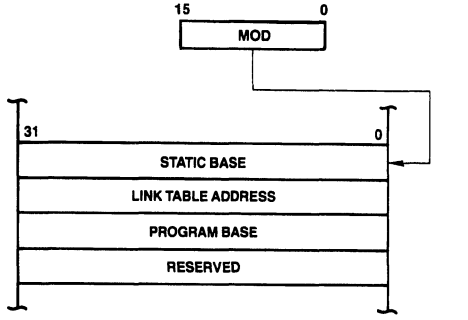


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FIGURE 2-4. Module Descriptor Format

The Link Table Address points to the Link Table for the currently running module. The Link Table provides the information needed for:

1) Sharing variables between modules. Such variables are accessed through the Link Table via the External addressing mode.
2) Transferring control from one module to another. This is done via the Call External Procedure (CXP) instruction.

The format of a Link Table is given in *Figure 2-5*. A Link Table Entry for an external variable contains the 32-bit address of that variable. An entry for an external procedure contains two 16-bit fields: Module and Offset. The Module field contains the new MOD register contents for the module being entered. The Offset field is an unsigned number giving the position of the entry point relative to the new module's Program Base pointer.

For further details of the functions of these tables, see the Series 32000 Instruction Set Reference Manual.

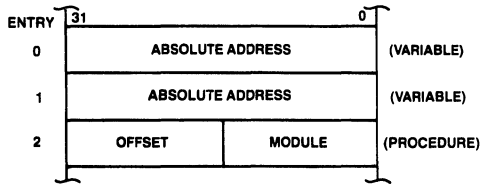

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FIGURE 2-5. A Sample Link Table

2.0 Architectural Description (Continued)

2.2 INSTRUCTION SET

2.2.1 General Instruction Format

Figure 2-6 shows the general format of a Series 32000 instruction. The Basic Instruction is one to three bytes long and contains the Opcode and up to two 5-bit General Addressing Mode ("Gen") fields. Following the Basic Instruction field is a set of optional extensions, which may appear depending on the instruction and the addressing modes selected.

Index Bytes appear when either or both Gen fields specify Scaled Index. In this case, the Gen field specifies only the Scale Factor (1, 2, 4 or 8), and the Index Byte specifies which General Purpose Register to use as the index, and which addressing mode calculation to perform before indexing. See *Figure 2-7*.

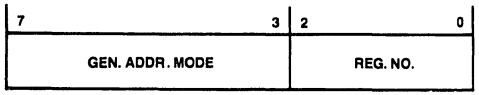

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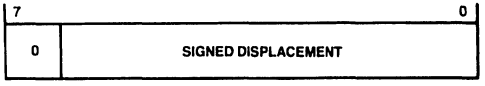
FIGURE 2-7. Index Byte Format

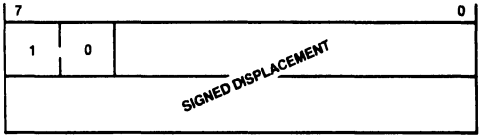
Following Index Bytes come any displacements (addressing constants) or immediate values associated with the selected address modes. Each Disp/Imm field may contain one or two displacements, or one immediate value. The size of a Displacement field is encoded with the top bits of that field, as shown in *Figure 2-8*, with the remaining bits interpreted as a signed (two's complement) value. The size of an immediate value is determined from the Opcode field. Both Displacement and Immediate fields are stored most significant byte first. Note that this is different from the memory representation of data (Sec. 2.1.4).

Some instructions require additional, "implied" immediates and/or displacements, apart from those associated with addressing modes. Any such extensions appear at the end of the instruction, in the order that they appear within the list of operands in the instruction definition (Sec. 2.2.3).

Byte Displacement: Range −64 to +63



Word Displacement: Range −8192 to +8191



Double Word Displacement: Range (Entire Addressing Space)

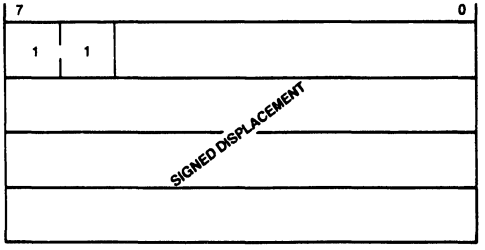


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FIGURE 2-8. Displacement Encodings

2.2.2 Addressing Modes

The NS32C032 CPU generally accesses an operand by calculating its Effective Address based on information available when the operand is to be accessed. The method to be used in performing this calculation is specified by the programmer as an "addressing mode."

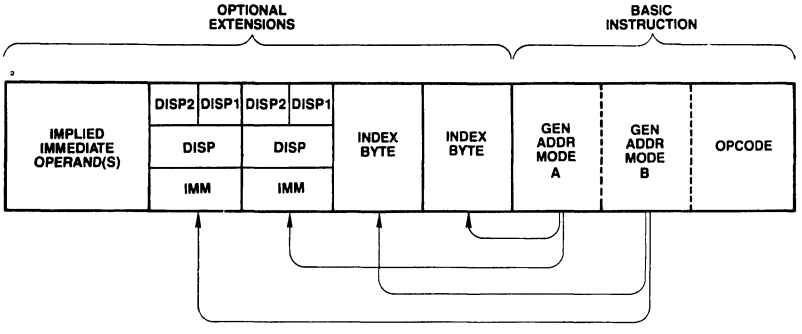

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FIGURE 2-6. General Instruction Format

2.0 Architectural Description (Continued)

Addressing modes in the NS32C032 are designed to optimally support high-level language accesses to variables. In nearly all cases, a variable access requires only one addressing mode, within the instruction that acts upon that variable. Extraneous data movement is therefore minimized.

NS32C032 Addressing Modes fall into nine basic types:

Register: The operand is available in one of the eight General Purpose Registers. In certain Slave Processor instructions, an auxiliary set of eight registers may be referenced instead.

Register Relative: A General Purpose Register contains an address to which is added a displacement value from the instruction, yielding the Effective Address of the operand in memory.

Memory Space. Identical to Register Relative above, except that the register used is one of the dedicated registers PC, SP, SB or FP. These registers point to data areas generally needed by high-level languages.

Memory Relative: A pointer variable is found within the memory space pointed to by the SP, SB or FP register. A displacement is added to that pointer to generate the Effective Address of the operand.

Immediate: The operand is encoded within the instruction. This addressing mode is not allowed if the operand is to be written.

Absolute: The address of the operand is specified by a displacement field in the instruction.

External: A pointer value is read from a specified entry of the current Link Table. To this pointer value is added a displacement, yielding the Effective Address of the operand.

Top of Stack: The currently-selected Stack Pointer (SP0 or SP1) specifies the location of the operand. The operand is pushed or popped, depending on whether it is written or read.

Scaled Index: Although encoded as an addressing mode. Scaled Indexing is an option on any addressing mode except Immediate or another Scaled Index. It has the effect of calculating an Effective Address, then multiplying any General Purpose Register by 1, 2, 4 or 8 and adding it into the total, yielding the final Effective Address of the operand.

Table 2-1 is a brief summary of the addressing modes. For a complete description of their actions, see the Instruction Set Reference Manual.

2.2.3 Instruction Set Summary

Table 2-2 presents a brief description of the NS32C032 instruction set. The Format column refers to the Instruction Format tables (Appendix A). The Instruction column gives the instruction as coded in assembly language, and the Description column provides a short description of the function provided by that instruction. Further details of the exact operations performed by each instruction may be found in the Instruction Set Reference Manual.

Notations:

i = Integer length suffix: B = Byte
W = Word
D = Double Word

f = Floating Point length suffix: F = Standard Floating
L = Long Floating

gen = General operand. Any addressing mode can be specified.

short = A 4-bit value encoded within the Basic Instruction (see Appendix A for encodings).

imm = Implied immediate operand. An 8-bit value appended after any addressing extensions.

disp = Displacement (addressing constant): 8, 16 or 32 bits. All three lengths legal.

reg = Any General Purpose Register: R0–R7.

areg = Any Dedicated/Address Register: SP, SB, FP, MOD, INTBASE, PSR, US (bottom 8 PSR bits).

mreg = Any Memory Management Status/Control Register.

creg = A Custom Slave Processor Register (Implementation Dependent).

cond = Any condition code, encoded as a 4-bit field within the Basic Instruction (see Appendix A for encodings).

2.0 Architectural Description (Continued)

TABLE 2-1
NS32C032 Addressing Modes

ENCODING	MODE	ASSEMBLER SYNTAX	EFFECTIVE ADDRESS
Register			
00000	Register 0	R0 or F0	None: Operand is in the specified register
00001	Register 1	R1 or F1	
00010	Register 2	R2 or F2	
00011	Register 3	R3 or F3	
00100	Register 4	R4 or F4	
00101	Register 5	R5 or F5	
00110	Register 6	R6 or F6	
00111	Register 7	R7 or F7	
Register Relative			
01000	Register 0 relative	disp(R0)	Disp + Register.
01001	Register 1 relative	disp(R1)	
01010	Register 2 relative	disp(R2)	
01011	Register 3 relative	disp(R3)	
01100	Register 4 relative	disp(R4)	
01101	Register 5 relative	disp(R5)	
01110	Register 6 relative	disp(R6)	
01111	Register 7 relative	disp(R7)	
Memory Relative			
10000	Frame memory relative	disp2(disp1(FP))	Disp2 + Pointer; Pointer found at address Disp1 + Register. "SP" is either SP0 or SP1, as selected in PSR.
10001	Stack memory relative	disp2(disp1(SP))	
10010	Static memory relative	disp2(disp1(SB))	
Reserved			
10011	(Reserved for Future Use)		
Immediate			
10100	Immediate	value	None: Operand is input from instruction queue.
Absolute			
10101	Absolute	@disp	Disp.
External			
10110	External	EXT (disp1) + disp2	Disp2 + Pointer; Pointer is found at Link Table Entry number Disp1.
Top of Stack			
10111	Top of stack	TOS	Top of current stack, using either User or Interrupt Stack Pointer, as selected in PSR. Automatic Push/Pop included.
Memory Space			
11000	Frame memory	disp(FP)	Disp + Register; "SP" is either SP0 or SP1, as selected in PSR.
11001	Stack memory	disp(SP)	
11010	Static memory	disp(SB)	
11011	Program memory	* + disp	
Scaled Index			
11100	Index, bytes	mode[Rn:B]	EA (mode) + Rn.
11101	Index, words	mode[Rn:W]	EA (mode) + 2× Rn.
11110	Index, double words	mode[Rn:D]	EA (mode) + 4× Rn.
11111	Index, quad words	mode[Rn:Q]	EA (mode) + 8 × Rn. 'Mode' and 'n' are contained within the Index Byte. EA (mode) denotes the effective address generated using mode.

2.0 Architectural Description (Continued)

TABLE 2-2
NS32C032 Instruction Set Summary

MOVES

Format	Operation	Operands	Description
4	MOVi	gen,gen	Move a value.
2	MOVQi	short,gen	Extend and move a signed 4-bit constant.
7	MOVMi	gen,gen,disp	Move Multiple: disp bytes (1 to 16).
7	MOVZBW	gen,gen	Move with zero extension.
7	MOVZiD	gen,gen	Move with zero extension.
7	MOVXBW	gen,gen	Move with sign extension.
7	MOVXiD	gen,gen	Move with sign extension.
4	ADDR	gen,gen	Move Effective Address.

INTEGER ARITHMETIC

Format	Operation	Operands	Description
4	ADDI	gen,gen	Add.
2	ADDQi	short,gen	Add signed 4-bit constant.
4	ADDCi	gen,gen	Add with carry.
4	SUBi	gen,gen	Subtract.
4	SUBCi	gen,gen	Subtract with carry (borrow).
6	NEGi	gen,gen	Negate (2's complement).
6	ABSi	gen,gen	Take absolute value.
7	MULi	gen,gen	Multiply
7	QUOi	gen,gen	Divide, rounding toward zero.
7	REMi	gen,gen	Remainder from QUO.
7	DIVi	gen,gen	Divide, rounding down.
7	MODi	gen,gen	Remainder from DIV (Modulus).
7	MEIi	gen,gen	Multiply to Extended Integer.
7	DEIi	gen,gen	Divide Extended Integer.

PACKED DECIMAL (BCD) ARITHMETIC

Format	Operation	Operands	Description
6	ADDPi	gen,gen	Add Packed.
6	SUBPi	gen,gen	Subtract Packed.

INTEGER COMPARISON

Format	Operation	Operands	Description
4	CMPi	gen,gen	Compare.
2	CMPQi	short,gen	Compare to signed 4-bit constant.
7	CMPMi	gen,gen,disp	Compare Multiple: disp bytes (1 to 16).

LOGICAL AND BOOLEAN

Format	Operation	Operands	Description
4	ANDi	gen,gen	Logical AND.
4	ORi	gen,gen	Logical OR.
4	BICi	gen,gen	Clear selected bits.
4	XORi	gen,gen	Logical Exclusive OR.
6	COMi	gen,gen	Complement all bits.
6	NOTi	gen,gen	Boolean complement: LSB only.
2	Scondi	gen	Save condition code (cond) as a Boolean variable of size i.

2.0 Architectural Description (Continued)

TABLE 2-2 (Continued)
NS32C032 Instruction Set Summary (Continued)

SHIFTS

Format	Operation	Operands	Description
6	LSHi	gen,gen	Logical Shift, left or right.
6	ASHi	gen,gen	Arithmetic Shift, left or right.
6	ROTi	gen,gen	Rotate, left or right.

BITS

Format	Operation	Operands	Description
4	TBITi	gen,gen	Test bit.
6	SBITi	gen,gen	Test and set bit.
6	SBITIi	gen,gen	Test and set bit, interlocked
6	CBITi	gen,gen	Test and clear bit.
6	CBITIi	gen,gen	Test and clear bit, interlocked.
6	IBITi	gen,gen	Test and invert bit.
8	FFSi	gen,gen	Find first set bit

BIT FIELDS

Bit fields are values in memory that are not aligned to byte boundaries. Examples are PACKED arrays and records used in Pascal. "Extract" instructions read and align a bit field. "Insert" instructions write a bit field from an aligned source.

Format	Operation	Operands	Description
8	EXTi	reg,gen,gen,disp	Extract bit field (array oriented).
8	INSi	reg,gen,gen,disp	Insert bit field (array oriented).
7	EXTSi	gen,gen,imm,imm	Extract bit field (short form).
7	INSSi	gen,gen,imm,imm	Insert bit field (short form).
8	CVTP	reg,gen,gen	Convert to Bit Field Pointer.

ARRAYS

Format	Operation	Operands	Description
8	CHECKi	reg,gen,gen	Index bounds check.
8	INDEXi	reg,gen,gen	Recursive indexing step for multiple-dimensional arrays.

STRINGS

String instructions assign specific functions to the General Purpose Registers:

R4 - Comparison Value

R3 - Translation Table Pointer

R2 - String 2 Pointer

R1 - String 1 Pointer

R0 - Limit Count

Options on all string instructions are:

B (Backward): Decrement string pointers after each step rather than incrementing.

U (Until match): End instruction if String 1 entry matches R4.

W (While match): End instruction if String 1 entry does not match R4.

All string instructions end when R0 decrements to zero.

Format	Operation	Operands	Descriptions
5	MOVSi	options	Move String 1 to String 2.
	MOVST	options	Move string, translating bytes.
5	CMPSi	options	Compare String 1 to String 2.
	CMPST	options	Compare translating, String 1 bytes.
5	SKPSi	options	Skip over String 1 entries
	SKPST	options	Skip, translating bytes for Until/While.

2.0 Architectural Description (Continued)

TABLE 2-2 (Continued)
NS32C032 Instruction Set Summary (Continued)

JUMPS AND LINKAGE

Format	Operation	Operands	Description
3	JUMP	gen	Jump.
0	BR	disp	Branch (PC Relative).
0	Bcond	disp	Conditional branch.
3	CASEi	gen	Multiway branch.
2	ACBi	short,gen,disp	Add 4-bit constant and branch if non-zero.
3	JSR	gen	Jump to subroutine.
1	BSR	disp	Branch to subroutine.
1	CXP	disp	Call external procedure.
3	CXPD	gen	Call external procedure using descriptor.
1	SVC		Supervisor Call.
1	FLAG		Flag Trap.
1	BPT		Breakpoint Trap.
1	ENTER	[reg list],disp	Save registers and allocate stack frame (Enter Procedure).
1	EXIT	[reg list]	Restore registers and reclaim stack frame (Exit Procedure).
1	RET	disp	Return from subroutine.
1	RXP	disp	Return from external procedure call.
1	RETT	disp	Return from trap. (Privileged)
1	RETI		Return from interrupt. (Privileged)

CPU REGISTER MANIPULATION

Format	Operation	Operands	Description
1	SAVE	[reg list]	Save General Purpose Registers.
1	RESTORE	[reg list]	Restore General Purpose Registers.
2	LPRi	areg,gen	Load Dedicated Register. (Privileged if PSR or INTBASE)
2	SPRi	areg,gen	Store Dedicated Register. (Privileged if PSR or INTBASE)
3	ADJSPi	gen	Adjust Stack Pointer.
3	BISPSRi	gen	Set selected bits in PSR. (Privileged if not Byte length)
3	BICPSRi	gen	Clear selected bits in PSR. (Privileged if not Byte length)
5	SETCFG	[option list]	Set Configuration Register. (Privileged)

FLOATING POINT

Format	Operation	Operands	Description
11	MOVf	gen,gen	Move a Floating Point value.
9	MOVLF	gen,gen	Move and shorten a Long value to Standard.
9	MOVFL	gen,gen	Move and lengthen a Standard value to Long.
9	MOVif	gen,gen	Convert any integer to Standard or Long Floating.
9	ROUNDfi	gen,gen	Convert to integer by rounding.
9	TRUNCfi	gen,gen	Convert to integer by truncating, toward zero.
9	FLOORfi	gen,gen	Convert to largest integer less than or equal to value.
11	ADDf	gen,gen	Add.
11	SUBf	gen,gen	Subtract.
11	MULf	gen,gen	Multiply.
11	DIVf	gen,gen	Divide.
11	CMPf	gen,gen	Compare.
11	NEGf	gen,gen	Negate.
11	ABSf	gen,gen	Take absolute value.
9	LFSR	gen	Load FSR.
9	SFSR	gen	Store FSR.

MEMORY MANAGEMENT

Format	Operation	Operands	Description
14	LMR	mreg,gen	Load Memory Management Register. (Privileged)
14	SMR	mreg,gen	Store Memory Management Register. (Privileged)
14	RDVAL	gen	Validate address for reading. (Privileged)
14	WRVAL	gen	Validate address for writing. (Privileged)
8	MOVSUi	gen,gen	Move a value from Supervisor Space to User Space. (Privileged)
8	MOVUSi	gen,gen	Move a value from User Space to Supervisor Space. (Privileged)

2.0 Architectural Description (Continued)

TABLE 2-2 (Continued)
NS32C032 Instruction Set Summary (Continued)

MISCELLANEOUS

Format	Operation	Operands	Description
1	NOP		No Operation.
1	WAIT		Wait for interrupt.
1	DIA		Diagnose. Single-byte "Branch to Self" for hardware breakpointing. Not for use in programming.

CUSTOM SLAVE

Format	Operation	Operands	Description
15.5	CCAL0c	gen,gen	Custom Calculate.
15.5	CCAL1c	gen,gen	
15.5	CCAL2c	gen,gen	
15.5	CCAL3c	gen,gen	
15.5	CMOV0c	gen,gen	Custom Move.
15.5	CMOV1c	gen,gen	
15.5	CMOV2c	gen,gen	
15.5	CMOV3c	gen,gen	
15.5	CCMP0c	gen,gen	Custom Compare.
15.5	CCMP1c	gen,gen	
15.1	CCV0ci	gen,gen	Custom Convert.
15.1	CCV1ci	gen,gen	
15.1	CCV2ci	gen,gen	
15.1	CCV3ic	gen,gen	
15.1	CCV4DQ	gen,gen	
15.1	CCV5QD	gen,gen	
15.1	LCSR	gen	Load Custom Status Register.
15.1	SCSR	gen	Store Custom Status Register.
15.0	CATST0	gen	Custom Address/Test. (Privileged)
15.0	CATST1	gen	(Privileged)
15.0	LCR	creg,gen	Load Custom Register. (Privileged)
15.0	SCR	creg,gen	Store Custom Register. (Privileged)

3.0 Functional Description

3.1 POWER AND GROUNDING

The NS32C032 requires a single 5-volt power supply, applied on 4 pins. The Logic Voltage pins ($V_{CC}L1$ and $V_{CC}L2$) supply the power to the on-chip logic. The Buffer Voltage pins (V_{CCB1} and V_{CCB2}) supply the power to the output drivers of the chip. The Logic Voltage pins and the Buffer Voltage pins should be connected together by a power (V_{CC}) plane on the printed circuit board.

The NS32C032 grounding connections are made on 5 pins. The Logic Ground pins (GNDL1 and GNDL2) are the ground pins for the on-chip logic. The Buffer Ground pins (GNDB1 to GNDB3) are the ground pins for the output drivers of the chip. The Logic Ground pins and the Buffer Ground pins should be connected together by a ground plane on the printed circuit board.

Both power and ground connections are shown below (Figure 3-1).

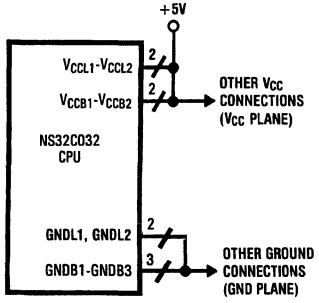

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FIGURE 3-1. Recommended Supply Connections

3.2 CLOCKING

The NS32C032 inputs clocking signals from the Timing Control Unit (TCU), which presents two non-overlapping phases of a single clock frequency. These phases are called PHI1 (pin 26) and PHI2 (pin 27). Their relationship to each other is shown in *Figure 3-2*.

Each rising edge of PHI1 defines a transition in the timing state ("T-State") of the CPU. One T-State represents the execution of one microinstruction within the CPU, and/or one step of an external bus transfer. See Section 4 for complete specifications of PHI1 and PHI2.

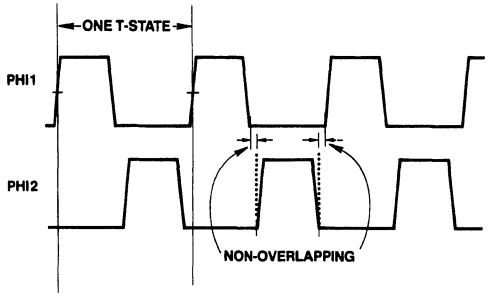

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FIGURE 3-2. Clock Timing Relationships

As the TCU presents signals with very fast transitions, it is recommended that the conductors carrying PHI1 and PHI2 be kept as short as possible, and that they not be connected anywhere except from the TCU to the CPU and, if present, the MMU. A TTL Clock signal (CTTL) is provided by the TCU for all other clocking.

3.3 RESETTING

The $\overline{RST}/\overline{ABT}$ pin serves both as a Reset for on-chip logic and as the Abort input for Memory-Managed systems. For its use as the Abort Command, see Sec. 3.5.4.

The CPU may be reset at any time by pulling the $\overline{RST}/\overline{ABT}$ pin low for at least 64 clock cycles. Upon detecting a reset, the CPU terminates instruction processing, resets its internal logic, and clears the Program Counter (PC) and Processor Status Register (PSR) to all zeroes.

On application of power, $\overline{RST}/\overline{ABT}$ must be held low for at least 50 μsec after V_{CC} is stable. This is to ensure that all on-chip voltages are completely stable before operation. Whenever a Reset is applied, it must also remain

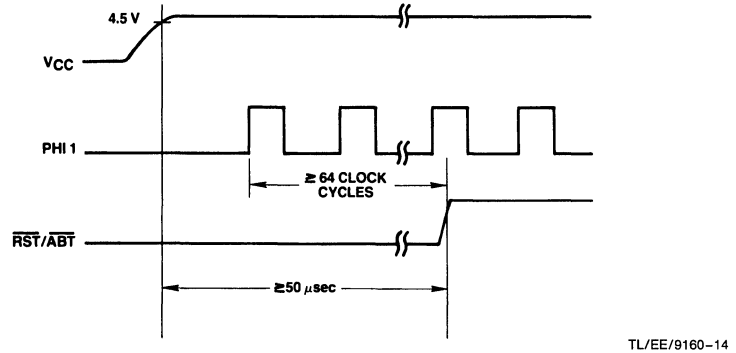

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FIGURE 3-3. Power-on Reset Requirements

3.0 Functional Description (Continued)

active for not less than 64 clock cycles. The rising edge must occur while PHI1 is high. See *Figures 3-3* and *3-4*.

The NS32C201 Timing Control Unit (TCU) provides circuitry to meet the Reset requirements of the NS32C032 CPU. *Figure 3-5a* shows the recommended connections for a non-Memory-Managed system. *Figure 3-5b* shows the connections for a Memory-Managed system.

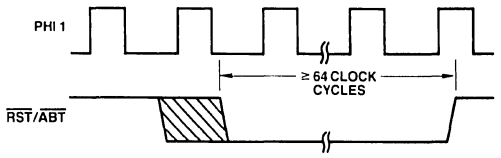

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FIGURE 3-4. General Reset Timing

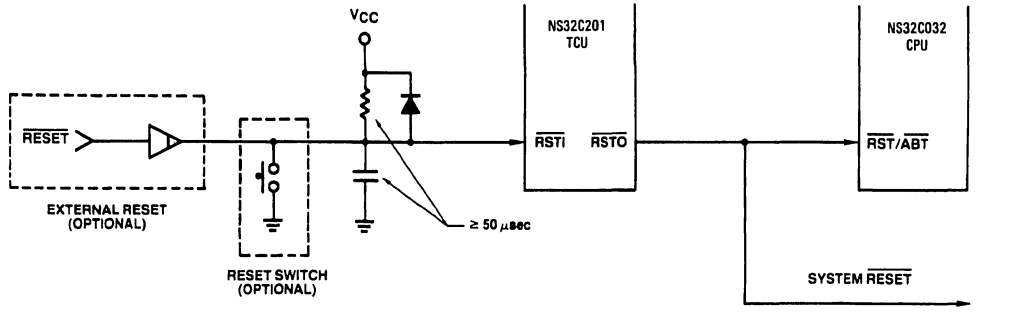

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FIGURE 3-5a. Recommended Reset Connections, Non-Memory-Managed System

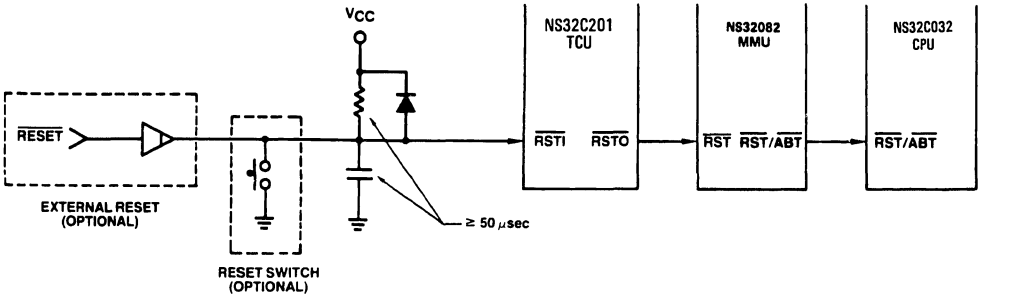

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FIGURE 3-5b. Recommended Reset Connections, Memory-Managed System

3.4 BUS CYCLES

The NS32C032 CPU has a strap option which defines the Bus Timing Mode as either With or Without Address Translation. This section describes only bus cycles under the No Address Translation option. For details of the use of the strap and of bus cycles with address translation, see Sec. 3.5.

The CPU will perform a bus cycle for one of the following reasons:

1) To write or read data, to or from memory or a peripheral interface device. Peripheral input and output are memory-mapped in the Series 32000 family.
2) To fetch instructions into the eight-byte instruction queue. This happens whenever the bus would otherwise be idle and the queue is not already full.
3) To acknowledge an interrupt and allow external circuitry to provide a vector number, or to acknowledge completion of an interrupt service routine.
4) To transfer information to or from a Slave Processor.

In terms of bus timing, cases 1 through 3 above are identical. For timing specifications, see Sec. 4. The only external difference between them is the four-bit code placed on the Bus Status pins (ST0–ST3). Slave Processor cycles differ in that separate control signals are applied (Sec. 3.4.6).

The sequence of events in a non-Slave bus cycle is shown below in *Figure 3-7* for a Read cycle and *Figure 3-8* for a Write cycle. The cases shown assume that the selected memory or interface device is capable of communicating with the CPU at full speed. If it is not, then cycle extension may be requested through the RDY line (Sec. 3.4.1).

3.0 Functional Description (Continued)

A full-speed bus cycle is performed in four cycles of the PHI1 clock signal, labeled T1 through T4. Clock cycles not associated with a bus cycle are designated Ti (for "Idle").

During T1, the CPU applies an address on pins AD0–AD23. It also provides a low-going pulse on the ADS pin, which serves the dual purpose of informing external circuitry that a bus cycle is starting and of providing control to an external latch for demultiplexing Address bits 0–23 from the AD0–AD23 pins. See *Figure 3-6*. During this time also the status signals DDIN, indicating the direction of the transfer, and $\overline{BE0}$–$\overline{BE3}$, indicating which of the four bus bytes are to be referenced, become valid.

During T2 the CPU switches the Data Bus, AD0–AD31 to either accept or present data. It also starts the data strobe ($\overline{DS}$), signalling the beginning of the data transfer. Associated signals from the NS32C201 Timing Control Unit are also activated at this time: $\overline{RD}$ (Read Strobe) or $\overline{WR}$ (Write Strobe), $\overline{TSO}$ (Timing State Output, indicating that T2 has been reached) and DBE (Data Buffer Enable).

The T3 state provides for access time requirements, and it occurs at least once in a bus cycle. At the end of T2 or T3, on the falling edge of the PHI2 clock, the RDY (Ready) line is sampled to determine whether the bus cycle will be extended (Sec. 3.4.1).

If the CPU is performing a Read cycle, the Data Bus (AD0–AD31) is sampled at the falling edge of PHI2 of the last T3 state. See Section 4. Data must, however, be held at least until the beginning of T4. $\overline{DS}$ and $\overline{RD}$ are guaranteed not to go inactive before this point, so the rising edge of either of them may safely be used to disable the device providing the input data.

The T4 state finishes the bus cycle. At the beginning of T4, the $\overline{DS}$, $\overline{RD}$ or $\overline{WR}$, and $\overline{TSO}$ signals go inactive, and at the rising edge of PHI2, $\overline{DBE}$ goes inactive, having provided for necessary data hold times. Data during Write cycles remains valid from the CPU throughout T4. Note that the Bus Status lines (ST0–ST3) change at the beginning of T4, anticipating the following bus cycle (if any).

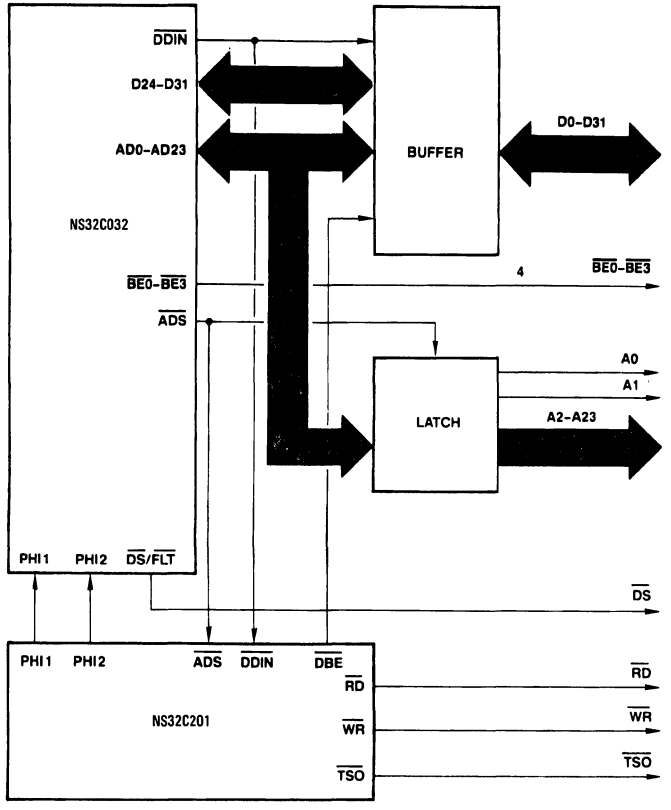

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FIGURE 3-6. Bus Connections

3.0 Functional Description (Continued)

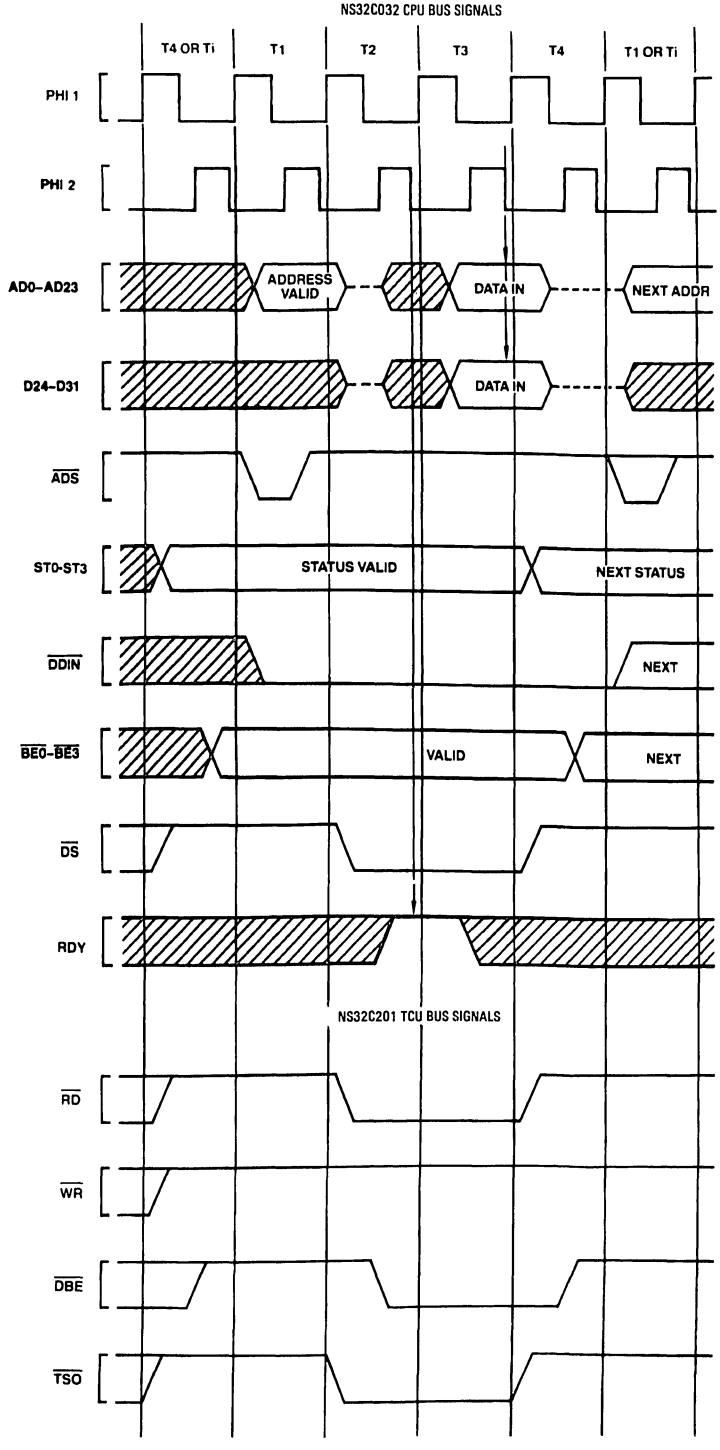

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FIGURE 3-7. Read Cycle Timing

3.0 Functional Description (Continued)

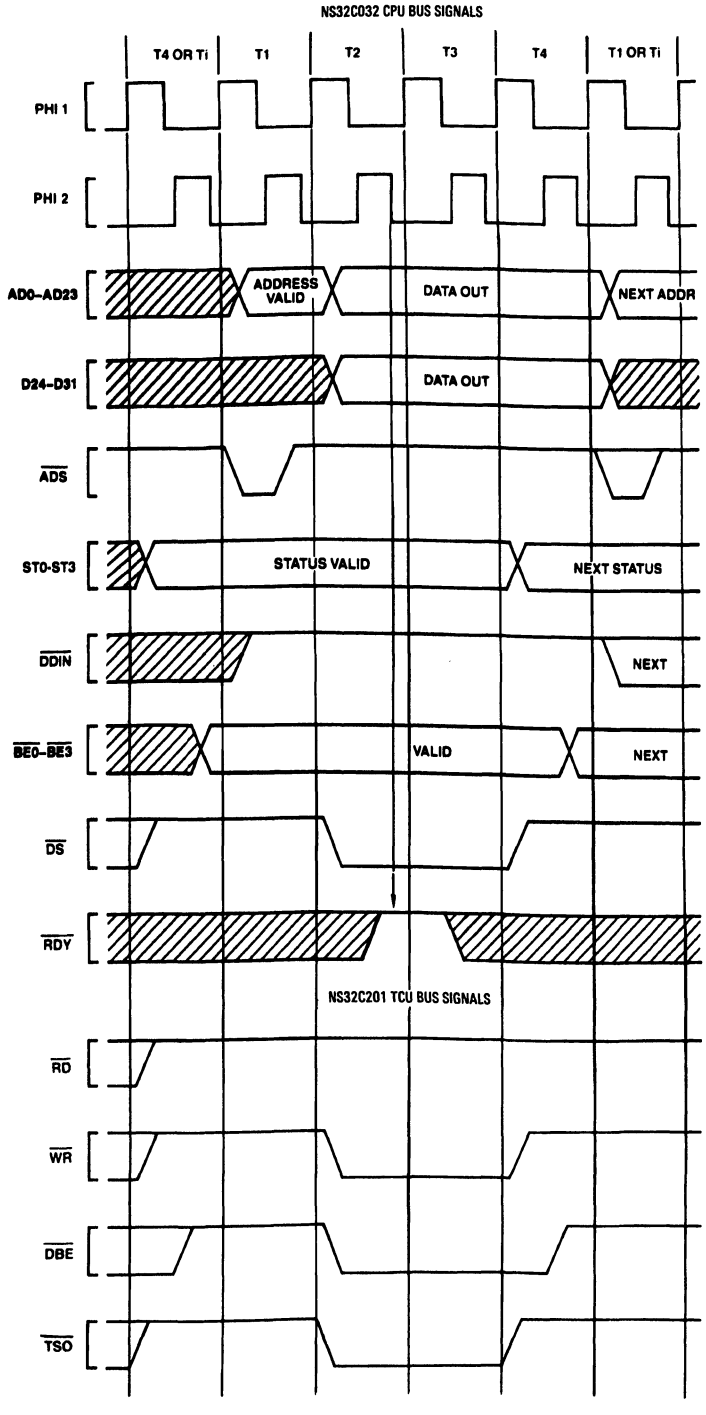

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FIGURE 3-8. Write Cycle Timing

3.0 Functional Description (Continued)

3.4.1 Cycle Extension

To allow sufficient strobe widths and access times for any speed of memory or peripheral device, the NS32C032 provides for extension of a bus cycle. Any type of bus cycle except a Slave Processor cycle can be extended.

In *Figures 3-7* and *3-8*, note that during T3 all bus control signals from the CPU and TCU are flat. Therefore, a bus cycle can be cleanly extended by causing the T3 state to be repeated. This is the purpose of the RDY (Ready) pin.

At the end of T2 on the falling edge of PHI2, the RDY line is sampled by the CPU. If RDY is high, the next T-states will be T3 and then T4, ending the bus cycle. If RDY is low, then another T3 state will be inserted after the next T-state and the RDY line will again be sampled on the falling edge of PHI2. Each additional T3 state after the first is referred to as a "WAIT STATE". See *Figure 3-9*.

The RDY pin is driven by the NS32C201 Timing Control Unit, which applies WAIT States to the CPU as requested on three sets of pin:

1) $\overline{\text{CWAIT}}$ (Continuous WAIT), which holds the CPU in WAIT states until removed.
2) $\overline{\text{WAIT1}}$, $\overline{\text{WAIT2}}$, $\overline{\text{WAIT4}}$, $\overline{\text{WAIT8}}$ (Collectively $\overline{\text{WAITn}}$), which may be given a four-bit binary value requesting a specific number of WAIT States from 0 to 15.
3) $\overline{\text{PER}}$ (Peripheral), which inserts five additional WAIT states and causes the TCU to reshape the $\overline{\text{RD}}$ and $\overline{\text{WR}}$ strobes. This provides the setup and hold times required by most MOS peripheral interface devices.

Combinations of these various WAIT requests are both legal and useful. For details of their use, see the NS32C201 Data Sheet.

Figure 3-10 illustrates a typical Read cycle, with two WAIT states requested through the TCU $\overline{\text{WAITn}}$ pins.

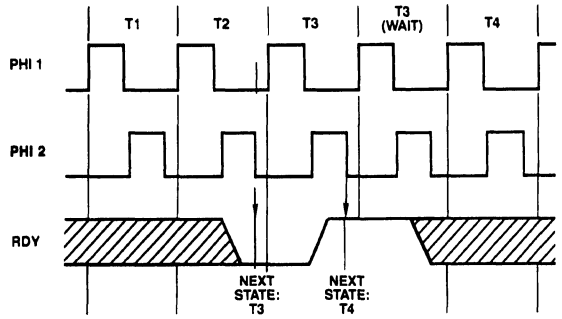

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FIGURE 3-9. RDY Pin Timing

3.4.2 Bus Status

The NS32C032 CPU presents four bits of Bus Status information on pins ST0–ST3. The various combinations on these pins indicate why the CPU is performing a bus cycle, or, if it is idle on the bus, then why is it idle.

Referring to *Figures 3-7* and *3-8*, note that Bus Status leads the corresponding Bus Cycle, going valid one clock cycle before T1, and changing to the next state at T4. This allows the system designer to fully decode the Bus Status and, if desired, latch the decoded signals before $\overline{\text{ADS}}$ initiates the Bus Cycle.

The Bus Status pins are interpreted as a four-bit value, with ST0 the least significant bit. Their values decode as follows:

0000 – The bus is idle because the CPU does not need to perform a bus access.

0001 – The bus is idle because the CPU is executing the WAIT instruction.

0010 – (Reserved for future use.)

0011 – The bus is idle because the CPU is waiting for a Slave Processor to complete an instruction.

0100 – Interrupt Acknowledge, Master.

The CPU is performing a Read cycle. To acknowledge receipt of a Non-Maskable Interrupt (on $\overline{\text{NMI}}$) it will read from address FFFF00_{16}, but will ignore any data provided.

To acknowledge receipt of a Maskable Interrupt (on $\overline{\text{INT}}$) it will read from address FFFE00_{16}, expecting a vector number to be provided from the Master NS32202 Interrupt Control Unit. If the vectoring mode selected by the last SETCFG instruction was Non-Vectored, then the CPU will ignore the value it has read and will use a default vector instead, having assumed that no NS32202 is present. See Sec. 3.4.5.

0101 – Interrupt Acknowledge, Cascaded.

The CPU is reading a vector number from a Cascaded NS32202 Interrupt Control Unit. The address provided is the address of the NS32202 Hardware Vector register. See Sec. 3.4.5.

0110 – End of Interrupt, Master.

The CPU is performing a Read cycle to indicate that it is executing a Return from Interrupt (RETI) instruction. See Sec. 3.4.5.

0111 – End of Interrupt, Cascaded.

The CPU is reading from a Cascaded Interrupt Control Unit to indicate that it is returning (through RETI) from an interrupt service routine requested by that unit. See Sec. 3.4.5.

1000 – Sequential Instruction Fetch.

The CPU is reading the next sequential word from the instruction stream into the Instruction

3.0 Functional Description (Continued)

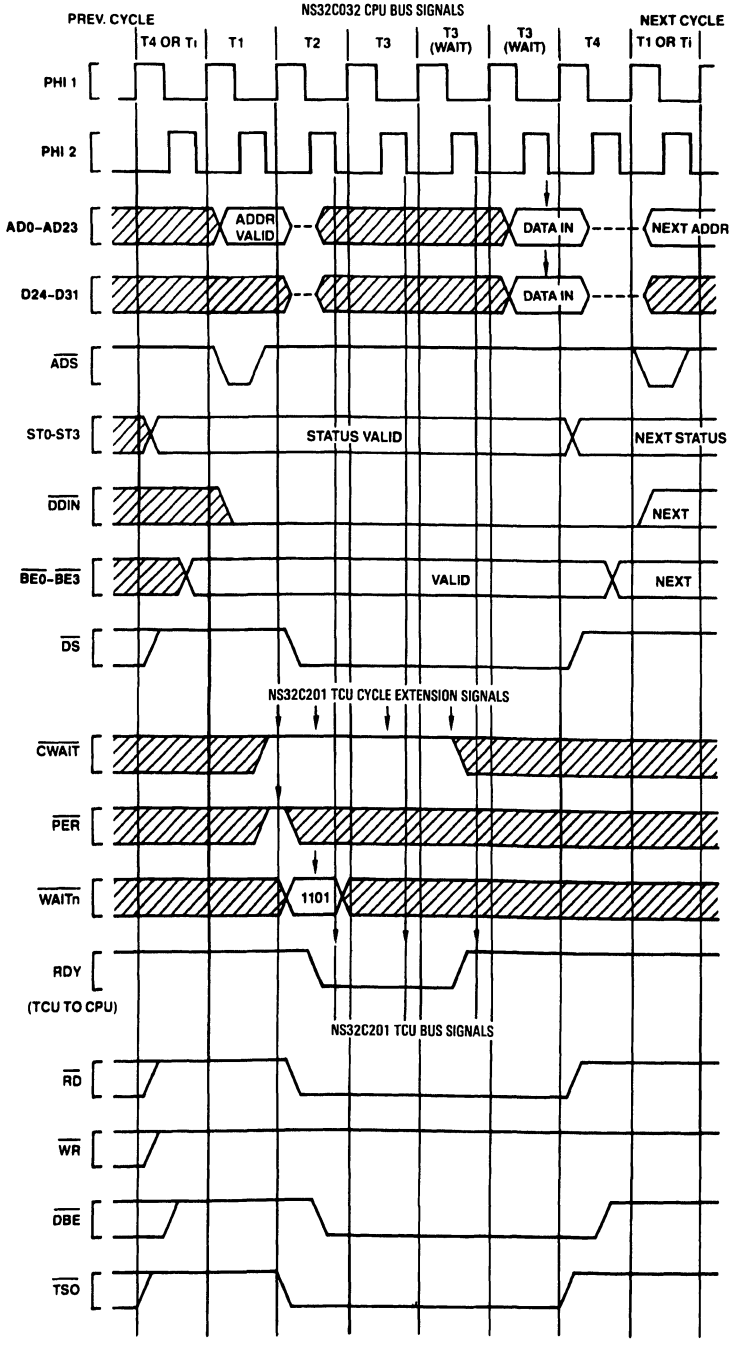

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FIGURE 3-10. Extended Cycle Example

Note: Arrows on $\overline{\text{CWAIT}}$, $\overline{\text{PER}}$, $\overline{\text{WAIT}}$n indicate points at which the TCU samples. Arrows on AD0–AD15 and RDY indicate points at which the CPU samples.

3.0 Functional Description (Continued)

Queue. It will do so whenever the bus would otherwise be idle and the queue is not already full.

1001 – Non-Sequential Instruction Fetch.

The CPU is performing the first fetch of instruction code after the Instruction Queue is purged. This will occur as a result of any jump or branch, or any interrupt or trap, or execution of certain instructions.

1010 – Data Transfer.

The CPU is reading or writing an operand of an instruction.

1011 – Read RMW Operand.

The CPU is reading an operand which will subsequently be modified and rewritten. If memory protection circuitry would not allow the following Write cycle, it must abort this cycle.

1100 – Read for Effective Address Calculation.

The CPU is reading information from memory in order to determine the Effective Address of an operand. This will occur whenever an instruction uses the Memory Relative or External addressing mode.

1101 – Transfer Slave Processor Operand.

The CPU is either transferring an instruction operand to or from a Slave Processor, or it is issuing the Operation Word of a Slave Processor instruction. See Sec. 3.9.1.

1110 – Read Slave Processor Status.

The CPU is reading a Status Word from a Slave Processor. This occurs after the Slave Processor has signalled completion of an instruction. The transferred word tells the CPU whether a trap should be taken, and in some instructions it presents new values for the CPU Processor Status Register bits N, Z, L or F. See Sec. 3.9.1.

1111 – Broadcast Slave ID.

The CPU is initiating the execution of a Slave Processor instruction. The ID Byte (first byte of the instruction) is sent to all Slave Processors, one of which will recognize it. From this point the CPU is communicating with only one Slave Processor. See Sec. 3.9.1.

3.4.3 Data Access Sequences

The 24-bit address provided by the NS32C032 is a byte address; that is, it uniquely identifies one of up to 16,777,216 eight-bit memory locations. An important feature of the NS32C032 is that the presence of a 32-bit data bus imposes no restrictions on data alignment; any data item, regardless of size, may be placed starting at any memory address. The NS32C032 provides special control signals. Byte Enable ($\overline{BE0}$–$\overline{BE3}$) which facilitate individual byte accessing on a 32-bit bus.

Memory is organized as four eight-bit banks, each bank receiving the double-word address (A2–A23) in parallel. One bank, connected to Data Bus pins AD0–AD7 is enabled when $\overline{BE0}$ is low. The second bank, connected to data bus pins AD8–AD15 is enabled when $\overline{BE1}$ is low. The third and fourth banks are enabled by $\overline{BE2}$ and $\overline{BE3}$, respectively. See *Figure 3-11*.

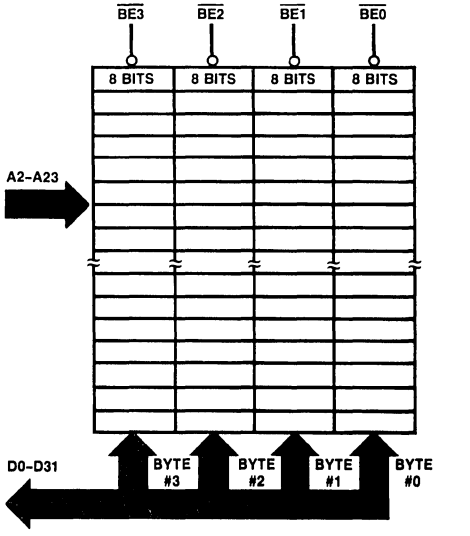

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FIGURE 3-11. Memory Interface

Since operands do not need to be aligned with respect to the double-word bus access performed by the CPU, a given double-word access can contain one, two, three, or four bytes of the operand being addressed, and these bytes can begin at various positions, as determined by A1, A0. Table 3-1 lists the 10 resulting access types.

TABLE 3-1
Bus Access Types

Type	Bytes Accessed	A1,A0	$\overline{BE3}$	$\overline{BE2}$	$\overline{BE1}$	$\overline{BE0}$
1	1	00	1	1	1	0
2	1	01	1	1	0	1
3	1	10	1	0	1	1
4	1	11	0	1	1	1
5	2	00	1	1	0	0
6	2	01	1	0	0	1
7	2	10	0	0	1	1
8	3	00	1	0	0	0
9	3	01	0	0	0	1
10	4	00	0	0	0	0

Accesses of operands requiring more than one bus cycle are performed sequentially, with no idle T-States separating them. The number of bus cycles required to transfer an operand depends on its size and its alignment. Table 3-2 lists the bus cycles performed for each situation.

3.0 Functional Description (Continued)

TABLE 3-2
Access Sequences

Cycle	Type	Address	$\overline{BE3}$	$\overline{BE2}$	$\overline{BE1}$	$\overline{BE0}$	Data Bus Byte 3	Byte 2	Byte 1	Byte 0
A. ***Word at address ending with 11***									BYTE 1 | BYTE 0	← A
1.	4	A	0	1	1	1	Byte 0	X	X	X
2.	1	A + 1	1	1	1	0	X	X	X	Byte 1
B. ***Double word at address ending with 01***							BYTE 3 | BYTE 2 | BYTE 1 | BYTE 0			← A
1.	9	A	0	0	0	1	Byte 2	Byte 1	Byte 0	X
2.	1	A + 3	1	1	1	0	X	X	X	Byte 3
C. ***Double word at address ending with 10***							BYTE 3 | BYTE 2 | BYTE 1 | BYTE 0			← A
1.	7	A	0	0	1	1	Byte 1	Byte 0	X	X
2.	5	A + 2	1	1	0	0	X	X	Byte 3	Byte 2
D. ***Double word at address ending with 11***							BYTE 3 | BYTE 2 | BYTE 1 | BYTE 0			← A
1.	4	A	0	1	1	1	Byte 0	X	X	X
2.	8	A + 1	1	0	0	0	X	Byte 3	Byte 2	Byte 1
E. ***Quad word at address ending with 00***							BYTE 7 | BYTE 6 | BYTE 5 | BYTE 4 | BYTE 3 | BYTE 2 | BYTE 1 | BYTE 0			← A
1.	10	A	0	0	0	0	Byte 3	Byte 2	Byte 1	Byte 0
Other bus cycles (instruction prefetch or slave) can occur here.										
2.	10	A + 4	0	0	0	0	Byte 7	Byte 6	Byte 5	Byte 4
F. ***Quad word at address ending with 01***							BYTE 7 | BYTE 6 | BYTE 5 | BYTE 4 | BYTE 3 | BYTE 2 | BYTE 1 | BYTE 0			← A
1.	9	A	0	0	0	1	Byte 2	Byte 1	Byte 0	X
2.	1	A + 3	1	1	1	0	X	X	X	Byte 3
Other bus cycles (instruction prefetch or slave) can occur here.										
3.	9	A + 4	0	0	0	1	Byte 6	Byte 5	Byte 4	X
4.	1	A + 7	1	1	1	0	X	X	X	Byte 7
G. ***Quad word at address ending with 10***							BYTE 7 | BYTE 6 | BYTE 5 | BYTE 4 | BYTE 3 | BYTE 2 | BYTE 1 | BYTE 0			← A
1.	7	A	0	0	1	1	Byte 1	Byte 0	X	X
2.	5	A + 2	1	1	0	0	X	X	Byte 3	Byte 2
Other bus cycles (instruction prefetch or slave) can occur here.										
3.	7	A + 4	0	0	1	1	Byte 5	Byte 4	X	X
4.	5	A + 6	1	1	0	0	X	X	Byte 7	Byte 6
H. ***Quad word at address ending with 11***							BYTE 7 | BYTE 6 | BYTE 5 | BYTE 4 | BYTE 3 | BYTE 2 | BYTE 1 | BYTE 0			← A
1.	4	A	0	1	1	1	Byte 0	X	X	X
2.	8	A + 1	1	0	0	0	X	Byte 3	Byte 2	Byte 1
Other bus cycles (instruction prefetch or slave) can occur here.										
1.	4	A + 4	0	1	1	1	Byte 4	X	X	X
2.	8	A + 5	1	0	0	0	X	Byte 7	Byte 6	Byte 5

X = Don't Care

3.0 Functional Description (Continued)

3.4.3.1 Bit Accesses

The Bit Instructions perform byte accesses to the byte containing the designated bit. The Test and Set Bit instruction (SBIT), for example, reads a byte, alters it, and rewrites it, having changed the contents of one bit.

3.4.3.2 Bit Field Accesses

An access to a Bit Field in memory always generates a Double-Word transfer at the address containing the least significant bit of the field. The Double Word is read by an Extract instruction; an Insert instruction reads a Double Word, modifies it, and rewrites it.

3.4.3.3 Extending Multiply Accesses

The Extending Multiply Instruction (MEI) will return a result which is twice the size in bytes of the operand it reads. If the multiplicand is in memory, the most-significant half of the result is written first (at the higher address), then the least-significant half. This is done in order to support retry if this instruction is aborted.

3.4.4 Instruction Fetches

Instructions for the NS32C032 CPU are "prefetched"; that is, they are input before being needed into the next available entry of the eight-byte Instruction Queue. The CPU performs two types of Instruction Fetch cycles: Sequential and Non-Sequential. These can be distinguished from each other by their differing status combinations on pins ST0–ST3 (Sec. 3.4.2).

A Sequential Fetch will be performed by the CPU whenever the Data Bus would otherwise be idle and the Instruction Queue is not currently full. Sequential Fetches are always type 10 Read cycles (Table 3-1).

A Non-Sequential Fetch occurs as a result of any break in the normally sequential flow of a program. Any jump or branch instruction, a trap or an interrupt will cause the next Instruction Fetch cycle to be Non-Sequential. In addition, certain instructions flush the instruction queue, causing the next instruction fetch to display Non-Sequential status. Only the first bus cycle after a break displays Non-Sequential status, and that cycle depends on the destination address.

Note: During non-sequential fetches, $\overline{BE0}$–$\overline{BE3}$ are all active regardless of the alignment.

3.4.5 Interrupt Control Cycles

Activating the $\overline{INT}$ or $\overline{NMI}$ pin on the CPU will initiate one or more bus cycles whose purpose is interrupt control rather than the transfer of instructions or data. Execution of the Return from Interrupt instruction (RETI) will also cause Interrupt Control bus cycles. These differ from instruction or data transfers only in the status pesented on pins ST0–ST3. All Interrupt Control cycles are single-byte Read cycles.

This section describes only the Interrupt Control sequences associated with each interrupt and with the return from its service routine. For full details of the NS32C032 interrupt structure, see Sec. 3.8.

3.0 Functional Description (Continued)

TABLE 3-3
Interrupt Sequences

Cycle	Status	Address	$\overline{DDIN}$	$\overline{BE3}$	$\overline{BE2}$	$\overline{BE1}$	$\overline{BE0}$	Data Bus Byte 3	Byte 2	Byte 1	Byte 0
A. Non-Maskable Interrupt Control Sequences											
Interrupt Acknowledge											
1	0100	$FFFF00_{16}$	0	1	1	1	0	X	X	X	X
Interrupt Return											
None: Performed through Return from Trap (RETT) instruction.											
B. Non-Vectored Interrupt Control Sequences											
Interrupt Acknowledge											
1	0100	$FFFE00_{16}$	0	1	1	1	0	X	X	X	X
Interrupt Return											
1	0110	$FFFE00_{16}$	0	1	1	1	0	X	X	X	X
C. Vectored Interrupt Sequences: Non-Cascaded.											
Interrupt Acknowledge											
1	0100	$FFFE00_{16}$	0	1	1	1	0	X	X	X	Vector: Range: 0-127
Interrupt Return											
1	0110	$FFFE00_{16}$	0	1	1	1	0	X	X	X	Vector: Same as in Previous Int. Ack. Cycle
D. Vectored Interrupt Sequences: Cascaded											
Interrupt Acknowledge											
1	0100	$FFFE00_{16}$	0	1	1	1	0	X	X	X	Cascade Index: range −16 to −1
(The CPU here uses the Cascade Index to find the Cascade Address.)											
2	0101	Cascade Address	0	See Note				Vector, range 9–255; on appropriate byte of data bus.			
Interrupt Return											
1	0110	$FFFE00_{16}$	0	1	1	1	0	X	X	X	Cascade Index: Same as in previous Int. Ack. Cycle
(The CPU here uses the Cascade Index to find the Cascade Address)											
2	0111	Cascade Address	0	See Note				X	X	X	X

X = Don't Care

Note: $\overline{BE0}$-$\overline{BE3}$ signals will be activated according to the cascaded ICU address. The cycle type can be 1, 2, 3 or 4, when reading the interrupt vector. The vector value can be in the range 0–255.

3.0 Functional Description (Continued)

3.4.6 Slave Processor Communication

In addition to its use as the Address Translation strap (Sec. 3.5.1), the $\overline{AT}/\overline{SPC}$ pin is used as the data strobe for Slave Processor transfers. In this role, it is referred to as Slave Processor Control ($\overline{SPC}$). In a Slave Processor bus cycle, data is transferred on the Data Bus (AD0–AD15), and the status lines (ST0–ST3) are monitored by each Slave Processor in order to determine the type of transfer being performed. $\overline{SPC}$ is bidirectional, but is driven by the CPU during all Slave Processor bus cycles. See Sec. 3.9 for full protocol sequences.

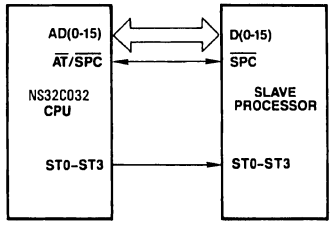

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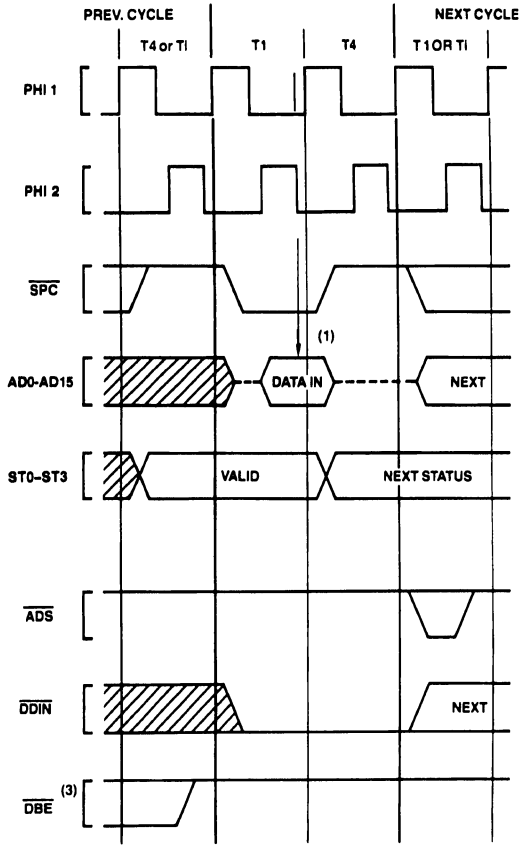
FIGURE 3-12. Slave Processor Connections



TL/EE/9160–25

Note:

(1) CPU samples Data Bus here.

(2) $\overline{DBE}$ and all other NS32C201 TCU bus signals remain inactive because no $\overline{ADS}$ pulse is received from the CPU.

FIGURE 3-13. CPU Read from Slave Processor

3.0 Functional Description (Continued)

3.4.6.1 Slave Processor Bus Cycles

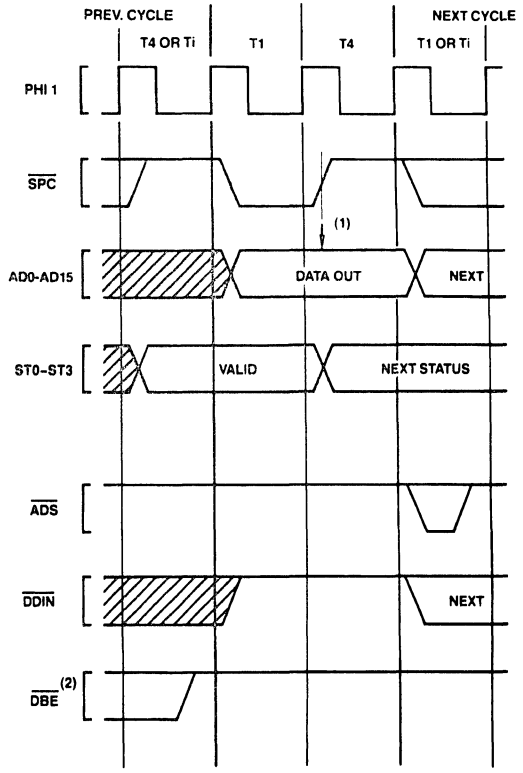
A Slave Processor bus cycle always takes exactly two clock cycles, labeled T1 and T4 (see *Figures 3-13* and *3-14*). During a Read cycle $\overline{SPC}$ is active from the beginning of T1 to the beginning of T4, and the data is sampled at the end of T1. The Cycle Status pins lead the cycle by one clock period, and are sampled at the leading edge of $\overline{SPC}$. During a Write cycle, the CPU applies data and activates $\overline{SPC}$ at T1, removing $\overline{SPC}$ at T4. The Slave Processor latches status on the leading edge of $\overline{SPC}$ and latches data on the trailing edge.

Since the CPU does not pulse the Address Strobe ($\overline{ADS}$), no bus signals are generated by the NS32C201 Timing Control Unit. The direction of a transfer is determined by the sequence ("protocol") established by the instruction under execution; but the CPU indicates the direction on the $\overline{DDIN}$ pin for hardware debugging purposes.

3.4.6.2 Slave Operand Transfer Sequences

A Slave Processor operand is transferred in one or more Slave bus cycles. A Byte operand is transferred on the least-significant byte of the Data Bus (AD0–AD7), and a Word operand is transferred on bits AD0–AD15. A Double Word is transferred in a consecutive pair of bus cycles, least-significant word first. A Quad Word is transferred in two pairs of Slave cycles, with other bus cycles possibly occurring between them. The word order is from least-significant word to most-significant.

Note that the NS32C032 uses only the two least significant bytes of the data bus for slave cycles. This is to maintain compatibility with existing slave processors.



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Note:

(1) Slave Processor samples Data Bus here.

(2) $\overline{DBE}$, being provided by the NS32C201 TCU, remains inactive due to the fact that no pulse is presented on $\overline{ADS}$. TCU signals $\overline{RD}$, $\overline{WR}$ and $\overline{TSO}$ also remain inactive.

FIGURE 3-14. CPU Write to Slave Processor

3.0 Functional Description (Continued)

3.5 MEMORY MANAGEMENT OPTION

The NS32C032 CPU, in conjunction with the NS32082 Memory Management Unit (MMU), provides full support for address translation, memory protection, and memory allocation techniques up to and including Virtual Memory.

3.5.1 Address Translation Strap

The Bus Interface Control section of the NS32C032 CPU has two bus timing modes: With or Without Address Translation. The mode of operation is selected by the CPU by sampling the $\overline{AT}/\overline{SPC}$ (Address Translation/Slave Processor Control) pin on the rising edge of the $\overline{RST}$ (Reset) pulse.

If $\overline{AT}/\overline{SPC}$ is sampled as high, the bus timing is as previously described in Sec. 3.4. If it is sampled as low, two changes occur:

1) An extra clock cycle, Tmmu, is inserted into all bus cycles except Slave Processor transfers.
2) The $\overline{DS}/\overline{FLT}$ pin changes in function from a Data Strobe output ($\overline{DS}$) to a Float Command input ($\overline{FLT}$).

The NS32082 MMU will itself pull the CPU $\overline{AT}/\overline{SPC}$ pin low when it is reset. In non-Memory-Managed systems this pin should be pulled up to V_{CC} through a 10 kΩ resistor.

Note that the Address Translation strap does not specifical-

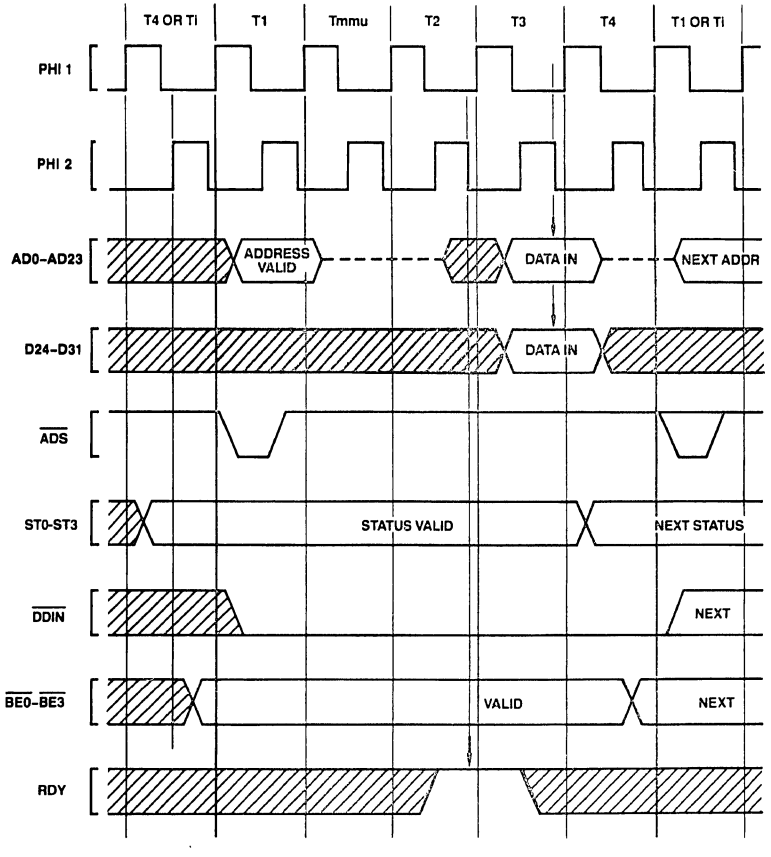

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FIGURE 3-15. Read Cycle with Address Translation (CPU Action)

3.0 Functional Description (Continued)

ly declare the presence of an NS32082 MMU, but only the presence of external address translation circuitry. MMU instructions will still trap as being undefined unless the SETCFG (Set Configuration) instruction is executed to declare the MMU instruction set valid. See Sec. 2.1.3.

3.5.2 Translated Bus Timing

Figures 3-15 and *3-16* illustrate the CPU activity during a Read cycle and a Write cycle in Address Translation mode. The additional T-State, Tmmu, is inserted between T1 and T2. During this time the CPU places AD0–AD23 into the TRI-STATE® mode, allowing the MMU to assert the translated address and issue the physical address strobe $\overline{PAV}$. T2 through T4 of the cycle are identical to their counterparts without Address Translation. Note that in order for the NS32082 MMU to operate correctly it must be set to the 32032 mode by forcing A24/$\overline{HBF}$ low during reset. In this mode the bus lines AD16–AD23 are floated after the MMU address has been latched, since they are used by the CPU to transfer data.

Figures 3-17 and *3-18* show a Read cycle and a Write cycle as generated by the 32C032/32082/32C201 group. Note that with the CPU $\overline{ADS}$ signal going only to the MMU, and with the MMU $\overline{PAV}$ signal substituting for $\overline{ADS}$ everywhere else, Tmmu through T4 look exactly like T1 through T4 in a non-Memory-Managed system. For the connection diagram, see Appendix B.

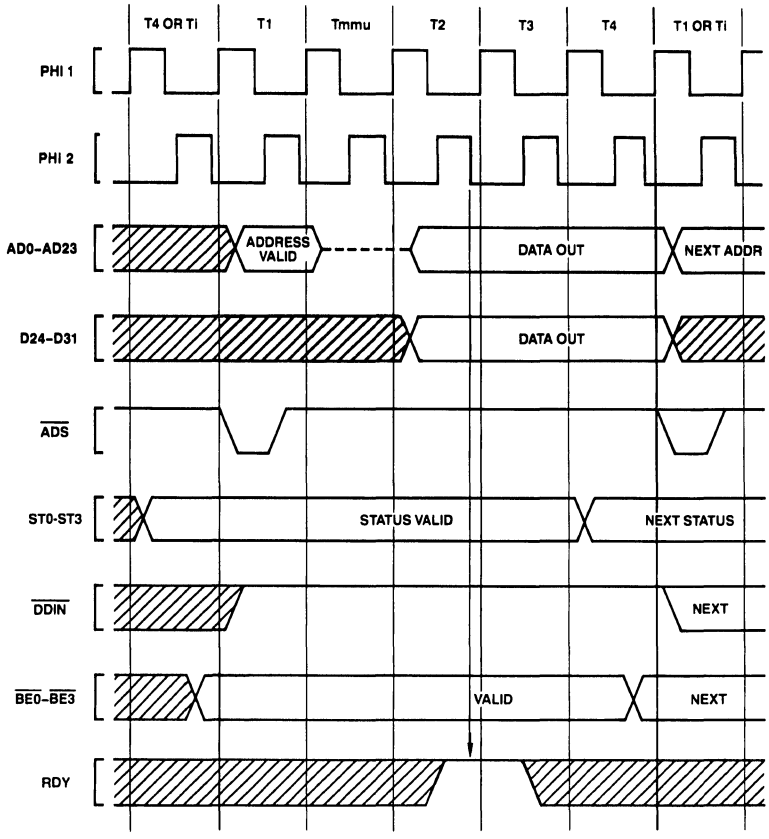

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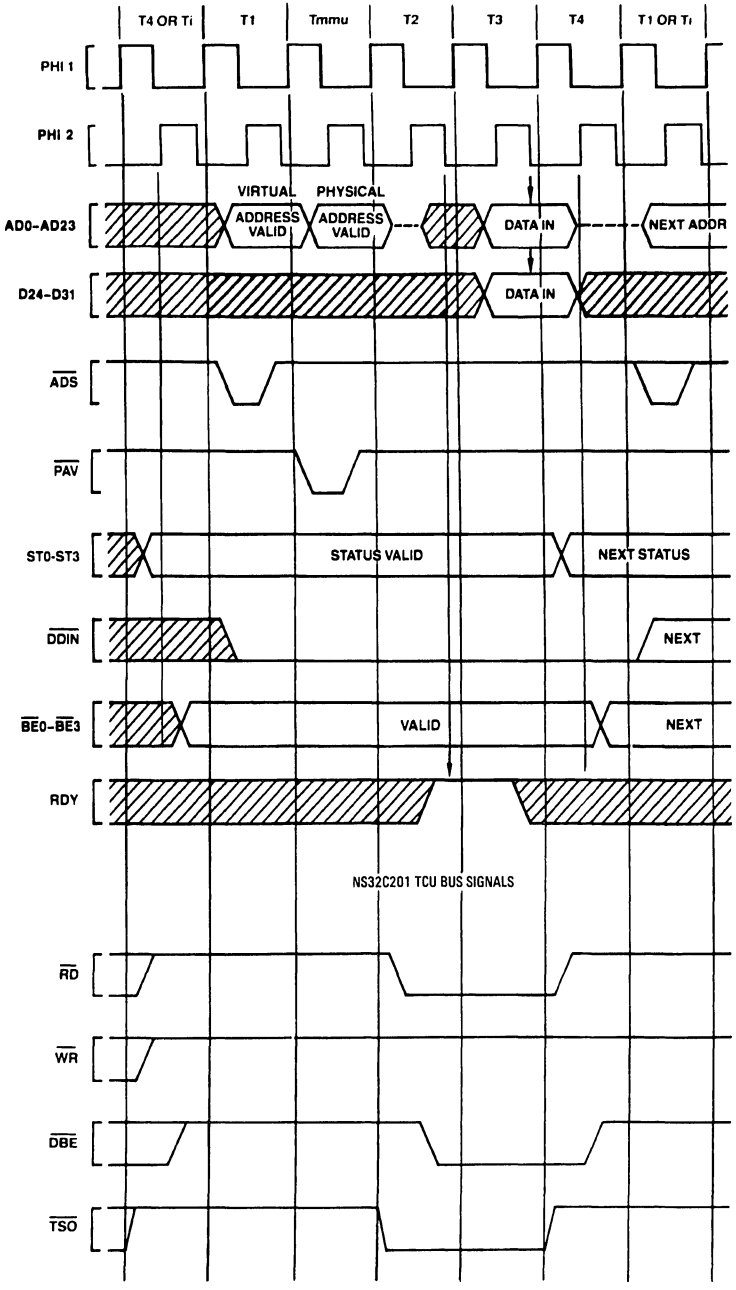
FIGURE 3-16. Write Cycle with Address Translation (CPU Action)

3.0 Functional Description (Continued)



TL/EE/9160–29

FIGURE 3-17. Memory-Managed Read Cycle

3.0 Functional Description (Continued)

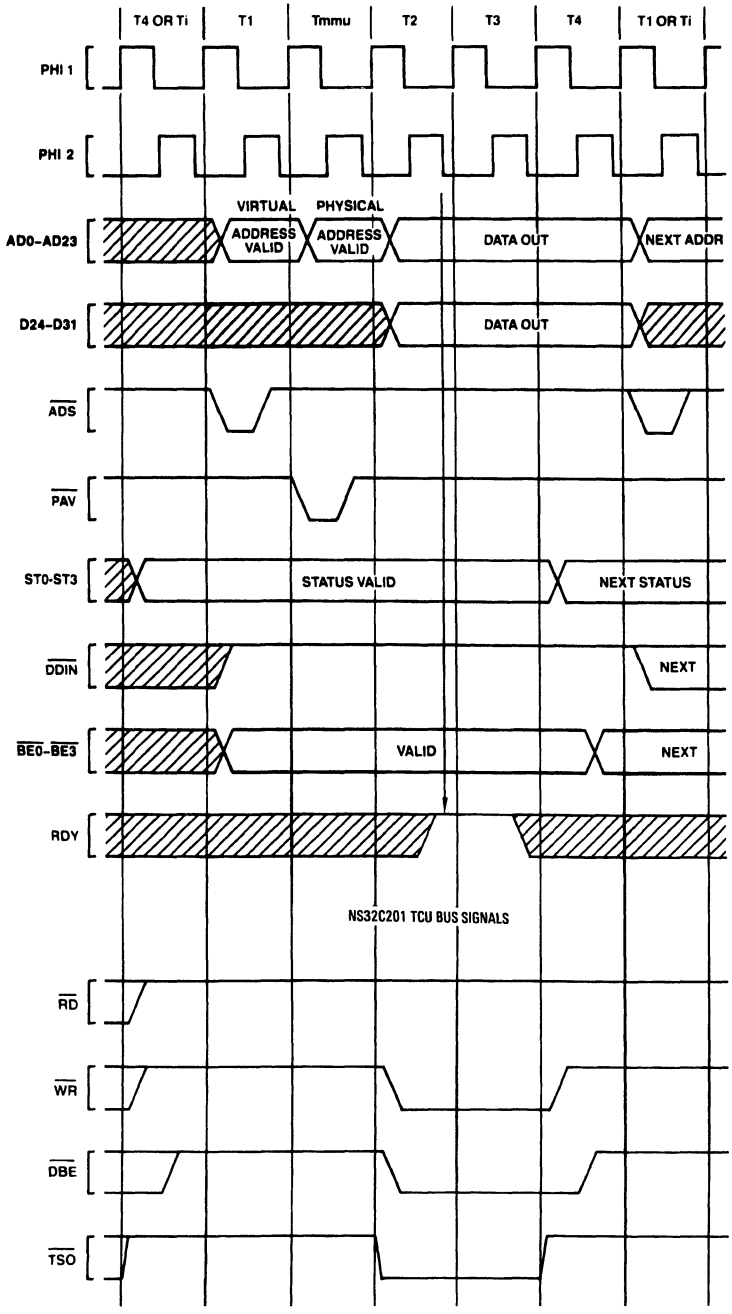


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FIGURE 3-18. Memory-Managed Write Cycle

3.0 Functional Description (Continued)

3.5.3 The $\overline{FLT}$ (Float) Pin

The $\overline{FLT}$ pin is used by the CPU for address translation support. Activating $\overline{FLT}$ during Tmmu causes the CPU to wait longer than Tmmu for address translation and validation. This feature is used occasionally by the NS32082 MMU in order to update its translation look-aside buffer (TLB) from page tables in memory, or to update certain status bits within them.

Figure 3-19 shows the effect of $\overline{FLT}$. Upon sampling $\overline{FLT}$ low, late in Tmmu, the CPU enters idle T-States (Tf) during which it:

1) Sets AD0–AD23, D24–D31 and $\overline{DDIN}$ to the TRI-STATE condition ("floating").
2) Suspends further internal processing of the current instruction. This ensures that the current instruction remains abortable with retry. (See $\overline{RST}/\overline{ABT}$ description, Sec. 3.5.4.)

Note that the AD0–AD23 pins may be briefly asserted during the first idle T-State. The above conditions remain in effect until $\overline{FLT}$ again goes high. See the Timing Specifications, Sec. 4.

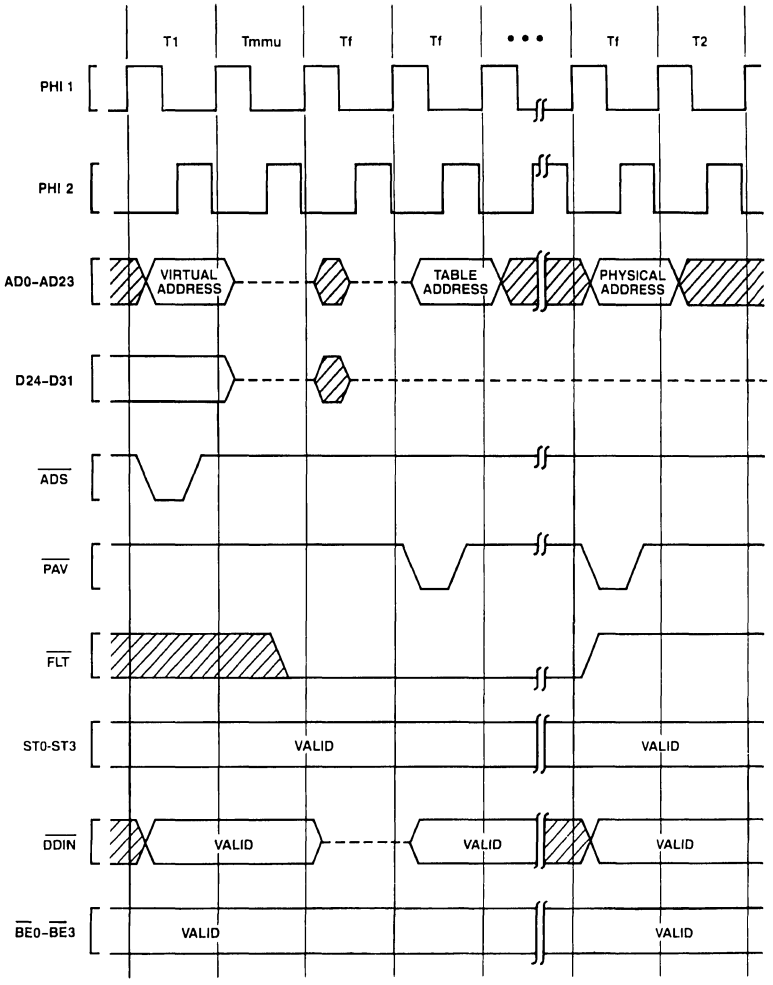

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FIGURE 3-19. $\overline{FLT}$ Timing

3.0 Functional Description (Continued)

3.5.4 Aborting Bus Cycles

The $\overline{RST}/\overline{ABT}$ pin, apart from its Reset function (Sec. 3.3), also serves as the means to "abort", or cancel, a bus cycle and the instruction, if any, which initiated it. An Abort request is distinguished from a Reset in that the $\overline{RST}/\overline{ABT}$ pin is held active for only one clock cycle.

If $\overline{RST}/\overline{ABT}$ is pulled low during Tmmu or Tf, this signals that the cycle must be aborted. The CPU itself will enter T2 and then Ti, thereby terminating the cycle. Since it is the MMU $\overline{PAV}$ signal which triggers a physical cycle, the rest of the system remains unaware that a cycle was started.

The NS32082 MMU will abort a bus cycle for either of two reasons:

1) The CPU is attempting to access a virtual address which is not currently resident in physical memory. The referenced page must be brought into physical memory from mass storage to make it accessible to the CPU.
2) The CPU is attempting to perform an access which is not allowed by the protection level assigned to that page.

When a bus cycle is aborted by the MMU, the instruction that caused it to occur is also aborted in such a manner that it is guaranteed re-executable later. The information that is changed irrecoverably by such a partly-executed instruction does not affect its re-execution.

3.5.4.1 The Abort Interrupt

Upon aborting an instruction, the CPU immediately performs an interrupt through the ABT vector in the Interrupt Table (see Sec. 3.8). The Return Address pushed on the Interrupt Stack is the address of the aborted instruction, so that a Return from Trap (RETT) instruction will automatically retry it.

The one exception to this sequence occurs if the aborted bus cycle was an instruction prefetch. If so, it is not yet certain that the aborted prefetched code is to be executed. Instead of causing an interrupt, the CPU only aborts the bus cycle, and stops prefetching. If the information in the Instruction Queue runs out, meaning that the instruction will actually be executed, the ABT interrupt will occur, in effect aborting the instruction that was being fetched.

3.5.4.2 Hardware Considerations

In order to guarantee instruction retry, certain rules must be followed in applying an Abort to the CPU. These rules are followed by the NS32082 Memory Management Unit.

1) If $\overline{FLT}$ has not been applied to the CPU, the Abort pulse must occur during or before Tmmu. See the Timing Specifications, *Figure 4-22*.
2) If $\overline{FLT}$ has been applied to the CPU, the Abort pulse must be applied before the T-State in which $\overline{FLT}$ goes inactive. The CPU will not actually respond to the Abort command until $\overline{FLT}$ is removed. See *Figure 4-23*.
3) The Write half of a Read-Modify-Write operand access may not be aborted. The CPU guarantees that this will never be necessary for Memory Management functions by applying a special RMW status (Status Code 1011) during the Read half of the access. When the CPU presents RMW status, that cycle must be aborted if it would be illegal to write to any of the accessed addresses.

If $\overline{RST}/\overline{ABT}$ is pulsed at any time other than as indicated above, it will abort either the instruction currently under execution or the next instruction and will act as a very high-priority interrupt. However, the program that was running at the time is not guaranteed recoverable.

3.6 BUS ACCESS CONTROL

The NS32C032 CPU has the capability of relinquishing its access to the bus upon request from a DMA device or another CPU. This capability is implemented on the $\overline{HOLD}$ (Hold Request) and $\overline{HLDA}$ (Hold Acknowledge) pins. By asserting HOLD low, an external device requests access to the bus. On receipt of $\overline{HLDA}$ from the CPU, the device may perform bus cycles, as the CPU at this point has set the AD0–AD23, D24–D31, $\overline{ADS}$, $\overline{DDIN}$ and $\overline{BE0}$–$\overline{BE3}$ pins to the TRI-STATE condition. To return control of the bus to the CPU, the device sets $\overline{HOLD}$ inactive, and the CPU acknowledges return of the bus by setting $\overline{HLDA}$ inactive.

How quickly the CPU releases the bus depends on whether it is idle on the bus at the time the $\overline{HOLD}$ request is made, as the CPU must always complete the current bus cycle. *Figure 3-20* shows the timing sequence when the CPU is idle. In this case, the CPU grants the bus during the immediately following clock cycle. *Figure 3-21* shows the sequence if the CPU is using the bus at the time that the $\overline{HOLD}$ request is made. If the request is made during or before the clock cycle shown (two clock cycles before T4), the CPU will release the bus during the clock cycle following T4. If the request occurs closer to T4, the CPU may already have decided to initiate another bus cycle. In that case it will not grant the bus until after the next T4 state. Note that this situation will also occur if the CPU is idle on the bus but has initiated a bus cycle internally.

In a Memory-Managed system, the $\overline{HLDA}$ signal is connected in a daisy-chain through the NS32082, so that the MMU can release the bus if it is using it.

3.0 Functional Description (Continued)

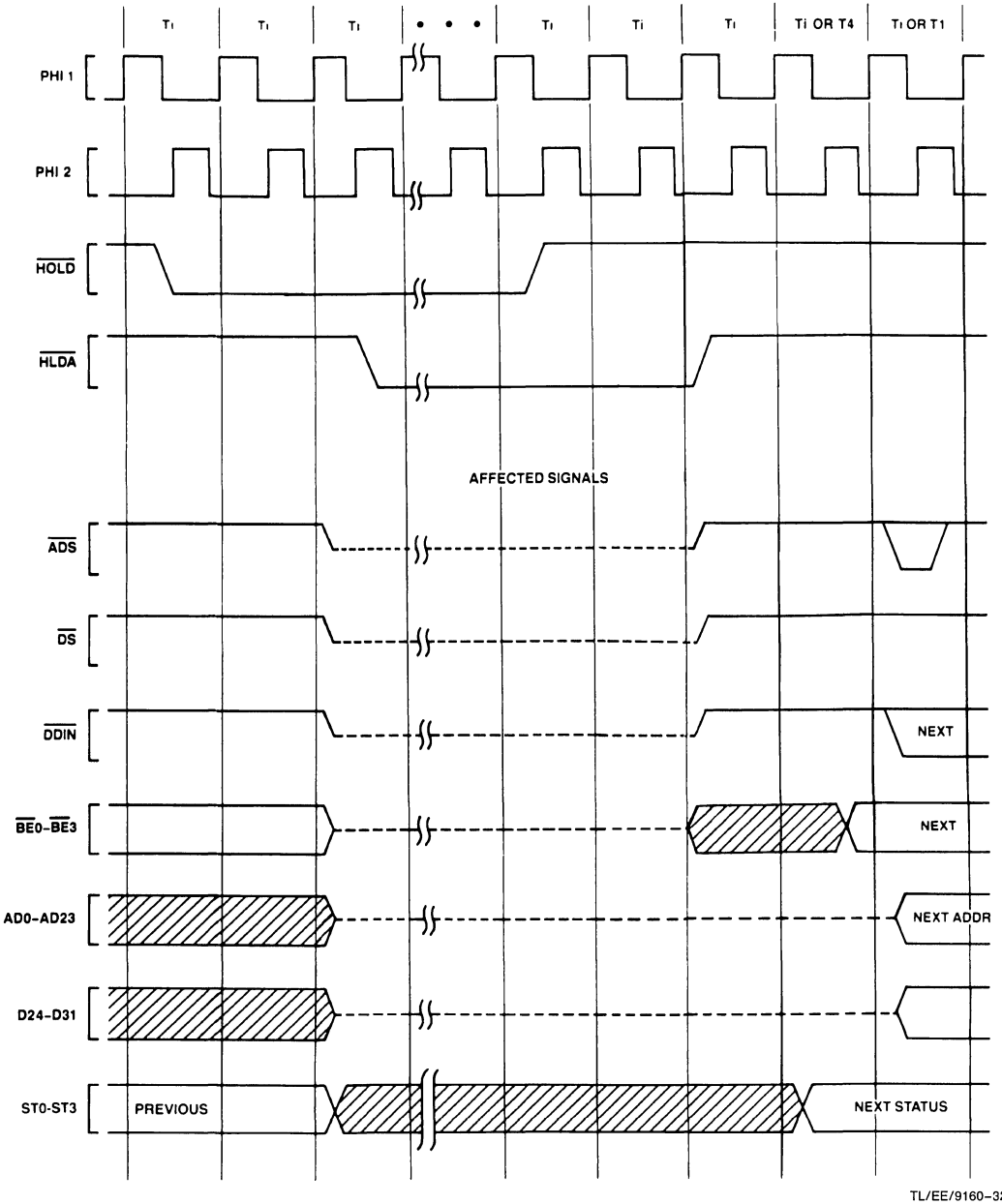

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FIGURE 3-20. HOLD Timing, Bus Initially Idle

3.0 Functional Description (Continued)

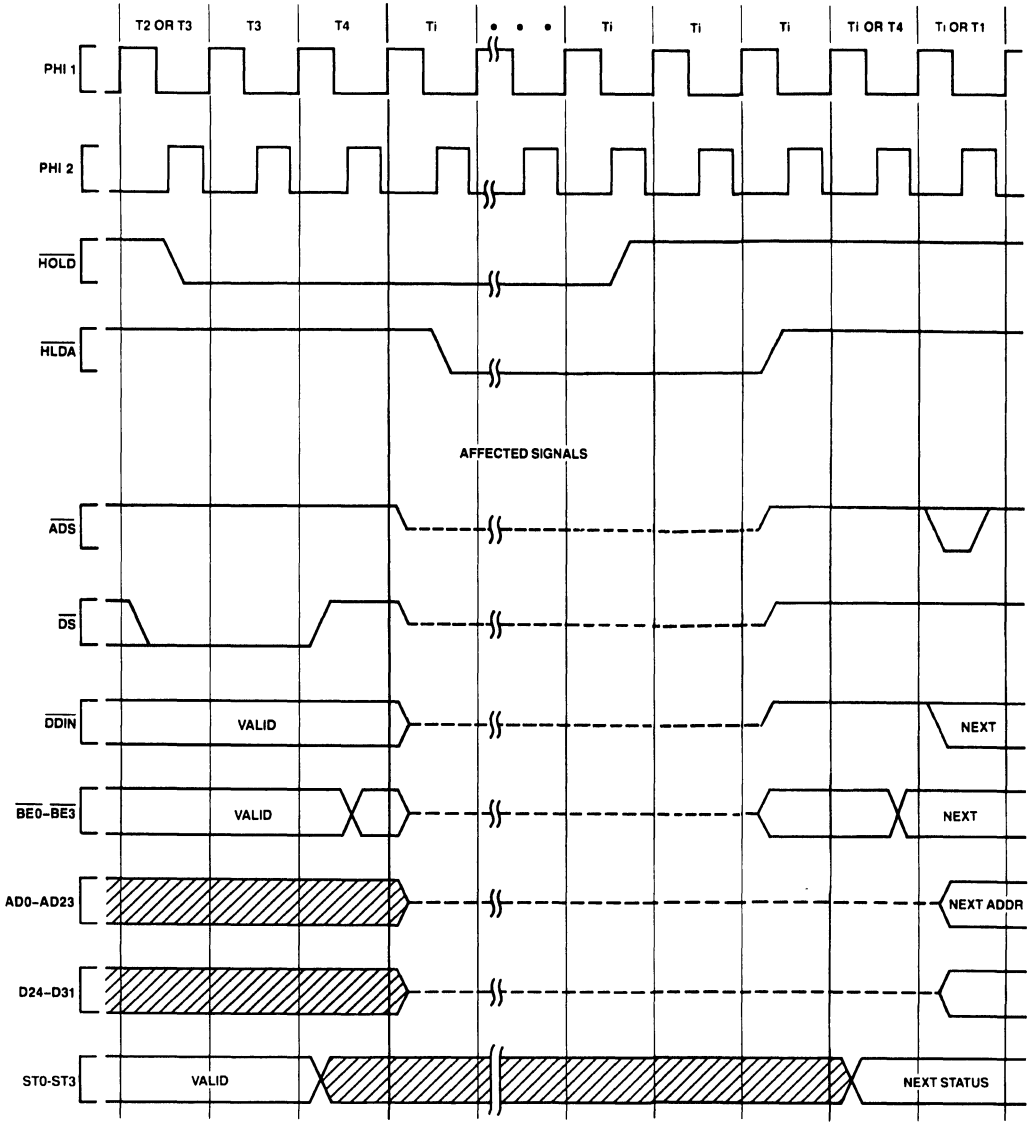

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FIGURE 3-21. HOLD Timing, Bus Initially Not Idle

3.0 Functional Description (Continued)

3.7 INSTRUCTION STATUS

In addition to the four bits of Bus Cycle status (ST0–ST3), the NS32C032 CPU also presents Instruction Status information on three separate pins. These pins differ from ST0–ST3 in that they are synchronous to the CPU's internal instruction execution section rather than to its bus interface section.

$\overline{PFS}$ (Program Flow Status) is pulsed low as each instruction begins execution. It is intended for debugging purposes, and is used that way by the NS32082 Memory Management Unit.

U/$\overline{S}$ originates from the U bit of the Processor Status Register, and indicates whether the CPU is currently running in User or Supervisor mode. It is sampled by the MMU for mapping, protection, and debugging purposes. Although it is not synchronous to bus cycles, there are guarantees on its validity during any given bus cycle. See the Timing Specifications, *Figure 4-21*.

$\overline{ILO}$ (Interlocked Operation) is activated during an SBITI (Set Bit, Interlocked) or CBITI (Clear Bit, Interlocked) instruction. It is made available to external bus arbitration circuitry in order to allow these instructions to implement the semaphore primitive operations for multi-processor communication and resource sharing. As with the U/$\overline{S}$ pin, there are guarantees on its validity during the operand accesses performed by the instructions. See the Timing Specification Section, *Figure 4-19*.

3.8 NS32C032 INTERRUPT STRUCTURE

$\overline{INT}$, on which maskable interrupts may be requested,

$\overline{NMI}$, on which non-maskable interrupts may be requested, and

$\overline{RST}$/$\overline{ABT}$, which may be used to abort a bus cycle and any associated instruction. See Sec. 3.5.4.

In addition there is a set of internally-generated "traps" which cause interrupt service to be performed as a result either of exceptional conditions (e.g., attempted division by zero) or of specific instructions whose purpose is to cause a trap to occur (e.g., the Supervisor Call instruction).

3.8.1 General Interrupt/Trap Sequence

Upon receipt of an interrupt or trap request, the CPU goes through three major steps:

1) Adjustment of Registers.

   Depending on the source of the interrupt or trap, the CPU may restore and/or adjust the contents of the Program Counter (PC), the Processor Status Register (PSR) and the currently-selected Stack Pointer (SP). A copy of the PSR is made, and the PSR is then set to reflect Supervisor Mode and selection of the Interrupt Stack.

2) Vector Acquisition.

   A Vector is either obtained from the Data Bus or is supplied by default.

3) Service Call.

   The Vector is used as an index into the Interrupt Dispatch Table, whose base address is taken from the CPU Interrupt Base (INTBASE) Register. See *Figure 3-22*. A 32-bit External Procedure Descriptor is read from the table entry, and an External Procedure Call is performed using it. The MOD Register (16 bits) and Program Counter (32 bits) are pushed on the Interrupt Stack.

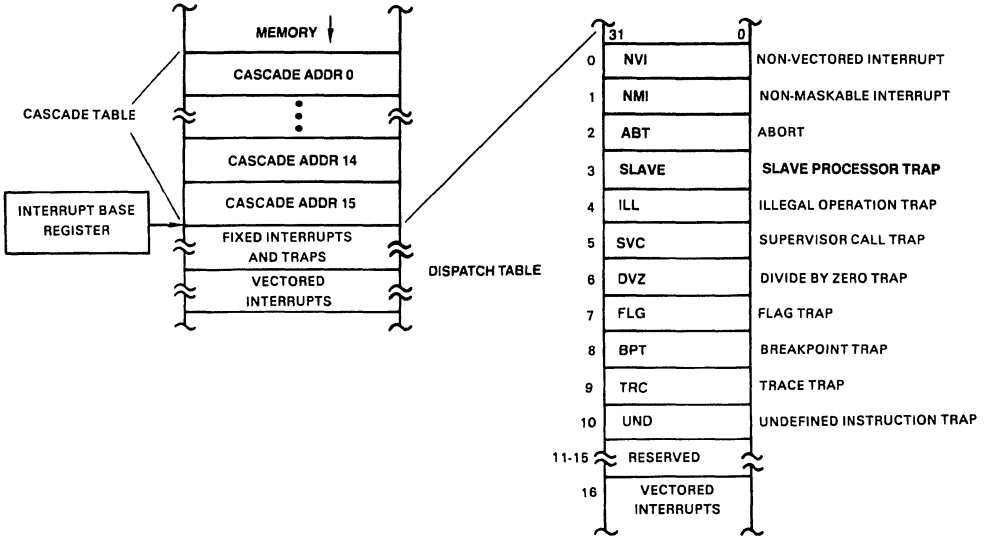

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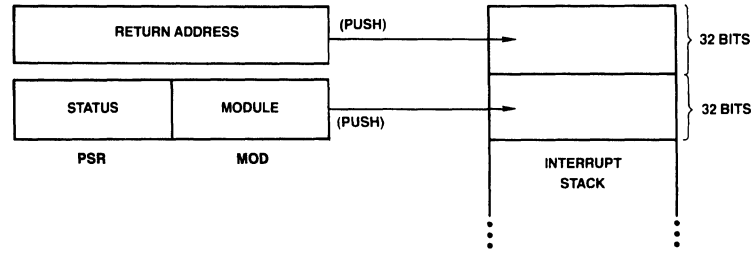
FIGURE 3-22. Interrupt Dispatch and Cascade Tables

3.0 Functional Description (Continued)

This process is illustrated in *Figure 3-23*, from the viewpoint of the programmer.



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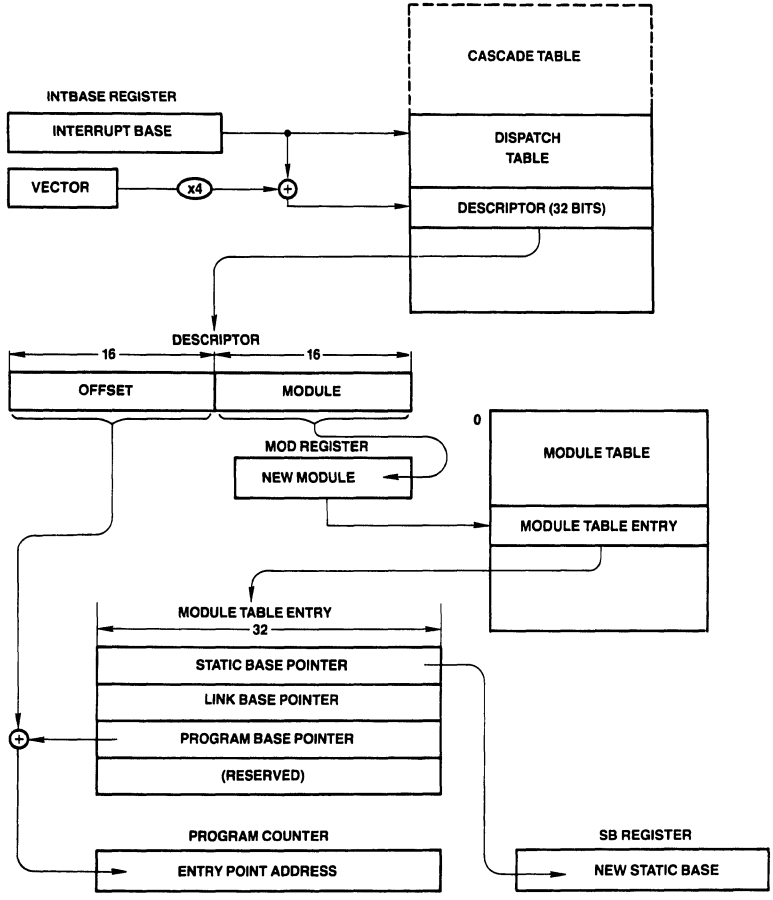

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FIGURE 3-23. Interrupt/Trap Service Routine Calling Sequence

3.0 Functional Description (Continued)

3.8.2 Interrupt/Trap Return

To return control to an interrupted program, one of two instructions is used. The RETT (Return from Trap) instruction (*Figure 3-24*) restores the PSR, MOD, PC and SB registers to their previous contents and, since traps are often used deliberately as a call mechanism for Supervisor Mode procedures, it also discards a specified number of bytes from the original stack as surplus parameter space. RETT is used to return from any trap or interrupt except the Maskable Interrupt. For this, the RETI (Return from Interrupt) instruction is used, which also informs any external Interrupt Control Units that interrupt service has completed. Since interrupts are generally asynchronous external events, RETI does not pop parameters. See *Figure 3-25*.

3.8.3 Maskable Interrupts (The $\overline{\text{INT}}$ Pin)

The $\overline{\text{INT}}$ pin is a level-sensitive input. A continuous low level is allowed for generating multiple interrupt requests. The input is maskable, and is therefore enabled to generate interrupt requests only while the Processor Status Register I bit is set. The I bit is automatically cleared during service of an $\overline{\text{INT}}$, $\overline{\text{NMI}}$ or Abort request, and is restored to its original setting upon return from the interrupt service routine via the RETT or RETI instruction.

The $\overline{\text{INT}}$ pin may be configured via the SETCFG instruction as either Non-Vectored (CFG Register bit I = C) or Vectored (bit I = 1).

3.8.3.1 Non-Vectored Mode

In the Non-Vectored mode, an interrupt request on the $\overline{\text{INT}}$ pin will cause an Interrupt Acknowledge bus cycle, but the CPU will ignore any value read from the bus and use instead a default vector of zero. This mode is useful for small systems in which hardware interrupt prioritization is unnecessary.

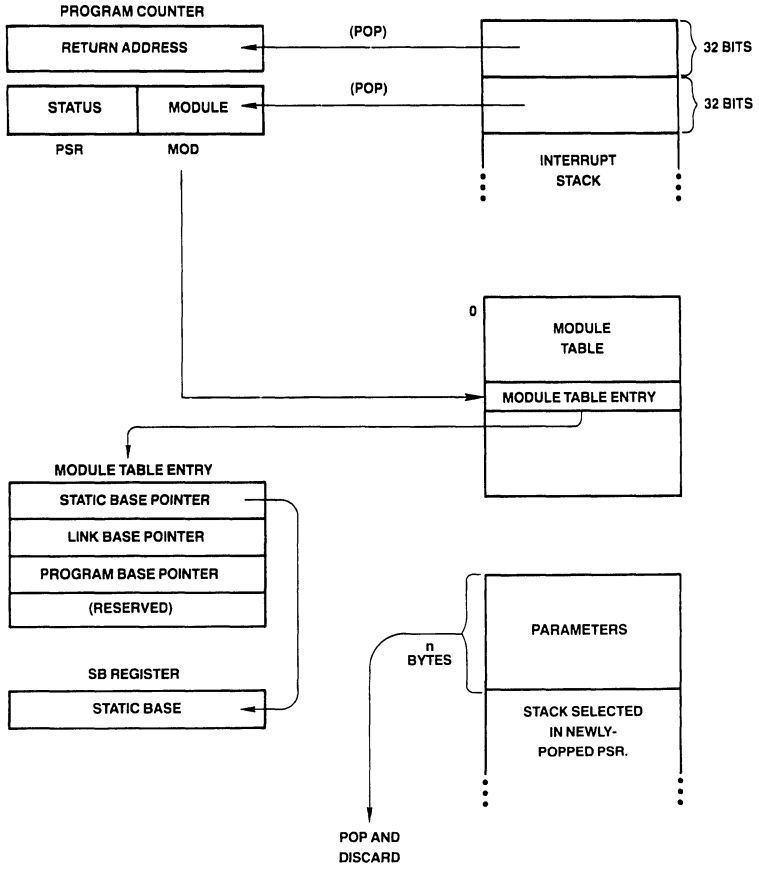

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FIGURE 3-24. Return from Trap (RETT n) Instruction Flow

3.0 Functional Description (Continued)

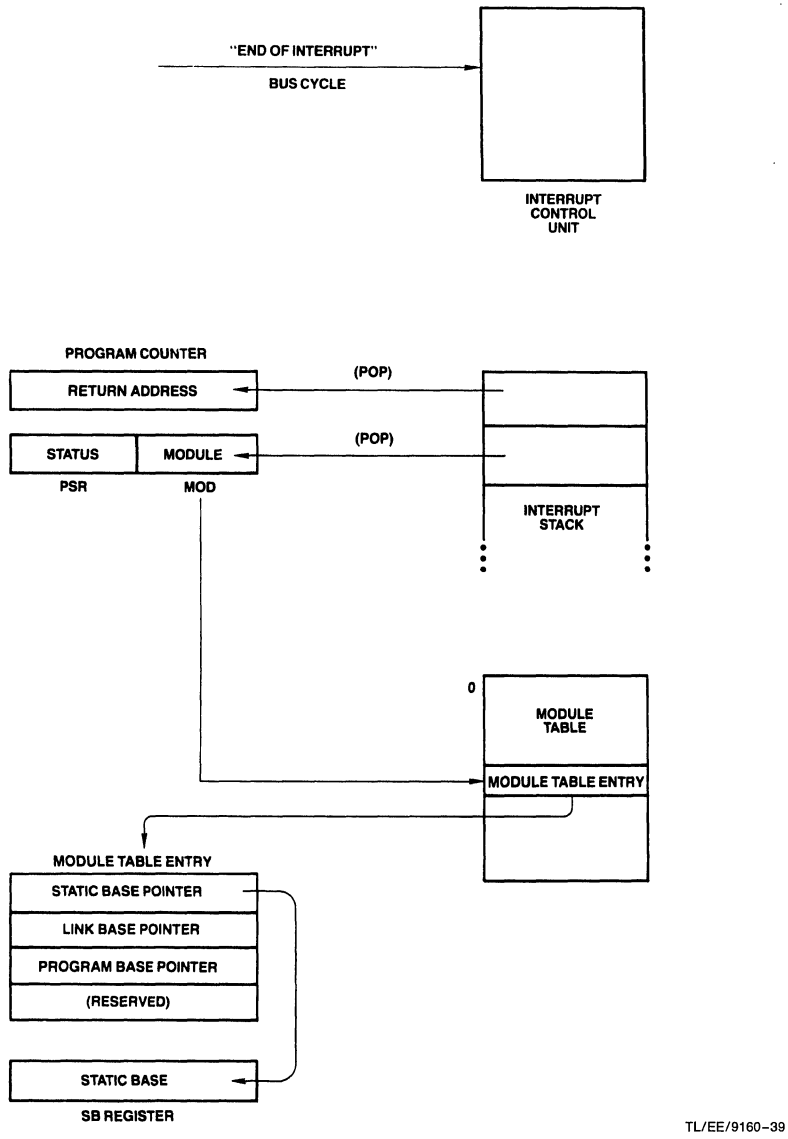

FIGURE 3-25. Return from Interrupt (RETI) Instruction Flow

3.0 Functional Description (Continued)

3.8.3.2 Vectored Mode: Non-Cascaded Case

In the Vectored mode, the CPU uses an Interrupt Control Unit (ICU) to prioritize up to 16 interrupt requests. Upon receipt of an interrupt request on the $\overline{INT}$ pin, the CPU performs an "Interrupt Acknowledge, Master" bus cycle (Sec. 3.4.2) reading a vector value from the low-order byte of the Data Bus. This vector is then used as an index into the Dispatch Table in order to find the External Procedure Descriptor for the proper interrupt service procedure. The service procedure eventually returns via the Return from Interrupt (RETI) instruction, which performs an End of Interrupt bus cycle, informing the ICU that it may re-prioritize any interrupt requests still pending. The ICU provides the vector number again, which the CPU uses to determine whether it needs also to inform a Cascaded ICU (see below).

In a system with only one ICU (16 levels of interrupt), the vectors provided must be in the range of 0 through 127; that is, they must be positive numbers in eight bits. By providing a negative vector number, an ICU flags the interrupt source as being a Cascaded ICU (see below).

3.8.3.3 Vectored Mode: Cascaded Case

In order to allow up to 256 levels of interrupt, provision is made both in the CPU and in the NS32202 Interrupt Control Unit (ICU) to transparently support cascading. *Figure 3-27*, shows a typical cascaded configuration. Note that the Interrupt output from a Cascaded ICU goes to an Interrupt Request input of the Master ICU, which is the only ICU which drives the CPU $\overline{INT}$ pin.

In a system which uses cascading, two tasks must be performed upon initialization:

1) For each Cascaded ICU in the system, the Master ICU must be informed of the line number (0 to 15) on which it receives the cascaded requests.

2) A Cascade Table must be established in memory. The Cascade Table is located in a NEGATIVE direction from the location indicated by the CPU Interrupt Base (INTBASE) Register. Its entries are 32-bit addresses, pointing to the Vector Registers of each of up to 16 Cascaded ICUs.

Figure 3-22 illustrates the position of the Cascade Table. To find the Cascade Table entry for a Cascaded ICU, take its Master ICU line number (0 to 15) and subtract 16 from it, giving an index in the range −16 to −1. Multiply this value by 4, and add the resulting negative number to the contents of the INTBASE Register. The 32-bit entry at this address must be set to the address of the Hardware Vector Register of the Cascaded ICU. This is referred to as the "Cascade Address."

Upon receipt of an interrupt request from a Cascaded ICU, the Master ICU interrupts the CPU and provides the negative Cascade Table index instead of a (positive) vector number. The CPU, seeing the negative value, uses it as an index into the Cascade Table and reads the Cascade Address from the referenced entry. Applying this address, the CPU performs an "Interrupt Acknowledge, Cascaded" bus cycle (Sec. 3.4.2), reading the final vector value. This vector is interpreted by the CPU as an unsigned byte, and can therefore be in the range of 0 through 255.

In returning from a Cascaded interrupt, the service procedure executes the Return from Interrupt (RETI) instruction, as it would for any Maskable Interrupt. The CPU performs an "End of Interrupt, Master" bus cycle (Sec. 3.4.2), whereupon the Master ICU again provides the negative Cascade Table index. The CPU, seeing a negative value, uses it to find the corresponding Cascade Address from the Cascade Table. Applying this address, it performs an "End of Interrupt, Cascaded" bus cycle (Sec. 3.4.2), informing the Cascaded ICU of the completion of the service routine. The byte read from the Cascaded ICU is discarded.

Note: If an interrupt must be masked off, the CPU can do so by setting the corresponding bit in the Interrupt Mask Register of the Interrupt Controller.

However, if an interrupt is set pending during the CPU instruction that masks off that interrupt, the CPU may still perform an interrupt acknowledge cycle following that instruction since it might have sampled the $\overline{INT}$ line before the ICU deasserted it. This could cause the ICU to provide an invalid vector. To avoid this problem the above operation should be performed with the CPU interrupt disabled.

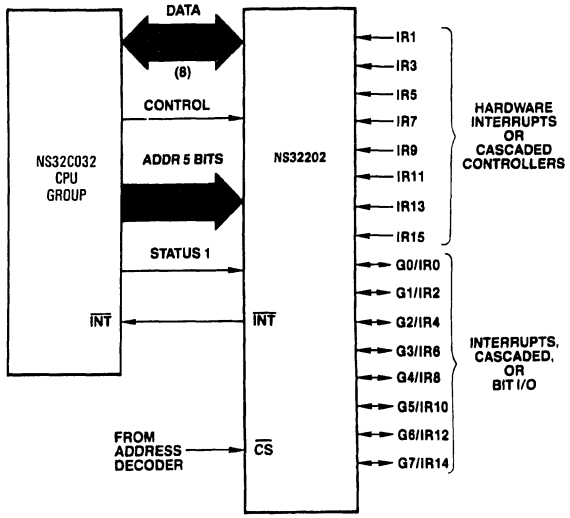

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FIGURE 3-26. Interrupt Control Unit Connections (16 Levels)

3.0 Functional Description (Continued)

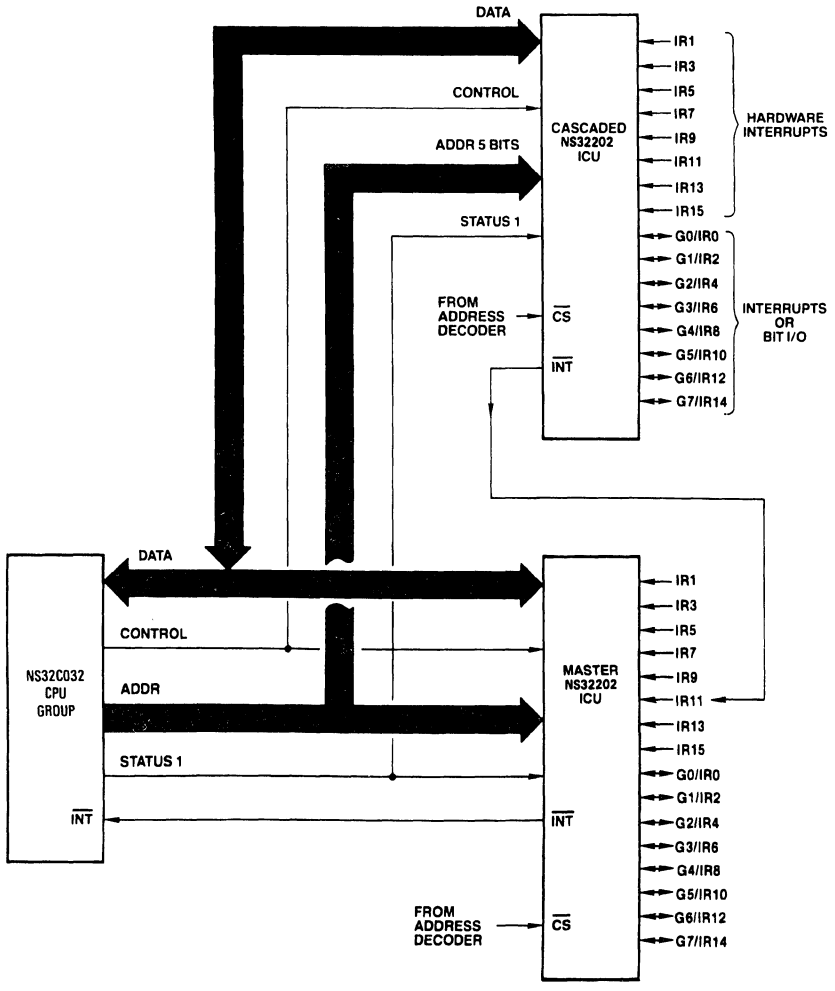

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FIGURE 3-27. Cascaded Interrupt Control Unit Connections

3.8.4 Non-Maskable Interrupt (The $\overline{\text{NMI}}$ Pin)

The Non-Maskable Interrupt is triggered whenever a falling edge is detected on the $\overline{\text{NMI}}$ pin. The CPU performs an "Interrupt Acknowledge, Master" bus cycle (Sec. 3.4.2) when processing of this interrupt actually begins. The Interrupt Acknowledge cycle differs from that provided for Maskable Interrupts in that the address presented is FFFF00_{16}. The vector value used for the Non-Maskable Interrupt is taken as 1, regardless of the value read from the bus.

The service procedure returns from the Non-Maskable Interrupt using the Return from Trap (RETT) instruction. No special bus cycles occur on return.

For the full sequence of events in processing the Non-Maskable Interrupt, see Sec. 3.8.7.1.

3.8.5 Traps

A trap is an internally-generated interrupt request caused as a direct and immediate result of the execution of an instruction. The Return Address pushed by any trap except Trap (TRC) is the address of the first byte of the instruction during which the trap occurred. Traps do not disable interrupts, as they are not associated with external events. Traps recognized by the NS32C032 CPU are:

Trap (SLAVE): An exceptional condition was detected by the Floating Point Unit or another Slave Processor during the execution of a Slave Instruction. This trap is requested via the Status Word returned as part of the Slave Processor Protocol (Sec. 3.9.1).

3.0 Functional Description (Continued)

Trap (ILL): Illegal operation. A privileged operation was attempted while the CPU was in User Mode (PSR bit U = 1).

Trap (SVC): The Supervisor Call (SVC) instruction was executed.

Trap (DVZ): An attempt was made to divide an integer by zero. (The FPU trap is used for Floating Point division by zero.)

Trap (FLG): The FLAG instruction detected a "1" in the CPU PSR F bit.

Trap (BPT): The Breakpoint (BPT) instruction was executed.

Trap (TRC): The instruction just completed is being traced. See below.

Trap (UND): An undefined opcode was encountered by the CPU.

A special case is the Trace Trap (TRC), which is enabled by setting the T bit in the Processor Status Register (PSR). At the beginning of each instruction, the T bit is copied into the PSR P (Trace "Pending") bit. If the P bit is set at the end of an instruction, then the Trace Trap is activated. If any other trap or interrupt request is made during a traced instruction, its entire service procedure is allowed to complete before the Trace Trap occurs. Each interrupt and trap sequence handles the P bit for proper tracing, guaranteeing one and only one Trace Trap per instruction, and guaranteeing that the Return Address pushed during a Trace Trap is always the address of the next instruction to be traced.

3.8.6 Prioritization

The NS32016 CPU internally prioritizes simultaneous interrupt and trap requests as follows:

1) Traps other than Trace (Highest priority)
2) Abort
3) Non-Maskable Interrupt
4) Maskable Interrupts
5) Trace Trap (Lowest priority)

3.8.7 Interrupt/Trap Sequences: Detailed Flow

For purposes of the following detailed discussion of interrupt and trap service sequences, a single sequence called "Service" is defined in *Figure 3-28*. Upon detecting any interrupt request or trap condition, the CPU first performs a sequence dependent upon the type of interrupt or trap. This sequence will include pushing the Processor Status Register and establishing a Vector and a Return Address. The CPU then performs the Service sequence.

For the sequence followed in processing either Maskable or Non-Maskable interrupts (on the $\overline{INT}$ or $\overline{NMI}$ pins, respectively), see Sec. 3.8.7.1 For Abort Interrupts, see Sec. 3.8.7.4. For the Trace Trap, see Sec. 3.8.7.3, and for all other traps see Sec. 3.8.7.2.

3.8.7.1 Maskable/Non-Maskable Interrupt Sequence

This sequence is performed by the CPU when the $\overline{NMI}$ pin receives a falling edge, or the $\overline{INT}$ pin becomes active with the PSR I bit set. The interrupt sequence begins either at the next instruction boundary or, in the case of the String instructions, at the next interruptible point during its execution.

1. If a String instruction was interrupted and not yet completed:
   a. Clear the Processor Status Register P bit.
   b. Set "Return Address" to the address of the first byte of the interrupted instruction.

   Otherwise, set "Return Address" to the address of the next instruction.
2. Copy the Processor Status Register (PSR) into a temporary register, then clear PSR bits S, U, T, P and I.
3. If the interrupt is Non-Maskable:
   a. Read a byte from address $FFFF00_{16}$, applying Status Code 0100 (Interrupt Acknowledge, Master, Sec. 3.4.2). Discard the byte read.
   b. Set "Vector" to 1.
   c. Go to Step 8.
4. If the interrupt is Non-Vectored:
   a. Read a byte from address $FFFF00_{16}$, applying Status Code 0100 (Interrupt Acknowledge, Master: Sec. 3.4.2). Discard the byte read.
   b. Set "Vector" to 0.
   c. Go to Step 8.
5. Here the interrupt is Vectored. Read "Byte" from address $FFFE00_{16}$, applying Status Code 0100 (Interrupt Acknowledge, Master: Sec. 3.4.2).
6. If "Byte" ≥ 0, then set "Vector" to "Byte" and go to Step 8.
7. If "Byte" is in the range -16 through -1, then the interrupt source is Cascaded. (More negative values are reserved for future use.) Perform the following:
   a. Read the 32-bit Cascade Address from memory. The address is calculated as INTBASE $+4*$ Byte.
   b. Read "Vector," applying the Cascade Address just read and Status Code 0101 (Interrupt Acknowledge, Cascaded: Sec. 3.4.2).
8. Push the PSR copy (from Step 2) onto the Interrupt Stack as a 16-bit value.
9. Perform Service (Vector, Return Address), *Figure 3-28*.

Service (Vector, Return Address):

1) Read the 32-bit External Procedure Descriptor from the Interrupt Dispatch Table: address is Vector* 4 + INTBASE Register contents.

2) Move the Module field of the Descriptor into the MOD Register.

3) Read the new Static Base pointer from the memory address contained in MOD, placing it into the SB Register.

4) Read the Program Base pointer from memory address MOD + 8, and add to it the Offset field from the Descriptor, placing the result in the Program Counter.

5) Flush queue: Non-sequentially fetch first instruction of interrupt routine.

6) Push MOD Register into the Interrupt Stack as a 16-bit value. (The PSR has already been pushed as a 16-bit value.)

7) Push the Return Address onto the Interrupt Stack as a 32-bit quantity.

FIGURE 3-28. Service Sequence

Invoked during all interrupt/trap sequences.

3.0 Functional Description (Continued)

3.8.7.2 Trap Sequence: Traps Other Than Trace

1) Restore the currently selected Stack Pointer and the Processor Status Register to their original values at the start of the trapped instruction.
2) Set "Vector" to the value corresponding to the trap type.
   - SLAVE: Vector = 3.
   - ILL: Vector = 4.
   - SVC: Vector = 5.
   - DVZ: Vector = 6.
   - FLG: Vector = 7.
   - BPT: Vector = 8.
   - UND: Vector = 10.
3) Copy the Processor Status Register (PSR) into a temporary register, then clear PSR bits S, U, P and T.
4) Push the PSR copy onto the Interrupt Stack as a 16-bit value.
5) Set "Return Address" to the address of the first byte of the trapped instruction.
6) Perform Service (Vector, Return Address), *Figure 3-28.*

3.8.7.3 Trace Trap Sequence

1) In the Processor Status Register (PSR), clear the P bit.
2) Copy the PSR into a temporary register, then clear PSR bits S, U and T.
3) Push the PSR copy onto the Interrupt Stack as a 16-bit value.
4) Set "Vector" to 9.
5) Set "Return Address" to the address of the next instruction.
6) Perform Service (Vector, Return Address), *Figure 3-28.*

3.8.7.4 Abort Sequence

1) Restore the currently selected Stack Pointer to its original contents at the beginning of the aborted instruction.
2) Clear the PSR P bit.
3) Copy the PSR into a temporary register, then clear PSR bits S, U, T and I.
4) Push the PSR copy onto the Interrupt Stack as a 16-bit value.
5) Set "Vector" to 2.
6) Set "Return Address" to the address of the first byte of the aborted instruction.
7) Perform Service (Vector, Return Address), *Figure 3-28.*

3.9 SLAVE PROCESSOR INSTRUCTIONS

The NS32C032 CPU recognizes three groups of instructions being executable by external Slave Processor:

Floating Point Instruction Set
Memory Management Instruction Set
Custom Instruction Set

Each Slave Instruction Set is validated by a bit in the Configuration Register (Sec. 2.1.3). Any Slave Instruction which does not have its corresponding Configuration Register bit set will trap as undefined, without any Slave Processor communication attempted by the CPU. This allows software simulation of a non-existent Slave Processor.

3.9.1 Slave Processor Protocol

Slave Processor instructions have a three-byte Basic Instruction field, consisting of an ID Byte followed by an Operation Word. The ID Byte has three functions:

1) It identifies the instruction as being a Slave Processor instruction.
2) It specifies which Slave Processor will execute it.
3) It determines the format of the following Operation Word of the instruction.

Upon receiving a Slave Processor instruction, the CPU initiates the sequence outlined in *Figure 3-29.* While applying Status Code 1111 (Broadcast ID, Sec. 3.4.2), the CPU transfers the ID Byte on the least-significant byte of the Data Bus (AD0–AD7). All Slave Processors input this byte and decode it. The Slave Processor selected by the ID Byte is activated, and from this point the CPU is communicating only with it. If any other slave protocol was in progress (e.g., an aborted Slave instruction), this transfer cancels it.

The CPU next sends the Operation Word while applying Status Code 1101 (Transfer Slave Operand, Sec. 3.4.2). Upon receiving it, the Slave Processor decodes it, and at this point both the CPU and the Slave Processor are aware of the number of operands to be transferred and their sizes. The operation Word is swapped on the Data Bus, that is, bits 0–7 appear on pins AD8–AD15 and bits 8–15 appear on pins AD0–AD7.

Using the Address Mode fields within the Operation Word, the CPU starts fetching operand and issuing them to the Slave Processor. To do so, it references any Addressing Mode extensions which may be appended to the Slave Processor instruction. Since the CPU is solely responsible

Status Combinations:

Send ID (ID): Code 1111
Xfer Operand (OP): Code 1101
Read Status (ST): Code 1110

Step	Status	Action
1	ID	CPU Send ID Byte.
2	OP	CPU Sends Operaton Word.
3	OP	CPY Sends Required Operands
4	—	Slave Starts Execution. CPU Pre-fetches.
5	—	Slave Pulses $\overline{SPC}$ Low.
6	ST	CPU Reads Status Word. (Trap? Alter Flags?)
7	OP	CPU Reads Results (If Any).

FIGURE 3-29. Slave Processor Protocol

3.0 Functional Description (Continued)

for memory accesses, these extensions are not sent to the Slave processor. The Status Code applied is 1101 (Transfer Slave Processor Operand, Sec. 3.4.2).

After the CPU has issued the last operand, the Slave Processor starts the actual execution of the instruction. Upon completion, it will signal the CPU by pulsing $\overline{SPC}$ low. To allow for this, and for the Address Translation strap function, $\overline{AT}/\overline{SPC}$ is normally held high only by an internal pull-up device of approximately 5 kΩ.

While the Slave Processor is executing the instruction, the CPU is free to prefetch instructions into its queue. If it fills the queue before the Slave Processor finishes, the CPU will wait, applying Status Code 0011 (Waiting for Slave, Sec. 3.4.2).

Upon receiving the pulse on $\overline{SPC}$, the CPU uses $\overline{SPC}$ to read a Status Word from the Slave Processor, applying Status Code 1110 (Read Slave Status, Sec. 3.4.2). This word has the format shown in *Figure 3-30*. If the Q bit ("Quit", Bit 0) is set, this indicates that an error was detected by the Slave Processor. The CPU will not continue the protocol, but will immediately trap through the Slave vector in the Interrupt Table. Certain Slave Processor instructions cause CPU PSR bits to be loaded from the Status Word.

The last step in the protocol is for the CPU to read a result, if any, and transfer it to the destination. The Read cycles from the Slave Processor are performed by the CPU while applying Status Code 1101 (Transfer Slave Operand, Sec. 3.4.2).

An exception to the protocol above is the LMR (Load Memory Management Register) instruction, and a corresponding Custom Slave instruction (LCR: Load Custom Register). In executing these instructions, the protocol ends after the CPU has issued the last operand. The CPU does not wait for an acknowledgement from the Slave Processor, and it does not read status.

3.9.2 Floating Point Instructions

Table 3-4 gives the protocols followed for each Floating Point instruction. The instructions are referenced by their mnemonics. For the bit encodings of each instruction, see Appendix A.

The Operand class columns give the Access Class for each general operand, defining how the addressing modes are interpreted (see Instruction Set Reference Manual).

The Operand Issued columns show the sizes of the operands issued to the Floating Point Unit by the CPU. "D" indicates a 32-bit Double Word. "i" indicates that the instruction specifies an integer size for the operand (B = Byte, W = Word, D = Double Word). "f" indicates that the instruction specifies a Floating Point size for the operand (F = 32-bit Standard Floating, L = 64-bit Long Floating).

The Returned Value Type and Destination column gives the size of any returned value and where the CPU places it. The PSR Bits Affected column indicates which PSR bits, if any, are updated from the Slave Processor Status Word (*Figure 3-30*).

TABLE 3-4
Floating Point Instruction Protocols.

Mnemonic	Operand 1 Class	Operand 2 Class	Operand 1 Issued	Operand 2 Issued	Returned Value Type and Dest.	PSR Bits Affected
ADDf	read.f	rmw.f	f	f	f to Op. 2	none
SUBf	read.f	rmw.f	f	f	f to Op. 2	none
MULf	read.f	rmw.f	f	f	f to Op. 2	none
DIVf	read.f	rmw.f	f	f	f to Op. 2	none
MOVf	read.f	write.f	f	N/A	f to Op. 2	none
ABSf	read.f	write.f	f	N/A	f to Op. 2	none
NEGf	read.f	write.f	f	N/A	f to Op. 2	none
CMPf	read.f	read.f	f	f	N/A	N,Z,L
FLOORfi	read.f	write.i	f	N/A	i to Op. 2	none
TRUNCfi	read.f	write.i	f	N/A	i to Op. 2	none
ROUNDfi	read.f	write.i	f	N/A	i to Op. 2	none
MOVFL	read.F	write.L	F	N/A	L to Op. 2	none
MOVLF	read.L	write.F	L	N/A	F to Op. 2	none
MOVif	read.i	write.f	i	N/A	f to Op. 2	none
LFSR	read.D	N/A	D	N/A	N/A	none
SFSR	N/A	write.D	N/A	N/A	D to Op. 2	none

Note:
D = Double Word
i = Integer size (B,W,D) specified in mnemonic.
f = Floating Point type (F,L) specified in mnemonic.
N/A = Not Applicable to this instruction.

3.0 Functional Description (Continued)

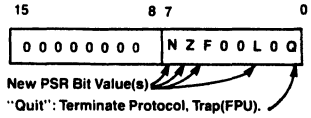

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FIGURE 3-30. Slave Processor Status Word Format

Any operand indicated as being of type "f" will not cause a transfer if the Register addressing mode is specified. This is because the Floating Point Registers are physically on the Floating Point Unit and are therefore available without CPU assistance.

3.9.3 Memory Management Instructions

Table 3-5 gives the protocols for Memory Management instructions. Encodings for these instructions may be found in Appendix A.

In executing the RDVAL and WRVAL instructions, the CPU calculates and issues the 32-bit Effective Address of the single operand. The CPU then performs a single-byte Read cycle from that address, allowing the MMU to safely abort the instruction if the necessary information is not currently in physical memory. Upon seeing the memory cycle complete, the MMU continues the protocol, and returns the validation result in the F bit of the Slave Status Word.

The size of a Memory Management operand is always a 32-bit Double Word. For further details of the Memory Management Instruction set, see the Instruction Set Reference Manual and the NS32082 MMU Data Sheet.

TABLE 3-5

Memory Management Instruction Protocols.

Mnemonic	Operand 1 Class	Operand 2 Class	Operand 1 Issued	Operand 2 Issued	Returned Value Type and Dest.	PSR Bits Affected
RDVAL*	addr	N/A	D	N/A	N/A	F
WRVAL*	addr	N/A	D	N/A	N/A	F
LMR*	read.D	N/A	D	N/A	N/A	none
SMR*	write.D	N/A	N/A	N/A	D to Op. 1	none

Note:

In the RDVAL and WRVAL instructions, the CPU issues the address as a Double Word, and performs a single-byte Read cycle from that memory address. For details, see the Instruction Set Reference Manual and the NS32082 Memory Management Unit Data Sheet.

D = Double Word

* = Privileged Instruction: will trap if CPU is in User Mode.

N/A = Not Applicable to this instruction.

3.0 Functional Description (Continued)

3.9.4 Custom Slave Instructions

Provided in the NS32C032 is the capability of communicating with a user-defined, "Custom" Slave Processor. The instruction set provided for a Custom Slave Processor defines the instruction formats, the operand classes and the communication protocol. Left to the user are the interpretations of the Op Code fields, the programming model of the Custom Slave and the actual types of data transferred. The protocol specifies only the size of an operand, not its data type.

Table 3-6 lists the relevant information for the Custom Slave instruction set. The designation "c" is used to represent an operand which can be a 32-bit ("D") or 64-bit ("Q") quantity in any format; the size is determined by the suffix on the mnemonic. Similarly, an "i" indicates an integer size (Byte, Word, Double Word) selected by the corresponding mnemonic suffix.

Any operand indicated as being of type "c" will not cause a transfer if the register addressing mode is specified. It is assumed in this case that the slave processor is already holding the operand internally.

For the instruction encodings, see Appendix A.

TABLE 3-6

Custom Slave Instruction Protocols.

Mnemonic	Operand 1 Class	Operand 2 Class	Operand 1 Issued	Operand 2 Issued	Returned Value Type and Dest.	PSR Bits Affected
CCAL0c	read.c	rmw.c	c	c	c to Op. 2	none
CCAL1c	read.c	rmw.c	c	c	c to Op. 2	none
CCAL2c	read.c	rmw.c	c	c	c to Op. 2	none
CCAL3c	read.c	rmw.c	c	c	c to Op. 2	none
CMOV0c	read.c	write.c	c	N/A	c to Op. 2	none
CMOV1c	read.c	write.c	c	N/A	c to Op. 2	none
CMOV2c	read.c	write.c	c	N/A	c to Op. 2	none
CMOV3c	read.c	write.c	c	N/A	c to Op.2	none
CCMP0c	read.c	read.c	c	c	N/A	N,Z,L
CCMP1c	read.c	read.c	c	c	N/A	N,Z,L
CCV0ci	read.c	write.i	c	N/A	i to Op. 2	none
CCV1ci	read.c	write.i	c	N/A	i to Op. 2	none
CCV2ci	read.c	write.i	c	N/A	i to Op. 2	none
CCV3ic	read.i	write.c	i	N/A	c to Op. 2	none
CCV4DQ	read.D	write.Q	D	N/A	Q to Op. 2	none
CCV5QD	read.Q	write.D	Q	N/A	D to Op. 2	none
LCSR	read.D	N/A	D	N/A	N/A	none
SCSR	N/A	write.D	N/A	N/A	D to OP. 2	none
CATST0*	addr	N/A	D	N/A	N/A	F
CATST1*	addr	N/A	D	N/A	N/A	F
LCR*	read.D	N/A	D	N/A	N/A	none
SCR*	write.D	N/A	N/A	N/A	D to Op.1	none

Note:

D = Double Word

i = Integer size (B,W,D) specified in mnemonic.

c = Custom size (D:32 bits or Q:64 bits) specified in mnemonic.

* = Privileged instruction: will trap if CPU is in User Mode.

N/A = Not Applicable to this instruction.

4.0 Device Specifications

4.1 NS32C032 PIN DESCRIPTIONS

The following is a brief description of all NS32C032 pins. The descriptions reference portions of the Functional Description. Sec. 3.

Unless otherwise indicated reserved pins should be left open.

4.1.1 Supplies

Logic Power ($V_{CCL1, 2}$): +5V positive supply.

Buffers Power ($V_{CCB1, 2}$): +5V positive supply.

Logic Ground (GNDL1, GNDL2): Ground reference for on-chip logic.

Buffer Grounds (GNDB1, GNDB2, GNDB3): Ground references for on-chip drivers.

4.1.2 Input Signals

Clocks (PHI1, PHI2): Two-phase clocking signals. Sec. 3.2.

Ready (RDY): Active high. While RDY is inactive, the CPU extends the current bus cycle to provide for a slower memory or peripheral reference. Upon detecting RDY active, the CPU terminates the bus cycle. Sec. 3.4.1.

Hold Request ($\overline{HOLD}$): Active low. Causes the CPU to release the bus for DMA or multiprocessing purposes. Sec. 3.6.

Note 1: $\overline{HOLD}$ must not be asserted until $\overline{HLDA}$ from a previous $\overline{HOLD}$/$\overline{HLDA}$ sequence is deasserted.

Note 2: If the $\overline{HOLD}$ signal is generated asynchronously, it's set up and hold times may be violated.

In this case it is recommended to synchronize it with CTTL to minimize the possibility of metastable states.

The CPU provides only one synchronization stage to minimize the $\overline{HLDA}$ latency. This is to avoid speed degradations in cases of heavy $\overline{HOLD}$ activity (i.e., DMA controller cycles interleaved with CPU cycles.)

Interrupt ($\overline{INT}$): Active low. Maskable Interrupt request. Sec. 3.8.

Non-Maskable Interrupt ($\overline{NMI}$): Active low. Non-Maskable Interrupt request. Sec. 3.8.

Reset/Abort ($\overline{RST}$/$\overline{ABT}$): Active low. If held active for one clock cycle and released, this pin causes an Abort Command, Sec. 3.5.4. If held longer, it initiates a Reset. Sec. 3.3.

4.1.3 Output Signals

Address Strobe ($\overline{ADS}$): Active low. Controls address latches: indicates start of a bus cycle. Sec. 3.4.

Data Direction in ($\overline{DDIN}$): Active low. Status signal indicating direction of data transfer during a bus cycle. Sec. 3.4.

Byte Enable ($\overline{BE0}$–$\overline{BE3}$): Active low. Four control signals enabling data transfers on individual bus bytes. Sec. 3.4.3.

Status (ST0–ST3): Bus cycle status code, ST0 least significant. Sec. 3.4.2. Encodings are:

0000 — Idle: CPU Inactive on Bus.
0001 — Idle: WAIT Instruction.
0010 — (Reserved).
0011 — Idle: Waiting for Slave.
0100 — Interrupt Acknowledge, Master.
0101 — Interrupt Acknowledge, Cascaded.
0110 — End of Interrupt, Master.
0111 — End of Interrupt, Cascaded.
1000 — Sequential Instruction Fetch.
1001 — Non-Sequential Instruction Fetch.
1010 — Data Transfer.
1011 — Read Read-Modify-Write Operand.
1100 — Read for Effective Address.
1101 — Transfer Slave Operand.
1110 — Read Slave Status Word.
1111 — Broadcast Slave ID.

Hold Acknowledge ($\overline{HLDA}$): Active low. Applied by the CPU in response to $\overline{HOLD}$ input, indicating that the bus has been released for DMA or multiprocessing purposes. Sec. 3.6.

User/Supervisor (U/$\overline{S}$): User or Supervisor Mode status. Sec. 3.7. High state indicates User Mode, low indicates Supervisor Mode. Sec. 3.7.

Interlocked Operation ($\overline{ILO}$): Active low. Indicates that an interlocked instruction is being executed. Sec. 3.7.

Program Flow Status ($\overline{PFS}$): Active low. Pulse indicates beginning of an instruction execution. Sec. 3.7.

4.1.4 Input-Output Signals

Address/Data 0–23 (AD0–AD23): Multiplexed Address/Data information. Bit 0 is the least significant bit of each. Sec. 3.4.

Data Bits 24–31 (D24–D31): The high order 8 bits of the data bus.

Address Translation/Slave Processor Control ($\overline{AT}$/$\overline{SPC}$): Active low. Used by the CPU as the data strobe output for Slave Processor transfers; used by Slave Processors to acknowledge completion of a slave instruction. Sec. 3.4.6; Sec. 3.9. Sampled on the rising edge of Reset pulse as Address Translation Strap. Sec. 3.5.1.

In non-memory-managed systems, this pin should be pulled-up to V_{CC} through a 10 kΩ resistor.

Data Strobe/Float ($\overline{DS}$/$\overline{FLT}$): Active low. Data Strobe output, Sec. 3.4, or Float Command input, Sec. 3.5.3. Pin function is selected on $\overline{AT}$/$\overline{SPC}$ pin, Sec. 3.5.1.

4.0 Device Specifications (Continued)

4.2 ABSOLUTE MAXIMUM RATINGS

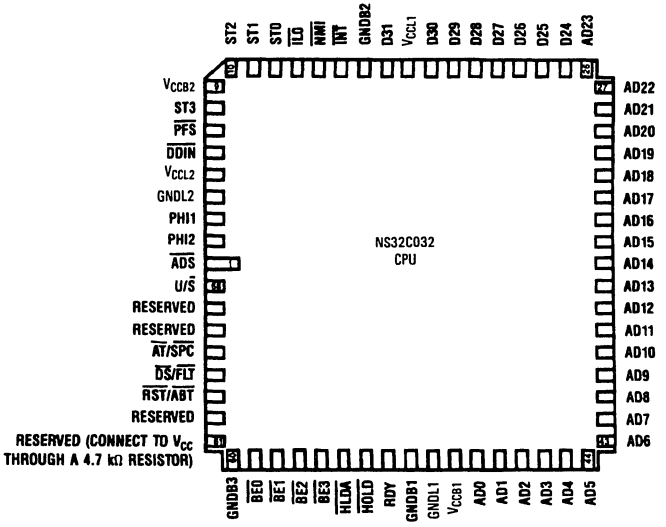
If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Temperature Under Bias	0°C to +70°C
Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to GND	−0.5V to +7V
Power Dissipation	1.5 Watt

Note: *Absolute maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended; operation should be limited to those conditions specified under Electrical Characteristics.*

4.3 ELECTRICAL CHARACTERISTICS T_A = 0° to +70°C, V_{CC} = 5V ±5%, GND = 0V

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High Level Input Voltage		2.0		V_{CC} +0.5	V
V_{IL}	Low Level Input Voltage		−0.5		0.8	V
V_{CH}	High Level Clock Voltage	PHI1, PHI2 pins only	0.85 V_{CC}		V_{CC} +0.5	V
V_{CL}	Low Level Clock Voltage	PHI1, PHI2 pins only	−0.5		0.10 V_{CC}	V
V_{CRT}	Clock Input Ringing Tolerance	PHI1, PHI2 pins only	−0.5		0.6	V
V_{OH}	High Level Output Voltage	I_{OH} = −400 μA	0.85 V_{CC}			V
V_{OL}	Low Level Output Voltage	I_{OL} = 2 mA			0.10 V_{CC}	V
I_{ILS}	$\overline{AT}/\overline{SPC}$ Input Current (low)	V_{IN} = 0.4V, $\overline{AT}/\overline{SPC}$ in input mode	0.05		1.0	mA
I_I	Input Load Current	0 ≤ V_{IN} ≤ V_{CC}, All inputs except PHI1, PHI2, $\overline{AT}/\overline{SPC}$	−20		20	μA
I_L	Leakage Current Output and I/O Pins in TRI-STATE/Input Mode	0.4 ≤ V_{OUT} ≤ V_{CC}	−20		20	μA
I_{CC}	Active Supply Current	I_{OUT} = 0, T_A = 25°C		70	100	mA



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Bottom View

FIGURE 4-1. NS32C032 Connection Diagram

Order Number NS32C032-10E, NS32C032-15E, NS32C032-10V or NS32C032-15V
See NS Package Number E68B or V68A

4.0 Device Specifications (Continued)

4.4 SWITCHING CHARACTERISTICS

4.4.1 Definitions

All the timing specifications given in this section refer to 2.0V on the rising or falling edges of the clock phases PHI1 and PHI2; to 15% or 85% of V_{CC} on all the CMOS output signals, and to 0.8V or 2.0V on all the TTL input signals as illustrated in *Figures 4-2* and *4-3* unless specifically stated otherwise.

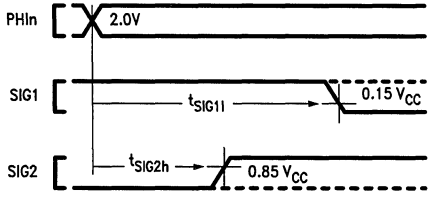

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FIGURE 4-2. Timing Specification Standard (CMOS Output Signals)

ABBREVIATIONS:

L.E. — leading edge R.E. — rising edge

T.E. — trailing edge F.E. — falling edge

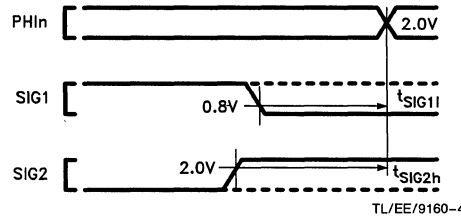

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FIGURE 4-3. Timing Specification Standard (TTL Input Signals)

4.4.2 Timing Tables

4.4.2.1 Output Signals: Internal Propagation Delays, NS32C032-10, NS32C032-15

Maximum times assume capacitive loading of 100 pF.

Name	Figure	Description	Reference/Conditions	NS32C032-10		NS32C032-15		Units
				Min	Max	Min	Max	
t_{ALv}	4-4	Address bits 0–23 valid	after R.E., PHI1 T1		40		35	ns
t_{ALh}	4-4	Address bits 0–23 hold	after R.E., PHI1 Tmmu or T2	5		5		ns
t_{Dv}	4-4	Data valid (write cycle)	after R.E., PHI1 T2		50		35	ns
t_{Dh}	4-4	Data hold (write cycle)	after R.E., PHI1 next T1 or Ti	0		0		ns
t_{ALADSs}	4-5	Address bits 0–23 setup	before $\overline{ADS}$ T.E.	25		20		ns
t_{ALADSh}	4-10	Address bits 0–23 hold	after $\overline{ADS}$ T.E.	15		10		ns
t_{ALf}	4-5	Address bits 0–23 floating (no MMU)	after R.E., PHI1 T2		25		20	ns
t_{ADf}	4-5	Data bits D24–D31 floating (no MMU)	after R.E., PHI1 T2		25		20	ns
t_{ALMf}	4-9	Address bits 0–23 floating (with MMU)	after R.E., PHI1 Tmmu		25		20	ns
t_{ADMf}	4-9	Data bits 21–31 floating (with MMU)	after R.E., PHI1 Tmmu		25		20	ns
t_{BEv}	4-4	$\overline{BEn}$ signals valid	after R.E., PHI2 T4		60		45	ns
t_{BEh}	4-4	$\overline{BEn}$ signals hold	after R.E., PHI2 T4 or Ti	0		0		ns
t_{STv}	4-4	Status (ST0–ST3) valid	after R.E., PHI1 T4 (before T1, see note)		45		35	ns
t_{STh}	4-4	Status (ST0–ST3) hold	after R.E., PHI1 T4 (after T1)	0		0		ns

4.0 Device Specifications (Continued)

4.4.2.1 Output Signals: Internal Propagation Delays, NS32C032-8, NS32C032-10 (Continued)

Name	Figure	Description	Reference/ Conditions	NS32C032-10		NS32C032-15		Units
				Min	Max	Min	Max	
t_{DDINv}	4-5	$\overline{DDIN}$ signal valid	after R.E., PHI1 T1		50		35	ns
t_{DDINh}	4-5	$\overline{DDIN}$ signal hold	after R.E., PHI1 next T1 or Ti	0		0		ns
t_{ADSa}	4-4	$\overline{ADS}$ signal active (low)	after R.E., PHI1 T1		35		26	ns
t_{ADSia}	4-4	$\overline{ADS}$ signal inactive	after R.E., PHI2 T1		40		30	ns
t_{ADSw}	4-4	$\overline{ADS}$ pulse width	at 15% V_{CC} (both edges)	30		25		ns
t_{DSa}	4-4	$\overline{DS}$ signal active (low)	after R.E., PHI1 T2		40		30	ns
t_{DSia}	4-4	$\overline{DS}$ signal inactive	after R.E., PHI1 T4		40		30	ns
t_{ALf}	4-6	AD0–AD23 floating (caused by $\overline{HOLD}$)	after R.E., PHI1 T1		25		20	ns
t_{ADf}	4-6	D24–D31 floating (caused by $\overline{HOLD}$)	after R.E., PHI1 T1		25		20	ns
t_{DSf}	4-6	$\overline{DS}$ floating (caused by $\overline{HOLD}$)	after R.E., PHI1 Ti		50		40	ns
t_{ADSf}	4-6	$\overline{ADS}$ floating (caused by $\overline{HOLD}$)	after R.E., PHI1 Ti		50		40	ns
t_{BEf}	4-6	$\overline{BEn}$ floating (caused by $\overline{HOLD}$)	after R.E., PHI1 Ti		50		40	ns
t_{DDINf}	4-6	$\overline{DDIN}$ floating (caused by $\overline{HOLD}$)	after R.E., PHI1 Ti		50		40	ns
t_{HLDAa}	4-6	$\overline{HLDA}$ signal active (low)	after R.E., PHI1 Ti		30		25	ns
t_{HLDAia}	4-8	$\overline{HLDA}$ signal inactive	after R.E., PHI1 Ti		40		30	ns
t_{DSr}	4-8	$\overline{DS}$ signal returns from floating (caused by $\overline{HOLD}$)	after R.E., PHI1 Ti		55		40	ns
t_{ADSr}	4-8	$\overline{ADS}$ signal returns from floating (caused by $\overline{HOLD}$)	after R.E., PHI1 Ti		55		40	ns
t_{BEr}	4-8	$\overline{BEn}$ signals return from floating (caused by $\overline{HOLD}$)	after R.E., PHI1 Ti		55		40	ns
t_{DDINr}	4-8	$\overline{DDIN}$ signal returns from floating (caused by $\overline{HOLD}$)	after R.E., PHI1 Ti		55		40	ns
t_{DDINf}	4-9	$\overline{DDIN}$ signal floating (caused by $\overline{FLT}$)	after $\overline{FLT}$ F.E.		55		50	ns
t_{DDINr}	4-10	$\overline{DDIN}$ signal returns from floating (caused by $\overline{FLT}$)	after $\overline{FLT}$ R.E.		40		30	ns
t_{SPCa}	4-13	$\overline{SPC}$ output active (low)	after R.E., PHI1 T1		35		26	ns
t_{SPCia}	4-13	$\overline{SPC}$ output inactive	after R.E., PHI1 T4		35		26	ns
t_{SPCnf}	4-15	$\overline{SPC}$ output nonforcing	after R.E., PHI2 T4		30		25	ns
t_{Dv}	4-13	Data valid (slave processor write)	after R.E., PHI1 T1		50		35	ns
t_{Dh}	4-13	Data hold (slave processor write)	after R.E., PHI1 next T1 or Ti	0		0		ns
t_{PFSw}	4-18	$\overline{PFS}$ pulse width	at 15% V_{CC} (both edges)	50		40		ns

4.0 Device Specifications (Continued)

4.4.2.1 Output Signals: Internal Propagation Delays, NS32C032-10, NS32C032-15 (Continued)

Name	Figure	Description	Reference/ Conditions	NS32C032-10		NS32C032-15		Units
				Min	Max	Min	Max	
t_{PFSa}	4-18	$\overline{PFS}$ pulse active (low)	after R.E., PHI2		40		35	ns
t_{PFSia}	4-18	$\overline{PFS}$ pulse inactive	after R.E., PHI2		40		35	ns
t_{ILOs}	4-20a	$\overline{ILO}$ signal setup	before R.E., PHI1 T1 of first interlocked read cycle	50		35		ns
t_{ILOh}	4-20b	$\overline{ILO}$ signal hold	after R.E., PHI1 T3 of last interlocked write cycle	10		7		ns
t_{ILOa}	4-21	$\overline{ILO}$ signal active (low)	after R.E., PHI1		35		30	ns
t_{ILOia}	4-21	$\overline{ILO}$ signal inactive	after R.E., PHI1		35		30	ns
t_{USv}	4-22	U/$\overline{S}$ signal valid	after R.E., PHI1 T4		35		30	ns
t_{USh}	4-22	U/$\overline{S}$ signal hold	after R.E., PHI1 T4	8		6		ns
t_{NSPF}	4-19b	Nonsequential fetch to next $\overline{PFS}$ clock cycle	after R.E., PHI1 T1	4		4		t_{Cp}
t_{PFNS}	4-19a	$\overline{PFS}$ clock cycle to next non-sequential fetch	before R.E., PHI1 T1	4		4		t_{Cp}
t_{LXPF}	4-29	Last operand transfer of an instruction to next $\overline{PFS}$ clock cycle	before R.E., PHI1 T1 of first of first bus cycle of transfer	0		0		t_{Cp}

Note: Every memory cycle starts with T4, during which Cycle Status is applied. If the CPU was idling, the sequence will be: " . . . Ti, T4, T1 . . . ". If the CPU was not idling, the sequence will be: " . . . T4, T1 . . . ".

4.4.2.2 Input Signal Requirements: NS32C032-10, NS32C032-15

Name	Figure	Description	Reference/Conditions	NS32C032-10		NS32C032-15		Units
				Min	Max	Min	Max	
t_{PWR}	4-25	Power stable to $\overline{RST}$ R.E.	after V_{CC} reaches 4.5V	50		50		μs
t_{DIs}	4-5	Data in setup (read cycle)	before F.E., PHI2 T3	15		10		ns
t_{DIh}	4-5	Data in hold (read cycle)	after R.E., PHI1 T4	3		3		ns
t_{HLDa}	4-6	$\overline{HOLD}$ active (low) setup time (see note)	before F.E., PHI2 TX1	25		17		ns
t_{HLDia}	4-8	$\overline{HOLD}$ inactive setup time	before F.E., PHI2 Ti	25		17		ns
t_{HLDh}	4-6	$\overline{HOLD}$ hold time	after R.E., PHI1 TX2	0		0		ns
t_{FLTa}	4-9	$\overline{FLT}$ active (low) setup time	before F.E., PHI2 Tmmu	25		17		ns
t_{FLTia}	4-10	$\overline{FLT}$ inactive setup time	before F.E., PHI2 T2	25		17		ns
t_{RDYs}	4-11, 4-12	RDY setup time	before F.E., PHI2 T2 or T3	15		10		ns
t_{RDYh}	4-11, 4-12	RDY hold time	after F.E., PHI1 T3	5		5		ns
t_{ABTs}	4-23	$\overline{ABT}$ setup time ($\overline{FLT}$ inactive)	before F.E., PHI2 Tmmu	20		13		ns
t_{ABTs}	4-24	$\overline{ABT}$ setup time ($\overline{FLT}$ active)	before F.E., PHI2 T_f	20		13		ns
t_{ABTh}	4-23	$\overline{ABT}$ hold time	after R.E., PHI1	0		0		ns

4.0 Device Specifications (Continued)

4.4.2.2 Input Signal Requirements NS32C032-10, NS32C032-15 (Continued)

Name	Figure	Description	Reference/ Conditions	NS32C032-10		NS32C032-15		Units
				Min	Max	Min	Max	
t_{RSTs}	4-25, 4-26	$\overline{RST}$ setup time	before F.E., PHI1	10		8		ns
t_{RSTw}	4-26	$\overline{RST}$ pulse width	at 0.8V (both edges)	64		64		t_{Cp}
t_{INTs}	4-27	$\overline{INT}$ setup time	before F.E., PHI1	20		15		ns
t_{NMIw}	4-28	$\overline{NMI}$ pulse width	at 0.8V (both edges)	70		70		ns
t_{DIs}	4-14	Data setup (slave read cycle)	before F.E., PHI2 T1	15		10		ns
t_{DIh}	4-14	Data hold (slave read cycle)	after R.E., PHI1 T4	3		3		ns
t_{SPCd}	4-15	$\overline{SPC}$ pulse delay from slave	after R.E., PHI2 T4	30		25		ns
t_{SPCs}	4-15	$\overline{SPC}$ setup time	before F.E., PHI1	30		25		ns
t_{SPCw}	4-15	$\overline{SPC}$ pulse width from slave processor (async input)	at 0.8V (both edges)	25		20		ns
t_{ATs}	4-16	$\overline{AT}/\overline{SPC}$ setup for address translation strap	before R.E., PHI1 of cycle during which $\overline{RST}$ pulse is removed	1		1		t_{Cp}
t_{ATh}	4-16	$\overline{AT}/\overline{SPC}$ hold for address translation strap	after F.E., PHI1 of cycle during which $\overline{RST}$ pulse is removed	2		2		t_{Cp}

Note: This setup time is necessary to ensure prompt acknowledgement via $\overline{HLDA}$ and the ensuing floating of CPU off the buses. Note that the time from the receipt of the $\overline{HOLD}$ signal until the CPU floats is a function of the time $\overline{HOLD}$ signal goes low, the state of the RDY input (in MMU systems), and the length of the current MMU cycle.

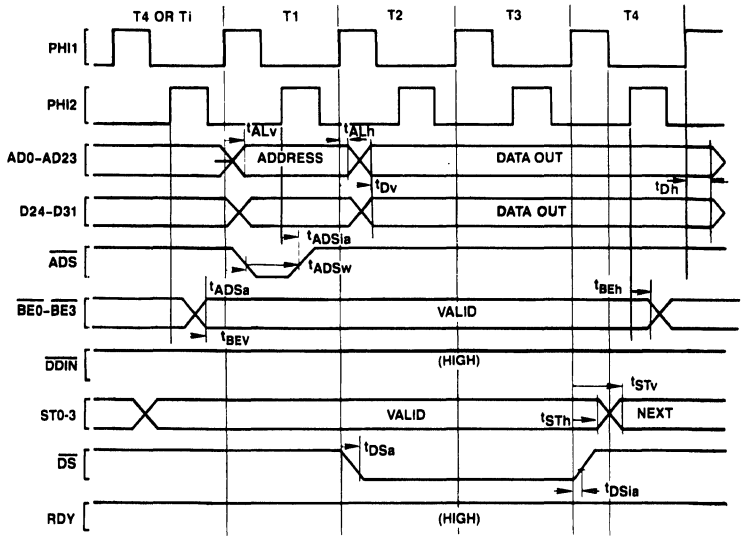
4.4.2.3 Clocking Requirements: NS32C032-10, and NS32C032-15

Name	Figure	Description	Reference/ Conditions	NS32C032-10		NS32C032-15		Units
				Min	Max	Min	Max	
t_{Cp}	4-17	Clock Period	R.E., PHI1, PHI2 to next R.E., PHI1, PHI2	100	250	66	250	ns
$t_{CLw(1,2)}$	4-17	PHI1, PHI2 Pulse Width	At 2.0V on PHI1, PHI2 (Both Edges)	0.5 t_{Cp} −10 ns		0.5 t_{Cp} −6 ns		
$t_{CLh(1,2)}$	4-17	PHI1, PHI2 High Time	At 90% V_{CC} on PHI1, PHI2	0.5 t_{Cp} −15 ns		0.5 t_{Cp} −10 ns		
$t_{CLl(1,2)}$	4-17	PHI1, PHI2 Low Time	At 15% V_{CC} on PHI1, PHI2	0.5 t_{CP} −6 ns		0.5 t_{CP} −5 ns		ns
$t_{nOVL(1,2)}$	4-17	Non-Overlap Time	At 15% V_{CC} on PHI1, PHI2	−2	2	−2	2	ns
t_{nOVLas}		Non-Overlap Asymmetry ($t_{nOVL(1)} - t_{nOVL(2)}$)	At 15% V_{CC} on PHI1, PHI2	−3	3	−3	3	ns
t_{CLwas}		PHI1, PHI2 Asymmetry ($t_{CLw(1)} - t_{CLw(2)}$)	At 2.0V on PHI1, PHI2	−5	5	−3	3	ns

2

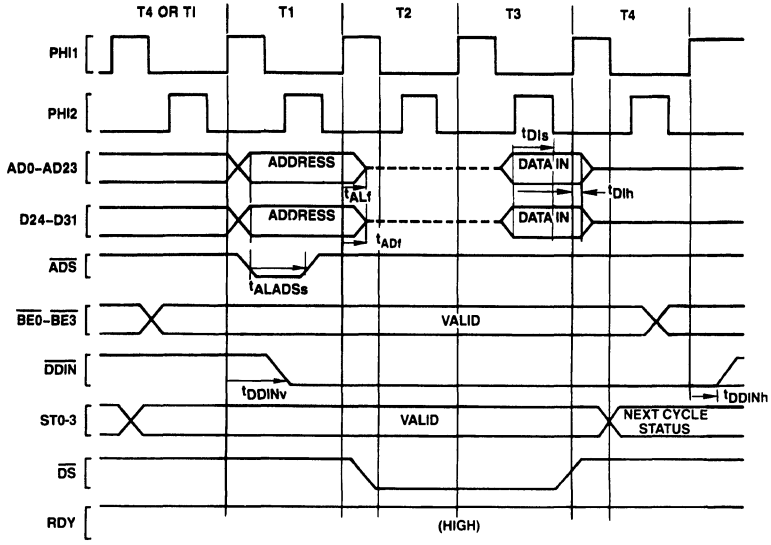
4.0 Device Specifications

4.4.3 Timing Diagrams



TL/EE/9160–45

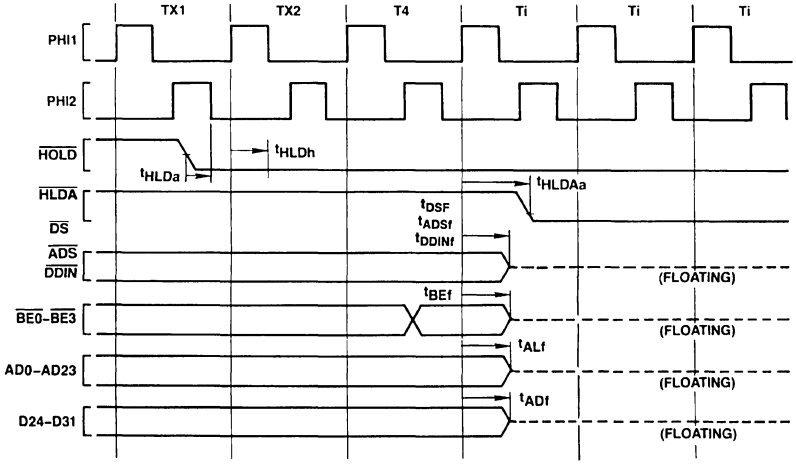
FIGURE 4-4. Write Cycle



TL/EE/9160–46

FIGURE 4-5. Read Cycle

4.0 Device Specifications (Continued)



TL/EE/9160-47

FIGURE 4-6. Floating by $\overline{\text{HOLD}}$ Timing (CPU Not Idle Initially).

Note that whenever the CPU is not idling (not in Ti), the $\overline{\text{HOLD}}$ request ($\overline{\text{HOLD}}$ low) must be active tHLDa before the falling edge of PHI2 of the clock cycle that appears two clock cycles before T4 (TX1) and stay low until tHLDh after the rising edge of PHI1 of the clock cycle that precedes T4 (TX2) for the request to be acknowledged.

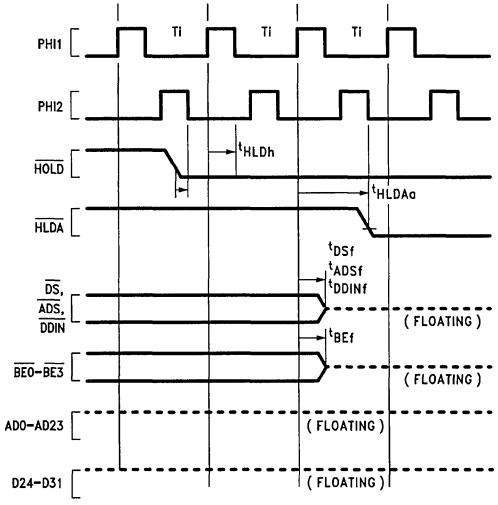


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FIGURE 4-7. Floating by $\overline{\text{HOLD}}$ Timing (CPU initially idle)

Note that during Ti1 the CPU is already idling.

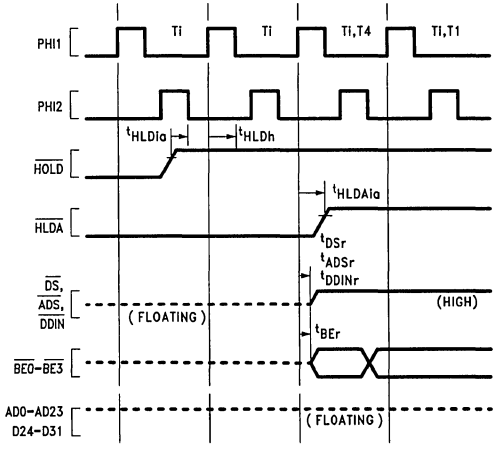

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FIGURE 4-8. Release from $\overline{\text{HOLD}}$

2

4.0 Device Specifications (Continued)

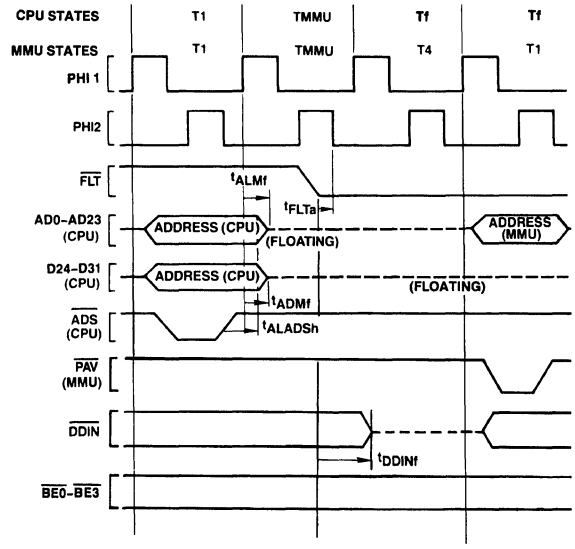

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FIGURE 4-9. FLT Initiated Float Cycle Timing

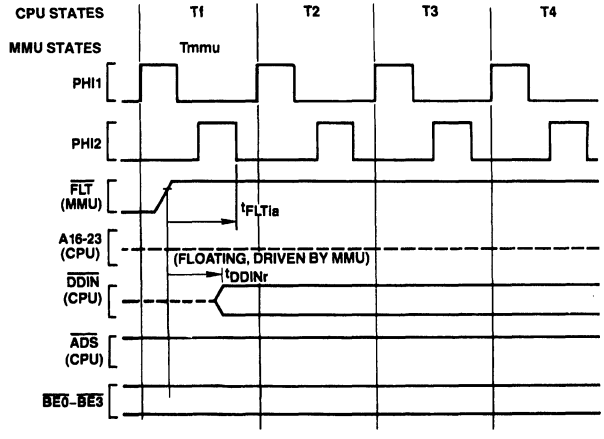

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FIGURE 4-10. Release from FLT Timing

Note that when FLT is deasserted the CPU restarts driving DDIN before the MMU releases it. This, however, does not cause any conflict, since both CPU and MMU force DDIN to the same logic level.

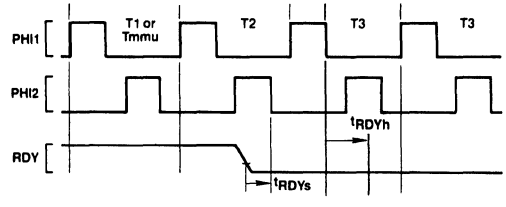

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FIGURE 4-11. Ready Sampling (CPU Initially READY)

4.0 Device Specifications (Continued)

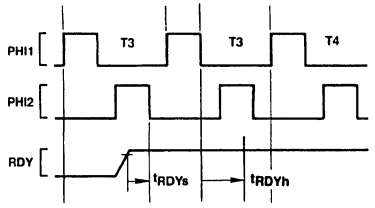

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FIGURE 4-12. Ready Sampling (CPU Initially NOT READY)

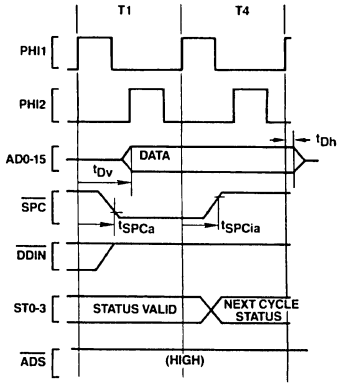

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FIGURE 4-13. Slave Processor Write Timing

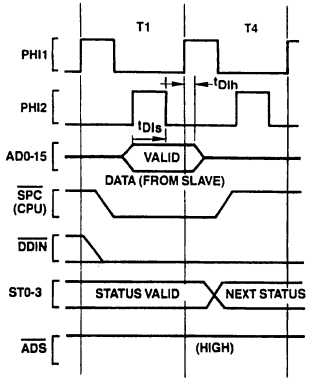

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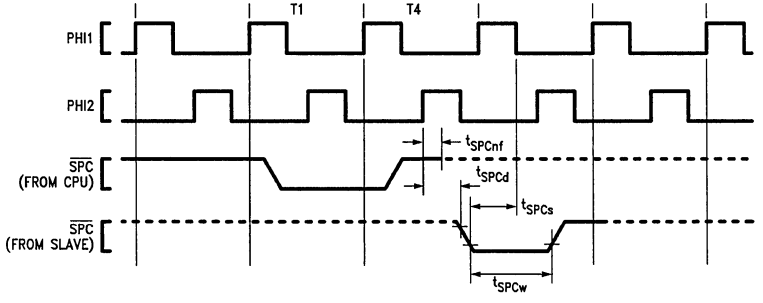
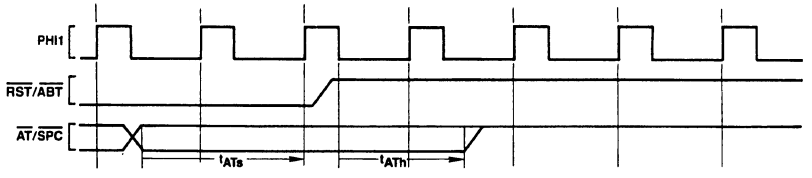
FIGURE 4-14. Slave Processor Read Timing



TL/EE/9160-56

FIGURE 4-15. $\overline{SPC}$ Timing

After transferring last operand to a Slave Processor, CPU turns OFF driver and holds $\overline{SPC}$ high with internal 5 kΩ pullup.



TL/EE/9160-57

FIGURE 4-16. Reset Configuration Timing

4.0 Device Specifications (Continued)

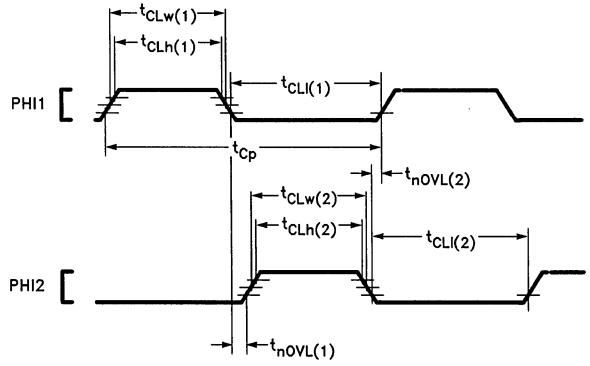


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FIGURE 4-17. Clock Waveforms

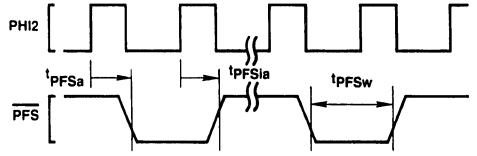

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FIGURE 4-18. Relationship of $\overline{PFS}$ to Clock Cycles

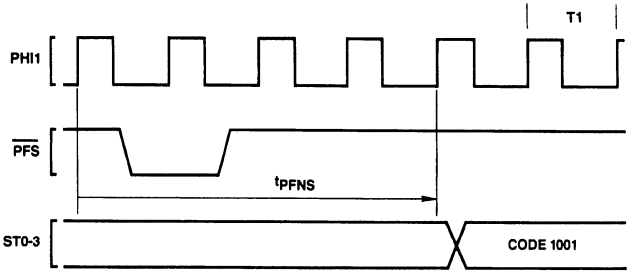

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FIGURE 4-19a. Guaranteed Delay, $\overline{PFS}$ to Non-Sequential Fetch

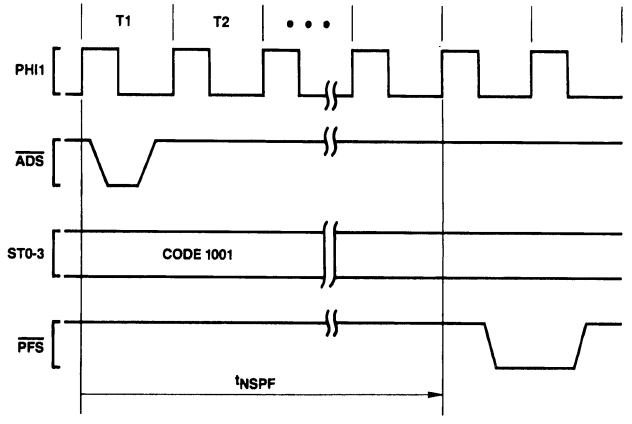

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FIGURE 4-19b. Guaranteed Delay, Non-Sequential Fetch to $\overline{PFS}$

4.0 Device Specifications (Continued)

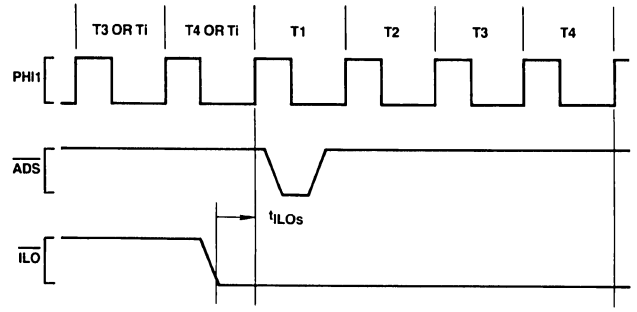

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FIGURE 4-20a. Relationship of $\overline{ILO}$ to First Operand Cycle of an Interlocked Instruction

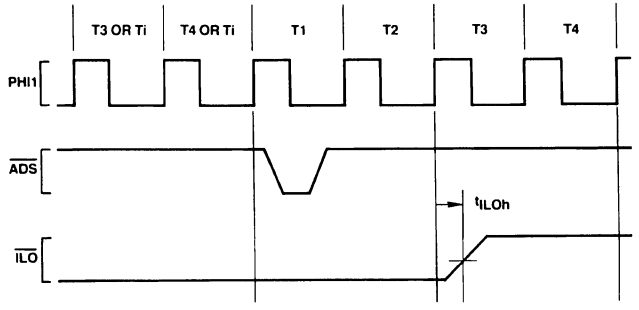

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FIGURE 4-20b. Relationship of $\overline{ILO}$ to Last Operand Cycle of an Interlocked Instruction

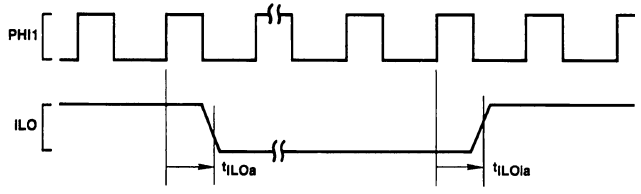

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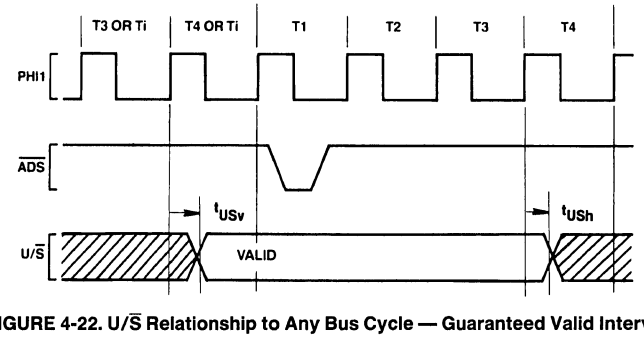
FIGURE 4-21. Relationship of $\overline{ILO}$ to Any Clock Cycle



TL/EE/9160-65

FIGURE 4-22. U/$\overline{S}$ Relationship to Any Bus Cycle — Guaranteed Valid Interval

4.0 Device Specifications (Continued)

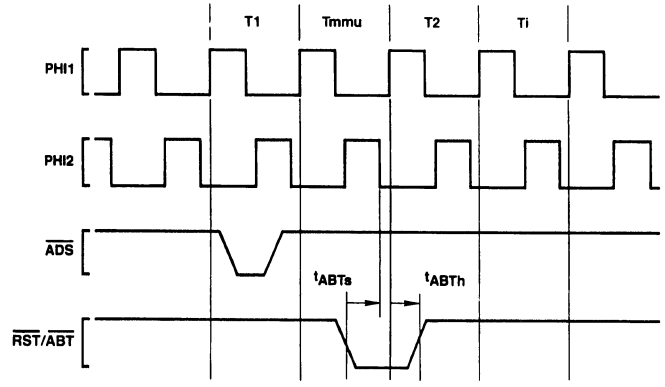


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FIGURE 4-23. Abort Timing, $\overline{FLT}$ Not Applied

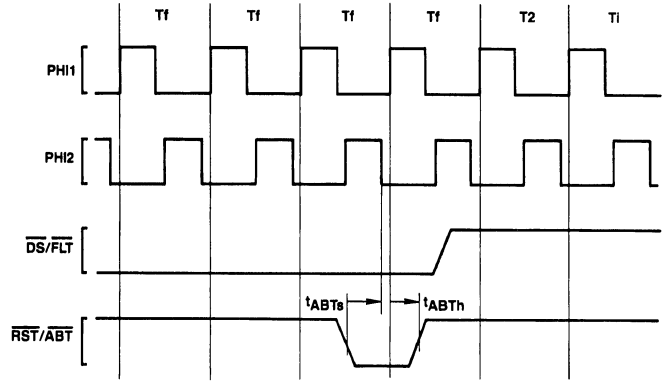

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FIGURE 4-24. Abort Timing, $\overline{FLT}$ Applied

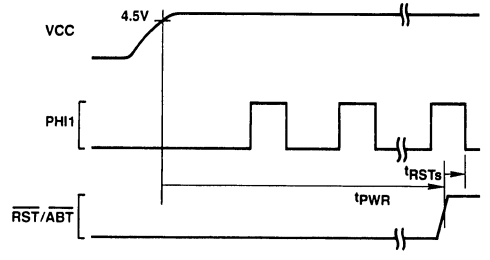

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FIGURE 4-25. Power-On Reset

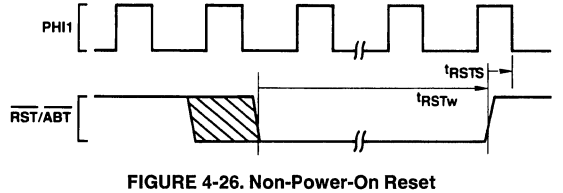

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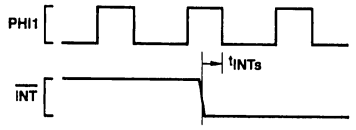
FIGURE 4-26. Non-Power-On Reset

4.0 Device Specifications (Continued)



TL/EE/9160-70

FIGURE 4-27. $\overline{INT}$ Interrupt Signal Detection

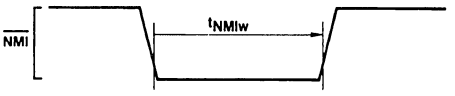


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FIGURE 4-28. $\overline{NMI}$ Interrupt Signal Timing

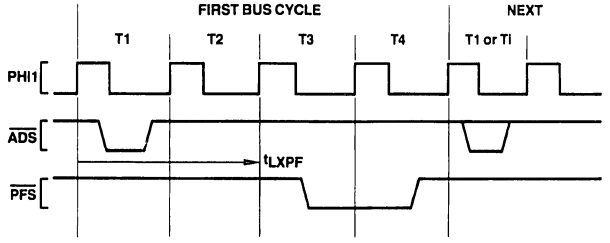

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FIGURE 4-29. Relationship Between Last Data Transfer of an Instruction and $\overline{PFS}$ Pulse of Next Instruction

Note: In a transfer of a Read-Modify-Write type operand, this is the Read transfer, displaying RMW Status (Code 1011).

Appendix A: Instruction Formats

NOTATIONS

i= Integer Type Field
- B = 00 (Byte)
- W = 01 (Word)
- D = 11 (Double Word)

f= Floating Point Type Field
- F = 1 (Std. Floating: 32 bits)
- L = 0 (Long Floating: 64 bits)

c= Custom Type Field
- D = 1 (Double Word)
- Q = 0 (Quad Word)

op= Operation Code
- Valid encodings shown with each format.

gen, gen 1, gen 2= General Addressing Mode Field
- See Sec. 2.2 for encodings.

reg= General Purpose Register Number

cond= Condition Code Field
- 0000 = EQual: Z = 1
- 0001 = Not Equal: Z = 0
- 0010 = Carry Set: C = 1
- 0011 = Carry Clear: C = 0
- 0100 = HIgher: L = 1
- 0101 = Lower or Same: L = 0
- 0110 = Greater Than: N = 1
- 0111 = Less or Equal: N = 0
- 1000 = Flag Set: F = 1
- 1001 = Flag Clear: F = 0
- 1010 = LOwer: L = 0 and Z = 0
- 1011 = Higher or Same: L = 1 or Z = 1
- 1100 = Less Than: N = 0 and Z = 0
- 1101 = Greater or Equal: N = 1 or Z = 1
- 1110 = (Unconditionally True)
- 1111 = (Unconditionally False)

short= Short Immediate value. May contain
- quick: Signed 4-bit value, in MOVQ, ADDQ, CMPQ, ACB.
- cond: Condition Code (above), in Scond.
- areg: CPU Dedicated Register, in LPR, SPR.
  - 0000 = US
  - 0001 – 0111 = (Reserved)
  - 1000 = FP
  - 1001 = SP
  - 1010 = SB
  - 1011 = (Reserved)
  - 1100 = (Reserved)
  - 1101 = PSR
  - 1110 = INTBASE
  - 1111 = MOD
- Options: in String Instructions

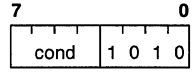
U/W	B	T

  - T = Translated
  - B = Backward
  - U/W = 00: None
    - 01: While Match
    - 11: Until Match

Configuration bits, in SETCFG:

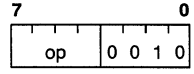
C	M	F	I

mreg: NS32082 Register number, in LMR, SMR.
- 0000 = BPR0
- 0001 = BPR1
- 0010 = (Reserved)
- 0011 = (Reserved)
- 0100 = (Reserved)
- 0101 = (Reserved)
- 0110 = (Reserved)
- 0111 = (Reserved)
- 1000 = (Reserved)
- 1001 = (Reserved)
- 1010 = MSR
- 1011 = BCNT
- 1100 = PTB0
- 1101 = PTB1
- 1110 = (Reserved)
- 1111 = EIA



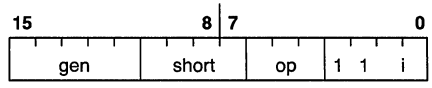
Format 0

Bcond (BR)



Format 1

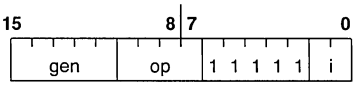
BSR	-0000	ENTER	-1000
RET	-0001	EXIT	-1001
CXP	-0010	NOP	-1010
RXP	-0011	WAIT	-1011
RETT	-0100	DIA	-1100
RETI	-0101	FLAG	-1101
SAVE	-0110	SVC	-1110
RESTORE	-0111	BPT	-1111



Format 2

ADDQ	-000	ACB	-100
CMPQ	-001	MOVQ	-101
SPR	-010	LPR	-110
Scond	-011		

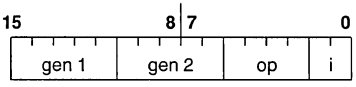
Appendix A: Instruction Formats (Continued)



Format 3

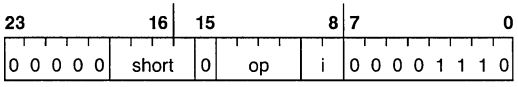
CXPD	-0000	ADJSP	-1010
BICPSR	-0010	JSR	-1100
JUMP	-0100	CASE	-1110
BISPSR	-0110		

Trap (UND) on XXX1, 1000



Format 4

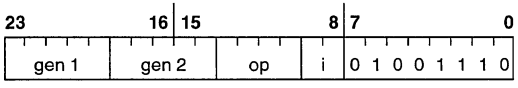
ADD	-0000	SUB	-1000
CMP	-0001	ADDR	-1001
BIC	-0010	AND	-1010
ADDC	-0100	SUBC	-1100
MOV	-0101	TBIT	-1101
OR	-0110	XOR	-1110



Format 5

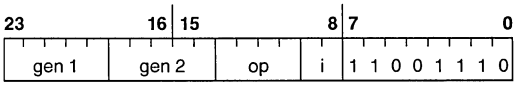
MOVS	-0000	SETCFG	-0010
CMPS	-0001	SKPS	-0011

Trap (UND) on 1XXX, 01XX



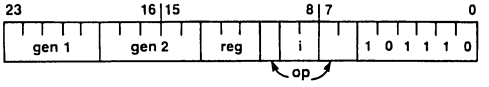
Format 6

ROT	-0000	NEG	-1000
ASH	-0001	NOT	-1001
CBIT	-0010	Trap (UND)	-1010
CBITI	-0011	SUBP	-1011
Trap (UND)	-0100	ABS	-1100
LSH	-0101	COM	-1101
SBIT	-0110	IBIT	-1110
SBITI	-0111	ADDP	-1111



Format 7

MOVM	-0000	MUL	-1000
CMPM	-0001	MEI	-1001
INSS	-0010	Trap (UND)	-1010
EXTS	-0011	DEI	-1011
MOVXBW	-0100	QUO	-1100
MOVZBW	-0101	REM	-1101
MOVZiD	-0110	MOD	-1110
MOVXiD	-0111	DIV	-1111



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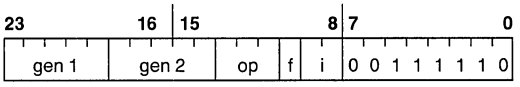
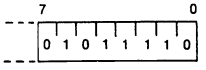
Format 8

EXT	-0 00	INDEX	-1 00
CVTP	-0 01	FFS	-1 01
INS	-0 10		
CHECK	-0 11		
MOVSU	-110, reg = 001		
MOVUS	-110, reg = 011		



Format 9

MOVif	-000	ROUND	-100
LFSR	-001	TRUNC	-101
MOVLF	-010	SFSR	-110
MOVFL	-011	FLOOR	-111



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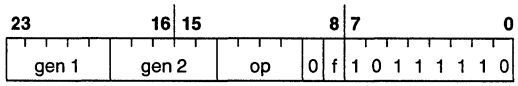
Format 10

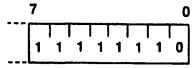
Trap (UND) Always

Appendix A: Instruction Formats (Continued)



Format 11

ADDf	-0000	DIVf	-1000
MOVf	-0001	Trap (SLAVE)	-1001
CMPf	-0010	Trap (UND)	-1010
Trap (SLAVE)	-0011	Trap (UND)	-1011
SUBf	-0100	MULf	-1100
NEGf	-0101	ABSf	-1101
Trap (UND)	-0110	Trap (UND)	-1110
Trap (UND)	-0111	Trap (UND)	-1111



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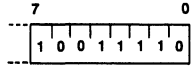
Format 12

Trap (UND) Always



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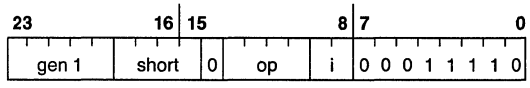
Format 13

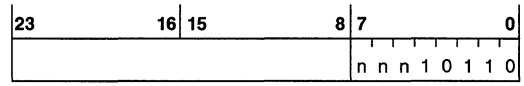
Trap (UND) Always



Format 14

RDVAL	-0000	LMR	-0010
WRVAL	-0001	SMR	-0011

Trap (UND) on 01XX, 1XXX



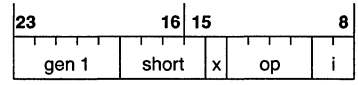
Operation Word ID Byte

Format 15

(Custom Slave)

nnn **Operation Word Format**

000

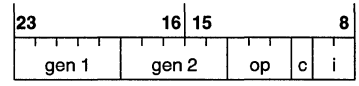


Format 15.0

CATST0	-0000	LCR	-0010
CATST1	-0001	SCR	-0011

Trap (UND) on all others

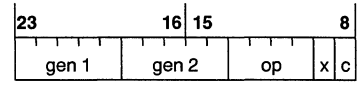
001



Format 15.1

CCV3	-000	CCV2	-100
LCSR	-001	CCV1	-101
CCV5	-010	SCSR	-110
CCV4	-011	CCV0	-111

101

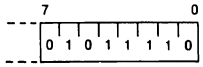


Format 15.5

CCAL0	-0000	CCAL3	-1000
CMOV0	-0001	CMOV3	-1001
CCMP0	-0010	Trap (UND)	-1010
CCMP1	-0011	Trap (UND)	-1011
CCAL1	-0100	CCAL2	-1100
CMOV2	-0101	CMOV1	-1101
Trap (UND)	-0110	Trap (UND)	-1110
Trap (UND)	-0111	Trap (UND)	-1111

If nnn = 010, 011, 100, 110, 111
then Trap (UND) Always

Appendix A: Instruction Formats (Continued)



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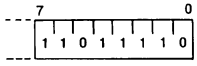
Format 16

Trap (UND) Always



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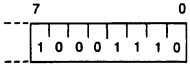
Format 17

Trap (UND) Always



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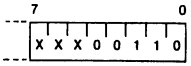
Format 18

Trap (UND) Always



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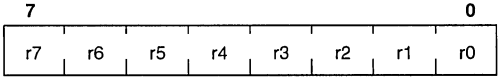
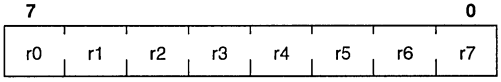
Format 19

Trap (UND) Always

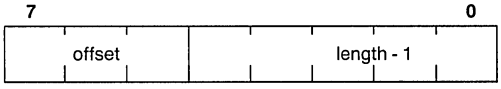
Implied Immediate Encodings:



Register Mark, appended to SAVE, ENTER



Register Mark, appended to RESTORE, EXIT



Offset/Length Modifier appended to INSS, EXTS

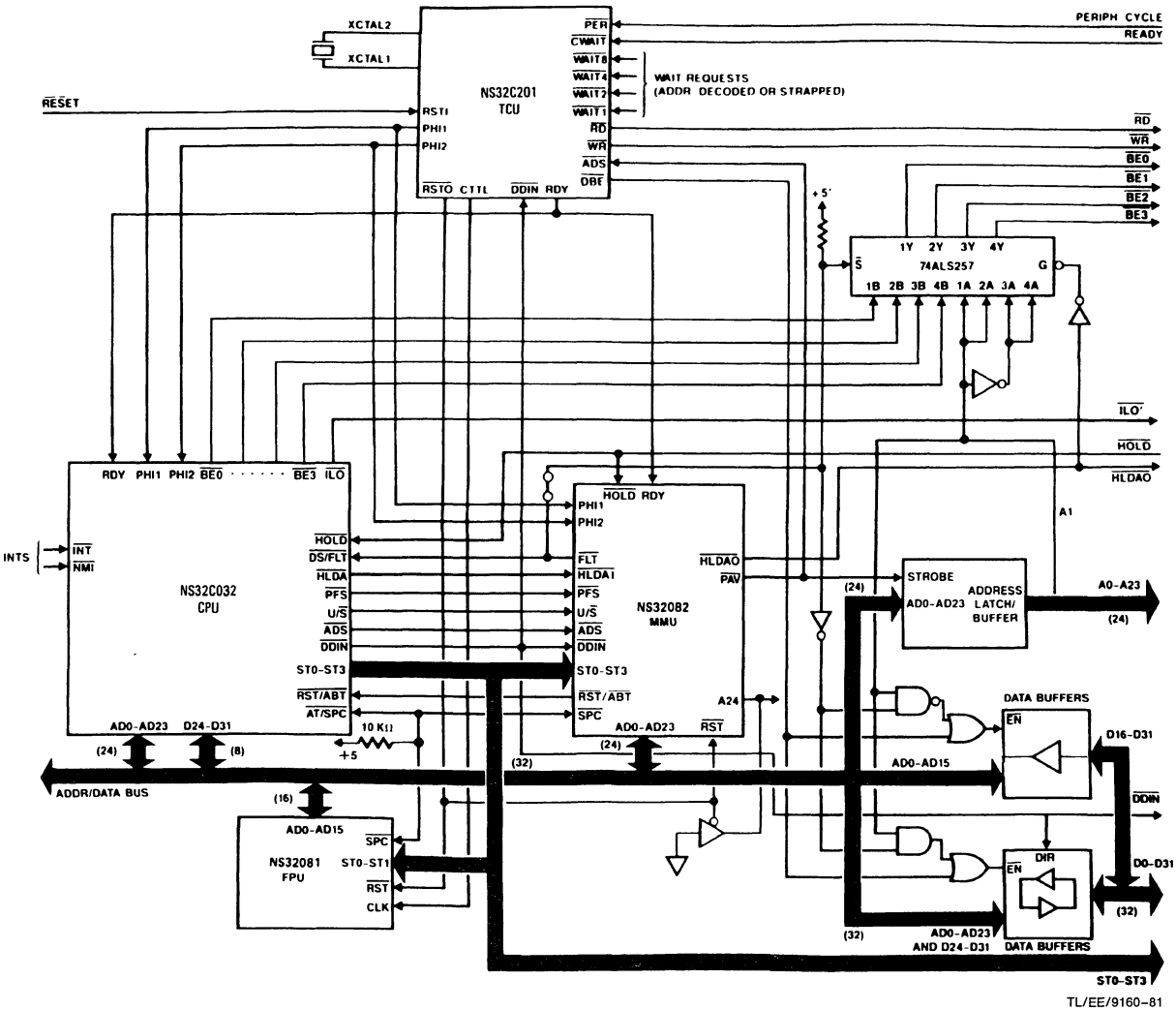


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FIGURE B-1. System Connection Diagram

National Semiconductor

NS32032-10 High-Performance Microprocessor

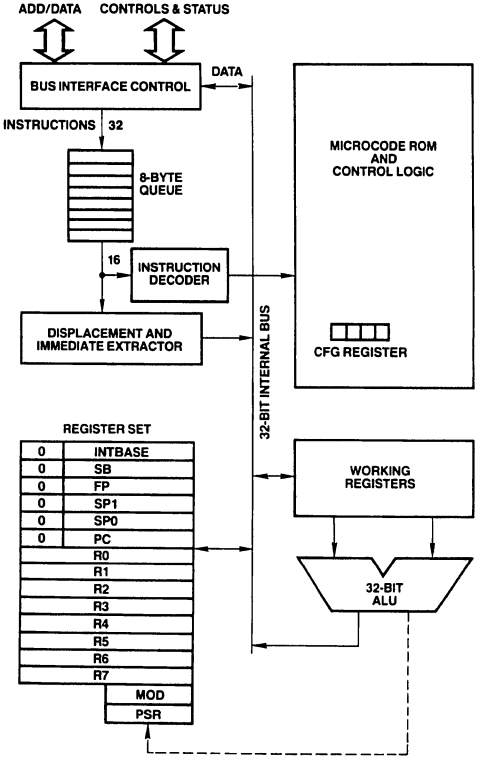
General Description

The NS32032 is a 32-bit, virtual memory microprocessor with a 16-MByte linear address space and a 32-bit external data bus. It has a 32-bit ALU, eight 32-bit general purpose registers, an eight-byte prefetch queue, and a slave processor interface. The NS32032 is fabricated with National Semiconductor's advanced XMOS™ process, and is fully object code compatible with other Series 32000® processors. The Series 32000 instruction set is optimized for modular, high-level languages (HLL). The set is very symmetric, it has a two address format, and it incorporates HLL oriented addressing modes. The capabilities of the NS32032 can be expanded with the use of the NS32081 floating point unit (FPU), and the NS32082 demand-paged virtual memory management unit (MMU). Both devices interface to the NS32032 as slave processors. The NS32032 is a general purpose microprocessor that is ideal for a wide range of computational intensive applications.

Features

- 32-bit architecture and implementation
- Virtual memory support
- 16-MByte linear address space
- 32-bit data bus
- Powerful instruction set
  - — General 2-address capability
  - — Very high degree of symmetry
  - — Addressing modes optimized for high-level languages
- Series 32000 slave processor support
- High-speed XMOS technology
- 68-pin leadless chip carrier

Block Diagram



TL/EE/5491–1

FIGURE 1

Table of Contents

List of Illustrations

List of Illustrations (Continued)

List of Tables

1.0 Product Introduction

The Series 32000 microprocessor family is a new generation of devices using National's XMOS and CMOS technologies. By combining state-of-the-art MOS technology with a very advanced architectural design philosophy, this family brings mainframe computer processing power to VLSI processors.

The Series 32000 family supports a variety of system configurations, extending from a minimum low-cost system to a powerful 4 gigabyte system. The architecture provides complete upward compatibility from one family member to another. The family consists of a selection of CPUs supported by a set of peripherals and slave processors that provide sophisticated interrupt and memory management facilities as well as high-speed floating-point operations. The architectural features of the Series 32000 family are described briefly below:

Powerful Addressing Modes. Nine addressing modes available to all instructions are included to access data structures efficiently.

Data Types. The architecture provides for numerous data types, such as byte, word, doubleword, and BCD, which may be arranged into a wide variety of data structures.

Symmetric Instruction Set. While avoiding special case instructions that compilers can't use, the Series 32000 family incorporates powerful instructions for control operations, such as array indexing and external procedure calls, which save considerable space and time for compiled code.

Memory-to-Memory Operations. The Series 32000 CPUs represent two-address machines. This means that each operand can be referenced by any one of the addressing modes provided. This powerful memory-to-memory architecture permits memory locations to be treated as registers for all useful operations. This is important for temporary operands as well as for context switching.

Memory Management. Either the NS32382 or the NS32082 Memory Management Unit may be added to the system to provide advanced operating system support functions, including dynamic address translation, virtual memory management, and memory protection.

Large, Uniform Addressing. The NS32032 has 24-bit address pointers that can address up to 16 megabytes without requiring any segmentation; this addressing scheme provides flexible memory management without added-on expense.

Modular Software Support. Any software package for the Series 32000 family can be developed independent of all other packages, without regard to individual addressing. In addition, ROM code is totally relocatable and easy to access, which allows a significant reduction in hardware and software cost.

Software Processor Concept. The Series 32000 architecture allows future expansions of the instruction set that can be executed by special slave processors, acting as extensions to the CPU. This concept of slave processors is unique to the Series 32000 family. It allows software compatibility even for future components because the slave hardware is transparent to the software. With future advances in semiconductor technology, the slaves can be physically integrated on the CPU chip itself.

To summarize, the architectural features cited above provide three primary performance advantages and characteristics:

- High-Level Language Support
- Easy Future Growth Path
- Application Flexibility

2.0 Architectural Description

2.1 PROGRAMMING MODEL

The Series 32000 architecture includes 16 registers on the NS32032 CPU.

2.1.1 General Purpose Registers

There are eight registers for meeting high speed general storage requirements, such as holding temporary variables and addresses. The general purpose registers are free for any use by the programmer. They are thirty-two bits in length. If a general register is specified for an operand that is eight or sixteen bits long, only the low part of the register is used; the high part is not referenced or modified.

2.1.2 Dedicated Registers

The eight dedicated registers of the NS32032 are assigned specific functions.

PC: The PROGRAM COUNTER register is a pointer to the first byte of the instruction currently being executed. The PC is used to reference memory in the program section. (In the NS32032 the upper eight bits of this register are always zero.)

SP0, SP1: The SP0 register points to the lowest address of the last item stored on the INTERRUPT STACK. This stack is normally used only by the operating system. It is used primarily for storing temporary data, and holding return information for operating system subroutines and interrupt and trap service routines. The SP1 register points to the lowest address of the last item stored on the USER STACK. This stack is used by normal user programs to hold temporary data and subroutine return information.

In this document, reference is made to the SP register. The terms "SP register" or "SP" refer to either SP0 or SP1, depending on the setting of the S bit in the PSR register. If the S bit in the PSR is 0 the SP refers to SP0. If the S bit in the PSR is 1 then SP refers to SP1. (In the NS32032 the upper eight bits of these registers are always zero).

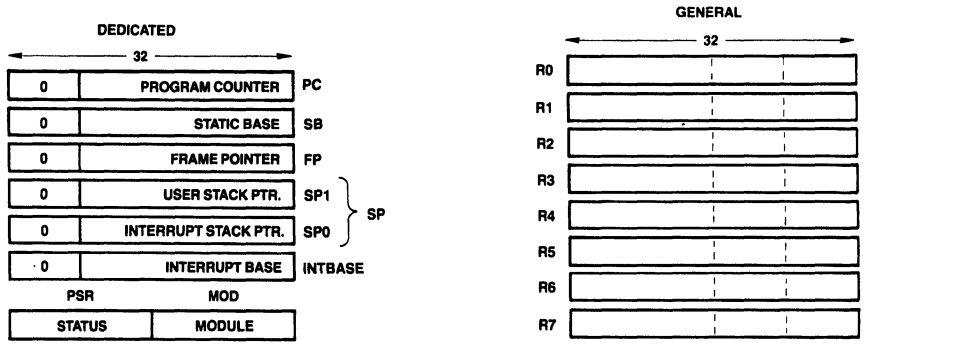
Stacks in the Series 32000 family grow downward in memory. A Push operation pre-decrements the Stack Pointer by the operand length. A Pop operation post-increments the Stack Pointer by the operand length.

FP: The FRAME POINTER register is used by a procedure to access parameters and local variables on the stack. The FP register is set up on procedure entry with the ENTER instruction and restored on procedure termination with the EXIT instruction.

The frame pointer holds the address in memory occupied by the old contents of the frame pointer. (In the NS32032 the upper eight bits of this register are always zero.)

SB: The STATIC BASE register points to the global variables of a software module. This register is used to support relocatable global variables for software modules.

2.0 Architectural Description (Continued)



TL/EE/5491-3

FIGURE 2-1. The General and Dedicated Registers

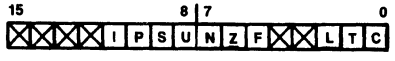
The SB register holds the lowest address in memory occupied by the global variables of a module. (In the NS32032 the upper eight bits of this register are always zero.)

INTBASE: The INTERRUPT BASE register holds the address of the dispatch table for interrupts and traps (Sec. 3.8). The INTBASE register holds the lowest address in memory occupied by the dispatch table. (In the NS32032 the upper eight bits of this register are always zero.)

MOD: The MODULE register holds the address of the module descriptor of the currently executing software module. The MOD register is sixteen bits long, therefore the module table must be contained within the first 64K bytes of memory.

PSR: The PROCESSOR STATUS REGISTER (PSR) holds the status codes for the NS32032 microprocessor.

The PSR is sixteen bits long, divided into two eight-bit halves. The low order eight bits are accessible to all programs, but the high order eight bits are accessible only to programs executing in Supervisor Mode.



TL/EE/5491-4

FIGURE 2-2. Processor Status Register

C: The C bit indicates that a carry or borrow occurred after an addition or subtraction instruction. It can be used with the ADDC and SUBC instructions to perform multiple-precision integer arithmetic calculations. It may have a setting of 0 (no carry or borrow) or 1 (carry or borrow).

T: The T bit causes program tracing. If this bit is a 1, a TRC trap is executed after every instruction (Sec. 3.8.5).

L: The L bit is altered by comparison instructions. In a comparison instruction the L bit is set to "1" if the second operand is less than the first operand, when both operands are interpreted as unsigned integers. Otherwise, it is set to "0". In Floating Point comparisons, this bit is always cleared.

F: The F bit is a general condition flag, which is altered by many instructions (e.g., integer arithmetic instructions use it to indicate overflow).

Z: The Z bit is altered by comparison instructions. In a comparison instruction the Z bit is set to "1" if the second operand is equal to the first operand; otherwise it is set to "0".

N: The N bit is altered by comparison instructions. In a comparison instruction the N bit is set to "1" if the second operand is less than the first operand, when both operands are interpreted as signed integers. Otherwise, it is set to "0".

U: If the U bit is "1" no privileged instructions may be executed. If the U bit is "0" then all instructions may be executed. When U = 0 the NS32032 is said to be in Supervisor Mode; when U = 1 the NS32032 is said to be in User Mode. A User Mode program is restricted from executing certain instructions and accessing certain registers which could interfere with the operating system. For example, a User Mode program is prevented from changing the setting of the flag used to indicate its own privilege mode. A Supervisor Mode program is assumed to be a trusted part of the operating system, hence it has no such restrictions.

S: The S bit specifies whether the SP0 register or SP1 register is used as the stack pointer. The bit is automatically cleared on interrupts and traps. It may have a setting of 0 (use the SP0 register) or 1 (use the SP1 register).

P: The P bit prevents a TRC trap from occurring more than once for an instruction (Sec. 3.8.5.). It may have a setting of 0 (no trace pending) or 1 (trace pending).

I: If I = 1, then all interrupts will be accepted (Sec. 3.8.). If I = 0, only the NMI interrupt is accepted. Trap enables are not affected by this bit.

2.1.3 The Configuration Register (CFG)

Within the Control section of the NS32032 CPU is the four-bit CFG Register, which declares the presence of certain external devices. It is referenced by only one instruction, SETCFG, which is intended to be executed only as part of system initialization after reset. The format of the CFG Register is shown in *Figure 2-3.*

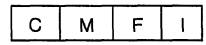


FIGURE 2-3. CFG Register

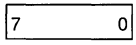
2.0 Architectural Description (Continued)

The CFG I bit declares the presence of external interrupt vectoring circuitry (specifically, the NS32202 Interrupt Control Unit). If the CFG I bit is set, interrupts requested through the $\overline{INT}$ pin are "Vectored." If it is clear, these interrupts are "Non-Vectored." See Sec. 3.8.

The F, M and C bits declare the presence of the FPU, MMU and Custom Slave Processors. If these bits are not set, the corresponding instructions are trapped as being undefined.

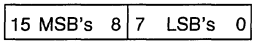
2.1.4 Memory Organization

The main memory of the NS32032 is a uniform linear address space. Memory locations are numbered sequentially starting at zero and ending at $2^{24} - 1$. The number specifying a memory location is called an address. The contents of each memory location is a byte consisting of eight bits. Unless otherwise noted, diagrams in this document show data stored in memory with the lowest address on the right and the highest address on the left. Also, when data is shown vertically, the lowest address is at the top of a diagram and the highest address at the bottom of the diagram. When bits are numbered in a diagram, the least significant bit is given the number zero, and is shown at the right of the diagram. Bits are numbered in increasing significance and toward the left.



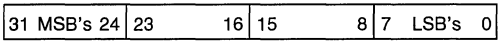
Byte at Address A

Two contiguous bytes are called a word. Except where noted (Sec. 2.2.1), the least significant byte of a word is stored at the lower address, and the most significant byte of a word is the address of its least significant byte, and a word may start at any address.



Word at Address A

Two contiguous words are called a double word. Except where noted (Sec. 2.2.1), the least significant word of a double word is stored at the lowest address and the most significant word of the double word is stored at the address two greater. In memory, the address of a double word is the address of its least significant byte, and a double word may start at any address.



Double Word at Address A

Although memory is addressed as bytes, it is actually organized as double-words. Note that access time to a word or a double-word depends upon its address, e.g. double-words that are aligned to start at addresses that are multiples of four will be accessed more quickly than those not so aligned. This also applies to words that cross a double-word boundary.

2.1.5 Dedicated Tables

Two of the NS32032 dedicated registers (MOD and INTBASE) serve as pointers to dedicated tables in memory.

The INTBASE register points to the Interrupt Dispatch and Cascade tables. These are described in Sec. 3.8.

The MOD register contains a pointer into the Module Table, whose entries are called Module Descriptors. A Module Descriptor contains four pointers, three of which are used by NS32032. The MOD register contains the address of the Module Descriptor for the currently running module. It is automatically up-dated by the Call External Procedure instructions (CXP and CXPD).

The format of a Module Descriptor is shown in *Figure 2-4*. The Static Base entry contains the address of static data assigned to the running module. It is loaded into the CPU Static Base register by the CXP and CXPD instructions. The Program Base entry contains the address of the first byte of instruction code in the module. Since a module may have multiple entry points, the Program Base pointer serves only as a reference to find them.

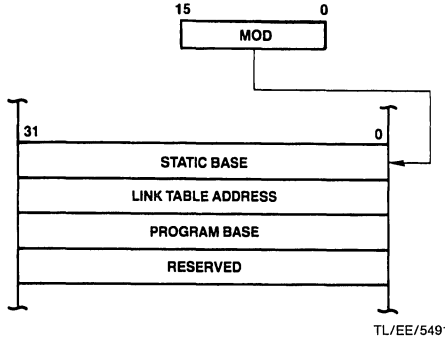


FIGURE 2-4. Module Descriptor Format

The Link Table Address points to the Link Table for the currently running module. The Link Table provides the information needed for:

1) Sharing variables between modules. Such variables are accessed through the Link Table via the External addressing mode.
2) Transferring control from one module to another. This is done via the Call External Procedure (CXP) instruction.

The format of a Link Table is given in *Figure 2-5*. A Link Table Entry for an external variable contains the 32-bit address of that variable. An entry for an external procedure contains two 16-bit fields: Module and Offset. The Module field contains the new MOD register contents for the module being entered. The Offset field is an unsigned number giving the position of the entry point relative to the new module's Program Base pointer.

For further details of the functions of these tables, see the Series 32000 Instruction Set Reference Manual.

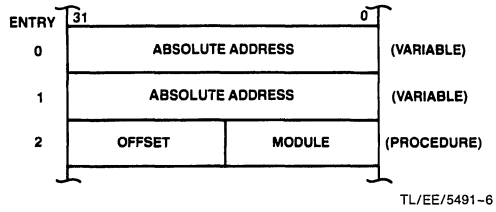


FIGURE 2-5. A Sample Link Table

2.0 Architectural Description (Continued)

2.2 INSTRUCTION SET

2.2.1 General Instruction Format

Figure 2-6 shows the general format of a Series 32000 instruction. The Basic Instruction is one to three bytes long and contains the Opcode and up to two 5-bit General Addressing Mode ("Gen") fields. Following the Basic Instruction field is a set of optional extensions, which may appear depending on the instruction and the addressing modes selected.

Index Bytes appear when either or both Gen fields specify Scaled Index. In this case, the Gen field specifies only the Scale Factor (1, 2, 4 or 8), and the Index Byte specifies which General Purpose Register to use as the index, and which addressing mode calculation to perform before indexing. See *Figure 2-7*.

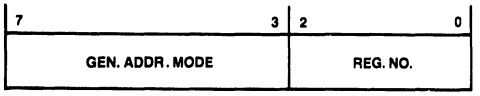


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FIGURE 2-7. Index Byte Format

Following Index Bytes come any displacements (addressing constants) or immediate values associated with the selected address modes. Each Disp/Imm field may contain one or two displacements, or one immediate value. The size of a Displacement field is encoded with the top bits of that field, as shown in *Figure 2-8*, with the remaining bits interpreted as a signed (two's complement) value. The size of an immediate value is determined from the Opcode field. Both Displacement and Immediate fields are stored most significant byte first. Note that this is different from the memory representation of data (Sec. 2.1.4).

Some instructions require additional, "implied" immediates and/or displacements, apart from those associated with addressing modes. Any such extensions appear at the end of the instruction, in the order that they appear within the list of operands in the instruction definition (Sec. 2.2.3).

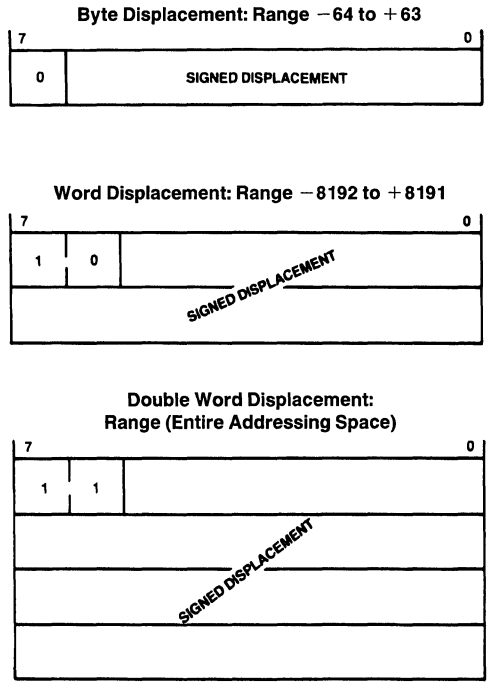

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FIGURE 2-8. Displacement Encodings

2.2.2 Addressing Modes

The NS32032 CPU generally accesses an operand by calculating its Effective Address based on information available when the operand is to be accessed. The method to be used in performing this calculation is specified by the programmer as an "addressing mode."

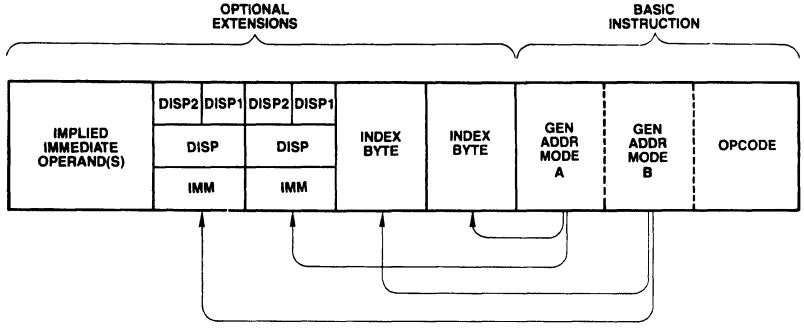

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FIGURE 2-6. General Instruction Format

2.0 Architectural Description (Continued)

Addressing modes in the NS32032 are designed to optimally support high-level language accesses to variables. In nearly all cases, a variable access requires only one addressing mode, within the instruction that acts upon that variable. Extraneous data movement is therefore minimized.

NS32032 Addressing Modes fall into nine basic types:

Register: The operand is available in one of the eight General Purpose Registers. In certain Slave Processor instructions, an auxiliary set of eight registers may be referenced instead.

Register Relative: A General Purpose Register contains an address to which is added a displacement value from the instruction, yielding the Effective Address of the operand in memory.

Memory Space. Identical to Register Relative above, except that the register used is one of the dedicated registers PC, SP, SB or FP. These registers point to data areas generally needed by high-level languages.

Memory Relative: A pointer variable is found within the memory space pointed to by the SP, SB or FP register. A displacement is added to that pointer to generate the Effective Address of the operand.

Immediate: The operand is encoded within the instruction. This addressing mode is not allowed if the operand is to be written.

Absolute: The address of the operand is specified by a displacement field in the instruction.

External: A pointer value is read from a specified entry of the current Link Table. To this pointer value is added a displacement, yielding the Effective Address of the operand.

Top of Stack: The currently-selected Stack Pointer (SP0 or SP1) specifies the location of the operand. The operand is pushed or popped, depending on whether it is written or read.

Scaled Index: Although encoded as an addressing mode. Scaled Indexing is an option on any addressing mode except Immediate or another Scaled Index. It has the effect of calculating an Effective Address, then multiplying any General Purpose Register by 1, 2, 4 or 8 and adding it into the total, yielding the final Effective Address of the operand.

Table 2-1 is a brief summary of the addressing modes. For a complete description of their actions, see the Instruction Set Reference Manual.

2.2.3 Instruction Set Summary

Table 2-2 presents a brief description of the NS32032 instruction set. The Format column refers to the Instruction Format tables (Appendix A). The Instruction column gives the instruction as coded in assembly language, and the Description column provides a short description of the function provided by that instruction. Further details of the exact operations performed by each instruction may be found in the Instruction Set Reference Manual.

Notations:

i = Integer length suffix: B = Byte
W = Word
D = Double Word

f = Floating Point length suffix: F = Standard Floating
L = Long Floating

gen = General operand. Any addressing mode can be specified.

short = A 4-bit value encoded within the Basic Instruction (see Appendix A for encodings).

imm = Implied immediate operand. An 8-bit value appended after any addressing extensions.

disp = Displacement (addressing constant): 8, 16 or 32 bits. All three lengths legal.

reg = Any General Purpose Register: R0–R7.

areg = Any Dedicated/Address Register: SP, SB, FP, MOD, INTBASE, PSR, US (bottom 8 PSR bits).

mreg = Any Memory Management Status/Control Register.

creg = A Custom Slave Processor Register (Implementation Dependent).

cond = Any condition code, encoded as a 4-bit field within the Basic Instruction (see Appendix A for encodings).

2.0 Architectural Description (Continued)

TABLE 2-1
NS32032 Addressing Modes

ENCODING	MODE	ASSEMBLER SYNTAX	EFFECTIVE ADDRESS
Register			
00000	Register 0	R0 or F0	None: Operand is in the specified register
00001	Register 1	R1 or F1	
00010	Register 2	R2 or F2	
00011	Register 3	R3 or F3	
00100	Register 4	R4 or F4	
00101	Register 5	R5 or F5	
00110	Register 6	R6 or F6	
00111	Register 7	R7 or F7	
Register Relative			
01000	Register 0 relative	disp(R0)	Disp + Register.
01001	Register 1 relative	disp(R1)	
01010	Register 2 relative	disp(R2)	
01011	Register 3 relative	disp(R3)	
01100	Register 4 relative	disp(R4)	
01101	Register 5 relative	disp(R5)	
01110	Register 6 relative	disp(R6)	
01111	Register 7 relative	disp(R7)	
Memory Relative			
10000	Frame memory relative	disp2(disp1(FP))	Disp2 + Pointer; Pointer found at address Disp1 + Register. "SP" is either SP0 or SP1, as selected in PSR.
10001	Stack memory relative	disp2(disp1(SP))	
10010	Static memory relative	disp2(disp1(SB))	
Reserved			
10011	(Reserved for Future Use)		
Immediate			
10100	Immediate	value	None: Operand is input from instruction queue.
Absolute			
10101	Absolute	@disp	Disp.
External			
10110	External	EXT (disp1) + disp2	Disp2 + Pointer; Pointer is found at Link Table Entry number Disp1.
Top of Stack			
10111	Top of stack	TOS	Top of current stack, using either User or Interrupt Stack Pointer, as selected in PSR. Automatic Push/Pop included.
Memory Space			
11000	Frame memory	disp(FP)	Disp + Register; "SP" is either SP0 or SP1, as selected in PSR.
11001	Stack memory	disp(SP)	
11010	Static memory	disp(SB)	
11011	Program memory	*+disp	
Scaled Index			
11100	Index, bytes	mode[Rn:B]	EA (mode) + Rn.
11101	Index, words	mode[Rn:W]	EA (mode) + 2× Rn.
11110	Index, double words	mode[Rn:D]	EA (mode) + 4× Rn.
11111	Index, quad words	mode[Rn:Q]	EA (mode) + 8 × Rn. 'Mode' and 'n' are contained within the Index Byte. EA (mode) denotes the effective address generated using mode.

2.0 Architectural Description (Continued)

TABLE 2-2
NS32032 Instruction Set Summary

MOVES

Format	Operation	Operands	Description
4	MOVi	gen,gen	Move a value.
2	MOVQi	short,gen	Extend and move a signed 4-bit constant.
7	MOVMi	gen,gen,disp	Move Multiple: disp bytes (1 to 16).
7	MOVZBW	gen,gen	Move with zero extension.
7	MOVZiD	gen,gen	Move with zero extension.
7	MOVXBW	gen,gen	Move with sign extension.
7	MOVXiD	gen,gen	Move with sign extension.
4	ADDR	gen,gen	Move Effective Address.

INTEGER ARITHMETIC

Format	Operation	Operands	Description
4	ADDI	gen,gen	Add.
2	ADDQi	short,gen	Add signed 4-bit constant.
4	ADDCi	gen,gen	Add with carry.
4	SUBi	gen,gen	Subtract.
4	SUBCi	gen,gen	Subtract with carry (borrow).
6	NEGi	gen,gen	Negate (2's complement).
6	ABSi	gen,gen	Take absolute value.
7	MULi	gen,gen	Multiply
7	QUOi	gen,gen	Divide, rounding toward zero.
7	REMi	gen,gen	Remainder from QUO.
7	DIVi	gen,gen	Divide, rounding down.
7	MODi	gen,gen	Remainder from DIV (Modulus).
7	MEIi	gen,gen	Multiply to Extended Integer.
7	DEIi	gen,gen	Divide Extended Integer.

PACKED DECIMAL (BCD) ARITHMETIC

Format	Operation	Operands	Description
6	ADDPi	gen,gen	Add Packed.
6	SUBPi	gen,gen	Subtract Packed.

INTEGER COMPARISON

Format	Operation	Operands	Description
4	CMPi	gen,gen	Compare.
2	CMPQi	short,gen	Compare to signed 4-bit constant.
7	CMPMi	gen,gen,disp	Compare Multiple: disp bytes (1 to 16).

LOGICAL AND BOOLEAN

Format	Operation	Operands	Description
4	ANDi	gen,gen	Logical AND.
4	ORi	gen,gen	Logical OR.
4	BICi	gen,gen	Clear selected bits.
4	XORi	gen,gen	Logical Exclusive OR.
6	COMi	gen,gen	Complement all bits.
6	NOTi	gen,gen	Boolean complement: LSB only.
2	Scondi	gen	Save condition code (cond) as a Boolean variable of size i.

2.0 Architectural Description (Continued)

TABLE 2-2 (Continued)
NS32032 Instruction Set Summary (Continued)

SHIFTS

Format	Operation	Operands	Description
6	LSHi	gen,gen	Logical Shift, left or right.
6	ASHi	gen,gen	Arithmetic Shift, left or right.
6	ROTi	gen,gen	Rotate, left or right.

BITS

Format	Operation	Operands	Description
4	TBITi	gen,gen	Test bit.
6	SBITi	gen,gen	Test and set bit.
6	SBITIi	gen,gen	Test and set bit, interlocked
6	CBITi	gen,gen	Test and clear bit.
6	CBITIi	gen,gen	Test and clear bit, interlocked.
6	IBITi	gen,gen	Test and invert bit.
8	FFSi	gen,gen	Find first set bit

BIT FIELDS

Bit fields are values in memory that are not aligned to byte boundaries. Examples are PACKED arrays and records used in Pascal. "Extract" instructions read and align a bit field. "Insert" instructions write a bit field from an aligned source.

Format	Operation	Operands	Description
8	EXTi	reg,gen,gen,disp	Extract bit field (array oriented).
8	INSi	reg,gen,gen,disp	Insert bit field (array oriented).
7	EXTSi	gen,gen,imm,imm	Extract bit field (short form).
7	INSSi	gen,gen,imm,imm	Insert bit field (short form).
8	CVTP	reg,gen,gen	Convert to Bit Field Pointer.

ARRAYS

Format	Operation	Operands	Description
8	CHECKi	reg,gen,gen	Index bounds check.
8	INDEXi	reg,gen,gen	Recursive indexing step for multiple-dimensional arrays.

STRINGS

String instructions assign specific functions to the General Purpose Registers:

R4 - Comparison Value

R3 - Translation Table Pointer

R2 - String 2 Pointer

R1 - String 1 Pointer

R0 - Limit Count

Options on all string instructions are:

B (Backward): Decrement string pointers after each step rather than incrementing.

U (Until match): End instruction if String 1 entry matches R4.

W (While match): End instruction if String 1 entry does not match R4.

All string instructions end when R0 decrements to zero.

Format	Operation	Operands	Descriptions
5	MOVSi	options	Move String 1 to String 2.
	MOVST	options	Move string, translating bytes.
5	CMPSi	options	Compare String 1 to String 2.
	CMPST	options	Compare translating, String 1 bytes.
5	SKPSi	options	Skip over String 1 entries
	SKPST	options	Skip, translating bytes for Until/While.

2.0 Architectural Description (Continued)

TABLE 2-2 (Continued)
NS32032 Instruction Set Summary (Continued)

JUMPS AND LINKAGE

Format	Operation	Operands	Description
3	JUMP	gen	Jump.
0	BR	disp	Branch (PC Relative).
0	Bcond	disp	Conditional branch.
3	CASEi	gen	Multiway branch.
2	ACBi	short,gen,disp	Add 4-bit constant and branch if non-zero.
3	JSR	gen	Jump to subroutine.
1	BSR	disp	Branch to subroutine.
1	CXP	disp	Call external procedure.
3	CXPD	gen	Call external procedure using descriptor.
1	SVC		Supervisor Call.
1	FLAG		Flag Trap.
1	BPT		Breakpoint Trap.
1	ENTER	[reg list],disp	Save registers and allocate stack frame (Enter Procedure).
1	EXIT	[reg list]	Restore registers and reclaim stack frame (Exit Procedure).
1	RET	disp	Return from subroutine.
1	RXP	disp	Return from external procedure call.
1	RETT	disp	Return from trap. (Privileged)
1	RETI		Return from interrupt. (Privileged)

CPU REGISTER MANIPULATION

Format	Operation	Operands	Description
1	SAVE	[reg list]	Save General Purpose Registers.
1	RESTORE	[reg list]	Restore General Purpose Registers.
2	LPRi	areg,gen	Load Dedicated Register. (Privileged if PSR or INTBASE)
2	SPRi	areg,gen	Store Dedicated Register. (Privileged if PSR or INTBASE)
3	ADJSPi	gen	Adjust Stack Pointer.
3	BISPSRi	gen	Set selected bits in PSR. (Privileged if not Byte length)
3	BICPSRi	gen	Clear selected bits in PSR. (Privileged if not Byte length)
5	SETCFG	[option list]	Set Configuration Register. (Privileged)

FLOATING POINT

Format	Operation	Operands	Description
11	MOVf	gen,gen	Move a Floating Point value.
9	MOVLF	gen,gen	Move and shorten a Long value to Standard.
9	MOVFL	gen,gen	Move and lengthen a Standard value to Long.
9	MOVif	gen,gen	Convert any integer to Standard or Long Floating.
9	ROUNDfi	gen,gen	Convert to integer by rounding.
9	TRUNCfi	gen,gen	Convert to integer by truncating, toward zero.
9	FLOORfi	gen,gen	Convert to largest integer less than or equal to value.
11	ADDf	gen,gen	Add.
11	SUBf	gen,gen	Subtract.
11	MULf	gen,gen	Multiply.
11	DIVf	gen,gen	Divide.
11	CMPf	gen,gen	Compare.
11	NEGf	gen,gen	Negate.
11	ABSf	gen,gen	Take absolute value.
9	LFSR	gen	Load FSR.
9	SFSR	gen	Store FSR.

MEMORY MANAGEMENT

Format	Operation	Operands	Description
14	LMR	mreg,gen	Load Memory Management Register. (Privileged)
14	SMR	mreg,gen	Store Memory Management Register. (Privileged)
14	RDVAL	gen	Validate address for reading. (Privileged)
14	WRVAL	gen	Validate address for writing. (Privileged)
8	MOVSUi	gen,gen	Move a value from Supervisor Space to User Space. (Privileged)
8	MOVUSi	gen,gen	Move a value from User Space to Supervisor Space. (Privileged)

2.0 Architectural Description (Continued)

TABLE 2-2 (Continued)
NS32032 Instruction Set Summary (Continued)

MISCELLANEOUS

Format	Operation	Operands	Description
1	NOP		No Operation.
1	WAIT		Wait for interrupt.
1	DIA		Diagnose. Single-byte "Branch to Self" for hardware breakpointing. Not for use in programming.

CUSTOM SLAVE

Format	Operation	Operands	Description
15.5	CCAL0c	gen,gen	Custom Calculate.
15.5	CCAL1c	gen,gen	
15.5	CCAL2c	gen,gen	
15.5	CCAL3c	gen,gen	
15.5	CMOV0c	gen,gen	Custom Move.
15.5	CMOV1c	gen,gen	
15.5	CMOV2c	gen,gen	
15.5	CMOV3c	gen,gen	
15.5	CCMP0c	gen,gen	Custom Compare.
15.5	CCMP1c	gen,gen	
15.1	CCV0ci	gen,gen	Custom Convert.
15.1	CCV1ci	gen,gen	
15.1	CCV2ci	gen,gen	
15.1	CCV3ic	gen,gen	
15.1	CCV4DQ	gen,gen	
15.1	CCV5QD	gen,gen	
15.1	LCSR	gen	Load Custom Status Register.
15.1	SCSR	gen	Store Custom Status Register.
15.0	CATST0	gen	Custom Address/Test. (Privileged)
15.0	CATST1	gen	(Privileged)
15.0	LCR	creg,gen	Load Custom Register. (Privileged)
15.0	SCR	creg,gen	Store Custom Register. (Privileged)

3.0 Functional Description

3.1 POWER AND GROUNDING

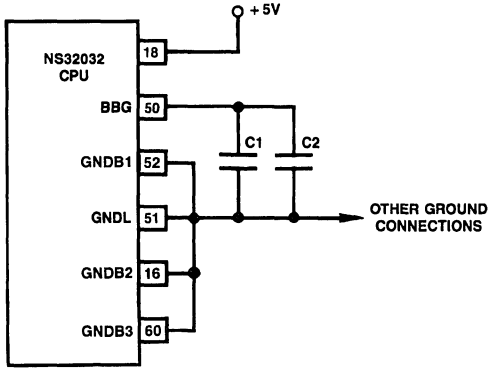
The NS32032 requires a single 5-volt power supply, applied on pin 18 (V_{CC}).

Grounding connections are made on four pins. Logic Ground (GNDL, pin 54) is the common pin for on-chip logic, and Buffer Grounds (GNDB1, pin 52 and GNDB2, pin 16 and GNDB3, pin 60) (16) are the common pins for the output drivers. For optimal noise immunity it is recommended that GNDB1 and GNDB2 be connected together through a single conductor, and GNDL be directly connected to the middle point of this conductor. All other ground connections should be made to the common line as shown in *Figure 3-1*.

In addition to V_{CC} and Ground, the NS32032 CPU uses an internally-generated negative voltage. It is necessary to filter this voltage externally by attaching a pair of capacitors (*Fig. 3-1*) from the BBG pin to ground. Recommended values for these are:

C_1: 1 μF, Tantalum.

C_2: 1000 pF, low inductance. This should be either a disc or monolithic ceramic capacitor.



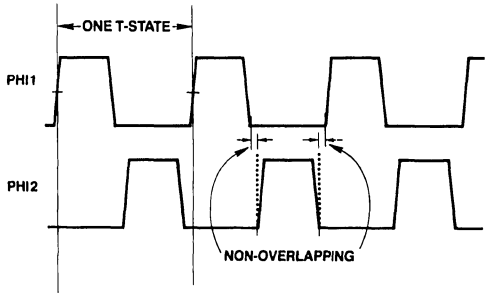
TL/EE/5491–12

FIGURE 3-1. Recommended Supply Connections

3.2 CLOCKING

The NS32032 inputs clocking signals from the Timing Control Unit (TCU), which presents two non-overlapping phases of a single clock frequency. These phases are called PHI1 (pin 26) and PHI2 (pin 27). Their relationship to each other is shown in *Figure 3-2*.

Each rising edge of PHI1 defines a transition in the timing state ("T-State") of the CPU. One T-State represents the execution of one microinstruction within the CPU, and/or one step of an external bus transfer. See Section 4 for complete specifications of PHI1 and PHI2.



TL/EE/5491–13

FIGURE 3-2. Clock Timing Relationships

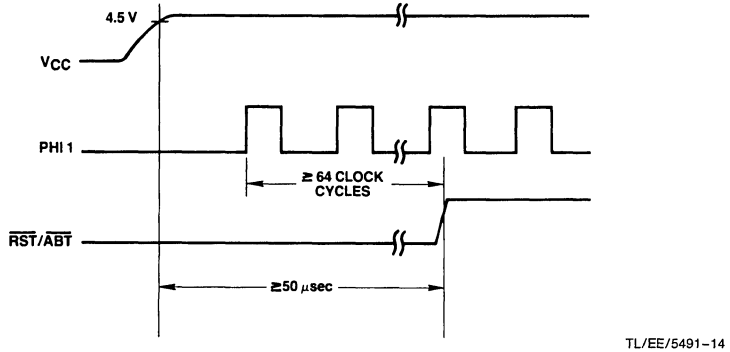
As the TCU presents signals with very fast transitions, it is recommended that the conductors carrying PHI1 and PHI2 be kept as short as possible, and that they not be connected anywhere except from the TCU to the CPU and, if present, the MMU. A TTL Clock signal (CTTL) is provided by the TCU for all other clocking.

3.3 RESETTING

The $\overline{RST}/\overline{ABT}$ pin serves both as a Reset for on-chip logic and as the Abort input for Memory-Managed systems. For its use as the Abort Command, see Sec. 3.5.4.

The CPU may be reset at any time by pulling the $\overline{RST}/\overline{ABT}$ pin low for at least 64 clock cycles. Upon detecting a reset, the CPU terminates instruction processing, resets its internal logic, and clears the Program Counter (PC) and Processor Status Register (PSR) to all zeroes.

On application of power, $\overline{RST}/\overline{ABT}$ must be held low for at least 50 μsec after V_{CC} is stable. This is to ensure that all on-chip voltages are completely stable before operation. Whenever a Reset is applied, it must also remain



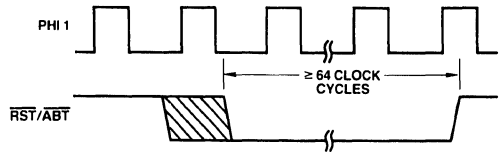
TL/EE/5491–14

FIGURE 3-3. Power-on Reset Requirements

3.0 Functional Description (Continued)

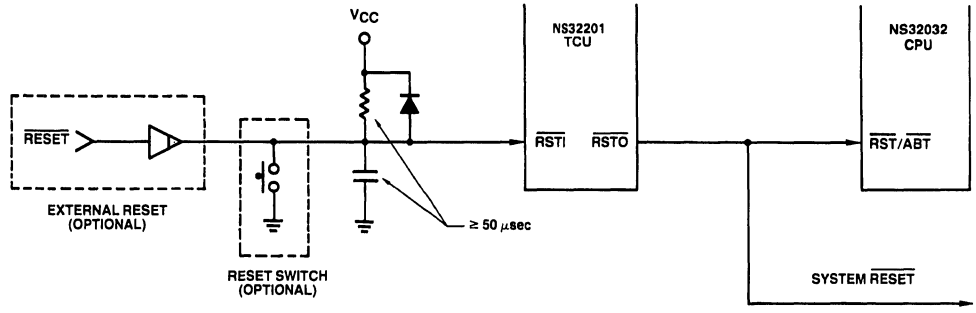
active for not less than 64 clock cycles. The rising edge must occur while PHI1 is high. See *Figures 3-3* and *3-4*.

The NS32201 Timing Control Unit (TCU) provides circuitry to meet the Reset requirements of the NS32032 CPU. *Figure 3-5a* shows the recommended connections for a non-Memory-Managed system. *Figure 3-5b* shows the connections for a Memory-Managed system.



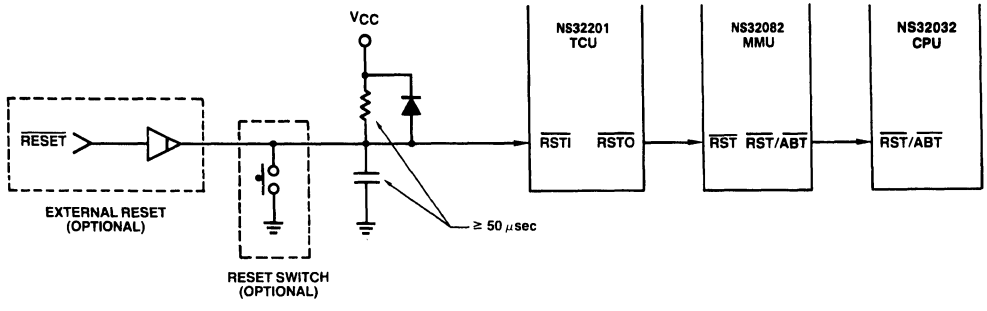
TL/EE/5491–15

FIGURE 3-4. General Reset Timing



TL/EE/5491–16

FIGURE 3-5a. Recommended Reset Connections, Non-Memory-Managed System



TL/EE/5491–17

FIGURE 3-5b. Recommended Reset Connections, Memory-Managed System

3.4 BUS CYCLES

The NS32032 CPU has a strap option which defines the Bus Timing Mode as either With or Without Address Translation. This section describes only bus cycles under the No Address Translation option. For details of the use of the strap and of bus cycles with address translation, see Sec. 3.5.

The CPU will perform a bus cycle for one of the following reasons:

1) To write or read data, to or from memory or a peripheral interface device. Peripheral input and output are memory-mapped in the Series 32000 family.
2) To fetch instructions into the eight-byte instruction queue. This happens whenever the bus would otherwise be idle and the queue is not already full.
3) To acknowledge an interrupt and allow external circuitry to provide a vector number, or to acknowledge completion of an interrupt service routine.
4) To transfer information to or from a Slave Processor.

In terms of bus timing, cases 1 through 3 above are identical. For timing specifications, see Sec. 4. The only external difference between them is the four-bit code placed on the Bus Status pins (ST0–ST3). Slave Processor cycles differ in that separate control signals are applied (Sec. 3.4.6).

The sequence of events in a non-Slave bus cycle is shown below in *Figure 3-7* for a Read cycle and *Figure 3-8* for a Write cycle. The cases shown assume that the selected memory or interface device is capable of communicating with the CPU at full speed. If it is not, then cycle extension may be requested through the RDY line (Sec. 3.4.1).

3.0 Functional Description (Continued)

A full-speed bus cycle is performed in four cycles of the PHI1 clock signal, labeled T1 through T4. Clock cycles not associated with a bus cycle are designated Ti (for "Idle").

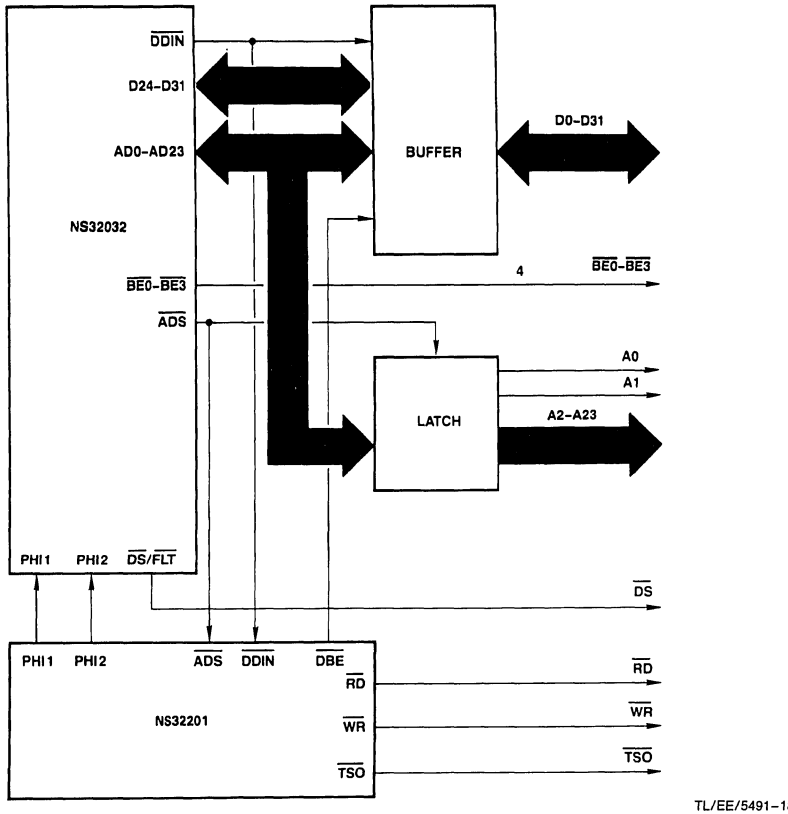
During T1, the CPU applies an address on pins AD0–AD23. It also provides a low-going pulse on the ADS pin, which serves the dual purpose of informing external circuitry that a bus cycle is starting and of providing control to an external latch for demultiplexing Address bits 0–23 from the AD0–AD23 pins. See *Figure 3-6*. During this time also the status signals DDIN, indicating the direction of the transfer, and $\overline{BE0}$–$\overline{BE3}$, indicating which of the four bus bytes are to be referenced, become valid.

During T2 the CPU switches the Data Bus, AD0–AD31 to either accept or present data. It also starts the data strobe ($\overline{DS}$), signalling the beginning of the data transfer. Associated signals from the NS32201 Timing Control Unit are also activated at this time: $\overline{RD}$ (Read Strobe) or $\overline{WR}$ (Write Strobe), $\overline{TSO}$ (Timing State Output, indicating that T2 has been reached) and DBE (Data Buffer Enable).

The T3 state provides for access time requirements, and it occurs at least once in a bus cycle. At the end of T2 or T3, on the falling edge of the PHI2 clock, the RDY (Ready) line is sampled to determine whether the bus cycle will be extended (Sec. 3.4.1).

If the CPU is performing a Read cycle, the Data Bus (AD0–AD31) is sampled at the falling edge of PHI2 of the last T3 state. See Section 4. Data must, however, be held at least until the beginning of T4. $\overline{DS}$ and $\overline{RD}$ are guaranteed not to go inactive before this point, so the rising edge of either of them may safely be used to disable the device providing the input data.

The T4 state finishes the bus cycle. At the beginning of T4, the $\overline{DS}$, $\overline{RD}$ or $\overline{WR}$, and $\overline{TSO}$ signals go inactive, and at the rising edge of PHI2, $\overline{DBE}$ goes inactive, having provided for necessary data hold times. Data during Write cycles remains valid from the CPU throughout T4. Note that the Bus Status lines (ST0–ST3) change at the beginning of T4, anticipating the following bus cycle (if any).



TL/EE/5491–18

FIGURE 3-6. Bus Connections

3.0 Functional Description (Continued)

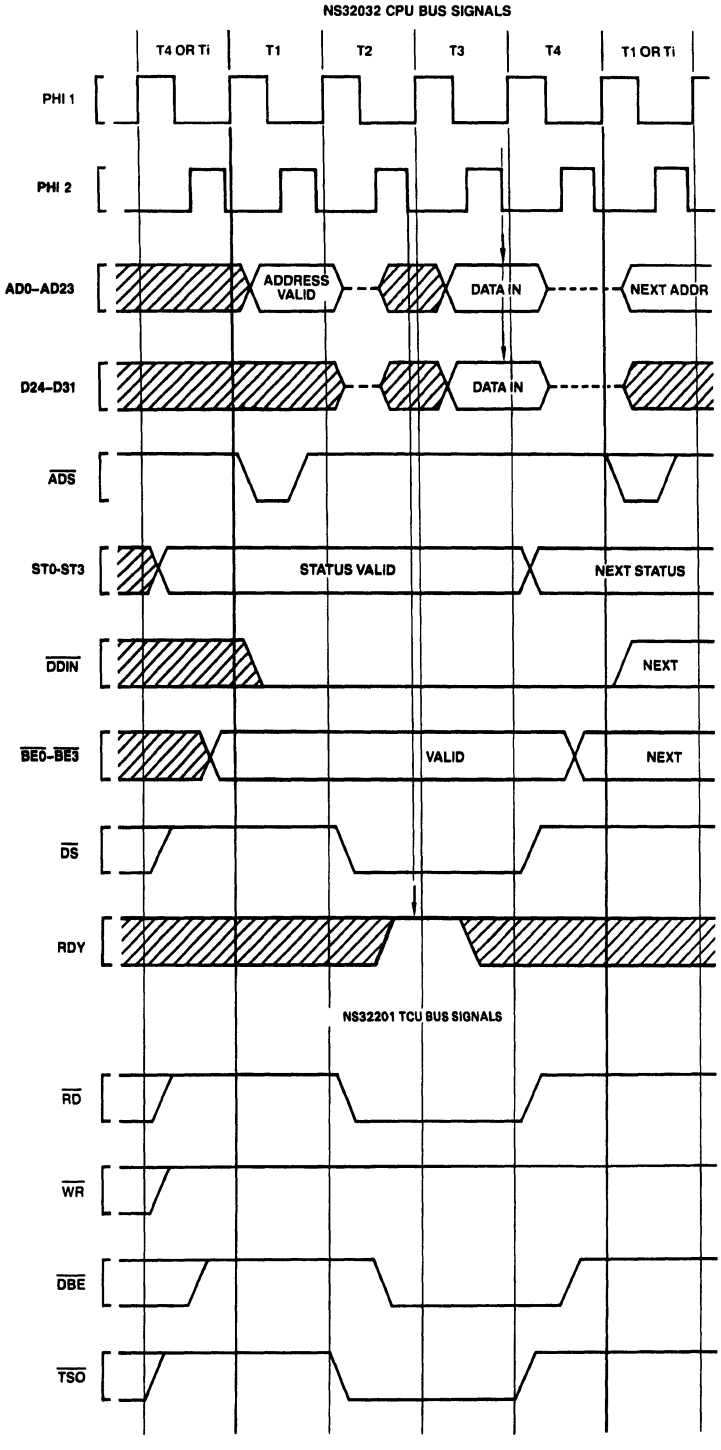
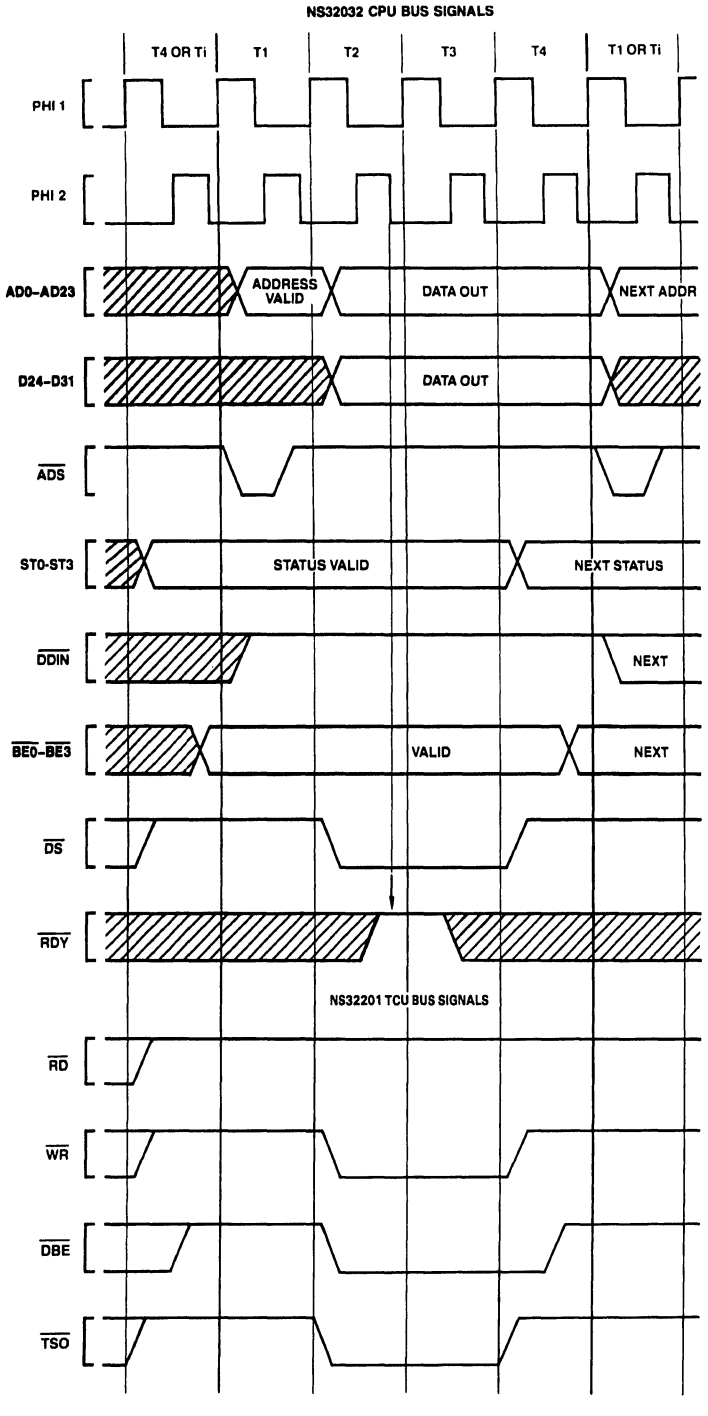


FIGURE 3-7. Read Cycle Timing

3.0 Functional Description (Continued)



TL/EE/5491–19

FIGURE 3-8. Write Cycle Timing

3.0 Functional Description (Continued)

3.4.1 Cycle Extension

To allow sufficient strobe widths and access times for any speed of memory or peripheral device, the NS32032 provides for extension of a bus cycle. Any type of bus cycle except a Slave Processor cycle can be extended.

In *Figures 3-7* and *3-8*, note that during T3 all bus control signals from the CPU and TCU are flat. Therefore, a bus cycle can be cleanly extended by causing the T3 state to be repeated. This is the purpose of the RDY (Ready) pin.

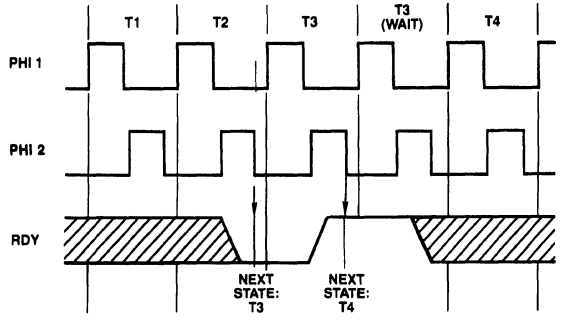
At the end of T2 on the falling edge of PHI2, the RDY line is sampled by the CPU. If RDY is high, the next T-states will be T3 and then T4, ending the bus cycle. If RDY is low, then another T3 state will be inserted after the next T-state and the RDY line will again be sampled on the falling edge of PHI2. Each additional T3 state after the first is referred to as a "WAIT STATE". See *Figure 3-9*.

The RDY pin is driven by the NS32201 Timing Control Unit, which applies WAIT States to the CPU as requested on three sets of pin:

1) $\overline{\text{CWAIT}}$ (Continuous WAIT), which holds the CPU in WAIT states until removed.
2) $\overline{\text{WAIT1}}$, $\overline{\text{WAIT2}}$, $\overline{\text{WAIT4}}$, $\overline{\text{WAIT8}}$ (Collectively $\overline{\text{WAITn}}$), which may be given a four-bit binary value requesting a specific number of WAIT States from 0 to 15.
3) $\overline{\text{PER}}$ (Peripheral), which inserts five additional WAIT states and causes the TCU to reshape the $\overline{\text{RD}}$ and $\overline{\text{WR}}$ strobes. This provides the setup and hold times required by most MOS peripheral interface devices.

Combinations of these various WAIT requests are both legal and useful. For details of their use, see the NS32201 Data Sheet.

Figure 3-10 illustrates a typical Read cycle, with two WAIT states requested through the TCU $\overline{\text{WAIT}}$n pins.



TL/EE/5491–21

FIGURE 3-9. RDY Pin Timing

3.4.2 Bus Status

The NS32032 CPU presents four bits of Bus Status information on pins ST0–ST3. The various combinations on these pins indicate why the CPU is performing a bus cycle, or, if it is idle on the bus, then why is it idle.

Referring to *Figures 3-7* and *3-8*, note that Bus Status leads the corresponding Bus Cycle, going valid one clock cycle before T1, and changing to the next state at T4. This allows the system designer to fully decode the Bus Status and, if desired, latch the decoded signals before $\overline{\text{ADS}}$ initiates the Bus Cycle.

The Bus Status pins are interpreted as a four-bit value, with ST0 the least significant bit. Their values decode as follows:

0000 – The bus is idle because the CPU does not need to perform a bus access.

0001 – The bus is idle because the CPU is executing the WAIT instruction.

0010 – (Reserved for future use.)

0011 – The bus is idle because the CPU is waiting for a Slave Processor to complete an instruction.

0100 – Interrupt Acknowledge, Master.

The CPU is performing a Read cycle. To acknowledge receipt of a Non-Maskable Interrupt (on $\overline{\text{NMI}}$) it will read from address FFFF00_{16}, but will ignore any data provided.

To acknowledge receipt of a Maskable Interrupt (on $\overline{\text{INT}}$) it will read from address FFFE00_{16}, expecting a vector number to be provided from the Master NS32202 Interrupt Control Unit. If the vectoring mode selected by the last SETCFG instruction was Non-Vectored, then the CPU will ignore the value it has read and will use a default vector instead, having assumed that no NS32202 is present. See Sec. 3.4.5.

0101 – Interrupt Acknowledge, Cascaded.

The CPU is reading a vector number from a Cascaded NS32202 Interrupt Control Unit. The address provided is the address of the NS32202 Hardware Vector register. See Sec. 3.4.5.

0110 – End of Interrupt, Master.

The CPU is performing a Read cycle to indicate that it is executing a Return from Interrupt (RETI) instruction. See Sec. 3.4.5.

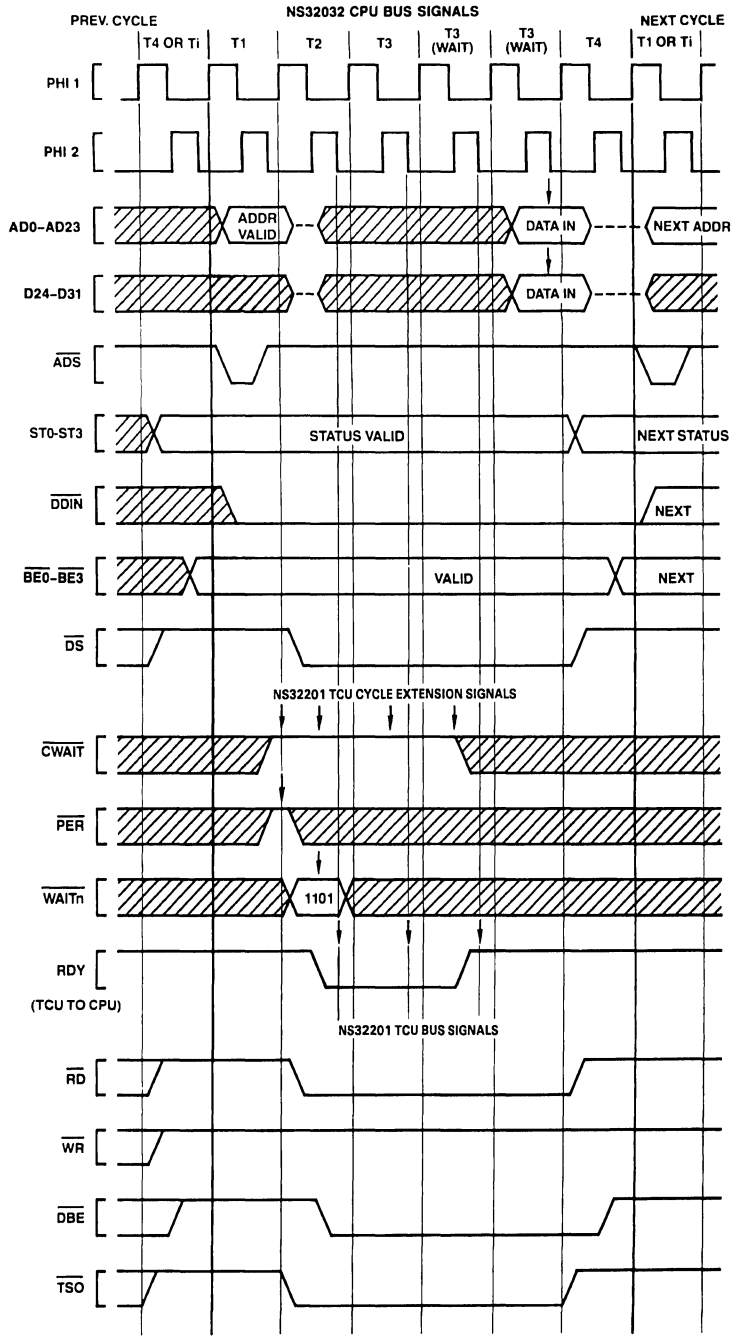
0111 – End of Interrupt, Cascaded.

The CPU is reading from a Cascaded Interrupt Control Unit to indicate that it is returning (through RETI) from an interrupt service routine requested by that unit. See Sec. 3.4.5.

1000 – Sequential Instruction Fetch.

The CPU is reading the next sequential word from the instruction stream into the Instruction

3.0 Functional Description (Continued)



TL/EE/5491–22

FIGURE 3-10. Extended Cycle Example

Note: Arrows on CWAIT, PER, WAITn indicate points at which the TCU samples. Arrows on AD0–AD15 and RDY indicate points at which the CPU samples.

3.0 Functional Description (Continued)

Queue. It will do so whenever the bus would otherwise be idle and the queue is not already full.

1001 – Non-Sequential Instruction Fetch.

The CPU is performing the first fetch of instruction code after the Instruction Queue is purged. This will occur as a result of any jump or branch, or any interrupt or trap, or execution of certain instructions.

1010 – Data Transfer.

The CPU is reading or writing an operand of an instruction.

1011 – Read RMW Operand.

The CPU is reading an operand which will subsequently be modified and rewritten. If memory protection circuitry would not allow the following Write cycle, it must abort this cycle.

1100 – Read for Effective Address Calculation.

The CPU is reading information from memory in order to determine the Effective Address of an operand. This will occur whenever an instruction uses the Memory Relative or External addressing mode.

1101 – Transfer Slave Processor Operand.

The CPU is either transferring an instruction operand to or from a Slave Processor, or it is issuing the Operation Word of a Slave Processor instruction. See Sec. 3.9.1.

1110 – Read Slave Processor Status.

The CPU is reading a Status Word from a Slave Processor. This occurs after the Slave Processor has signalled completion of an instruction. The transferred word tells the CPU whether a trap should be taken, and in some instructions it presents new values for the CPU Processor Status Register bits N, Z, L or F. See Sec. 3.9.1.

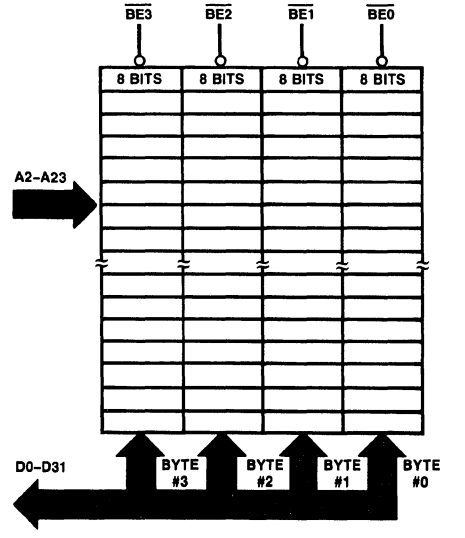
1111 – Broadcast Slave ID.

The CPU is initiating the execution of a Slave Processor instruction. The ID Byte (first byte of the instruction) is sent to all Slave Processors, one of which will recognize it. From this point the CPU is communicating with only one Slave Processor. See Sec. 3.9.1.

3.4.3 Data Access Sequences

The 24-bit address provided by the NS32032 is a byte address; that is, it uniquely identifies one of up to 16,777,216 eight-bit memory locations. An important feature of the NS32032 is that the presence of a 32-bit data bus imposes no restrictions on data alignment; any data item, regardless of size, may be placed starting at any memory address. The NS32032 provides special control signals. Byte Enable ($\overline{BE0}$–$\overline{BE3}$) which facilitate individual byte accessing on a 32-bit bus.

Memory is organized as four eight-bit banks, each bank receiving the double-word address (A2–A23) in parallel. One bank, connected to Data Bus pins AD0–AD7 is enabled when $\overline{BE0}$ is low. The second bank, connected to data bus pins AD8–AD15 is enabled when $\overline{BE1}$ is low. The third and fourth banks are enabled by $\overline{BE2}$ and $\overline{BE3}$, respectively. See *Figure 3-11*.



TL/EE/5491–23

FIGURE 3-11. Memory Interface

Since operands do not need to be aligned with respect to the double-word bus access performed by the CPU, a given double-word access can contain one, two, three, or four bytes of the operand being addressed, and these bytes can begin at various positions, as determined by A1, A0. Table 3-1 lists the 10 resulting access types.

TABLE 3-1
Bus Access Types

Type	Bytes Accessed	A1,A0	$\overline{BE3}$	$\overline{BE2}$	$\overline{BE1}$	$\overline{BE0}$
1	1	00	1	1	1	0
2	1	01	1	1	0	1
3	1	10	1	0	1	1
4	1	11	0	1	1	1
5	2	00	1	1	0	0
6	2	01	1	0	0	1
7	2	10	0	0	1	1
8	3	00	1	0	0	0
9	3	01	0	0	0	1
10	4	00	0	0	0	0

Accesses of operands requiring more than one bus cycle are performed sequentially, with no idle T-States separating them. The number of bus cycles required to transfer an operand depends on its size and its alignment. Table 3-2 lists the bus cycles performed for each situation.

3.0 Functional Description (Continued)

TABLE 3-2
Access Sequences

Cycle	Type	Address	$\overline{BE3}$	$\overline{BE2}$	$\overline{BE1}$	$\overline{BE0}$	Data Bus Byte 3	Byte 2	Byte 1	Byte 0
A. ***Word at address ending with 11***									BYTE 1	BYTE 0 ← A
1.	4	A	0	1	1	1	Byte 0	X	X	X
2.	1	A + 1	1	1	1	0	X	X	X	Byte 1
B. ***Double word at address ending with 01***								BYTE 3	BYTE 2	BYTE 1	BYTE 0 ← A
1.	9	A	0	0	0	1	Byte 2	Byte 1	Byte 0	X
2.	1	A + 3	1	1	1	0	X	X	X	Byte 3
C. ***Double word at address ending with 10***								BYTE 3	BYTE 2	BYTE 1	BYTE 0 ← A
1.	7	A	0	0	1	1	Byte 1	Byte 0	X	X
2.	5	A + 2	1	1	0	0	X	X	Byte 3	Byte 2
D. ***Double word at address ending with 11***								BYTE 3	BYTE 2	BYTE 1	BYTE 0 ← A
1.	4	A	0	1	1	1	Byte 0	X	X	X
2.	8	A + 1	1	0	0	0	X	Byte 3	Byte 2	Byte 1
E. ***Quad word at address ending with 00***							BYTE 7	BYTE 6	BYTE 5	BYTE 4	BYTE 3	BYTE 2	BYTE 1	BYTE 0 ← A
1.	10	A	0	0	0	0	Byte 3	Byte 2	Byte 1	Byte 0
Other bus cycles (instruction prefetch or slave) can occur here.										
2.	10	A + 4	0	0	0	0	Byte 7	Byte 6	Byte 5	Byte 4
F. ***Quad word at address ending with 01***							BYTE 7	BYTE 6	BYTE 5	BYTE 4	BYTE 3	BYTE 2	BYTE 1	BYTE 0 ← A
1.	9	A	0	0	0	1	Byte 2	Byte 1	Byte 0	X
2.	1	A + 3	1	1	1	0	X	X	X	Byte 3
Other bus cycles (instruction prefetch or slave) can occur here.										
3.	9	A + 4	0	0	0	1	Byte 6	Byte 5	Byte 4	X
4.	1	A + 7	1	1	1	0	X	X	X	Byte 7
G. ***Quad word at address ending with 10***							BYTE 7	BYTE 6	BYTE 5	BYTE 4	BYTE 3	BYTE 2	BYTE 1	BYTE 0 ← A
1.	7	A	0	0	1	1	Byte 1	Byte 0	X	X
2.	5	A + 2	1	1	0	0	X	X	Byte 3	Byte 2
Other bus cycles (instruction prefetch or slave) can occur here.										
3.	7	A + 4	0	0	1	1	Byte 5	Byte 4	X	X
4.	5	A + 6	1	1	0	0	X	X	Byte 7	Byte 6
H. ***Quad word at address ending with 11***							BYTE 7	BYTE 6	BYTE 5	BYTE 4	BYTE 3	BYTE 2	BYTE 1	BYTE 0 ← A
1.	4	A	0	1	1	1	Byte 0	X	X	X
2.	8	A + 1	1	0	0	0	X	Byte 3	Byte 2	Byte 1
Other bus cycles (instruction prefetch or slave) can occur here.										
1.	4	A + 4	0	1	1	1	Byte 4	X	X	X
2.	8	A + 5	1	0	0	0	X	Byte 7	Byte 6	Byte 5

X = Don't Care

3.0 Functional Description (Continued)

3.4.3.1 Bit Accesses

The Bit Instructions perform byte accesses to the byte containing the designated bit. The Test and Set Bit instruction (SBIT), for example, reads a byte, alters it, and rewrites it, having changed the contents of one bit.

3.4.3.2 Bit Field Accesses

An access to a Bit Field in memory always generates a Double-Word transfer at the address containing the least significant bit of the field. The Double Word is read by an Extract instruction; an Insert instruction reads a Double Word, modifies it, and rewrites it.

3.4.3.3 Extending Multiply Accesses

The Extending Multiply Instruction (MEI) will return a result which is twice the size in bytes of the operand it reads. If the multiplicand is in memory, the most-significant half of the result is written first (at the higher address), then the least-significant half. This is done in order to support retry if this instruction is aborted.

3.4.4 Instruction Fetches

Instructions for the NS32032 CPU are "prefetched"; that is, they are input before being needed into the next available entry of the eight-byte Instruction Queue. The CPU performs two types of Instruction Fetch cycles: Sequential and Non-Sequential. These can be distinguished from each other by their differing status combinations on pins ST0–ST3 (Sec. 3.4.2).

A Sequential Fetch will be performed by the CPU whenever the Data Bus would otherwise be idle and the Instruction Queue is not currently full. Sequential Fetches are always type 10 Read cycles (Table 3-1).

A Non-Sequential Fetch occurs as a result of any break in the normally sequential flow of a program. Any jump or branch instruction, a trap or an interrupt will cause the next Instruction Fetch cycle to be Non-Sequential. In addition, certain instructions flush the instruction queue, causing the next instruction fetch to display Non-Sequential status. Only the first bus cycle after a break displays Non-Sequential status, and that cycle depends on the destination address.

Note: During non-sequential fetches, $\overline{BE0}$–$\overline{BE3}$ are all active regardless of the alignment.

3.4.5 Interrupt Control Cycles

Activating the $\overline{INT}$ or $\overline{NMI}$ pin on the CPU will initiate one or more bus cycles whose purpose is interrupt control rather than the transfer of instructions or data. Execution of the Return from Interrupt instruction (RETI) will also cause Interrupt Control bus cycles. These differ from instruction or data transfers only in the status pesented on pins ST0–ST3. All Interrupt Control cycles are single-byte Read cycles.

This section describes only the Interrupt Control sequences associated with each interrupt and with the return from its service routine. For full details of the NS32032 interrupt structure, see Sec. 3.8.

3.0 Functional Description (Continued)

TABLE 3-3
Interrupt Sequences

								Data Bus			
Cycle	**Status**	**Address**	**$\overline{DDIN}$**	**$\overline{BE3}$**	**$\overline{BE2}$**	**$\overline{BE1}$**	**$\overline{BE0}$**	**Byte 3**	**Byte 2**	**Byte 1**	**Byte 0**
				A. Non-Maskable Interrupt Control Sequences							
Interrupt Acknowledge											
1	0100	$FFFF00_{16}$	0	1	1	1	0	X	X	X	X
Interrupt Return											
None: Performed through Return from Trap (RETT) instruction.											
				B. Non-Vectored Interrupt Control Sequences							
Interrupt Acknowledge											
1	0100	$FFFE00_{16}$	0	1	1	1	0	X	X	X	X
Interrupt Return											
1	0110	$FFFE00_{16}$	0	1	1	1	0	X	X	X	X
				C. Vectored Interrupt Sequences: Non-Cascaded.							
Interrupt Acknowledge											
1	0100	$FFFE00_{16}$	0	1	1	1	0	X	X	X	Vector: Range: 0-127
Interrupt Return											
1	0110	$FFFE00_{16}$	0	1	1	1	0	X	X	X	Vector: Same as in Previous Int. Ack. Cycle
				D. Vectored Interrupt Sequences: Cascaded							
Interrupt Acknowledge											
1	0100	$FFFE00_{16}$	0	1	1	1	0	X	X	X	Cascade Index: range −16 to −1
(The CPU here uses the Cascade Index to find the Cascade Address.)											
2	0101	Cascade Address	0			See Note		Vector, range 9–255; on appropriate byte of data bus.			
Interrupt Return											
1	0110	$FFFE00_{16}$	0	1	1	1	0	X	X	X	Cascade Index: Same as in previous Int. Ack. Cycle
(The CPU here uses the Cascade Index to find the Cascade Address)											
2	0111	Cascade Address	0			See Note		X	X	X	X

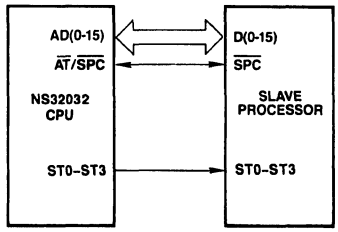
X = Don't Care

Note: $\overline{BE0}$-$\overline{BE3}$ signals will be activated according to the cascaded ICU address. The cycle type can be 1, 2, 3 or 4, when reading the interrupt vector. The vector value can be in the range 0–255.

3.0 Functional Description (Continued)

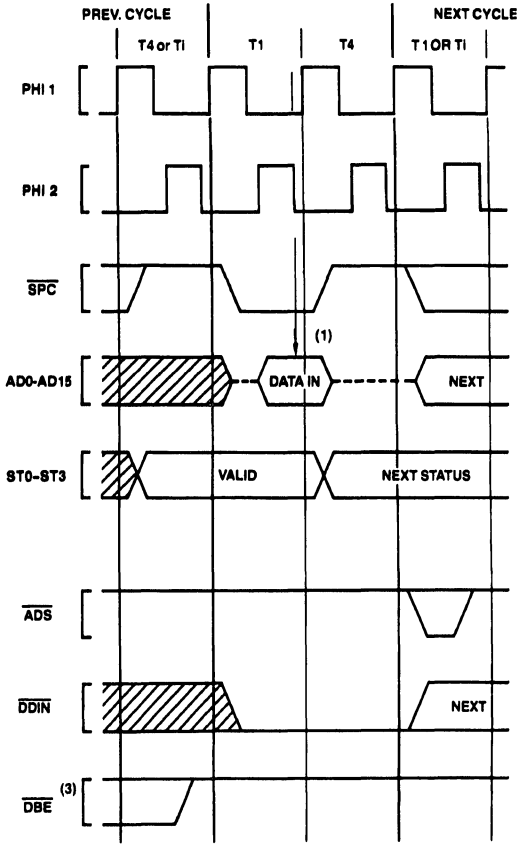
3.4.6 Slave Processor Communication

In addition to its use as the Address Translation strap (Sec. 3.5.1), the $\overline{AT}/\overline{SPC}$ pin is used as the data strobe for Slave Processor transfers. In this role, it is referred to as Slave Processor Control ($\overline{SPC}$). In a Slave Processor bus cycle, data is transferred on the Data Bus (AD0–AD15), and the status lines (ST0–ST3) are monitored by each Slave Processor in order to determine the type of transfer being performed. $\overline{SPC}$ is bidirectional, but is driven by the CPU during all Slave Processor bus cycles. See Sec. 3.9 for full protocol sequences.



TL/EE/5491–24

FIGURE 3-12. Slave Processor Connections



TL/EE/5491–25

Note:

(1) CPU samples Data Bus here.

(2) $\overline{DBE}$ and all other NS32201 TCU bus signals remain inactive because no $\overline{ADS}$ pulse is received from the CPU.

FIGURE 3-13. CPU Read from Slave Processor

3.0 Functional Description (Continued)

3.4.6.1 Slave Processor Bus Cycles

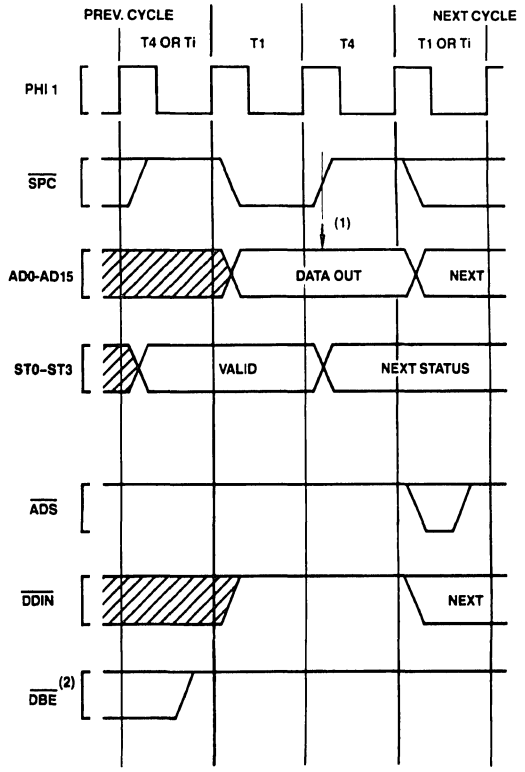
A Slave Processor bus cycle always takes exactly two clock cycles, labeled T1 and T4 (see *Figures 3-13* and *3-14*). During a Read cycle $\overline{SPC}$ is active from the beginning of T1 to the beginning of T4, and the data is sampled at the end of T1. The Cycle Status pins lead the cycle by one clock period, and are sampled at the leading edge of $\overline{SPC}$. During a Write cycle, the CPU applies data and activates $\overline{SPC}$ at T1, removing $\overline{SPC}$ at T4. The Slave Processor latches status on the leading edge of $\overline{SPC}$ and latches data on the trailing edge.

Since the CPU does not pulse the Address Strobe ($\overline{ADS}$), no bus signals are generated by the NS32201 Timing Control Unit. The direction of a transfer is determined by the sequence ("protocol") established by the instruction under execution; but the CPU indicates the direction on the $\overline{DDIN}$ pin for hardware debugging purposes.

3.4.6.2 Slave Operand Transfer Sequences

A Slave Processor operand is transferred in one or more Slave bus cycles. A Byte operand is transferred on the least-significant byte of the Data Bus (AD0–AD7), and a Word operand is transferred on bits AD0–AD15. A Double Word is transferred in a consecutive pair of bus cycles, least-significant word first. A Quad Word is transferred in two pairs of Slave cycles, with other bus cycles possibly occurring between them. The word order is from least-significant word to most-significant.

Note that the NS32032 uses only the two least significant bytes of the data bus for slave cycles. This is to maintain compatibility with existing slave processors.



TL/EE/5491–26

Note:

(1) Slave Processor samples Data Bus here.

(2) $\overline{DBE}$, being provided by the NS32201 TCU, remains inactive due to the fact that no pulse is presented on $\overline{ADS}$. TCU signals $\overline{RD}$, $\overline{WR}$ and $\overline{TSO}$ also remain inactive.

FIGURE 3-14. CPU Write to Slave Processor

3.0 Functional Description (Continued)

3.5 MEMORY MANAGEMENT OPTION

The NS32032 CPU, in conjunction with the NS32082 Memory Management Unit (MMU), provides full support for address translation, memory protection, and memory allocation techniques up to and including Virtual Memory.

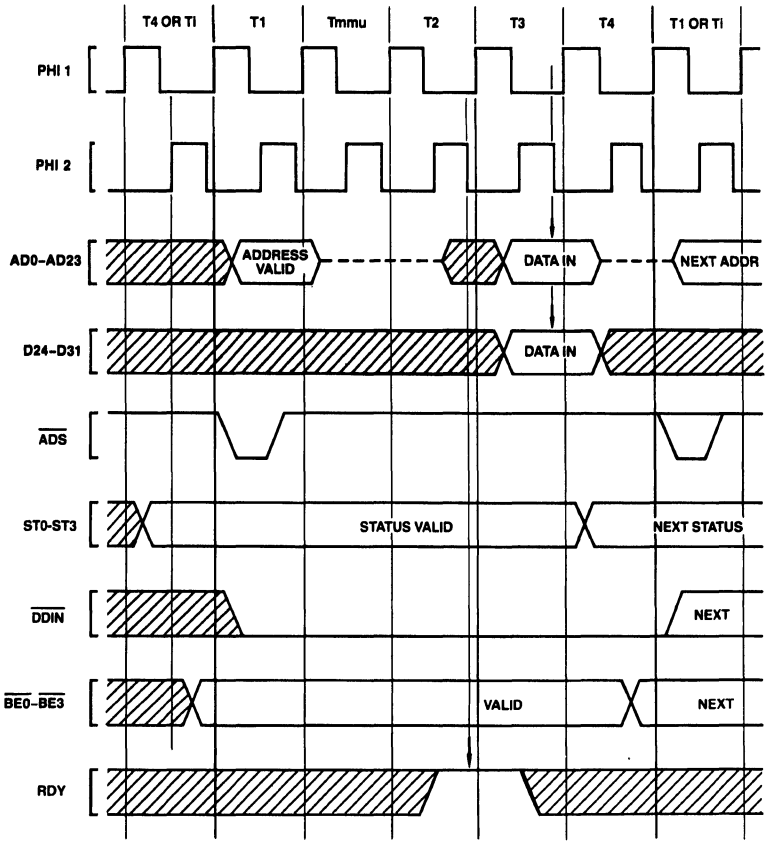
3.5.1 Address Translation Strap

The Bus Interface Control section of the NS32032 CPU has two bus timing modes: With or Without Address Translation. The mode of operation is selected by the CPU by sampling the $\overline{AT}/\overline{SPC}$ (Address Translation/Slave Processor Control) pin on the rising edge of the $\overline{RST}$ (Reset) pulse. If $\overline{AT}/\overline{SPC}$ is sampled as high, the bus timing is as previously described in Sec. 3.4. If it is sampled as low, two changes occur:

1) An extra clock cycle, Tmmu, is inserted into all bus cycles except Slave Processor transfers.
2) The $\overline{DS}/\overline{FLT}$ pin changes in function from a Data Strobe output ($\overline{DS}$) to a Float Command input ($\overline{FLT}$).

The NS32082 MMU will itself pull the CPU $\overline{AT}/\overline{SPC}$ pin low when it is reset. In non-Memory-Managed systems this pin should be pulled up to V_{CC} through a 10 kΩ resistor.

Note that the Address Translation strap does not specifically declare the presence of an NS32082 MMU, but only the



TL/EE/5491-27

FIGURE 3-15. Read Cycle with Address Translation (CPU Action)

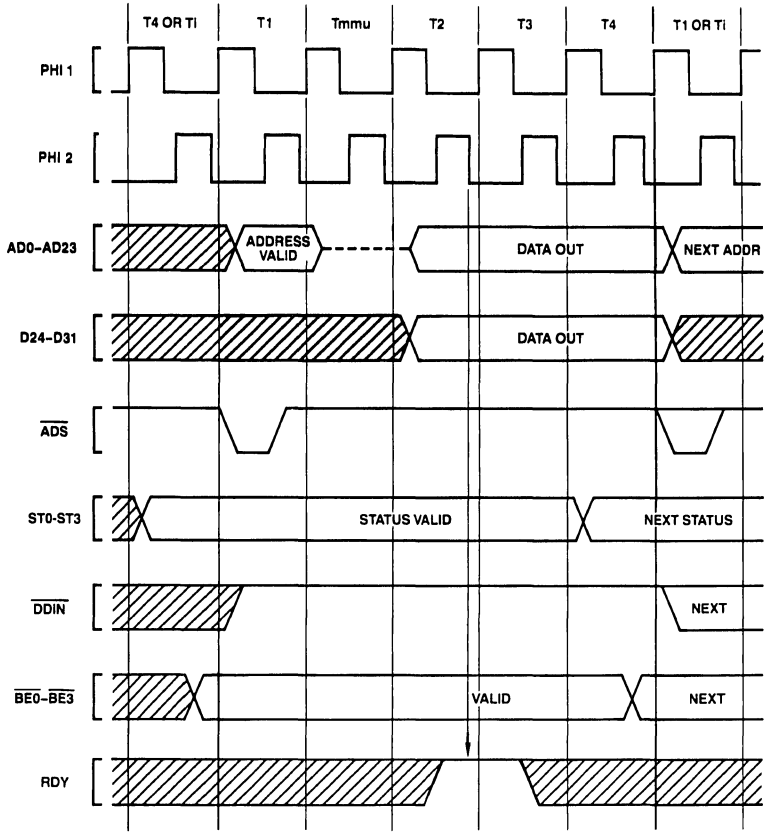
3.0 Functional Description (Continued)

presence of external address translation circuitry. MMU instructions will still trap as being undefined unless the SETCFG (Set Configuration) instruction is executed to declare the MMU instruction set valid. See Sec. 2.1.3.

3.5.2 Translated Bus Timing

Figures 3-15 and *3-16* illustrate the CPU activity during a Read cycle and a Write cycle in Address Translation mode. The additional T-State, Tmmu, is inserted between T1 and T2. During this time the CPU places AD0–AD23 into the TRI-STATE® mode, allowing the MMU to assert the translated address and issue the physical address strobe $\overline{PAV}$. T2 through T4 of the cycle are identical to their counterparts without Address Translation. Note that in order for the NS32082 MMU to operate correctly it must be set to the 32032 mode by forcing A24/$\overline{HBF}$ low during reset. In this mode the bus lines AD16–AD23 are floated after the MMU address has been latched, since they are used by the CPU to transfer data.

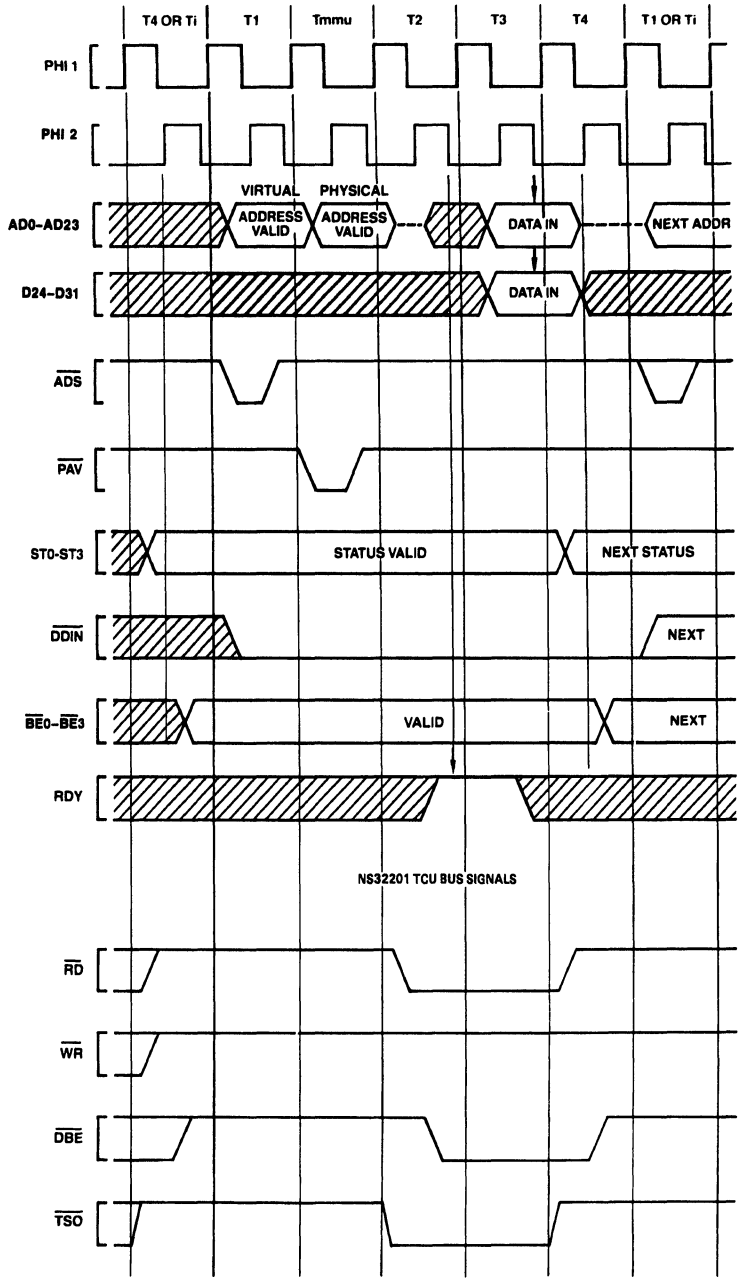
Figures 3-17 and *3-18* show a Read cycle and a Write cycle as generated by the 32032/32082/32201 group. Note that with the CPU $\overline{ADS}$ signal going only to the MMU, and with the MMU $\overline{PAV}$ signal substituting for $\overline{ADS}$ everywhere else, Tmmu through T4 look exactly like T1 through T4 in a non-Memory-Managed system. For the connection diagram, see Appendix B.



TL/EE/5491–28

FIGURE 3-16. Write Cycle with Address Translation (CPU Action)

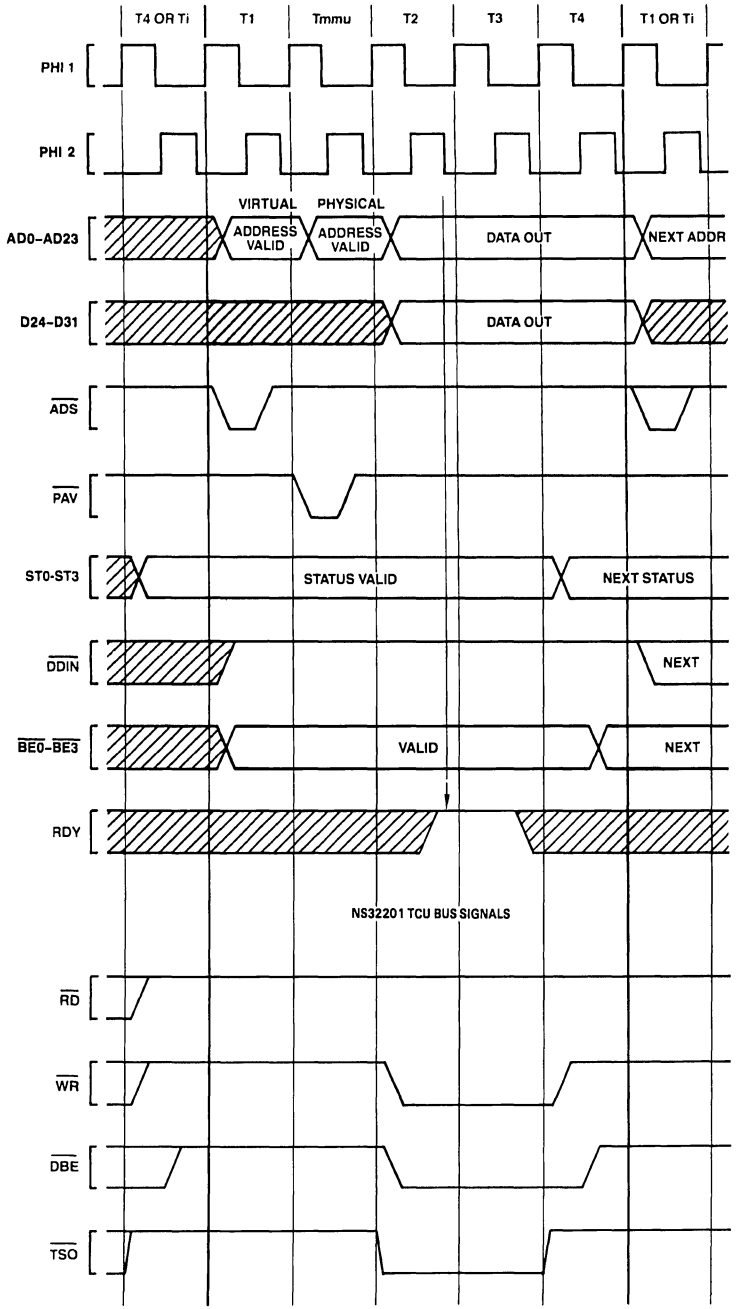
3.0 Functional Description (Continued)



TL/EE/5491-29

FIGURE 3-17. Memory-Managed Read Cycle

3.0 Functional Description (Continued)



TL/EE/5491–30

FIGURE 3-18. Memory-Managed Write Cycle

3.0 Functional Description (Continued)

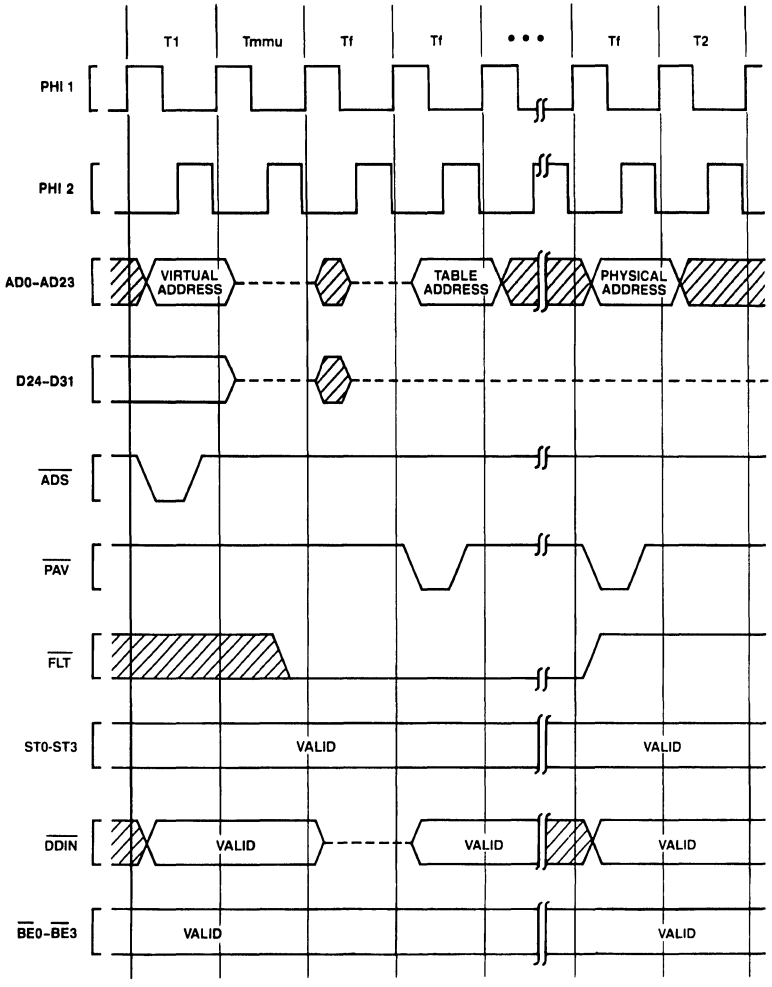
3.5.3 The $\overline{FLT}$ (Float) Pin

The $\overline{FLT}$ pin is used by the CPU for address translation support. Activating $\overline{FLT}$ during Tmmu causes the CPU to wait longer than Tmmu for address translation and validation. This feature is used occasionally by the NS32082 MMU in order to update its translation look-aside buffer (TLB) from page tables in memory, or to update certain status bits within them.

Figure 3-19 shows the effect of $\overline{FLT}$. Upon sampling $\overline{FLT}$ low, late in Tmmu, the CPU enters idle T-States (Tf) during which it:

1) Sets AD0–AD23, D24–D31 and $\overline{DDIN}$ to the TRI-STATE condition ("floating").
2) Suspends further internal processing of the current instruction. This ensures that the current instruction remains abortable with retry. (See $\overline{RST}/\overline{ABT}$ description, Sec. 3.5.4.)

Note that the AD0–AD23 pins may be briefly asserted during the first idle T-State. The above conditions remain in effect until $\overline{FLT}$ again goes high. See the Timing Specifications, Sec. 4.



TL/EE/5491–31

FIGURE 3-19. $\overline{FLT}$ Timing

3.0 Functional Description (Continued)

3.5.4 Aborting Bus Cycles

The RST/ABT pin, apart from its Reset function (Sec. 3.3), also serves as the means to "abort", or cancel, a bus cycle and the instruction, if any, which initiated it. An Abort request is distinguished from a Reset in that the RST/ABT pin is held active for only one clock cycle.

If RST/ABT is pulled low during Tmmu or Tf, this signals that the cycle must be aborted. The CPU itself will enter T2 and then Ti, thereby terminating the cycle. Since it is the MMU PAV signal which triggers a physical cycle, the rest of the system remains unaware that a cycle was started.

The NS32082 MMU will abort a bus cycle for either of two reasons:

1) The CPU is attempting to access a virtual address which is not currently resident in physical memory. The referenced page must be brought into physical memory from mass storage to make it accessible to the CPU.
2) The CPU is attempting to perform an access which is not allowed by the protection level assigned to that page.

When a bus cycle is aborted by the MMU, the instruction that caused it to occur is also aborted in such a manner that it is guaranteed re-executable later. The information that is changed irrecoverably by such a partly-executed instruction does not affect its re-execution.

3.5.4.1 The Abort Interrupt

Upon aborting an instruction, the CPU immediately performs an interrupt through the ABT vector in the Interrupt Table (see Sec. 3.8). The Return Address pushed on the Interrupt Stack is the address of the aborted instruction, so that a Return from Trap (RETT) instruction will automatically retry it.

The one exception to this sequence occurs if the aborted bus cycle was an instruction prefetch. If so, it is not yet certain that the aborted prefetched code is to be executed. Instead of causing an interrupt, the CPU only aborts the bus cycle, and stops prefetching. If the information in the Instruction Queue runs out, meaning that the instruction will actually be executed, the ABT interrupt will occur, in effect aborting the instruction that was being fetched.

3.5.4.2 Hardware Considerations

In order to guarantee instruction retry, certain rules must be followed in applying an Abort to the CPU. These rules are followed by the NS32082 Memory Management Unit.

1) If FLT has not been applied to the CPU, the Abort pulse must occur during or before Tmmu. See the Timing Specifications, *Figure 4-22.*
2) If FLT has been applied to the CPU, the Abort pulse must be applied before the T-State in which FLT goes inactive. The CPU will not actually respond to the Abort command until FLT is removed. See *Figure 4-23.*
3) The Write half of a Read-Modify-Write operand access may not be aborted. The CPU guarantees that this will never be necessary for Memory Management functions by applying a special RMW status (Status Code 1011) during the Read half of the access. When the CPU presents RMW status, that cycle must be aborted if it would be illegal to write to any of the accessed addresses.

If RST/ABT is pulsed at any time other than as indicated above, it will abort either the instruction currently under execution or the next instruction and will act as a very high-priority interrupt. However, the program that was running at the time is not guaranteed recoverable.

3.6 BUS ACCESS CONTROL

The NS32032 CPU has the capability of relinquishing its access to the bus upon request from a DMA device or another CPU. This capability is implemented on the HOLD (Hold Request) and HLDA (Hold Acknowledge) pins. By asserting HOLD low, an external device requests access to the bus. On receipt of HLDA from the CPU, the device may perform bus cycles, as the CPU at this point has set the AD0–AD23, D24–D31, ADS, DDIN and BE0–BE3 pins to the TRI-STATE condition. To return control of the bus to the CPU, the device sets HOLD inactive, and the CPU acknowledges return of the bus by setting HLDA inactive.

How quickly the CPU releases the bus depends on whether it is idle on the bus at the time the HOLD request is made, as the CPU must always complete the current bus cycle. *Figure 3-20* shows the timing sequence when the CPU is idle. In this case, the CPU grants the bus during the immediately following clock cycle. *Figure 3-21* shows the sequence if the CPU is using the bus at the time that the HOLD request is made. If the request is made during or before the clock cycle shown (two clock cycles before T4), the CPU will release the bus during the clock cycle following T4. If the request occurs closer to T4, the CPU may already have decided to initiate another bus cycle. In that case it will not grant the bus until after the next T4 state. Note that this situation will also occur if the CPU is idle on the bus but has initiated a bus cycle internally.

In a Memory-Managed system, the HLDA signal is connected in a daisy-chain through the NS32082, so that the MMU can release the bus if it is using it.

3.0 Functional Description (Continued)

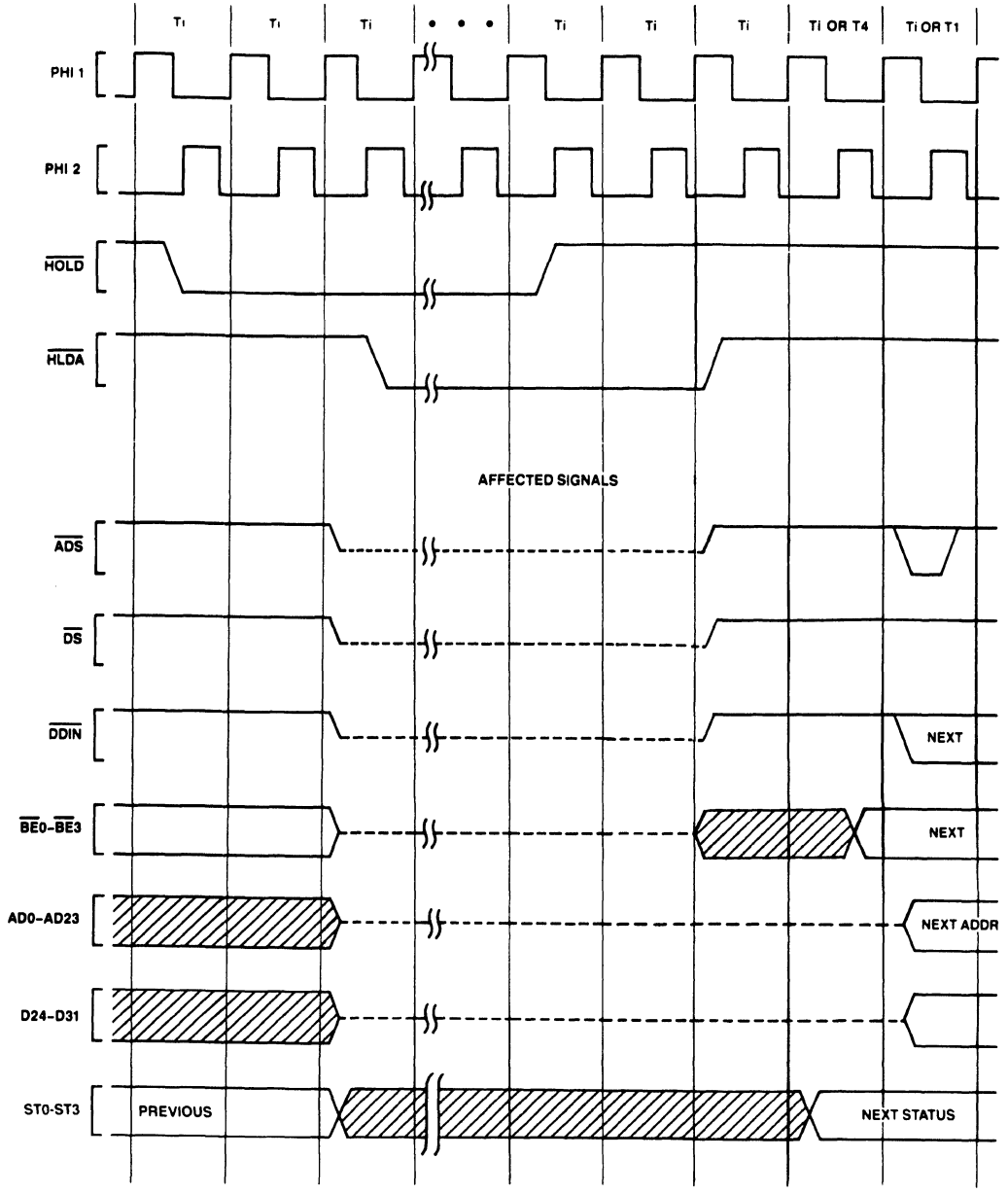


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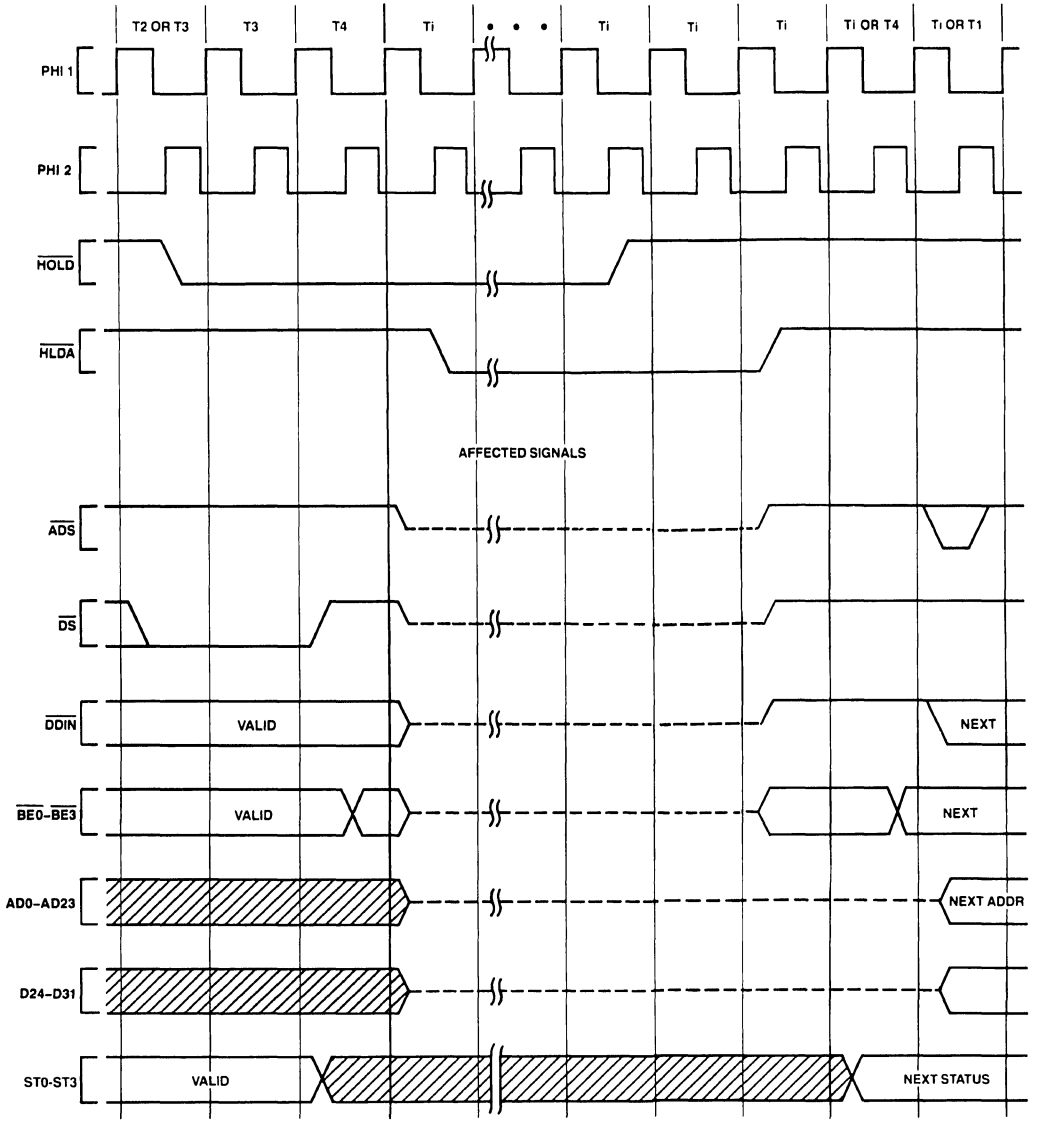
FIGURE 3-20. HOLD Timing, Bus Initially Idle

3.0 Functional Description (Continued)



TL/EE/5491–33

FIGURE 3-21. HOLD Timing, Bus Initially Not Idle

3.0 Functional Description (Continued)

3.7 INSTRUCTION STATUS

In addition to the four bits of Bus Cycle status (ST0–ST3), the NS32032 CPU also presents Instruction Status information on three separate pins. These pins differ from ST0–ST3 in that they are synchronous to the CPU's internal instruction execution section rather than to its bus interface section.

$\overline{PFS}$ (Program Flow Status) is pulsed low as each instruction begins execution. It is intended for debugging purposes, and is used that way by the NS32082 Memory Management Unit.

U/$\overline{S}$ originates from the U bit of the Processor Status Register, and indicates whether the CPU is currently running in User or Supervisor mode. It is sampled by the MMU for mapping, protection, and debugging purposes. Although it is not synchronous to bus cycles, there are guarantees on its validity during any given bus cycle. See the Timing Specifications, *Figure 4-21*.

$\overline{ILO}$ (Interlocked Operation) is activated during an SBITI (Set Bit, Interlocked) or CBITI (Clear Bit, Interlocked) instruction. It is made available to external bus arbitration circuitry in order to allow these instructions to implement the semaphore primitive operations for multi-processor communication and resource sharing. As with the U/$\overline{S}$ pin, there are guarantees on its validity during the operand accesses performed by the instructions. See the Timing Specification Section, *Figure 4-19*.

3.8 NS32032 INTERRUPT STRUCTURE

$\overline{INT}$, on which maskable interrupts may be requested,

$\overline{NMI}$, on which non-maskable interrupts may be requested, and

$\overline{RST}$/$\overline{ABT}$, which may be used to abort a bus cycle and any associated instruction. See Sec. 3.5.4.

In addition there is a set of internally-generated "traps" which cause interrupt service to be performed as a result either of exceptional conditions (e.g., attempted division by zero) or of specific instructions whose purpose is to cause a trap to occur (e.g., the Supervisor Call instruction).

3.8.1 General Interrupt/Trap Sequence

Upon receipt of an interrupt or trap request, the CPU goes through three major steps:

1) Adjustment of Registers.

   Depending on the source of the interrupt or trap, the CPU may restore and/or adjust the contents of the Program Counter (PC), the Processor Status Register (PSR) and the currently-selected Stack Pointer (SP). A copy of the PSR is made, and the PSR is then set to reflect Supervisor Mode and selection of the Interrupt Stack.

2) Vector Acquisition.

   A Vector is either obtained from the Data Bus or is supplied by default.

3) Service Call.

   The Vector is used as an index into the Interrupt Dispatch Table, whose base address is taken from the CPU Interrupt Base (INTBASE) Register. See *Figure 3-22*. A 32-bit External Procedure Descriptor is read from the table entry, and an External Procedure Call is performed using it. The MOD Register (16 bits) and Program Counter (32 bits) are pushed on the Interrupt Stack.

This process is illustrated in *Figure 3-23*, from the viewpoint of the programmer.

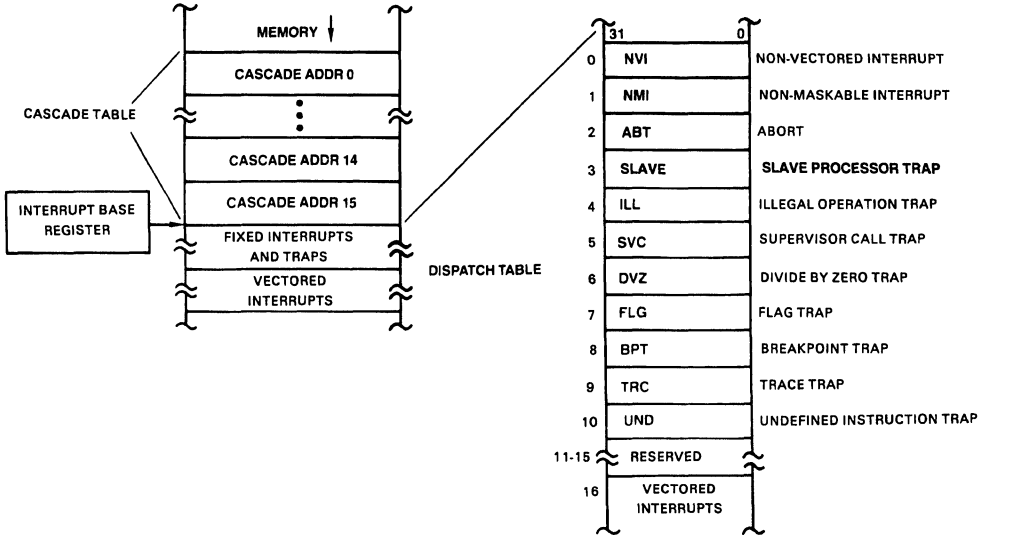


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FIGURE 3-22. Interrupt Dispatch and Cascade Tables

3.0 Functional Description (Continued)

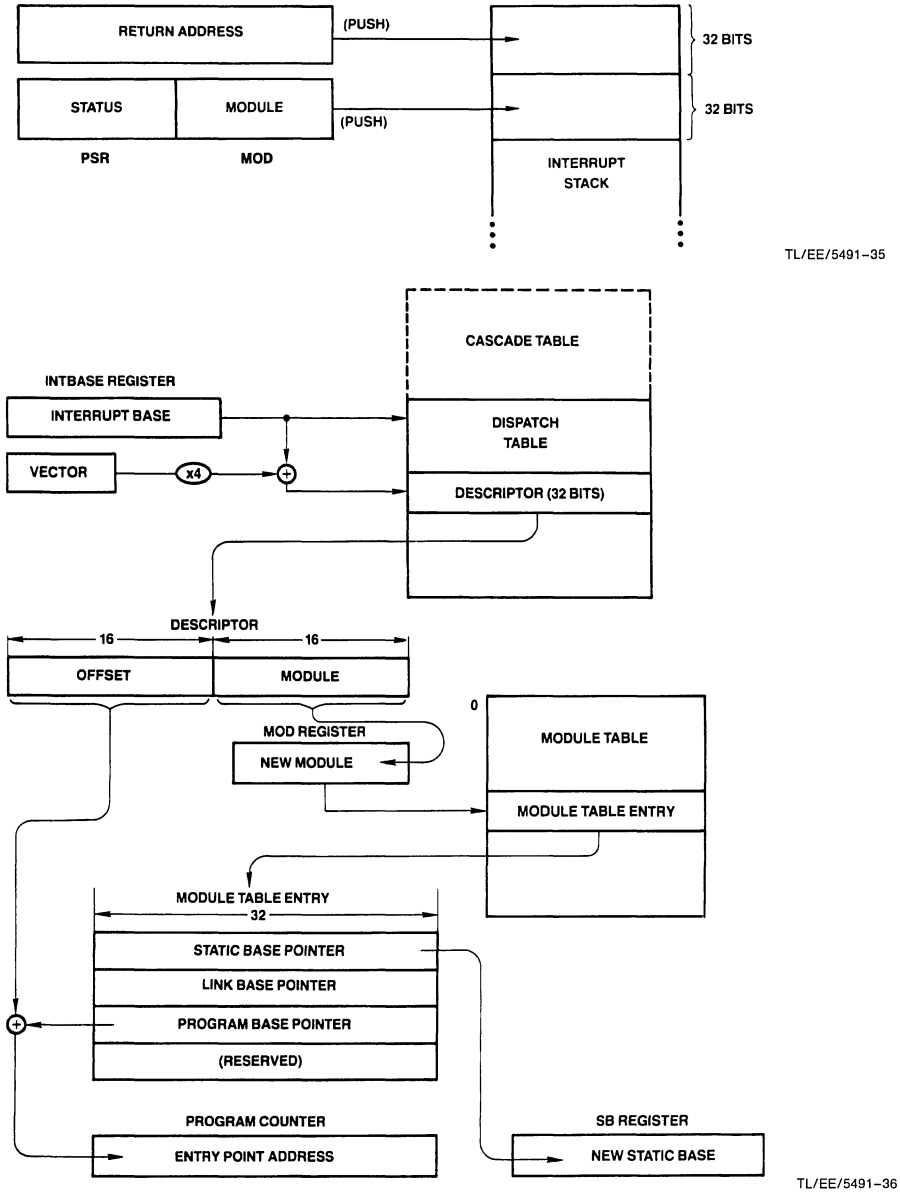

FIGURE 3-23. Interrupt/Trap Service Routine Calling Sequence

3.0 Functional Description (Continued)

3.8.2 Interrupt/Trap Return

To return control to an interrupted program, one of two instructions is used. The RETT (Return from Trap) instruction (*Figure 3-24*) restores the PSR, MOD, PC and SB registers to their previous contents and, since traps are often used deliberately as a call mechanism for Supervisor Mode procedures, it also discards a specified number of bytes from the original stack as surplus parameter space. RETT is used to return from any trap or interrupt except the Maskable Interrupt. For this, the RETI (Return from Interrupt) instruction is used, which also informs any external Interrupt Control Units that interrupt service has completed. Since interrupts are generally asynchronous external events, RETI does not pop parameters. See *Figure 3-25*.

3.8.3 Maskable Interrupts (The $\overline{\text{INT}}$ Pin)

The $\overline{\text{INT}}$ pin is a level-sensitive input. A continuous low level is allowed for generating multiple interrupt requests. The input is maskable, and is therefore enabled to generate interrupt requests only while the Processor Status Register I bit is set. The I bit is automatically cleared during service of an $\overline{\text{INT}}$, $\overline{\text{NMI}}$ or Abort request, and is restored to its original setting upon return from the interrupt service routine via the RETT or RETI instruction.

The $\overline{\text{INT}}$ pin may be configured via the SETCFG instruction as either Non-Vectored (CFG Register bit I = C) or Vectored (bit I = 1).

3.8.3.1 Non-Vectored Mode

In the Non-Vectored mode, an interrupt request on the $\overline{\text{INT}}$ pin will cause an Interrupt Acknowledge bus cycle, but the CPU will ignore any value read from the bus and use instead a default vector of zero. This mode is useful for small systems in which hardware interrupt prioritization is unnecessary.

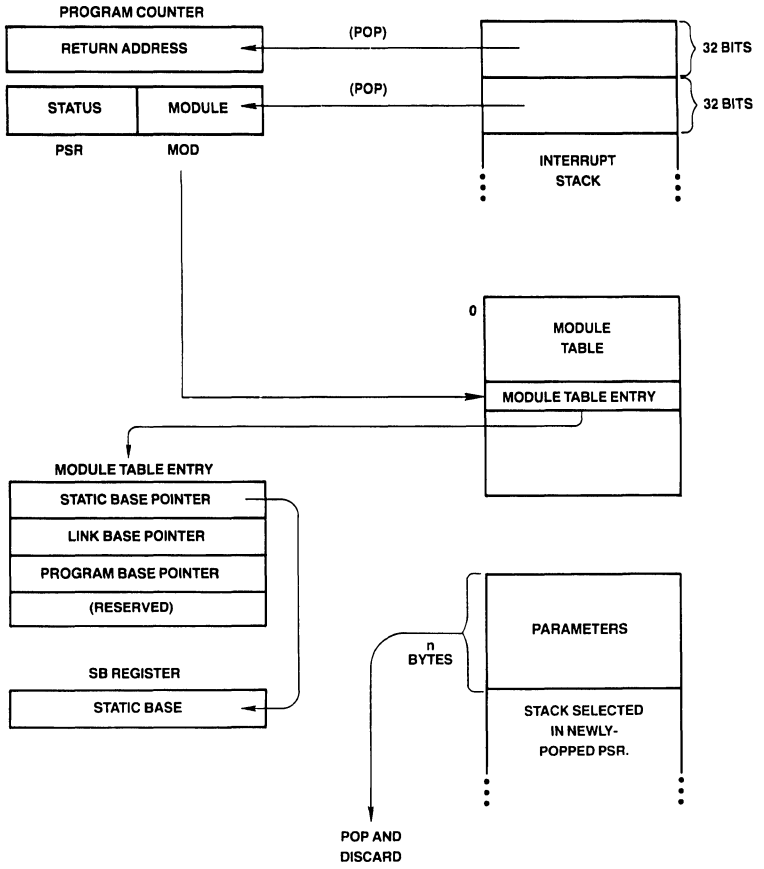

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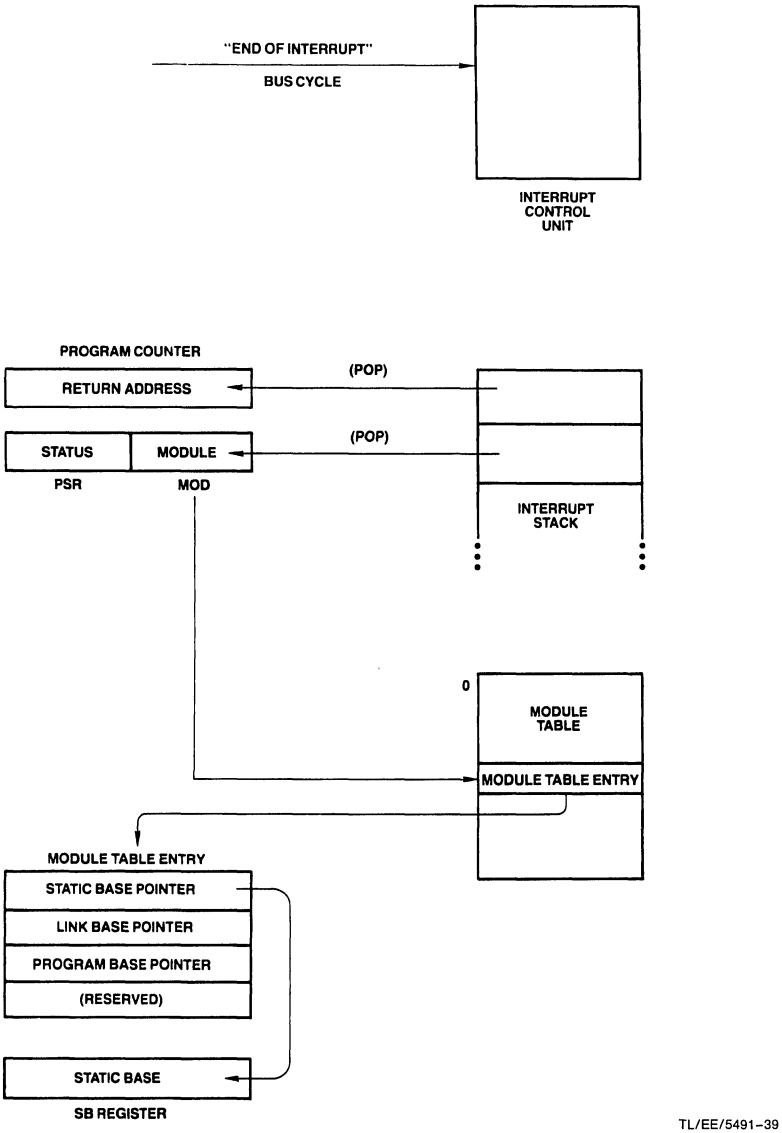
FIGURE 3-24. Return from Trap (RETT n) Instruction Flow

3.0 Functional Description (Continued)



TL/EE/5491–39

FIGURE 3-25. Return from Interrupt (RETI) Instruction Flow

3.0 Functional Description (Continued)

3.8.3.2 Vectored Mode: Non-Cascaded Case

In the Vectored mode, the CPU uses an Interrupt Control Unit (ICU) to prioritize up to 16 interrupt requests. Upon receipt of an interrupt request on the $\overline{INT}$ pin, the CPU performs an "Interrupt Acknowledge, Master" bus cycle (Sec. 3.4.2) reading a vector value from the low-order byte of the Data Bus. This vector is then used as an index into the Dispatch Table in order to find the External Procedure Descriptor for the proper interrupt service procedure. The service procedure eventually returns via the Return from Interrupt (RETI) instruction, which performs an End of Interrupt bus cycle, informing the ICU that it may re-prioritize any interrupt requests still pending. The ICU provides the vector number again, which the CPU uses to determine whether it needs also to inform a Cascaded ICU (see below).

In a system with only one ICU (16 levels of interrupt), the vectors provided must be in the range of 0 through 127; that is, they must be positive numbers in eight bits. By providing a negative vector number, an ICU flags the interrupt source as being a Cascaded ICU (see below).

3.8.3.3 Vectored Mode: Cascaded Case

In order to allow up to 256 levels of interrupt, provision is made both in the CPU and in the NS32202 Interrupt Control Unit (ICU) to transparently support cascading. *Figure 3-27*, shows a typical cascaded configuration. Note that the Interrupt output from a Cascaded ICU goes to an Interrupt Request input of the Master ICU, which is the only ICU which drives the CPU $\overline{INT}$ pin.

In a system which uses cascading, two tasks must be performed upon initialization:

1) For each Cascaded ICU in the system, the Master ICU must be informed of the line number (0 to 15) on which it receives the cascaded requests.

2) A Cascade Table must be established in memory. The Cascade Table is located in a NEGATIVE direction from the location indicated by the CPU Interrupt Base (INTBASE) Register. Its entries are 32-bit addresses, pointing to the Vector Registers of each of up to 16 Cascaded ICUs.

Figure 3-22 illustrates the position of the Cascade Table. To find the Cascade Table entry for a Cascaded ICU, take its Master ICU line number (0 to 15) and subtract 16 from it, giving an index in the range −16 to −1. Multiply this value by 4, and add the resulting negative number to the contents of the INTBASE Register. The 32-bit entry at this address must be set to the address of the Hardware Vector Register of the Cascaded ICU. This is referred to as the "Cascade Address."

Upon receipt of an interrupt request from a Cascaded ICU, the Master ICU interrupts the CPU and provides the negative Cascade Table index instead of a (positive) vector number. The CPU, seeing the negative value, uses it as an index into the Cascade Table and reads the Cascade Address from the referenced entry. Applying this address, the CPU performs an "Interrupt Acknowledge, Cascaded" bus cycle (Sec. 3.4.2), reading the final vector value. This vector is interpreted by the CPU as an unsigned byte, and can therefore be in the range of 0 through 255.

In returning from a Cascaded interrupt, the service procedure executes the Return from Interrupt (RETI) instruction, as it would for any Maskable Interrupt. The CPU performs an "End of Interrupt, Master" bus cycle (Sec. 3.4.2), whereupon the Master ICU again provides the negative Cascade Table index. The CPU, seeing a negative value, uses it to find the corresponding Cascade Address from the Cascade Table. Applying this address, it performs an "End of Interrupt, Cascaded" bus cycle (Sec. 3.4.2), informing the Cascaded ICU of the completion of the service routine. The byte read from the Cascaded ICU is discarded.

Note: If an interrupt must be masked off, the CPU can do so by setting the corresponding bit in the Interrupt Mask Register of the Interrupt Controller.

However, if an interrupt is set pending during the CPU instruction that masks off that interrupt, the CPU may still perform an interrupt acknowledge cycle following that instruction since it might have sampled the $\overline{INT}$ line before the ICU deasserted it. This could cause the ICU to provide an invalid vector. To avoid this problem the above operation should be performed with the CPU interrupt disabled.

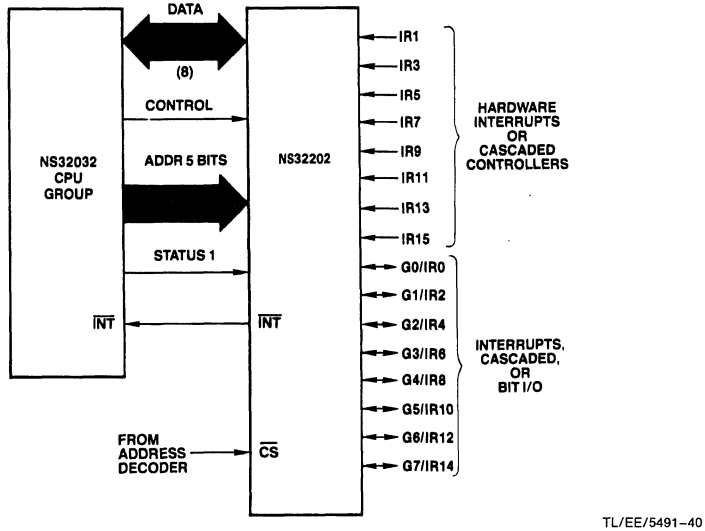


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FIGURE 3-26. Interrupt Control Unit Connections (16 Levels)

3.0 Functional Description (Continued)

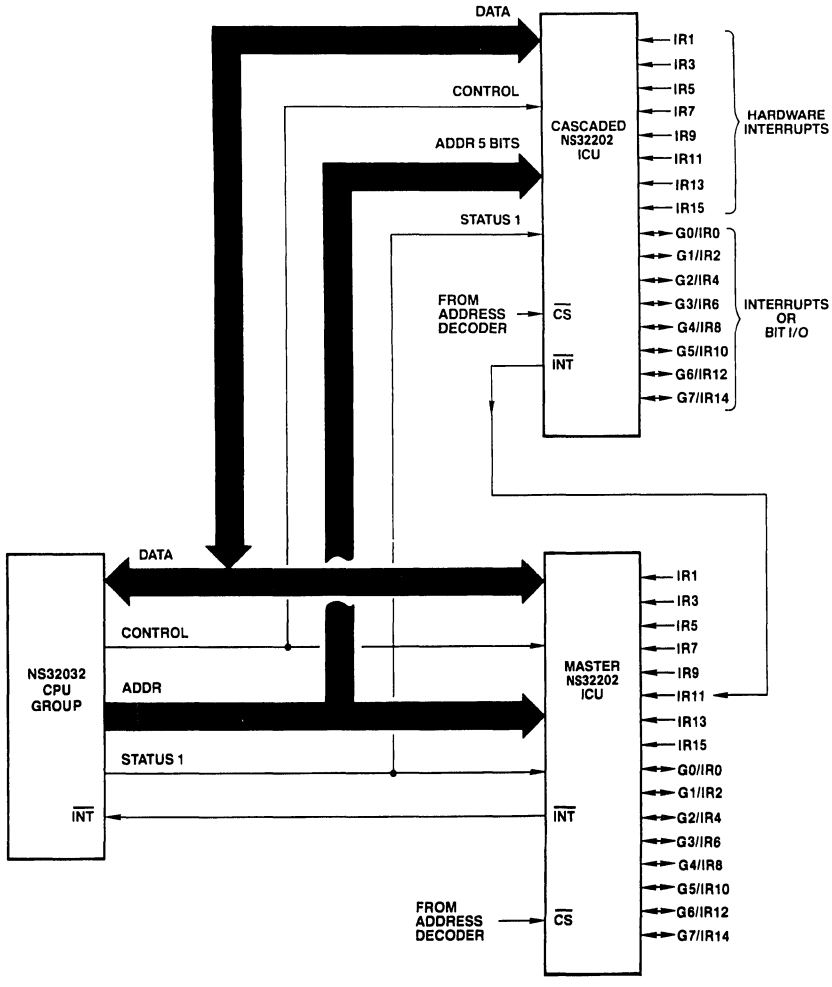

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FIGURE 3-27. Cascaded Interrupt Control Unit Connections

3.8.4 Non-Maskable Interrupt (The $\overline{\text{NMI}}$ Pin)

The Non-Maskable Interrupt is triggered whenever a falling edge is detected on the $\overline{\text{NMI}}$ pin. The CPU performs an "Interrupt Acknowledge, Master" bus cycle (Sec. 3.4.2) when processing of this interrupt actually begins. The Interrupt Acknowledge cycle differs from that provided for Maskable Interrupts in that the address presented is $FFFF00_{16}$. The vector value used for the Non-Maskable Interrupt is taken as 1, regardless of the value read from the bus.

The service procedure returns from the Non-Maskable Interrupt using the Return from Trap (RETT) instruction. No special bus cycles occur on return.

For the full sequence of events in processing the Non-Maskable Interrupt, see Sec. 3.8.7.1.

3.8.5 Traps

A trap is an internally-generated interrupt request caused as a direct and immediate result of the execution of an instruction. The Return Address pushed by any trap except Trap (TRC) is the address of the first byte of the instruction during which the trap occurred. Traps do not disable interrupts, as they are not associated with external events. Traps recognized by the NS32032 CPU are:

Trap (SLAVE): An exceptional condition was detected by the Floating Point Unit or another Slave Processor during the execution of a Slave Instruction. This trap is requested via the Status Word returned as part of the Slave Processor Protocol (Sec. 3.9.1).

3.0 Functional Description (Continued)

Trap (ILL): Illegal operation. A privileged operation was attempted while the CPU was in User Mode (PSR bit U = 1).

Trap (SVC): The Supervisor Call (SVC) instruction was executed.

Trap (DVZ): An attempt was made to divide an integer by zero. (The slave trap is used for Floating Point division by zero.)

Trap (FLG): The FLAG instruction detected a "1" in the CPU PSR F bit.

Trap (BPT): The Breakpoint (BPT) instruction was executed.

Trap (TRC): The instruction just completed is being traced. See below.

Trap (UND): An undefined opcode was encountered by the CPU.

A special case is the Trace Trap (TRC), which is enabled by setting the T bit in the Processor Status Register (PSR). At the beginning of each instruction, the T bit is copied into the PSR P (Trace "Pending") bit. If the P bit is set at the end of an instruction, then the Trace Trap is activated. If any other trap or interrupt request is made during a traced instruction, its entire service procedure is allowed to complete before the Trace Trap occurs. Each interrupt and trap sequence handles the P bit for proper tracing, guaranteeing one and only one Trace Trap per instruction, and guaranteeing that the Return Address pushed during a Trace Trap is always the address of the next instruction to be traced.

3.8.6 Prioritization

The NS32016 CPU internally prioritizes simultaneous interrupt and trap requests as follows:

1) Traps other than Trace (Highest priority)
2) Abort
3) Non-Maskable Interrupt
4) Maskable Interrupts
5) Trace Trap (Lowest priority)

3.8.7 Interrupt/Trap Sequences: Detailed Flow

For purposes of the following detailed discussion of interrupt and trap service sequences, a single sequence called "Service" is defined in *Figure 3-28*. Upon detecting any interrupt request or trap condition, the CPU first performs a sequence dependent upon the type of interrupt or trap. This sequence will include pushing the Processor Status Register and establishing a Vector and a Return Address. The CPU then performs the Service sequence.

For the sequence followed in processing either Maskable or Non-Maskable interrupts (on the $\overline{INT}$ or $\overline{NMI}$ pins, respectively), see Sec. 3.8.7.1 For Abort Interrupts, see Sec. 3.8.7.4. For the Trace Trap, see Sec. 3.8.7.3, and for all other traps see Sec. 3.8.7.2.

3.8.7.1 Maskable/Non-Maskable Interrupt Sequence

This sequence is performed by the CPU when the $\overline{NMI}$ pin receives a falling edge, or the $\overline{INT}$ pin becomes active with the PSR I bit set. The interrupt sequence begins either at the next instruction boundary or, in the case of the String instructions, at the next interruptible point during its execution.

1. If a String instruction was interrupted and not yet completed:
   a. Clear the Processor Status Register P bit.
   b. Set "Return Address" to the address of the first byte of the interrupted instruction.

   Otherwise, set "Return Address" to the address of the next instruction.
2. Copy the Processor Status Register (PSR) into a temporary register, then clear PSR bits S, U, T, P and I.
3. If the interrupt is Non-Maskable:
   a. Read a byte from address $FFFF00_{16}$, applying Status Code 0100 (Interrupt Acknowledge, Master, Sec. 3.4.2). Discard the byte read.
   b. Set "Vector" to 1.
   c. Go to Step 8.
4. If the interrupt is Non-Vectored:
   a. Read a byte from address $FFFF00_{16}$, applying Status Code 0100 (Interrupt Acknowledge, Master: Sec. 3.4.2). Discard the byte read.
   b. Set "Vector" to 0.
   c. Go to Step 8.
5. Here the interrupt is Vectored. Read "Byte" from address $FFFE00_{16}$, applying Status Code 0100 (Interrupt Acknowledge, Master: Sec. 3.4.2).
6. If "Byte" ≥ 0, then set "Vector" to "Byte" and go to Step 8.
7. If "Byte" is in the range −16 through −1, then the interrupt source is Cascaded. (More negative values are reserved for future use.) Perform the following:
   a. Read the 32-bit Cascade Address from memory. The address is calculated as INTBASE +4* Byte.
   b. Read "Vector," applying the Cascade Address just read and Status Code 0101 (Interrupt Acknowledge, Cascaded: Sec. 3.4.2).
8. Push the PSR copy (from Step 2) onto the Interrupt Stack as a 16-bit value.
9. Perform Service (Vector, Return Address), *Figure 3-28*.

Service (Vector, Return Address):

1) Read the 32-bit External Procedure Descriptor from the Interrupt Dispatch Table: address is Vector* 4 + INTBASE Register contents.

2) Move the Module field of the Descriptor into the MOD Register.

3) Read the new Static Base pointer from the memory address contained in MOD, placing it into the SB Register.

4) Read the Program Base pointer from memory address MOD + 8, and add to it the Offset field from the Descriptor, placing the result in the Program Counter.

5) Flush queue: Non-sequentially fetch first instruction of Interrupt routine.

6) Push MOD Register into the Interrupt Stack as a 16-bit value. (The PSR has already been pushed as a 16-bit value.)

7) Push the Return Address onto the Interrupt Stack as a 32-bit quantity.

FIGURE 3-28. Service Sequence

Invoked during all interrupt/trap sequences.

3.0 Functional Description (Continued)

3.8.7.2 Trap Sequence: Traps Other Than Trace

1) Restore the currently selected Stack Pointer and the Processor Status Register to their original values at the start of the trapped instruction.
2) Set "Vector" to the value corresponding to the trap type.
   SLAVE: Vector = 3.
   ILL: Vector = 4.
   SVC: Vector = 5.
   DVZ: Vector = 6.
   FLG: Vector = 7.
   BPT: Vector = 8.
   UND: Vector = 10.
3) Copy the Processor Status Register (PSR) into a temporary register, then clear PSR bits S, U, P and T.
4) Push the PSR copy onto the Interrupt Stack as a 16-bit value.
5) Set "Return Address" to the address of the first byte of the trapped instruction.
6) Perform Service (Vector, Return Address), *Figure 3-28.*

3.8.7.3 Trace Trap Sequence

1) In the Processor Status Register (PSR), clear the P bit.
2) Copy the PSR into a temporary register, then clear PSR bits S, U and T.
3) Push the PSR copy onto the Interrupt Stack as a 16-bit value.
4) Set "Vector" to 9.
5) Set "Return Address" to the address of the next instruction.
6) Perform Service (Vector, Return Address), *Figure 3-28.*

3.8.7.4 Abort Sequence

1) Restore the currently selected Stack Pointer to its original contents at the beginning of the aborted instruction.
2) Clear the PSR P bit.
3) Copy the PSR into a temporary register, then clear PSR bits S, U, T and I.
4) Push the PSR copy onto the Interrupt Stack as a 16-bit value.
5) Set "Vector" to 2.
6) Set "Return Address" to the address of the first byte of the aborted instruction.
7) Perform Service (Vector, Return Address), *Figure 3-28.*

3.9 SLAVE PROCESSOR INSTRUCTIONS

The NS32032 CPU recognizes three groups of instructions being executable by external Slave Processor:

Floating Point Instruction Set
Memory Management Instruction Set
Custom Instruction Set

Each Slave Instruction Set is validated by a bit in the Configuration Register (Sec. 2.1.3). Any Slave Instruction which does not have its corresponding Configuration Register bit set will trap as undefined, without any Slave Processor communication attempted by the CPU. This allows software simulation of a non-existent Slave Processor.

3.9.1 Slave Processor Protocol

Slave Processor instructions have a three-byte Basic Instruction field, consisting of an ID Byte followed by an Operation Word. The ID Byte has three functions:

1) It identifies the instruction as being a Slave Processor instruction.
2) It specifies which Slave Processor will execute it.
3) It determines the format of the following Operation Word of the instruction.

Upon receiving a Slave Processor instruction, the CPU initiates the sequence outlined in *Figure 3-29.* While applying Status Code 1111 (Broadcast ID, Sec. 3.4.2), the CPU transfers the ID Byte on the least-significant byte of the Data Bus (AD0–AD7). All Slave Processors input this byte and decode it. The Slave Processor selected by the ID Byte is activated, and from this point the CPU is communicating only with it. If any other slave protocol was in progress (e.g., an aborted Slave instruction), this transfer cancels it.

The CPU next sends the Operation Word while applying Status Code 1101 (Transfer Slave Operand, Sec. 3.4.2). Upon receiving it, the Slave Processor decodes it, and at this point both the CPU and the Slave Processor are aware of the number of operands to be transferred and their sizes. The operation Word is swapped on the Data Bus, that is, bits 0–7 appear on pins AD8–AD15 and bits 8–15 appear on pins AD0–AD7.

Using the Address Mode fields within the Operation Word, the CPU starts fetching operand and issuing them to the Slave Processor. To do so, it references any Addressing Mode extensions which may be appended to the Slave Processor instruction. Since the CPU is solely responsible

Status Combinations:

Send ID (ID): Code 1111
Xfer Operand (OP): Code 1101
Read Status (ST): Code 1110

Step	Status	Action
1	ID	CPU Send ID Byte.
2	OP	CPU Sends Operaton Word.
3	OP	CPY Sends Required Operands
4	—	Slave Starts Execution. CPU Pre-fetches.
5	—	Slave Pulses $\overline{SPC}$ Low.
6	ST	CPU Reads Status Word. (Trap? Alter Flags?)
7	OP	CPU Reads Results (If Any).

FIGURE 3-29. Slave Processor Protocol

3.0 Functional Description (Continued)

for memory accesses, these extensions are not sent to the Slave processor. The Status Code applied is 1101 (Transfer Slave Processor Operand, Sec. 3.4.2).

After the CPU has issued the last operand, the Slave Processor starts the actual execution of the instruction. Upon completion, it will signal the CPU by pulsing $\overline{SPC}$ low. To allow for this, and for the Address Translation strap function, $\overline{AT}/\overline{SPC}$ is normally held high only by an internal pull-up device of approximately 5 kΩ.

While the Slave Processor is executing the instruction, the CPU is free to prefetch instructions into its queue. If it fills the queue before the Slave Processor finishes, the CPU will wait, applying Status Code 0011 (Waiting for Slave, Sec. 3.4.2).

Upon receiving the pulse on $\overline{SPC}$, the CPU uses $\overline{SPC}$ to read a Status Word from the Slave Processor, applying Status Code 1110 (Read Slave Status, Sec. 3.4.2). This word has the format shown in *Figure 3-30*. If the Q bit ("Quit", Bit 0) is set, this indicates that an error was detected by the Slave Processor. The CPU will not continue the protocol, but will immediately trap through the Slave vector in the Interrupt Table. Certain Slave Processor instructions cause CPU PSR bits to be loaded from the Status Word.

The last step in the protocol is for the CPU to read a result, if any, and transfer it to the destination. The Read cycles from the Slave Processor are performed by the CPU while applying Status Code 1101 (Transfer Slave Operand, Sec. 3.4.2).

An exception to the protocol above is the LMR (Load Memory Management Register) instruction, and a corresponding Custom Slave instruction (LCR: Load Custom Register). In executing these instructions, the protocol ends after the CPU has issued the last operand. The CPU does not wait for an acknowledgement from the Slave Processor, and it does not read status.

3.9.2 Floating Point Instructions

Table 3-4 gives the protocols followed for each Floating Point instruction. The instructions are referenced by their mnemonics. For the bit encodings of each instruction, see Appendix A.

The Operand class columns give the Access Class for each general operand, defining how the addressing modes are interpreted (see Instruction Set Reference Manual).

The Operand Issued columns show the sizes of the operands issued to the Floating Point Unit by the CPU. "D" indicates a 32-bit Double Word. "i" indicates that the instruction specifies an integer size for the operand (B = Byte, W = Word, D = Double Word). "f" indicates that the instruction specifies a Floating Point size for the operand (F = 32-bit Standard Floating, L = 64-bit Long Floating).

The Returned Value Type and Destination column gives the size of any returned value and where the CPU places it. The PSR Bits Affected column indicates which PSR bits, if any, are updated from the Slave Processor Status Word (*Figure 3-30*).

TABLE 3-4
Floating Point Instruction Protocols.

Mnemonic	Operand 1 Class	Operand 2 Class	Operand 1 Issued	Operand 2 Issued	Returned Value Type and Dest.	PSR Bits Affected
ADDf	read.f	rmw.f	f	f	f to Op. 2	none
SUBf	read.f	rmw.f	f	f	f to Op. 2	none
MULf	read.f	rmw.f	f	f	f to Op. 2	none
DIVf	read.f	rmw.f	f	f	f to Op. 2	none
MOVf	read.f	write.f	f	N/A	f to Op. 2	none
ABSf	read.f	write.f	f	N/A	f to Op. 2	none
NEGf	read.f	write.f	f	N/A	f to Op. 2	none
CMPf	read.f	read.f	f	f	N/A	N,Z,L
FLOORfi	read.f	write.i	f	N/A	i to Op. 2	none
TRUNCfi	read.f	write.i	f	N/A	i to Op. 2	none
ROUNDfi	read.f	write.i	f	N/A	i to Op. 2	none
MOVFL	read.F	write.L	F	N/A	L to Op. 2	none
MOVLF	read.L	write.F	L	N/A	F to Op. 2	none
MOVif	read.i	write.f	i	N/A	f to Op. 2	none
LFSR	read.D	N/A	D	N/A	N/A	none
SFSR	N/A	write.D	N/A	N/A	D to Op. 2	none

Note:

D = Double Word

i = Integer size (B,W,D) specified in mnemonic.

f = Floating Point type (F,L) specified in mnemonic.

N/A = Not Applicable to this instruction.

3.0 Functional Description (Continued)

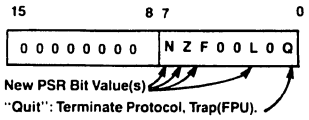

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FIGURE 3-30. Slave Processor Status Word Format

Any operand indicated as being of type "f" will not cause a transfer if the Register addressing mode is specified. This is because the Floating Point Registers are physically on the Floating Point Unit and are therefore available without CPU assistance.

3.9.3 Memory Management Instructions

Table 3-5 gives the protocols for Memory Management instructions. Encodings for these instructions may be found in Appendix A.

In executing the RDVAL and WRVAL instructions, the CPU calculates and issues the 32-bit Effective Address of the single operand. The CPU then performs a single-byte Read cycle from that address, allowing the MMU to safely abort the instruction if the necessary information is not currently in physical memory. Upon seeing the memory cycle complete, the MMU continues the protocol, and returns the validation result in the F bit of the Slave Status Word.

The size of a Memory Management operand is always a 32-bit Double Word. For further details of the Memory Management Instruction set, see the Instruction Set Reference Manual and the NS32082 MMU Data Sheet.

TABLE 3-5

Memory Management Instruction Protocols.

Mnemonic	Operand 1 Class	Operand 2 Class	Operand 1 Issued	Operand 2 Issued	Returned Value Type and Dest.	PSR Bits Affected
RDVAL*	addr	N/A	D	N/A	N/A	F
WRVAL*	addr	N/A	D	N/A	N/A	F
LMR*	read.D	N/A	D	N/A	N/A	none
SMR*	write.D	N/A	N/A	N/A	D to Op. 1	none

Note:

In the RDVAL and WRVAL instructions, the CPU issues the address as a Double Word, and performs a single-byte Read cycle from that memory address. For details, see the Instruction Set Reference Manual and the NS32082 Memory Management Unit Data Sheet.

D = Double Word

* = Privileged Instruction: will trap if CPU is in User Mode.

N/A = Not Applicable to this instruction.

3.0 Functional Description (Continued)

3.9.4 Custom Slave Instructions

Provided in the NS32032 is the capability of communicating with a user-defined, "Custom" Slave Processor. The instruction set provided for a Custom Slave Processor defines the instruction formats, the operand classes and the communication protocol. Left to the user are the interpretations of the Op Code fields, the programming model of the Custom Slave and the actual types of data transferred. The protocol specifies only the size of an operand, not its data type.

Table 3-6 lists the relevant information for the Custom Slave instruction set. The designation "c" is used to represent an operand which can be a 32-bit ("D") or 64-bit ("Q") quantity in any format; the size is determined by the suffix on the mnemonic. Similarly, an "i" indicates an integer size (Byte, Word, Double Word) selected by the corresponding mnemonic suffix.

Any operand indicated as being of type "c" will not cause a transfer if the register addressing mode is specified. It is assumed in this case that the slave processor is already holding the operand internally.

For the instruction encodings, see Appendix A.

TABLE 3-6
Custom Slave Instruction Protocols.

Mnemonic	Operand 1 Class	Operand 2 Class	Operand 1 Issued	Operand 2 Issued	Returned Value Type and Dest.	PSR Bits Affected
CCAL0c	read.c	rmw.c	c	c	c to Op. 2	none
CCAL1c	read.c	rmw.c	c	c	c to Op. 2	none
CCAL2c	read.c	rmw.c	c	c	c to Op. 2	none
CCAL3c	read.c	rmw.c	c	c	c to Op. 2	none
CMOV0c	read.c	write.c	c	N/A	c to Op. 2	none
CMOV1c	read.c	write.c	c	N/A	c to Op. 2	none
CMOV2c	read.c	write.c	c	N/A	c to Op. 2	none
CMOV3c	read.c	write.c	c	N/A	c to Op. 2	none
CCMP0c	read.c	read.c	c	c	N/A	N,Z,L
CCMP1c	read.c	read.c	c	c	N/A	N,Z,L
CCV0ci	read.c	write.i	c	N/A	i to Op. 2	none
CCV1ci	read.c	write.i	c	N/A	i to Op. 2	none
CCV2ci	read.c	write.i	c	N/A	i to Op. 2	none
CCV3ic	read.i	write.c	i	N/A	c to Op. 2	none
CCV4DQ	read.D	write.Q	D	N/A	Q to Op. 2	none
CCV5QD	read.Q	write.D	Q	N/A	D to Op. 2	none
LCSR	read.D	N/A	D	N/A	N/A	none
SCSR	N/A	write.D	N/A	N/A	D to OP. 2	none
CATST0*	addr	N/A	D	N/A	N/A	F
CATST1*	addr	N/A	D	N/A	N/A	F
LCR*	read.D	N/A	D	N/A	N/A	none
SCR*	write.D	N/A	N/A	N/A	D to Op.1	none

Note:

D = Double Word

i = Integer size (B,W,D) specified in mnemonic.

c = Custom size (D:32 bits or Q:64 bits) specified in mnemonic.

* = Privileged instruction: will trap if CPU is in User Mode.

N/A = Not Applicable to this instruction.

4.0 Device Specifications

4.1 NS32032 PIN DESCRIPTIONS

The following is a brief description of all NS32032 pins. The descriptions reference portions of the Functional Description. Sec. 3.

Unless otherwise indicated reserved pins should be left open.

4.1.1 Supplies

Power (V_{CC}): +5V Positive Supply. Sec. 3.1.

Logic Ground (GNDL): Ground reference for on-chip logic. Sec. 3.1.

Buffer Grounds #1 (GNDB1, GNDB2, GNDB3): Ground references for the on-chip output drivers connected to output pins. Sec. 3.1.

Back-Bias Generator (BBG): Output of on-chip substrate voltage generator. Sec. 3.1.

4.1.2 Input Signals

Clocks (PHI1, PHI2): Two-phase clocking signals. Sec. 3.2.

Ready (RDY): Active high. While RDY is inactive, the CPU extends the current bus cycle to provide for a slower memory or peripheral reference. Upon detecting RDY active, the CPU terminates the bus cycle. Sec. 3.4.1.

Hold Request ($\overline{\text{HOLD}}$): Active low. Causes the CPU to release the bus for DMA or multiprocessing purposes. Sec. 3.6.

Note 1: $\overline{\text{HOLD}}$ must not be asserted until $\overline{\text{HLDA}}$ from a previous $\overline{\text{HOLD}}$/$\overline{\text{HLDA}}$ sequence is deasserted.

Note 2: If the $\overline{\text{HOLD}}$ signal is generated asynchronously, it's set up and hold times may be violated.

In this case it is recommended to synchronize it with CTTL to minimize the possibility of metastable states.

The CPU provides only one synchronization stage to minimize the $\overline{\text{HLDA}}$ latency. This is to avoid speed degradations in cases of heavy $\overline{\text{HOLD}}$ activity (i.e., DMA controller cycles interleaved with CPU cycles.)

Interrupt ($\overline{\text{INT}}$): Active low. Maskable Interrupt request. Sec. 3.8.

Non-Maskable Interrupt ($\overline{\text{NMI}}$): Active low. Non-Maskable Interrupt request. Sec. 3.8.

Reset/Abort ($\overline{\text{RST}}$/$\overline{\text{ABT}}$): Active low. If held active for one clock cycle and released, this pin causes an Abort Command, Sec. 3.5.4. If held longer, it initiates a Reset. Sec. 3.3.

4.1.3 Output Signals

Address Strobe ($\overline{\text{ADS}}$): Active low. Controls address latches: indicates start of a bus cycle. Sec. 3.4.

Data Direction in ($\overline{\text{DDIN}}$): Active low. Status signal indicating direction of data transfer during a bus cycle. Sec. 3.4.

Byte Enable ($\overline{\text{BE0}}$–$\overline{\text{BE3}}$): Active low. Four control signals enabling data transfers on individual bus bytes. Sec. 3.4.3.

Status (ST0–ST3): Bus cycle status code, ST0 least significant. Sec. 3.4.2. Encodings are:

0000 — Idle: CPU Inactive on Bus.
0001 — Idle: WAIT Instruction.
0010 — (Reserved).
0011 — Idle: Waiting for Slave.
0100 — Interrupt Acknowledge, Master.
0101 — Interrupt Acknowledge, Cascaded.
0110 — End of Interrupt, Master.
0111 — End of Interrupt, Cascaded.
1000 — Sequential Instruction Fetch.
1001 — Non-Sequential Instruction Fetch.
1010 — Data Transfer.
1011 — Read Read-Modify-Write Operand.
1100 — Read for Effective Address.
1101 — Transfer Slave Operand.
1110 — Read Slave Status Word.
1111 — Broadcast Slave ID.

Hold Acknowledge ($\overline{\text{HLDA}}$): Active low. Applied by the CPU in response to $\overline{\text{HOLD}}$ input, indicating that the bus has been released for DMA or multiprocessing purposes. Sec. 3.6.

User/Supervisor (U/$\overline{\text{S}}$): User or Supervisor Mode status. Sec. 3.7. High state indicates User Mode, low indicates Supervisor Mode. Sec. 3.7.

Interlocked Operation ($\overline{\text{ILO}}$): Active low. Indicates that an interlocked instruction is being executed. Sec. 3.7.

Program Flow Status ($\overline{\text{PFS}}$): Active low. Pulse indicates beginning of an instruction execution. Sec. 3.7.

4.1.4 Input-Output Signals

Address/Data 0–23 (AD0–AD23): Multiplexed Address/Data information. Bit 0 is the least significant bit of each. Sec. 3.4.

Data Bits 24–31 (D24–D31): The high order 8 bits of the data bus.

Address Translation/Slave Processor Control ($\overline{\text{AT}}$/$\overline{\text{SPC}}$): Active low. Used by the CPU as the data strobe output for Slave Processor transfers; used by Slave Processors to acknowledge completion of a slave instruction. Sec. 3.4.6; Sec. 3.9. Sampled on the rising edge of Reset pulse as Address Translation Strap. Sec. 3.5.1.

In non-memory-managed systems, this pin should be pulled-up to V_{CC} through a 10 kΩ resistor.

Data Strobe/Float ($\overline{\text{DS}}$/$\overline{\text{FLT}}$): Active low. Data Strobe output, Sec. 3.4, or Float Command input, Sec. 3.5.3. Pin function is selected on $\overline{\text{AT}}$/$\overline{\text{SPC}}$ pin, Sec. 3.5.1.

4.0 Device Specifications (Continued)

4.2 ABSOLUTE MAXIMUM RATINGS

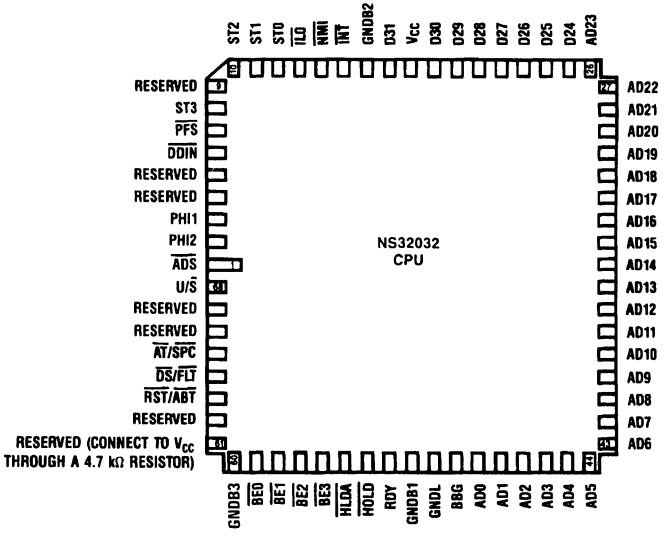
If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Temperature Under Bias	0°C to +70°C
Storage Temperature	−65°C to +150°C
All Input or Output Voltages With Respect to GND	−0.5V to +7V
Power Dissipation	1.5 Watt

Note: *Absolute maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended; operation should be limited to those conditions specified under Electrical Characteristics.*

4.3 ELECTRICAL CHARACTERISTICS $T_A = 0°$ to +70°C, $V_{CC} = 5V \pm 5\%$, GND = 0V

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High Level Input Voltage		2.0		$V_{CC}+0.5$	V
V_{IL}	Low Level Input Voltage		−0.5		0.8	V
V_{CH}	High Level Clock Voltage	PHI1, PHI2 pins only	$V_{CC}-0.35$		$V_{CC}+0.5$	V
V_{CL}	Low Level Clock Voltage	PHI1, PHI2 pins only	−0.5		0.3	V
V_{CLT}	Low Level Clock Voltage. Transient (ringing tolerance)	PHI1, PHI2 pins only	−0.5		0.6	V
V_{OH}	High Level Output Voltage	$I_{OH} = -400\ \mu A$	2.4			V
V_{OL}	Low Level Output Voltage	$I_{OL} = 2$ mA			0.45	V
I_{ILS}	$\overline{AT}/\overline{SPC}$ Input Current (low)	$V_{IN} = 0.4V$, $\overline{AT}/\overline{SPC}$ in input mode	0.05		1.0	mA
I_I	Input Load Current	$0 \le V_{IN} \le V_{CC}$, All inputs except PHI1, PHI2, $\overline{AT}/\overline{SPC}$	−20		20	μA
I_L	Leakage Current Output and I/O Pins in TRI-STATE/Input Mode	$0.4 \le V_{IN} \le V_{CC}$	−20		30	μA
I_{CC}	Active Supply Current	$I_{OUT} = 0$, $T_A = 25°C$		180	300	mA



TL/EE/5491–2

Bottom View

FIGURE 4-1. NS32032 Connection Diagram

Order Number NS32032E-10 or NS32032V-10
See NS Package E68B or V68A

4.0 Device Specifications (Continued)

4.4 SWITCHING CHARACTERISTICS

4.4.1 Definitions

All the timing specifications given in this section refer to 2.0V on the rising or falling edges of the clock phases PHI1 and PHI2 and 0.8V or 2.0V on all other signals as illustrated in *Figures 4-2* and *4-3*, unless specifically stated otherwise.

ABBREVIATIONS:

L.E. — leading edge R.E. — rising edge
T.E. — trailing edge F.E. — falling edge

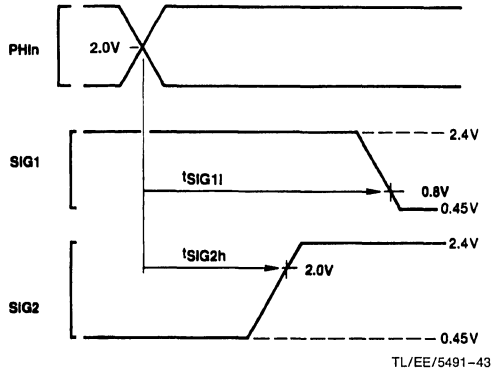


FIGURE 4-2. Timing Specification Standard (Signal Valid After Clock Edge)

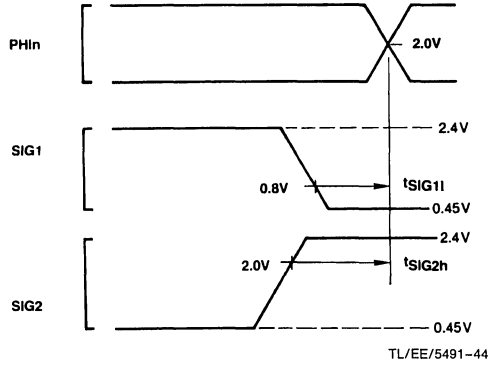


FIGURE 4-3. Timing Specification Standard (Signal Valid Before Clock Edge)

4.4.2 Timing Tables

4.4.2.1 Output Signals: Internal Propagation Delays, NS32032-10

Maximum times assume capacitive loading of 100 pF.

Name	Figure	Description	Reference/Conditions	NS32032-10		Units
				Min	Max	
t_{ALv}	4-4	Address bits 0–23 valid	after R.E., PHI1 T1		40	ns
t_{ALh}	4-4	Address bits 0–23 hold	after R.E., PHI1 Tmmu or T2	5		ns
t_{Dv}	4-4	Data valid (write cycle)	after R.E., PHI1 T2		50	ns
t_{Dh}	4-4	Data hold (write cycle)	after R.E., PHI1 next T1 or Ti	0		ns
t_{ALADSs}	4-5	Address bits 0–23 setup	before $\overline{ADS}$ T.E.	25		ns
t_{ALADSh}	4-10	Address bits 0–23 hold	after $\overline{ADS}$ T.E.	15		ns
t_{ALf}	4-5	Address bits 0–23 floating (no MMU)	after R.E., PHI1 T2		25	ns
t_{ADf}	4-5	Data bits D24–D31 floating (no MMU)	after R.E., PHI1 T2		25	ns
t_{ALMf}	4-9	Address bits 0–23 floating (with MMU)	after R.E., PHI1 Tmmu		25	ns
t_{ADMf}	4-9	Data bits 21–31 floating (with MMU)	after R.E., PHI1 Tmmu		25	ns
t_{BEv}	4-4	$\overline{BEn}$ signals valid	after R.E., PHI2 T4		60	ns
t_{BEh}	4-4	$\overline{BEn}$ signals hold	after R.E., PHI2 T4 or Ti	0		ns
t_{STv}	4-4	Status (ST0–ST3) valid	after R.E., PHI1 T4 (before T1, see note)		60	ns
t_{STh}	4-4	Status (ST0–ST3) hold	after R.E., PHI1 T4 (after T1)	0		ns

4.0 Device Specifications (Continued)

4.4.2.1 Output Signals: Internal Propagation Delays, NS32032-10 (Continued)

Name	Figure	Description	Reference/ Conditions	NS32032-10		Units
				Min	Max	
t_{DDINv}	4-5	$\overline{DDIN}$ signal valid	after R.E., PHI1 T1		50	ns
t_{DDINh}	4-5	$\overline{DDIN}$ signal hold	after R.E., PHI1 next T1 or Ti	0		ns
t_{ADSa}	4-4	$\overline{ADS}$ signal active (low)	after R.E., PHI1 T1		35	ns
t_{ADSia}	4-4	$\overline{ADS}$ signal inactive	after R.E., PHI2 T1		40	ns
t_{ADSw}	4-4	$\overline{ADS}$ pulse width	at 0.8V (both edges)	30		ns
t_{DSa}	4-4	$\overline{DS}$ signal active (low)	after R.E., PHI1 T2		40	ns
t_{DSia}	4-4	$\overline{DS}$ signal inactive	after R.E., PHI1 T4		40	ns
t_{ALf}	4-6	AD0–AD23 floating (caused by $\overline{HOLD}$)	after R.E., PHI1 T1		25	ns
t_{ADf}	4-6	D24–D31 floating (caused by $\overline{HOLD}$)	after R.E., PHI1 T1		25	ns
t_{DSf}	4-6	$\overline{DS}$ floating (caused by $\overline{HOLD}$)	after R.E., PHI1 Ti		50	ns
t_{ADSf}	4-6	$\overline{ADS}$ floating (caused by $\overline{HOLD}$)	after R.E., PHI1 Ti		50	ns
t_{BEf}	4-6	$\overline{BEn}$ floating (caused by $\overline{HOLD}$)	after R.E., PHI1 Ti		50	ns
t_{DDINf}	4-6	$\overline{DDIN}$ floating (caused by $\overline{HOLD}$)	after R.E., PHI1 Ti		50	ns
t_{HLDAa}	4-6	$\overline{HLDA}$ signal active (low)	after R.E., PHI1 Ti		30	ns
t_{HLDAia}	4-8	$\overline{HLDA}$ signal inactive	after R.E., PHI1 Ti		40	ns
t_{DSr}	4-8	$\overline{DS}$ signal returns from floating (caused by $\overline{HOLD}$)	after R.E., PHI1 Ti		50	ns
t_{ADSr}	4-8	$\overline{ADS}$ signal returns from floating (caused by $\overline{HOLD}$)	after R.E., PHI1 Ti		55	ns
t_{BEr}	4-8	$\overline{BEn}$ signals return from floating (caused by $\overline{HOLD}$)	after R.E., PHI1 Ti		55	ns
t_{DDINr}	4-8	$\overline{DDIN}$ signal returns from floating (caused by $\overline{HOLD}$)	after R.E., PHI1 Ti		55	ns
t_{DDINf}	4-9	$\overline{DDIN}$ signal floating (caused by $\overline{FLT}$)	after $\overline{FLT}$ F.E.		55	ns
t_{DDINr}	4-10	$\overline{DDIN}$ signal returns from floating (caused by $\overline{FLT}$)	after $\overline{FLT}$ R.E.		40	ns
t_{SPCa}	4-13	$\overline{SPC}$ output active (low)	after R.E., PHI1 T1		35	ns
t_{SPCia}	4-13	$\overline{SPC}$ output inactive	after R.E., PHI1 T4		35	ns
t_{SPCnf}	4-15	$\overline{SPC}$ output nonforcing	after R.E., PHI2 T4		30	ns
t_{Dv}	4-13	Data valid (slave processor write)	after R.E., PHI1 T1		55	ns
t_{Dh}	4-13	Data hold (slave processor write)	after R.E., PHI1 next T1 or Ti	0		ns
t_{PFSw}	4-18	$\overline{PFS}$ pulse width	at 0.8V (both edges)	50		ns

4.0 Device Specifications (Continued)

4.4.2.1 Output Signals: Internal Propagation Delays, NS32032-10 (Continued)

Name	Figure	Description	Reference/ Conditions	NS32032-10		Units
				Min	Max	
t_{PFSa}	4-18	$\overline{PFS}$ pulse active (low)	after R.E., PHI2		40	ns
t_{PFSia}	4-18	$\overline{PFS}$ pulse inactive	after R.E., PHI2		40	ns
t_{ILOs}	4-20a	$\overline{ILO}$ signal setup	before R.E., PHI1 T1 of first interlocked read cycle	50		ns
t_{ILOh}	4-20b	$\overline{ILO}$ signal hold	after R.E., PHI1 T3 of last interlocked write cycle	10		ns
t_{ILOa}	4-21	$\overline{ILO}$ signal active (low)	after R.E., PHI1		35	ns
t_{ILOia}	4-21	$\overline{ILO}$ signal inactive	after R.E., PHI1		35	ns
t_{USv}	4-22	U/$\overline{S}$ signal valid	after R.E., PHI1 T4		35	ns
t_{USh}	4-22	U/$\overline{S}$ signal hold	after R.E., PHI1 T4	8		ns
t_{NSPF}	4-19b	Nonsequential fetch to next $\overline{PFS}$ clock cycle	after R.E., PHI1 T1	4		t_{Cp}
t_{PFNS}	4-19a	$\overline{PFS}$ clock cycle to next non-sequential fetch	before R.E., PHI1 T1	4		t_{Cp}
t_{LXPF}	4-29	Last operand transfer of an instruction to next $\overline{PFS}$ clock cycle	before R.E., PHI1 T1 of first of first bus cycle of transfer	0		t_{Cp}

Note: Every memory cycle starts with T4, during which Cycle Status is applied. If the CPU was idling, the sequence will be: ". . . Ti, T4, T1 . . .". If the CPU was not idling, the sequence will be: ". . . T4, T1 . . .".

4.4.2.2 Input Signal Requirements: NS32032-10

Name	Figure	Description	Reference/Conditions	NS32032-10		Units
				Min	Max	
t_{PWR}	4-25	Power stable to $\overline{RST}$ R.E.	after V_{CC} reaches 4.5V	50		μs
t_{DIs}	4-5	Data in setup (read cycle)	before F.E., PHI2 T3	15		ns
t_{DIh}	4-5	Data in hold (read cycle)	after R.E., PHI1 T4	3		ns
t_{HLDa}	4-6	$\overline{HOLD}$ active (low) setup time (see note)	before F.E., PHI2 TX1	25		ns
t_{HLDia}	4-8	$\overline{HOLD}$ inactive setup time	before F.E., PHI2 Ti	25		ns
t_{HLDh}	4-6	$\overline{HOLD}$ hold time	after R.E., PHI1 TX2	0		ns
t_{FLTa}	4-9	$\overline{FLT}$ active (low) setup time	before F.E., PHI2 Tmmu	25		ns
t_{FLTia}	4-10	$\overline{FLT}$ inactive setup time	before F.E., PHI2 T2	25		ns
t_{RDYs}	4-11, 4-12	RDY setup time	before F.E., PHI2 T2 or T3	15		ns
t_{RDYh}	4-11, 4-12	RDY hold time	after F.E., PHI1 T3	5		ns
t_{ABTs}	4-23	$\overline{ABT}$ setup time ($\overline{FLT}$ inactive)	before F.E., PHI2 Tmmu	20		ns
t_{ABTs}	4-24	$\overline{ABT}$ setup time ($\overline{FLT}$ active)	before F.E., PHI2 T_f	20		ns
t_{ABTh}	4-23	$\overline{ABT}$ hold time	after R.E., PHI1	0		ns

4.0 Device Specifications (Continued)

4.4.2.2 Input Signal Requirements: NS32032-10 (Continued)

Name	Figure	Description	Reference/ Conditions	NS32032-10		Units
				Min	Max	
t_{RSTs}	4-25, 4-26	$\overline{RST}$ setup time	before F.E., PHI1	15		ns
t_{RSTw}	4-26	$\overline{RST}$ pulse width	at 0.8V (both edges)	64		t_{Cp}
t_{INTs}	4-27	$\overline{INT}$ setup time	before F.E., PHI1	25		ns
t_{NMIw}	4-28	$\overline{NMI}$ pulse width	at 0.8V (both edges)	70		ns
t_{DIs}	4-14	Data setup (slave read cycle)	before F.E., PHI2 T1	15		ns
t_{DIh}	4-14	Data hold (slave read cycle)	after R.E., PHI1 T4	3		ns
t_{SPCd}	4-15	$\overline{SPC}$ pulse delay from slave	after R.E., PHI2 T4	25		ns
t_{SPCs}	4-15	$\overline{SPC}$ setup time	before F.E., PHI1	25		ns
t_{SPCw}	4-15	$\overline{SPC}$ pulse width from slave processor (async input)	at 0.8V (both edges)	20		ns
t_{ATs}	4-16	$\overline{AT}/\overline{SPC}$ setup for address translation strap	before R.E., PHI1 of cycle during which $\overline{RST}$ pulse is removed	1		t_{Cp}
t_{ATh}	4-16	$\overline{AT}/\overline{SPC}$ hold for address translation strap	after F.E., PHI1 of cycle during which $\overline{RST}$ pulse is removed	2		t_{Cp}

Note: This setup time is necessary to ensure prompt acknowledgement via $\overline{HLDA}$ and the ensuing floating of CPU off the buses. Note that the time from the receipt of the $\overline{HOLD}$ signal until the CPU floats is a function of the time $\overline{HOLD}$ signal goes low, the state of the RDY input (in MMU systems), and the length of the current MMU cycle.

4.4.2.3 Clocking Requirements: NS32032-10

Name	Figure	Description	Reference/ Conditions	NS32032-10		Units
				Min	Max	
t_{Cp}	4-17	Clock period	R.E., PHI1, PHI2 to next R.E., PHI1, PHI2	100	250	ns
t_{CLw}	4-17	PHI1, PHI2 pulse width	At 2.0V on PHI1, PHI2 (both edges)	$0.5t_{Cp}$ −10ns		
t_{CLh}	4-17	PHI1, PHI2 high time	At V_{CC} − 0.9V on PHI1, PHI2 (both edges)	$0.5t_{Cp}$ −15ns		
t_{CLl}	4-17	PHI1, PHI2, Low Time	at 0.8V on PHI1, PHI2	$0.5\ t_{Cp}$ −5 ns		
$t_{nOVL(1,2)}$	4-17	Non-overlap time	0.8V on F.E., PHI1, PHI2 to 0.8V on R.E., PHI2, PHI1	−2	5	ns
t_{nOVLas}		Non-overlap asymmetry ($t_{nOVL(1)} - t_{nOVL(2)}$)	at 0.8V on PHI1, PHI2	−4	4	ns
t_{CLwas}		PHI1, PHI2 asymmetry ($t_{CLw(1)} - t_{CLw(2)}$)	at 2.0V on PHI1, PHI2	−5	5	ns

4.0 Device Specifications

4.4.3 Timing Diagrams

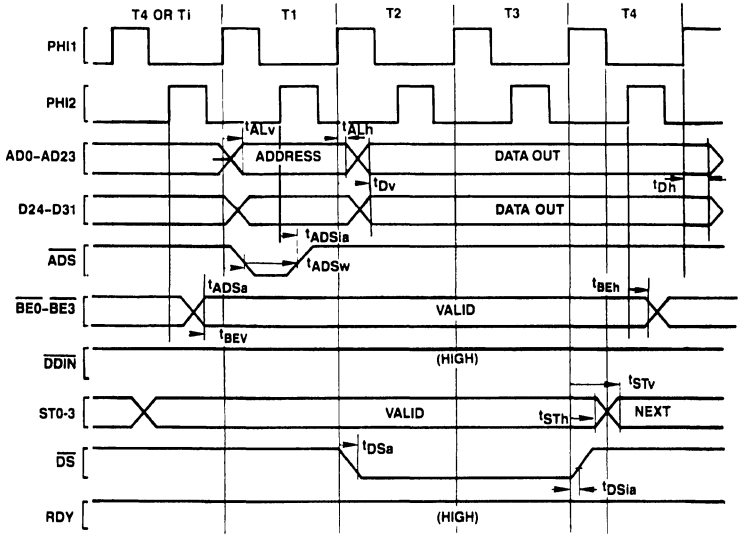


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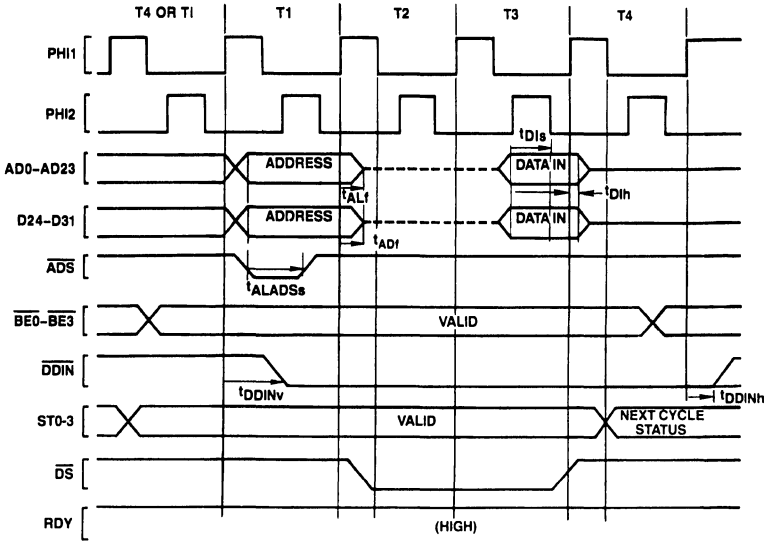
FIGURE 4-4. Write Cycle



TL/EE/5491–46

FIGURE 4-5. Read Cycle

4.0 Device Specifications (Continued)

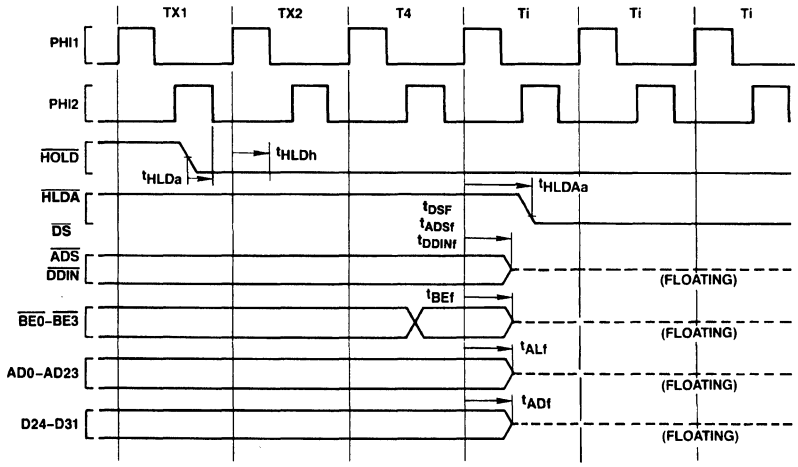


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FIGURE 4-6. Floating by $\overline{\text{HOLD}}$ Timing (CPU Not Idle Initially).

Note that whenever the CPU is not idling (not in Ti), the $\overline{\text{HOLD}}$ request ($\overline{\text{HOLD}}$ low) must be active tHLDa before the falling edge of PHI2 of the clock cycle that appears two clock cycles before T4 (TX1) and stay low until tHLDh after the rising edge of PHI1 of the clock cycle that precedes T4 (TX2) for the request to be acknowledged.

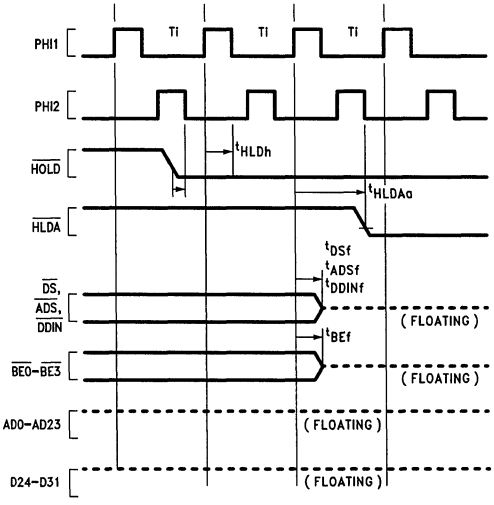

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FIGURE 4-7. Floating by $\overline{\text{HOLD}}$ Timing (CPU initially idle)

Note that during Ti1 the CPU is already idling.

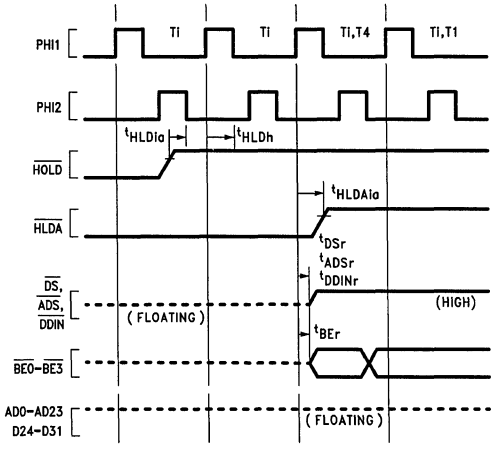

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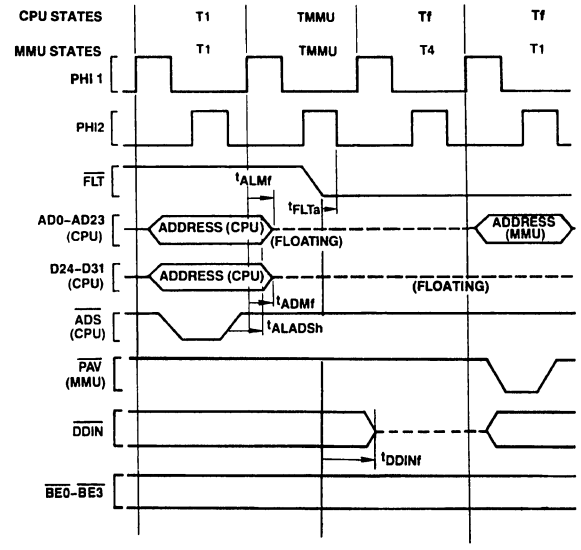
FIGURE 4-8. Release from $\overline{\text{HOLD}}$

4.0 Device Specifications (Continued)



TL/EE/5491–50

FIGURE 4-9. FLT Initiated Float Cycle Timing

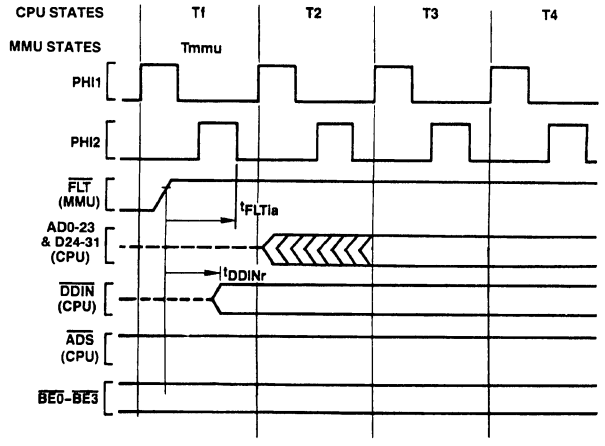


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FIGURE 4-10. Release from FLT Timing

Note that when FLT is deasserted the CPU restarts driving DDIN before the MMU releases it. This, however, does not cause any conflict, since both CPU and MMU force DDIN to the same logic level.

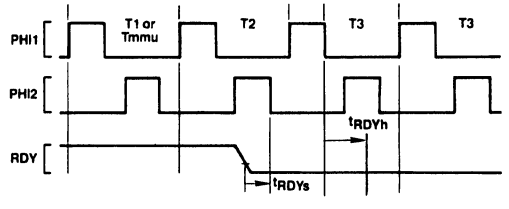

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FIGURE 4-11. Ready Sampling (CPU Initially READY)

4.0 Device Specifications (Continued)

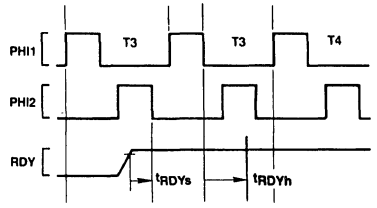

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FIGURE 4-12. Ready Sampling (CPU Initially NOT READY)

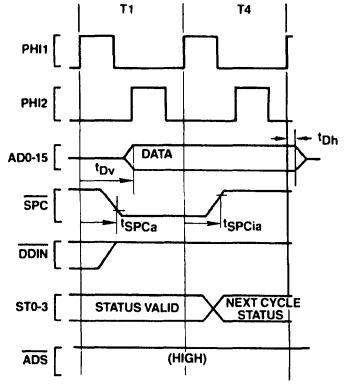

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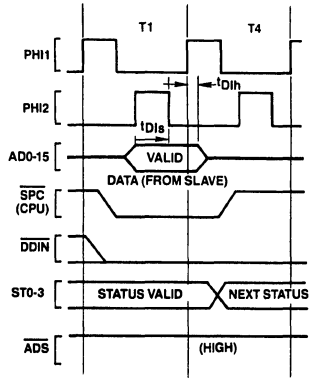
FIGURE 4-13. Slave Processor Write Timing



TL/EE/5491–55

FIGURE 4-14. Slave Processor Read Timing

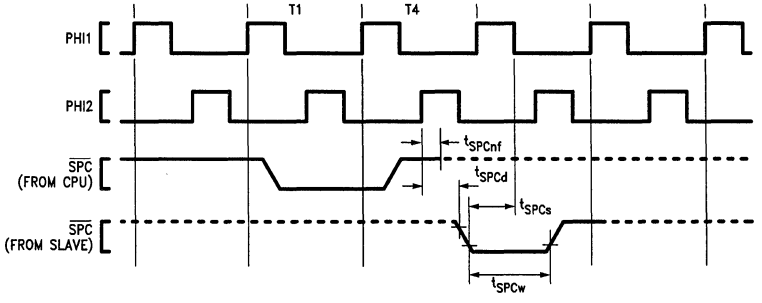


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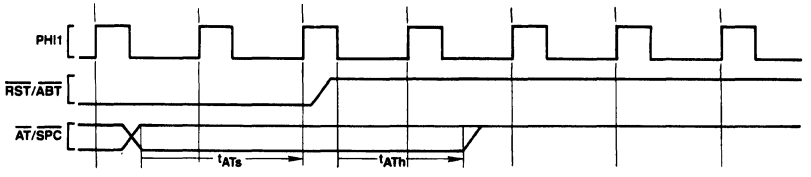
FIGURE 4-15. $\overline{SPC}$ Timing

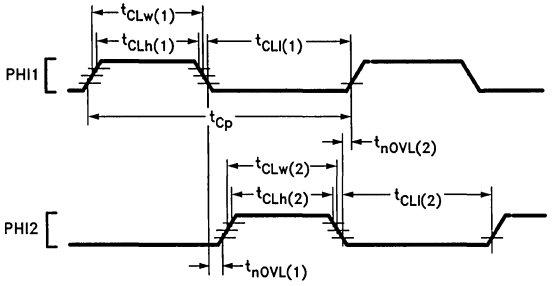
After transferring last operand to a Slave Processor, CPU turns OFF driver and holds $\overline{SPC}$ high with internal 5 kΩ pullup.



TL/EE/5491–57

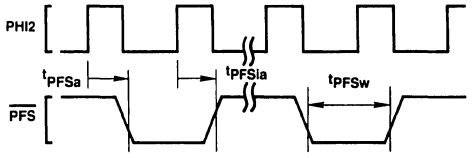
FIGURE 4-16. Reset Configuration Timing

4.0 Device Specifications (Continued)



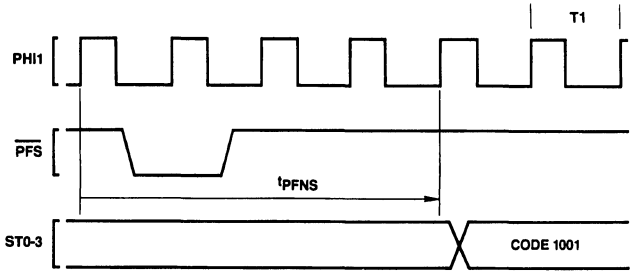
TL/EE/5491-58

FIGURE 4-17. Clock Waveforms



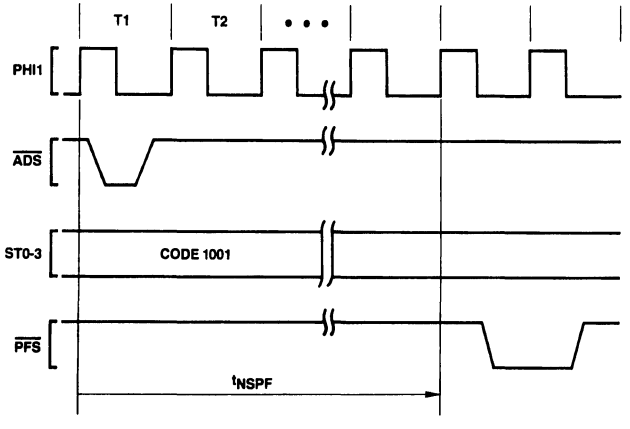
TL/EE/5491-59

FIGURE 4-18. Relationship of $\overline{PFS}$ to Clock Cycles



TL/EE/5491-60

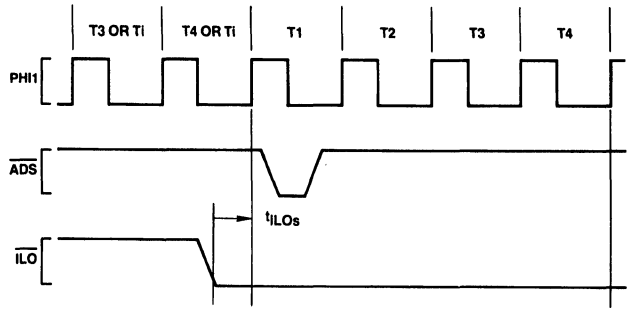
FIGURE 4-19a. Guaranteed Delay, $\overline{PFS}$ to Non-Sequential Fetch



TL/EE/5491-61

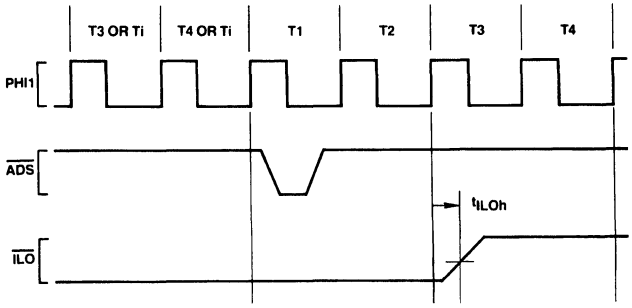
FIGURE 4-19b. Guaranteed Delay, Non-Sequential Fetch to $\overline{PFS}$

4.0 Device Specifications (Continued)



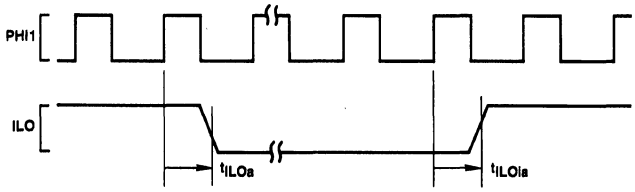
TL/EE/5491–62

FIGURE 4-20a. Relationship of $\overline{ILO}$ to First Operand Cycle of an Interlocked Instruction



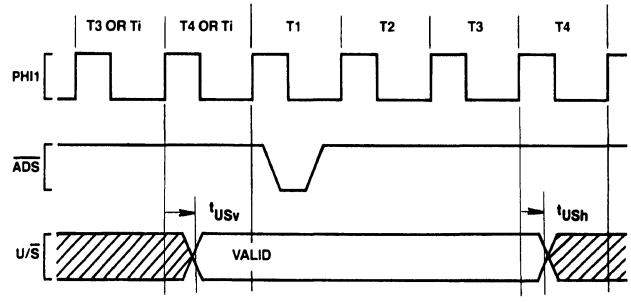
TL/EE/5491–63

FIGURE 4-20b. Relationship of $\overline{ILO}$ to Last Operand Cycle of an Interlocked Instruction



TL/EE/5491–64

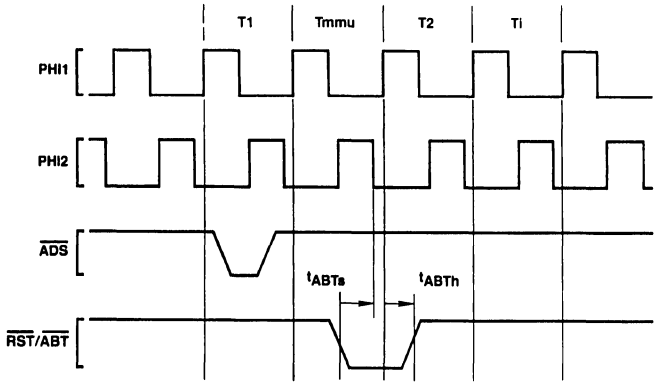
FIGURE 4-21. Relationship of $\overline{ILO}$ to Any Clock Cycle



TL/EE/5491–65

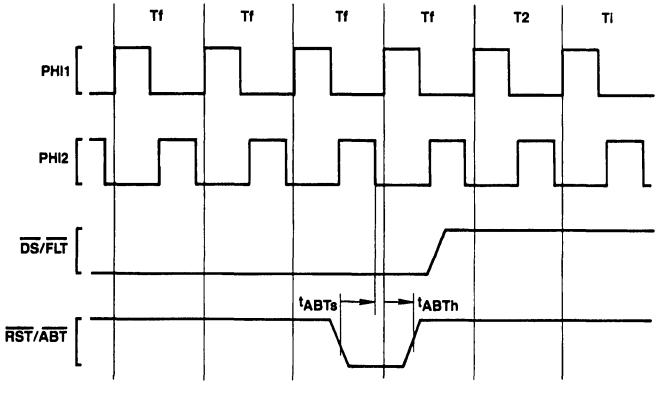
FIGURE 4-22. U/$\overline{S}$ Relationship to Any Bus Cycle — Guaranteed Valid Interval

4.0 Device Specifications (Continued)



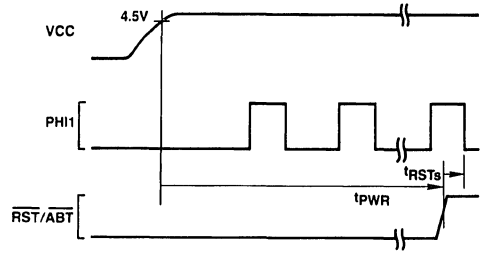
TL/EE/5491–66

FIGURE 4-23. Abort Timing, $\overline{FLT}$ Not Applied



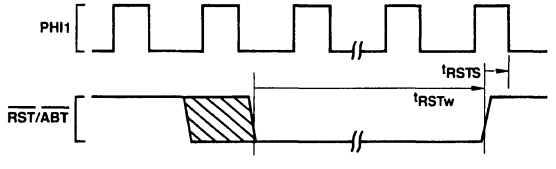
TL/EE/5491–67

FIGURE 4-24. Abort Timing, $\overline{FLT}$ Applied



TL/EE/5491–68

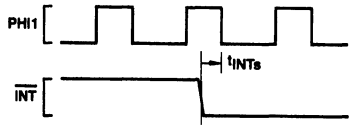
FIGURE 4-25. Power-On Reset



TL/EE/5491–69

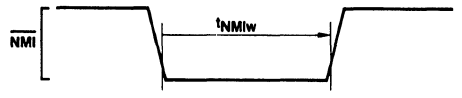
FIGURE 4-26. Non-Power-On Reset

4.0 Device Specifications (Continued)



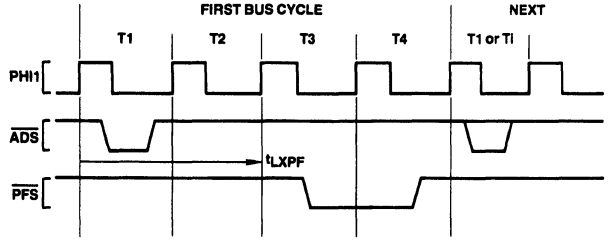
TL/EE/5491–70

FIGURE 4-27. $\overline{INT}$ Interrupt Signal Detection



TL/EE/5491–71

FIGURE 4-28. $\overline{NMI}$ Interrupt Signal Timing



TL/EE/5491–72

FIGURE 4-29. Relationship Between Last Data Transfer of an Instruction and $\overline{PFS}$ Pulse of Next Instruction

Note: In a transfer of a Read-Modify-Write type operand, this is the Read transfer, displaying RMW Status (Code 1011).

Appendix A: Instruction Formats

NOTATIONS

i= Integer Type Field
B = 00 (Byte)
W = 01 (Word)
D = 11 (Double Word)

f= Floating Point Type Field
F = 1 (Std. Floating: 32 bits)
L = 0 (Long Floating: 64 bits)

c= Custom Type Field
D = 1 (Double Word)
Q = 0 (Quad Word)

op= Operation Code
Valid encodings shown with each format.

gen, gen 1, gen 2= General Addressing Mode Field
See Sec. 2.2 for encodings.

reg= General Purpose Register Number

cond= Condition Code Field
0000 = EQual: Z = 1
0001 = Not Equal: Z = 0
0010 = Carry Set: C = 1
0011 = Carry Clear: C = 0
0100 = HIgher: L = 1
0101 = Lower or Same: L = 0
0110 = Greater Than: N = 1
0111 = Less or Equal: N = 0
1000 = Flag Set: F = 1
1001 = Flag Clear: F = 0
1010 = LOwer: L = 0 and Z = 0
1011 = Higher or Same: L = 1 or Z = 1
1100 = Less Than: N = 0 and Z = 0
1101 = Greater or Equal: N = 1 or Z = 1
1110 = (Unconditionally True)
1111 = (Unconditionally False)

short= Short Immediate value. May contain
quick: Signed 4-bit value, in MOVQ, ADDQ, CMPQ, ACB.
cond: Condition Code (above), in Scond.
areg: CPU Dedicated Register, in LPR, SPR.
0000 = US
0001 – 0111 = (Reserved)
1000 = FP
1001 = SP
1010 = SB
1011 = (Reserved)
1100 = (Reserved)
1101 = PSR
1110 = INTBASE
1111 = MOD
Options: in String Instructions

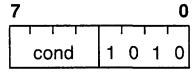
U/W	B	T

T = Translated
B = Backward
U/W = 00: None
01: While Match
11: Until Match

Configuration bits, in SETCFG:

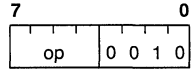
C	M	F	I

mreg NS32082: MMU Register number, in LMR, SMR.
0000 = BPR0
0001 = BPR1
0010 = (Reserved)
0011 = (Reserved)
0100 = (Reserved)
0101 = (Reserved)
0110 = (Reserved)
0111 = (Reserved)
1000 = (Reserved)
1001 = (Reserved)
1010 = MSR
1011 = BCNT
1100 = PTB0
1101 = PTB1
1110 = (Reserved)
1111 = EIA



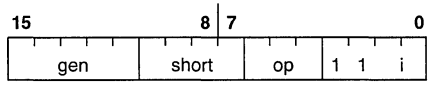
Format 0

Bcond (BR)



Format 1

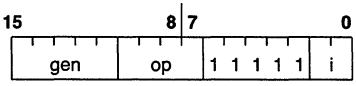
BSR	-0000	ENTER	-1000
RET	-0001	EXIT	-1001
CXP	-0010	NOP	-1010
RXP	-0011	WAIT	-1011
RETT	-0100	DIA	-1100
RETI	-0101	FLAG	-1101
SAVE	-0110	SVC	-1110
RESTORE	-0111	BPT	-1111



Format 2

ADDQ	-000	ACB	-100
CMPQ	-001	MOVQ	-101
SPR	-010	LPR	-110
Scond	-011		

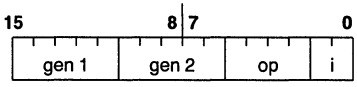
Appendix A: Instruction Formats (Continued)



Format 3

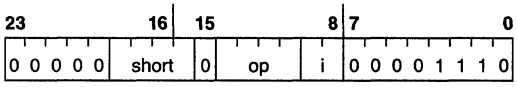
CXPD	-0000	ADJSP	-1010
BICPSR	-0010	JSR	-1100
JUMP	-0100	CASE	-1110
BISPSR	-0110		

Trap (UND) on XXX1, 1000



Format 4

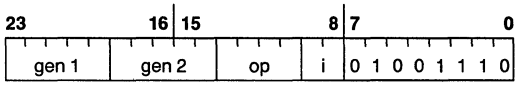
ADD	-0000	SUB	-1000
CMP	-0001	ADDR	-1001
BIC	-0010	AND	-1010
ADDC	-0100	SUBC	-1100
MOV	-0101	TBIT	-1101
OR	-0110	XOR	-1110



Format 5

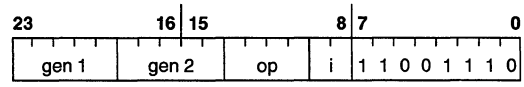
MOVS	-0000	SETCFG	-0010
CMPS	-0001	SKPS	-0011

Trap (UND) on 1XXX, 01XX



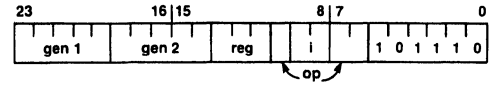
Format 6

ROT	-0000	NEG	-1000
ASH	-0001	NOT	-1001
CBIT	-0010	Trap (UND)	-1010
CBITI	-0011	SUBP	-1011
Trap (UND)	-0100	ABS	-1100
LSH	-0101	COM	-1101
SBIT	-0110	IBIT	-1110
SBITI	-0111	ADDP	-1111



Format 7

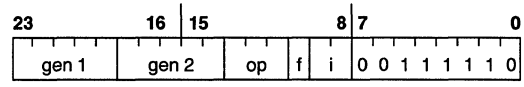
MOVM	-0000	MUL	-1000
CMPM	-0001	MEI	-1001
INSS	-0010	Trap (UND)	-1010
EXTS	-0011	DEI	-1011
MOVXBW	-0100	QUO	-1100
MOVZBW	-0101	REM	-1101
MOVZiD	-0110	MOD	-1110
MOVXiD	-0111	DIV	-1111



TL/EE/5491–73

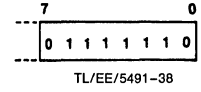
Format 8

EXT	-0 00	INDEX	-1 00
CVTP	-0 01	FFS	-1 01
INS	-0 10		
CHECK	-0 11		
MOVSU	-110, reg = 001		
MOVUS	-110, reg = 011		



Format 9

MOVif	-000	ROUND	-100
LFSR	-001	TRUNC	-101
MOVLF	-010	SFSR	-110
MOVFL	-011	FLOOR	-111

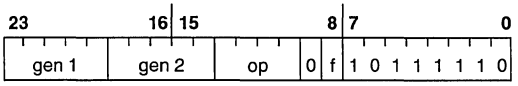


TL/EE/5491–38

Format 10

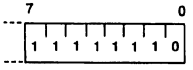
Trap (UND) Always

Appendix A: Instruction Formats (Continued)



Format 11

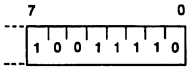
ADDf	-0000	DIVf	-1000
MOVf	-0001	Trap (SLAVE)	-1001
CMPf	-0010	Trap (UND)	-1010
Trap (SLAVE)	-0011	Trap (UND)	-1011
SUBf	-0100	MULf	-1100
NEGf	-0101	ABSf	-1101
Trap (UND)	-0110	Trap (UND)	-1110
Trap (UND)	-0111	Trap (UND)	-1111



TL/EE/5491–75

Format 12

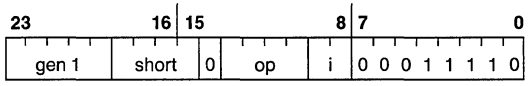
Trap (UND) Always



TL/EE/5491–76

Format 13

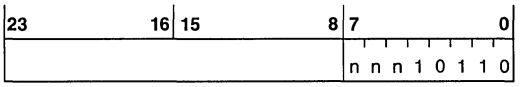
Trap (UND) Always



Format 14

RDVAL	-0000	LMR	-0010
WRVAL	-0001	SMR	-0011

Trap (UND) on 01XX, 1XXX



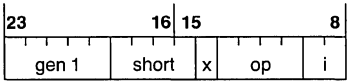
Operation Word ID Byte

Format 15

(Custom Slave)

nnn **Operation Word Format**

000

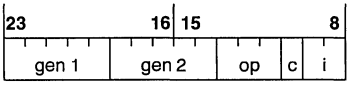


Format 15.0

CATST0	-0000	LCR	-0010
CATST1	-0001	SCR	-0011

Trap (UND) on all others

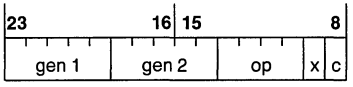
001



Format 15.1

CCV3	-000	CCV2	-100
LCSR	-001	CCV1	-101
CCV5	-010	SCSR	-110
CCV4	-011	CCV0	-111

101

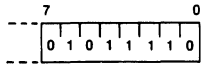


Format 15.5

CCAL0	-0000	CCAL3	-1000
CMOV0	-0001	CMOV3	-1001
CCMP0	-0010	Trap (UND)	-1010
CCMP1	-0011	Trap (UND)	-1011
CCAL1	-0100	CCAL2	-1100
CMOV2	-0101	CMOV1	-1101
Trap (UND)	-0110	Trap (UND)	-1110
Trap (UND)	-0111	Trap (UND)	-1111

If nnn = 010, 011, 100, 110, 111
then Trap (UND) Always

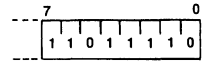
Appendix A: Instruction Formats (Continued)



TL/EE/5491-77

Format 16

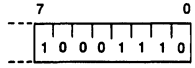
Trap (UND) Always



TL/EE/5491-78

Format 17

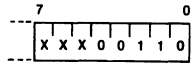
Trap (UND) Always



TL/EE/5491-79

Format 18

Trap (UND) Always

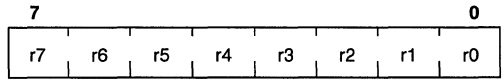


TL/EE/5491-80

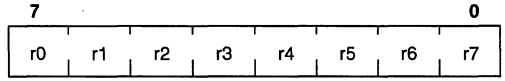
Format 19

Trap (UND) Always

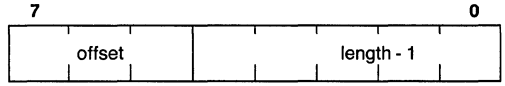
Implied Immediate Encodings:



Register Mark, appended to SAVE, ENTER



Register Mark, appended to RESTORE, EXIT



Offset/Length Modifier appended to INSS, EXTS

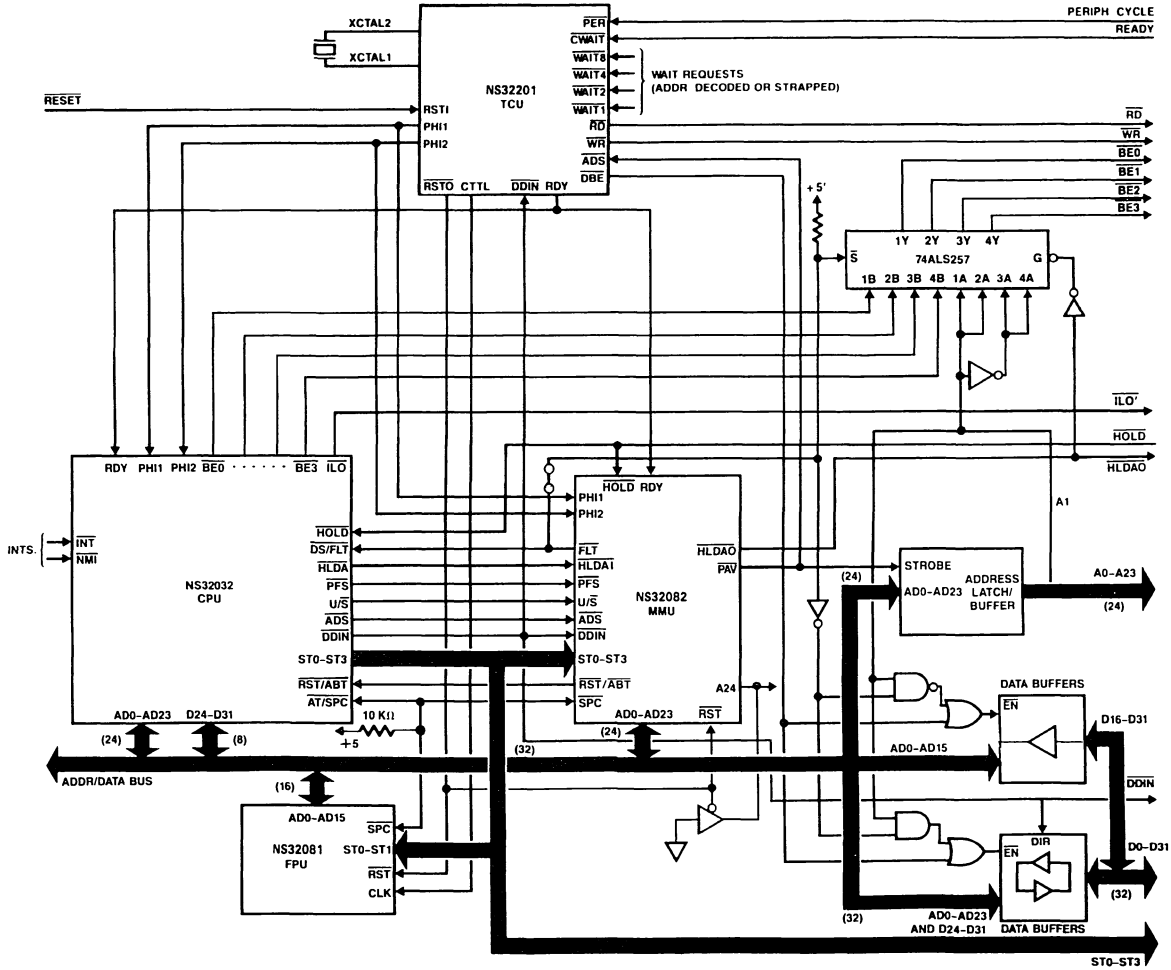


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FIGURE B-1. System Connection Diagram

National Semiconductor

PRELIMINARY

NS32CG16-10/NS32CG16-15
High-Performance Printer/Display Processor

General Description

The NS32CG16 is a 32-bit microprocessor in the Series 32000® family that provides special features for graphics applications. It is specifically designed to support page oriented printing technologies such as Laser, LCS, LED, Ion-Deposition and InkJet.

The NS32CG16 provides a 16 Mbyte linear address space and a 16-bit external data bus. It also has a 32-bit ALU, an eight-byte prefetch queue, and a slave processor interface.

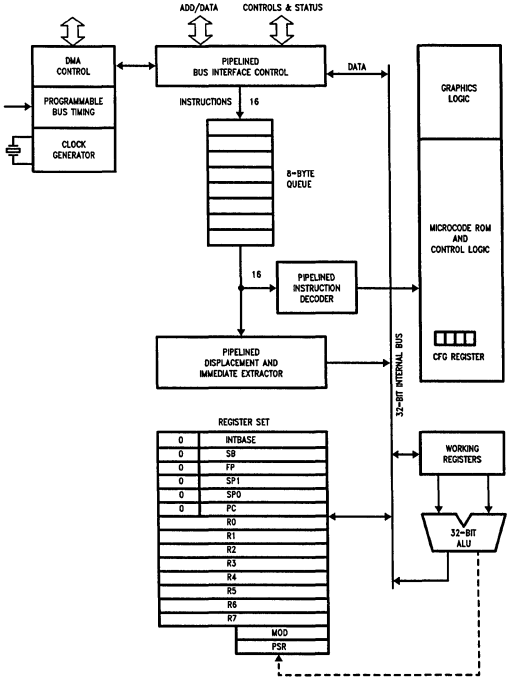
The capabilities of the NS32CG16 can be expanded by using an external floating point unit which interfaces to the NS32CG16 as a slave processor. This combination provides optimal support for outline character fonts.

The NS32CG16 highly efficient architecture, in addition to the built-in capabilities for supporting BITBLT (BIT-aligned BLock Transfer) operations and other special graphics functions, make the device the ideal choice to handle a variety of page description languages such as Postscript™, CCS-Page™ and PCL™.

Features

- Software compatible with the Series 32000 family
- 32-bit architecture and implementation
- 16 Mbyte linear address space
- Special support for graphics applications
  - — 18 graphics instructions
  - — Binary compression/expansion capability for font storage using RLL encoding
  - — Pattern magnification for Epson and HP LaserJet™ emulations
  - — 6 BITBLT instructions on chip
  - — Interface to an external BITBLT processing unit for very fast BITBLT operations (optional)
- Floating point support via the NS32081 or the NS32381 for outline font, scaling and rotation
- On-chip clock generator
- Optimal interface to large memory arrays via the DP84xx family of DRAM controllers
- Power save mode
- High-speed CMOS technology
- 68-pin plastic PCC package

Block Diagram



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National Semiconductor

PRELIMINARY

NS32C016-10/NS32C016-15
High-Performance Microprocessors

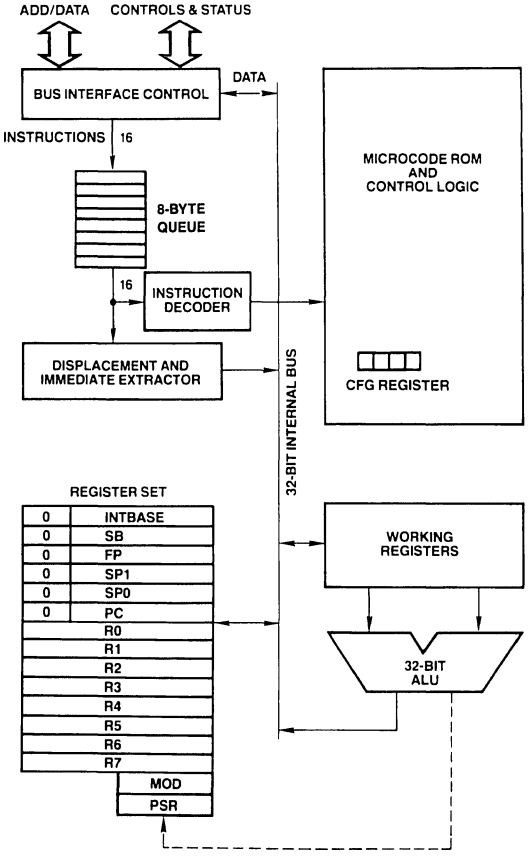
General Description

The NS32C016 is a 32-bit, CMOS microprocessor with TTL compatible inputs. The NS32C016 has a 16M byte linear address space and a 16-bit external data bus. It is fabricated with National Semiconductor's advanced CMOS process and is fully object code compatible with other Series 32000® CPU's. The NS32C016 has a 32-bit ALU, eight 32-bit general purpose registers, an eight-byte prefetch queue and a highly symmetric architecture. It also incorporates a slave processor interface and provides for full virtual memory capability in conjunction with the NS32082 memory management unit (MMU). High performance floating-point instructions are provided with the NS32081 floating-point unit (FPU). The NS32C016 is intended for a wide range of high performance computer applications.

Features

- 32-bit architecture and implementation
- 16M byte uniform addressing space
- Powerful instruction set
  - — General 2-address capability
  - — Very high degree of symmetry
  - — Addressing modes optimized for high-level Language references
- High-speed CMOS technology
- TTL compatible inputs
- Single 5V supply
- 48-pin dual-in-line package

Block Diagram



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1.0 Product Introduction

The Series 32000 Microprocessor family is a new generation of devices using National's XMOS and CMOS technologies. By combining state-of-the-art MOS technology with a very advanced architectural design philosophy, this family brings mainframe computer processing power to VLSI processors.

The Series 32000 family supports a variety of system configurations, extending from a minimum low-cost system to a powerful 4 gigabyte system. The architecture provides complete upward compatibility from one family member to another. The family consists of a selection of CPUs supported by a set of peripherals and slave processors that provide sophisticated interrupt and memory management facilities as well as high-speed floating-point operations. The architectural features of the Series 32000 family are described briefly below:

Powerful Addressing Modes. Nine addressing modes available to all instructions are included to access data structures efficiently.

Data Types. The architecture provides for numerous data types, such as byte, word, doubleword, and BCD, which may be arranged into a wide variety of data structures.

Symmetric Instruction Set. While avoiding special case instructions that compilers can't use, the Series 32000 family incorporates powerful instructions for control operations, such as array indexing and external procedure calls, which save considerable space and time for compiled code.

Memory-to-Memory Operations. The Series 32000 CPUs represent two-address machines. This means that each operand can be referenced by any one of the addressing modes provided. This powerful memory-to-memory architecture permits memory locations to be treated as registers for all useful operations. This is important for temporary operands as well as for context switching.

Memory Management. Either the NS32382 or the NS32082 Memory Management Unit may be added to the system to provide advanced operating system support functions, including dynamic address translation, virtual memory management, and memory protection.

Large, Uniform Addressing. The NS32C016 has 24-bit address pointers that can address up to 16 megabytes without any segmentation; this addressing scheme provides flexible memory management without added-on expense.

Modular Software Support. Any software package for the Series 32000 family can be developed independent of all other packages, without regard to individual addressing. In addition, ROM code is totally relocatable and easy to access, which allows a significant reduction in hardware and software cost.

Software Processor Concept. The Series 32000 architecture allows future expansions of the instruction set that can be executed by special slave processors, acting as extensions to the CPU. This concept of slave processors is unique to the Series 32000 family. It allows software compatibility even for future components because the slave hardware is transparent to the software. With future advances in semiconductor technology, the slaves can be physically integrated on the CPU chip itself.

To summarize, the architectural features cited above provide three primary performance advantages and characteristics:

- High-Level Language Support
- Easy Future Growth Path
- Application Flexibility

2.0 Architectural Description

2.1 PROGRAMMING MODEL

The Series 32000 architecture includes 16 registers on the NS32C016 CPU.

2.1.1 General Purpose Registers

There are eight registers for meeting high speed general storage requirements, such as holding temporary variables and addresses. The general purpose registers are free for any use by the programmer. They are thirty-two bits in length. If a general register is specified for an operand that is eight or sixteen bits long, only the low part of the register is used; the high part is not referenced or modified.

2.1.2 Dedicated Registers

The eight dedicated registers of the NS32C016 are assigned specific functions.

PC: The PROGRAM COUNTER register is a pointer to the first byte of the instruction currently being executed. The PC is used to reference memory in the program section. (In the NS32C016 the upper eight bits of this register are always zero.)

SP0, SP1: The SP0 register points to the lowest address of the last item stored on the INTERRUPT STACK. This stack is normally used only by the operating system. It is used primarily for storing temporary data, and holding return information for operating system subroutines and interrupt and

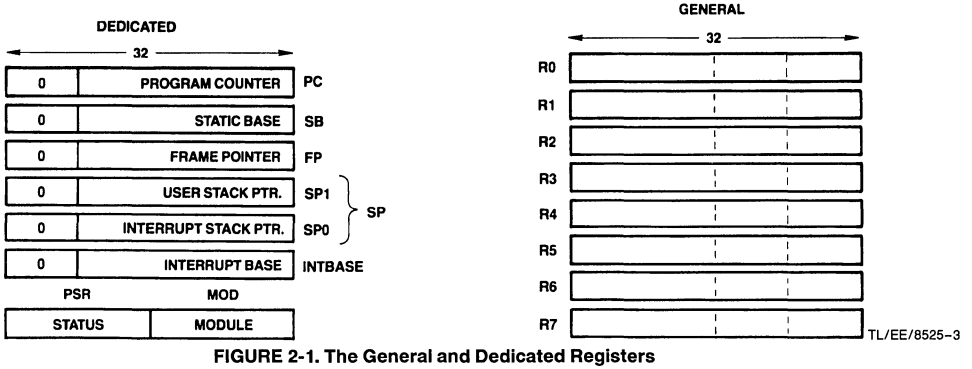

FIGURE 2-1. The General and Dedicated Registers

2.0 Architectural Description (Continued)

trap service routines. The SP1 register points to the lowest address of the last item stored on the USER STACK. This stack is used by normal user programs to hold temporary data and subroutine return information.

In this document, reference is made to the SP register. The terms "SP register" or "SP" refer to either SP0 or SP1, depending on the setting of the S bit in the PSR register. If the S bit in the PSR is 0 then SP refers to SP0. If the S bit in the PSR is 1 then SP refers to SP1. (In the NS32C016 the upper eight bits of these registers are always zero.)

Stacks in the Series 32000 family grow downward in memory. A Push operation pre-decrements the Stack Pointer by the operand length. A Pop operation post-increments the Stack Pointer by the operand length.

FP: The FRAME POINTER register is used by a procedure to access parameters and local variables on the stack. The FP register is set up on procedure entry with the ENTER instruction and restored on procedure termination with the EXIT instruction.

The frame pointer holds the address in memory occupied by the old contents of the frame pointer. (In the NS32C016 the upper eight bits of this register are always zero.)

SB: The STATIC BASE register points to the global variables of a software module. This register is used to support relocatable global variables for software modules. The SB register holds the lowest address in memory occupied by the global variables of a module. (In the NS32C016 the upper eight bits of this register are always zero.)

INTBASE: The INTERRUPT BASE register holds the address of the dispatch table for interrupts and traps (Section 3.8). The INTBASE register holds the lowest address in memory occupied by the dispatch table. (In the NS32C016 the upper eight bits of this register are always zero.)

MOD: The MODULE register holds the address of the module descriptor of the currently executing software module. The MOD register is sixteen bits long, therefore the module table must be contained within the first 64k bytes of memory.

PSR: The PROCESSOR STATUS REGISTER (PSR) holds the status codes for the NS32C016 microprocessor.

The PSR is sixteen bits long, divided into two eight-bit halves. The low order eight bits are accessible to all programs, but the high order eight bits are accessible only to programs executing in Supervisor Mode.

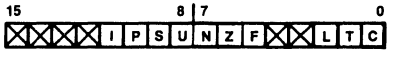

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FIGURE 2-2. Processor Status Register

C: The C bit indicates that a carry or borrow occurred after an addition or subtraction instruction. It can be used with the ADDC and SUBC instructions to perform multiple-precision integer arithmetic calculations. It may have a setting of 0 (no carry or borrow) or 1 (carry or borrow).

T: The T bit causes program tracing. If this bit is a 1, a TRC trap is executed after every instruction (Section 3.8.5).

L: The L bit is altered by comparison instructions. In a comparison instruction the L bit is set to "1" if the second operand is less than the first operand, when both operands are interpreted as unsigned integers. Otherwise, it is set to "0". In Floating Point comparisons, this bit is always cleared.

F: The F bit is a general condition flag, which is altered by many instructions (e.g., integer arithmetic instructions use it to indicate overflow).

Z: The Z bit is altered by comparison instructions. In a comparison instruction the Z bit is set to "1" if the second operand is equal to the first operand; otherwise it is set to "0".

N: The N bit is altered by comparison instructions. In a comparison instruction the N bit is set to "1" if the second operand is less than the first operand, when both operands are interpreted as signed integers. Otherwise, it is set to "0".

U: If the U bit is "1" no privileged instructions may be executed. If the U bit is "0" then all instructions may be executed. When U=0 the NS32C016 is said to be in Supervisor Mode; when U=1 the NS32C016 is said to be in User Mode. A User Mode program is restricted from executing certain instructions and accessing certain registers which could interfere with the operating system. For example, a User Mode program is prevented from changing the setting of the flag used to indicate its own privilege mode. A Supervisor Mode program is assumed to be a trusted part of the operating system, hence it has no such restrictions.

S: The S bit specifies whether the SP0 register or SP1 register is used as the stack pointer. The bit is automatically cleared on interrupts and traps. It may have a setting of 0 (use the SP0 register) or 1 (use the SP1 register).

P: The P bit prevents a TRC trap from occurring more than once for an instruction (Section 3.8.5). It may have a setting of 0 (no trace pending) or 1 (trace pending).

I: If I=1, then all interrupts will be accepted (Section 3.8). If I=0, only the NMI interrupt is accepted. Trap enables are not affected by this bit.

2.1.3 The Configuration Register (CFG)

Within the Control section of the NS32C016 CPU is the four-bit CFG Register, which declares the presence of certain external devices. It is referenced by only one instruction, SETCFG, which is intended to be executed only as part of system initialization after reset. The format of the CFG Register is shown in *Figure 2-3.*

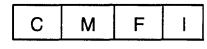


FIGURE 2-3. CFG Register

The CFG I bit declares the presence of external interrupt vectoring circuitry (specifically, the NS32202 Interrupt Control Unit). If the CFG I bit is set, interrupts requested through the $\overline{\text{INT}}$ pin are "Vectored." If it is clear, these interrupts are "Non-Vectored." See Section 3.8.

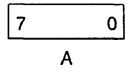
The F, M and C bits declare the presence of the FPU, MMU and Custom Slave Processors. If these bits are not set, the corresponding instructions are trapped as being undefined.

2.1.4 Memory Organization

The main memory of the NS32C016 is a uniform linear address space. Memory locations are numbered sequentially starting at zero and ending at $2^{24} - 1$. The number specifying a memory location is called an address. The contents of each memory location is a byte consisting of eight bits. Unless otherwise noted, diagrams in this document show data stored in memory with the lowest address on the right and the highest address on the left. Also, when data is shown vertically, the lowest address is at the top of a diagram and

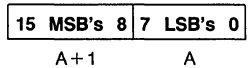
2.0 Architectural Description (Continued)

the highest address at the bottom of the diagram. When bits are numbered in a diagram, the least significant bit is given the number zero, and is shown at the right of the diagram. Bits are numbered in increasing significance and toward the left.



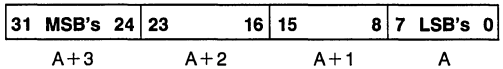
Byte at Address A

Two contiguous bytes are called a word. Except where noted (Section 2.2.1), the least significant byte of a word is stored at the lower address, and the most significant byte of the word is stored at the next higher address. In memory, the address of a word is the address of its least significant byte, and a word may start at any address.



Word at Address A

Two contiguous words are called a double word. Except where noted (Section 2.2.1), the least significant word of a double word is stored at the lowest address and the most significant word of the double word is stored at the address two greater. In memory, the address of a double word is the address of its least significant byte, and a double word may start at any address.



Double Word at Address A

Although memory is addressed as bytes, it is actually organized as words. Therefore, words and double words that are aligned to start at even addresses (multiples of two) are accessed more quickly than words and double words that are not so aligned.

2.1.5 Dedicated Tables

Two of the NS32C016 dedicated registers (MOD and INTBASE) serve as pointers to dedicated tables in memory.

The INTBASE register points to the Interrupt Dispatch and Cascade tables. These are described in Section 3.8.

The MOD register contains a pointer into the Module Table, whose entries are called Module Descriptors. A Module Descriptor contains four pointers, three of which are used by the NS32C016. The MOD register contains the address of the Module Descriptor for the currently running module. It is automatically updated by the Call External Procedure instructions (CXP and CXPD).

The format of a Module Descriptor is shown in *Figure 2-4*. The Static Base entry contains the address of static data assigned to the running module. It is loaded into the CPU Static Base register by the CXP and CXPD instructions. The Program Base entry contains the address of the first byte of instruction code in the module. Since a module may have multiple entry points, the Program Base pointer serves only as a reference to find them.

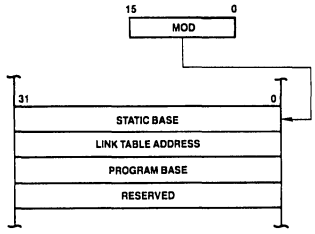


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FIGURE 2-4. Module Descriptor Format

The Link Table Address points to the Link Table for the currently running module. The Link Table provides the information needed for:

1) Sharing variables between modules. Such variables are accessed through the Link Table via the External addressing mode.
2) Transferring control from one module to another. This is done via the Call External Procedure (CXP) instruction.

The format of a Link Table is given in *Figure 2-5*. A Link Table Entry for an external variable contains the 32-bit address of that variable. An entry for an external procedure contains two 16-bit fields: Module and Offset. The Module field contains the new MOD register contents for the module being entered. The Offset field is an unsigned number giving the position of the entry point relative to the new module's Program Base pointer.

For further details of the functions of these tables, see the Series 32000 Instruction Set Reference Manual.

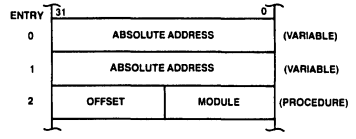

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FIGURE 2-5. A Sample Link Table

2.2 INSTRUCTION SET

2.2.1 General Instruction Format

Figure 2-6 shows the general format of a Series 32000 instruction. The Basic Instruction is one to three bytes long and contains the Opcode and up to 5-bit General Addressing Mode ("Gen") fields. Following the Basic Instruction field is a set of optional extensions, which may appear depending on the instruction and the addressing modes selected.

Index Bytes appear when either or both Gen fields specify Scaled Index. In this case, the Gen field specifies only the Scale Factor (1, 2, 4 or 8), and the Index Byte specifies which General Purpose Register to use as the index, and which addressing mode calculation to perform before indexing. See *Figure 2-7*.

Following Index Bytes come any displacements (addressing constants) or immediate values associated with the selected addressing modes. Each Disp/Imm field may contain

2.0 Architectural Description (Continued)

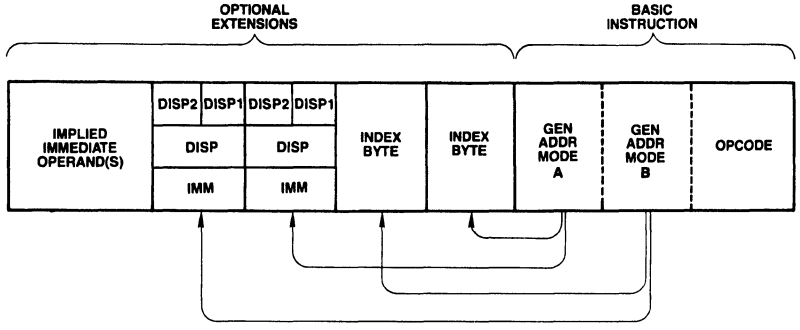

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FIGURE 2-6. General Instruction Format

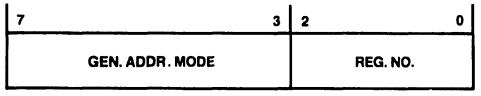

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FIGURE 2-7. Index Byte Format

one of two displacements, or one immediate value. The size of a Displacement field is encoded within the top bits of that field, as shown in *Figure 2-8,* with the remaining bits interpreted as a signed (two's complement) value. The size of an immediate value is determined from the Opcode field. Both Displacement and Immediate fields are stored most-significant byte first. Note that this is different from the memory representation of data (Section 2.1.4).

Some instructions require additional "implied" immediates and/or displacements, apart from those associated with addressing modes. Any such extensions appear at the end of the instruction, in the order that they appear within the list of operands in the instruction definition (Section 2.2.3).

2.2.2 Addressing Modes

The NS32C016 CPU generally accesses an operand by calculating its Effective Address based on information available when the operand is to be accessed. The method to be used in performing this calculation is specified by the programmer as an "addressing mode."

Addressing modes in the NS32C016 are designed to optimally support high-level language accesses to variables. In nearly all cases, a variable access requires only one addressing mode, within the instruction that acts upon that variable. Extraneous data movement is therefore minimized.

NS32C016 Addressing Modes fall into nine basic types:

Register: The operand is available in one of the eight General Purpose Registers. In certain Slave Processor instructions, an auxiliary set of eight registers may be referenced instead.

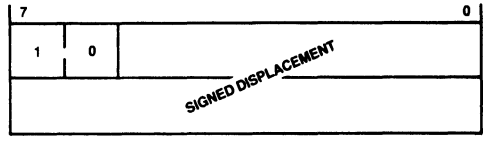
Register Relative: A General Purpose Register contains an address to which is added a displacement value from the instruction, yielding the Effective Address of the operand in memory.

Memory Space: Identical to Register Relative above, except that the register used is one of the dedicated registers PC, SP, SB or FP. These registers point to data areas generally needed by high-level languages.

Memory Relative: A pointer variable is found within the memory space pointed to by the SP, SB or FP register. A

Byte Displacement: Range −64 to +63

Word Displacement: Range −8192 to +8191



Double Word Displacement: Range (Entire Addressing Space)

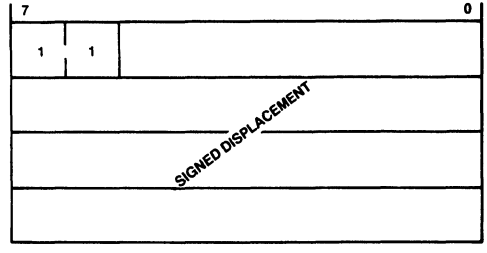


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FIGURE 2-8. Displacement Encodings

displacement is added to that pointer to generate the Effective Address of the operand.

Immediate: The operand is encoded within the instruction. This addressing mode is not allowed if the operand is to be written.

Absolute: The address of the operand is specified by a displacement field in the instruction.

External: A pointer value is read from a specified entry of the current Link Table. To this pointer value is added a displacement, yielding the Effective Address of the operand.

Top of Stack: The currently-selected Stack Pointer (SP0 or SP1) specifies the location of the operand. The operand is pushed or popped, depending on whether it is written or read.

2.0 Architectural Description (Continued)

Scaled Index: Although encoded as an addressing mode, Scaled Indexing is an option on any addressing mode except Immediate or another Scaled Index. It has the effect of calculating an Effective Address, then multiplying any General Purpose Register by 1, 2, 4 or 8 and adding into the total, yielding the final Effective Address of the operand.

Table 2-1 is a brief summary of the addressing modes. For a complete description of their actions, see the Series 32000 Instruction Set Reference Manual.

TABLE 2-1. NS32C016 Addressing Modes

ENCODING	MODE	ASSEMBLER SYNTAX	EFFECTIVE ADDRESS
Register			
00000	Register 0	R0 or F0	None: Operand is in the specified register.
00001	Register 1	R1 or F1	
00010	Register 2	R2 or F2	
00011	Register 3	R3 or F3	
00100	Register 4	R4 or F4	
00101	Register 5	R5 or F5	
00110	Register 6	R6 or F6	
00111	Register 7	R6 or F7	
Register Relative			
01000	Register 0 relative	disp(R0)	Disp + Register.
01001	Register 1 relative	disp(R1)	
01010	Register 2 relative	disp(R2)	
01011	Register 3 relative	disp(R3)	
01100	Register 4 relative	disp(R4)	
01101	Register 5 relative	disp(R5)	
01110	Register 6 relative	disp(R6)	
01111	Register 7 relative	disp(R7)	
Memory Relative			
10000	Frame memory relative	disp2(disp1 (FP))	Disp2 + Pointer; Pointer found at address Disp 1 + Register. "SP" is either SP0 or SP1, as selected in PSR.
10001	Stack memory relative	disp2(disp1 (SP))	
10010	Static memory relative	disp2(disp1 (SB))	
Reserved			
10011	(Reserved for Future Use)		
Immediate			
10100	Immediate	value	None: Operand is input from instruction queue.
Absolute			
10101	Absolute	@disp	Disp.
External			
10110	External	EXT (disp1) + disp2	Disp2 + Pointer; Pointer is found at Link Table Entry number Disp1.
Top Of Stack			
10111	Top of stack	TOS	Top of current stack, using either User or Interrupt Stack Pointer, as selected in PSR. Automatic Push/Pop included.
Memory Space			
11000	Frame memory	disp(FP)	Disp + Register; "SP" is either SP0 or SP1, as selected in PSR.
11001	Stack memory	disp(SP)	
11010	Static memory	disp(SB)	
11011	Program memory	* + disp	
Scaled Index			
11100	Index, bytes	mode[Rn:B]	EA (mode) + Rn.
11101	Index, words	mode[Rn:W]	EA (mode) + 2×Rn.
11110	Index, double words	mode[Rn:D]	EA (mode) + 4×Rn.
11111	Index, quad words	mode[Rn:Q]	EA (mode) + 8×Rn. "Mode" and "n" are contained within the Index Byte. EA (mode) denotes the effective address generated using mode.

2.0 Architectural Description (Continued)

2.2.3 Instruction Set Summary

Table 2-2 presents a brief description of the NS32C016 instruction set. The Format column refers to the Instruction Format tables (Appendix A). The Instruction column gives the instruction as coded in assembly language, and the Description column provides a short description of the function provided by that instruction. Further details of the exact operations performed by each instruction may be found in the Series 32000 Instruction Set Reference Manual.

Notations:

i = Integer length suffix: B = Byte
W = Word
D = Double Word

f = Floating Point length suffix: F = Standard Floating
L = Long Floating

gen = General operand. Any addressing mode can be specified.

short = A 4-bit value encoded within the Basic Instruction (see Appendix A for encodings).

imm = Implied immediate operand. An 8-bit value appended after any addressing extensions.

disp = Displacement (addressing constant): 8, 16 or 32 bits. All three lengths legal.

reg = Any General Purpose Register: R0–R7.

areg = Any Dedicated/Address Register: SP, SB, FP, MOD, INTBASE, PSR, US (bottom 8 PSR bits).

mreg = Any Memory Management Status/Control Register.

creg = A Custom Slave Processor Register (Implementation Dependent).

cond = Any condition code, encoded as a 4-bit field within the Basic Instruction (see Appendix A for encodings).

TABLE 2-2. NS32C016 Instruction Set Summary

MOVES

Format	Operation	Operands	Description
4	MOVi	gen,gen	Move a value.
2	MOVQi	short,gen	Extend and move a signed 4-bit constant.
7	MOVMi	gen,gen,disp	Move multiple: disp bytes (1 to 16).
7	MOVZBW	gen,gen	Move with zero extension.
7	MOVZiD	gen,gen	Move with zero extension.
7	MOVXBW	gen,gen	Move with sign extension.
7	MOVXiD	gen,gen	Move with sign extension.
4	ADDR	gen,gen	Move effective address.

INTEGER ARITHMETIC

Format	Operation	Operands	Description
4	ADDi	gen,gen	Add.
2	ADDQi	short,gen	Add signed 4-bit constant.
4	ADDCi	gen,gen	Add with carry.
4	SUBi	gen,gen	Subtract.
4	SUBCi	gen,gen	Subtract with carry (borrow).
6	NEGi	gen,gen	Negate (2's complement).
6	ABSi	gen,gen	Take absolute value.
7	MULi	gen,gen	Multiply.
7	QUOi	gen,gen	Divide, rounding toward zero.
7	REMi	gen,gen	Remainder from QUO.
7	DIVi	gen,gen	Divide, rounding down.
7	MODi	gen,gen	Remainder from DIV (Modulus).
7	MEIi	gen,gen	Multiply to extended integer.
7	DEIi	gen,gen	Divide extended integer.

PACKED DECIMAL (BCD) ARITHMETIC

Format	Operation	Operands	Description
6	ADDPi	gen,gen	Add packed.
6	SUBPi	gen,gen	Subtract packed.

2.0 Architectural Description (Continued)

TABLE 2-2. NS32C016 Instruction Set Summary (Continued)

INTEGER COMPARISON

Format	Operation	Operands	Description
4	CMPi	gen,gen	Compare.
2	CMPQi	short,gen	Compare to signed 4-bit constant.
7	CMPMi	gen,gen,disp	Compare multiple: disp bytes (1 to 16).

LOGICAL AND BOOLEAN

Format	Operation	Operands	Description
4	ANDi	gen,gen	Logical AND.
4	ORi	gen,gen	Logical OR.
4	BICi	gen,gen	Clear selected bits.
4	XORi	gen,gen	Logical exclusive OR.
6	COMi	gen,gen	Complement all bits.
6	NOTi	gen,gen	Boolean complement: LSB only.
2	Scondi	gen	Save condition code (cond) as a Boolean variable of size i.

SHIFTS

Format	Operation	Operands	Description
6	LSHi	gen,gen	Logical shift, left or right.
6	ASHi	gen,gen	Arithmetic shift, left or right.
6	ROTi	gen,gen	Rotate, left or right.

BITS

Format	Operation	Operands	Description
4	TBITi	gen,gen	Test bit.
6	SBITi	gen,gen	Test and set bit.
6	SBITIi	gen,gen	Test and set bit, interlocked.
6	CBITi	gen,gen	Test and clear bit.
6	CBITIi	gen,gen	Test and clear bit, interlocked.
6	IBITi	gen,gen	Test and invert bit.
8	FFSi	gen,gen	Find first set bit.

BIT FIELDS

Bit fields are values in memory that are not aligned to byte boundaries. Examples are PACKED arrays and records used in Pascal. "Extract" instructions read and align a bit field. "Insert" instructions write a bit field from an aligned source.

Format	Operation	Operands	Description
8	EXTi	reg,gen,gen,disp	Extract bit field (array oriented).
8	INSi	reg,gen,gen,disp	Insert bit field (array oriented).
7	EXTSi	gen,gen,imm,imm	Extract bit field (short form).
7	INSSi	gen,gen,imm,imm	Insert bit field (short form).
8	CVTP	reg,gen,gen	Convert to bit field pointer.

ARRAYS

Format	Operation	Operands	Description
8	CHECKi	reg,gen,gen	Index bounds check.
8	INDEXi	reg,gen,gen	Recursive indexing step for multiple-dimensional arrays.

2.0 Architectural Description (Continued)

TABLE 2-2. NS32C016 Instruction Set Summary (Continued)

STRINGS

String instructions assign specific functions to the General Purpose Registers:

R4 — Comparison Value
R3 — Translation Table Pointer
R2 — String 2 Pointer
R1 — String 1 Pointer
R0 — Limit Count

Options on all string instructions are:

B (Backward): Decrement strong pointers after each step rather than incrementing.

U (Until match): End instruction if String 1 entry matches R4.

W (While match): End instruction if String 1 entry does not match R4.

All string instructions end when R0 decrements to zero.

Format	Operation	Operands	Description
5	MOVSi	options	Move string 1 to string 2.
	MOVST	options	Move string, translating bytes.
5	CMPSi	options	Compare string 1 to string 2.
	CMPST	options	Compare, translating string 1 bytes.
5	SKPSi	options	Skip over string 1 entries.
	SKPST	options	Skip, translating bytes for until/while.

JUMPS AND LINKAGE

Format	Operation	Operands	Description
3	JUMP	gen	Jump.
0	BR	disp	Branch (PC Relative).
0	Bcond	disp	Conditional branch.
3	CASEi	gen	Multiway branch.
2	ACBi	short,gen,disp	Add 4-bit constant and branch if non-zero.
3	JSR	gen	Jump to subroutine.
1	BSR	disp	Branch to subroutine.
1	CXP	disp	Call external procedure
3	CXPD	gen	Call external procedure using descriptor.
1	SVC		Supervisor call.
1	FLAG		Flag trap.
1	BPT		Breakpoint trap.
1	ENTER	[reg list], disp	Save registers and allocate stack frame (Enter Procedure).
1	EXIT	[reg list]	Restore registers and reclaim stack frame (Exit Procedure).
1	RET	disp	Return from subroutine.
1	RXP	disp	Return from external procedure call.
1	RETT	disp	Return from trap. (Privileged)
1	RETI		Return from interrupt. (Privileged)

CPU REGISTER MANIPULATION

Format	Operation	Operands	Description
1	SAVE	[reg list]	Save general purpose registers.
1	RESTORE	[reg list]	Restore general purpose registers.
2	LPRi	areg,gen	Load dedicated register. (Privileged if PSR or INTBASE)
2	SPRi	areg,gen	Store dedicated register. (Privileged if PSR or INTBASE)
3	ADJSPi	gen	Adjust stack pointer.
3	BISPSRi	gen	Set selected bits in PSR. (Privileged if not Byte length)
3	BICPSRi	gen	Clear selected bits in PSR. (Privileged if not Byte length)
5	SETCFG	[option list]	Set configuration register. (Privileged)

2.0 Architectural Description (Continued)

TABLE 2-2. NS32C016 Instruction Set Summary (Continued)

FLOATING POINT

Format	Operation	Operands	Description
11	MOVf	gen,gen	Move a floating point value.
9	MOVLF	gen,gen	Move and shorten a long value to standard.
9	MOVFL	gen,gen	Move and lengthen a standard value to long.
9	MOVif	gen,gen	Convert any integer to standard or long floating.
9	ROUNDfi	gen,gen	Convert to integer by rounding.
9	TRUNCfi	gen,gen	Convert to integer by truncating, toward zero.
9	FLOORfi	gen,gen	Convert to largest integer less than or equal to value.
11	ADDf	gen,gen	Add.
11	SUBf	gen,gen	Subtract.
11	MULf	gen,gen	Multiply.
11	DIVf	gen,gen	Divide.
11	CMPf	gen,gen	Compare.
11	NEGf	gen,gen	Negate.
11	ABSf	gen,gen	Take absolute value.
9	LFSR	gen	Load FSR.
9	SFSR	gen	Store FSR.

MEMORY MANAGEMENT

Format	Operation	Operands	Description
14	LMR	mreg,gen	Load memory management register. (Privileged)
14	SMR	mreg,gen	Store memory management register. (Privileged)
14	RDVAL	gen	Validate address for reading. (Privileged)
14	WRVAL	gen	Validate address for writing. (Privileged)
8	MOVSUi	gen,gen	Move a value from supervisor space to user space. (Privileged)
8	MOVUSi	gen,gen	Move a value from user space to supervisor space. (Privileged)

MISCELLANEOUS

Format	Operation	Operands	Description
1	NOP		No operation.
1	WAIT		Wait for interrupt.
1	DIA		Diagnose. Single-byte "Branch to Self" for hardware breakpointing. Not for use in programming.

CUSTOM SLAVE

Format	Operation	Operands	Description
15.5	CCAL0c	gen,gen	Custom calculate.
15.5	CCAL1c	gen,gen	
15.5	CCAL2c	gen,gen	
15.5	CCAL3c	gen,gen	
15.5	CMOV0c	gen,gen	Custom move.
15.5	CMOV1c	gen,gen	
15.5	CMOV2c	gen,gen	
15.5	CMOV3c	gen,gen	
15.5	CCMP0c	gen,gen	Custom compare.
15.5	CCMP1c	gen,gen	
15.1	CCV0ci	gen,gen	Custom convert.
15.1	CCV1ci	gen,gen	
15.1	CCV2ci	gen,gen	
15.1	CCV3ic	gen,gen	
15.1	CCV4DQ	gen,gen	
15.1	CCV5QD	gen,gen	
15.1	LCSR	gen	Load custom status register.
15.1	SCSR	gen	Store custom status register.
15.0	CATST0	gen	Custom address/test. (Privileged)
15.0	CATST1	gen	(Privileged)
15.0	LCR	creg,gen	Load custom register. (Privileged)
15.0	SCR	creg,gen	Store custom register. (Privileged)

3.0 Functional Description

3.1 POWER AND GROUNDING

Power and ground connections for the NS32C016 are made on four pins. On-chip logic is connected to power through the logic power pin (VCCL, pin 48) and to ground through the logic ground pin (GNDL, pin 24). On-chip output drivers are connected to power through the buffer power pin (VCCP, pin 29) and to ground through the buffer ground pin (GNDB, pin 25). For optimal noise immunity, it is recommended that single conductors be connected directly from VCCL to VCCB and from GNDL to GNDB, as shown below (*Figure 3-1*).

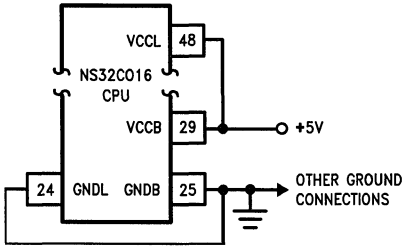

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FIGURE 3-1. Recommended Supply Connections

3.2 CLOCKING

The NS32C016 inputs clocking signals from the NS32C201 Timing Control Unit (TCU), which presents two non-overlapping phases of a single clock frequency. These phases are called PHI1 (pin 26) and PHI2 (pin 27). Their relationship to each other is shown in *Figure 3-2*.

Each rising edge of PHI1 defines a transition in the timing state ("T-State") of the CPU. One T-State represents the execution of one microinstruction within the CPU, and/or one step of an external bus transfer. See Section 4 for complete specifications of PHI1 and PHI2.

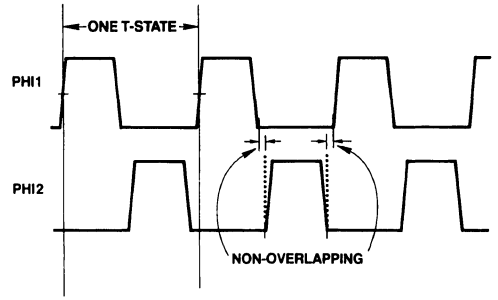

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FIGURE 3-2. Clock Timing Relationships

As the TCU presents signals with very fast transitions, it is recommended that the conductors carrying PHI1 and PHI2 be kept as short as possible, and that they not be connected anywhere except from the TCU to the CPU and, if present, the MMU. A TTL Clock signal (CTTL) is provided by the TCU for all other clocking.

3.3 RESETTING

The $\overline{RST}/\overline{ABT}$ pin serves both as a Reset for on-chip logic and as the Abort input for Memory-Managed systems. For its use as the Abort Command, see Section 3.5.4.

The CPU may be reset at any time by pulling the $\overline{RST}/\overline{ABT}$ pin low for at least 64 clock cycles. Upon detecting a reset, the CPU terminates instruction processing, resets its internal logic, and clears the Program Counter (PC) and Processor Status Register (PSR) to all zeroes.

On application of power, $\overline{RST}/\overline{ABT}$ must be held low for at least 50 μs after V_{CC} is stable. This is to ensure that all on-chip voltages are completely stable before operation. Whenever a Reset is applied, it must also remain active

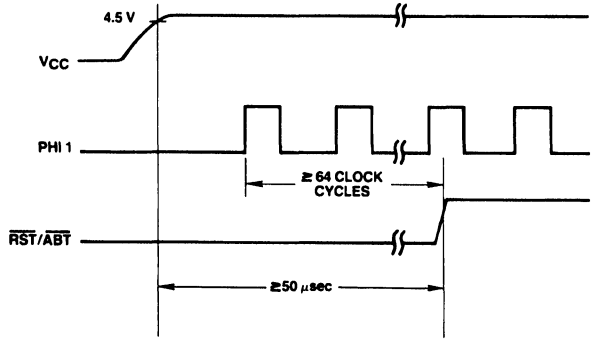

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FIGURE 3-3. Power-On Reset Requirements

3.0 Functional Description (Continued)

for not less than 64 clock cycles. The rising edge must occur while PHI1 is high. See *Figures 3-3* and *3-4.*

The NS32C201 Timing Control Unit (TCU) provides circuitry to meet the Reset requirements of the NS32C016 CPU. *Figure 3-5a* shows the recommended connections for a non-Memory-Managed system. *Figure 3-5b* shows the connections for a Memory-Managed system.

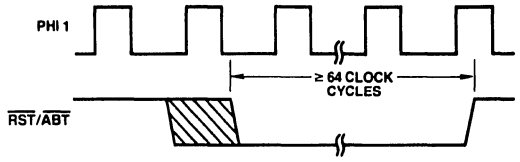

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FIGURE 3-4. General Reset Timing

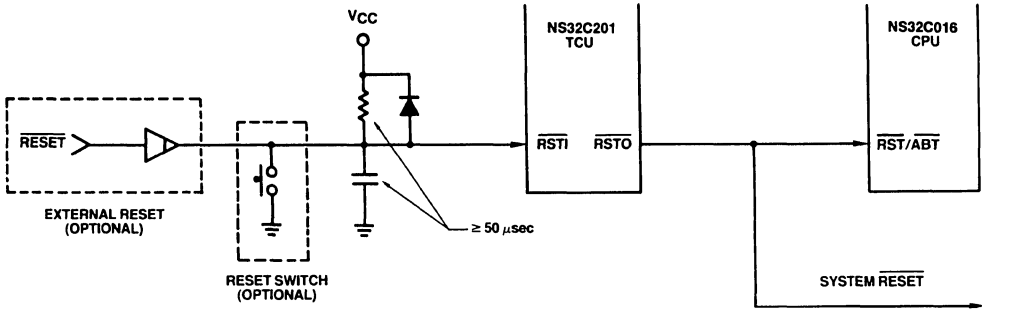

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FIGURE 3-5a. Recommended Reset Connections, Non-Memory-Managed System

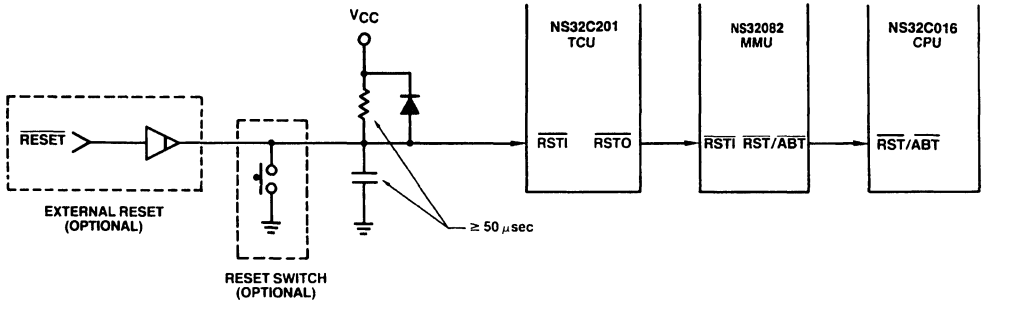

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FIGURE 3-5b. Recommended Reset Connections, Memory-Managed System

3.4 BUS CYCLES

The NS32C016 CPU has a strap option which defines the Bus Timing Mode as either With or Without Address Translation. This section describes only bus cycles under the No Address Translation option. For details of the use of the strap and of bus cycles with address translation, see Section 3.5.

The CPU will perform a bus cycle for one of the following reasons:

1) To write or read data, to or from memory or a peripheral interface device. Peripheral input and output are memory-mapped in the Series 32000 family.
2) To fetch instructions into the eight-byte instruction queue. This happens whenever the bus would otherwise be idle and the queue is not already full.
3) To acknowledge an interrupt and allow external circuitry to provide a vector number, or to acknowledge completion of an interrupt service routine.
4) To transfer information to or from a Slave Processor.

In terms of bus timing, cases 1 through 3 above are identical. For timing specifications, see Section 4. The only external difference between them is the four-bit code placed on the Bus Status pins (ST0–ST3). Slave Processor cycles differ in that separate control signals are applied (Section 3.4.6).

The sequence of events in a non-Slave bus cycle is shown in *Figure 3-7* for a Read cycle and *Figure 3-8* for a Write cycle. The cases shown assume that the selected memory or interface device is capable of communicating with the CPU at full speed. If it is not, then cycle extension may be requested through the RDY line (Section 3.4.1).

3.0 Functional Description (Continued)

A full-speed bus cycle is performed in four cycles of the PHI1 clock signal, labeled T1 through T4. Clock cycles not associated with a bus cycle are designated Ti (for "Idle").

During T1, the CPU applies an address on pins AD0–AD15 and A16–A23. It also provides a low-going pulse on the $\overline{ADS}$ pin, which serves the dual purpose of informing external circuitry that a bus cycle is starting and of providing control to an external latch for demultiplexing Address bits 0–15 from the AD0–AD15 pins. See *Figure 3-6*. During this time also the status signals $\overline{DDIN}$, indicating the direction of the transfer, and $\overline{HBE}$, indicating whether the high byte (AD8–AD15) is to be referenced, become valid.

During T2 the CPU switches the Data Bus, AD0–AD15, to either accept or present data. Note that the signals A16–A23 remain valid, and need not be latched. It also starts the data strobe ($\overline{DS}$), signaling the beginning of the data transfer. Associated signals from the NS32C201 Timing Control Unit are also activated at this time: $\overline{RD}$ (Read Strobe) or $\overline{WR}$ (Write Strobe), $\overline{TSO}$ (Timing State Output, indicating that T2 has been reached) and $\overline{DBE}$ (Data Buffer Enable).

The T3 state provides for access time requirements, and it occurs at least once in a bus cycle. At the end of T2, on the falling edge of the PHI2 clock, the RDY (Ready) line is sampled to determine whether the bus cycle will be extended (Section 3.4.1).

If the CPU is performing a Read cycle, the Data Bus (AD0–AD15) is sampled at the falling edge of PHI2 of the last T3 state, see Section 4. Data must, however, be held at least until the beginning of T4. $\overline{DS}$ and $\overline{RD}$ are guaranteed not to go inactive before this point, so the rising edge of either of them may safely be used to disable the device providing the input data.

The T4 state finishes the bus cycle. At the beginning of T4, the $\overline{DS}$, $\overline{RD}$, or $\overline{WR}$, and $\overline{TSO}$ signals go inactive, and at the rising edge of PHI2, $\overline{DBE}$ goes inactive, having provided for necessary data hold times. Data during Write cycles remains valid from the CPU throughout T4. Note that the Bus Status lines (ST0–ST3) change at the beginning of T4, anticipating the following bus cycle (if any).

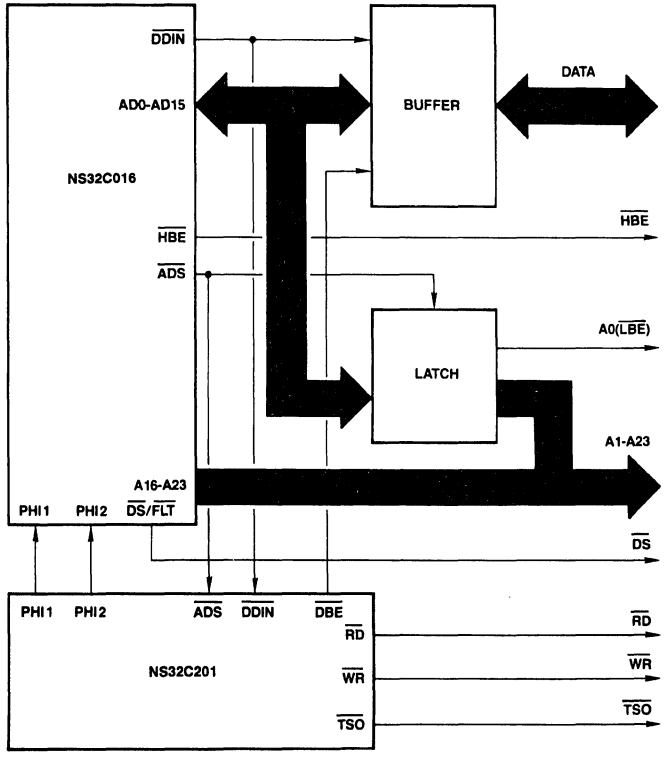

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FIGURE 3-6. Bus Connections

3.0 Functional Description (Continued)

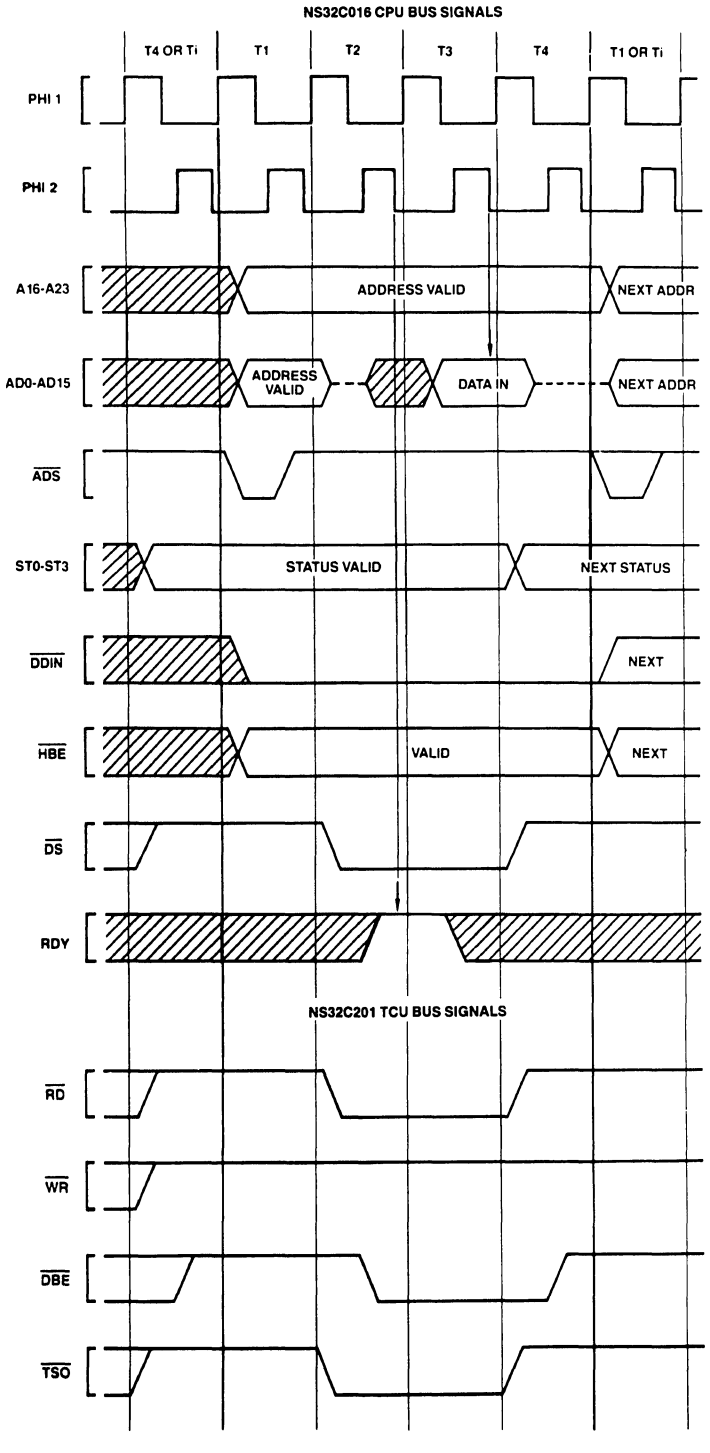

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FIGURE 3-7. Read Cycle Timing

3.0 Functional Description (Continued)

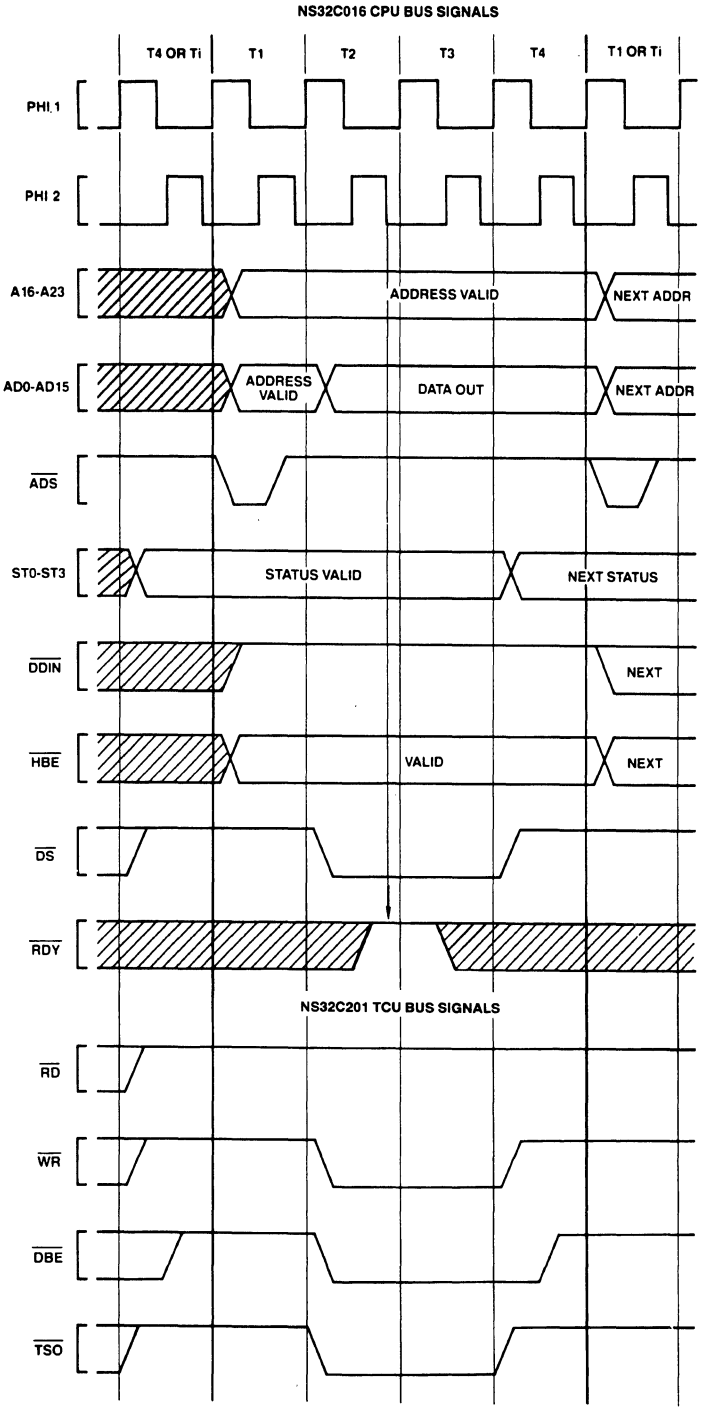

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FIGURE 3-8. Write Cycle Timing

3.0 Functional Description (Continued)

3.4.1 Cycle Extension

To allow sufficient strobe widths and access times for any speed of memory or peripheral device, the NS32C016 provides for extension of a bus cycle. Any type of bus cycle except a Slave Processor cycle can be extended.

In *Figures 3-7* and *3-8*, note that during T3 all bus control signals from the CPU and TCU are flat. Therefore, a bus cycle can be cleanly extended by causing the T3 state to be repeated. This is the purpose of the RDY (Ready) pin.

At the end of T2 on the falling edge of PHI2, the RDY line is sampled by the CPU. If RDY is high, the next T-states will be T3 and then T4, ending the bus cycle. If it is sampled low, then another T3 state will be inserted after the next T-state and the RDY line will again be sampled on the falling edge of PHI2. Each additional T3 state after the first is referred to as a "wait state." See *Figure 3-9*.

The RDY pin is driven by the NS32C201 Timing Control Unit, which applies WAIT States to the CPU as requested on three sets of pins:

1) $\overline{\text{CWAIT}}$ (Continues WAIT), which holds the CPU in WAIT states until removed.
2) $\overline{\text{WAIT1}}$, $\overline{\text{WAIT2}}$, $\overline{\text{WAIT4}}$, $\overline{\text{WAIT8}}$ (Collectively $\overline{\text{WAITn}}$), which may be given a four-bit binary value requesting a specific number of WAIT States from 0 to 15.
3) $\overline{\text{PER}}$ (Peripheral), which inserts five additional WAIT states and causes the TCU to reshape the $\overline{\text{RD}}$ and $\overline{\text{WR}}$ strobes. This provides the setup and hold times required by most MOS peripheral interface devices.

Combinations of these various WAIT requests are both legal and useful. For details of their use, see the NS32C201 TCU Data Sheet.

Figure 3-10 illustrates a typical Read cycle, with two WAIT states requested through the TCU $\overline{\text{WAITn}}$ pins.

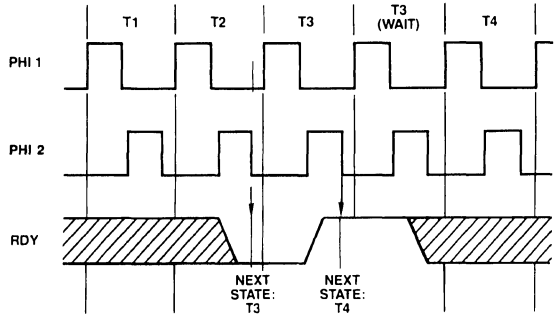

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FIGURE 3-9. RDY Pin Timing

3.4.2 Bus Status

The NS32C016 CPU presents four bits of Bus Status information on pins ST0–ST3. The various combinations on these pins indicate why the CPU is performing a bus cycle, or, if it is idle on the bus, then why it is idle.

Referring to *Figures 3-7* and *3-8*, note that Bus Status leads the corresponding Bus Cycle, going valid one clock cycle before T1, and changing to the next state at T4. This allows the system designer to fully decode the Bus Status and, if desired, latch the decoded signals before $\overline{\text{ADS}}$ initiates the Bus Cycle.

The Bus Status pins are interpreted as a four-bit value, with ST0 the least significant bit. Their values decode as follows:

0000 — The bus is idle because the CPU does not need to perform a bus access.

0001 — The bus is idle because the CPU is executing the WAIT instruction.

0010 — (Reserved for future use.)

0011 — The bus is idle because the CPU is waiting for a Slave Processor to complete an instruction.

0100 — Interrupt Acknowledge, Master.

The CPU is performing a Read cycle. To acknowledge receipt of a Non-Maskable Interrupt (on $\overline{\text{NMI}}$) it will read from address FFFF00_{16}, but will ignore any data provided.

To acknowledge receipt of a Maskable Interrupt (on $\overline{\text{INT}}$) it will read from address FFFE00_{16}, expecting a vector number to be provided from the Master NS32202 Interrupt Control Unit. If the vectoring mode selected by the last SETCFG instruction was Non-Vectored, then the CPU will ignore the value it has read and will use a default vector instead, having assumed that no NS32202 is present. See Section 3.4.5.

0101 — Interrupt Acknowledge, Cascaded.

The CPU is reading a vector number from a Cascaded NS32202 Interrupt Control Unit. The address provided is the address of the NS32202 Hardware Vector register. See Section 3.4.5.

0110 — End of Interrupt, Master.

The CPU is performing a Read cycle to indicate that it is executing a Return from Interrupt (RETI) instruction. See Section 3.4.5.

0111 — End of Interrupt, Cascaded.

The CPU is reading from a Cascaded Interrupt Control Unit to indicate that it is returning (through RETI) from an interrupt service routine requested by that unit. See Section 3.4.5.

1000 — Sequential Instruction Fetch.

The CPU is reading the next sequential word from the instruction stream into the Instruction Queue. It will do so whenever the bus would otherwise be idle and the queue is not already full.

3.0 Functional Description (Continued)

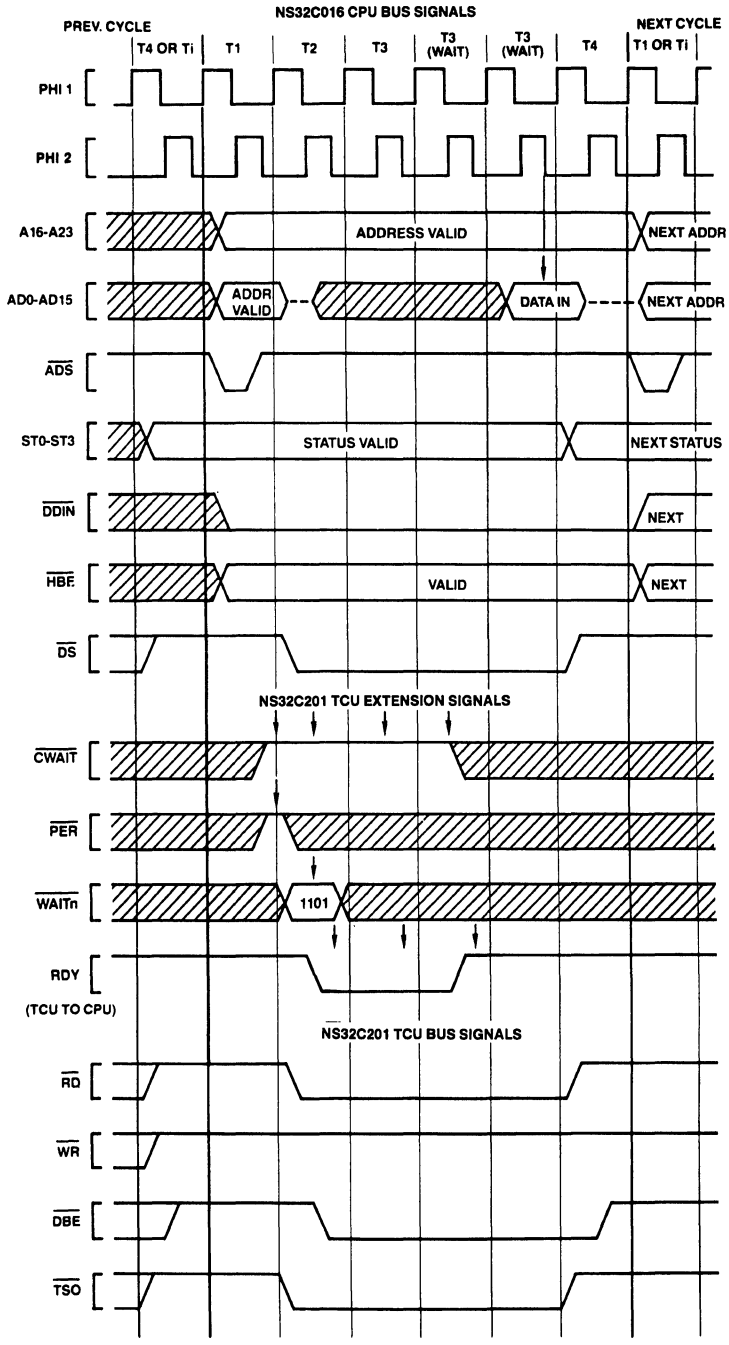

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FIGURE 3-10. Extended Cycle Example

Note: Arrows on $\overline{\text{CWAIT}}$, $\overline{\text{PER}}$, $\overline{\text{WAIT}}$n indicate points at which the TCU samples. Arrows on AD0–AD15 and RDY indicate points at which the CPU samples.

3.0 Functional Description (Continued)

1001 — Non-Sequential Instruction Fetch.
The CPU is performing the first fetch of instruction code after the Instruction Queue is purged. This will occur as a result of any jump or branch, or any interrupt or trap, or execution of certain instructions.

1010 — Data Transfer.
The CPU is reading or writing an operand of an instruction.

1011 — Read RMW Operand.
The CPU is reading an operand which will subsequently be modified and rewritten. If memory protection circuitry would not allow the following Write cycle, it must abort this cycle.

1100 — Read for Effective Address Calculation.
The CPU is reading information from memory in order to determine the Effective Address of an operand. This will occur whenever an instruction uses the Memory Relative or External addressing mode.

1101 — Transfer Slave Processor Operand.
The CPU is either transferring an instruction operand to or from a Slave Processor, or it is issuing the Operation Word of a Slave Processor instruction. See Section 3.9.1.

1110 — Read Slave Processor Status.
The CPU is reading a Status Word from a Slave Processor. This occurs after the Slave Processor has signalled completion of an instruction. The transferred word tells the CPU whether a trap should be taken, and in some instructions it presents new values for the CPU Processor Status Register bits N, Z, L or F. See Section 3.9.1.

1111 — Broadcast Slave ID.
The CPU is initiating the execution of a Slave Processor instruction. The ID Byte (first byte of the instruction) is sent to all Slave Processors, one of which will recognize it. From this point the CPU is communicating with only one Slave Processor. See Section 3.9.1.

3.4.3 Data Access Sequences

The 24-bit address provided by the NS32C016 is a byte address; that is, it uniquely identifies one of up to 16,777,216 eight-bit memory locations. An important feature of the NS32C016 is that the presence of a 16-bit data bus imposes no restrictions on data alignment; any data item, regardless of size, may be placed starting at any memory address. The NS32C016 provides a special control signal, High Byte Enable ($\overline{HBE}$), which facilitates individual byte addressing on a 16-bit bus.

Memory is organized as two eight-bit banks, each bank receiving the word address (A1–A23) in parallel. One bank, connected to Data Bus pins AD0–AD7, is enabled to respond to even byte addresses; i.e., when the least significant address bit (A0) is low. The other bank, connected to Data Bus pins AD8–AD15, is enabled when $\overline{HBE}$ is low. See *Figure 3-11.*

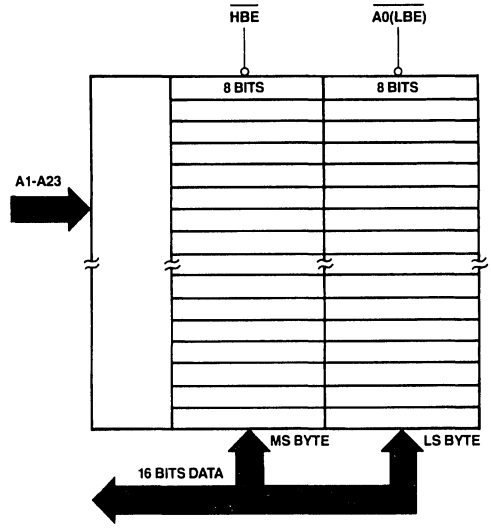

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FIGURE 3-11. Memory Interface

Any bus cycle falls into one of three categories: Even Byte Access, Odd Byte Access, and Even Word Access. All accesses to any data type are made up of sequences of these cycles. Table 3-1 gives the state of A0 and $\overline{HBE}$ for each category.

TABLE 3-1. Bus Cycle Categories

Category	$\overline{HBE}$	A0
Even Byte	1	0
Odd Byte	0	1
Even Word	0	0

Accesses of operands requiring more than one bus cycle are performed sequentially, with no idle T-States separating them. The number of bus cycles required to transfer an operand depends on its size and its alignment (i.e., whether it starts on an even byte address or an odd byte address). Table 3-2 lists the bus cycle performed for each situation. For the timing of A0 and $\overline{HBE}$, see Section 3.4.

3.0 Functional Description (Continued)

TABLE 3-2. Access Sequences

A. Odd Word Access Sequence

Cycle	Type	Address	$\overline{HBE}$	A0	High Bus	Low Bus
					BYTE 1	BYTE 0 ← A
1	Odd Byte	A	0	1	Byte 0	Don't Care
2	Even Byte	A+1	1	0	Don't Care	Byte 1

B. Even Double-Word Access Sequence

Cycle	Type	Address	BYTE 3	BYTE 2	BYTE 1	BYTE 0 ← A
1	Even Word	A	0	0	Byte 1	Byte 0
2	Even Word	A+2	0	0	Byte 3	Byte 2

C. Odd Double-Word Access Sequence

Cycle	Type	Address	BYTE 3	BYTE 2	BYTE 1	BYTE 0 ← A
1	Odd Byte	A	0	1	Byte 0	Don't Care
2	Even Word	A+1	0	0	Byte 2	Byte 1
3	Even Byte	A+3	1	0	Don't Care	Byte 3

D. Even Quad-Word Access Sequence

Cycle	Type	Address	BYTE 7	BYTE 6	BYTE 5	BYTE 4	BYTE 3	BYTE 2	BYTE 1	BYTE 0 ← A
1	Even Word	A					0	0	Byte 1	Byte 0
2	Even Word	A+2					0	0	Byte 3	Byte 2
Other bus cycles (instruction prefetch or slave) can occur here.										
3	Even Word	A+4					0	0	Byte 5	Byte 4
4	Even Word	A+6					0	0	Byte 7	Byte 6

E. Odd Quad-Word Access Sequence

Cycle	Type	Address	BYTE 7	BYTE 6	BYTE 5	BYTE 4	BYTE 3	BYTE 2	BYTE 1	BYTE 0 ← A
1	Odd Byte	A					0	1	Byte 0	Don't Care
2	Even Word	A+1					0	0	Byte 2	Byte 1
3	Even Byte	A+3					1	0	Don't Care	Byte 3
Other bus cycles (instruction prefetch or slave) can occur here.										
4	Odd Byte	A+4					0	1	Byte 4	Don't Care
5	Even Word	A+5					0	0	Byte 6	Byte 5
6	Even Byte	A+7					1	0	Don't Care	Byte 7

3.0 Functional Description (Continued)

3.4.3.1 Bit Accesses

The Bit Instructions perform byte accesses to the byte containing the designated bit. The Test and Set Bit instruction (SBIT), for example, reads a byte, alters it, and rewrites it, having changed the contents of one bit.

3.4.3.2 Bit Field Accesses

An access to a Bit Field in memory always generates a Double-Word transfer at the address containing the least significant bit of the field. The Double Word is read by an Extract instruction; an Insert instruction reads a Double Word, modifies it, and rewrites it.

3.4.3.3 Extending Multiply Accesses

The Extending Multiply Instruction (MEI) will return a result which is twice the size in bytes of the operand it reads. If the multiplicand is in memory, the most-significant half of the result is written first (at the higher address), then the least-significant half. This is done in order to support retry if this instruction is aborted.

3.4.4 Instruction Fetches

Instructions for the NS32C016 CPU are "prefetched"; that is, they are input before being needed into the next available entry of the eight-byte Instruction Queue. The CPU performs two types of Instruction Fetch cycles: Sequential and Non-Sequential. These can be distinguished from each other by their differing status combinations on pins ST0–ST3 (Section 3.4.2).

A Sequential Fetch will be performed by the CPU whenever the Data Bus would otherwise be idle and the Instruction Queue is not currently full. Sequential Fetches are always Even Word Read cycles (Table 3-1).

A Non-Sequential Fetch occurs as a result of any break in the normally sequential flow of a program. Any jump or branch instruction, a trap or an interrupt will cause the next Instruction Fetch cycle to be Non-Sequential. In addition, certain instructions flush the instruction queue, causing the next instruction fetch to display Non-Sequential status. Only the first bus cycle after a break displays Non-Sequential status, and that cycle is either an Even Word Read or an Odd Byte Read, depending on whether the destination address is even or odd.

3.4.5 Interrupt Control Cycles

Activating the $\overline{\text{INT}}$ or $\overline{\text{NMI}}$ pin on the CPU will initiate one or more bus cycles whose purpose is interrupt control rather than the transfer of instructions or data. Execution of the Return from Interrupt instruction (RETI) will also cause Interrupt Control bus cycles. These differ from instruction or data transfers only in the status presented on pins ST0–ST3. All Interrupt Control cycles are single-byte Read cycles.

This section describes only the Interrupt Control sequences associated with each interrupt and with the return from its service routine. For full details of the NS32C016 interrupt structure, see Section 3.8.

3.0 Functional Description (Continued)

TABLE 3-3. Interrupt Sequences

Cycle	Status	Address	$\overline{DDIN}$	$\overline{HBE}$	A0	High Bus	Low Bus
			A. Non-Maskable Interrupt Control Sequences.				
Interrupt Acknowledge							
1	0100	$FFFF00_{16}$	0	1	0	Don't Care	Don't Care
Interrupt Return							
None: Performed through Return from Trap (RETT) instruction.							
			B. Non-Vectored Interrupt Control Sequences.				
Interrupt Acknowledge							
1	0100	$FFFE00_{16}$	0	1	0	Don't Care	Don't Care
Interrupt Return							
None: Performed through Return from Trap (RETT) instruction.							
			C. Vectored Interrupt Sequences: Non-Cascaded.				
Interrupt Acknowledge							
1	0100	$FFFE00_{16}$	0	1	0	Don't Care	Vector: Range: 0–127
Interrupt Return							
1	0110	$FFFE00_{16}$	0	1	0	Don't Care	Vector: Same as in Previous Int. Ack. Cycle
			D. Vectored Interrupt Sequences: Cascaded.				
Interrupt Acknowledge							
1	0100	$FFFE00_{16}$	0	1	0	Don't Care	Cascade Index: range −16 to −1
(The CPU here uses the Cascade Index to find the Cascade Address.)							
2	0101	Cascade Address	0	1 or 0*	0 or 1*	Vector, range 0–255; on appropriate half of Data Bus for even/odd address	
Interrupt Return							
1	0110	$FFFE00_{16}$	0	1	0	Don't Care	Cascade Index: same as in previous Int. Ack. Cycle
(The CPU here uses the Cascade Index to find the Cascade Address.)							
2	0111	Cascade Address	0	1 or 0*	0 or 1*	Don't Care	Don't Care

* If the Cascaded ICU Address is Even (A0 is low), then the CPU applies $\overline{HBE}$ high and reads the vector number from bits 0–7 of the Data Bus.
If the address is Odd (A0 is high), then the CPU applies $\overline{HBE}$ low and reads the vector number from bits 8–15 of the Data Bus. The vector number may be in the range 0–255.

3.0 Functional Description (Continued)

3.4.6 Slave Processor Communication

In addition to its use as the Address Translation strap (Section 3.5.1), the $\overline{AT}/\overline{SPC}$ pin is used as the data strobe for Slave Processor transfers. In this role, it is referred to as Slave Processor Control ($\overline{SPC}$). In a Slave Processor bus cycle, data is transferred on the Data Bus (AD0–AD15), and the status lines ST0–ST3 are monitored by each Slave Processor in order to determine the type of transfer being performed. $\overline{SPC}$ is bidirectional, but is driven by the CPU during all Slave Processor bus cycles. See Section 3.9 for full protocol sequences.

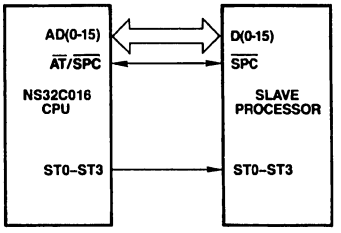

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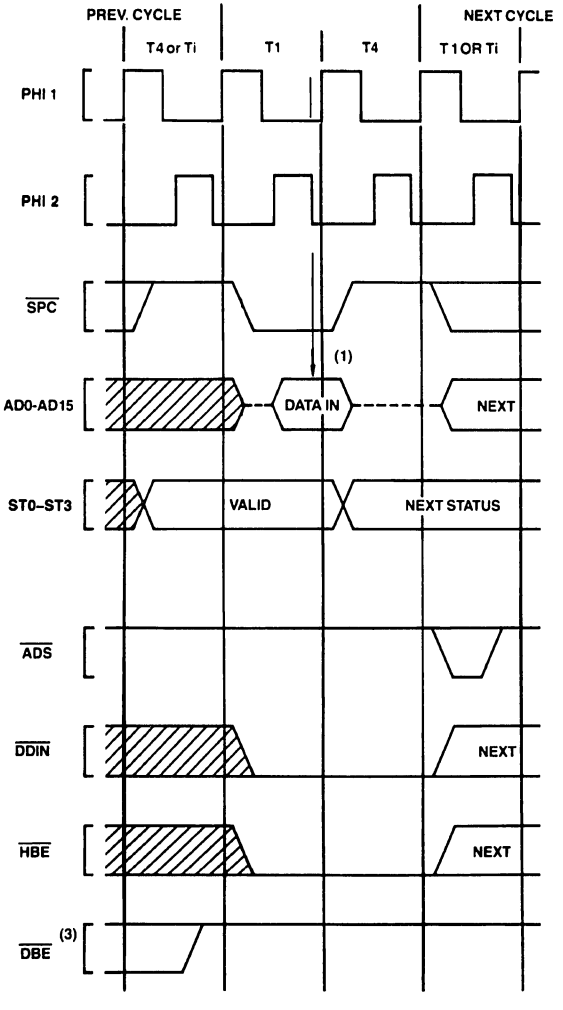
FIGURE 3-12. Slave Processor Connections



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Notes:

(1) CPU samples Data Bus here.

(2) $\overline{DBE}$ and all other NS32C201 TCU bus signals remain inactive because no $\overline{ADS}$ pulse is received from the CPU.

FIGURE 3-13. CPU Read from Slave Processor

3.0 Functional Description (Continued)

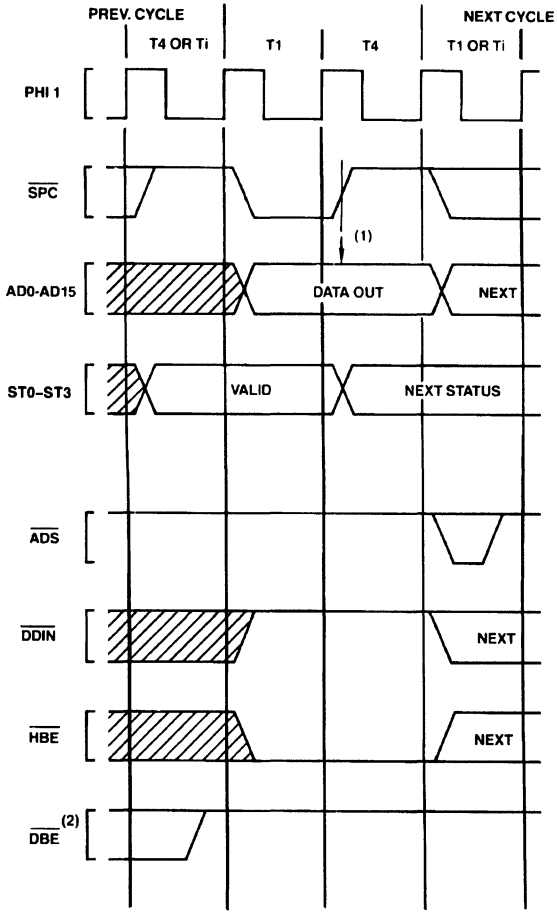
3.4.6.1 Slave Processor Bus Cycles

A Slave Processor bus cycle always takes exactly two clock cycles, labeled T1 and T4 (see *Figures 3-13* and *3-14*). During a Read cycle $\overline{SPC}$ is active from the beginning of T1 to the beginning of T4, and the data is sampled at the end of T1. The Cycle Status pins lead the cycle by one clock period, and are sampled at the leading edge of $\overline{SPC}$. During a Write cycle, the CPU applies data and activates $\overline{SPC}$ at T1, removing $\overline{SPC}$ at T4. The Slave Processor latches status on the leading edge of $\overline{SPC}$ and latches data on the trailing edge.

Since the CPU does not pulse the Address Strobe ($\overline{ADS}$), no bus signals are generated by the NS32C201 Timing Control Unit. The direction of a transfer is determined by the sequence ("protocol") established by the instruction under execution; but the CPU indicates the direction on the $\overline{DDIN}$ pin for hardware debugging purposes.

3.4.6.2 Slave Operand Transfer Sequences

A Slave Processor operand is transferred in one or more Slave bus cycles. A Byte operand is transferred on the least-significant byte of the Data Bus (AD0–AD7), and a Word operand is transferred on the entire bus. A Double Word is transferred in a consecutive pair of bus cycles, least-significant word first. A Quad Word is transferred in two pairs of Slave cycles, with other bus cycles possibly occurring between them. The word order is from least-significant word to most-significant.



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Notes:

(1) Slave Processor samples Data Bus here.

(2) $\overline{DBE}$, being provided by the NS32C201 TCU, remains inactive due to the fact that no pulse is presented on $\overline{ADS}$. $\overline{TCU}$ signals $\overline{RD}$, $\overline{WR}$ and $\overline{TSO}$ also remain inactive.

FIGURE 3-14. CPU Write to Slave Processor

3.0 Functional Description (Continued)

3.5 MEMORY MANAGEMENT OPTION

The NS32C016 CPU, in conjunction with the NS32082 Memory Management Unit (MMU), provides full support for address translation, memory protection, and memory allocation techniques up to and including Virtual Memory.

3.5.1 Address Translation Strap

The Bus Interface Control section of the NS32C016 CPU has two bus timing modes: With or Without Address Translation. The mode of operation is selected by the CPU by sampling the $\overline{AT}/\overline{SPC}$ (Address Translation/Slave Processor Control) pin on the rising edge of the $\overline{RST}$ (Reset) pulse. If $\overline{AT}/\overline{SPC}$ is sampled as high, the bus timing is as previously described in Section 3.4. If it is sampled as low, two changes occur:

1) An extra clock cycle, Tmmu, is inserted into all bus cycles except Slave Processor transfers.
2) The $\overline{DS}/\overline{FLT}$ pin changes in function from a Data Strobe output ($\overline{DS}$) to a Float Command input ($\overline{FLT}$).

The NS32082 MMU will itself pull the CPU $\overline{AT}/\overline{SPC}$ pin low when it is reset. In non-Memory-Managed systems this pin should be pulled up to V_{CC} through a 10 kΩ resistor.

Note that the Address Translation strap does not specifically declare the presence of an NS32082 MMU, but only the

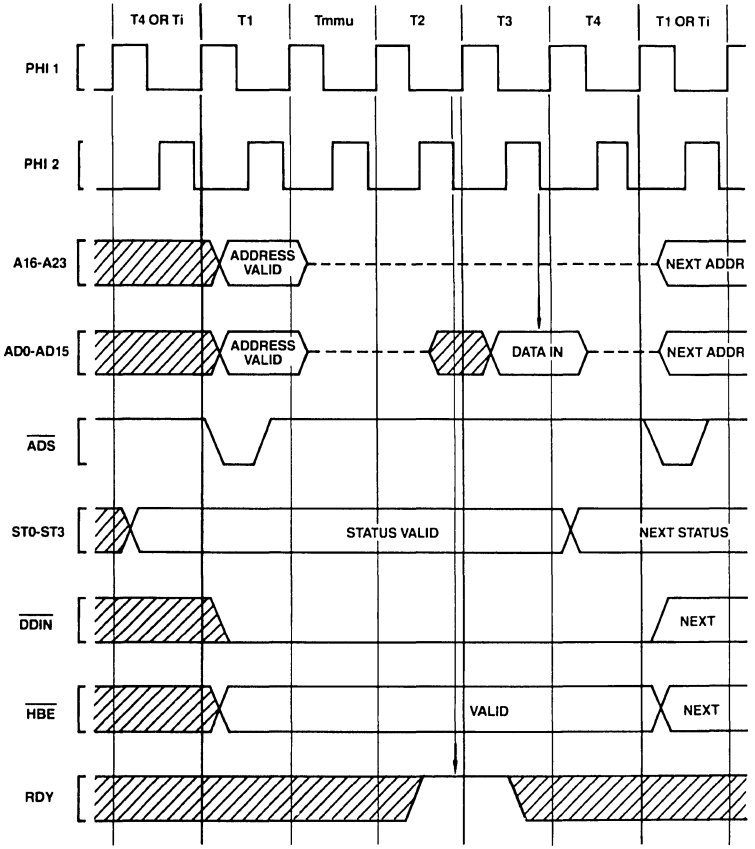

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FIGURE 3-15. Read Cycle with Address Translation (CPU Action)

3.0 Functional Description (Continued)

presence of external address translation circuitry. MMU instructions will still trap as being undefined unless the SETCFG (Set Configuration) instruction is executed to declare the MMU instruction set valid. See Section 2.1.3.

3.5.2 Translated Bus Timing

Figures 3-15 and *3-16* illustrate the CPU activity during a Read cycle and a Write cycle in Address Translation mode. The additional T-State, Tmmu, is inserted between T1 and T2. During this time the CPU places AD0–AD15 and A16–A23 into the TRI-STATE® mode, allowing the MMU to assert the translated address and issue the physical address strobe $\overline{PAV}$. T2 through T4 of the cycle are identical to their counter-parts without Address Translation, with the exception that the CPU Address lines A16–A23 remain in the TRI-STATE condition. This allows the MMU to continue asserting the translated address on those pins.

Note that in order for the NS32082 MMU to operate correctly, it must be set to the 32C016 mode by forcing A24 high during reset.

Figures 3-17 and *3-18* show a Read cycle and a Write cycle as generated by the 32C016/32082/32C201 group. Note that with the CPU $\overline{ADS}$ signal going only to the MMU, and with the MMU $\overline{PAV}$ signal substituting for $\overline{ADS}$ everywhere else, Tmmu through T4 look exactly like T1 through T4 in a non-Memory-Managed system. For the connection diagram, see Appendix B.

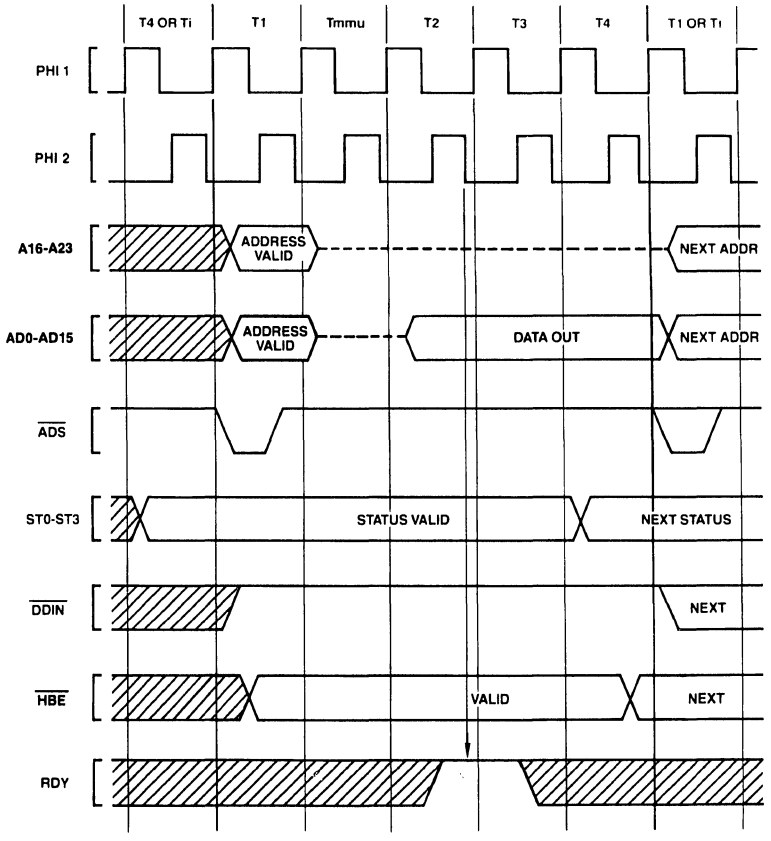

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FIGURE 3-16. Write Cycle with Address Translation (CPU Action)

3.0 Functional Description (Continued)

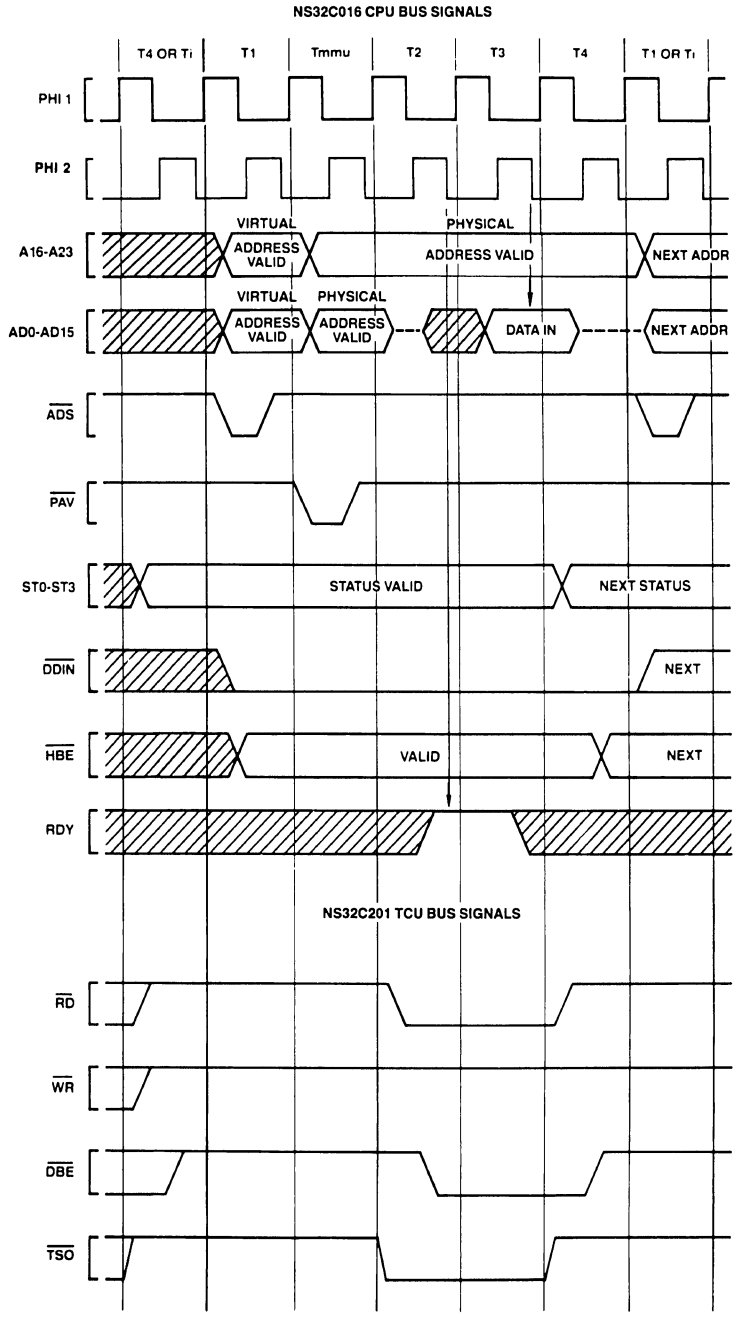

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FIGURE 3-17. Memory-Managed Read Cycle

3.0 Functional Description (Continued)

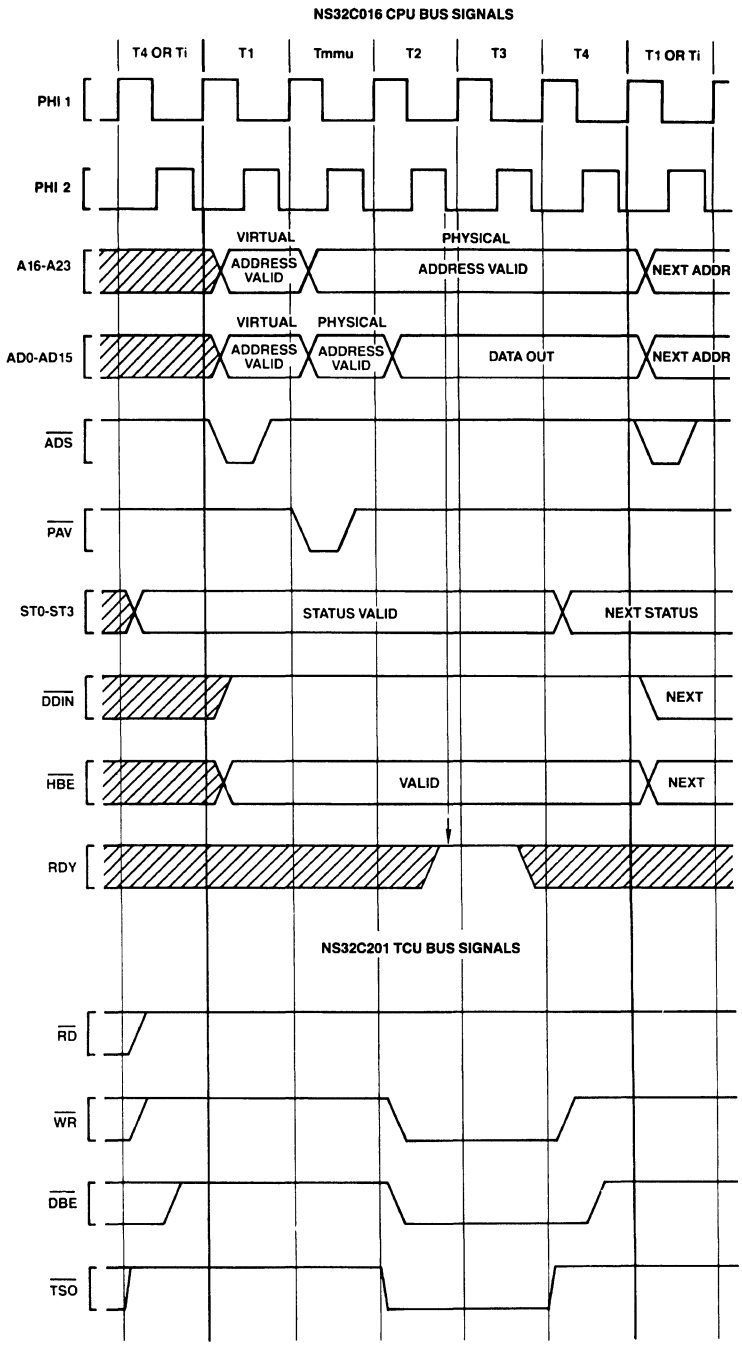

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FIGURE 3-18. Memory-Managed Write Cycle

3.0 Functional Description (Continued)

3.5.3 The $\overline{FLT}$ (Float) Pin

The $\overline{FLT}$ pin is used by the CPU for address translation support. Activating $\overline{FLT}$ during Tmmu causes the CPU to wait longer than Tmmu for address translation and validation. This feature is used occasionally by the NS32082 MMU in order to update its internal translation Look-Aside Buffer (TLB) from page tables in memory, or to update certain status bits within them.

Figure 3-19 shows the effects of $\overline{FLT}$. Upon sampling $\overline{FLT}$ low, late in Tmmu, the CPU enters idle T-States (Tf) during which it:

1) Sets AD0–AD15, A16–A23 and $\overline{DDIN}$ to the TRI-STATE condition ("floating").
2) Sets $\overline{HBE}$ low.
3) Suspends further internal processing of the current instruction. This ensures that the current instruction remains abortable with retry. (See $\overline{RST}$/$\overline{ABT}$ description, Section 3.5.4.)

Note that the AD0–AD15 pins may be briefly asserted during the first idle T-State. The above conditions remain in effect until $\overline{FLT}$ again goes high. See the Timing Specifications, Section 4.

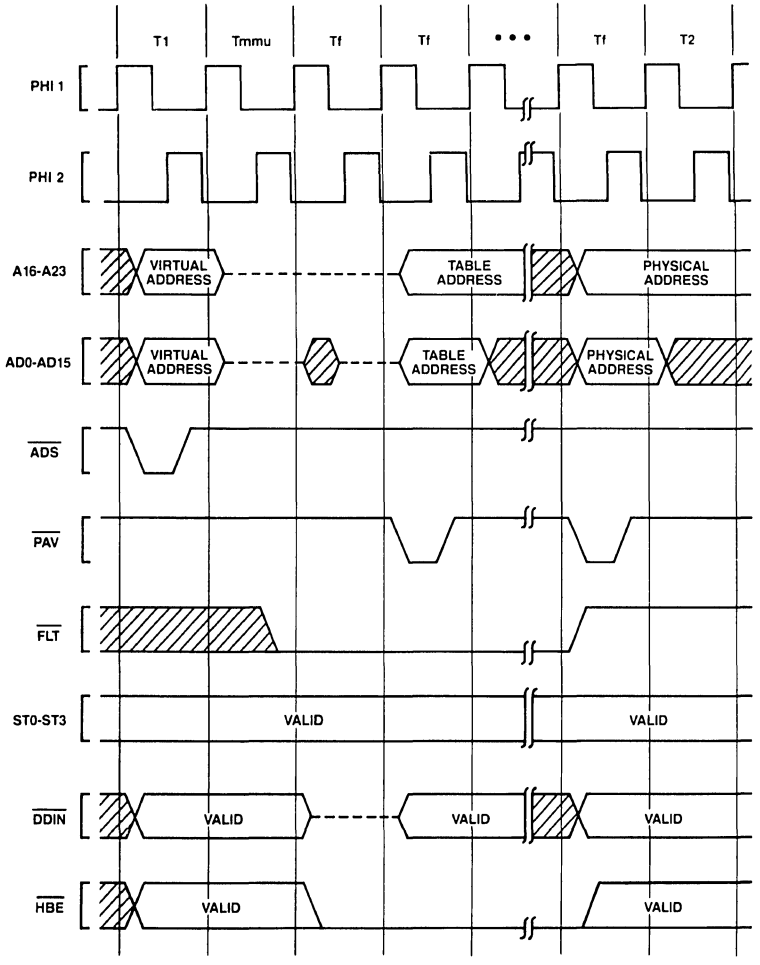

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FIGURE 3-19. $\overline{FLT}$ Timing

3.0 Functional Description (Continued)

3.5.4 Aborting Bus Cycles

The $\overline{RST}/\overline{ABT}$ pin, apart from its Reset function (Section 3.3), also serves as the means to "abort," or cancel, a bus cycle and the instruction, if any, which initiated it. An Abort request is distinguished from a Reset in that the $\overline{RST}/\overline{ABT}$ pin is held active for only one clock cycle.

If $\overline{RST}/\overline{ABT}$ is pulled low during Tmmu or Tf, this signals that the cycle must be aborted. The CPU itself will enter T2 and then Ti, thereby terminating the cycle. Since it is the MMU $\overline{PAV}$ signal which triggers a physical cycle, the rest of the system remains unaware that a cycle was started.

The NS32082 MMU will abort a bus cycle for either of two reasons:

1) The CPU is attempting to access a virtual address which is not currently resident in physical memory. The reference page must be brought into physical memory from mass storage to make it accessible to the CPU.
2) The CPU is attempting to perform an access which is not allowed by the protection level assigned to that page.

When a bus cycle is aborted by the MMU, the instruction that caused it to occur is also aborted in such a manner that it is guaranteed re-executable later. The information that is changed irrecoverably by such a partly-executed instruction does not affect its re-execution.

3.5.4.1 The Abort Interrupt

Upon aborting an instruction, the CPU immediately performs an interrupt through the ABT vector in the Interrupt Table (see Section 3.8). The Return Address pushed on the Interrupt Stack is the address of the aborted instruction, so that a Return from Trap (RETT) instruction will automatically retry it.

The one exception to this sequence occurs if the aborted bus cycle was an instruction prefetch. If so, it is not yet certain that the aborted prefetched code is to be executed. Instead of causing an interrupt, the CPU only aborts the bus cycle, and stops prefetching. If the information in the Instruction Queue runs out, meaning that the instruction will actually be executed, the ABT interrupt will occur, in effect aborting the instruction that was being fetched.

3.5.4.2 Hardware Considerations

In order to guarantee instruction retry, certain rules must be followed in applying an Abort to the CPU. These rules are followed by the NS32082 Memory Management Unit.

1) If $\overline{FLT}$ has not been applied to the CPU, the Abort pulse must occur during or before Tmmu. See the Timing Specifications, *Figure 4-23.*
2) If $\overline{FLT}$ has been applied to the CPU, the Abort pulse must be applied before the T-State in which $\overline{FLT}$ goes inactive. The CPU will not actually respond to the Abort command until $\overline{FLT}$ is removed. See *Figure 4-24.*
3) The Write half of a Read-Modify-Write operand access may not be aborted. The CPU guarantees that this will never be necessary for Memory Management funtions by applying a special RMW status (Status Code 1011) during the Read half of the access. When the CPU presents RMW status, that cycle must be aborted if it would be illegal to write to any of the accessed addresses.

If $\overline{RST}/\overline{ABT}$ is pulsed at any time other than as indicated above, it will abort either the instruction currently under execution or the next instruction and will act as a very high-priority interrupt. However, the program that was running at the time is not guaranteed recoverable.

3.6 BUS ACCESS CONTROL

The NS32C016 CPU has the capability of relinquishing its access to the bus upon request from a DMA device or another CPU. This capability is implemented on the $\overline{HOLD}$ (Hold Request) and $\overline{HLDA}$ (Hold Acknowledge) pins. By asserting $\overline{HOLD}$ low, an external device requests access to the bus. On receipt of $\overline{HLDA}$ from the CPU, the device may perform bus cycles, as the CPU at this point has set the AD0–AD15, A16–A23, $\overline{ADS}$, $\overline{DDIN}$ and $\overline{HBE}$ pins to the TRI-STATE condition. To return control of the bus to the CPU, the device sets $\overline{HOLD}$ inactive, and the CPU acknowledges return of the bus by setting $\overline{HLDA}$ inactive.

How quickly the CPU releases the bus depends on whether it is idle on the bus at the time the $\overline{HOLD}$ request is made, as the CPU must always complete the current bus cycle. *Figure 3-20* shows the timing sequence when the CPU is idle. In this case, the CPU grants the bus during the immediately following clock cycle. *Figure 3-21* shows the sequence if the CPU is using the bus at the time that the $\overline{HOLD}$ request is made. If the request is made during or before the clock cycle shown (two clock cycles before T4), the CPU will release the bus during the clock cycle following T4. If the request occurs closer to T4, the CPU may already have decided to initiate another bus cycle. In that case it will not grant the bus until after the next T4 state. Note that this situation will also occur if the CPU is idle on the bus but has initiated a bus cycle internally.

In a Memory-Managed system, the $\overline{HLDA}$ signal is connected in a daisy-chain through the NS32082, so that the MMU can release the bus if it is using it.

3.0 Functional Description (Continued)

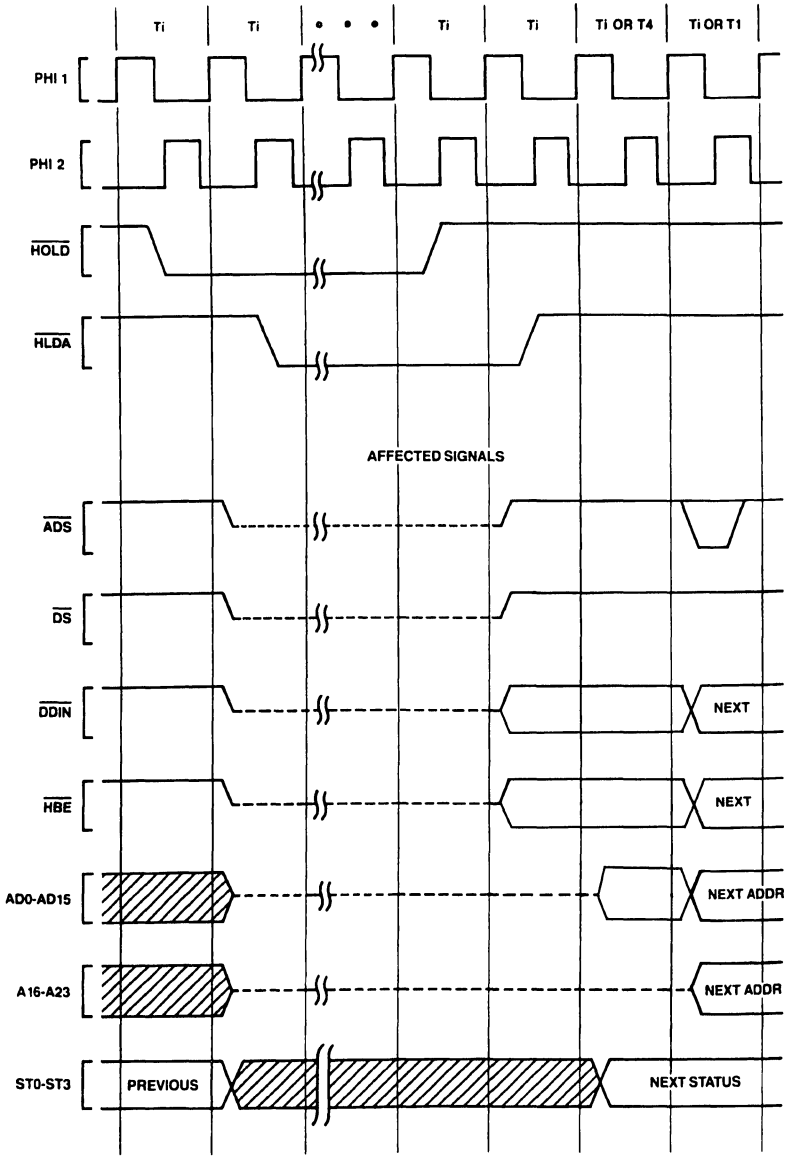

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FIGURE 3-20. HOLD Timing, Bus Initially Idle

3.0 Functional Description (Continued)

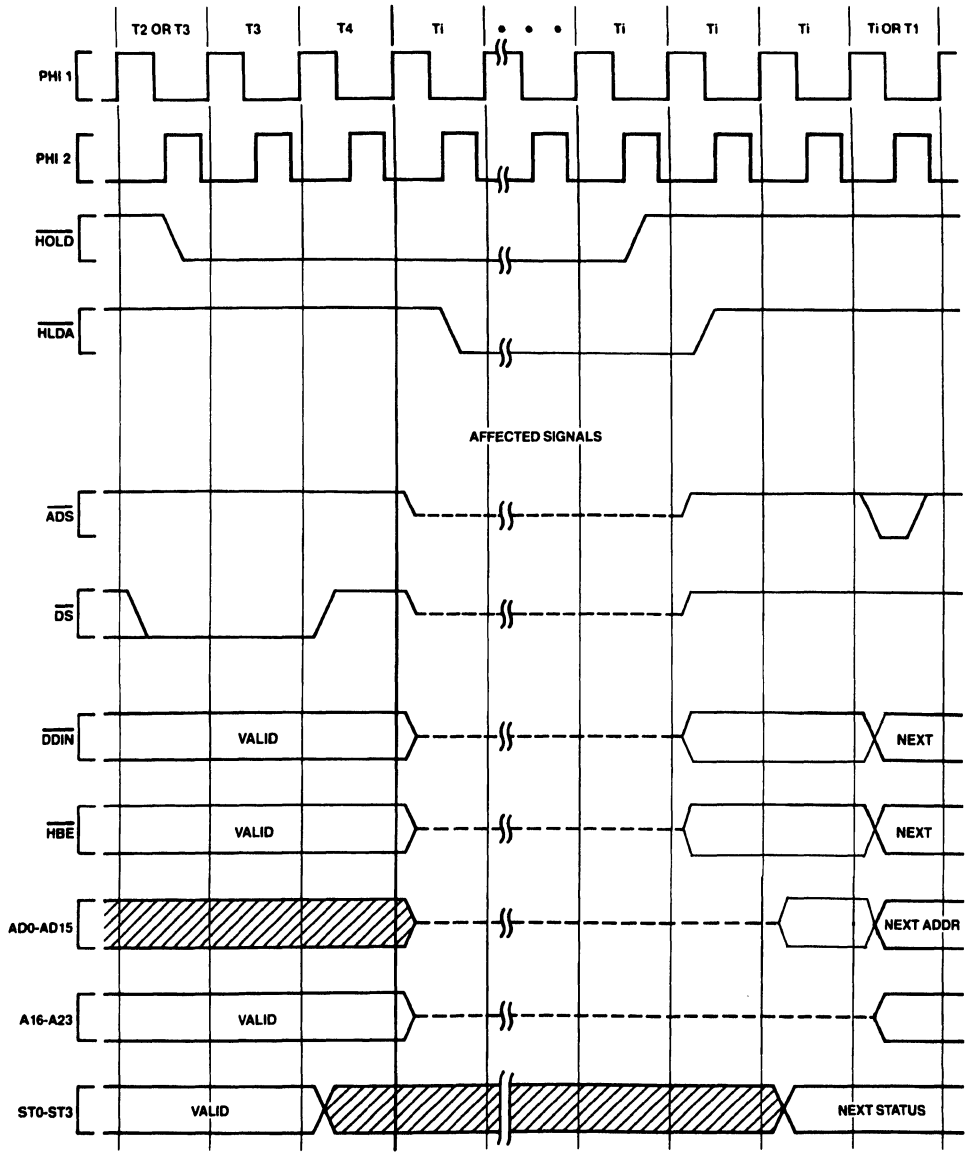

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FIGURE 3-21. HOLD Timing, Bus Initially Not Idle

3.0 Functional Description (Continued)

3.7 INSTRUCTION STATUS

In addition to the four bits of Bus Cycle status (ST0–ST3), the NS32C016 CPU also presents Instruction Status information on three separate pins. These pins differ from ST0–ST3 in that they are synchronous to the CPU's internal instruction execution section rather than to its bus interface section.

$\overline{PFS}$ (Program Flow Status) is pulsed low as each instruction begins execution. It is intended for debugging purposes, and is used that way by the NS32082 Memory Management Unit.

U/$\overline{S}$ originates from the U bit of the Processor Status Register, and indicates whether the CPU is currently running in User or Supervisor mode. It is sampled by the MMU for mapping, protection and debugging purposes. Although it is not synchronous to bus cycles, there are guarantees on its validity during any given bus cycle. See the Timing Specifications, *Figure 4-22.*

$\overline{ILO}$ (Interlocked Operation) is activated during an SBITI (Set Bit, Interlocked) or CBITI (Clear Bit, Interlocked) instruction. It is made available to external bus arbitration circuitry in order to allow these instructions to implement the semaphore primitive operations for multi-processor communication and resource sharing. As with the U/$\overline{S}$ pin, there are guarantees on its validity during the operand accesses performed by the instructions. See the Timing Specification Section, *Figure 4-20.*

3.8 NS32C016 INTERRUPT STRUCTURE

$\overline{INT}$, on which maskable interrupts may be requested,

$\overline{NMI}$, on which non-maskable interrupts may be requested, and

$\overline{RST}$/$\overline{ABT}$, which may be used to abort a bus cycle and any associated instruction. See Section 3.5.4.

In addition, there is a set of internally-generated "traps" which cause interrupt service to be performed as a result either of exceptional conditions (e.g., attempted division by zero) or of specific instructions whose purpose is to cause a trap to occur (e.g., the Supervisor Call instruction).

3.8.1 General Interrupt/Trap Sequence

Upon receipt of an interrupt or trap request, the CPU goes through three major steps:

1) Adjustment of Registers.

   Depending on the source of the interrupt or trap, the CPU may restore and/or adjust the contents of the Program Counter (PC), the Processor Status Register (PSR) and the currently-selected Stack Pointer (SP). A copy of the PSR is made, and the PSR is then set to reflect Supervisor Mode and selection of the Interrupt Stack.

2) Vector Acquisition.

   A Vector is either obtained from the Data Bus or is supplied by default.

3) Service Call.

   The Vector is used as an index into the Interrupt Dispatch Table, whose base address is taken from the CPU Interrupt Base (INTBASE) Register. See *Figure 3-22.* A 32-bit External Procedure Descriptor is read from the table entry, and an External Procedure Call is performed using it. The MOD Register (16 bits) and Program Counter (32 bits) are pushed on the Interrupt Stack.

This process is illustrated in *Figure 3-23,* from the viewpoint of the programmer.

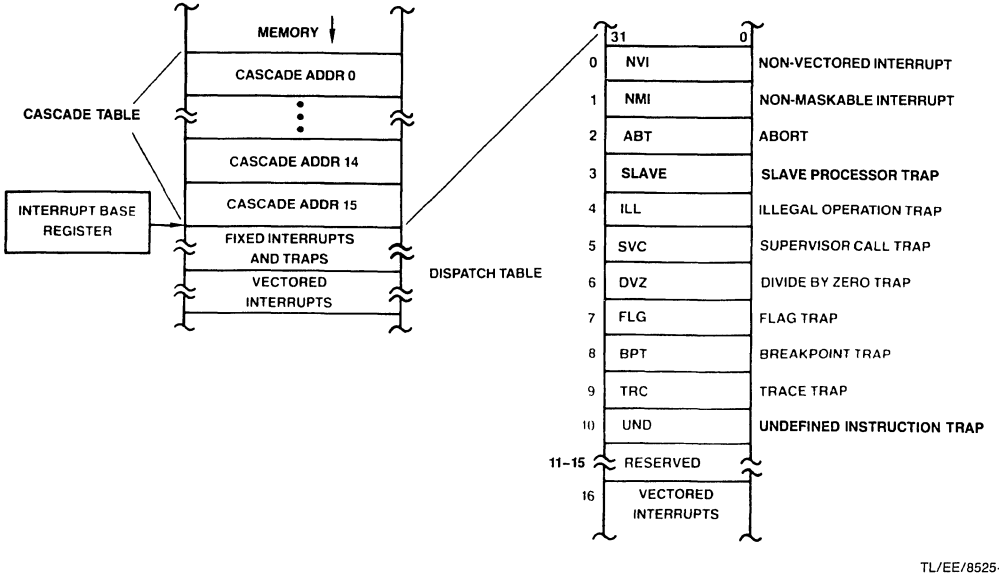

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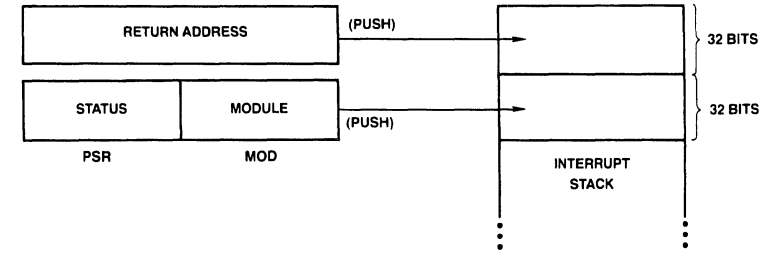
FIGURE 3-22. Interrupt Dispatch and Cascade Tables

3.0 Functional Description (Continued)



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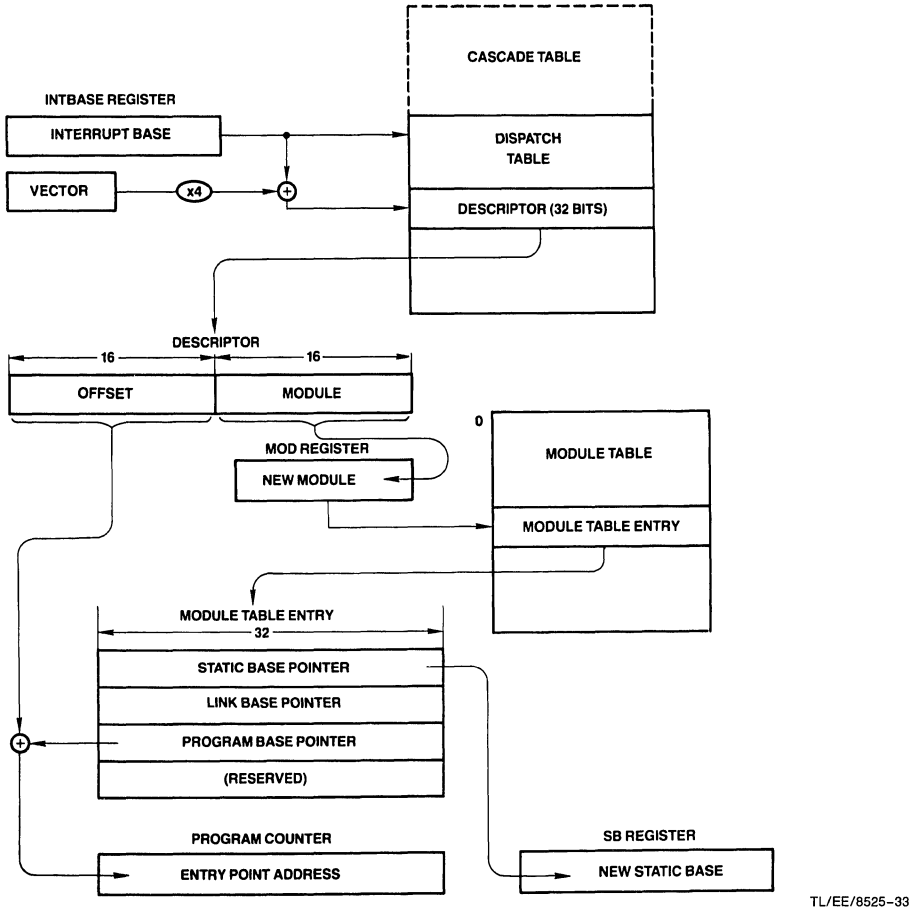

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FIGURE 3-23. Interrupt/Trap Service Routine Calling Sequence

3.0 Functional Description (Continued)

3.8.2 Interrupt/Trap Return

To return control to an interrupted program, one of two instructions is used. The RETT (Return from Trap) instruction (*Figure 3-24*) restores the PSR, MOD, PC and SB registers to their previous contents and, since traps are often used deliberately as a call mechanism for Supervisor Mode procedures, it also discards a specified number of bytes from the original stack as surplus parameter space. RETT is used to return from any trap or interrupt except the Maskable Interrupt. For this, the RETI (Return from Interrupt) instruction is used, which also informs any external Interrupt Control Units that interrupt service has completed. Since interrupts are generally asynchronous external events, RETI does not pop parameters. See *Figure 3-25*.

3.8.3 Maskable Interrupts (The $\overline{\text{INT}}$ Pin)

The $\overline{\text{INT}}$ pin is a level-sensitive input. A continuous low level is allowed for generating multiple interrupt requests. The input is maskable, and is therefore enabled to generate interrupt requests only while the Processor Status Register I bit is set. The I bit is automatically cleared during service of an $\overline{\text{INT}}$, $\overline{\text{NMI}}$ or Abort request, and is restored to its original setting upon return from the interrupt service routine via the RETT or RETI instruction.

The $\overline{\text{INT}}$ pin may be configured via the SETCFG instruction as either Non-Vectored (CFG Register bit I = 0) or Vectored (bit I = 1).

3.8.3.1 Non-Vectored Mode

In the Non-Vectored mode, an interrupt request on the $\overline{\text{INT}}$ pin will cause an Interrupt Acknowledge bus cycle, but the CPU will ignore any value read from the bus and use instead a default vector of zero. This mode is useful for small systems in which hardware interrupt prioritization is unnecessary.

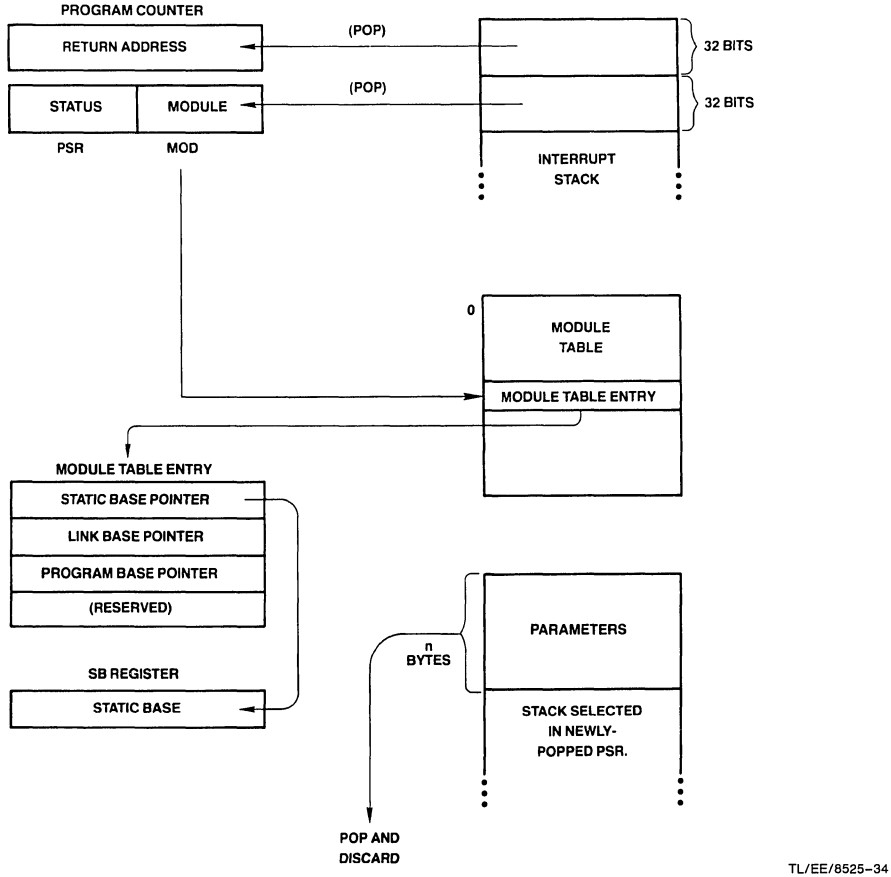

FIGURE 3-24. Return from Trap (RETT n) Instruction Flow

3.0 Functional Description (Continued)

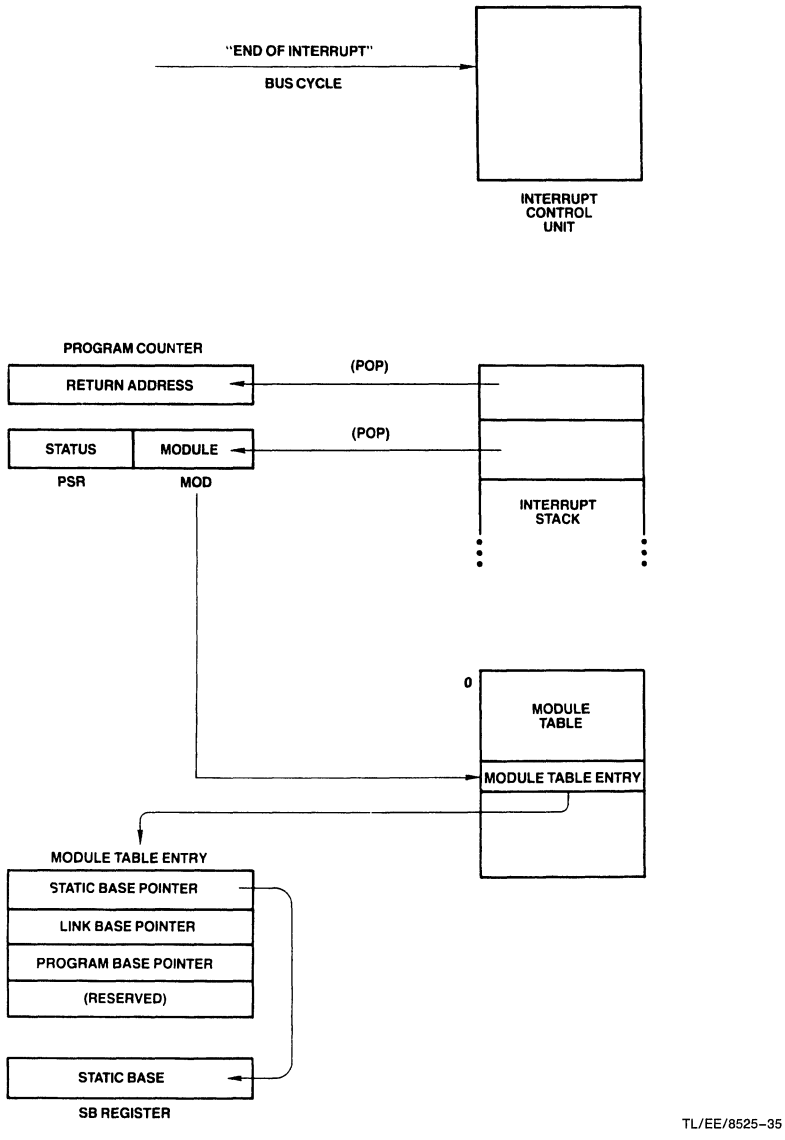

FIGURE 3-25. Return from Interrupt (RET I) Instruction Flow

3.0 Functional Description (Continued)

3.8.3.2 Vectored Mode: Non-Cascaded Case

In the Vectored mode, the CPU uses an Interrupt Control Unit (ICU) to prioritize up to 16 interrupt requests. Upon receipt of an interrupt request on the $\overline{INT}$ pin, the CPU performs an "Interrupt Acknowledge, Master" bus cycle (Section 3.4.2) reading a vector value from the low-order byte of the Data Bus. This vector is then used as an index into the Dispatch Table in order to find the External Procedure Descriptor for the proper interrupt service procedure. The service procedure eventually returns via the Return from Interrupt (RETI) instruction, which performs an End of Interrupt bus cycle, informing the ICU that it may re-prioritize any interrupt requests still pending. The ICU provides the vector number again, which the CPU uses to determine whether it needs also to inform a Cascaded ICU (see below).

In a system with only one ICU (16 levels of interrupt), the vectors provided must be in the range of 0 through 127; that is, they must be positive numbers in eight bits. By providing a negative vector number, an ICU flags the interrupt source as being a Cascaded ICU (see below).

3.8.3.3 Vectored Mode: Cascaded Case

In order to allow up to 256 levels of interrupt, provision is made both in the CPU and in the NS32202 Interrupt Control Unit (ICU) to transparently support cascading. *Figure 3-27* shows a typical cascaded configuration. Note that the Interrupt output from a Cascaded ICU goes to an Interrupt Request input of the Master ICU, which is the only ICU which drives the CPU $\overline{INT}$ pin.

In a system which uses cascading, two tasks must be performed upon initialization:

1) For each Cascaded ICU in the system, the Master ICU must be informed of the line number (0 to 15) on which it receives the cascaded requests.
2) A Cascade Table must be established in memory. The Cascade Table is located in a NEGATIVE direction from the location indicated by the CPU Interrupt Base (INTBASE) Register. Its entries are 32-bit addresses, pointing to the Vector Registers of each of up to 16 Cascaded ICUs.

Figure 3-22 illustrates the position of the Cascade Table. To find the Cascade Table entry for a Cascaded ICU, take its Master ICU line number (0 to 15) and subtract 16 from it, giving an index in the range −16 to −1. Multiply this value by 4, and add the resulting negative number to the contents of the INTBASE Register. The 32-bit entry at this address must be set to the address of the Hardware Vector Register of the Cascaded ICU. This is referred to as the "Cascade Address."

Upon receipt of an interrupt request from a Cascaded ICU, the Master ICU interrupts the CPU and provides the negative Cascade Table index instead of a (positive) vector number. The CPU, seeing the negative value, uses it as an index into the Cascade Table and reads the Cascade Address from the referenced entry. Applying this address, the CPU performs an "Interrupt Acknowledge, Cascaded" bus cycle (Section 3.4.2), reading the final vector value. This vector is interpreted by the CPU as an unsigned byte, and can therefore be in the range of 0 through 255.

In returning from a Cascaded interrupt, the service procedure executes the Return from Interrupt (RETI) instruction, as it would for any Maskable Interrupt. The CPU performs an "End of Interrupt, Master" bus cycle (Section 3.4.2), whereupon the Master ICU again provides the negative Cascaded Table index. The CPU, seeing a negative value, uses it to find the corresponding Cascade Address from the Cascade Table. Applying this address, it performs an "End of Interrupt, Cascaded" bus cycle (Section 3.4.2), informing the Cascaded ICU of the completion of the service routine. The byte read from the Cascaded ICU is discarded.

Note: If an interrupt must be masked off, the CPU can do so by setting the corresponding bit in the Interrupt Mask Register of the Interrupt Controller. However, if an interrupt is set pending during the CPU instruction that masks off that interrupt, the CPU may still perform an interrupt acknowledge cycle following that instruction since it might have sampled the $\overline{INT}$ line before the ICU deasserted it. This could cause the ICU to provide an invalid vector. To avoid this problem the above operation should be performed with the CPU interrupt disabled.

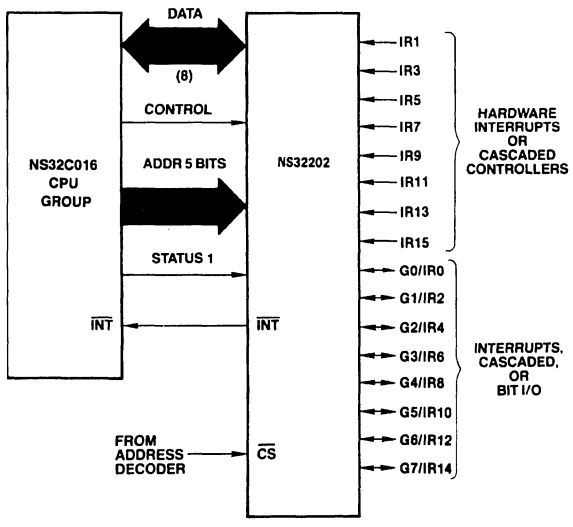

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FIGURE 3-26. Interrupt Control Unit Connections (16 Levels)

3.0 Functional Description (Continued)

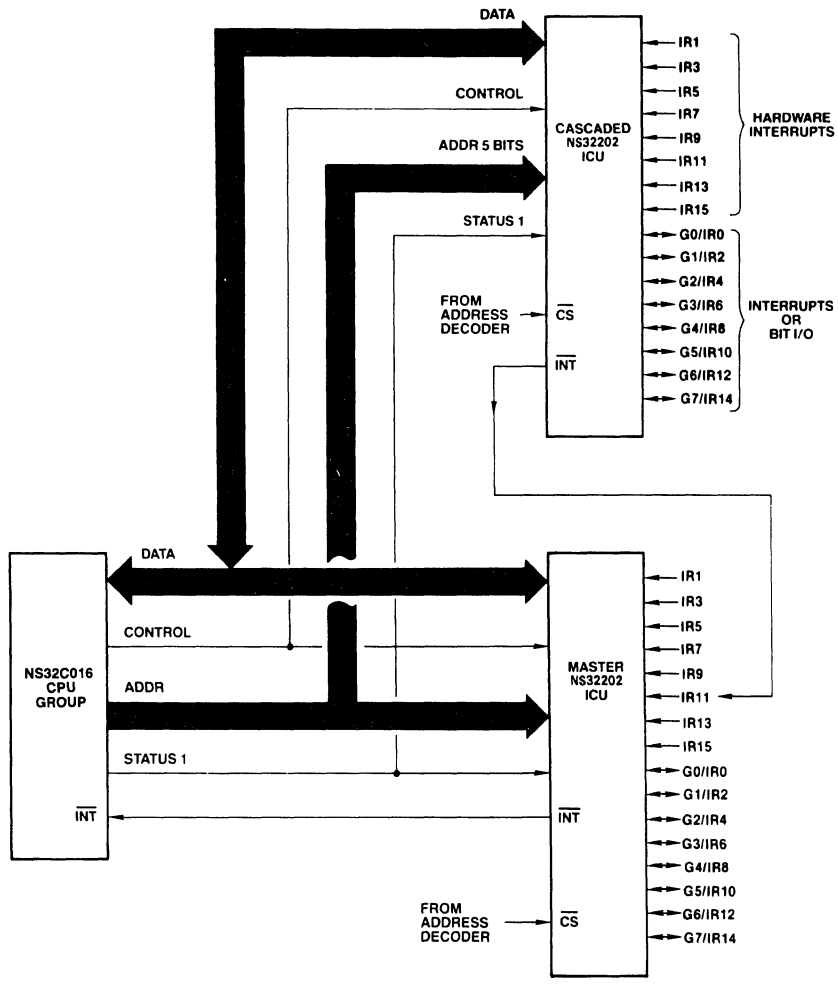

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FIGURE 3-27. Cascaded Interrupt Control Unit Connections

3.8.4 Non-Maskable Interrupt (The $\overline{\text{NMI}}$ Pin)

The Non-Maskable Interrupt is triggered whenever a falling edge is detected on the $\overline{\text{NMI}}$ pin. The CPU performs an "Interrupt Acknowledge, Master" bus cycle (Section 3.4.2) when processing of this interrupt actually begins. The Interrupt Acknowledge cycle differs from that provided for Maskable Interrupts in that the address presented is FFFF00_{16}. The vector value used for the Non-Maskable Interrupt is taken as 1, regardless of the value read from the bus.

The service procedure returns from the Non-Maskable Interrupt using the Return from Trap (RETT) instruction. No special bus cycles occur on return.

For the full sequence of events in processing the Non-Maskable Interrupt, see Section 3.8.7.1.

3.8.5 Traps

A trap is an internally-generated interrupt request caused as a direct and immediate result of the execution of an instruction. The Return Address pushed by any trap except Trap (TRC) below is the address of the first byte of the instruction during which the trap occurred. Traps do not disable interrupts, as they are not associated with external events. Traps recognized by NS32C016 CPU are:

Trap (SLAVE): An exceptional condition was detected by the Floating Point Unit or another Slave Processor during the execution of a Slave Instruction. This trap is requested via the Status Word returned as part of the Slave Processor Protocol (Section 3.9.1).

3.0 Functional Description (Continued)

Trap (ILL): Illegal operation. A privileged operation was attempted while the CPU was in User Mode (PSR bit U=1).

Trap (SVC): The Supervisor Call (SVC) instruction was executed.

Trap (DVZ): An attempt was made to divide an integer by zero. (The Slave trap is used for Floating Point division by zero.)

Trap (FLG): The FLAG instruction detected a "1" in the CPU PSR F bit.

Trap (BPT): The Breakpoint (BPT) instruction was executed.

Trap (TRC): The instruction just completed is being traced. See below.

Trap (UND): An undefined opcode was encountered by the CPU.

A special case is the Trace Trap (TRC), which is enabled by setting the T bit in the Processor Status Register (PSR). At the beginning of each instruction, the T bit is copied into the PSR P (Trace "Pending") bit. If the P bit is set at the end of an instruction, then the Trace Trap is activated. If any other trap or interrupt request is made during a traced instruction, its entire service procedure is allowed to complete before the Trace Trap occurs. Each interrupt and trap sequence handles the P bit for proper tracing, guaranteeing one and only one Trace Trap per instruction, and guaranteeing that the Return Address pushed during a Trace Trap is always the address of the next instruction to be traced.

3.8.6 Prioritization

The NS32C016 CPU internally prioritizes simultaneous interrupt and trap requests as follows:

1) Traps other than Trace (Highest priority)
2) Abort
3) Non-Maskable Interrupt
4) Maskable Interrupts
5) Trace Trap (Lowest priority)

3.8.7 Interrupt/Trap Sequences: Detail Flow

For purposes of the following detailed discussion of interrupt and trap service sequences, a single sequence called "Service" is defined in *Figure 3-28.* Upon detecting any interrupt request or trap condition, the CPU first performs a sequence dependent upon the type of interrupt or trap. This sequence will include pushing the Processor Status Register and establishing a Vector and a Return Address. The CPU then performs the Service sequence.

For the sequenced followed in processing either Maskable or Non-Maskable Interrupts (on the $\overline{INT}$ or $\overline{NMI}$ pins, respectively), see Section 3.8.7.1. For Abort interrupts, see Section 3.8.7.4. For the Trace Trap, see Section 3.8.7.3, and for all other traps see Section 3.8.7.2.

3.8.7.1 Maskable/Non-Maskable Interrupt Sequence

This sequence is performed by the CPU when the $\overline{NMI}$ pin receives a falling edge, or the $\overline{INT}$ pin becomes active with the PSR I bit set. The interrupt sequence begins either at the next instruction boundary or, in the case of the String instructions, at the next interruptible point during its execution.

1. If a String instruction was interrupted and not yet completed:
   a. Clear the Processor Status Register P bit.
   b. Set "Return Address" to the address of the first byte of the interrupted instruction.

   Otherwise, set "Return Address" to the address of the next instruction.
2. Copy the Processor Status Register (PSR) into a temporary register, then clear PSR bits S, U, T, P and I.
3. If the interrupt is Non-Maskable:
   a. Read a byte from address $FFFF00_{16}$, applying Status Code 0100 (Interrupt Acknowledge, Master: Section 3.4.2). Discard the byte read.
   b. Set "Vector" to 1.
   c. Go to Step 8.
4. If the interrupt is Non-Vectored:
   a. Read a byte from address $FFFF00_{16}$, applying Status Code 0100 (Interrupt Acknowledge, Master: Section 3.4.2). Discard the byte read.
   b. Set "Vector" to 0.
   c. Go to Step 8.
5. Here the interrupt is Vectored. Read "Byte" from address $FFFE00_{16}$, applying Status Code 0100 (Interrupt Acknowledge, Master: Section 3.4.2).
6. If "Byte" ≥ 0, then set "Vector" to "Byte" and go to Step 8.
7. If "Byte" is in the range -16 through -1, then the interrupt source is Cascaded. (More negative values are reserved for future use.) Perform the following:
   a. Read the 32-bit Cascade Address from memory. The address is calculated as INTBASE + 4* Byte.
   b. Read "Vector," applying the Cascade Address just read and Status Code 0101 (Interrupt Acknowledge, Cascaded: Section 3.4.2).
8. Push the PSR copy (from Step 2) onto the Interrupt Stack as a 16-bit value.
9. Perform Service (Vector, Return Address), *Figure 3-28.*

Service (Vector, Return Address):

1) Read the 32-bit External Procedure Descriptor from the Interrupt Dispatch Table: address is Vector*4+INTBASE Register contents.
2) Move the Module field of the Descriptor into the MOD Register.
3) Read the new Static Base pointer from the memory address contained in MOD, placing it into the SB Register.
4) Read the Program Base pointer from memory address MOD+8, and add to it the Offset field from the Descriptor, placing the result in the Program Counter.
5) Flush Queue: Non-sequentially fetch first instruction of Interrupt Routine.
6) Push MOD Register onto the Interrupt Stack as a 16-bit value. (The PSR has already been pushed as a 16-bit value.)
7) Push the Return Address onto the Interrupt Stack as a 32-bit quantity.

FIGURE 3-28. Service Sequence
Invoked during all interrupt/trap sequences

3.0 Functional Description (Continued)

3.8.7.2 Trap Sequence: Traps Other Than Trace

1) Restore the currently selected Stack Pointer and the Processor Status Register to their original values at the start of the trapped instruction.
2) Set "Vector" to the value corresponding to the trap type.
   SLAVE: Vector=3.
   ILL: Vector=4.
   SVC: Vector=5.
   DVZ: Vector=6.
   FLG: Vector=7.
   BPT: Vector=8.
   UND: Vector=10.
3) Copy the Processor Status Register (PSR) into a temporary register, then clear PSR bits S, U, P and T.
4) Push the PSR copy onto the Interrupt Stack as a 16-bit value.
5) Set "Return Address" to the address of the first byte of the trapped instruction.
6) Perform Service (Vector, Return Address), *Figure 3-28.*

3.8.7.3 Trace Trap Sequence

1) In the Processor Status Register (PSR), clear the P bit.
2) Copy the PSR into a temporary register, then clear PSR bits S, U and T.
3) Push the PSR copy onto the Interrupt Stack as a 16-bit value.
4) Set "Vector" to 9.
5) Set "Return Address" to the address of the next instruction.
6) Perform Service (Vector, Return Address), *Figure 3-28.*

3.8.7.4 Abort Sequence

1) Restore the currently selected Stack Pointer to its original contents at the beginning of the aborted instruction.
2) Clear the PSR P bit.
3) Copy the PSR into a temporary register, then clear PSR bits S, U, T and I.
4) Push the PSR copy onto the Interrupt Stack as a 16-bit value.
5) Set "Vector" to 2.
6) Set "Return Address" to the address of the first byte of the aborted instruction.
7) Perform Service (Vector, Return Address), *Figure 3-28.*

3.9 SLAVE PROCESSOR INSTRUCTIONS

The NS32C016 CPU recognizes three groups of instructions as being executable by external Slave Processors:

Floating Point Instruction Set
Memory Management Instruction Set
Custom Instruction Set

Each Slave Instruction Set is validated by a bit in the Configuration Register (Section 2.1.3). Any Slave Instruction which does not have its corresponding Configuration Register bit set will trap as undefined, without any Slave Processor communication attempted by the CPU. This allows software simulation of a non-existent Slave Processor.

3.9.1 Slave Processor Protocol

Slave Processor instructions have a three-byte Basic Instruction field, consisting of an ID Byte followed by an Operation Word. The ID Byte has three functions:

1) It identifies the instruction as being a Slave Processor instruction.
2) It specifies which Slave Processor will execute it.
3) It determines the format of the following Operation Word of the instruction.

Upon receiving a Slave Processor instruction, the CPU initiates the sequence outlined in *Figure 3-29.* While applying Status Code 1111 (Broadcast ID, Section 3.4.2), the CPU transfers the ID Byte on the least-significant half of the Data Bus (AD0–AD7). All Slave Processors input this byte and decode it. The Slave Processor selected by the ID Byte is activated, and from this point the CPU is communicating only with it. If any other slave protocol was in progress (e.g., an aborted Slave instruction), this transfer cancels it.

The CPU next sends the Operation Word while applying Status Code 1101 (Transfer Slave Operand, Section 3.4.2). Upon receiving it, the Slave Processor decodes it, and at this point both the CPU and the Slave Processor are aware of the number of operands to be transferred and their sizes. The Operation Word is swapped on the Data Bus; that is, bits 0–7 appear on pins AD8–AD15 and bits 8–15 appear on pins AD0–AD7.

Using the Addressing Mode fields within the Operation Word, the CPU starts fetching operands and issuing them to the Slave Processor. To do so, it references any Addressing Mode extensions which may be appended to the Slave Processor instruction. Since the CPU is solely responsible for memory accesses, these extensions are not sent to the Slave Processor. The Status Code applied is 1101 (Transfer Slave Processor Operand, Section 3.4.2).

Status Combinations:
Send ID (ID): Code 1111
Xfer Operand (OP): Code 1101
Read Status (ST): Code 1110

Step	Status	Action
1	ID	CPU Send ID Byte.
2	OP	CPU Sends Operation Word.
3	OP	CPU Sends Required Operands.
4	—	Slave Starts Execution. CPU Pre-Fetches.
5	—	Slave Pulses $\overline{SPC}$ Low.
6	ST	CPU Reads Status Word. (Trap? Alter Flags?)
7	OP	CPU Reads Results (If Any).

FIGURE 3-29. Slave Processor Protocol

3.0 Functional Description (Continued)

After the CPU has issued the last operand, the Slave Processor starts the actual execution of the instruction. Upon completion, it will signal the CPU by pulsing $\overline{SPC}$ low. To allow for this, and for the Address Translation strap function, $\overline{AT}/\overline{SPC}$ is normally held high only by an internal pull-up device of approximately 5 kΩ.

While the Slave Processor is executing the instruction, the CPU is free to prefetch instructions into its queue. If it fills the queue before the Slave Processor finishes, the CPU will wait, applying Status Code 0011 (Waiting for Slave, Section 3.4.2).

Upon receiving the pulse on $\overline{SPC}$, the CPU uses $\overline{SPC}$ to read a Status Word from the Slave Processor, applying Status Code 1110 (Read Slave Status, Section 3.4.2). This word has the format shown in *Figure 3-30.* If the Q bit ("Quit", Bit 0) is set, this indicates that an error was detected by the Slave Processor. The CPU will not continue the protocol, but will immediately trap through the Slave vector in the Interrupt Table. Certain Slave Processor instructions cause CPU PSR bits to be loaded from the Status Word.

The last step in the protocol is for the CPU to read a result, if any, and transfer it to the destination. The Read cycles from the Slave Processor are performed by the CPU while applying Status Code 1101 (Transfer Slave Operand, Section 3.4.2).

An exception to the protocol above is the LMR (Load Memory Management Register) instruction, and a corresponding Custom Slave instruction (LCR: Load Custom Register). In executing these instructions, the protocol ends after the CPU has issued the last operand. The CPU does not wait for an acknowledgement from the Slave Processor, and it does not read status.

3.9.2 Floating Point Instructions

Table 3-4 gives the protocols followed for each Floating Point instruction. The instructions are referenced by their mnemonics. For the bit encodings of each instruction, see Appendix A.

The Operand class columns give the Access Class for each general operand, defining how the addressing modes are interpreted (see Series 32000 Instruction Set Reference Manual).

The Operand Issued columns show the sizes of the operands issued to the Floating Point Unit by the CPU. "D" indicates a 32-bit Double Word. "i" indicates that the instruction specifies an integer size for the operand (B=Byte, W=Word, D=Double Word). "f" indicates that the instruction specifies a Floating Point size for the operand (F=32-bit Standard Floating, L=64-bit Long Floating).

The Returned Value Type and Destination column gives the size of any returned value and where the CPU places it. The PSR Bits Affected column indicates which PSR bits, if any, are updated from the Slave Processor Status Word (*Figure 3-30).*

TABLE 3-4. Floating Point Instruction Protocols

Mnemonic	Operand 1 Class	Operand 2 Class	Operand 1 Issued	Operand 2 Issued	Returned Value Type and Dest.	PSR Bits Affected
ADDf	read.f	rmw.f	f	f	f to Op. 2	none
SUBf	read.f	rmw.f	f	f	f to Op. 2	none
MULf	read.f	rmw.f	f	f	f to Op. 2	none
DIVf	read.f	rmw.f	f	f	f to Op. 2	none
MOVf	read.f	write.f	f	N/A	f to Op. 2	none
ABSf	read.f	write.f	f	N/A	f to Op. 2	none
NEGf	read.f	write.f	f	N/A	f to Op. 2	none
CMPf	read.f	read.f	f	f	N/A	N,Z,L
FLOORfi	read.f	write.i	f	N/A	i to Op. 2	none
TRUNCfi	read.f	write.i	f	N/A	i to Op. 2	none
ROUNDfi	read.f	write.i	f	N/A	i to Op. 2	none
MOVFL	read.F	write.L	F	N/A	L to Op. 2	none
MOVLF	read.L	write.F	L	N/A	F to Op. 2	none
MOVif	read.i	write.f	i	N/A	f to Op. 2	none
LFSR	read.D	N/A	D	N/A	N/A	none
SFSR	N/A	write.D	N/A	N/A	D to Op. 2	none

Notes:

D = Double Word

i = integer size (B,W,D) specified in mnemonic.

f = Floating Point type (F,L) specified in mnemonic.

N/A = Not Applicable to this instruction.

3.0 Functional Description (Continued)

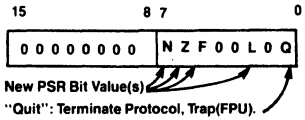

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FIGURE 3-30. Slave Processor Status Word Format

Any operand indicated as being of type "f" will not cause a transfer if the Register addressing mode is specified. This is because the Floating Point Registers are physically on the Floating Point Unit and are therefore available without CPU assistance.

3.9.3 Memory Management Instructions

Table 3-5 gives the protocols for Memory Management instructions. Encodings for these instructions may be found in Appendix A.

In executing the RDVAL and WRVAL instructions, the CPU calculates and issues the 32-bit Effective Address of the single operand. The CPU then performs a single-byte Read cycle from that address, allowing the MMU to safely abort the instruction if the necessary information is not currently in physical memory. Upon seeing the memory cycle complete, the MMU continues the protocol, and returns the validation result in the F bit of the Slave Status Word.

The size of a Memory Management operand is always a 32-bit Double Word. For further details of the Memory Management Instruction set, see the Series 32000 Instruction Set Reference Manual and the NS32082 MMU Data Sheet.

TABLE 3-5. Memory Management Instruction Protocols

Mnemonic	Operand 1 Class	Operand 2 Class	Operand 1 Issued	Operand 2 Issued	Returned Value Type and Dest.	PSR Bits Affected
RDVAL*	addr	N/A	D	N/A	N/A	F
WRVAL*	addr	N/A	D	N/A	N/A	F
LMR*	read.D	N/A	D	N/A	N/A	none
SMR*	write.D	N/A	N/A	N/A	D to Op. 1	none

Note:

In the RDVAL and WRVAL instructions, the CPU issues the address as a Double Word, and performs a single-byte Read cycle from that memory address. For details, see the Series 32000 Instruction Set Reference Manual and the NS32082 Memory Management Unit Data Sheet.

D = Double Word

* = Privileged Instruction: will trap if CPU is in User Mode.

N/A = Not Applicable to this instruction.

3.0 Functional Description (Continued)

3.9.4 Custom Slave Instructions

Provided in the NS32C016 is the capability of communicating with a user-defined, "Custom" Slave Processor. The instruction set provided for a Custom Slave Processor defines the instruction formats, the operand classes and the communication protocol. Left to the user are the interpretations of the Op Code fields, the programming model of the Custom Slave and the actual types of data transferred. The protocol specifies only the size of an operand, not its data type.

Table 3-6 lists the relevant information for the Custom Slave instruction set. The designation "c" is used to represent an operand which can be a 32-bit ("D") or 64-bit ("Q") quantity in any format; the size is determined by the suffix on the mnemonic. Similarly, an "i" indicates an integer size (Byte, Word, Double Word) selected by the corresponding mnemonic suffix.

Any operand indicated as being of type 'c' will not cause a transfer if the register addressing mode is specified. It is assumed in this case that the slave processor is already holding the operand internally.

For the instruction encodings, see Appendix A.

TABLE 3-6. Custom Slave Instruction Protocols

Mnemonic	Operand 1 Class	Operand 2 Class	Operand 1 Issued	Operand 2 Issued	Returned Value Type and Dest.	PSR Bits Affected
CCAL0c	read.c	rmw.c	c	c	c to Op. 2	none
CCAL1c	read.c	rmw.c	c	c	c to Op. 2	none
CCAL2c	read.c	rmw.c	c	c	c to Op. 2	none
CCAL3c	read.c	rmw.c	c	c	c to Op. 2	none
CMOV0c	read.c	write.c	c	N/A	c to Op. 2	none
CMOV1c	read.c	write.c	c	N/A	c to Op. 2	none
CMOV2c	read.c	write.c	c	N/A	c to Op. 2	none
CMOV3c	read.c	write.c	c	N/A	c to Op. 2	none
CCMP0c	read.c	read.c	c	c	N/A	N,Z,L
CCMP1c	read.c	read.c	c	c	N/A	N,Z,L
CCV0ci	read.c	write.i	c	N/A	i to Op. 2	none
CCV1ci	read.c	write.i	c	N/A	i to Op. 2	none
CCV2ci	read.c	write.i	c	N/A	i to Op. 2	none
CCV3ic	readi	write.c	i	N/A	c to Op. 2	none
CCV4DQ	read.D	write.Q	D	N/A	Q to Op. 2	none
CCV5QD	read.Q	write.D	Q	N/A	D to Op. 2	none
LCSR	read.D	N/A	D	N/A	N/A	none
SCSR	N/A	write.D	N/A	N/A	D to Op. 2	none
CATST0*	addr	N/A	D	N/A	N/A	F
CATST1*	addr	N/A	D	N/A	N/A	F
LCR*	read.D	N/A	D	N/A	N/A	none
SCR*	write.D	N/A	N/A	N/A	D to Op.1	none

Notes:

D = Double Word

i = integer size (B,W,D) specified in mnemonic.

c = Custom size (D:32 bits or Q:64 bits) specified in mnemonic.

* = Privileged instruction: will trap if CPU is in User Mode.

N/A = Not Applicable to this instruction.

4.0 Device Specifications

4.1 NS32C016 PIN DESCRIPTIONS

The following is a brief description of all NS32C016 pins. The descriptions reference portions of the Functional Description, Section 3.

4.1.1 Supplies

Logic Power (V_{CCL}): +5V positive supply for on-chip logic. Section 3.1.

Buffer Power (V_{CCB}): +5V positive supply for on-chip output buffers. Section 3.1.

Logic Ground (GNDL): Ground reference for on-chip logic. Section 3.1.

Buffer Ground (GNDB): Ground reference for on-chip drivers connected to output pins. Section 3.1.

4.1.2 Input Signals

Clocks (PHI1, PHI2): Two-phase clocking signals. Section 3.2.

Ready (RDY): Active high. While RDY is inactive, the CPU extends the current bus cycle to provide for a slower memory or peripheral reference. Upon detecting RDY active, the CPU terminates the bus cycle. Section 3.4.1.

Hold Request ($\overline{HOLD}$): Active low. Causes the CPU to release the bus for DMA or multiprocessing purposes. Section 3.6.

Note: If the $\overline{HOLD}$ signal is generated asynchronously, its set up and hold times may be violated. In this case it is recommended to synchronize it with CTTL to minimize the possibility of metastable states.

The CPU provides only one synchronization stage to minimize the $\overline{HLDA}$ latency. This is to avoid speed degradations in cases of heavy $\overline{HOLD}$ activity (i.e. DMA controller cycles interleaved with CPU cycles).

Interrupt ($\overline{INT}$): Active low. Maskable Interrupt request. Section 3.8.

Non-Maskable Interrupt ($\overline{NMI}$): Active low. Non-Maskable Interrupt request. Section 3.8.

Reset/Abort ($\overline{RST}/\overline{ABT}$): Active low. If held active for one clock cycle and released, this pin causes an Abort Command, Section 3.5.4. If held longer, it initiates a Reset, Section 3.3.

4.1.3 Output Signals

Address Bits 16–23 (A16–A23): These are the most significant 8 bits of the memory address bus. Section 3.4.

Address Strobe ($\overline{ADS}$): Active low. Controls address latches; indicates start of a bus cycle. Section 3.4.

Data Direction In ($\overline{DDIN}$): Active low. Status signal indicating direction of data transfer during a bus cycle. Section 3.4.

High Byte Enable ($\overline{HBE}$): Active low. Status signal enabling transfer on the most significant byte of the Data Bus. Section 3.4; Section 3.4.3.

Note: In the current NS32C016, the $\overline{HBE}$ signal is forced low by the CPU when $\overline{FLT}$ is asserted by the MMU. However, in future revisions of the CPU, $\overline{HBE}$ will no longer be affected by $\overline{FLT}$. Therefore, in a memory managed system, an external 'AND' gate is required. This is shown in *Figure B-1* in Appendix B.

Status (ST0–ST3): Active high. Bus cycle status code, ST0 least significant. Section 3.4.2. Encodings are:

0000—Idle: CPU Inactive on Bus.
0001—Idle: WAIT Instruction.
0010—(Reserved)
0011—Idle: Waiting for Slave.
0100—Interrupt Acknowledge, Master.
0101—Interrupt Acknowledge, Cascaded.
0110—End of Interrupt, Master.
0111—End of Interrupt, Cascaded.
1000—Sequential Instruction Fetch.
1001—Non-Sequential Instruction Fetch.
1010—Data Transfer.
1011—Read Read-Modify-Write Operand.
1100—Read for Effective Address.
1101—Transfer Slave Operand.
1110—Read Slave Status Word.
1111—Broadcast Slave ID.

Hold Acknowledge ($\overline{HLDA}$): Active low. Applied by the CPU in response to $\overline{HOLD}$ input, indicating that the bus has been released for DMA or multiprocessing purposes. Section 3.6.

User/Supervisor (U/$\overline{S}$): User or Supervisor Mode status. Section 3.7. High state indicates User Mode, low indicates Supervisor Mode. Section 3.7.

Interlocked Operation ($\overline{ILO}$): Active low. Indicates that an interlocked instruction is being executed. Section 3.7.

Program Flow Status ($\overline{PFS}$): Active Low. Pulse indicates beginning of an instruction execution. Section 3.7.

4.1.4 Input-Output Signals

Address/Data 0–15 (AD0–AD15): Multiplexed Address/Data information. Bit 0 is the least significant bit of each. Section 3.4.

Address Translation/Slave Processor Control ($\overline{AT}/\overline{SPC}$): Active low. Used by the CPU as the data strobe output for Slave Processor transfers; used by Slave Processors to acknowledge completion of a slave instruction. Section 3.4.6; Section 3.9. Sampled on the rising edge of Reset as Address Translation Strap. Section 3.5.1.

In non-memory-managed systems this pin should be pulled up to V_{CC} through a 10 kΩ resistor.

Data Strobe/Float ($\overline{DS}/\overline{FLT}$): Active low. Data Strobe output, Section 3.4, or Float Command input, Section 3.5.3. Pin function is selected on $\overline{AT}/\overline{SPC}$ pin, Section 3.5.1.

4.0 Device Specifications (Continued)

4.2 ABSOLUTE MAXIMUM RATINGS

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Temperature Under Bias	0°C to +70°C
Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to GND	−0.5V to +7V
Power Dissipation	1.5 Watt

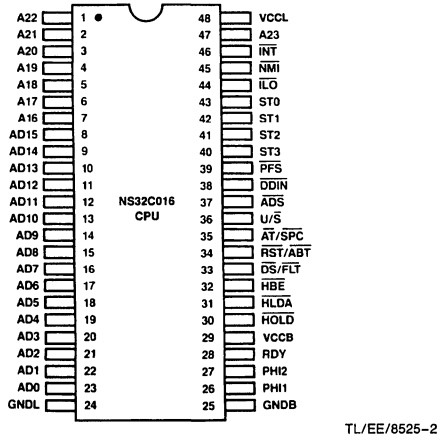
Note: *Absolute maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended; operation should be limited to those conditions specified under Electrical Characteristics.*

4.3 ELECTRICAL CHARACTERISTICS: $T_A = -40°C$ to $+85°C$, $V_{CC} = 5V \pm 10\%$, GND = 0V

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High Level Input Voltage		2.0		$V_{CC} + 0.5$	V
V_{IL}	Low Level Input Voltage		−0.5		0.8	V
V_{CH}	High Level Clock Voltage	PHI1, PHI2 pins only	0.90 V_{CC}		$V_{CC} + 0.5$	V
V_{CL}	Low Level Clock Voltage	PHI1, PHI2 pins only	−0.5		0.10 V_{CC}	V
V_{CRT}	Clock Input Ringing Tolerance	PHI1, PHI2 pins only	−0.5		0.6	V
V_{OH}	High Level Output Voltage	$I_{OH} = -400\ \mu A$	0.90 V_{CC}			V
V_{OL}	Low Level Output Voltage	$I_{OL} = 2$ mA			0.10 V_{CC}	V
I_{ILS}	$\overline{AT}/\overline{SPC}$ Input Current (low)	$V_{IN} = 0.4V$, $\overline{AT}/\overline{SPC}$ in input mode	0.05		1.0	mA
I_I	Input Load Current	$0 \le V_{IN} \le V_{CC}$, All inputs except PHI1, PHI2, $\overline{AT}/\overline{SPC}$	−20		20	μA
I_L	Leakage Current Output and IO Pins in TRI-STATE/ Input Mode	$0.4 \le V_{IN} \le V_{CC}$	−20		20	μA
I_{CC}	Active Supply Current	$I_{OUT} = 0$, $T_A = 25°C$		70	100	mA

Connection Diagram

Dual-In-Line Package



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Top View

FIGURE 4-1

Order Number NS32C016D-10, NS32C016D-15, NS32C016N-10 or NS32C016N-15
See NS Package Number D48A or N48A

4.0 Device Specifications (Continued)

4.4 SWITCHING CHARACTERISTICS

4.4.1 Definitions

All the timing specifications given in this section refer to 2.0V on the rising or falling edges of the clock phases PHI1 and PHI2; to 15% or 85% of V_{CC} on all the CMOS output signals, and to 0.8V or 2.0V on all the TTL input signals as illustrated in *Figures 4-2* and *4-3* unless specifically stated otherwise.

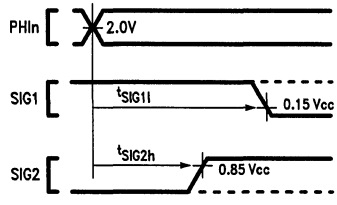

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FIGURE 4-2. Timing Specification Standard (CMOS Output Signals)

ABBREVIATIONS:

L.E. — leading edge R.E. — rising edge

T.E. — trailing edge F.E. — falling edge

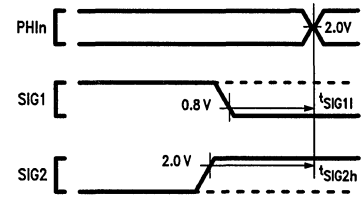

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FIGURE 4-3. Timing Specification Standard (TTL Input Signals)

4.4.2 Timing Tables

4.4.2.1 Output Signals: Internal Propagation Delays, NS32C016-10 and NS32C016-15

Maximum times assume capacitive loading of 75 pF, on the address/data bus signals and 50 pF on all other signals.

Name	Figure	Description	Reference/Conditions	NS32C016-10		NS32C016-15		Units
				Min	Max	Min	Max	
t_{ALv}	4-4	Address bits 0–15 valid	after R.E., PHI1 T1		40		35	ns
t_{ALh}	4-4	Address bits 0–15 hold	after R.E., PHI1 Tmmu or T2	5		5		ns
t_{Dv}	4-4	Data valid (write cycle)	after R.E., PHI1 T2		50		35	ns
t_{Dh}	4-4	Data hold (write cycle)	after R.E., PHI1 next T1 or Ti	0		0		ns
t_{AHv}	4-4	Address bits 16–23 valid	after R.E., PHI1 T1		40		35	ns
t_{AHh}	4-4	Address bits 16–23 hold	after R.E., PHI1 next T1 or Ti	0		0		ns
t_{ALADSs}	4-5	Address bits 0–15 set up	before $\overline{ADS}$ T.E.	25		20		ns
t_{AHADSs}	4-5	Address bits 16–23 set up	before $\overline{ADS}$ T.E.	25		20		ns
t_{ALADSh}	4-9	Address bits 0–15 hold	after $\overline{ADS}$ T.E.	15		10		ns
t_{AHADSh}	4-9	Address bits 16–23 hold	after $\overline{ADS}$ T.E.	15		10		ns
t_{ALf}	4-5	Address bits 0–15 floating (no MMU)	after R.E., PHI1 T2		25		20	ns
t_{ALMf}	4-9	Address bits 0–15 floating (with MMU)	after R.E., PHI1 TMMU		25		20	ns
t_{AHMf}	4-9	Address bits 16–23 floating (with MMU)	after R.E., PHI1 TMMU		25		20	ns
t_{HBEv}	4-4	$\overline{HBE}$ signal valid	after R.E., PHI1 T1		45		35	ns
t_{HBEh}	4-4	$\overline{HBE}$ signal hold	after R.E., PHI1 next T1 or Ti	0		0		ns
t_{STv}	4-4	Status (ST0–ST3) valid	after R.E., PHI1 T4 (before T1, see note)		45		35	ns
t_{STh}	4-4	Status (ST0–ST3) hold	after R.E., PHI1 T4 (after T1)	0		0		ns
t_{DDINv}	4-5	$\overline{DDIN}$ signal valid	after R.E., PHI1 T1		50		35	ns

4.0 Device Specifications (Continued)

4.4.2.1 Output Signals: Internal Propagation Delays, NS32C016-10 and NS32C016-15 (Continued)

Name	Figure	Description	Reference/Conditions	NS32C016-10		NS32C016-15		Units
				Min	Max	Min	Max	
t_{DDINh}	4-5	$\overline{DDIN}$ signal hold	after R.E., PHI1 next T1 or Ti	0		0		ns
t_{ADSa}	4-4	$\overline{ADS}$ signal active (low)	after R.E., PHI1 T1		35		26	ns
t_{ADSia}	4-4	$\overline{ADS}$ signal inactive	after R.E., PHI2 T1		40		30	ns
t_{ADSw}	4-4	$\overline{ADS}$ pulse width	at 15% V_{CC} (both edges)	30		25		ns
t_{DSa}	4-4	$\overline{DS}$ signal active (low)	after R.E., PHI1 T2		40		30	ns
t_{DSia}	4-4	$\overline{DS}$ signal inactive	after R.E., PHI1 T4		40		30	ns
t_{ALf}	4-6	AD0–AD15 floating	after R.E., PHI1 T1 (caused by $\overline{HOLD}$)		25		20	ns
t_{AHf}	4-6	A16–A23 floating	after R.E., PHI1 T1 (caused by $\overline{HOLD}$)		25		20	ns
t_{DSf}	4-6	$\overline{DS}$ floating (caused by $\overline{HOLD}$)	after R.E., PHI1 Ti		50		40	ns
t_{ADSf}	4-6	$\overline{ADS}$ floating (caused by $\overline{HOLD}$)	after R.E., PHI1 Ti		50		40	ns
t_{HBEf}	4-6	$\overline{HBE}$ floating (caused by $\overline{HOLD}$)	after R.E., PHI1 Ti		50		40	ns
t_{DDINf}	4-6	$\overline{DDIN}$ floating (caused by $\overline{HOLD}$)	after R.E., PHI1 Ti		50		40	ns
t_{HLDAa}	4-6	$\overline{HLDA}$ signal active (low)	after R.E., PHI1 Ti		30		25	ns
t_{HLDAia}	4-8	$\overline{HLDA}$ signal inactive	after R.E., PHI1 Ti		40		30	ns
t_{DSr}	4-8	$\overline{DS}$ signal returns from floating (caused by HOLD)	after R.E., PHI1 Ti		55		40	ns
t_{ADSr}	4-8	$\overline{ADS}$ signal returns from floating (caused by $\overline{HOLD}$)	after R.E., PHI1 Ti		55		40	ns
t_{HBEr}	4-8	$\overline{HBE}$ signal returns from floating (caused by $\overline{HOLD}$)	after R.E., PHI1 Ti		55		40	ns
t_{DDINr}	4-8	$\overline{DDIN}$ signal returns from floating (caused by $\overline{HOLD}$)	after R.E., PHI1 Ti		55		40	ns
t_{DDINf}	4-9	$\overline{DDIN}$ signal floating (caused by $\overline{FLT}$)	after $\overline{FLT}$ F.E.		55		50	ns
t_{HBEl}	4-9	$\overline{HBE}$ signal low (caused by $\overline{FLT}$)	after $\overline{FLT}$ F.E.		40		30	ns
t_{DDINr}	4-10	$\overline{DDIN}$ signal returns from floating (caused by $\overline{FLT}$)	after $\overline{FLT}$ R.E.		40		30	ns
t_{HBEr}	4-10	$\overline{HBE}$ signal returns from low (caused by $\overline{FLT}$)	after $\overline{FLT}$ R.E.		35		25	ns
t_{SPCa}	4-13	$\overline{SPC}$ output active (low)	after R.E., PHI1 T1		35		26	ns
t_{SPCia}	4-13	$\overline{SPC}$ output inactive	after R.E., PHI1 T4		35		26	ns
t_{SPCnf}	4-15	$\overline{SPC}$ output nonforcing	after R.E., PHI2 T4		30		25	ns
t_{Dv}	4-13	Data valid (slave processor write)	after R.E., PHI1 T1		50		35	ns
t_{Dh}	4-13	Data hold (slave processor write)	after R.E., PHI1 next T1 or Ti	0		0		ns
t_{PFSw}	4-18	$\overline{PFS}$ pulse width	at 15% V_{CC} (both edges)	50		40		ns
t_{PFSa}	4-18	$\overline{PFS}$ pulse active (low)	after R.E., PHI2		40		35	ns
t_{PFSia}	4-18	$\overline{PFS}$ pulse inactive	after R.E., PHI2		40		35	ns
t_{ILOs}	4-20a	$\overline{ILO}$ signal setup	before R.E., PHI1 T1 of first interlocked write cycle	50		35		ns
t_{ILOh}	4-20b	$\overline{ILO}$ signal hold	after R.E., PHI1 T3 of last interlocked read cycle	10		7		ns
t_{ILOa}	4-21	$\overline{ILO}$ signal active (low)	after R.E., PHI1		35		30	ns

4.0 Device Specifications (Continued)

4.4.2.1 Output Signals: Internal Propagation Delays, NS32C016-10 and NS32C016-15 (Continued)

Name	Figure	Description	Reference/Conditions	NS32C016-10		NS32C016-15		Units
				Min	Max	Min	Max	
t_{ILOia}	4-21	$\overline{ILO}$ signal inactive	after R.E., PHI1		35		30	ns
t_{USV}	4-22	U/$\overline{S}$ signal valid	after R.E., PHI1 T4		35		30	ns
t_{USh}	4-22	U/$\overline{S}$ signal hold	after R.E., PHI1 T4	8		6		ns
t_{NSPF}	4-19b	Nonsequential fetch to next $\overline{PFS}$ clock cycle	after R.E., PHI1 T1	4		4		t_{Cp}
t_{PFNS}	4-19a	$\overline{PFS}$ clock cycle to next nonsequential fetch	before R.E., PHI1 T1	4		4		t_{Cp}
t_{LXPF}	4-29	Last operand transfer of an instruction to next $\overline{PFS}$ clock cycle	before R.E., PHI1 T1 of first bus cycle of transfer	0		0		t_{Cp}

Note: Every memory cycle starts with T4, during which Cycle Status is applied. If the CPU was idling, the sequence will be: ". . . Ti, T4, T1 . . .". If the CPU was not idling, the sequence will be: ". . . T4, T1 . . .".

4.4.2.2 Input Signal Requirements: NS32C016-10 and NS32C016-15

Name	Figure	Description	Reference/Conditions	NS32C016-10		NS32C016-15		Units
				Min	Max	Min	Max	
t_{PWR}	4-25	Power stable to $\overline{RST}$ R.E.	after V_{CC} reaches 4.5V	50		33		µs
t_{DIs}	4-5	Data in setup (read cycle)	before F.E., PHI2 T3	15		10		ns
t_{DIh}	4-5	Data in hold (read cycle)	after F.E., PHI1 T4	3		3		ns
t_{HLDa}	4-6	$\overline{HOLD}$ active (low) setup time (see note)	before F.E., PHI2 TX1	25		17		ns
t_{HLDia}	4-8	$\overline{HOLD}$ inactive setup time	before F.E., PHI2 Ti	25		17		ns
t_{HLDh}	4-6	$\overline{HOLD}$ hold time	after R.E., PHI1 TX2	0		0		ns
t_{FLTa}	4-9	$\overline{FLT}$ active (low) setup time	before F.E., PHI2 Tmmu	25		17		ns
t_{FLTia}	4-10	$\overline{FLT}$ inactive setup time	before F.E., PHI2 T2	25		17		ns
t_{RDYs}	4-11, 4-12	RDY setup time	before F.E., PHI2 T2 or T3	15		10		ns
t_{RDYh}	4-11, 4-12	RDY hold time	after F.E., PHI1 T3	5		5		ns
t_{ABTs}	4-23	$\overline{ABT}$ setup time ($\overline{FLT}$ inactive)	before F.E., PHI2 Tmmu	20		13		ns
t_{ABTs}	4-24	$\overline{ABT}$ setup time ($\overline{FLT}$ active)	before F.E., PHI2 Tf	20		13		ns
t_{ABTh}	4-23	$\overline{ABT}$ hold time	after R.E., PHI1	0		0		ns
t_{RSTs}	4-25, 4-26	$\overline{RST}$ setup time	before F.E., PHI1	10		8		ns
t_{RSTw}	4-26	$\overline{RST}$ pulse width	at 0.8V (both edges)	64		64		t_{Cp}
t_{INTs}	4-27	$\overline{INT}$ setup time	before R.E., PHI1	20		15		ns
t_{NMIw}	4-28	$\overline{NMI}$ pulse width	at 0.8V (both edges)	70		70		ns
t_{DIs}	4-14	Data setup (slave read cycle)	before F.E., PHI2 T1	15		10		ns
t_{DIh}	4-14	Data hold (slave read cycle)	after R.E., PHI1 T4	3		3		ns

4.0 Device Specifications (Continued)

4.4.2.2 Input Signal Requirements: NS32C016-10 and NS32C016-15 (Continued)

Name	Figure	Description	Reference/Conditions	NS32C016-10		NS32C016-15		Units
				Min	Max	Min	Max	
t_{SPCd}	4-15	$\overline{SPC}$ pulse delay from slave	after R.E., PHI2 T4	30		25		ns
t_{SPCs}	4-15	$\overline{SPC}$ setup time	before F.E., PHI1	30		25		ns
t_{SPCw}	4-15	$\overline{SPC}$ pulse width from slave processor (async. input)	at 0.8V (both edges)	20		20		ns
t_{ATs}	4-16	$\overline{AT}/\overline{SPC}$ setup for address translation strap	before R.E., PHI1 of cycle during which $\overline{RST}$ pulse is removed	1		1		t_{Cp}
t_{ATh}	4-16	$\overline{AT}/\overline{SPC}$ hold for address translation strap	after F.E., PHI1 of cycle during which $\overline{RST}$ pulse is removed	2		2		t_{Cp}

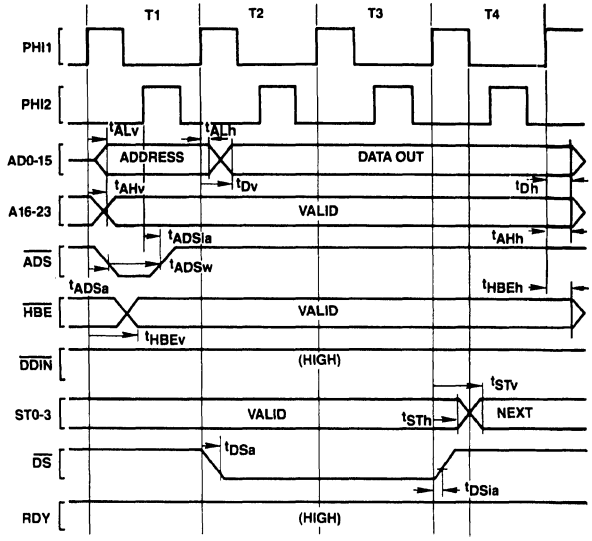
Note: This setup time is necessary to ensure prompt acknowledgement via $\overline{HLDA}$ and the ensuing floating of CPU off the buses. Note that the time from the receipt of the $\overline{HOLD}$ signal until the CPU floats is a function of the time $\overline{HOLD}$ signal goes low, the state of the RDY input (in MMU systems), and the length of the current MMU cycle.

4.4.2.3 Clocking Requirements: NS32C016-10 and NS32C016-15

Name	Figure	Description	Reference/Conditions	NS32C016-10		NS32C016-15		Units
				Min	Max	Min	Max	
t_{Cp}	4-17	Clock period	R.E., PHI1, PHI2 to next R.E., PHI1, PHI2	100	250	66	250	ns
t_{CLw}	4-17	PHI1, PHI2 pulse width	At 2.0V on PHI1, PHI2 (both edges)	$0.5t_{Cp}$ −10 ns		$0.5t_{Cp}$ −6 ns		
t_{CLh}	4-17	PHI1, PHI2 High Time	At 90% V_{CC} on PHI1, PHI2	$0.5t_{Cp}$ −15 ns		$0.5t_{Cp}$ −10 ns		
t_{CLl}	4-17	PHI1, PHI2 Low Time	At 15% V_{CC} on PHI1, PHI2	$0.5t_{Cp}$ −5 ns		$0.5t_{Cp}$ −5 ns		
$t_{nOVL(1,2)}$	4-17	Non-overlap time	At 15% V_{CC} on PHI1, PHI2	−2	2	−2	2	ns
t_{nOVLas}		Non-overlap asymmetry ($t_{nOVL(1)} - t_{nOVL(2)}$)	At 15% V_{CC} on PHI1, PHI2	−3	3	−3	3	ns
t_{CLwas}		PHI1, PHI2 asymmetry ($t_{CLw(1)} - t_{CLw(2)}$)	At 2.0V on PHI1, PHI2	−5	5	−3	3	ns

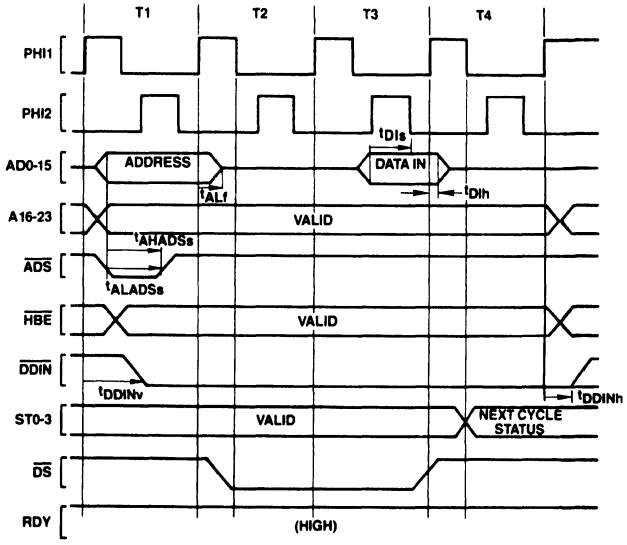
4.0 Device Specifications (Continued)

4.4.3 Timing Diagrams



TL/EE/8525–41

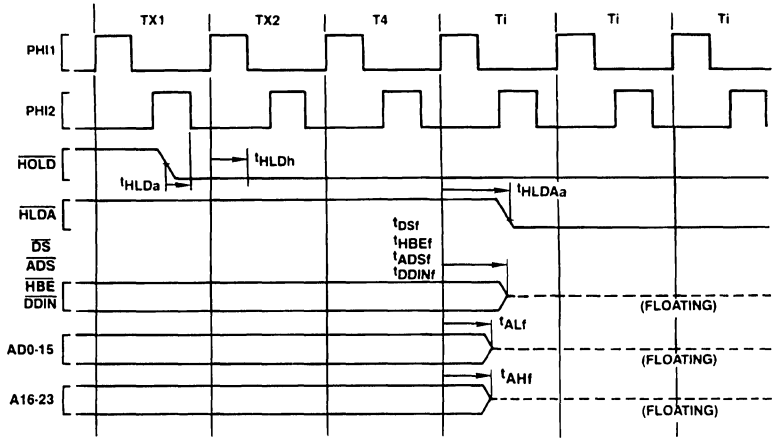
FIGURE 4-4. Write Cycle



TL/EE/8525–42

FIGURE 4-5. Read Cycle

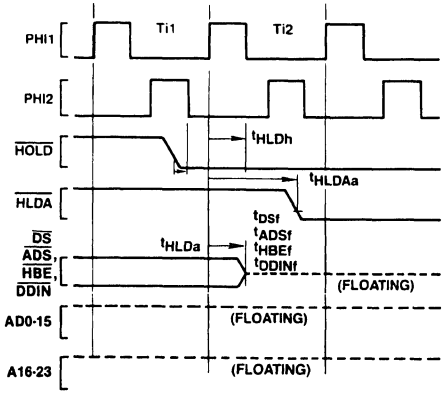
4.0 Device Specifications (Continued)



TL/EE/8525-43

FIGURE 4-6. Floating by $\overline{\text{HOLD}}$ Timing (CPU Not Idle Initially)

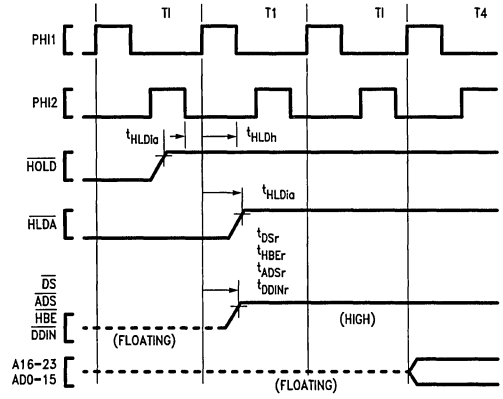
Note that whenever the CPU is not idling (not in Ti), the $\overline{\text{HOLD}}$ request ($\overline{\text{HOLD}}$ low) must be active t_{HLDa} before the falling edge of PHI2 of the clock cycle that appears two clock cycles before T4 (TX1) and stay low until t_{HLDh} after the rising edge of PHI1 of the clock cycle that precedes T4 (TX2) for the request to be acknowledged.



TL/EE/8525-44

FIGURE 4-7. Floating by $\overline{\text{HOLD}}$ Timing (CPU Initially Idle)

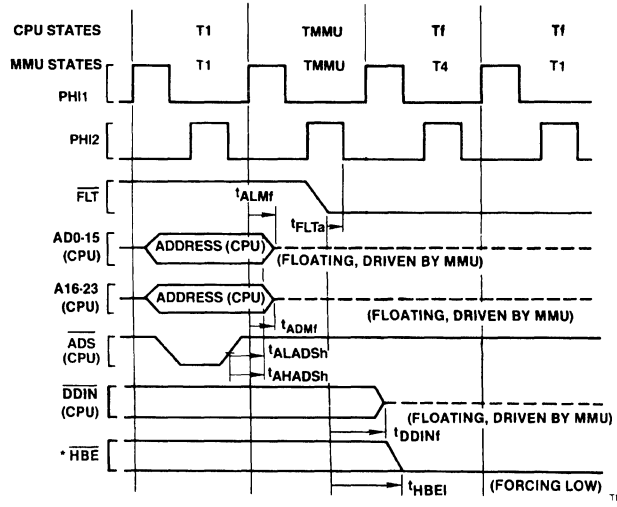
Note that during Ti1 the CPU is already idling.



TL/EE/8525-80

FIGURE 4-8. Release from $\overline{\text{HOLD}}$

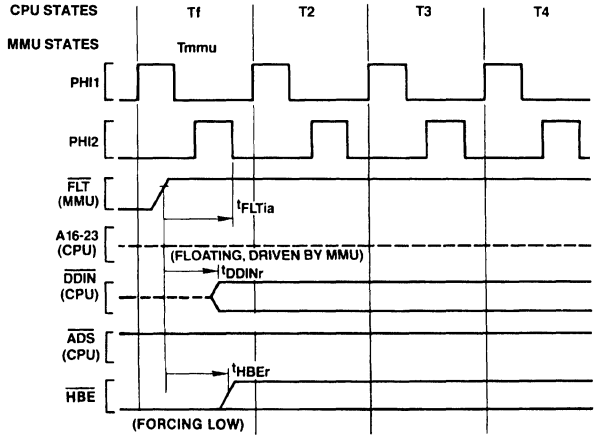
4.0 Device Specifications (Continued)



TL/EE/8525-46

***Note:** In future higher speed versions of the NS32C016, $\overline{HBE}$ will no longer be affected by $\overline{FLT}$. See *Figure B-1* in Appendix B for the required modification to the interface logic.

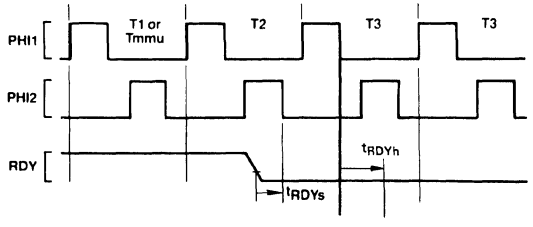
FIGURE 4-9. $\overline{FLT}$ Initiated Cycle Timing



TL/EE/8525-47

Note that when $\overline{FLT}$ is deasserted the CPU restarts driving $\overline{DDIN}$ before the MMU releases it. This, however, does not cause any conflict, since both CPU and MMU force $\overline{DDIN}$ to the same logic level.

FIGURE 4-10. Release from $\overline{FLT}$ Timing



TL/EE/8525-48

FIGURE 4-11. Ready Sampling (CPU Initially READY)

4.0 Device Specifications (Continued)

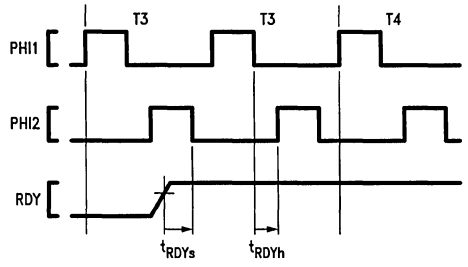


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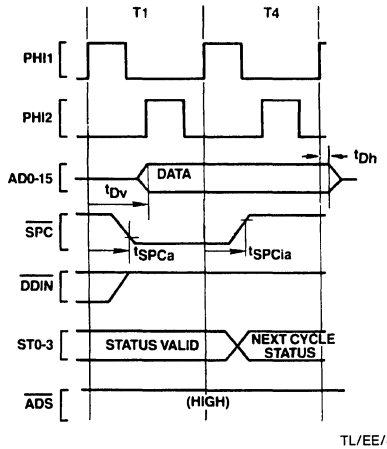
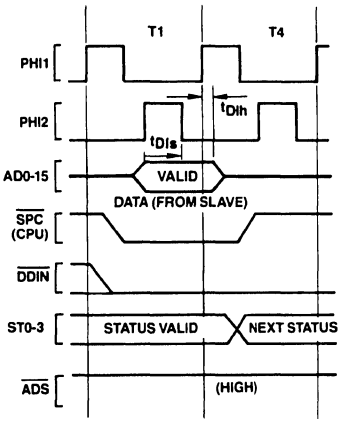
FIGURE 4-12. Ready Sampling (CPU Initially NOT READY)



TL/EE/8525-50

FIGURE 4-13. Slave Processor Write Timing



TL/EE/8525-51

FIGURE 4-14. Slave Processor Read Timing

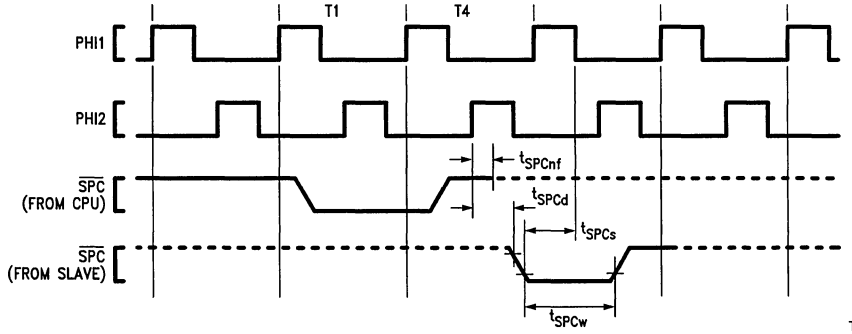


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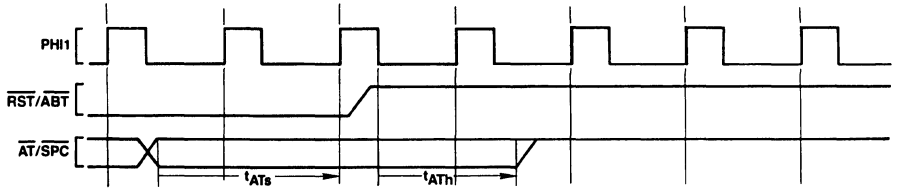
FIGURE 4-15. $\overline{SPC}$ Timing

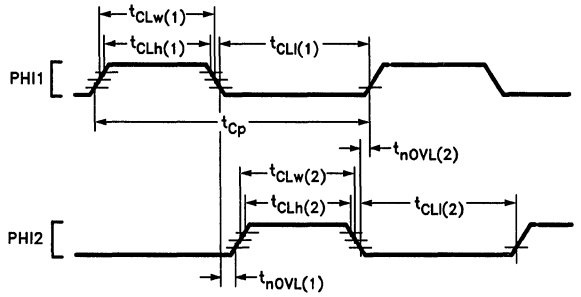
After transferring last operand to a Slave Processor, CPU turns OFF driver and holds $\overline{SPC}$ high with internal 5 kΩ pullup.



TL/EE/8525-53

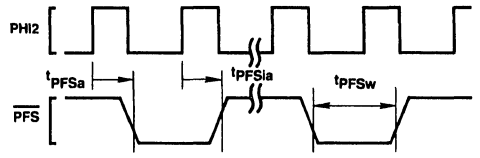
FIGURE 4-16. Reset Configuration Timing

4.0 Device Specifications (Continued)



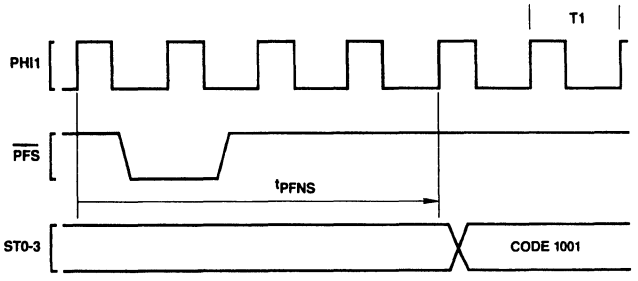
TL/EE/8525-54

FIGURE 4-17. Clock Waveforms



TL/EE/8525-55

FIGURE 4-18. Relationship of $\overline{PFS}$ to Clock Cycles



TL/EE/8525-56

FIGURE 4-19a. Guaranteed Delay, $\overline{PFS}$ to Non-Sequential Fetch

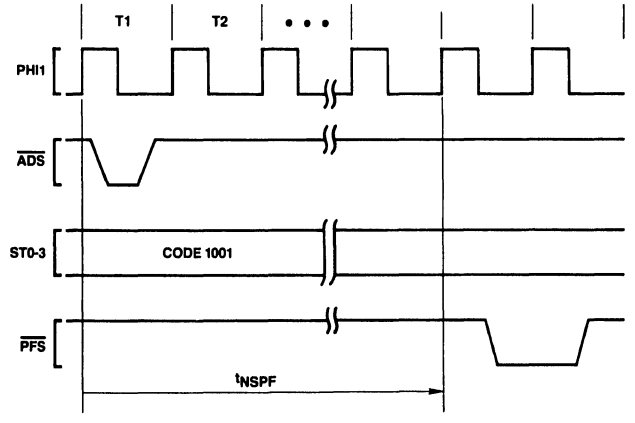


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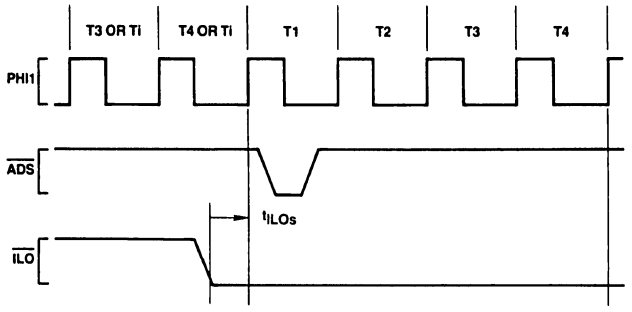
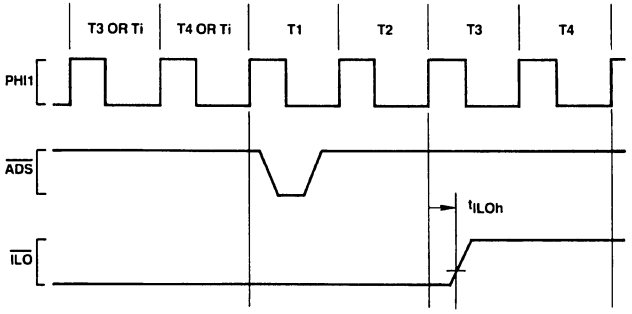
FIGURE 4-19b. Guaranteed Delay, Non-Sequential Fetch to $\overline{PFS}$

4.0 Device Specifications (Continued)



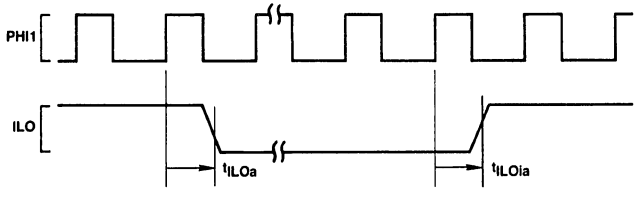
TL/EE/8525-58

FIGURE 4-20a. Relationship of $\overline{ILO}$ to First Operand Cycle of an Interlocked Instruction



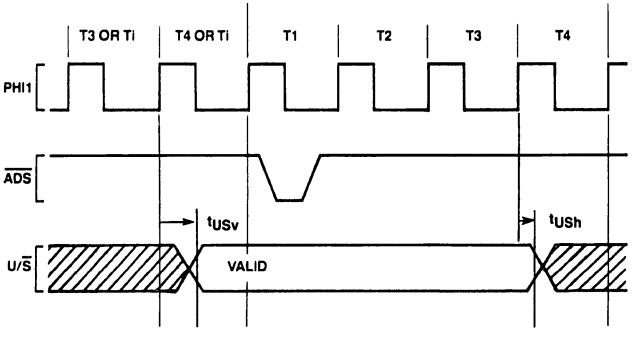
TL/EE/8525-59

FIGURE 4-20b. Relationship of $\overline{ILO}$ to Last Operand Cycle of an Interlocked Instruction



TL/EE/8525-60

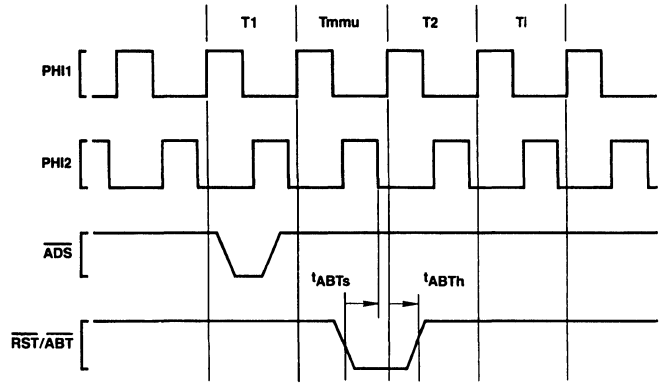
FIGURE 4-21. Relationship of $\overline{ILO}$ to Any Clock Cycle



TL/EE/8525-61

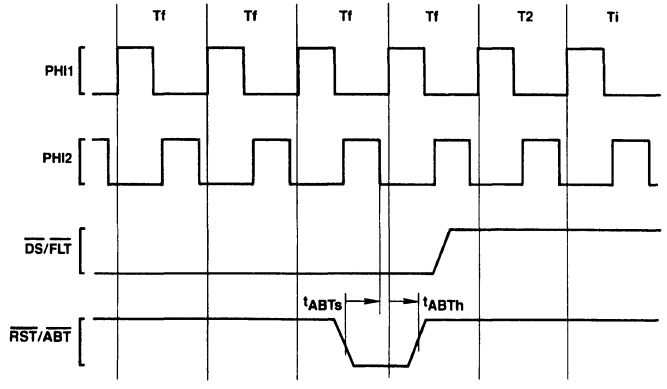
FIGURE 4-22. U/$\overline{S}$ Relationship to Any Bus Cycle—Guaranteed Valid Interval

4.0 Device Specifications (Continued)



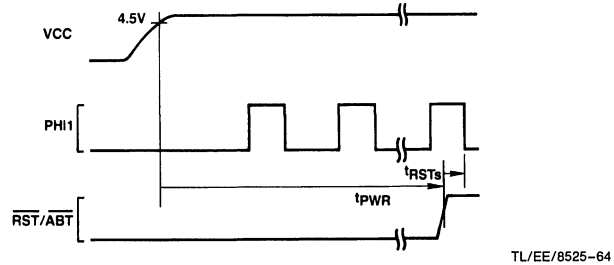
TL/EE/8525-62

FIGURE 4-23. Abort Timing, $\overline{FLT}$ Not Applied



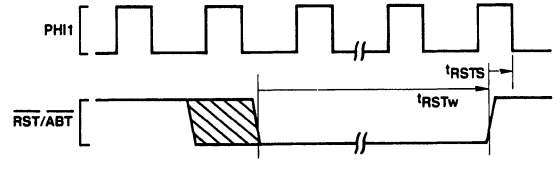
TL/EE/8525-63

FIGURE 4-24. Abort Timing, $\overline{FLT}$ Applied



TL/EE/8525-64

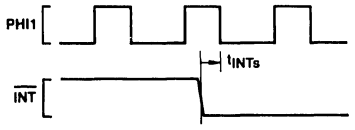
FIGURE 4-25. Power-On Reset



TL/EE/8525-65

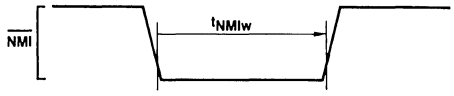
FIGURE 4-26. Non-Power-On Reset

4.0 Device Specifications (Continued)



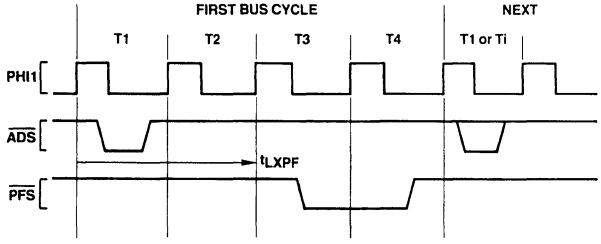
TL/EE/8525-66

FIGURE 4-27. $\overline{INT}$ Interrupt Signal Detection



TL/EE/8525-67

FIGURE 4-28. $\overline{NMI}$ Interrupt Signal Timing



TL/EE/8525-68

FIGURE 4-29. Relationship Between Last Data Transfer of an Instruction and $\overline{PFS}$ Pulse of Next Instruction

NOTE:

In a transfer of a Read-Modify-Write type operand, this is the Read transfer, displaying RMW Status (Code 1011).

Appendix A: Instruction Formats

NOTATIONS:

i = Integer Type Field
- B = 00 (Byte)
- W = 01 (Word)
- D = 11 (Double Word)

f = Floating Point Type Field
- F = 1 (Std. Floating: 32 bits)
- L= 0 (Long Floating: 64 bits)

c = Custom Type Field
- D = 1 (Double Word)
- Q = 0 (Quad Word)

op = Operation Code
- Valid encodings shown with each format.

gen, gen 1, gen 2 = General Addressing Mode Field
- See Sec. 2.2 for encodings.

reg = General Purpose Register Number

cond = Condition Code Field
- 0000 = EQual: Z = 1
- 0001 = Not Equal: Z = 0
- 0010 = Carry Set: C = 1
- 0011 = Carry Clear: C = 0
- 0100 = Higher: L = 1
- 0101 = Lower or Same: L = 0
- 0110 = Greater Than: N = 1
- 0111 = Less or Equal: N = 0
- 1000 = Flag Set: F = 1
- 1001 = Flag Clear: F = 0
- 1010 = LOwer: L = 0 and Z = 0
- 1011 = Higher or Same: L = 1 or Z = 1
- 1100 = Less Than: N = 0 and Z = 0
- 1101 = Greater or Equal: N = 1 or Z = 1
- 1110 = (Unconditionally True)
- 1111 = (Unconditionally False)

short = Short Immediate Value. May contain:
- quick: Signed 4-bit value, in MOVQ, ADDQ, CMPQ, ACB.
- cond: Condition Code (above), in Scond.
- areg: CPU Dedicated Register, in LPR, SPR.
  - 0000 = US
  - 0001 – 0111 = (Reserved)
  - 1000 = FP
  - 1001 = SP
  - 1010 = SB
  - 1011 = (Reserved)
  - 1100 = (Reserved)
  - 1101 = PSR
  - 1110 = INTBASE
  - 1111 = MOD

Options: in String Instructions

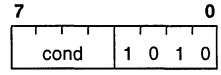
U/W	B	T

T = Translated
B = Backward
U/W = 00: None
- 01: While Match
- 11: Until Match

Configuration bits, in SETCFG:

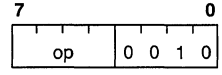
C	M	F	I

mreg: NS32082 Register number, in LMR, SMR.
- 0000 = BPR0
- 0001 = BPR1
- 0010 = (Reserved)
- 0011 = (Reserved)
- 0100 = (Reserved)
- 0101 = (Reserved)
- 0110 = (Reserved)
- 0111 = (Reserved)
- 1000 = (Reserved)
- 1001 = (Reserved)
- 1010 = MSR
- 1011 = BCNT
- 1100 = PTB0
- 1101 = PTB1
- 1110 = (Reserved)
- 1111 = EIA



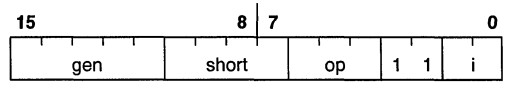
Format 0

Bcond (BR)



Format 1

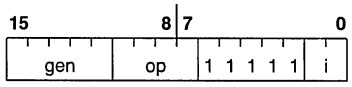
BSR	–0000	ENTER	–1000
RET	–0001	EXIT	–1001
CXP	–0010	NOP	–1010
RXP	–0011	WAIT	–1011
RETT	–0100	DIA	–1100
RETI	–0101	FLAG	–1101
SAVE	–0110	SVC	–1110
RESTORE	–0111	BPT	–1111



Format 2

ADDQ	–000	ACB	–100
CMPQ	–001	MOVQ	–101
SPR	–010	LPR	–110
Scond	–011		

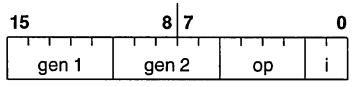
Appendix A: Instruction Formats (Continued)



Format 3

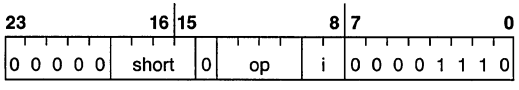
CXPD	−0000	ADJSP	−1010
BICPSR	−0010	JSR	−1100
JUMP	−0100	CASE	−1110
BISPSR	−0110		

Trap (UND) on XXX1, 1000



Format 4

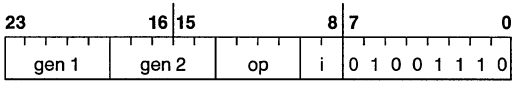
ADD	−0000	SUB	−1000
CMP	−0001	ADDR	−1001
BIC	−0010	AND	−1010
ADDC	−0100	SUBC	−1100
MOV	−0101	TBIT	−1101
OR	−0110	XOR	−1110



Format 5

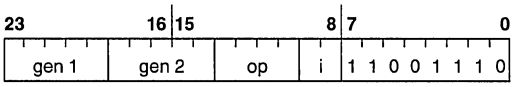
MOVS	−0000	SETCFG	−0010
CMPS	−0001	SKPS	−0011

Trap (UND) on 1XXX, 01XX



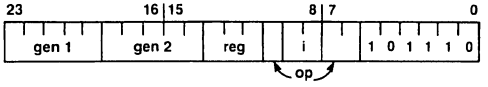
Format 6

ROT	−0000	NEG	−1000
ASH	−0001	NOT	−1001
CBIT	−0010	Trap (UND)	−1010
CBITI	−0011	SUBP	−1011
Trap (UND)	−0100	ABS	−1100
LSH	−0101	COM	−1101
SBIT	−0110	IBIT	−1110
SBITI	−0111	ADDP	−1111



Format 7

MOVM	−0000	MUL	−1000
CMPM	−0001	MEI	−1001
INSS	−0010	Trap (UND)	−1010
EXTS	−0011	DEI	−1011
MOVXBW	−0100	QUO	−1100
MOVZBW	−0101	REM	−1101
MOVZiD	−0110	MOD	−1110
MOVXiD	−0111	DIV	−1111



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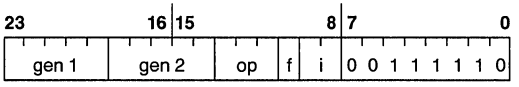
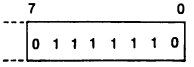
Format 8

EXT	−000	INDEX	−100
CVTP	−001	FFS	−101
INS	−010		
CHECK	−011		
MOVSU	−110, reg=001		
MOVUS	−110, reg=011		



Format 9

MOVif	−000	ROUND	−100
LFSR	−001	TRUNC	−101
MOVLF	−010	SFSR	−110
MOVFL	−011	FLOOR	−111



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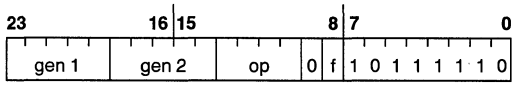
Format 10

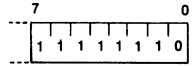
Trap (UND) Always

Appendix A: Instruction Formats (Continued)



Format 11

ADDf	−0000	DIVf	−1000
MOVf	−0001	Trap (SLAVE)	−1001
CMPf	−0010	Trap (UND)	−1010
Trap (SLAVE)	−0011	Trap (UND)	−1011
SUBf	−0100	MULf	−1100
NEGf	−0101	ABSf	−1101
Trap (UND)	−0110	Trap (UND)	−1110
Trap (UND)	−0111	Trap (UND)	−1111



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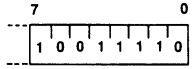
Format 12

Trap (UND) Always



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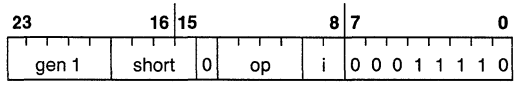
Format 13

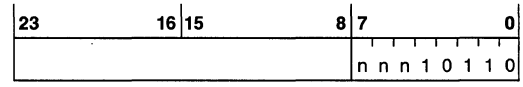
Trap (UND) Always



Format 14

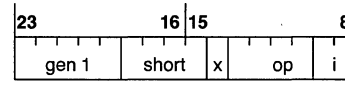
RDVAL	−0000	LMR	−0010
WRVAL	−0001	SMR	−0011

Trap (UND) on 01XX, 1XXX



Format 15 (Custom Slave)

nnn **Operation Word Format**

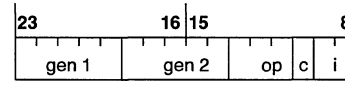


000

Format 15.0

CATST0	−0000	LCR	−0010
CATST1	−0001	SCR	−0011

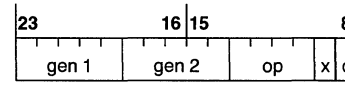
Trap (UND) on all others



001

Format 15.1

CCV3	−000	CCV2	−100
LCSR	−001	CCV1	−101
CCV5	−010	SCSR	−110
CCV4	−011	CCV0	−111



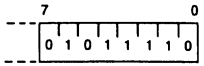
101

Format 15.5

CCAL0	−0000	CCAL3	−1000
CMOV0	−0001	CMOV3	−1001
CCMP0	−0010	Trap (UND)	−1010
CCMP1	−0011	Trap (UND)	−1011
CCAL1	−0100	CCAL2	−1100
CMOV2	−0101	CMOV1	−1101
Trap (UND)	−0110	Trap (UND)	−1110
Trap (UND)	−0111	Trap (UND)	−1111

If nnn = 010, 011, 100, 110, 111
then Trap (UND) Always

Appendix A: Instruction Formats (Continued)



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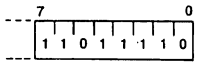
Format 16

Trap (UND) Always



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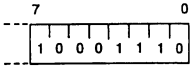
Format 17

Trap (UND) Always



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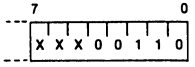
Format 18

Trap (UND) Always



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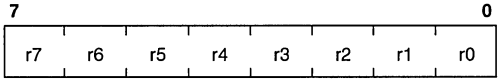
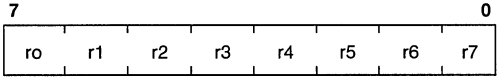
Format 19

Trap (UND) Always

Implied Immediate Encodings:



Register Mask, appended to SAVE, ENTER



Register Mask, appended to RESTORE, EXIT

Offset/Length Modifier appended to INSS, EXTS

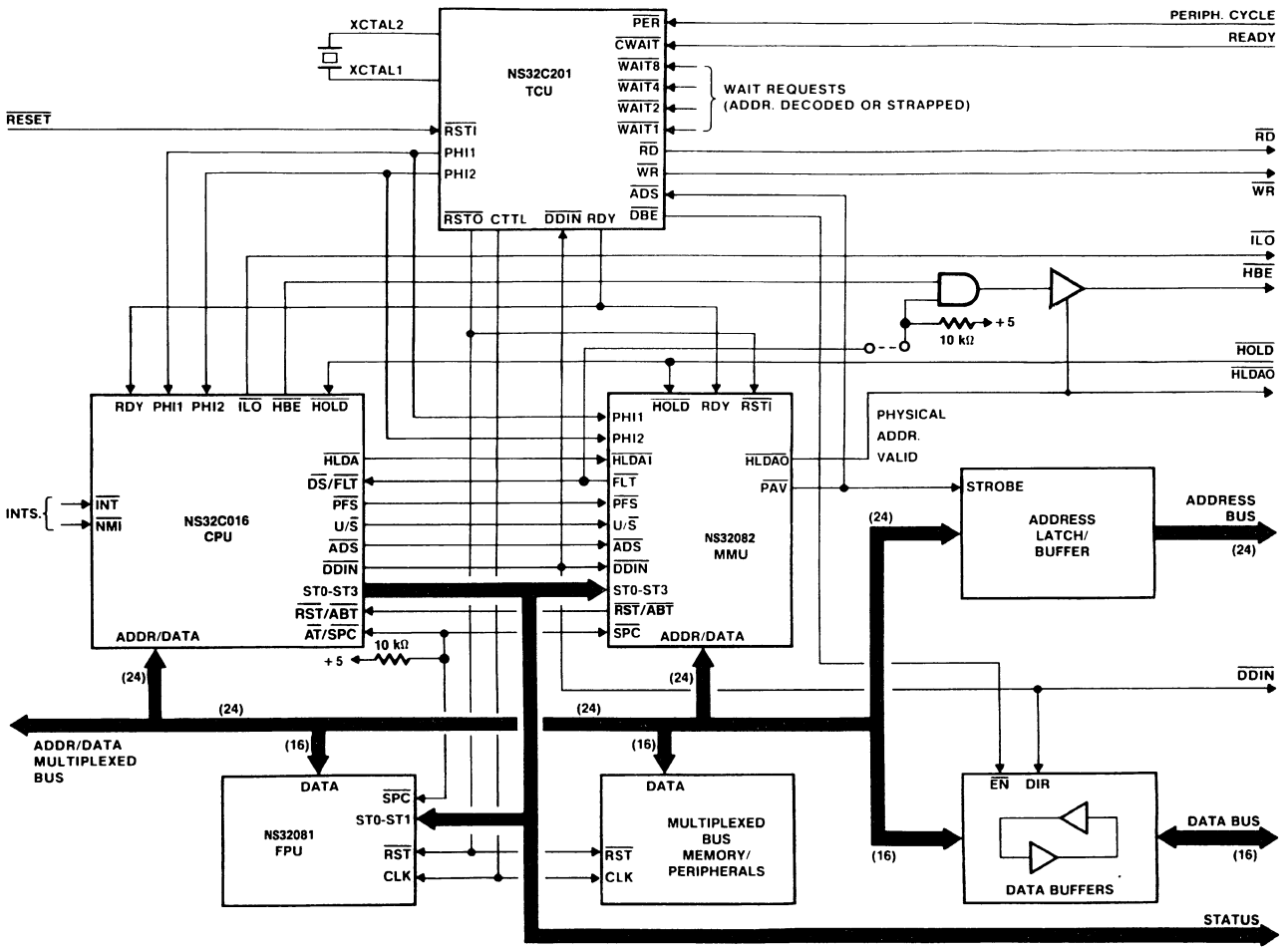


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FIGURE B-1. System Connection Diagram

National Semiconductor

PRELIMINARY

NS32016-10 High-Performance Microprocessor

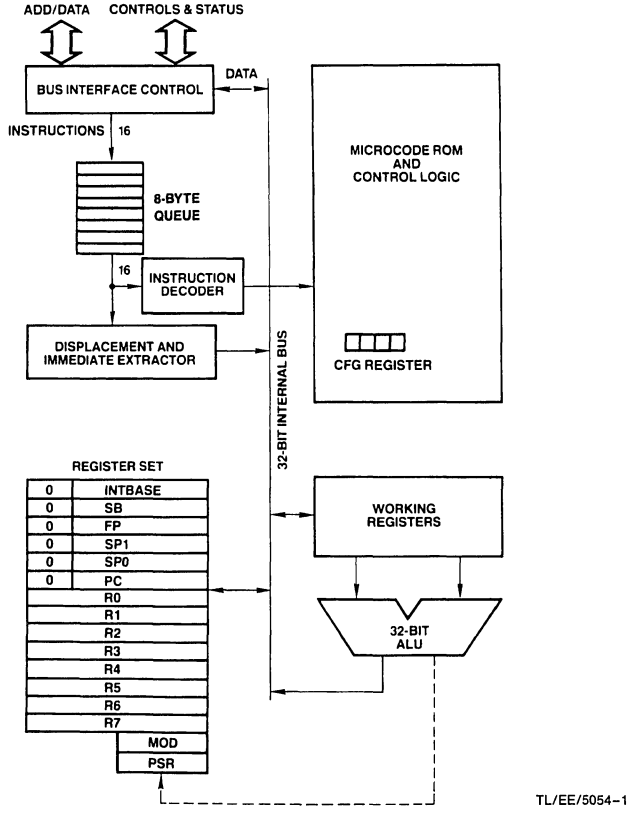
General Description

The NS32016 is a 32-bit, virtual memory microprocessor with a 16-MByte linear address space and a 16-bit external data bus. It has a 32-bit ALU, eight 32-bit general purpose registers, an eight-byte prefetch queue, and a slave processor interface. The NS32016 is fabricated with National Semiconductor's advanced XMOS process, and is fully object code compatible with other Series 32000 processors. The Series 32000 instructions set is optimized for modular high-level languages (HLL). The set is very symmetric, it has a two address format, and it incorporates HLL oriented addressing modes. The capabilities of the NS32016 can be expanded with the use of the NS32081 floating point unit (FPU), and the NS32082 demand-paged virtual memory management unit (MMU). Both devices interface to the NS32016 as slave processors. The NS32016 is a general purpose microprocessor that is ideal for a wide range of computational intensive applications.

Features

- 32-bit architecture and implementation
- Virtual memory support
- 16-MByte linear address space
- 16-bit external data bus
- Powerful instruction set
  - — General 2-address capability
  - — High degree of symmetry
  - — Addressing modes optimized for high-level languages
- Series 32000 slave processor support
- High-speed XMOS™ technology
- 48-pin dual-in-line (DIP) package

Block Diagram



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List of Tables

1.0 Product Introduction

The Series 32000 Microprocessor family is a new generation of devices using National's XMOS and CMOS technologies. By combining state-of-the-art MOS technology with a very advanced architectural design philosophy, this family brings mainframe computer processing power to VLSI processors.

The Series 32000 family supports a variety of system configurations, extending from a minimum low-cost system to a powerful 4 gigabyte system. The architecture provides complete upward compatibility from one family member to another. The family consists of a selection of CPUs supported by a set of peripherals and slave processors that provide sophisticated interrupt and memory management facilities as well as high-speed floating-point operations. The architectural features of the Series 32000 family are described briefly below:

Powerful Addressing Modes: Nine addressing modes available to all instructions are included to access data structures efficiently.

Data Types: The architecture provides for numerous data types, such as byte, word, doubleword, and BCD, which may be arranged into a wide variety of data structures.

Symmetric Instruction Set: While avoiding special case instructions that compilers can't use, the Series 32000 family incorporates powerful instructions for control operations, such as array indexing and external procedure calls, which save considerable space and time for compiled code.

Memory-to-Memory Operations: The Series 32000 CPUs represent two-address machines. This means that each operand can be referenced by any one of the addressing modes provided. This powerful memory-to-memory architecture permits memory locations to be treated as registers for all useful operations. This is important for temporary operands as well as for context switching.

Memory Management: Either the NS32382 or the NS32082 Memory Management Unit may be added to the system to provide advanced operating system support functions, including dynamic address translation, virtual memory management, and memory protection.

Large, Uniform Addressing: The NS32016 has 24-bit address pointers that can address up to 16 megabytes without requiring any segmentation; this addressing scheme provides flexible memory management without added-on expense.

Modular Software Support: Any software package for the Series 32000 family can be developed independent of all other packages, without regard to individual addressing. In addition, ROM code is totally relocatable and easy to access, which allows a significant reduction in hardware and software cost.

Software Processor Concept: The Series 32000 architecture allows future expansions of the instruction set that can be executed by special slave processors, acting as extensions to the CPU. This concept of slave processors is unique to the Series 32000 family. It allows software compatibility even for future components because the slave hardware is transparent to the software. With future advances in semiconductor technology, the slaves can be physically integrated on the CPU chip itself.

To summarize, the architectural features cited above provide three primary performance advantages and characteristics:

- High-Level Language Support
- Easy Future Growth Path
- Application Flexibility

2.0 Architectural Description

2.1 PROGRAMMING MODEL

The Series 32000 architecture includes 16 registers on the NS32016 CPU.

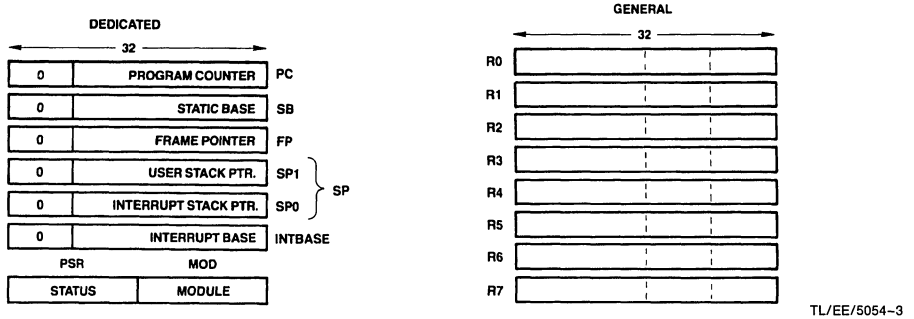

FIGURE 2-1. The General and Dedicated Registers

2.1.1 General Purpose Registers

There are eight registers for meeting high speed general storage requirements, such as holding temporary variables and addresses. The general purpose registers are free for any use by the programmer. They are thirty-two bits in length. If a general register is specified for an operand that is eight or sixteen bits long, only the low part of the register is used; the high part is not referenced or modified.

2.0 Architectural Description (Continued)

2.1.2 Dedicated Registers

The eight dedicated registers of the NS32016 are assigned specific functions.

PC: The PROGRAM COUNTER register is a pointer to the first byte of the instruction currently being executed. The PC is used to reference memory in the program section. (In the NS32016 the upper eight bits of this register are always zero.)

SP0, SP1: The SP0 register points to the lowest address of the last item stored on the INTERRUPT STACK. This stack is normally used only by the operating system. It is used primarily for storing temporary data, and holding return information for operating system subroutines and interrupt and trap service routines. The SP1 register points to the lowest address of the last item stored on the USER STACK. This stack is used by normal user programs to hold temporary data and subroutine return information.

In this document, reference is made to the SP register. The terms "SP register" or "SP" refer to either SP0 or SP1, depending on the setting of the S bit in the PSR register. If the S bit in the PSR is 0 then SP refers to SP0. If the S bit in the PSR is 1 then SP refers to SP1. (In the NS32016 the upper eight bits of these registers are always zero.)

Stacks in the Series 32000 family grow downward in memory. A Push operation pre-decrements the Stack Pointer by the operand length. A Pop operation post-increments the Stack Pointer by the operand length.

FP: The FRAME POINTER register is used by a procedure to access parameters and local variables on the stack. The FP register is set up on procedure entry with the ENTER instruction and restored on procedure termination with the EXIT instruction.

The frame pointer holds the address in memory occupied by the old contents of the frame pointer. (In the NS32016 the upper eight bits of this register are always zero.)

SB: The STATIC BASE register points to the global variables of a software module. This register is used to support relocatable global variables for software modules. The SB register holds the lowest address in memory occupied by the global variables of a module. (In the NS32016 the upper eight bits of this register are always zero.)

INTBASE: The INTERRUPT BASE register holds the address of the dispatch table for interrupts and traps (Section 3.8). The INTBASE register holds the lowest address in memory occupied by the dispatch table. (In the NS32016 the upper eight bits of this register are always zero.)

MOD: The MODULE register holds the address of the module descriptor of the currently executing software module. The MOD register is sixteen bits long, therefore the module table must be contained within the first 64K bytes of memory.

PSR: The PROCESSOR STATUS REGISTER (PSR) holds the status codes for the NS32016 microprocessor.

The PSR is sixteen bits long, divided into two eight-bit halves. The low order eight bits are accessible to all programs, but the high order eight bits are accessible only to programs executing in Supervisor Mode.

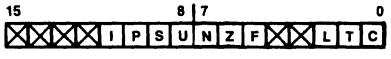

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FIGURE 2-2. Processor Status Register

C: The C bit indicates that a carry or borrow occurred after an addition or subtraction instruction. It can be used with the ADDC and SUBC instructions to perform multiple-precision integer arithmetic calculations. It may have a setting of 0 (no carry or borrow) or 1 (carry or borrow).

T: The T bit causes program tracing. If this bit is a 1, a TRC trap is executed after every instruction (Section 3.8.5).

L: The L bit is altered by comparison instructions. In a comparison instruction the L bit is set to "1" if the second operand is less than the first operand, when both operands are interpreted as unsigned integers. Otherwise, it is set to "0". In Floating Point comparisons, this bit is always cleared.

F: The F bit is a general condition flag, which is altered by many instructions (e.g., integer arithmetic instructions use it to indicate overflow).

Z: The Z bit is altered by comparison instructions. In a comparison instruction the Z bit is set to "1" if the second operand is equal to the first operand; otherwise it is set to "0".

N: The N bit is altered by comparison instructions. In a comparison instruction the N bit is set to "1" if the second operand is less than the first operand, when both operands are interpreted as signed integers. Otherwise, it is set to "0".

U: If the U bit is "1" no privileged instructions may be executed. If the U bit is "0" then all instructions may be executed. When U=0 the NS32016 is said to be in Supervisor Mode; when U=1 the NS32016 is said to be in User Mode. A User Mode program is restricted from executing certain instructions and accessing certain registers which could interfere with the operating system. For example, a User Mode program is prevented from changing the setting of the flag used to indicate its own privilege mode. A Supervisor Mode program is assumed to be a trusted part of the operating system, hence it has no such restrictions.

S: The S bit specifies whether the SP0 register or SP1 register is used as the stack pointer. The bit is automatically cleared on interrupts and traps. It may have a setting of 0 (use the SP0 register) or 1 (use the SP1 register).

P: The P bit prevents a TRC trap from occurring more than once for an instruction (Section 3.8.5). It may have a setting of 0 (no trace pending) or 1 (trace pending).

I: If I=1, then all interrupts will be accepted (Section 3.8). If I=0, only the NMI interrupt is accepted. Trap enables are not affected by this bit.

2.1.3 The Configuration Register (CFG)

Within the Control section of the NS32016 CPU is the four-bit CFG Register, which declares the presence of certain external devices. It is referenced by only one instruction, SETCFG, which is intended to be executed only as part of system initialization after reset. The format of the CFG Register is shown in *Figure 2-3.*

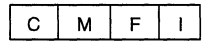


FIGURE 2-3. CFG Register

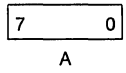
The CFG I bit declares the presence of external interrupt vectoring circuitry (specifically, the NS32202 Interrupt Control Unit). If the CFG I bit is set, interrupts requested through the $\overline{INT}$ pin are "Vectored." If it is clear, these interrupts are "Non-Vectored." See Section 3.8.

The F, M and C bits declare the presence of the FPU, MMU and Custom Slave Processors. If these bits are not set, the corresponding instructions are trapped as being undefined.

2.0 Architectural Description (Continued)

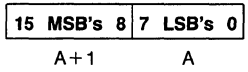
2.1.4 Memory Organization

The main memory of the NS32016 is a uniform linear address space. Memory locations are numbered sequentially starting at zero and ending at $2^{24} - 1$. The number specifying a memory location is called an address. The contents of each memory location is a byte consisting of eight bits. Unless otherwise noted, diagrams in this document show data stored in memory with the lowest address on the right and the highest address on the left. Also, when data is shown vertically, the lowest address is at the top of a diagram and the highest address at the bottom of the diagram. When bits are numbered in a diagram, the least significant bit is given the number zero, and is shown at the right of the diagram. Bits are numbered in increasing significance and toward the left.



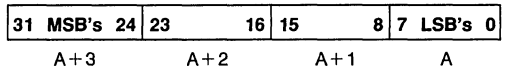
Byte at Address A

Two contiguous bytes are called a word. Except where noted (Section 2.2.1), the least significant byte of a word is stored at the lower address, and the most significant byte of the word is stored at the next higher address. In memory, the address of a word is the address of its least significant byte, and a word may start at any address.



Word at Address A

Two contiguous words are called a double word. Except where noted (Section 2.2.1), the least significant word of a double word is stored at the lowest address and the most significant word of the double word is stored at the address two greater. In memory, the address of a double word is the address of its least significant byte, and a double word may start at any address.



Double Word at Address A

Although memory is addressed as bytes, it is actually organized as words. Therefore, words and double words that are aligned to start at even addresses (multiples of two) are accessed more quickly than words and double words that are not so aligned.

2.1.5 Dedicated Tables

Two of the NS32016 dedicated registers (MOD and INTBASE) serve as pointers to dedicated tables in memory.

The INTBASE register points to the Interrupt Dispatch and Cascade tables. These are described in Section 3.8.

The MOD register contains a pointer into the Module Table, whose entries are called Module Descriptors. A Module Descriptor contains four pointers, three of which are used by the NS32016. The MOD register contains the address of the Module Descriptor for the currently running module. It is automatically updated by the Call External Procedure instructions (CXP and CXPD).

The format of a Module Descriptor is shown in *Figure 2-4*. The Static Base entry contains the address of static data assigned to the running module. It is loaded into the CPU Static Base register by the CXP and CXPD instructions. The Program Base entry contains the address of the first byte of instruction code in the module. Since a module may have multiple entry points, the Program Base pointer serves only as a reference to find them.

The Link Table Address points to the Link Table for the currently running module. The Link Table provides the information needed for:

1) Sharing variables between modules. Such variables are accessed through the Link Table via the External addressing mode.

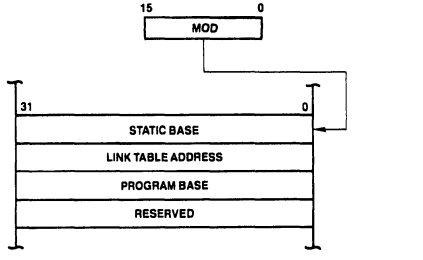


FIGURE 2-4. Module Descriptor Format

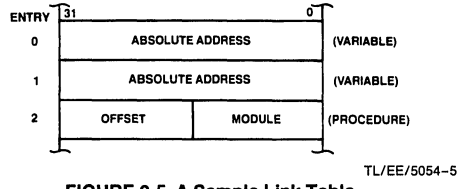


FIGURE 2-5. A Sample Link Table

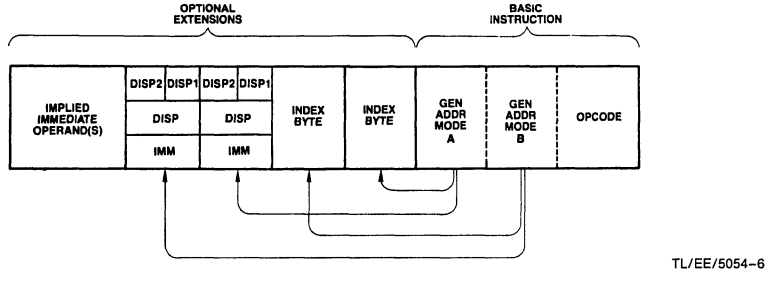


FIGURE 2-6. General Instruction Format

2.0 Architectural Description (Continued)

2) Transferring control from one module to another. This is done via the Call External Procedure (CXP) instruction.

The format of a Link Table is given in *Figure 2-5.* A Link Table Entry for an external variable contains the 32-bit address of that variable. An entry for an external procedure contains two 16-bit fields: Module and Offset. The Module field contains the new MOD register contents for the module being entered. The Offset field is an unsigned number giving the position of the entry point relative to the new module's Program Base pointer.

For further details of the functions of these tables, see the Series 32000 Instruction Set Reference Manual.

2.2 INSTRUCTION SET

2.2.1 General Instruction Format

Figure 2-6 shows the general format of a Series 32000 instruction. The Basic Instruction is one to three bytes long and contains the Opcode and up to 5-bit General Addressing Mode ("Gen") fields. Following the Basic Instruction field is a set of optional extensions, which may appear depending on the instruction and the addressing modes selected.

Index Bytes appear when either or both Gen fields specify Scaled Index. In this case, the Gen field specifies only the Scale Factor (1, 2, 4 or 8), and the Index Byte specifies which General Purpose Register to use as the index, and which addressing mode calculation to perform before indexing. See *Figure 2-7.*

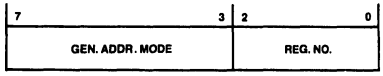


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FIGURE 2-7. Index Byte Format

Following Index Bytes come any displacements (addressing constants) or immediate values associated with the selected addressing modes. Each Disp/Imm field may contain one of two displacements, or one immediate value. The size of a Displacement field is encoded within the top bits of that field, as shown in *Figure 2-8,* with the remaining bits interpreted as a signed (two's complement) value. The size of an immediate value is determined from the Opcode field. Both Displacement and Immediate fields are stored most-significant byte first. Note that this is different from the memory representation of data (Section 2.1.4).

Some instructions require additional "implied" immediates and/or displacements, apart from those associated with addressing modes. Any such extensions appear at the end of the instruction, in the order that they appear within the list of operands in the instruction definition (Section 2.2.3).

2.2.2 Addressing Modes

The NS32016 CPU generally accesses an operand by calculating its Effective Address based on information available when the operand is to be accessed. The method to be used in performing this calculation is specified by the programmer as an "addressing mode."

Addressing modes in the NS32016 are designed to optimally support high-level language accesses to variables. In nearly all cases, a variable access requires only one addressing mode, within the instruction that acts upon that variable. Extraneous data movement is therefore minimized.

NS32016 Addressing Modes fall into nine basic types:

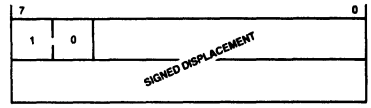
Register: The operand is available in one of the eight General Purpose Registers. In certain Slave Processor instructions, an auxiliary set of eight registers may be referenced instead.

Register Relative: A General Purpose Register contains an address to which is added a displacement value from the instruction, yielding the Effective Address of the operand in memory.

Memory Space: Identical to Register Relative above, except that the register used is one of the dedicated registers PC, SP, SB or FP. These registers point to data areas generally needed by high-level languages.

Byte Displacement: Range −64 to +63

Word Displacement: Range −8192 to +8191



Double Word Displacement: Range (Entire Addressing Space)

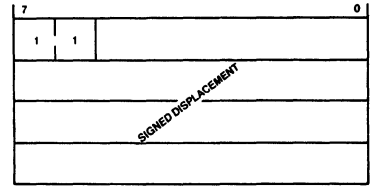


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FIGURE 2-8. Displacement Encodings

Memory Relative: A pointer variable is found within the memory space pointed to by the SP, SB or FP register. A displacement is added to that pointer to generate the Effective Address of the operand.

Immediate: The operand is encoded within the instruction. This addressing mode is not allowed if the operand is to be written.

Absolute: The address of the operand is specified by a displacement field in the instruction.

External: A pointer value is read from a specified entry of the current Link Table. To this pointer value is added a displacement, yielding the Effective Address of the operand.

Top of Stack: The currently-selected Stack Pointer (SP0 or SP1) specifies the location of the operand. The operand is pushed or popped, depending on whether it is written or read.

Scaled Index: Although encoded as an addressing mode, Scaled Indexing is an option on any addressing mode except Immediate or another Scaled Index. It has the effect of calculating an Effective Address, then multiplying any General Purpose Register by 1, 2, 4 or 8 and adding into the total, yielding the final Effective Address of the operand.

Table 2-1 is a brief summary of the addressing modes. For a complete description of their actions, see the Series 32000 Instruction Set Reference Manual.

2.0 Architectural Description (Continued)

TABLE 2-1
NS32016 Addressing Modes

ENCODING	MODE	ASSEMBLER SYNTAX	EFFECTIVE ADDRESS
Register			
00000	Register 0	R0 or F0	None: Operand is in the specified register.
00001	Register 1	R1 or F1	
00010	Register 2	R2 or F2	
00011	Register 3	R3 or F3	
00100	Register 4	R4 or F4	
00101	Register 5	R5 or F5	
00110	Register 6	R6 or F6	
00111	Register 7	R6 or F7	
Register Relative			
01000	Register 0 relative	disp(R0)	Disp + Register.
01001	Register 1 relative	disp(R1)	
01010	Register 2 relative	disp(R2)	
01011	Register 3 relative	disp(R3)	
01100	Register 4 relative	disp(R4)	
01101	Register 5 relative	disp(R5)	
01110	Register 6 relative	disp(R6)	
01111	Register 7 relative	disp(R7)	
Memory Relative			
10000	Frame memory relative	disp2(disp1 (FP))	Disp2 + Pointer; Pointer found at address Disp 1 + Register. "SP" is either SP0 or SP1, as selected in PSR.
10001	Stack memory relative	disp2(disp1 (SP))	
10010	Static memory relative	disp2(disp1 (SB))	
Reserved			
10011	(Reserved for Future Use)		
Immediate			
10100	Immediate	value	None: Operand is input from instruction queue.
Absolute			
10101	Absolute	@disp	Disp.
External			
10110	External	EXT (disp1) + disp2	Disp2 + Pointer; Pointer is found at Link Table Entry number Disp1.
Top Of Stack			
10111	Top of stack	TOS	Top of current stack, using either User or Interrupt Stack Pointer, as selected in PSR. Automatic Push/Pop included.
Memory Space			
11000	Frame memory	disp(FP)	Disp + Register; "SP" is either SP0 or SP1, as selected in PSR.
11001	Stack memory	disp(SP)	
11010	Static memory	disp(SB)	
11011	Program memory	*+ disp	
Scaled Index			
11100	Index, bytes	mode[Rn:B]	EA (mode) + Rn.
11101	Index, words	mode[Rn:W]	EA (mode) + 2×Rn.
11110	Index, double words	mode[Rn:D]	EA (mode) + 4×Rn.
11111	Index, quad words	mode[Rn:Q]	EA (mode) + 8×Rn. "Mode" and "n" are contained within the Index Byte. EA (mode) denotes the effective address generated using mode.

2.0 Architectural Description (Continued)

2.2.3 Instruction Set Summary

Table 2-2 presents a brief description of the NS32016 instruction set. The Format column refers to the Instruction Format tables (Appendix A). The Instruction column gives the instruction as coded in assembly language, and the Description column provides a short description of the function provided by that instruction. Further details of the exact operations performed by each instruction may be found in the Series 32000 Instruction Set Reference Manual.

Notations:

i = Integer length suffix: B = Byte
W = Word
D = Double Word

f = Floating Point length suffix: F = Standard Floating
L = Long Floating

gen = General operand. Any addressing mode can be specified.

short = A 4-bit value encoded within the Basic Instruction (see Appendix A for encodings).

imm = Implied immediate operand. An 8-bit value appended after any addressing extensions.

disp = Displacement (addressing constant): 8, 16 or 32 bits. All three lengths legal.

reg = Any General Purpose Register: R0-R7.

areg = Any Dedicated/Address Register: SP, SB, FP, MOD, INTBASE, PSR, US (bottom 8 PSR bits).

mreg = Any Memory Management Status/Control Register.

creg = A Custom Slave Processor Register (Implementation Dependent).

cond = Any condition code, encoded as a 4-bit field within the Basic Instruction (see Appendix A for encodings).

TABLE 2-2
NS32016 Instruction Set Summary

MOVES

Format	Operation	Operands	Description
4	MOVi	gen,gen	Move a value.
2	MOVQi	short,gen	Extend and move a signed 4-bit constant.
7	MOVMi	gen,gen,disp	Move multiple: disp bytes (1 to 16).
7	MOVZBW	gen,gen	Move with zero extension.
7	MOVZiD	gen,gen	Move with zero extension.
7	MOVXBW	gen,gen	Move with sign extension.
7	MOVXiD	gen,gen	Move with sign extension.
4	ADDR	gen,gen	Move effective address.

INTEGER ARITHMETIC

Format	Operation	Operands	Description
4	ADDi	gen,gen	Add.
2	ADDQi	short,gen	Add signed 4-bit constant.
4	ADDCi	gen,gen	Add with carry.
4	SUBi	gen,gen	Subtract.
4	SUBCi	gen,gen	Subtract with carry (borrow).
6	NEGi	gen,gen	Negate (2's complement).
6	ABSi	gen,gen	Take absolute value.
7	MULi	gen,gen	Multiply.
7	QUOi	gen,gen	Divide, rounding toward zero.
7	REMi	gen,gen	Remainder from QUO.
7	DIVi	gen,gen	Divide, rounding down.
7	MODi	gen,gen	Remainder from DIV (Modulus).
7	MEIi	gen,gen	Multiply to extended integer.
7	DEIi	gen,gen	Divide extended integer.

PACKED DECIMAL (BCD) ARITHMETIC

Format	Operation	Operands	Description
6	ADDPi	gen,gen	Add packed.
6	SUBPi	gen,gen	Subtract packed.

2.0 Architectural Description (Continued)

TABLE 2-2
NS32016 Instruction Set Summary (Continued)

INTEGER COMPARISON

Format	Operation	Operands	Description
4	CMPi	gen,gen	Compare.
2	CMPQi	short,gen	Compare to signed 4-bit constant.
7	CMPMi	gen,gen,disp	Compare multiple: disp bytes (1 to 16).

LOGICAL AND BOOLEAN

Format	Operation	Operands	Description
4	ANDi	gen,gen	Logical AND.
4	ORi	gen,gen	Logical OR.
4	BICi	gen,gen	Clear selected bits.
4	XORi	gen,gen	Logical exclusive OR.
6	COMi	gen,gen	Complement all bits.
6	NOTi	gen,gen	Boolean complement: LSB only.
2	Scondi	gen	Save condition code (cond) as a Boolean variable of size i.

SHIFTS

Format	Operation	Operands	Description
6	LSHi	gen,gen	Logical shift, left or right.
6	ASHi	gen,gen	Arithmetic shift, left or right.
6	ROTi	gen,gen	Rotate, left or right.

BITS

Format	Operation	Operands	Description
4	TBITi	gen,gen	Test bit.
6	SBITi	gen,gen	Test and set bit.
6	SBITIi	gen,gen	Test and set bit, interlocked.
6	CBITi	gen,gen	Test and clear bit.
6	CBITIi	gen,gen	Test and clear bit, interlocked.
6	IBITi	gen,gen	Test and invert bit.
8	FFSi	gen,gen	Find first set bit.

BIT FIELDS

Bit fields are values in memory that are not aligned to byte boundaries. Examples are PACKED arrays and records used in Pascal. "Extract" instructions read and align a bit field. "Insert" instructions write a bit field from an aligned source.

Format	Operation	Operands	Description
8	EXTi	reg,gen,gen,disp	Extract bit field (array oriented).
8	INSi	reg,gen,gen,disp	Insert bit field (array oriented).
7	EXTSi	gen,gen,imm,imm	Extract bit field (short form).
7	INSSi	gen,gen,imm,imm	Insert bit field (short form).
8	CVTP	reg,gen,gen	Convert to bit field pointer.

ARRAYS

Format	Operation	Operands	Description
8	CHECKi	reg,gen,gen	Index bounds check.
8	INDEXi	reg,gen,gen	Recursive indexing step for multiple-dimensional arrays.

2.0 Architectural Description (Continued)

TABLE 2-2
NS32016 Instruction Set Summary (Continued)

STRINGS

String instructions assign specific functions to the General Purpose Registers:

R4 — Comparison Value

R3 — Translation Table Pointer

R2 — String 2 Pointer

R1 — String 1 Pointer

R0 — Limit Count

Options on all string instructions are:

B (Backward): Decrement strong pointers after each step rather than incrementing.

U (Until match): End instruction if String 1 entry matches R4.

W (While match): End instruction if String 1 entry does not match R4.

All string instructions end when R0 decrements to zero.

Format	Operation	Operands	Description
5	MOVSi	options	Move string 1 to string 2.
	MOVST	options	Move string, translating bytes.
5	CMPSi	options	Compare string 1 to string 2.
	CMPST	options	Compare, translating string 1 bytes.
5	SKPSi	options	Skip over string 1 entries.
	SKPST	options	Skip, translating bytes for until/while.

JUMPS AND LINKAGE

Format	Operation	Operands	Description
3	JUMP	gen	Jump.
0	BR	disp	Branch (PC Relative).
0	Bcond	disp	Conditional branch.
3	CASEi	gen	Multiway branch.
2	ACBi	short,gen,disp	Add 4-bit constant and branch if non-zero.
3	JSR	gen	Jump to subroutine.
1	BSR	disp	Branch to subroutine.
1	CXP	disp	Call external procedure
3	CXPD	gen	Call external procedure using descriptor.
1	SVC		Supervisor call.
1	FLAG		Flag trap.
1	BPT		Breakpoint trap.
1	ENTER	[reg list], disp	Save registers and allocate stack frame (Enter Procedure).
1	EXIT	[reg list]	Restore registers and reclaim stack frame (Exit Procedure).
1	RET	disp	Return from subroutine.
1	RXP	disp	Return from external procedure call.
1	RETT	disp	Return from trap. (Privileged)
1	RETI		Return from interrupt. (Privileged)

CPU REGISTER MANIPULATION

Format	Operation	Operands	Description
1	SAVE	[reg list]	Save general purpose registers.
1	RESTORE	[reg list]	Restore general purpose registers.
2	LPRi	areg,gen	Load dedicated register. (Privileged if PSR or INTBASE)
2	SPRi	areg,gen	Store dedicated register. (Privileged if PSR or INTBASE)
3	ADJSPi	gen	Adjust stack pointer.
3	BISPSRi	gen	Set selected bits in PSR. (Privileged if not Byte length)
3	BICPSRi	gen	Clear selected bits in PSR. (Privileged if not Byte length)
5	SETCFG	[option list]	Set configuration register. (Privileged)

2.0 Architectural Description (Continued)

TABLE 2-2
NS32016 Instruction Set Summary (Continued)

FLOATING POINT

Format	Operation	Operands	Description
11	MOVf	gen,gen	Move a floating point value.
9	MOVLF	gen,gen	Move and shorten a long value to standard.
9	MOVFL	gen,gen	Move and lengthen a standard value to long.
9	MOVif	gen,gen	Convert any integer to standard or long floating.
9	ROUNDfi	gen,gen	Convert to integer by rounding.
9	TRUNCfi	gen,gen	Convert to integer by truncating, toward zero.
9	FLOORfi	gen,gen	Convert to largest integer less than or equal to value.
11	ADDf	gen,gen	Add.
11	SUBf	gen,gen	Subtract.
11	MULf	gen,gen	Multiply.
11	DIVf	gen,gen	Divide.
11	CMPf	gen,gen	Compare.
11	NEGf	gen,gen	Negate.
11	ABSf	gen,gen	Take absolute value.
9	LFSR	gen	Load FSR.
9	SFSR	gen	Store FSR.

MEMORY MANAGEMENT

Format	Operation	Operands	Description
14	LMR	mreg,gen	Load memory management register. (Privileged)
14	SMR	mreg,gen	Store memory management register. (Privileged)
14	RDVAL	gen	Validate address for reading. (Privileged)
14	WRVAL	gen	Validate address for writing. (Privileged)
8	MOVSUi	gen,gen	Move a value from supervisor space to user space. (Privileged)
8	MOVUSi	gen,gen	Move a value from user space to supervisor space. (Privileged)

MISCELLANEOUS

Format	Operation	Operands	Description
1	NOP		No operation.
1	WAIT		Wait for interrupt.
1	DIA		Diagnose. Single-byte "Branch to Self" for hardware breakpointing. Not for use in programming.

CUSTOM SLAVE

Format	Operation	Operands	Description
15.5	CCAL0c	gen,gen	Custom calculate.
15.5	CCAL1c	gen,gen	
15.5	CCAL2c	gen,gen	
15.5	CCAL3c	gen,gen	
15.5	CMOV0c	gen,gen	Custom move.
15.5	CMOV1c	gen,gen	
15.5	CMOV2c	gen,gen	
15.5	CMOV3c	gen,gen	
15.5	CCMP0c	gen,gen	Custom compare.
15.5	CCMP1c	gen,gen	
15.1	CCV0ci	gen,gen	Custom convert.
15.1	CCV1ci	gen,gen	
15.1	CCV2ci	gen,gen	
15.1	CCV3ic	gen,gen	
15.1	CCV4DQ	gen,gen	
15.1	CCV5QD	gen,gen	
15.1	LCSR	gen	Load custom status register.
15.1	SCSR	gen	Store custom status register.
15.0	CATST0	gen	Custom address/test. (Privileged)
15.0	CATST1	gen	(Privileged)
15.0	LCR	creg,gen	Load custom register. (Privileged)
15.0	SCR	creg,gen	Store custom register. (Privileged)

3.0 Functional Description

3.1 POWER AND GROUNDING

The NS32016 requires a single 5-volt power supply, applied on pin 48 (V_{CC}).

Grounding connections are made on two pins. Logic Ground (GNDL, pin 24) is the common pin for on-chip logic, and Buffer Ground (GNDB, pin 25) is the common pin for the output drivers. For optimal noise immunity, it is recommended that GNDL be attached through a single conductor directly to GNDB, and that all other grounding connections be made only to GNDB, as shown below (*Figure 3-1*).

In addition to V_{CC} and Ground, the NS32016 CPU uses an internally-generated negative voltage. It is necessary to filter this voltage externally by attaching a pair of capacitors (*Figure 3-1*) from the BBG pin to ground. Recommended values of these are:

C_1: 1 μF, Tantalum.

C_2: 1000 pF, low inductance. This should be either a disc or monolithic ceramic capacitor.

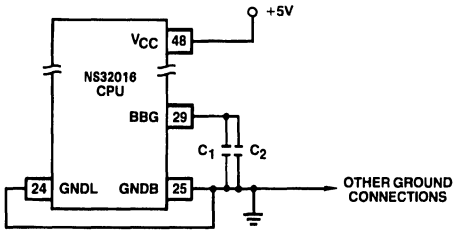

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FIGURE 3-1. Recommended Supply Connections

3.2 CLOCKING

The NS32016 inputs clocking signals from the NS32201 Timing Control Unit (TCU), which presents two non-overlapping phases of a single clock frequency. These phases are called PHI1 (pin 26) and PHI2 (pin 27). Their relationship to each other is shown in *Figure 3-2.*

Each rising edge of PHI1 defines a transition in the timing state ("T-State") of the CPU. One T-State represents the execution of one microinstruction within the CPU, and/or one step of an external bus transfer. See Section 4 for complete specifications of PHI1 and PHI2.

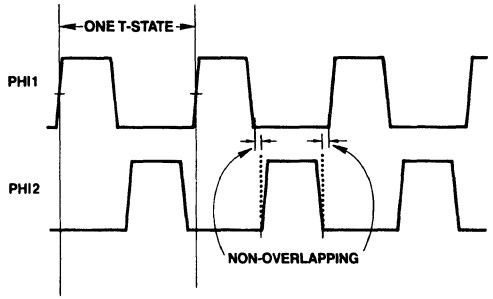

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FIGURE 3-2. Clock Timing Relationships

As the TCU presents signals with very fast transitions, it is recommended that the conductors carrying PHI1 and PHI2 be kept as short as possible, and that they not be connected anywhere except from the TCU to the CPU and, if present, the MMU. A TTL Clock signal (CTTL) is provided by the TCU for all other clocking.

3.3 RESETTING

The $\overline{RST}/\overline{ABT}$ pin serves both as a Reset for on-chip logic and as the Abort input for Memory-Managed systems. For its use as the Abort Command, see Section 3.5.4.

The CPU may be reset at any time by pulling the $\overline{RST}/\overline{ABT}$ pin low for at least 64 clock cycles. Upon detecting a reset, the CPU terminates instruction processing, resets its internal logic, and clears the Program Counter (PC) and Processor Status Register (PSR) to all zeroes.

On application of power, $\overline{RST}/\overline{ABT}$ must be held low for at least 50 μs after V_{CC} is stable. This is to ensure that all on-chip voltages are completely stable before operation. Whenever a Reset is applied, it must also remain active

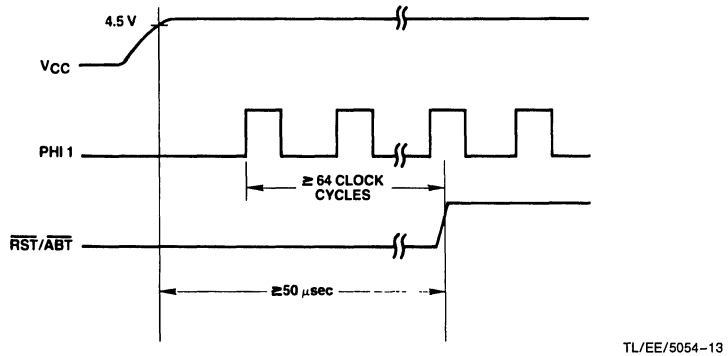

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FIGURE 3-3. Power-On Reset Requirements

3.0 Functional Description (Continued)

for not less than 64 clock cycles. The rising edge must occur while PHI1 is high. See *Figures 3-3* and *3-4.*

The NS32201 Timing Control Unit (TCU) provides circuitry to meet the Reset requirements of the NS32016 CPU. *Figure 3-5a* shows the recommended connections for a non-Memory-Managed system. *Figure 3-5b* shows the connections for a Memory-Managed system.

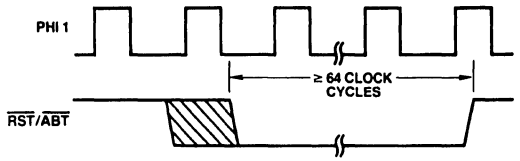

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FIGURE 3-4. General Reset Timing

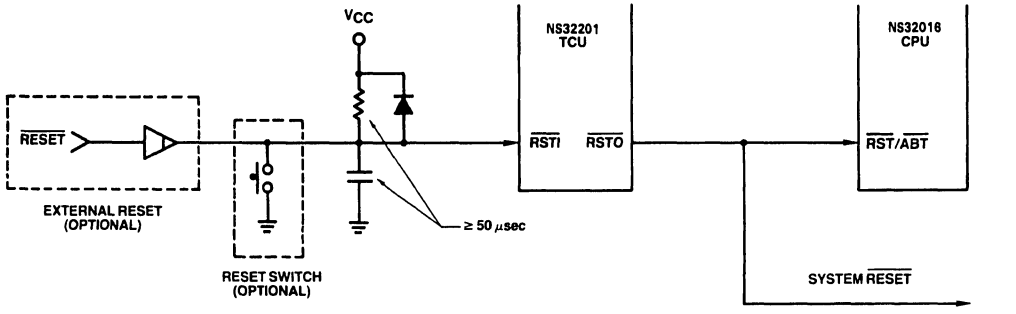

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FIGURE 3-5a. Recommended Reset Connections, Non-Memory-Managed System

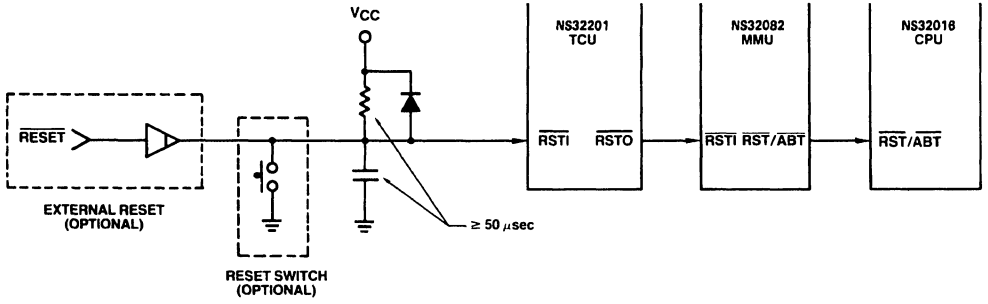

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FIGURE 3-5b. Recommended Reset Connections, Memory-Managed System

3.4 BUS CYCLES

The NS32016 CPU has a strap option which defines the Bus Timing Mode as either With or Without Address Translation. This section describes only bus cycles under the No Address Translation option. For details of the use of the strap and of bus cycles with address translation, see Section 3.5.

The CPU will perform a bus cycle for one of the following reasons:

1) To write or read data, to or from memory or a peripheral interface device. Peripheral input and output are memory-mapped in the Series 32000 family.
2) To fetch instructions into the eight-byte instruction queue. This happens whenever the bus would otherwise be idle and the queue is not already full.
3) To acknowledge an interrupt and allow external circuitry to provide a vector number, or to acknowledge completion of an interrupt service routine.
4) To transfer information to or from a Slave Processor.

In terms of bus timing, cases 1 through 3 above are identical. For timing specifications, see Section 4. The only external difference between them is the four-bit code placed on the Bus Status pins (ST0-ST3). Slave Processor cycles differ in that separate control signals are applied (Section 3.4.6).

The sequence of events in a non-Slave bus cycle is shown in *Figure 3-7* for a Read cycle and *Figure 3-8* for a Write cycle. The cases shown assume that the selected memory or interface device is capable of communicating with the CPU at full speed. If it is not, then cycle extension may be requested through the RDY line (Section 3.4.1).

3.0 Functional Description (Continued)

A full-speed bus cycle is performed in four cycles of the PHI1 clock signal, labeled T1 through T4. Clock cycles not associated with a bus cycle are designated Ti (for "Idle").

During T1, the CPU applies an address on pins AD0–AD15 and A16–A23. It also provides a low-going pulse on the $\overline{ADS}$ pin, which serves the dual purpose of informing external circuitry that a bus cycle is starting and of providing control to an external latch for demultiplexing Address bits 0–15 from the AD0–AD15 pins. See *Figure 3-6*. During this time also the status signals $\overline{DDIN}$, indicating the direction of the transfer, and $\overline{HBE}$, indicating whether the high byte (AD8–AD15) is to be referenced, become valid.

During T2 the CPU switches the Data Bus, AD0–AD15, to either accept or present data. Note that the signals A16–A23 remain valid, and need not be latched. It also starts the data strobe ($\overline{DS}$), signaling the beginning of the data transfer. Associated signals from the NS32201 Timing Control Unit are also activated at this time: $\overline{RD}$ (Read Strobe) or $\overline{WR}$ (Write Strobe), $\overline{TSO}$ (Timing State Output, indicating that T2 has been reached) and $\overline{DBE}$ (Data Buffer Enable).

The T3 state provides for access time requirements, and it occurs at least once in a bus cycle. At the end of T2 or T3, on the falling edge of the PHI2 clock, the RDY (Ready) line is sampled to determine whether the bus cycle will be extended (Section 3.4.1).

If the CPU is performing a Read cycle, the Data Bus (AD0–AD15) is sampled at the falling edge of PHI2 of the last T3 state. See Section 4. Data must, however, be held at least until the beginning of T4. $\overline{DS}$ and $\overline{RD}$ are guaranteed not to go inactive before this point, so the rising edge of either of them may safely be used to disable the device providing the input data.

The T4 state finishes the bus cycle. At the beginning of T4, the $\overline{DS}$, $\overline{RD}$, or $\overline{WR}$, and $\overline{TSO}$ signals go inactive, and at the rising edge of PHI2, $\overline{DBE}$ goes inactive, having provided for necessary data hold times. Data during Write cycles remains valid from the CPU throughout T4. Note that the Bus Status lines (ST0–ST3) change at the beginning of T4, anticipating the following bus cycle (if any).

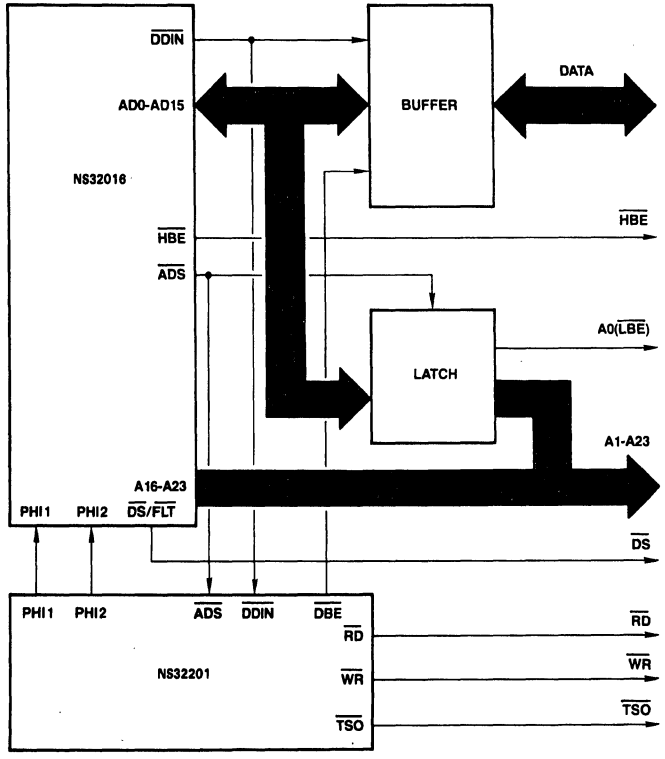

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FIGURE 3-6. Bus Connections

3.0 Functional Description (Continued)

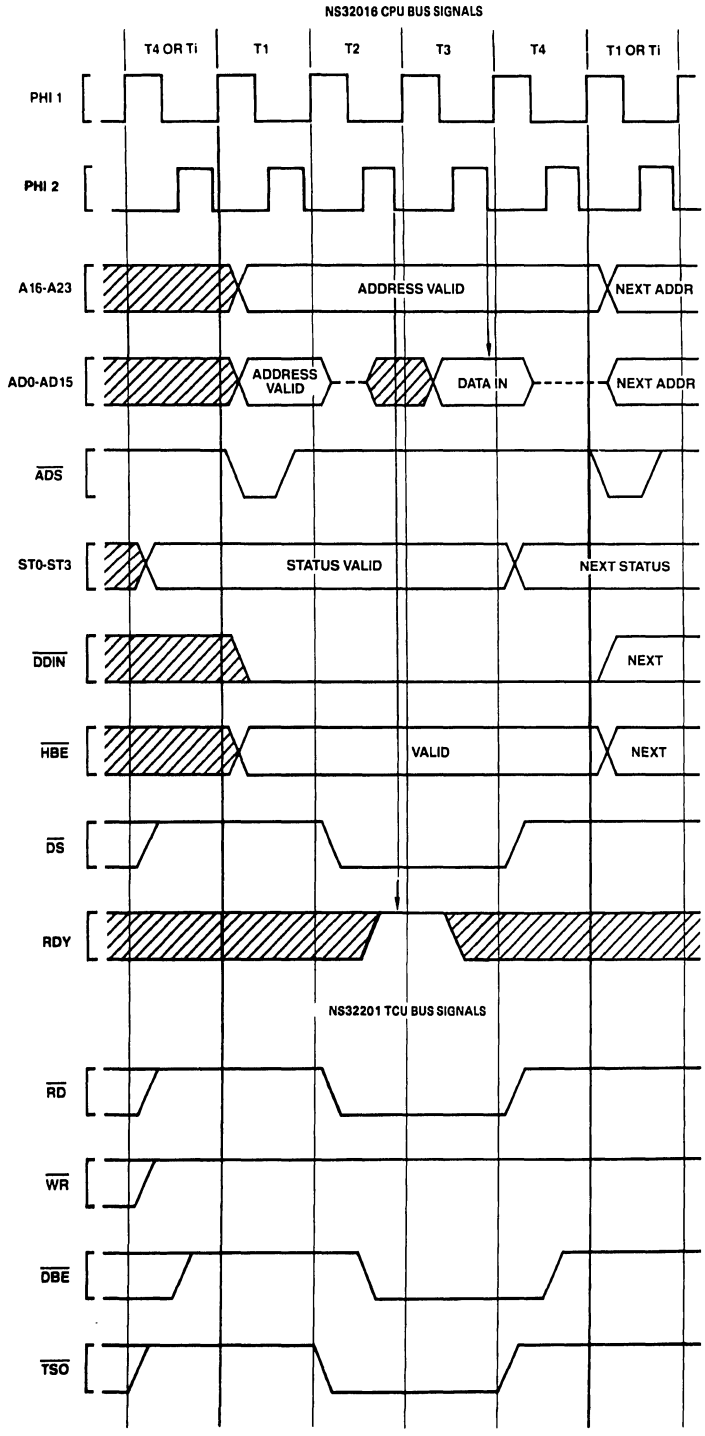

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FIGURE 3-7. Read Cycle Timing

3.0 Functional Description (Continued)

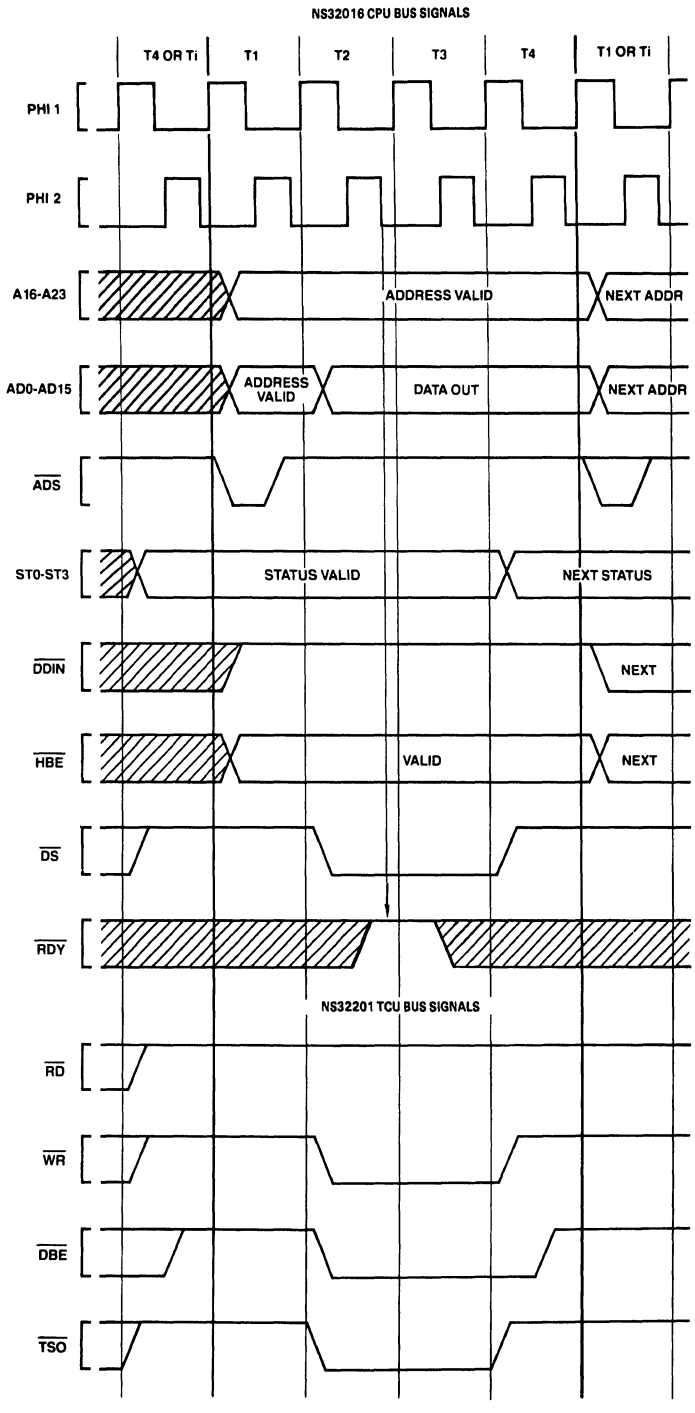

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FIGURE 3-8. Write Cycle Timing

3.0 Functional Description (Continued)

3.4.1 Cycle Extension

To allow sufficient strobe widths and access times for any speed of memory or peripheral device, the NS32016 provides for extension of a bus cycle. Any type of bus cycle except a Slave Processor cycle can be extended.

In *Figures 3-7* and *3-8*, note that during T3 all bus control signals from the CPU and TCU are flat. Therefore, a bus cycle can be cleanly extended by causing the T3 state to be repeated. This is the purpose of the RDY (Ready) pin.

At the end of T2 on the falling edge of PHI2, the RDY line is sampled by the CPU. If RDY is high, the next T-states will be T3 and then T4, ending the bus cycle. If it is sampled low, then another T3 state will be inserted after the next T-state and the RDY line will again be sampled on the falling edge of PHI2. Each additional T3 state after the first is referred to as a "wait state." See *Figure 3-9.*

The RDY pin is driven by the NS32201 Timing Control Unit, which applies WAIT States to the CPU as requested on three sets of pins:

1) $\overline{\text{CWAIT}}$ (Continues WAIT), which holds the CPU in WAIT states until removed.
2) $\overline{\text{WAIT1}}$, $\overline{\text{WAIT2}}$, $\overline{\text{WAIT4}}$, $\overline{\text{WAIT8}}$ (Collectively $\overline{\text{WAIT}}$n), which may be given a four-bit binary value requesting a specific number of WAIT States from 0 to 15.
3) $\overline{\text{PER}}$ (Peripheral), which inserts five additional WAIT states and causes the TCU to reshape the $\overline{\text{RD}}$ and $\overline{\text{WR}}$ strobes. This provides the setup and hold times required by most MOS peripheral interface devices.

Combinations of these various WAIT requests are both legal and useful. For details of their use, see the NS32201 TCU Data Sheet.

Figure 3-10 illustrates a typical Read cycle, with two WAIT states requested through the TCU $\overline{\text{WAIT}}$n pins.

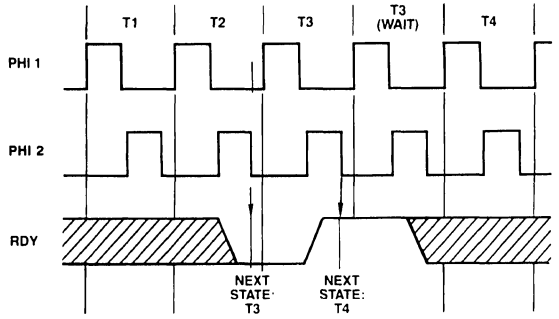

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FIGURE 3-9. RDY Pin Timing

3.4.2 Bus Status

The NS32016 CPU presents four bits of Bus Status information on pins ST0–ST3. The various combinations on these pins indicate why the CPU is performing a bus cycle, or, if it is idle on the bus, then why it is idle.

Referring to *Figures 3-7* and *3-8,* note that Bus Status leads the corresponding Bus Cycle, going valid one clock cycle before T1, and changing to the next state at T4. This allows the system designer to fully decode the Bus Status and, if desired, latch the decoded signals before $\overline{\text{ADS}}$ initiates the Bus Cycle.

The Bus Status pins are interpreted as a four-bit value, with ST0 the least significant bit. Their values decode as follows:

0000 — The bus is idle because the CPU does not need to perform a bus access.

0001 — The bus is idle because the CPU is executing the WAIT instruction.

0010 — (Reserved for future use.)

0011 — The bus is idle because the CPU is waiting for a Slave Processor to complete an instruction.

0100 — Interrupt Acknowledge, Master.
The CPU is performing a Read cycle. To acknowledge receipt of a Non-Maskable Interrupt (on $\overline{\text{NMI}}$) it will read from address FFFF00_{16}, but will ignore any data provided.

To acknowledge receipt of a Maskable Interrupt (on $\overline{\text{INT}}$) it will read from address FFFE00_{16}, expecting a vector number to be provided from the Master NS32202 Interrupt Control Unit. If the vectoring mode selected by the last SETCFG instruction was Non-Vectored, then the CPU will ignore the value it has read and will use a default vector instead, having assumed that no NS32202 is present. See Section 3.4.5.

0101 — Interrupt Acknowledge, Cascaded.
The CPU is reading a vector number from a Cascaded NS32202 Interrupt Control Unit. The address provided is the address of the NS32202 Hardware Vector register. See Section 3.4.5.

0110 — End of Interrupt, Master.
The CPU is performing a Read cycle to indicate that it is executing a Return from Interrupt (RETI) instruction. See Section 3.4.5.

0111 — End of Interrupt, Cascaded.
The CPU is reading from a Cascaded Interrupt Control Unit to indicate that it is returning (through RETI) from an interrupt service routine requested by that unit. See Section 3.4.5.

1000 — Sequential Instruction Fetch.
The CPU is reading the next sequential word from the instruction stream into the Instruction Queue. It will do so whenever the bus would otherwise be idle and the queue is not already full.

3.0 Functional Description (Continued)

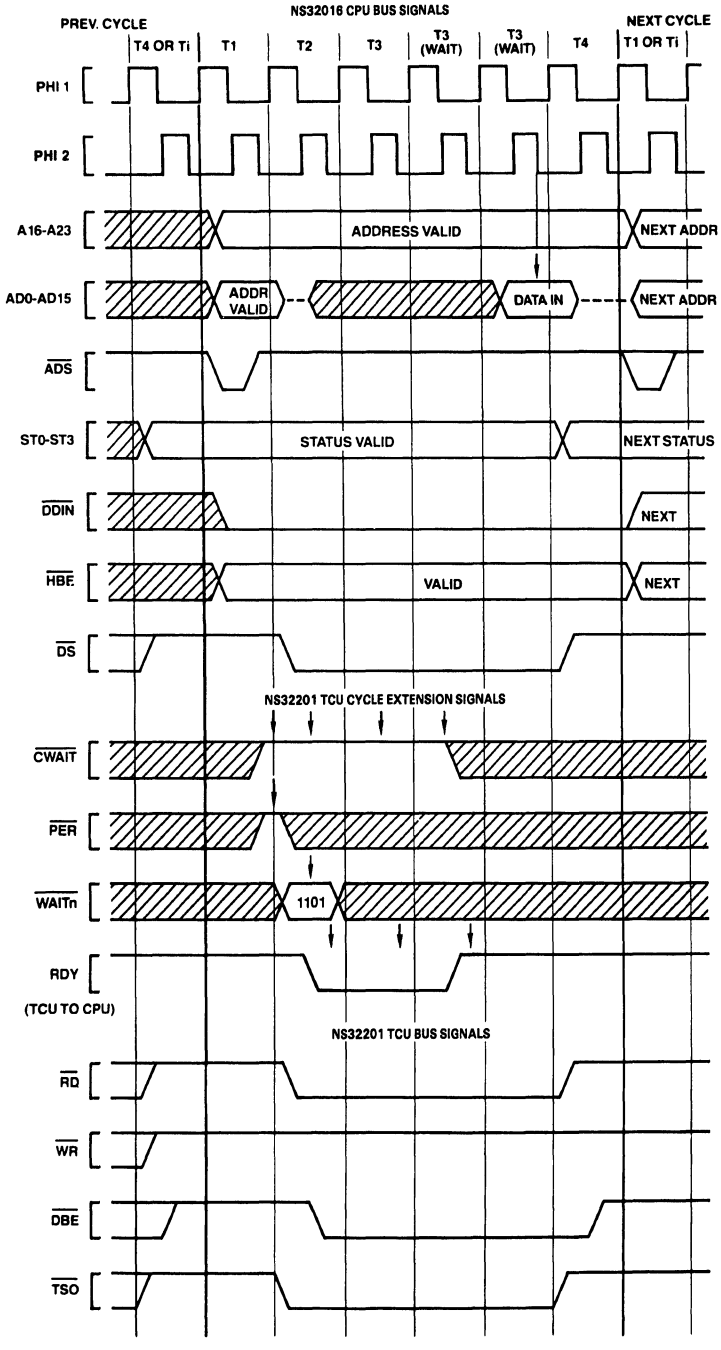

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FIGURE 3-10. Extended Cycle Example

Note: Arrows on $\overline{\text{CWAIT}}$, $\overline{\text{PER}}$, $\overline{\text{WAITn}}$ indicate points at which the TCU samples. Arrows on AD0–AD15 and RDY indicate points at which the CPU samples.

3.0 Functional Description (Continued)

1001 — Non-Sequential Instruction Fetch.
The CPU is performing the first fetch of instruction code after the Instruction Queue is purged. This will occur as a result of any jump or branch, or any interrupt or trap, or execution of certain instructions.

1010 — Data Transfer.
The CPU is reading or writing an operand of an instruction.

1011 — Read RMW Operand.
The CPU is reading an operand which will subsequently be modified and rewritten. If memory protection circuitry would not allow the following Write cycle, it must abort this cycle.

1100 — Read for Effective Address Calculation.
The CPU is reading information from memory in order to determine the Effective Address of an operand. This will occur whenever an instruction uses the Memory Relative or External addressing mode.

1101 — Transfer Slave Processor Operand.
The CPU is either transferring an instruction operand to or from a Slave Processor, or it is issuing the Operation Word of a Slave Processor instruction. See Section 3.9.1.

1110 — Read Slave Processor Status.
The CPU is reading a Status Word from a Slave Processor. This occurs after the Slave Processor has signalled completion of an instruction. The transferred word tells the CPU whether a trap should be taken, and in some instructions it presents new values for the CPU Processor Status Register bits N, Z, L or F. See Section 3.9.1.

1111 — Broadcast Slave ID.
The CPU is initiating the execution of a Slave Processor instruction. The ID Byte (first byte of the instruction) is sent to all Slave Processors, one of which will recognize it. From this point the CPU is communicating with only one Slave Processor. See Section 3.9.1.

3.4.3 Data Access Sequences

The 24-bit address provided by the NS32016 is a byte address; that is, it uniquely identifies one of up to 16,777,216 eight-bit memory locations. An important feature of the NS32016 is that the presence of a 16-bit data bus imposes no restrictions on data alignment; any data item, regardless of size, may be placed starting at any memory address. The NS32016 provides a special control signal, High Byte Enable ($\overline{HBE}$), which facilitates individual byte addressing on a 16-bit bus.

Memory is organized as two eight-bit banks, each bank receiving the word address (A1–A23) in parallel. One bank, connected to Data Bus pins AD0–AD7, is enabled to respond to even byte addresses; i.e., when the least significant address bit (A0) is low. The other bank, connected to Data Bus pins AD8–AD15, is enabled when $\overline{HBE}$ is low. See *Figure 3-11.*

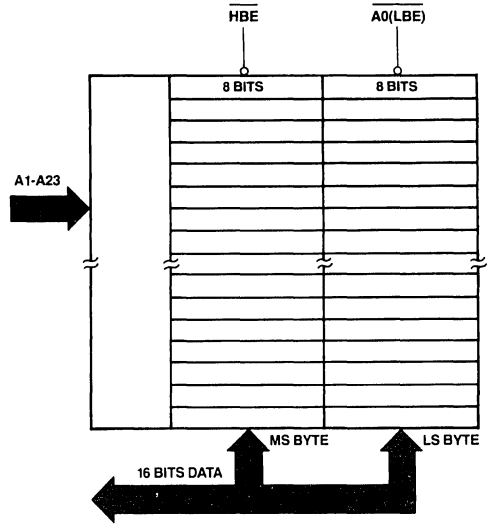

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FIGURE 3-11. Memory Interface

Any bus cycle falls into one of three categories: Even Byte Access, Odd Byte Access, and Even Word Access. All accesses to any data type are made up of sequences of these cycles. Table 3-1 gives the state of A0 and $\overline{HBE}$ for each category.

TABLE 3-1
Bus Cycle Categories

Category	$\overline{HBE}$	A0
Even Byte	1	0
Odd Byte	0	1
Even Word	0	0

Accesses of operands requiring more than one bus cycle are performed sequentially, with no idle T-States separating them. The number of bus cycles required to transfer an operand depends on its size and its alignment (i.e., whether it starts on an even byte address or an odd byte address). Table 3-2 lists the bus cycle performed for each situation. For the timing of A0 and $\overline{HBE}$, see Section 3.4.

3.0 Functional Description (Continued)

TABLE 3.2
Access Sequences

Cycle	Type	Address	$\overline{HBE}$	A0	High Bus	Low Bus
					BYTE 1	BYTE 0 ← A
1	Odd Byte	A	0	1	Byte 0	Don't Care
2	Even Byte	A+1	1	0	Don't Care	Byte 1

A. Odd Word Access Sequence

Cycle	Type	Address	$\overline{HBE}$	A0	BYTE 3	BYTE 2	BYTE 1	BYTE 0 ← A
1	Even Word	A	0	0	Byte 1	Byte 0		
2	Even Word	A+2	0	0	Byte 3	Byte 2		

B. Even Double-Word Access Sequence

Cycle	Type	Address	$\overline{HBE}$	A0	BYTE 3	BYTE 2	BYTE 1	BYTE 0 ← A
1	Odd Byte	A	0	1	Byte 0	Don't Care		
2	Even Word	A+1	0	0	Byte 2	Byte 1		
3	Even Byte	A+3	1	0	Don't Care	Byte 3		

C. Odd Double-Word Access Sequence

Cycle	Type	Address	$\overline{HBE}$	A0	BYTE 7	BYTE 6	BYTE 5	BYTE 4	BYTE 3	BYTE 2	BYTE 1	BYTE 0 ← A
1	Even Word	A	0	0	Byte 3	Byte 2	Byte 1	Byte 0				
2	Even Word	A+4	0	0	Byte 7	Byte 6	Byte 5	Byte 4				

D. Even Quad-Word Access Sequence

Cycle	Type	Address	$\overline{HBE}$	A0	BYTE 7	BYTE 6	BYTE 5	BYTE 4	BYTE 3	BYTE 2	BYTE 1	BYTE 0 ← A
1	Odd Byte	A	0	1	Byte 0	Don't Care						
2	Even Word	A+1	0	0	Byte 4	Byte 3	Byte 2	Byte 1				
3	Even Byte	A+5	1	0	Don't Care	Byte 5						

E. Odd Quad-Word Access Sequence

3.0 Functional Description (Continued)

3.4.3.1 Bit Accesses

The Bit Instructions perform byte accesses to the byte containing the designated bit. The Test and Set Bit instruction (SBIT), for example, reads a byte, alters it, and rewrites it, having changed the contents of one bit.

3.4.3.2 Bit Field Accesses

An access to a Bit Field in memory always generates a Double-Word transfer at the address containing the least significant bit of the field. The Double Word is read by an Extract instruction; an Insert instruction reads a Double Word, modifies it, and rewrites it.

3.4.3.3 Extending Multiply Accesses

The Extending Multiply Instruction (MEI) will return a result which is twice the size in bytes of the operand it reads. If the multiplicand is in memory, the most-significant half of the result is written first (at the higher address), then the least-significant half. This is done in order to support retry if this instruction is aborted.

3.4.4 Instruction Fetches

Instructions for the NS32016 CPU are "prefetched"; that is, they are input before being needed into the next available entry of the eight-byte Instruction Queue. The CPU performs two types of Instruction Fetch cycles: Sequential and Non-Sequential. These can be distinguished from each other by their differing status combinations on pins ST0–ST3 (Section 3.4.2).

A Sequential Fetch will be performed by the CPU whenever the Data Bus would otherwise be idle and the Instruction Queue is not currently full. Sequential Fetches are always Even Word Read cycles (Table 3-1).

A Non-Sequential Fetch occurs as a result of any break in the normally sequential flow of a program. Any jump or branch instruction, a trap or an interrupt will cause the next Instruction Fetch cycle to be Non-Sequential. In addition, certain instructions flush the instruction queue, causing the next instruction fetch to display Non-Sequential status. Only the first bus cycle after a break displays Non-Sequential status, and that cycle is either an Even Word Read or an Odd Byte Read, depending on whether the destination address is even or odd.

3.4.5 Interrupt Control Cycles

Activating the $\overline{\text{INT}}$ or $\overline{\text{NMI}}$ pin on the CPU will initiate one or more bus cycles whose purpose is inerrupt control rather than the transfer of instructions or data. Execution of the Return from Interrupt instruction (RETI) will also cause Interrupt Control bus cycles. These differ from instruction or data transfers only in the status presented on pins ST0–ST3. All Interrupt Control cycles are single-byte Read cycles.

This section describes only the Interrupt Control sequences associated with each interrupt and with the return from its service routine. For full details of the NS32016 interrupt structure, see Section 3.8.

3.0 Functional Description (Continued)

TABLE 3-3
Interrupt Sequences

Cycle	Status	Address	$\overline{DDIN}$	$\overline{HBE}$	A0	High Bus	Low Bus
			A. Non-Maskable Interrupt Control Sequences.				
Interrupt Acknowledge							
1	0100	$FFFF00_{16}$	0	1	0	Don't Care	Don't Care
Interrupt Return							
None: Performed through Return from Trap (RETT) instruction.							
			B. Non-Vectored Interrupt Control Sequences.				
Interrupt Acknowledge							
1	0100	$FFFE00_{16}$	0	1	0	Don't Care	Don't Care
Interrupt Return							
None: Performed through Return from Trap (RETT) instruction.							
			C. Vectored Interrupt Sequences: Non-Cascaded.				
Interrupt Acknowledge							
1	0100	$FFFE00_{16}$	0	1	0	Don't Care	Vector: Range: 0–127
Interrupt Return							
1	0110	$FFFE00_{16}$	0	1	0	Don't Care	Vector: Same as in Previous Int. Ack. Cycle
			D. Vectored Interrupt Sequences: Cascaded.				
Interrupt Acknowledge							
1	0100	$FFFE00_{16}$	0	1	0	Don't Care	Cascade Index: range −16 to −1
(The CPU here uses the Cascade Indx to find the Cascade Address.)							
2	0101	Cascade Address	0	1 or 0*	0 or 1*	Vector, range 0–255; on appropriate half of Data Bus for even/odd address	
Interrupt Return							
1	0110	$FFFE00_{16}$	0	1	0	Don't Care	Cascade Index: same as in previous Int. Ack. Cycle
(The CPU here uses the Cascade Index to find the Cascade Address.)							
2	0111	Cascade Address	0	1 or 0*	0 or 1*	Don't Care	Don't Care

* If the Cascaded ICU Address is Even (A0 is low), then the CPU applies $\overline{HBE}$ high and reads the vector number from bits 0–7 of the Data Bus.
If the address is Odd (A0 is high), then the CPU applies $\overline{HBE}$ low and reads the vector number from bits 8–15 of the Data Bus. The vector number may be in the range 0–255.

3.0 Functional Description (Continued)

3.4.6 Slave Processor Communication

In addition to its use as the Address Translation strap (Section 3.5.1), the $\overline{AT}/\overline{SPC}$ pin is used as the data strobe for Slave Processor transfers. In this role, it is referred to as Slave Processor Control ($\overline{SPC}$). In a slave processor bus cycle, data is transferred on the Data Bus (AD0–AD15), and the Status Lines ST0–ST3 are monitored by each Slave Processor in order to determine the type of transfer being performed. $\overline{SPC}$ is bidirectional, but is driven by the CPU during all Slave Processor bus cycles. See Section 3.9 for full protocol sequences.

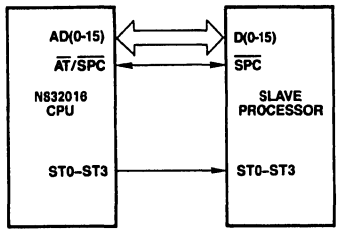

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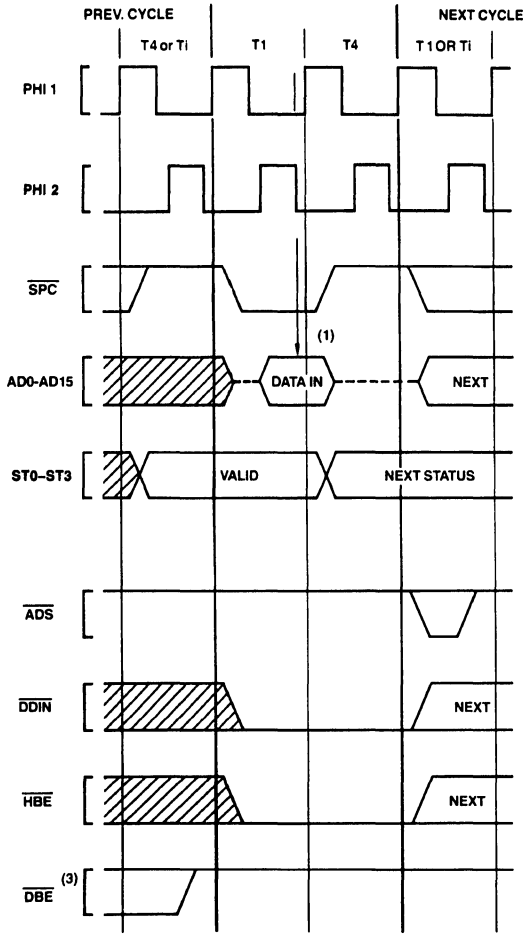
FIGURE 3-12. Slave Processor Connections



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Note:

(1) CPU samples Data Bus here.

(2) $\overline{DBE}$ and all other NS32201 TCU bus signals remain inactive because no $\overline{ADS}$ pulse is received from the CPU.

FIGURE 3-13. CPU Read from Slave Processor

3.0 Functional Description (Continued)

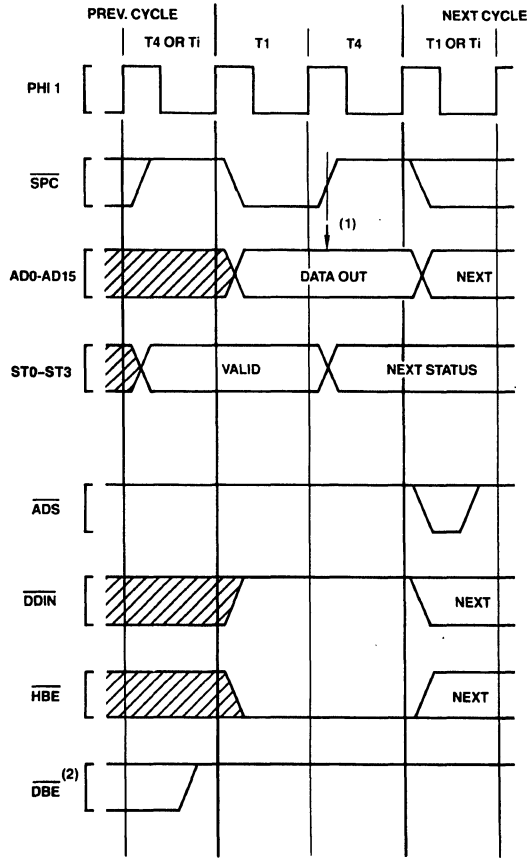
3.4.6.1 Slave Processor Bus Cycles

A Slave Processor bus cycle always takes exactly two clock cycles, labeled T1 and T4 (see *Figures 3-13* and *3-14*). During a Read cycle $\overline{SPC}$ is active from the beginning of T1 to the beginning of T4, and the data is sampled at the end of T1. The Cycle Status pins lead the cycle by one clock period, and are sampled at the leading edge of $\overline{SPC}$. During a Write cycle, the CPU applies data and activates $\overline{SPC}$ at T1, removing $\overline{SPC}$ at T4. The Slave Processor latches status on the leading edge of $\overline{SPC}$ and latches data on the trailing edge.

Since the CPU does not pulse the Address Strobe ($\overline{ADS}$), no bus signals are generated by the NS32201 Timing Control Unit. The direction of a transfer is determined by the sequence ("protocol") established by the instruction under execution; but the CPU indicates the direction on the $\overline{DDIN}$ pin for hardware debugging purposes.

3.4.6.2 Slave Operand Transfer Sequences

A Slave Processor operand is transferred in one or more Slave bus cycles. A Byte operand is transferred on the least-significant byte of the Data Bus (AD0–AD7), and a Word operand is transferred on the entire bus. A Double Word is transferred in a consecutive pair of bus cycles, least-significant word first. A Quad Word is transferred in two pairs of Slave cycles, with other bus cycles possibly occurring between them. The word order is from least-significant word to most-significant.



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Note:

(1) Slave Processor samples data bus here.

(2) $\overline{DBE}$, being provided by the NS32201 TCU, remains inactive due to the fact that no pulse is presented on $\overline{ADS}$. $\overline{TCU}$ signals $\overline{RD}$, $\overline{WR}$ and $\overline{TSO}$ also remain inactive.

FIGURE 3-14. CPU Write to Slave Processor

3.0 Functional Description (Continued)

3.5 MEMORY MANAGEMENT OPTION

The NS32016 CPU, in conjunction with the NS32082 Memory Management Unit (MMU), provides full support for address translation, memory protection, and memory allocation techniques up to and including Virtual Memory.

3.5.1 Address Translation Strap

The Bus Interface Control section of the NS32016 CPU has two bus timing modes: With or Without Address Translation. The mode of operation is selected by the CPU by sampling the $\overline{AT}/\overline{SPC}$ (Address Translation/Slave Processor Control) pin on the rising edge of the $\overline{RST}$ (Reset) pulse. If $\overline{AT}/\overline{SPC}$ is sampled as high, the bus timing is as previously described in Section 3.4. If it is sampled as low, two changes occur:

1) An extra clock cycle, Tmmu, is inserted into all bus cycles except Slave Processor transfers.
2) The $\overline{DS}/\overline{FLT}$ pin changes in function from a Data Strobe output ($\overline{DS}$) to a Float Command input ($\overline{FLT}$).

The NS32082 MMU will itself pull the CPU $\overline{AT}/\overline{SPC}$ pin low when it is reset. In non-Memory-Managed systems this pin should be pulled up to V_{CC} through a 10 kΩ resistor.

Note that the Address Translation strap does not specifically declare the presence of an NS32082 MMU, but only the

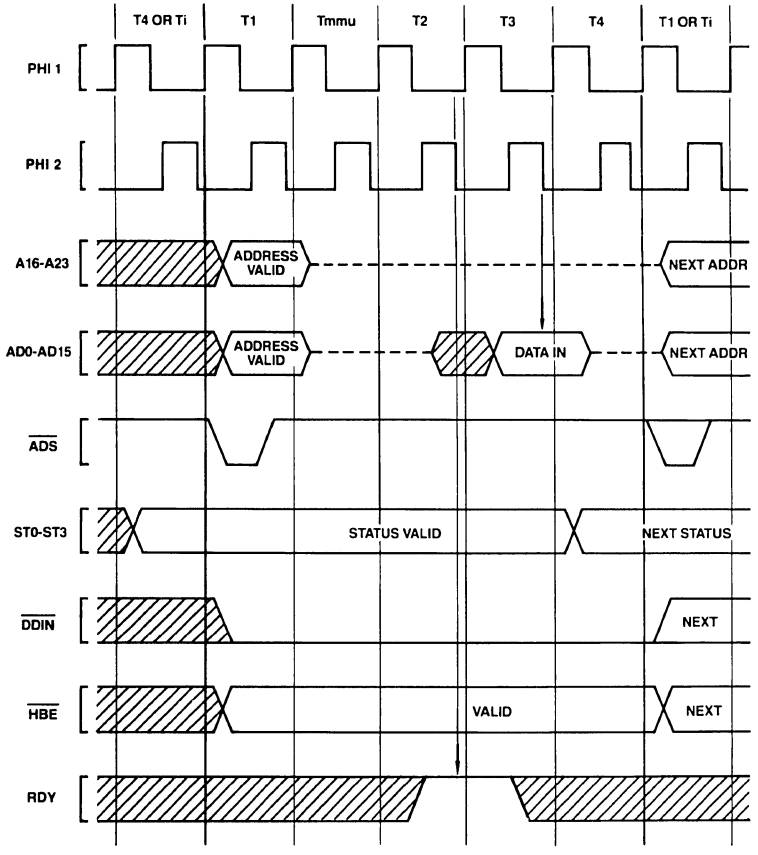

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FIGURE 3-15. Read Cycle with Address Translation (CPU Action)

3.0 Functional Description (Continued)

presence of external address translation circuitry. MMU instructions will still trap as being undefined unless the SETCFG (Set Configuration) instruction is executed to declare the MMU instruction set valid. See Section 2.1.3.

3.5.2 Translated Bus Timing

Figures 3-15 and *3-16* illustrate the CPU activity during a Read cycle and a Write cycle in Address Translation mode. The additional T-State, Tmmu, is inserted between T1 and T2. During this time the CPU places AD0–AD15 and A16–A23 into the TRI-STATE® mode, allowing the MMU to assert the translated address and issue the physical address strobe $\overline{PAV}$. T2 through T4 of the cycle are identical to their counter-parts without Address Translation, with the exception that the CPU Address lines A16–A23 remain in the TRI-STATE condition. This allows the MMU to continue asserting the translated address on those pins.

Note that in order for the NS32082 MMU to operate correctly it must be set to the 32016 mode by forcing A24/$\overline{HBF}$ high during reset.

Figures 3-17 and *3-18* show a Read cycle and a Write cycle as generated by the 32016/32082/32201 group. Note that with the CPU $\overline{ADS}$ signal going only to the MMU, and with the MMU $\overline{PAV}$ signal substituting for $\overline{ADS}$ everywhere else, Tmmu through T4 look exactly like T1 through T4 in a non-Memory-Managed system. For the connection diagram, see Appendix B.

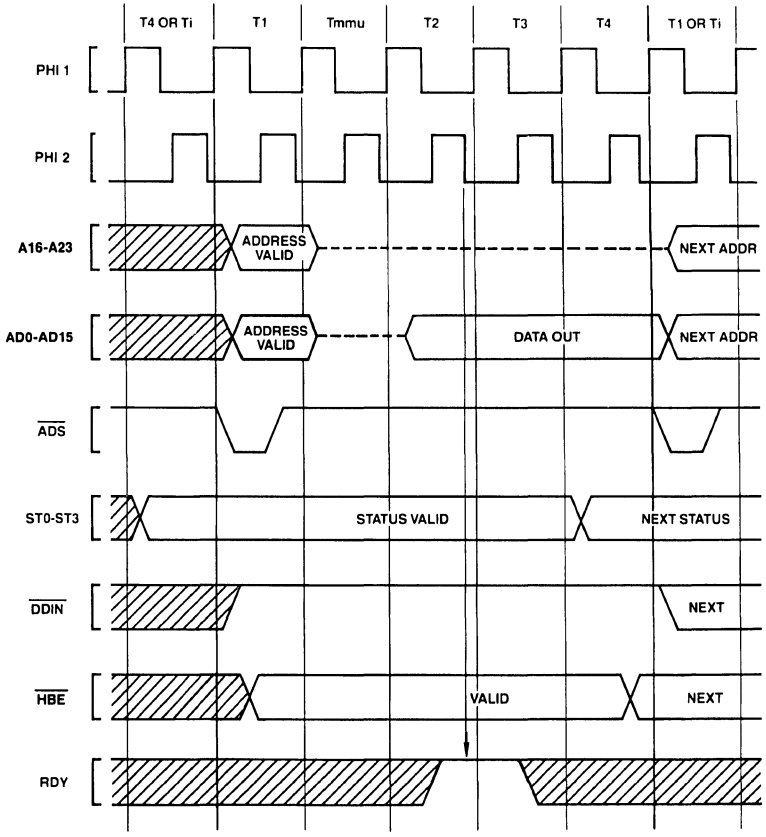

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FIGURE 3-16. Write Cycle with Address Translation (CPU Action)

3.0 Functional Description (Continued)

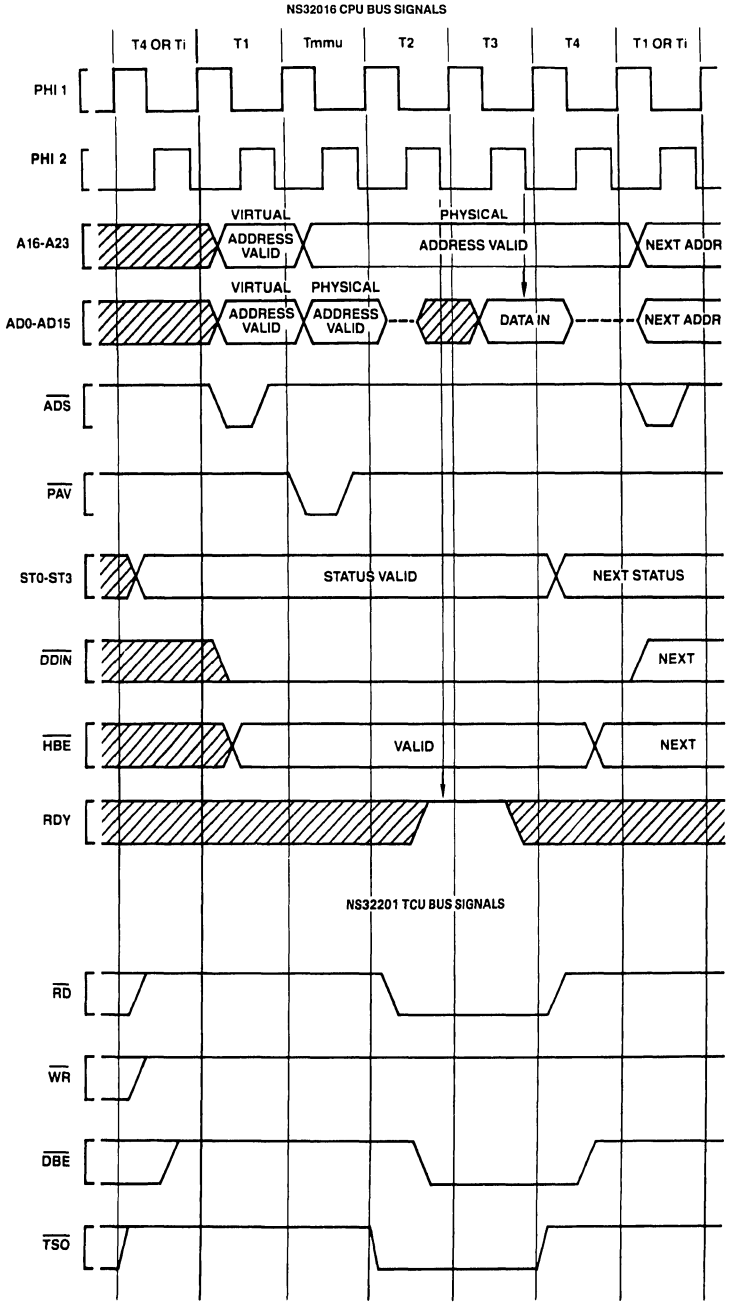

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FIGURE 3-17. Memory-Managed Read Cycle

3.0 Functional Description (Continued)

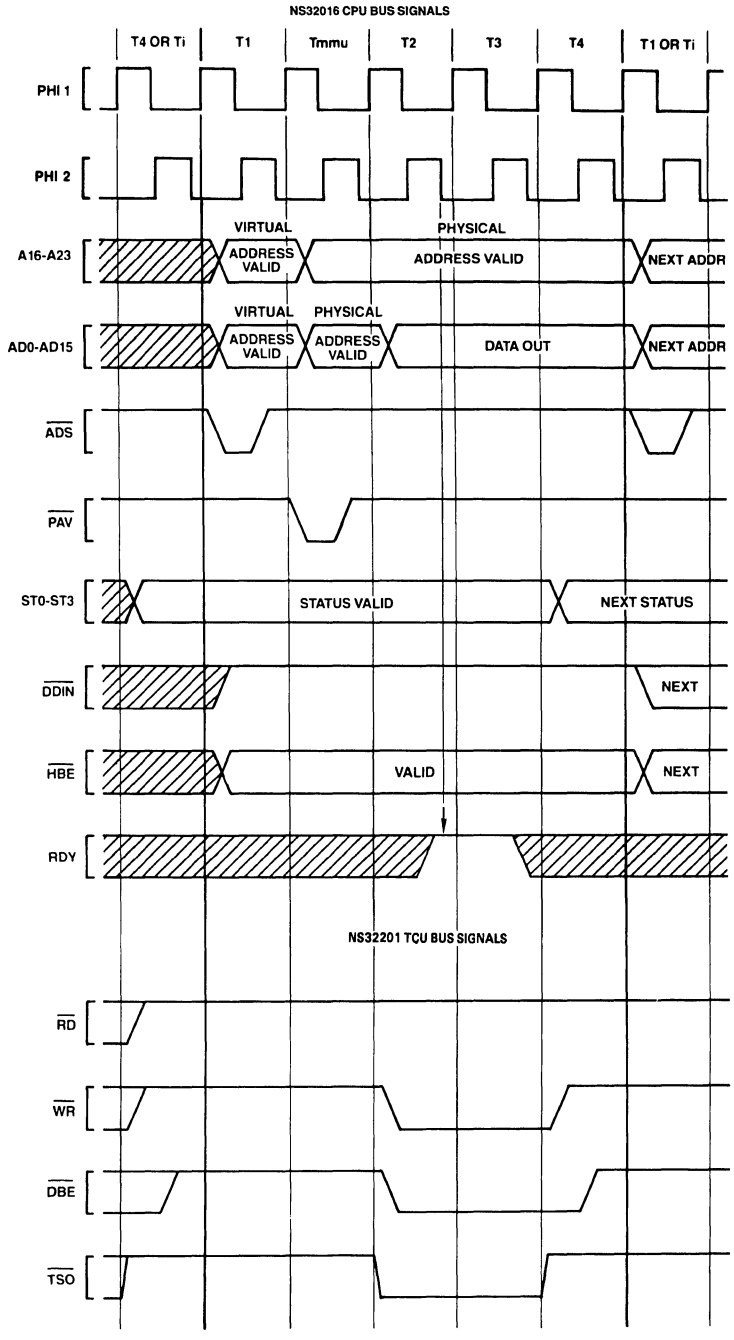

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FIGURE 3-18. Memory-Managed Write Cycle

3.0 Functional Description (Continued)

3.5.3 The $\overline{FLT}$ (Float) Pin

The $\overline{FLT}$ pin is used by the CPU for address translation support. Activating $\overline{FLT}$ during Tmmu causes the CPU to wait longer than Tmmu for address translation and validation. This feature is used occasionally by the NS32082 MMU in order to update its internal translation look.aside buffer (TLB) from page tables in memory, or to update certain status bits within them.

Figure 3-19 shows the effects of $\overline{FLT}$. Upon sampling $\overline{FLT}$ low, late in Tmmu, the CPU enters idle T-States (Tf) during which it:

1) Sets AD0–AD15, A16–A23 and $\overline{DDIN}$ to the TRI-STATE condition ("floating").
2) Sets $\overline{HBE}$ low.
3) Suspends further internal processing of the current instruction. This ensures that the current instruction remains abortable with retry. (See $\overline{RST}$/$\overline{ABT}$ description, Section 3.5.4.)

Note that the AD0–AD15 pins may be briefly asserted during the first idle T-State. The above conditions remain in effect until $\overline{FLT}$ again goes high. See the Timing Specifications, Section 4.

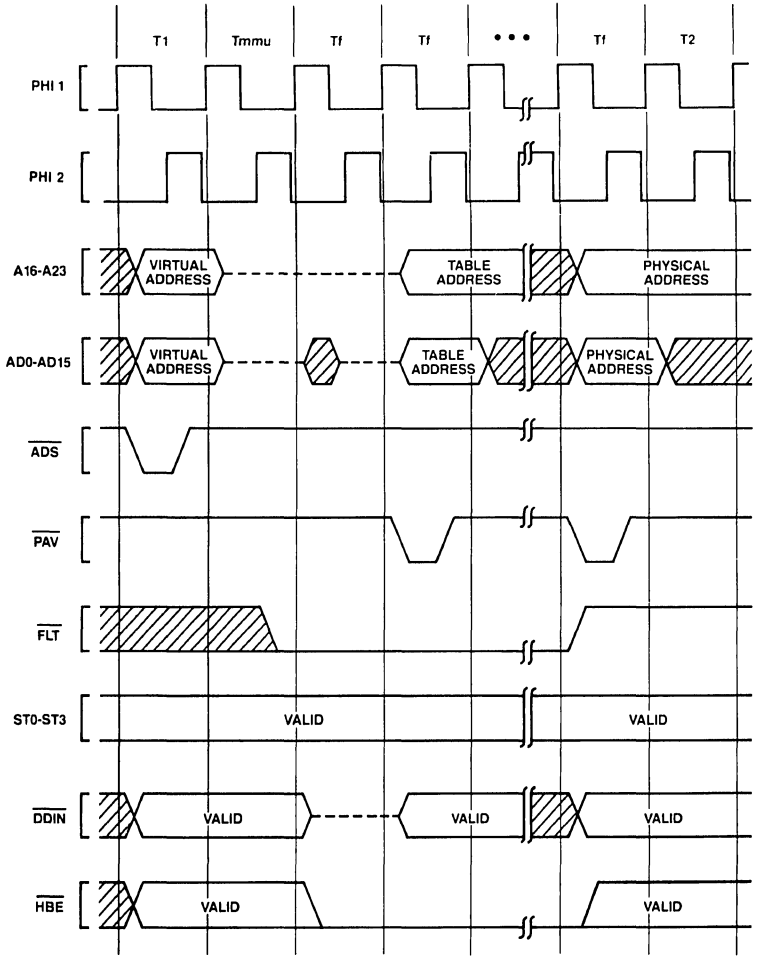

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FIGURE 3-19. $\overline{FLT}$ Timing

3.0 Functional Description (Continued)

3.5.4 Aborting Bus Cycles

The $\overline{RST}/\overline{ABT}$ pin, apart from its Reset function (Section 3.3), also serves as the means to "abort," or cancel, a bus cycle and the instruction, if any, which initiated it. An Abort request is distinguished from a Reset in that the $\overline{RST}/\overline{ABT}$ pin is held active for only one clock cycle.

If $\overline{RST}/\overline{ABT}$ is pulled low during Tmmu or Tf, this signals that the cycle must be aborted. The CPU itself will enter T2 and then Ti, thereby terminating the cycle. Since it is the MMU $\overline{PAV}$ signal which triggers a physical cycle, the rest of the system remains unaware that a cycle was started.

The NS32082 MMU will abort a bus cycle for either of two reasons:

1) The CPU is attempting to access a virtual address which is not currently resident in physical memory. The reference page must be brought into physical memory from mass storage to make it accessible to the CPU.
2) The CPU is attempting to perform an access which is not allowed by the protection level assigned to that page.

When a bus cycle is aborted by the MMU, the instruction that caused it to occur is also aborted in such a manner that it is guaranteed re-executable later. The information that is changed irrecoverably by such a partly-executed instruction does not affect its re-execution.

3.5.4.1 The Abort Interrupt

Upon aborting an instruction, the CPU immediately performs an interrupt through the ABT vector in the Interrupt Table (see Section 3.8). The Return Address pushed on the Interrupt Stack is the address of the aborted instruction, so that a Return from Trap (RETT) instruction will automatically retry it.

The one exception to this sequence occurs if the aborted bus cycle was an instruction prefetch. If so, it is not yet certain that the aborted prefetched code is to be executed. Instead of causing an interrupt, the CPU only aborts the bus cycle, and stops prefetching. If the information in the Instruction Queue runs out, meaning that the instruction will actually be executed, the ABT interrupt will occur, in effect aborting the instruction that was being fetched.

3.5.4.2 Hardware Considerations

In order to guarantee instruction retry, certain rules must be followed in applying an Abort to the CPU. These rules are followed by the NS32082 Memory Management Unit.

1) If $\overline{FLT}$ has not been applied to the CPU, the Abort pulse must occur during or before Tmmu. See the Timing Specifications, *Figure 4-22.*
2) If $\overline{FLT}$ has been applied to the CPU, the Abort pulse must be applied before the T-State in which $\overline{FLT}$ goes inactive. The CPU will not actually respond to the Abort command until $\overline{FLT}$ is removed. See *Figure 4-23.*
3) The Write half of a Read-Modify-Write operand access may not be aborted. The CPU guarantees that this will never be necessary for Memory Management funtions by applying a special RMW status (Status Code 1011) during the Read half of the access. When the CPU presents RMW status, that cycle must be aborted if it would be illegal to write to any of the accessed addresses.

If $\overline{RST}/\overline{ABT}$ is pulsed at any time other than as indicated above, it will abort either the instruction currently under execution or the next instruction and will act as a very high-priority interrupt. However, the program that was running at the time is not guaranteed recoverable.

3.6 BUS ACCESS CONTROL

The NS32016 CPU has the capability of relinquishing its access to the bus upon request from a DMA device or another CPU. This capability is implemented on the $\overline{HOLD}$ (Hold Request) and $\overline{HLDA}$ (Hold Acknowledge) pins. By asserting $\overline{HOLD}$ low, an external device requests access to the bus. On receipt of $\overline{HLDA}$ from the CPU, the device may perform bus cycles, as the CPU at this point has set the AD0–AD15, A16–A23, $\overline{ADS}$, $\overline{DDIN}$ and $\overline{HBE}$ pins to the TRI-STATE condition. To return control of the bus to the CPU, the device sets $\overline{HOLD}$ inactive, and the CPU acknowledges return of the bus by setting $\overline{HLDA}$ inactive.

How quickly the CPU releases the bus depends on whether it is idle on the bus at the time the $\overline{HOLD}$ request is made, as the CPU must always complete the current bus cycle. *Figure 3-20* shows the timing sequence when the CPU is idle. In this case, the CPU grants the bus during the immediately following clock cycle. *Figure 3-21* shows the sequence if the CPU is using the bus at the time that the $\overline{HOLD}$ request is made. If the request is made during or before the clock cycle shown (two clock cycles before T4), the CPU will release the bus during the clock cycle following T4. If the request occurs closer to T4, the CPU may already have decided to initiate another bus cycle. In that case it will not grant the bus until after the next T4 state. Note that this situation will also occur if the CPU is idle on the bus but has initiated a bus cycle internally.

In a Memory-Managed system, the $\overline{HLDA}$ signal is connected in a daisy-chain through the NS32082, so that the MMU can release the bus if it is using it.

3.0 Functional Description (Continued)

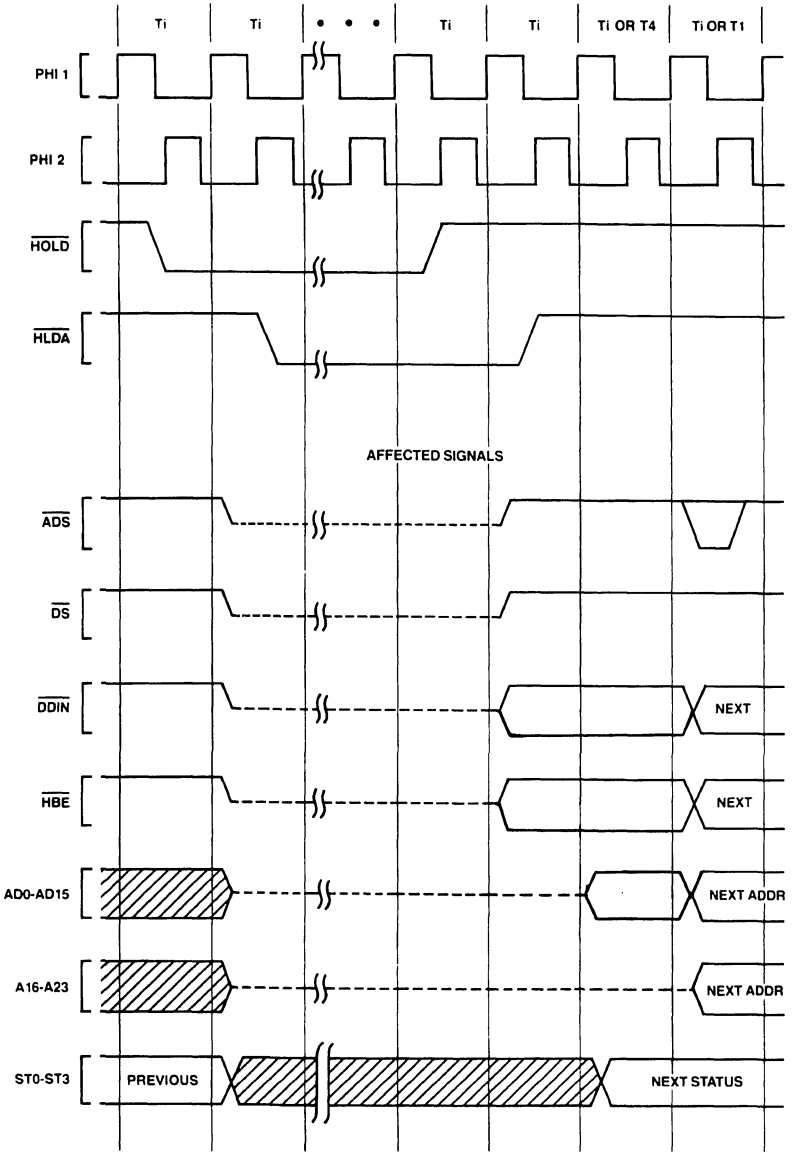

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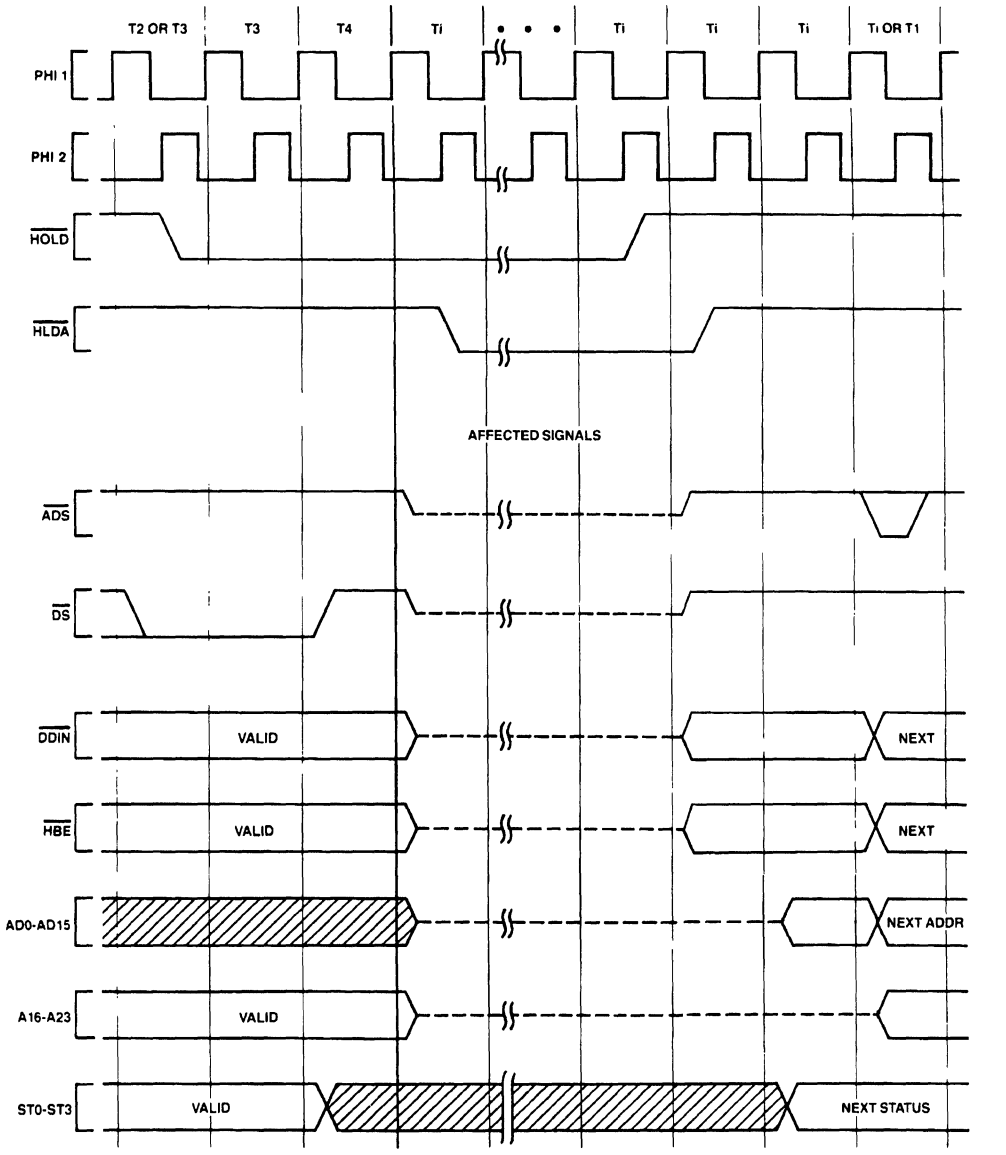
FIGURE 3-20. HOLD Timing, Bus Initially Idle

3.0 Functional Description (Continued)



TL/EE/5054–32

FIGURE 3-21. $\overline{\text{HOLD}}$ Timing, Bus Initially Not Idle

3.0 Functional Description (Continued)

3.7 INSTRUCTION STATUS

In addition to the four bits of Bus Cycle status (ST0–ST3), the NS32016 CPU also presents Instruction Status information on three separate pins. These pins differ from ST0–ST3 in that they are synchronous to the CPU's internal instruction execution section rather than to its bus interface section.

$\overline{PFS}$ (Program Flow Status) is pulsed low as each instruction begins execution. It is intended for debugging purposes, and is used that way by the NS32082 Memory Management Unit.

U/$\overline{S}$ originates from the U bit of the Processor Status Register, and indicates whether the CPU is currently running in User or Supervisor mode. It is sampled by the MMU for mapping, protection and debugging purposes. Although it is not synchronous to bus cycles, there are guarantees on its validity during any given bus cycle. See the Timing Specifications, *Figure 4-21.*

$\overline{ILO}$ (Interlocked Operation) is activated during an SBITI (Set Bit, Interlocked) or CBITI (Clear Bit, Interlocked) instruction. It is made available to external bus arbitration circuitry in order to allow these instructions to implement the semaphore primitive operations for multi-processor communication and resource sharing. As with the U/$\overline{S}$ pin, there are guarantees on its validity during the operand accesses performed by the instructions. See the Timing Specification Section, *Figure 4-19.*

3.8 NS32016 INTERRUPT STRUCTURE

$\overline{INT}$, on which maskable interrupts may be requested,

$\overline{NMI}$, on which non-maskable interrupts may be requested, and

$\overline{RST}$/$\overline{ABT}$, which may be used to abort a bus cycle and any associated instruction. See Section 3.5.4.

In addition, there is a set of internally-generated "traps" which cause interrupt service to be performed as a result either of exceptional conditions (e.g., attempted division by zero) or of specific instructions whose purpose is to cause a trap to occur (e.g., the Supervisor Call instruction).

3.8.1 General Interrupt/Trap Sequence

Upon receipt of an interrupt or trap request, the CPU goes through three major steps:

1) Adjustment of Registers.

   Depending on the source of the interrupt or trap, the CPU may restore and/or adjust the contents of the Program Counter (PC), the Processor Status Register (PSR) and the currently-selected Stack Pointer (SP). A copy of the PSR is made, and the PSR is then set to reflect Supervisor Mode and selection of the Interrupt Stack.

2) Vector Acquisition.

   A Vector is either obtained from the Data Bus or is supplied by default.

3) Service Call.

   The Vector is used as an index into the Interrupt Dispatch Table, whose base address is taken from the CPU Interrupt Base (INTBASE) Register. See *Figure 3-22.* A 32-bit External Procedure Descriptor is read from the table entry, and an External Procedure Call is performed using it. The MOD Register (16 bits) and Program Counter (32 bits) are pushed on the Interrupt Stack.

This process is illustrated in *Figure 3-23,* from the viewpoint of the programmer.

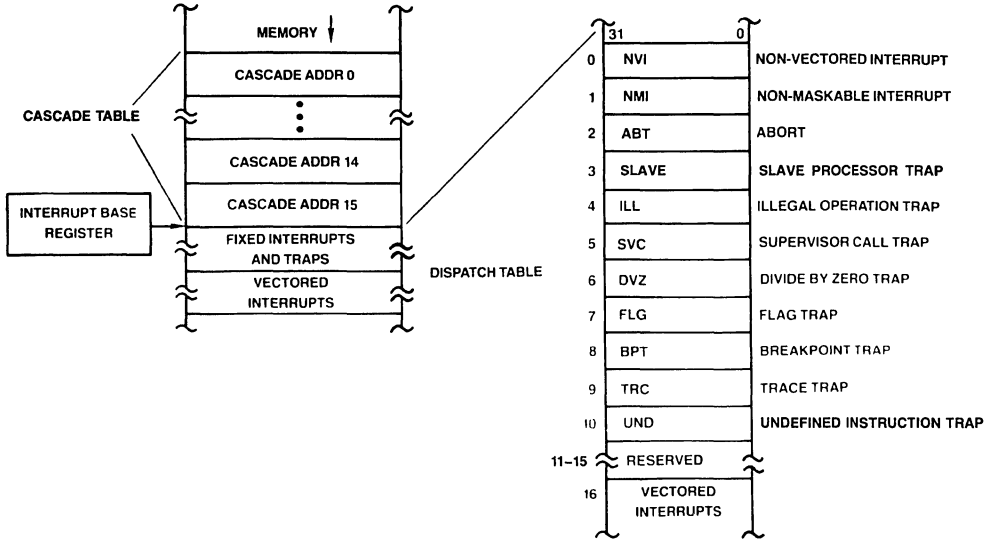


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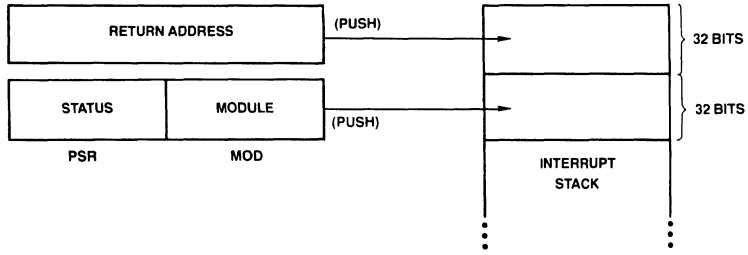
FIGURE 3-22. Interrupt Dispatch and Cascade Tables

3.0 Functional Description (Continued)



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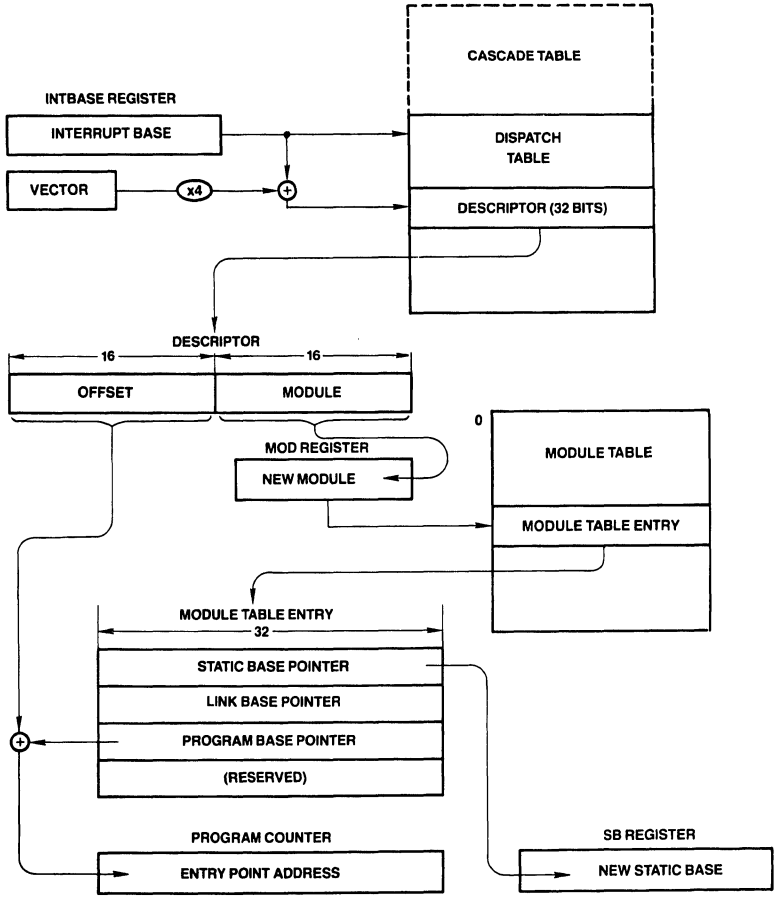

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FIGURE 3-23. Interrupt/Trap Service Routine Calling Sequence

3.0 Functional Description (Continued)

3.8.2 Interrupt/Trap Return

To return control to an interrupted program, one of two instructions is used. The RETT (Return from Trap) instruction (*Figure 3-24)* restores the PSR, MOD, PC and SB registers to their previous contents and, since traps are often used deliberately as a call mechanism for Supervisor Mode procedures, it also discards a specified number of bytes from the original stack as surplus parameter space. RETT is used to return from any trap or interrupt except the Maskable Interrupt. For this, the RETI (Return from Interrupt) instruction is used, which also informs any external Interrupt Control Units that interrupt service has completed. Since interrupts are generally asynchronous external events, RETI does not pop parameters. See *Figure 3-25.*

3.8.3 Maskable Interrupts (The $\overline{\text{INT}}$ Pin)

The $\overline{\text{INT}}$ pin is a level-sensitive input. A continuous low level is allowed for generating multiple interrupt requests. The input is maskable, and is therefore enabled to generate interrupt requests only while the Processor Status Register I bit is set. The I bit is automatically cleared during service of an $\overline{\text{INT}}$, $\overline{\text{NMI}}$ or Abort request, and is restored to its original setting upon return from the interrupt service routine via the RETT or RETI instruction.

The $\overline{\text{INT}}$ pin may be configured via the SETCFG instruction as either Non-Vectored (CFG Register bit I = 0) or Vectored (bit I = 1).

3.8.3.1 Non-Vectored Mode

In the Non-Vectored mode, an interrupt request on the $\overline{\text{INT}}$ pin will cause an Interrupt Acknowledge bus cycle, but the CPU will ignore any value read from the bus and use instead a default vector of zero. This mode is useful for small systems in which hardware interrupt prioritization is unnecessary.

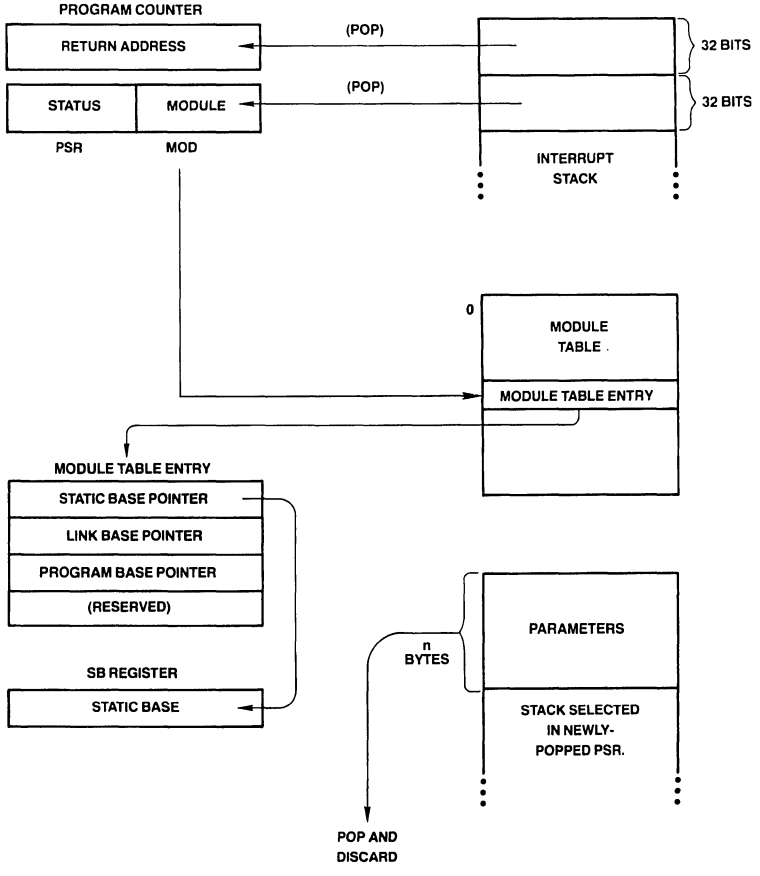

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FIGURE 3-24. Return from Trap (RETT n) Instruction Flow

3.0 Functional Description (Continued)

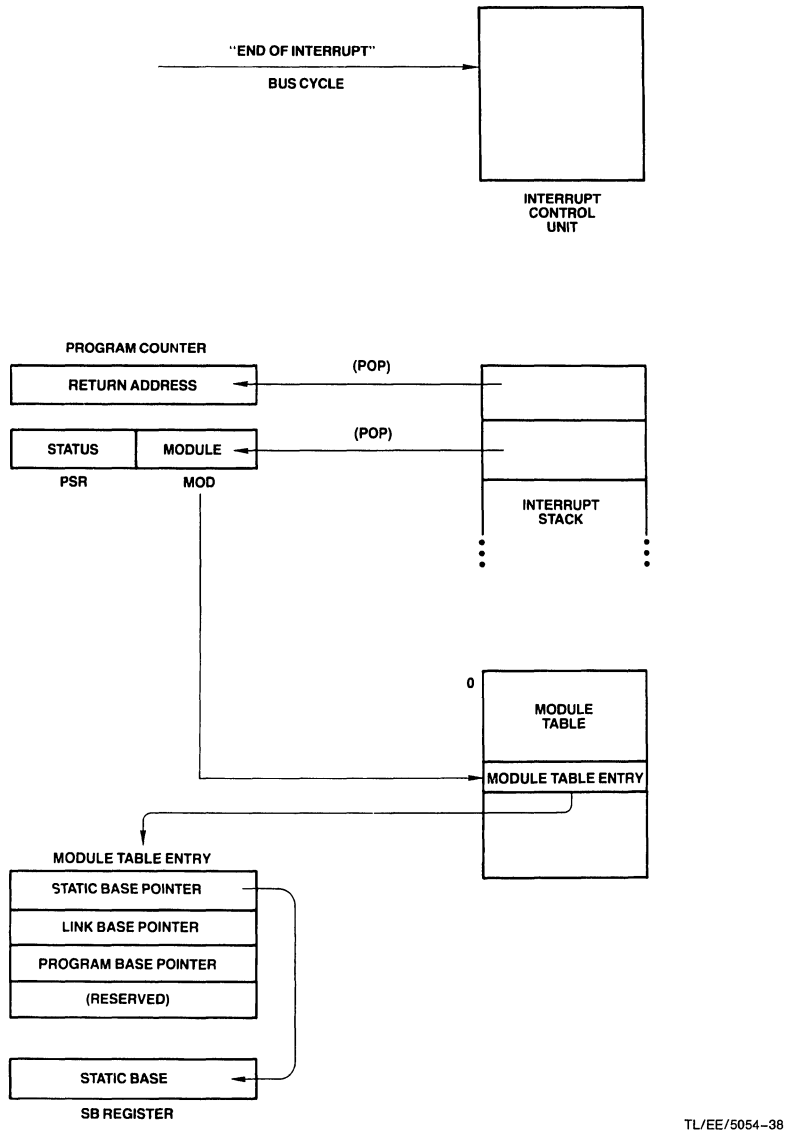

FIGURE 3-25. Return from Interrupt (RET) Instruction Flow

3.0 Functional Description (Continued)

3.8.3.2 Vectored Mode: Non-Cascaded Case

In the Vectored mode, the CPU uses an Interrupt Control Unit (ICU) to prioritize up to 16 interrupt requests. Upon receipt of an interrupt request on the $\overline{INT}$ pin, the CPU performs an "Interrupt Acknowledge, Master" bus cycle (Section 3.4.2) reading a vector value from the low-order byte of the Data Bus. This vector is then used as an index into the Dispatch Table in order to find the External Procedure Descriptor for the proper interrupt service procedure. The service procedure eventually returns via the Return from Interrupt (RETI) instruction, which performs an End of Interrupt bus cycle, informing the ICU that it may re-prioritize any interrupt requests still pending. The ICU provides the vector number again, which the CPU uses to determine whether it needs also to inform a Cascaded ICU (see below).

In a system with only one ICU (16 levels of interrupt), the vectors provided must be in the range of 0 through 127; that is, they must be positive numbers in eight bits. By providing a negative vector number, an ICU flags the interrupt source as being a Cascaded ICU (see below).

3.8.3.3 Vectored Mode: Cascaded Case

In order to allow up to 256 levels of interrupt, provision is made both in the CPU and in the NS32202 Interrupt Control Unit (ICU) to transparently support cascading. *Figure 3-27* shows a typical cascaded configuration. Note that the Interrupt output from a Cascaded ICU goes to an Interrupt Request input of the Master ICU, which is the only ICU which drives the CPU $\overline{INT}$ pin.

In a system which uses cascading, two tasks must be performed upon initialization:

1) For each Cascaded ICU in the system, the Master ICU must be informed of the line number (0 to 15) on which it receives the cascaded requests.
2) A Cascade Table must be established in memory. The Cascade Table is located in a NEGATIVE direction from the location indicated by the CPU Interrupt Base (INTBASE) Register. Its entries are 32-bit addresses, pointing to the Vector Registers of each of up to 16 Cascaded ICUs.

Figure 3-22 illustrates the position of the Cascade Table. To find the Cascade Table entry for a Cascaded ICU, take its Master ICU line number (0 to 15) and subtract 16 from it, giving an index in the range −16 to −1. Multiply this value by 4, and add the resulting negative number to the contents of the INTBASE Register. The 32-bit entry at this address must be set to the address of the Hardware Vector Register of the Cascaded ICU. This is referred to as the "Cascade Address."

Upon receipt of an interrupt request from a Cascaded ICU, the Master ICU interrupts the CPU and provides the negative Cascade Table index instead of a (positive) vector number. The CPU, seeing the negative value, uses it as an index into the Cascade Table and reads the Cascade Address from the referenced entry. Applying this address, the CPU performs an "Interrupt Acknowledge, Cascaded" bus cycle (Section 3.4.2), reading the final vector value. This vector is interpreted by the CPU as an unsigned byte, and can therefore be in the range of 0 through 255.

In returning from a Cascaded interrupt, the service procedure executes the Return from Interrupt (RETI) instruction, as it would for any Maskable Interrupt. The CPU performs an "End of Interrupt, Master" bus cycle (Section 3.4.2), whereupon the Master ICU again provides the negative Cascaded Table index. The CPU, seeing a negative value, uses it to find the corresponding Cascade Address from the Cascade Table. Applying this address, it performs an "End of Interrupt, Cascaded" bus cycle (Section 3.4.2), informing the Cascaded ICU of the completion of the service routine. The byte read from the Cascaded ICU is discarded.

Note: If an interrupt must be masked off, the CPU can do so by setting the corresponding bit in the interrupt mask register of the interrupt controller. However, if an interrupt is set pending during the CPU instruction that masks off that interrupt, the CPU may still perform an interrupt acknowledge cycle following that instruction since it might have sampled the $\overline{INT}$ line before the ICU deasserted it. This could cause the ICU to provide an invalid vector. To avoid this problem the above operation should be performed with the CPU interrupt disabled.

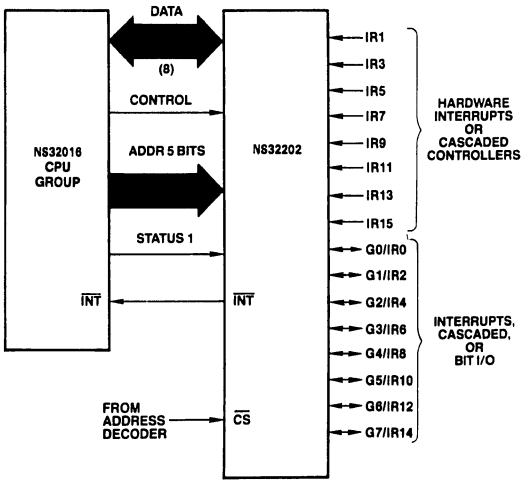

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FIGURE 3-26. Interrupt Control Unit Connections (16 Levels)

3.0 Functional Description (Continued)

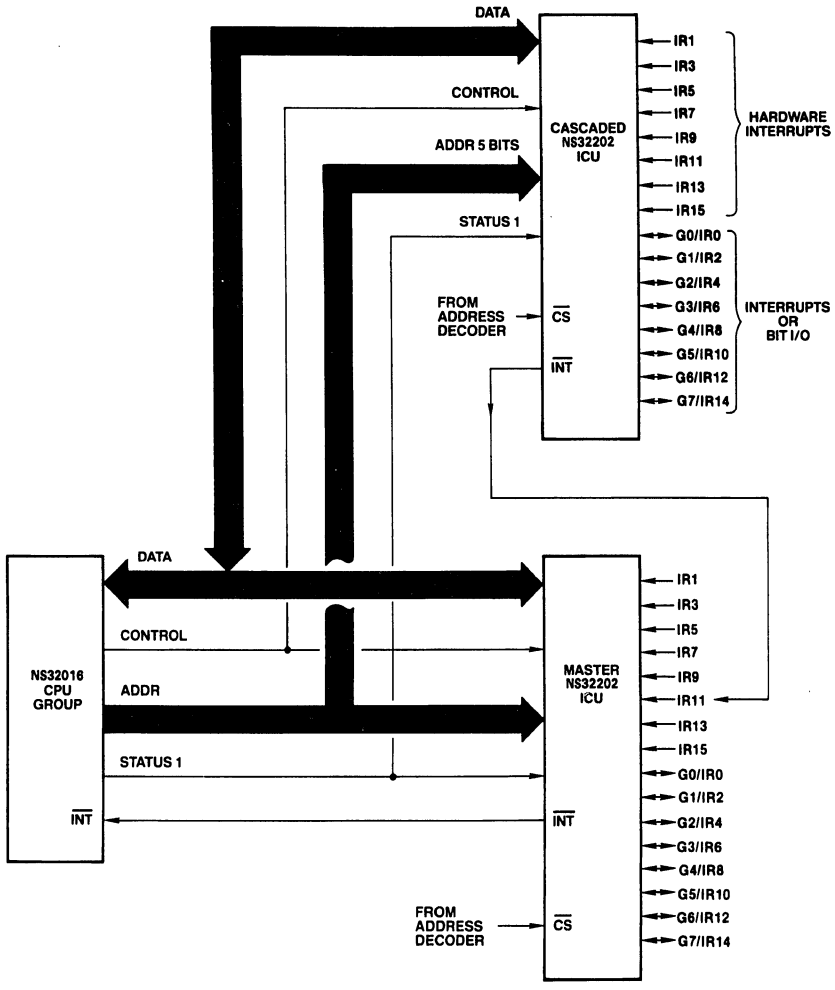

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FIGURE 3–27. Cascaded Interrupt Control Unit Connections

3.8.4 Non-Maskable Interrupt (The $\overline{\text{NMI}}$ Pin)

The Non-Maskable Interrupt is triggered whenever a falling edge is detected on the $\overline{\text{NMI}}$ pin. The CPU performs an "Interrupt Acknowledge, Master" bus cycle (Section 3.4.2) when processing of this interrupt actually begins. The Interrupt Acknowledge cycle differs from that provided for Maskable Interrupts in that the address presented is FFFF00_{16}. The vector value used for the Non-Maskable Interrupt is taken as 1, regardless of the value read from the bus.

The service procedure returns from the Non-Maskable Interrupt using the Return from Trap (RETT) instruction. No special bus cycles occur on return.

For the full sequence of events in processing the Non-Maskable Interrupt, see Section 3.8.7.1.

3.8.5 Traps

A trap is an internally-generated interrupt request caused as a direct and immediate result of the execution of an instruction. The Return Address pushed by any trap except Trap (TRC) below is the address of the first byte of the instruction during which the trap occurred. Traps do not disable interrupts, as they are not associated with external events. Traps recognized by NS32016 CPU are:

Trap (Slave): An exceptional condition was detected by the Floating Point Unit or another Slave Processor during the execution of a Slave Instruction. This trap is requested via the Status Word returned as part of the Slave Processor Protocol (Section 3.9.1).

3.0 Functional Description (Continued)

Trap (ILL): Illegal operation. A privileged operation was attempted while the CPU was in User Mode (PSR bit U = 1).

Trap (SVC): The Supervisor Call (SVC) instruction was executed.

Trap (DVZ): An attempt was made to divide an integer by zero. (The SLAVE trap is used for Floating Point division by zero.)

Trap (FLG): The FLAG instruction detected a "1" in the CPU PSR F bit.

Trap (BPT): The Breakpoint (BPT) instruction was executed.

Trap (TRC): The instruction just completed is being traced. See below.

Trap (UND): An undefined opcode was encountered by the CPU.

A special case is the Trace Trap (TRC), which is enabled by setting the T bit in the Processor Status Register (PSR). At the beginning of each instruction, the T bit is copied into the PSR P (Trace "Pending") bit. If the P bit is set at the end of an instruction, then the Trace Trap is activated. If any other trap or interrupt request is made during a traced instruction, its entire service procedure is allowed to complete before the Trace Trap occurs. Each interrupt and trap sequence handles the P bit for proper tracing, guaranteeing one and only one Trace Trap per instruction, and guaranteeing that the Return Address pushed during a Trace Trap is always the address of the next instruction to be traced.

3.8.6 Prioritization

The NS32016 CPU internally prioritizes simultaneous interrupt and trap requests as follows:

1) Traps other than Trace (Highest priority)
2) Abort
3) Non-Maskable Interrupt
4) Maskable Interrupts
5) Trace Trap (Lowest priority)

3.8.7 Interrupt/Trap Sequences: Detail Flow

For purposes of the following detailed discussion of interrupt and trap service sequences, a single sequence called "Service" is defined in *Figure 3-28.* Upon detecting any interrupt request or trap condition, the CPU first performs a sequence dependent upon the type of interrupt or trap. This sequence will include pushing the Processor Status Register and establishing a Vector and a Return Address. The CPU then performs the Service sequence.

For the sequenced followed in processing either Maskable or Non-Maskable Interrupts (on the $\overline{INT}$ or $\overline{NMI}$ pins, respectively), see Section 3.8.7.1. For Abort interrupts, see Section 3.8.7.4. For the Trace Trap, see Section 3.8.7.3, and for all other traps see Section 3.8.7.2.

3.8.7.1 Maskable/Non-Maskable Interrupt Sequence

This sequence is performed by the CPU when the $\overline{NMI}$ pin receives a falling edge, or the $\overline{INT}$ pin becomes active with the PSR I bit set. The interrupt sequence begins either at the next instruction boundary or, in the case of the String instructions, at the next interruptible point during its execution.

1. If a String instruction was interrupted and not yet completed:
   a. Clear the Processor Status Register P bit.
   b. Set "Return Address" to the address of the first byte of the interrupted instruction.

   Otherwise, set "Return Address" to the address of the next instruction.
2. Copy the Processor Status Register (PSR) into a temporary register, then clear PSR bits S, U, T, P and I.
3. If the interrupt is Non-Maskable:
   a. Read a byte from address $FFFF00_{16}$, applying Status Code 0100 (Interrupt Acknowledge, Master: Section 3.4.2). Discard the byte read.
   b. Set "Vector" to 1.
   c. Go to Step 8.
4. If the interrupt is Non-Vectored:
   a. Read a byte from address $FFFF00_{16}$, applying Status Code 0100 (Interrupt Acknowledge, Master: Section 3.4.2). Discard the byte read.
   b. Set "Vector" to 0.
   c. Go to Step 8.
5. Here the interrupt is Vectored. Read "Byte" from address $FFFE00_{16}$, applying Status Code 0100 (Interrupt Acknowledge, Master: Section 3.4.2).
6. If "Byte" ≥ 0, then set "Vector" to "Byte" and go to Step 8.
7. If "Byte" is in the range -16 through -1, then the interrupt source is Cascaded. (More negative values are reserved for future use.) Perform the following:
   a. Read the 32-bit Cascade Address from memory. The address is calculated as INTBASE + 4* Byte.
   b. Read "Vector," applying the Cascade Address just read and Status Code 0101 (Interrupt Acknowledge, Cascaded: Section 3.4.2).
8. Push the PSR copy (from Step 2) onto the Interrupt Stack as a 16-bit value.
9. Perform Service (Vector, Return Address), *Figure 3-28.*

Service (Vector, Return Address):

1) Read the 32-bit External Procedure Descriptor from the Interrupt Dispatch Table: address is Vector*4 + INTBASE Register contents.
2) Move the Module field of the Descriptor into the MOD Register.
3) Read the new Static Base pointer from the memory address contained in MOD, placing it into the SB Register.
4) Read the Program Base pointer from memory address MOD + 8, and add to it the Offset field from the Descriptor, placing the result in the Program Counter.
5) Flush Queue: Non-sequentially fetch first instruction of Interrupt Routine.
6) Push MOD Register onto the Interrupt Stack as a 16-bit value. (The PSR has already been pushed as a 16-bit value.)
7) Push the Return Address onto the Interrupt Stack as a 32-bit quantity.

FIGURE 3-28. Service Sequence
Invoked during all interrupt/trap sequences

3.0 Functional Description (Continued)

3.8.7.2 Trap Sequence: Traps Other Than Trace

1) Restore the currently selected Stack Pointer and the Processor Status Register to their original values at the start of the trapped instruction.
2) Set "Vector" to the value corresponding to the trap type.

SLAVE:	Vector = 3.
ILL:	Vector = 4.
SVC:	Vector = 5.
DVZ:	Vector = 6.
FLG:	Vector = 7.
BPT:	Vector = 8.
UND:	Vector = 10.

3) Copy the Processor Status Register (PSR) into a temporary register, then clear PSR bits S, U, P and T.
4) Push the PSR copy onto the Interrupt Stack as a 16-bit value.
5) Set "Return Address" to the address of the first byte of the trapped instruction.
6) Perform Service (Vector, Return Address), *Figure 3-28.*

3.8.7.3 Trace Trap Sequence

1) In the Processor Status Register (PSR), clear the P bit.
2) Copy the PSR into a temporary register, then clear PSR bits S, U and T.
3) Push the PSR copy onto the Interrupt Stack as a 16-bit value.
4) Set "Vector" to 9.
5) Set "Return Address" to the address of the next instruction.
6) Perform Service (Vector, Return Address), *Figure 3-28.*

3.8.7.4 Abort Sequence

1) Restore the currently selected Stack Pointer to its original contents at the beginning of the aborted instruction.
2) Clear the PSR P bit.
3) Copy the PSR into a temporary register, then clear PSR bits S, U, T and I.
4) Push the PSR copy onto the Interrupt Stack as a 16-bit value.
5) Set "Vector" to 2.
6) Set "Return Address" to the address of the first byte of the aborted instruction.
7) Perform Service (Vector, Return Address), *Figure 3-28.*

3.9 SLAVE PROCESSOR INSTRUCTIONS

The NS32016 CPU recognizes three groups of instructions as being executable by external Slave Processors:

Floating Point Instruction Set

Memory Management Instruction Set

Custom Instruction Set

Each Slave Instruction Set is validated by a bit in the Configuration Register (Section 2.1.3). Any Slave Instruction which does not have its corresponding Configuration Register bit set will trap as undefined, without any Slave Processor communication attempted by the CPU. This allows software simulation of a non-existent Slave Processor.

3.9.1 Slave Processor Protocol

Slave Processor instructions have a three-byte Basic Instruction field, consisting of an ID Byte followed by an Operation Word. The ID Byte has three functions:

1) It identifies the instruction as being a Slave Processor instruction.
2) It specifies which Slave Processor will execute it.
3) It determines the format of the following Operation Word of the instruction.

Upon receiving a Slave Processor instruction, the CPU initiates the sequence outlined in *Figure 3-29.* While applying Status Code 1111 (Broadcast ID, Section 3.4.2), the CPU transfers the ID Byte on the least-significant half of the Data Bus (AD0–AD7). All Slave Processors input this byte and decode it. The Slave Processor selected by the ID Byte is activated, and from this point the CPU is communicating only with it. If any other slave protocol was in progress (e.g., an aborted Slave instruction), this transfer cancels it.

The CPU next sends the Operation Word while applying Status Code 1101 (Transfer Slave Operand, Section 3.4.2). Upon receiving it, the Slave Processor decodes it, and at this point both the CPU and the Slave Processor are aware of the number of operands to be transferred and their sizes. The Operation Word is swapped on the Data Bus; that is, bits 0–7 appear on pins AD8–AD15 and bits 8–15 appear on pins AD0–AD7.

Using the Addressing Mode fields within the Operation Word, the CPU starts fetching operands and issuing them to the Slave Processor. To do so, it references any Addressing Mode extensions which may be appended to the Slave Processor instruction. Since the CPU is solely responsible for memory accesses, these extensions are not sent to the Slave Processor. The Status Code applied is 1101 (Transfer Slave Processor Operand, Section 3.4.2).

Status Combinations:
Send ID (ID): Code 1111
Xfer Operand (OP): Code 1101
Read Status (ST): Code 1110

Step	Status	Action
1	ID	CPU Send ID Byte.
2	OP	CPU Sends Operation Word.
3	OP	CPU Sends Required Operands.
4	—	Slave Starts Execution. CPU Pre-Fetches.
5	—	Slave Pulses $\overline{SPC}$ Low.
6	ST	CPU Reads Status Word. (Trap? Alter Flags?)
7	OP	CPU Reads Results (If Any).

FIGURE 3-29. Slave Processor Protocol

3.0 Functional Description (Continued)

After the CPU has issued the last operand, the Slave Processor starts the actual execution of the instruction. Upon completion, it will signal the CPU by pulsing $\overline{SPC}$ low. To allow for this, and for the Address Translation strap function, $\overline{AT}/\overline{SPC}$ is normally held high only by an internal pull-up device of approximately 5 kΩ.

While the Slave Processor is executing the instruction, the CPU is free to prefetch instructions into its queue. If it fills the queue before the Slave Processor finishes, the CPU will wait, applying Status Code 0011 (Waiting for Slave, Section 3.4.2).

Upon receiving the pulse on $\overline{SPC}$, the CPU uses $\overline{SPC}$ to read a Status Word from the Slave Processor, applying Status Code 1110 (Read Slave Status, Section 3.4.2). This word has the format shown in *Figure 3-30*. If the Q bit ("Quit", Bit 0) is set, this indicates that an error was detected by the Slave Processor. The CPU will not continue the protocol, but will immediately trap through the Slave vector in the Interrupt Table. Certain Slave Processor instructions cause CPU PSR bits to be loaded from the Status Word.

The last step in the protocol is for the CPU to read a result, if any, and transfer it to the destination. The Read cycles from the Slave Processor are performed by the CPU while applying Status Code 1101 (Transfer Slave Operand, Section 3.4.2).

An exception to the protocol above is the LMR (Load Memory Management Register) instruction, and a corresponding Custom Slave instruction (LCR: Load Custom Register). In executing these instructions, the protocol ends after the CPU has issued the last operand. The CPU does not wait for an acknowledgement from the Slave Processor, and it does not read status.

3.9.2 Floating Point Instructions

Table 3-4 gives the protocols followed for each Floating Point instruction. The instructions are referenced by their mnemonics. For the bit encodings of each instruction, see Appendix A.

The Operand class columns give the Access Class for each general operand, defining how the addressing modes are interpreted (see Series 32000 Instruction Set Reference Manual).

The Operand Issued columns show the sizes of the operands issued to the Floating Point Unit by the CPU. "D" indicates a 32-bit Double Word. "i" indicates that the instruction specifies an integer size for the operand (B=Byte, W=Word, D=Double Word). "f" indicates that the instruction specifies a Floating Point size for the operand (F=32-bit Standard Floating, L=64-bit Long Floating).

The Returned Value Type and Destination column gives the size of any returned value and where the CPU places it. The PSR Bits Affected column indicates which PSR bits, if any, are updated from the Slave Processor Status Word (*Figure 3-30*).

TABLE 3-4
Floating Point Instruction Protocols

Mnemonic	Operand 1 Class	Operand 2 Class	Operand 1 Issued	Operand 2 Issued	Returned Value Type and Dest.	PSR Bits Affected
ADDf	read.f	rmw.f	f	f	f to Op. 2	none
SUBf	read.f	rmw.f	f	f	f to Op. 2	none
MULf	read.f	rmw.f	f	f	f to Op. 2	none
DIVf	read.f	rmw.f	f	f	f to Op. 2	none
MOVf	read.f	write.f	f	N/A	f to Op. 2	none
ABSf	read.f	write.f	f	N/A	f to Op. 2	none
NEGf	read.f	write.f	f	N/A	f to Op. 2	none
CMPf	read.f	read.f	f	f	N/A	N,Z,L
FLOORfi	read.f	write.i	f	N/A	i to Op. 2	none
TRUNCfi	read.f	write.i	f	N/A	i to Op. 2	none
ROUNDfi	read.f	write.i	f	N/A	i to Op. 2	none
MOVFL	read.F	write.L	F	N/A	L to Op. 2	none
MOVLF	read.L	write.F	L	N/A	F to Op. 2	none
MOVif	read.i	write.f	i	N/A	f to Op. 2	none
LFSR	read.D	N/A	D	N/A	N/A	none
SFSR	N/A	write.D	N/A	N/A	D to Op. 2	none

Note:
D = Double Word
i = integer size (B,W,D) specified in mnemonic.
f = Floating Point type (F,L) specified in mnemonic.
N/A = Not Applicable to this instruction.

3.0 Functional Description (Continued)

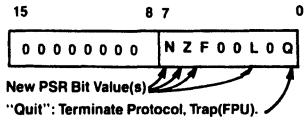

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FIGURE 3-30. Slave Processor Status Word Format

Any operand indicated as being of type "f" will not cause a transfer if the Register addressing mode is specified. This is because the Floating Point Registers are physically on the Floating Point Unit and are therefore available without CPU assistance.

3.9.3 Memory Management Instructions

Table 3-5 gives the protocols for Memory Management instructions. Encodings for these instructions may be found in Appendix A.

In executing the RDVAL and WRVAL instructions, the CPU calculates and issues the 32-bit Effective Address of the single operand. The CPU then performs a single-byte Read cycle from that address, allowing the MMU to safely abort the instruction if the necessary information is not currently in physical memory. Upon seeing the memory cycle complete, the MMU continues the protocol, and returns the validation result in the F bit of the Slave Status Word.

The size of a Memory Management operand is always a 32-bit Double Word. For further details of the Memory Management Instruction set, see the Series 32000 Instruction Set Reference Manual and the NS32082 MMU Data Sheet.

TABLE 3-5.
Memory Management Instruction Protocols

Mnemonic	Operand 1 Class	Operand 2 Class	Operand 1 Issued	Operand 2 Issued	Returned Value Type and Dest.	PSR Bits Affected
RDVAL*	addr	N/A	D	N/A	N/A	F
WRVAL*	addr	N/A	D	N/A	N/A	F
LMR*	read.D	N/A	D	N/A	N/A	none
SMR*	write.D	N/A	N/A	N/A	D to Op. 1	none

Note:

In the RDVAL and WRVAL instructions, the CPU issues the address as a Double Word, and performs a single-byte Read cycle from that memory address. For details, see the Series 32000 Instruction Set Reference Manual and the NS32082 Memory Management Unit Data Sheet.

D = Double Word

* = Privileged Instruction: will trap if CPU is in User Mode.

N/A = Not Applicable to this instruction.

3.0 Functional Description (Continued)

3.9.4 Custom Slave Instructions

Provided in the NS32016 is the capability of communicating with a user-defined, "Custom" Slave Processor. The instruction set provided for a Custom Slave Processor defines the instruction formats, the operand classes and the communication protocol. Left to the user are the interpretations of the Op Code fields, the programming model of the Custom Slave and the actual types of data transferred. The protocol specifies only the size of an operand, not its data type.

Table 3-6 lists the relevant information for the Custom Slave instruction set. The designation "c" is used to represent an operand which can be a 32-bit ("D") or 64-bit ("Q") quantity in any format; the size is determined by the suffix on the mnemonic. Similarly, an "i" indicates an integer size (Byte, Word, Double Word) selected by the corresponding mnemonic suffix.

Any operand indicated as being of type 'c' will not cause a transfer if the register addressing mode is specified. It is assumed in this case that the slave processor is already holding the operand internally.

For the instruction encodings, see Appendix A.

TABLE 3-6.
Custom Slave Instruction Protocols

Mnemonic	Operand 1 Class	Operand 2 Class	Operand 1 Issued	Operand 2 Issued	Returned Value Type and Dest.	PSR Bits Affected
CCAL0c	read.c	rmw.c	c	c	c to Op. 2	none
CCAL1c	read.c	rmw.c	c	c	c to Op. 2	none
CCAL2c	read.c	rmw.c	c	c	c to Op. 2	none
CCAL3c	read.c	rmw.c	c	c	c to Op. 2	none
CMOV0c	read.c	write.c	c	N/A	c to Op. 2	none
CMOV1c	read.c	write.c	c	N/A	c to Op. 2	none
CMOV2c	read.c	write.c	c	N/A	c to Op. 2	none
CMOV3c	read.c	write.c	c	N/A	c to Op. 2	none
CCMP0c	read.c	read.c	c	c	N/A	N,Z,L
CCMP1c	read.c	read.c	c	c	N/A	N,Z,L
CCV0ci	read.c	write.i	c	N/A	i to Op. 2	none
CCV1ci	read.c	write.i	c	N/A	i to Op. 2	none
CCV2ci	read.c	write.i	c	N/A	i to Op. 2	none
CCV3ic	readi	write.c	i	N/A	c to Op. 2	none
CCV4DQ	read.D	write.Q	D	N/A	Q to Op. 2	none
CCV5QD	read.Q	write.D	Q	N/A	D to Op. 2	none
LCSR	read.D	N/A	D	N/A	N/A	none
SCSR	N/A	write.D	N/A	N/A	D to Op. 2	none
CATST0*	addr	N/A	D	N/A	N/A	F
CATST1*	addr	N/A	D	N/A	N/A	F
LCR*	read.D	N/A	D	N/A	N/A	none
SCR*	write.D	N/A	N/A	N/A	D to Op.1	none

Note:

D = Double Word

i = integer size (B,W,D) specified in mnemonic.

c = Custom size (D:32 bits or Q:64 bits) specified in mnemonic.

* = Privileged Instruction: will trap if CPU is in User Mode.

N/A = Not Applicable to this instruction.

4.0 Device Specifications

4.1 PIN DESCRIPTIONS

The following is a brief description of all NS32016 pins. The descriptions reference portions of the Functional Description, Section 3.

4.1.1 Supplies

Power (V_{CC}): +5V positive supply. Section 3.1

Logic Ground (GNDL): Ground reference for on-chip logic. Section 3-1.

Buffer Ground (GNDB): Ground reference for on-chip drivers connected to output pins. Section 3.1.

Back-Bias Generator (BBG): Output of on-chip substrate voltage generator. Section 3.1.

4.1.2 Input Signals

Clocks (PHI1, PHI2): Two-phase clocking signals. Section 3.2.

Ready (RDY): Active high. While RDY is inactive, the CPU extends the current bus cycle to provide for a slower memory or peripheral reference. Upon detecting RDY active, the CPU terminates the bus cycle. Section 3.4.1.

Hold Request ($\overline{\text{HOLD}}$): Active low. Causes the CPU to release the bus for DMA or multiprocessing purposes. Section 3.6.

Note: If the $\overline{\text{HOLD}}$ signal is generated asynchronously, it's set up and hold times may be violated.

In this case it is recommended to synchronize it with CTTL to minimize the possibility of metastable states.

The CPU provides only one synchronization stage to minimize the $\overline{\text{HLDA}}$ latency. This is to avoid speed degradations in cases of heavy $\overline{\text{HOLD}}$ activity (i.e. DMA controller cycles interleaved with CPU cycles.)

Interrupt ($\overline{\text{INT}}$): Active low, Maskable interrupt request. Section 3.8.

Non-Maskable Interrupt ($\overline{\text{NMI}}$): Active low, Non-Maskable interrupt request. Section 3.8.

Reset/Abort ($\overline{\text{RST}}/\overline{\text{ABT}}$): Active low. If held active for one clock cycle and released, this pin causes an Abort Command, Section 3.5.4. If held longer, it initiates a Reset, Section 3.3.

4.1.3 Output Signals

Address Bits 16–23 (A16–A23): These are the most significant 8 bits of the memory address bus. Section 3.4.

Address Strobe ($\overline{\text{ADS}}$): Address low. Controls address latches; indicates start of a bus cycle. Section 3.4.

Data Direction In ($\overline{\text{DDIN}}$): Active low. Status signal indicating direction of data transfer during a bus cycle. Section 3.4.

High Byte Enable ($\overline{\text{HBE}}$): Active low. Status signal enabling transfer on the most significant byte of the Data Bus. Section 3.4; Section 3.4.3.

Note: The $\overline{\text{HBE}}$ signal is normally floated when the CPU grants the bus in response to a DMA request on the $\overline{\text{HOLD}}$ pin.

However, when an MMU is used and the bus is granted during an MMU page table look-up, $\overline{\text{HBE}}$ is not floated since the CPU does not have sufficient information to synchronize the release of $\overline{\text{HBE}}$ to the MMU's bus cycles.

Therefore, in a memory managed system, an external TRI-STATE buffer is required. This is shown in Figure B-1 in Appendix B.

Status (ST0–ST3): Active high. Bus cycle status code, ST0 least significant. Section 3.4.2. Encodings are:

0000 — Idle: CPU Inactive on Bus.
0001 — Idle: WAIT Instruction.
0010 — (Reserved)
0011 — Idle: Waiting for Slave.
0100 — Interrupt Acknowledge, Master.
0101 — Interrupt Acknowledge, Cascaded.
0110 — End of Interrupt, Master.
0111 — End of Interrupt, Cascaded.
1000 — Sequential Instruction Fetch.
1001 — Non-Sequential Instruction Fetch.
1010 — Data Transfer.
1011 — Read Read-Modify-Write Operand.
1100 — Read for Effective Address.
1101 — Transfer Slave Operand.
1110 — Read Slave Status Word.
1111 — Broadcast Slave ID.

Hold Acknowledge ($\overline{\text{HLDA}}$): Active low. Applied by the CPU in response to $\overline{\text{HOLD}}$ input, indicating that the bus has been released for DMA or multiprocessing purposes. Section 3.7.

User/Superior (U/$\overline{\text{S}}$): User or Supervisor Mode status. Section 3.7. High state indicates User Mode, low indicates Supervisor Mode. Section 3.7.

Interlocked Operation ($\overline{\text{ILO}}$): Active low. Indicates that an interlocked instruction is being executed. Section 3.7.

Program Flow Status ($\overline{\text{PFS}}$): Active low. Pulse indicates beginning of an instruction execution. Section 3.7.

4.1.4 Input/Output Signals

Address/Data 0–15 (AD0–AD15): Multiplexed Address/Data information. Bit 0 is the least significant bit of each. Section 3.4.

Address Translation/Slave Processor Control ($\overline{\text{AT}}/\overline{\text{SPC}}$): Active low. Used by the CPU as the data strobe output for Slave Processor transfers; used by Slave Processors to acknowledge completion of a slave instruction. Section 3.4.6. Section 3.9. Sampled on the rising edge of Reset as Address Translation Strap. Section 3.5.1.

In Non-Memory-Managed systems this pin should be pulled-up to V_{CC} through a 10 kΩ resistor.

Data Strobe/Float ($\overline{\text{DS}}/\overline{\text{FLT}}$): Active low. Data Strobe output, Section 3.4, or Float Command input, Section 3.5.3. Pin function is selected on $\overline{\text{AT}}/\overline{\text{SPC}}$ pin, Section 3.5.1.

4.0 Device Specifications (Continued)

4.2 ABSOLUTE MAXIMUM RATINGS

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Temperature Under Bias	0°C to +70°C
Storage Temperature	−65°C to +150°C
All Input or Output Voltages With Respect to GND	−0.5V to +7V
Power Dissipation	1.5 Watt

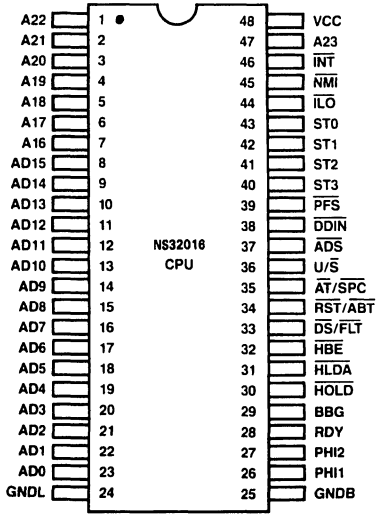
Note: *Absolute maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended; operation should be limited to those conditions specified under Electrical Characteristics.*

4.3 ELECTRICAL CHARACTERISTICS $T_A = 0$ to +70°C, $V_{CC} = 5V \pm 5\%$, GND = 0V

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High Level Input Voltage		2.0		$V_{CC}+0.5$	V
V_{IL}	Low Level Input Voltage		−0.5		0.8	V
V_{CH}	High Level Clock Voltage	PHI1, PHI2 pins only	$V_{CC}-0.35$		$V_{CC}+0.5$	V
V_{CL}	Low Level Clock Voltage	PHI1, PHI2 pins only	−0.5		0.3	V
V_{CLT}	Low Level Clock Voltage, Transient (ringing tolerance)	PHI1, PHI2 pins only	−0.5		0.6	V
V_{OH}	High Level Output Voltage	$I_{OH} = -400\ \mu A$	2.4			V
V_{OL}	Low Level 0 Output Voltage	$I_{OL} = 2$ mA			0.45	V
I_{ILS}	$\overline{AT}/\overline{SPC}$ Input Current (low)	$V_{IN} = 0.4V$, $\overline{AT}/\overline{SPC}$ in input mode	0.05		1.0	mA
I_I	Input Load Current	$0 \le V_{IN} \le V_{CC}$, All inputs except PHI1, PHI2, $\overline{AT}/\overline{SPC}$	−20		20	μA
I_L	Leakage Current Output and I/O Pins in in TRI-STATE/Input Mode	$0.4 \le V_{IN} \le V_{CC}$	−20		30	μA
I_{CC}	Active Supply Current	$I_{OUT} = 0$, $T_A = 25°C$		200	300	mA

Connection Diagram

Dual-In-Line Package



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Top View

FIGURE 4-1

Order Number NS32016D or NS32016N
See NS Package Number D48A or N48A

4.0 Device Specifications (Continued)

4.4 SWITCHING CHARACTERISTICS

4.4.1 Definitions

All the timing specifications given in this section refer to 2.0V on the rising or falling edges of the clock phases PHI1 and PHI2 and 0.8V or 2.0V on all other signals as illustrated in *Figures 4-2* and *4-3*, unless specifically stated otherwise.

ABBREVIATIONS:

L.E. — leading edge R.E. — rising edge
T.E. — trailing edge F.E. — falling edge

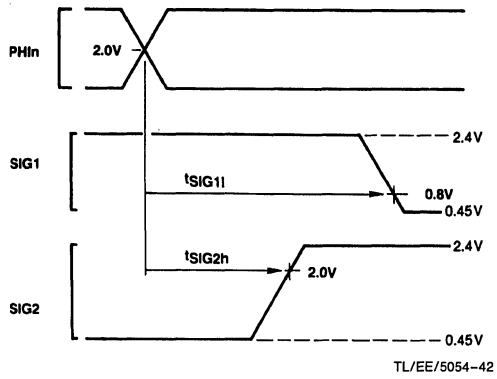

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FIGURE 4-2. Timing Specification Standard (Signal Valid After Clock Edge)

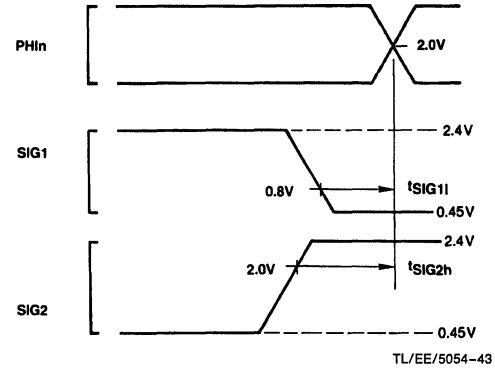

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FIGURE 4-3. Timing Specification Standard (Signal Valid Before Clock Edge)

4.4.2 Timing Tables

4.4.2.1 Output Signals: Internal Propagation Delays, NS32016-10

Maximum times assume capacitive loading of 100 pF.

Name	Figure	Description	Reference/Conditions	NS32016-10		Units
				Min	Max	
t_{ALv}	4-4	Address bits 0–15 valid	after R.E., PHI1 T1		40	ns
t_{ALh}	4-4	Address bits 0–15 hold	after R.E., PHI1 Tmmu or T2	5		ns
t_{Dv}	4-4	Data valid (write cycle)	after R.E., PHI1 T2		50	ns
t_{Dh}	4-4	Data hold (write cycle)	after R.E., PHI1 next T1 or Ti	0		ns
t_{AHv}	4-4	Address bits 16–23 valid	after R.E., PHI1 T1		40	ns
t_{AHh}	4-4	Address bits 16–23 hold	after R.E., PHI1 next T1 or Ti	0		ns
t_{ALADSs}	4-5	Address bits 0–15 setup	before $\overline{ADS}$ T.E.	25		ns
t_{AHADSs}	4-5	Address bits 16–23 set up	before $\overline{ADS}$ T.E.	25		ns
t_{ALADSh}	4-9	Address bits 0–15 hold	after $\overline{ADS}$ T.E.	15		ns
t_{AHADSh}	4-9	Address bits 16–23 hold	after $\overline{ADS}$ T.E.	15		ns
t_{ALf}	4-5	Address bits 0–15 floating (no MMU)	after R.E., PHI1 T2		25	ns
t_{ALMf}	4-9	Address bits 0–15 floating (with MMU)	after R.E., PHI1 Tmmu		25	ns
t_{AHMf}	4-9	Address bits 16–23 floating (with MMU)	after R.E., PHI1 Tmmu		25	ns
t_{HBEv}	4-4	$\overline{HBE}$ signal valid	after R.E., PHI1 T1		50	ns
t_{HBEh}	4-4	$\overline{HBE}$ signal hold	after R.E., PHI1 next T1 or Ti	0		ns
t_{STv}	4-4	Status (ST0–ST3) valid	after R.E., PHI1 T4 (before T1, see note)		45	ns
t_{STh}	4-4	Status (ST0–ST3) hold	after R.E., PHI1 T4 (after T1)	0		ns
t_{DDINv}	4-5	$\overline{DDIN}$ signal valid	after R.E., PHI1 T1		50	ns

4.0 Device Specifications (Continued)

4.4.2.1 Output Signals: Internal Propagation Delays, NS32016-10 (Continued)

Name	Figure	Description	Reference/Conditions	NS32016-10		Units
				Min	Max	
t_{DDINh}	4-5	$\overline{DDIN}$ signal hold	after R.E., PHI1 next T1 or Ti	0		ns
t_{ADSa}	4-4	$\overline{ADS}$ signal active (low)	after R.E., PHI1 T1		35	ns
t_{ADSia}	4-4	$\overline{ADS}$ signal inactive	after R.E., PHI2 T1		40	ns
t_{ADSw}	4-4	$\overline{ADS}$ pulse width	at 0.8V (both edges)	30		ns
t_{DSa}	4-4	$\overline{DS}$ signal active (low)	after R.E., PHI1 T2		40	ns
t_{DSia}	4-4	$\overline{DS}$ signal inactive	after R.E., PHI1 T4		40	ns
t_{ALf}	4-6	AD0–AD15 floating (caused by $\overline{HOLD}$)	after R.E., PHI1 T1		25	ns
t_{AHf}	4-6	A16–A23 floating (caused by $\overline{HOLD}$)	after R.E., PHI1 T1		25	ns
t_{DSf}	4-6	$\overline{DS}$ floating (caused by $\overline{HOLD}$)	after R.E., PHI1 Ti		50	ns
t_{ADSf}	4-6	$\overline{ADS}$ floating (caused by $\overline{HOLD}$)	after R.E., PHI1 Ti		50	ns
t_{HBEf}	4-6	$\overline{HBE}$ floating (caused by $\overline{HOLD}$)	after R.E., PHI1 Ti		50	ns
t_{DDINf}	4-6	$\overline{DDIN}$ floating (caused by $\overline{HOLD}$)	after R.E., PHI1 Ti		50	ns
t_{HLDAa}	4-6	$\overline{HLDA}$ signal active (low)	after R.E., PHI1 Ti		30	ns
t_{HLDAia}	4-8	$\overline{HLDA}$ signal inactive	after R.E., PHI1 Ti		40	ns
t_{DSr}	4-8	$\overline{DS}$ signal returns from floating (caused by $\overline{HOLD}$)	after R.E., PHI1 Ti		55	ns
t_{ADSr}	4-8	$\overline{ADS}$ signal returns from floating (caused by $\overline{HOLD}$)	after R.E., PHI1 Ti		55	ns
t_{HBEr}	4-8	$\overline{HBE}$ signal returns from floating (caused by $\overline{HOLD}$)	after R.E., PHI1 Ti		55	ns
t_{DDINr}	4-8	$\overline{DDIN}$ signal returns from floating (caused by $\overline{HOLD}$)	after R.E., PHI1 Ti		55	ns
t_{DDINf}	4-9	$\overline{DDIN}$ signal floating (caused by $\overline{FLT}$)	after $\overline{FLT}$ F.E.		55	ns
t_{HBEl}	4-9	$\overline{HBE}$ signal low (caused by $\overline{FLT}$)	after $\overline{FLT}$ F.E.		35	ns
t_{DDINr}	4-10	$\overline{DDIN}$ signal returns from floating (caused by $\overline{FLT}$)	after $\overline{FLT}$ F.E.		40	ns
t_{HBEr}	4-10	$\overline{HBE}$ signal returns from LOW (caused by $\overline{FLT}$)	after $\overline{FLT}$ F.E.		35	ns
t_{SPCa}	4-13	$\overline{SPC}$ output active (low)	after R.E., PHI1 T1		35	ns
t_{SPCia}	4-13	$\overline{SPC}$ output inactive	after R.E., PHI1 T4		35	ns
t_{SPCnf}	4-15	$\overline{SPC}$ output nonforcing	after R.E., PHI2 T4		30	ns
t_{Dv}	4-13	Data valid (slave processor write)	after R.E., PHI1 T1		50	ns
t_{Dh}	4-13	Data hold (slave processor write)	after R.E., PHI1 next T1 or Ti	0		ns
t_{PFSw}	4-18	$\overline{PFS}$ pulse width	at 0.8V (both edges)	50		ns
t_{PFSa}	4-18	$\overline{PFS}$ pulse active (low)	after R.E., PHI2		40	ns
t_{PFSia}	4-18	$\overline{PFS}$ pulse inactive	after R.E., PHI2		40	ns
t_{ILOs}	4-20a	$\overline{ILO}$ signal setup	before R.E., PHI1 T1 of first interlocked write cycle	50		ns
t_{ILOh}	4-20b	$\overline{ILO}$ signal hold	after R.E., PHI1 T3 of last interlocked read cycle	10		ns
t_{ILOa}	4-21	$\overline{ILO}$ signal active (low)	after R.E., PHI1		35	ns

4.0 Device Specifications (Continued)

4.4.2.1 Output Signals: Internal Propagation Delays, NS32016-10 (Continued)

Name	Figure	Description	Reference/Conditions	NS32016-10		Units
				Min	Max	
t_{ILOia}	4-21	$\overline{ILO}$ signal inactive	after R.E., PHI1		35	ns
t_{USv}	4-22	U/$\overline{S}$ signal valid	after R.E., PHI1 T4		35	ns
t_{USh}	4-22	U/$\overline{S}$ signal hold	after R.E., PHI1 T4	8		ns
t_{NSPF}	4-19b	Nonsequential fetch to next $\overline{PFS}$ clock cycle	after R.E., PHI1 T1	4		t_{Cp}
t_{PFNS}	4-19a	$\overline{PFS}$ clock cycle to next non-sequential fetch	before R.E., PHI1 T1	4		t_{Cp}
t_{LXPF}	4-29	Last operand transfer of an instruction to next $\overline{PFS}$ clock cycle	before R.E., PHI1 T1 of first bus cycle of transfer	0		t_{Cp}

Note: Every memory cycle starts with T4, during which Cycle Status is applied. If the CPU was idling, the sequence will be: ". . . Ti, T4, T1 . . .". If the CPU was not idling, the sequence will be: ". . . T4, T1 . . .".

4.4.2.2 Input Signal Requirements: NS32016-10

Name	Figure	Description	Reference/Conditions	NS32016-10		Units
				Min	Max	
t_{PWR}	4-25	Power stable to $\overline{RST}$ R.E.	after V_{CC} reaches 4.5V	50		μs
t_{DIs}	4-5	Data in setup (read cycle)	before F.E., PHI2 T3	15		ns
t_{DIh}	4-5	Data in hold (read cycle)	after R.E., PHI1 T4	3		ns
t_{HLDa}	4-6	$\overline{HOLD}$ active (low) setup time (see note)	before F.E., PHI2 TX1	25		ns
t_{HLDia}	4-8	$\overline{HOLD}$ inactive setup time	before F.E., PHI2 Ti	25		ns
t_{HLDh}	4-6	$\overline{HOLD}$ hold time	after R.E., PHI1 TX2	0		ns
t_{FLTa}	4-9	$\overline{FLT}$ active (low) setup time	before F.E., PHI2 Tmmu	25		ns
t_{FLTia}	4-11	$\overline{FLT}$ inactive setup time	before F.E., PHI2 T2	25		ns
t_{RDYs}	4-11, 4-12	RDY setup time	before F.E., PHI2 T2 or T3	15		ns
t_{RDYh}	4-11, 4-12	RDY hold time	after F.E., PHI1 T3	5		ns
t_{ABTs}	4-23	$\overline{ABT}$ setup time ($\overline{FLT}$ inactive)	before F.E., PHI2 Tmmu	20		ns
t_{ABTs}	4-24	$\overline{ABT}$ setup time ($\overline{FLT}$ active)	before F.E., PHI2 T_f	20		ns
t_{ABTh}	4-23	$\overline{ABT}$ hold time	after R.E., PHI1	0		ns
t_{RSTs}	4-25, 4-26	$\overline{RST}$ setup time	before F.E., PHI1	15		ns
t_{RSTw}	4-26	$\overline{RST}$ pulse width	at 0.8V (both edges)	64		t_{Cp}
t_{INTs}	4-27	$\overline{INT}$ setup time	before F.E., PHI1	25		ns
t_{NMIw}	4-28	$\overline{NMI}$ pulse width	at 0.8V (both edges)	70		ns
t_{DIs}	4-14	Data setup (slave read cycle)	before F.E., PHI2 T1	15		ns
t_{DIh}	4-14	Data hold (slave read cycle)	after R.E., PHI1 T4	3		ns
t_{SPCd}	4-15	$\overline{SPC}$ pulse delay from slave	after R.E., PHI2 T4	25		ns
t_{SPCs}	4-15	$\overline{SPC}$ setup time	before F.E., PHI1	25		ns
t_{SPCw}	4-15	$\overline{SPC}$ pulse width from slave processor (async.input)	at 0.8V (both edges)	20		ns

4.0 Device Specifications (Continued)

4.4.2.2 Input Signal Requirements: NS32016-10 (Continued)

Name	Figure	Description	Reference/Conditions	NS32016-10		Units
				Min	Max	
t_{ATh}	4-16	$\overline{AT}/\overline{SPC}$ hold for address translation strap	after F.E., PHI1 of cycle during which $\overline{RST}$ pulse is removed	2		t_{Cp}
t_{ATs}	4-16	$\overline{AT}/\overline{SPC}$ setup for address translation strap	before R.E., PHI1 of cycle during which $\overline{RST}$ pulse is removed	1		t_{Cp}

Note: This setup time is necessary to ensure prompt acknowledgement via $\overline{HLDA}$ and the ensuing floating of CPU off the buses. Note that the time from the receipt of the $\overline{HOLD}$ signal until the CPU floats is a function of the time $\overline{HOLD}$ signal goes low, the state of the RDY input (in MMU systems), and the length of the current MMU cycle.

4.2.3 Clocking Requirements: NS32016-10

Name	Figure	Description	Reference/ Conditions	NS32016-10		Units
				Min	Max	
t_{Cp}	4-17	Clock period	R.E., PHI1, PHI2 to next R.E., PHI1, PHI2	100	250	ns
t_{CLw}	4-17	PHI1, PHI2 pulse width	at 2.0V on PHI1, PHI2 (both edges)	0.5 t_{Cp} − 10 ns		
t_{CLh}	4-17	PHI1, PHI2 high time	at V_{CC} − 0.9V on PHI1, PHI2 (both edges)	0.5 t_{Cp} − 15 ns		
t_{CLl}	4-17	PHI1, PHI2 low time	at 0.8V on PHI1, PHI2	0.5 t_{Cp} − 5 ns		
$t_{nOVL(1,2)}$	4-17	Non-overlap time	0.8V on F.E., PHI1, PHI2 to 0.8V on R.E., PHI2, PHI1	−2	5	ns
t_{nOVLas}		Non-overlap asymmetry ($t_{nOVL(1)} - t_{nOVL(2)}$)	At 0.8V on PHI1, PHI2	−4	4	ns
t_{CLwas}		PHI1, PHI2 asymmetry ($t_{CLw(1)} - t_{CLw(2)}$)	At 2.0V on PHI1, PHI2	−5	5	ns

4.0 Device Specifications (Continued)

4.4.3 Timing Diagrams

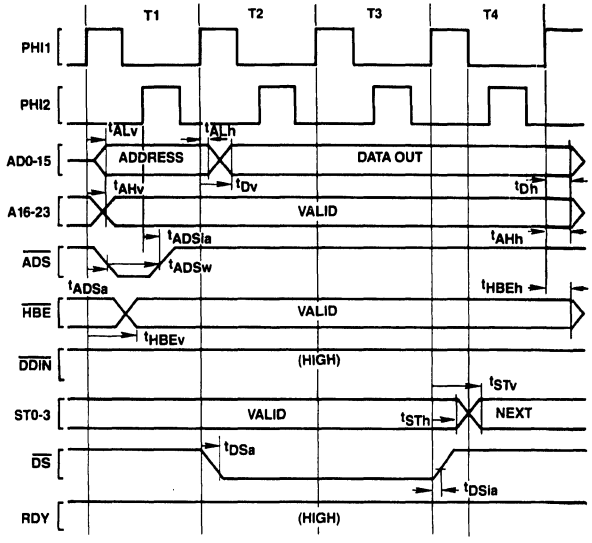

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FIGURE 4-4. Write Cycle

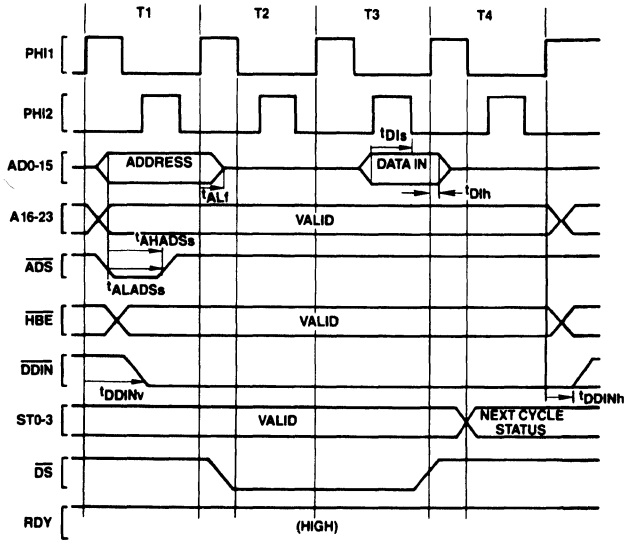

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FIGURE 4-5. Read Cycle

4.0 Device Specifications (Continued)

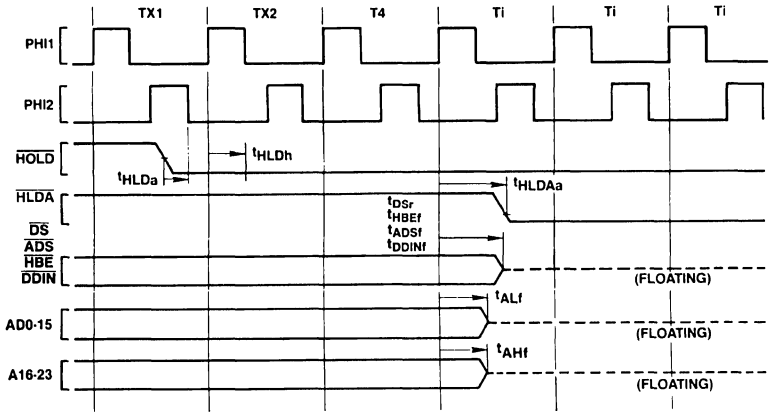

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FIGURE 4-6. Floating by $\overline{\text{HOLD}}$ Timing (CPU Not Idle Initially)

Note that whenever the CPU is not idling (not in Ti), the $\overline{\text{HOLD}}$ request ($\overline{\text{HOLD}}$ low) must be active t_{HLDa} before the falling edge of PHI2 of the clock cycle that appears two clock cycles before T4 (TX1) and stay low until t_{HLDh} after the rising edge of PHI1 of the clock cycle that precedes T4 (TX2) for the request to be acknowledged.

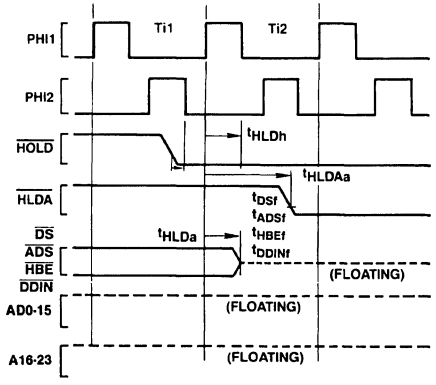

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FIGURE 4-7. Floating by $\overline{\text{HOLD}}$ Timing (CPU Initially Idle)

Note that during Ti1 the CPU is already idling.

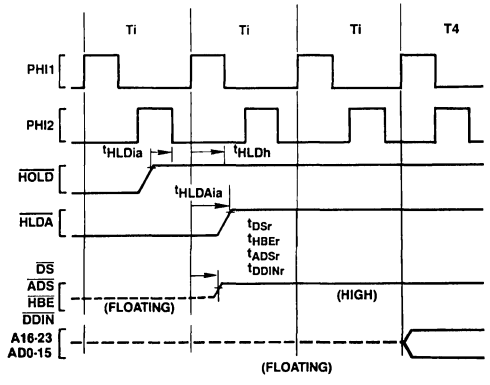

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FIGURE 4-8. Release from $\overline{\text{HOLD}}$

4.0 Device Specifications (Continued)

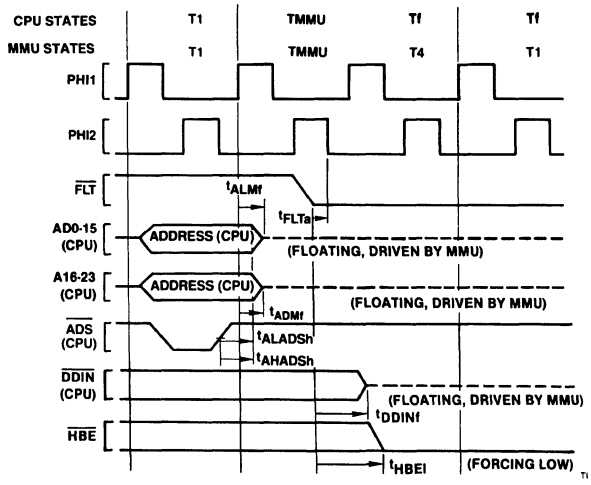

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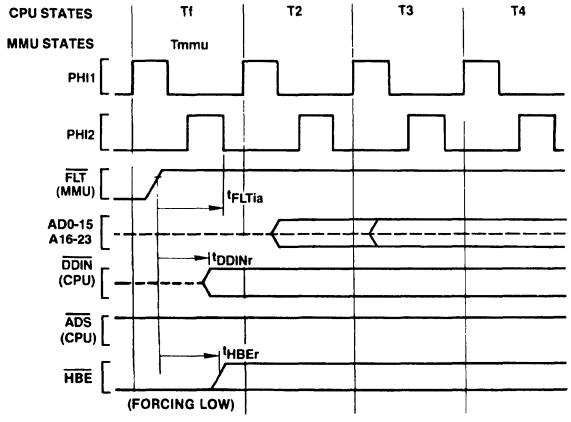
FIGURE 4-9. $\overline{\text{FLT}}$ Initiated Cycle Timing



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Note that when $\overline{\text{FLT}}$ is deasserted the CPU restarts driving $\overline{\text{DDIN}}$ before the MMU releases it. This, however, does not cause any conflict, since both CPU and MMU force $\overline{\text{DDIN}}$ to the same logic level.

FIGURE 4-10. Release from $\overline{\text{FLT}}$ Timing

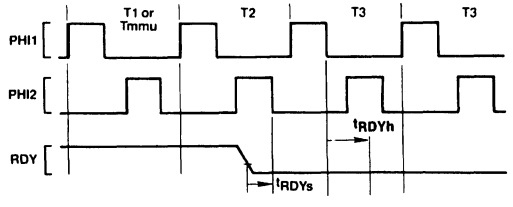

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FIGURE 4-11. Ready Sampling (CPU Initially READY)

4.0 Device Specifications (Continued)

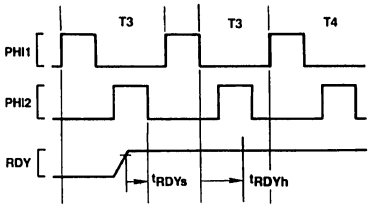

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FIGURE 4-12. Ready Sampling (CPU Initially NOT READY)

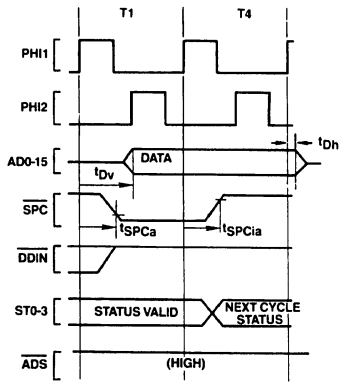

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FIGURE 4-13. Slave Processor Write Timing

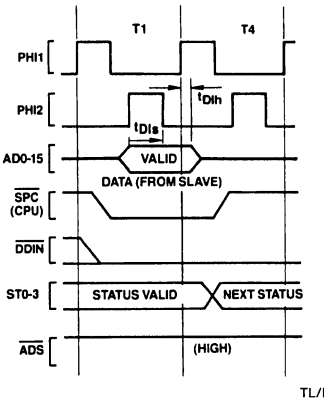

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FIGURE 4-14. Slave Processor Read Timing

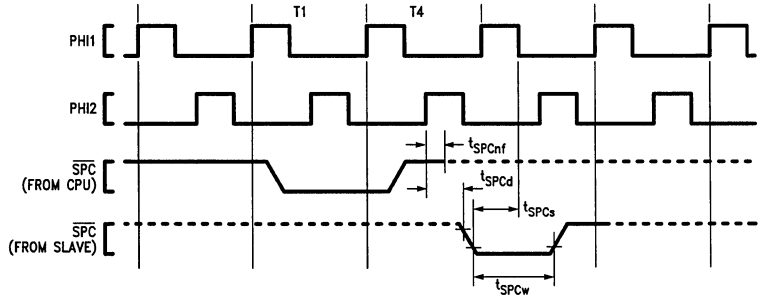

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FIGURE 4-15. $\overline{SPC}$ Timing

After transferring last operand to a Slave Processor, CPU turns OFF driver and holds $\overline{SPC}$ high with internal 5 kΩ pullup.

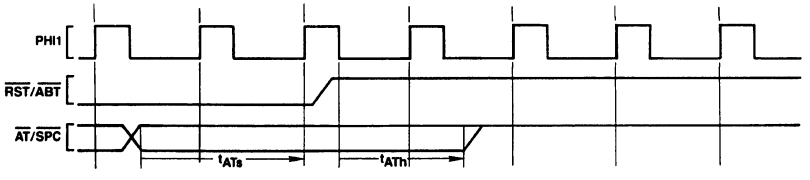

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FIGURE 4-16. Reset Configuration Timing

4.0 Device Specifications (Continued)

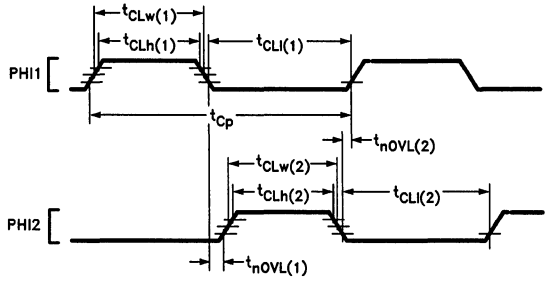

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FIGURE 4-17. Clock Waveforms

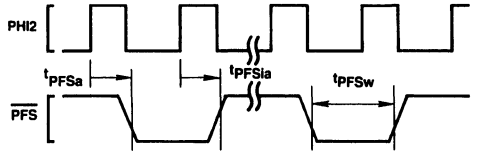

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FIGURE 4-18. Relationship of $\overline{PFS}$ to Clock Cycles

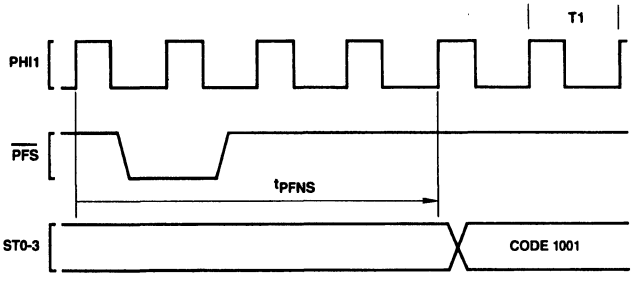

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FIGURE 4-19a. Guaranteed Delay, $\overline{PFS}$ to Non-Sequential Fetch

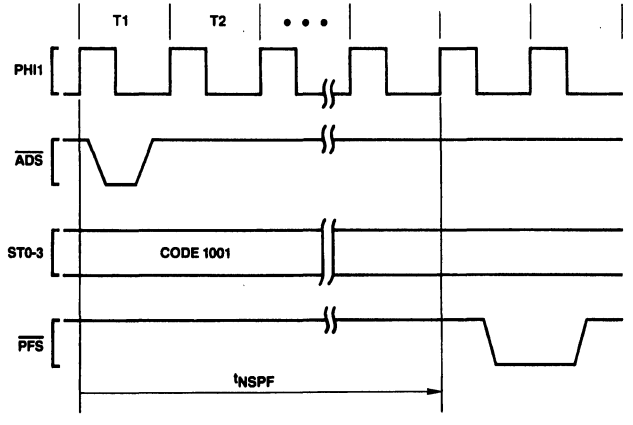

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FIGURE 4-19b. Guaranteed Delay, Non-Sequential Fetch to $\overline{PFS}$

4.0 Device Specifications (Continued)

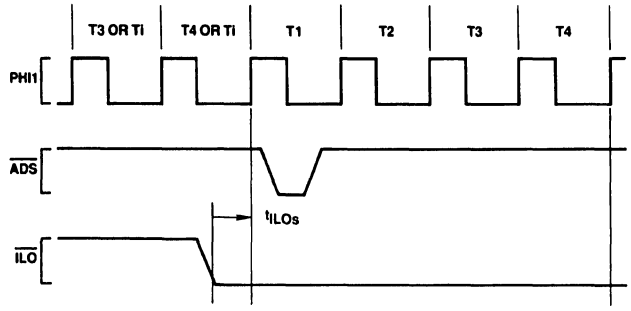

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FIGURE 4-20a. Relationship of $\overline{ILO}$ to First Operand Cycle of an Interlocked Instruction

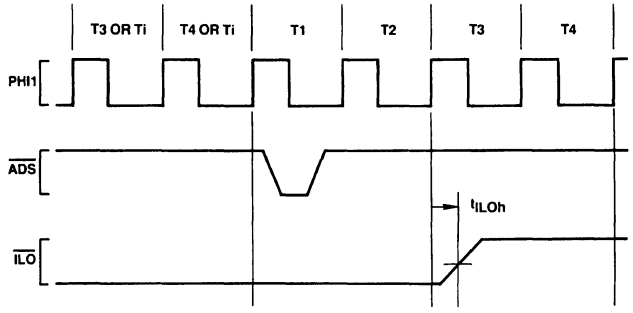

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FIGURE 4-20b. Relationship of $\overline{ILO}$ to Last Operand Cycle of an Interlocked Instruction

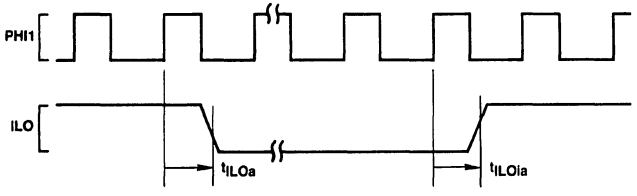

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FIGURE 4-21. Relationship of $\overline{ILO}$ to Any Clock Cycle

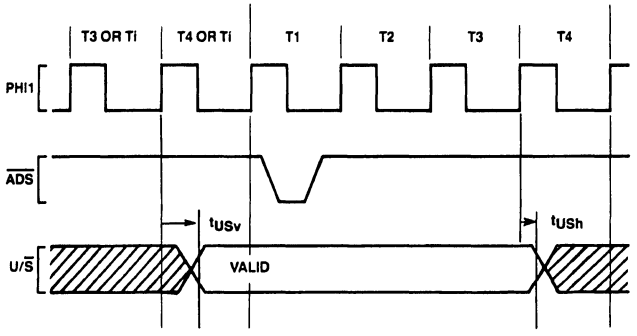

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FIGURE 4-22. U/$\overline{S}$ Relationship to Any Bus Cycle— Guaranteed Valid Interval

4.0 Device Specifications (Continued)

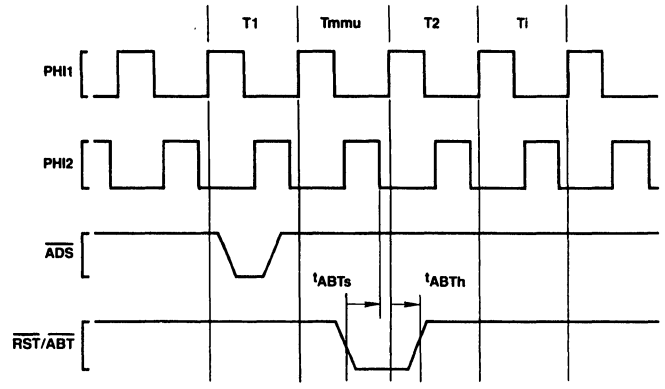

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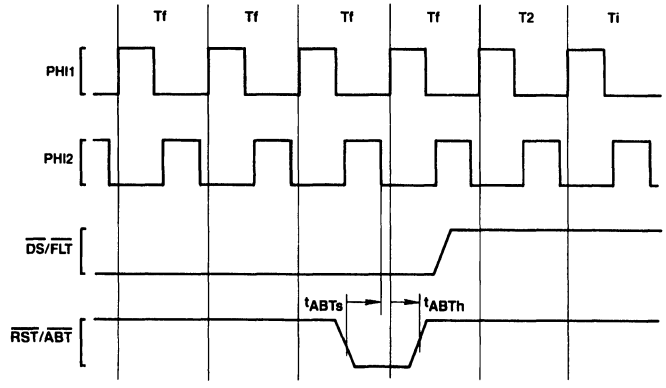
FIGURE 4-23. Abort Timing, $\overline{FLT}$ Not Applied



TL/EE/5054–66

FIGURE 4-24. Abort Timing, $\overline{FLT}$ Applied

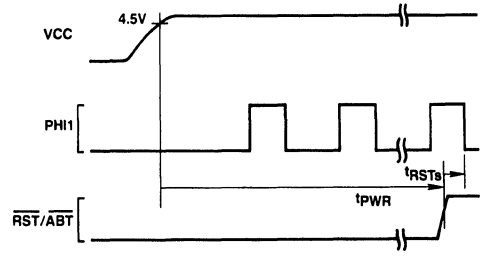


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FIGURE 4-25. Power-On Reset

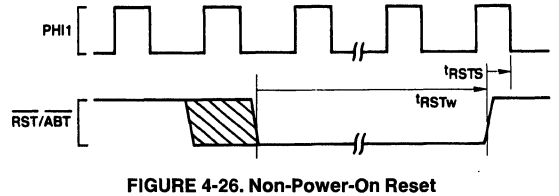

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FIGURE 4-26. Non-Power-On Reset

4.0 Device Specifications (Continued)

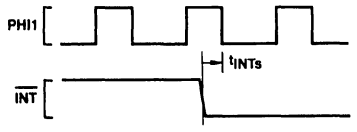

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FIGURE 4-27. $\overline{INT}$ Interrupt Signal Detection

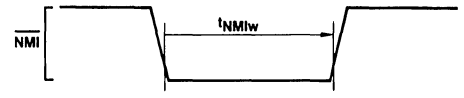

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FIGURE 4-28. $\overline{NMI}$ Interrupt Signal Timing

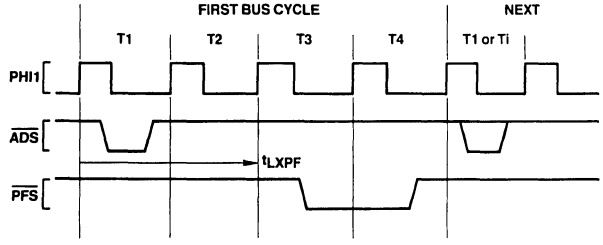

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FIGURE 4-29. Relationship Between Last Data Transfer of an Instruction and $\overline{PFS}$ Pulse of Next Instruction

NOTE:

In a transfer of a Read-Modify-Write type operand, this is the Read transfer, displaying RMW Status (Code 1011).

Appendix A: Instruction Formats

NOTATIONS:

i = Integer Type Field
B = 00 (Byte)
W = 01 (Word)
D = 11 (Double Word)

f = Floating Point Type Field
F = 1 (Std. Floating: 32 bits)
L= 0 (Long Floating: 64 bits)

c = Custom Type Field
D = 1 (Double Word)
Q = 0 (Quad Word)

op = Operation Code
Valid encodings shown with each format.

gen, gen 1, gen 2 = General Addressing Mode Field
See Sec. 2.2 for encodings.

reg = General Purpose Register Number

cond = Condition Code Field
0000 = EQual: Z = 1
0001 = Not Equal: Z = 0
0010 = Carry Set: C = 1
0011 = Carry Clear: C = 0
0100 = Higher: L = 1
0101 = Lower or Same: L = 0
0110 = Greater Than: N = 1
0111 = Less or Equal: N = 0
1000 = Flag Set: F = 1
1001 = Flag Clear: F = 0
1010 = LOwer: L = 0 and Z = 0
1011 = Higher or Same: L = 1 or Z = 1
1100 = Less Than: N = 0 and Z = 0
1101 = Greater or Equal: N = 1 or Z = 1
1110 = (Unconditionally True)
1111 = (Unconditionally False)

short = Short Immediate Value. May contain:
quick: Signed 4-bit value, in MOVQ, ADDQ, CMPQ, ACB.
cond: Condition Code (above), in Scond.
areg: CPU Dedicated Register, in LPR, SPR.
0000 = US
0001 – 0111 = (Reserved)
1000 = FP
1001 = SP
1010 = SB
1011 = (Reserved)
1100 = (Reserved)
1101 = PSR
1110 = INTBASE
1111 = MOD

Options: in String Instructions

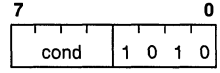
U/W	B	T

T = Translated
B = Backward
U/W = 00: None
01: While Match
11: Until Match

Configuration bits, in SETCFG:

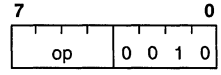
C	M	F	I

mreg: NS32082 Register number, in LMR, SMR.
0000 = BPR0
0001 = BPR1
0010 = (Reserved)
0011 = (Reserved)
0100 = (Reserved)
0101 = (Reserved)
0110 = (Reserved)
0111 = (Reserved)
1000 = (Reserved)
1001 = (Reserved)
1010 = MSR
1011 = BCNT
1100 = PTB0
1101 = PTB1
1110 = (Reserved)
1111 = EIA



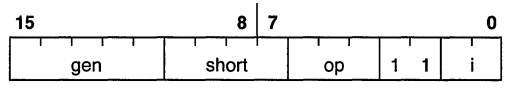
Format 0

Bcond (BR)



Format 1

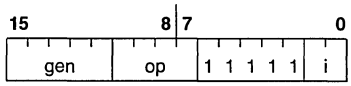
BSR	–0000	ENTER	–1000
RET	–0001	EXIT	–1001
CXP	–0010	NOP	–1010
RXP	–0011	WAIT	–1011
RETT	–0100	DIA	–1100
RETI	–0101	FLAG	–1101
SAVE	–0110	SVC	–1110
RESTORE	–0111	BPT	–1111



Format 2

ADDQ	–000	ACB	–100
CMPQ	–001	MOVQ	–101
SPR	–010	LPR	–110
Scond	–011		

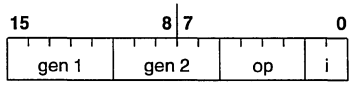
Appendix A: Instruction Formats (Continued)



Format 3

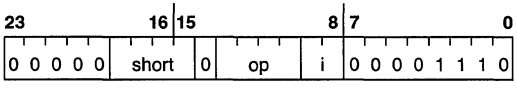
CXPD	−0000	ADJSP	−1010
BICPSR	−0010	JSR	−1100
JUMP	−0100	CASE	−1110
BISPSR	−0110		

Trap (UND) on XXX1, 1000



Format 4

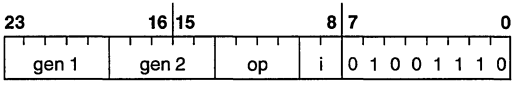
ADD	−0000	SUB	−1000
CMP	−0001	ADDR	−1001
BIC	−0010	AND	−1010
ADDC	−0100	SUBC	−1100
MOV	−0101	TBIT	−1101
OR	−0110	XOR	−1110



Format 5

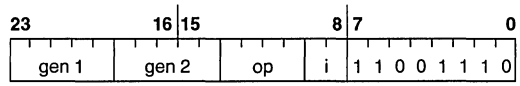
MOVS	−0000	SETCFG	−0010
CMPS	−0001	SKPS	−0011

Trap (UND) on 1XXX, 01XX



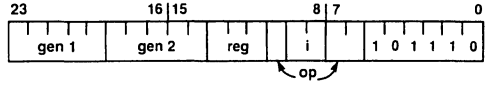
Format 6

ROT	−0000	NEG	−1000
ASH	−0001	NOT	−1001
CBIT	−0010	Trap (UND)	−1010
CBITI	−0011	SUBP	−1011
Trap (UND)	−0100	ABS	−1100
LSH	−0101	COM	−1101
SBIT	−0110	IBIT	−1110
SBITI	−0111	ADDP	−1111



Format 7

MOVM	−0000	MUL	−1000
CMPM	−0001	MEI	−1001
INSS	−0010	Trap (UND)	−1010
EXTS	−0011	DEI	−1011
MOVXBW	−0100	QUO	−1100
MOVZBW	−0101	REM	−1101
MOVZiD	−0110	MOD	−1110
MOVXiD	−0111	DIV	−1111



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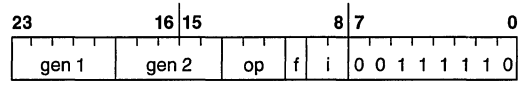
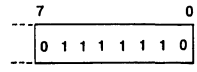
Format 8

EXT	−000	INDEX	−100
CVTP	−001	FFS	−101
INS	−010		
CHECK	−011		
MOVSU	−110, reg=001		
MOVUS	−110, reg=011		



Format 9

MOVif	−000	ROUND	−100
LFSR	−001	TRUNC	−101
MOVLF	−010	SFSR	−110
MOVFL	−011	FLOOR	−111



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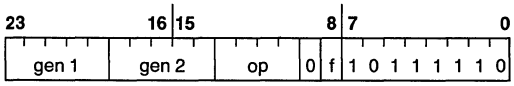
Format 10

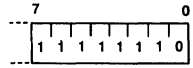
Trap (UND) Always

Appendix A: Instruction Formats (Continued)



Format 11

ADDf	−0000	DIVf	−1000
MOVf	−0001	Trap (SLAVE)	−1001
CMPf	−0010	Trap (UND)	−1010
Trap (SLAVE)	−0011	Trap (UND)	−1011
SUBf	−0100	MULf	−1100
NEGf	−0101	ABSf	−1101
Trap (UND)	−0110	Trap (UND)	−1110
Trap (UND)	−0111	Trap (UND)	−1111



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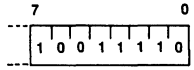
Format 12

Trap (UND) Always



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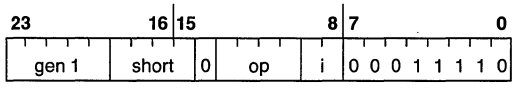
Format 13

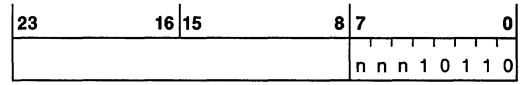
Trap (UND) Always



Format 14

RDVAL	−0000	LMR	−0010
WRVAL	−0001	SMR	−0011

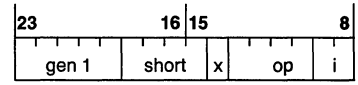
Trap (UND) on 01XX, 1XXX



Format 15
(Custom Slave)

nnn **Operation Word Format**

000

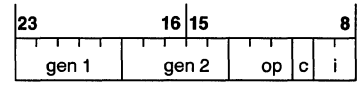


Format 15.0

CATST0	−0000	LCR	−0010
CATST1	−0001	SCR	−0011

Trap (UND) on all others

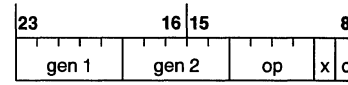
001



Format 15.1

CCV3	−000	CCV2	−100
LCSR	−001	CCV1	−101
CCV5	−010	SCSR	−110
CCV4	−011	CCV0	−111

101

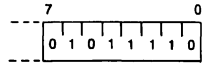


Format 15.5

CCAL0	−0000	CCAL3	−1000
CMOV0	−0001	CMOV3	−1001
CCMP0	−0010	Trap (UND)	−1010
CCMP1	−0011	Trap (UND)	−1011
CCAL1	−0100	CCAL2	−1100
CMOV2	−0101	CMOV1	−1101
Trap (UND)	−0110	Trap (UND)	−1110
Trap (UND)	−0111	Trap (UND)	−1111

If nnn = 010, 011, 100, 110, 111
then Trap (UND) Always

Appendix A: Instruction Formats (Continued)



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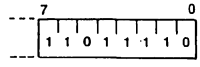
Format 16

Trap (UND) Always



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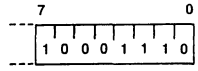
Format 17

Trap (UND) Always



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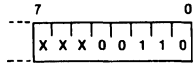
Format 18

Trap (UND) Always



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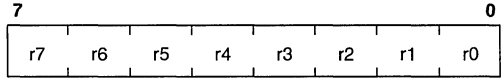
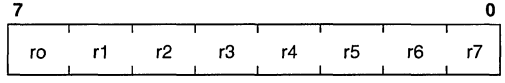
Format 19

Trap (UND) Always

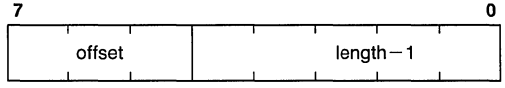
Implied Immediate Encodings:



Register Mask, appended to SAVE, ENTER



Register Mask, appended to RESTORE, EXIT



Offset/Length Modifier appended to INSS, EXTS

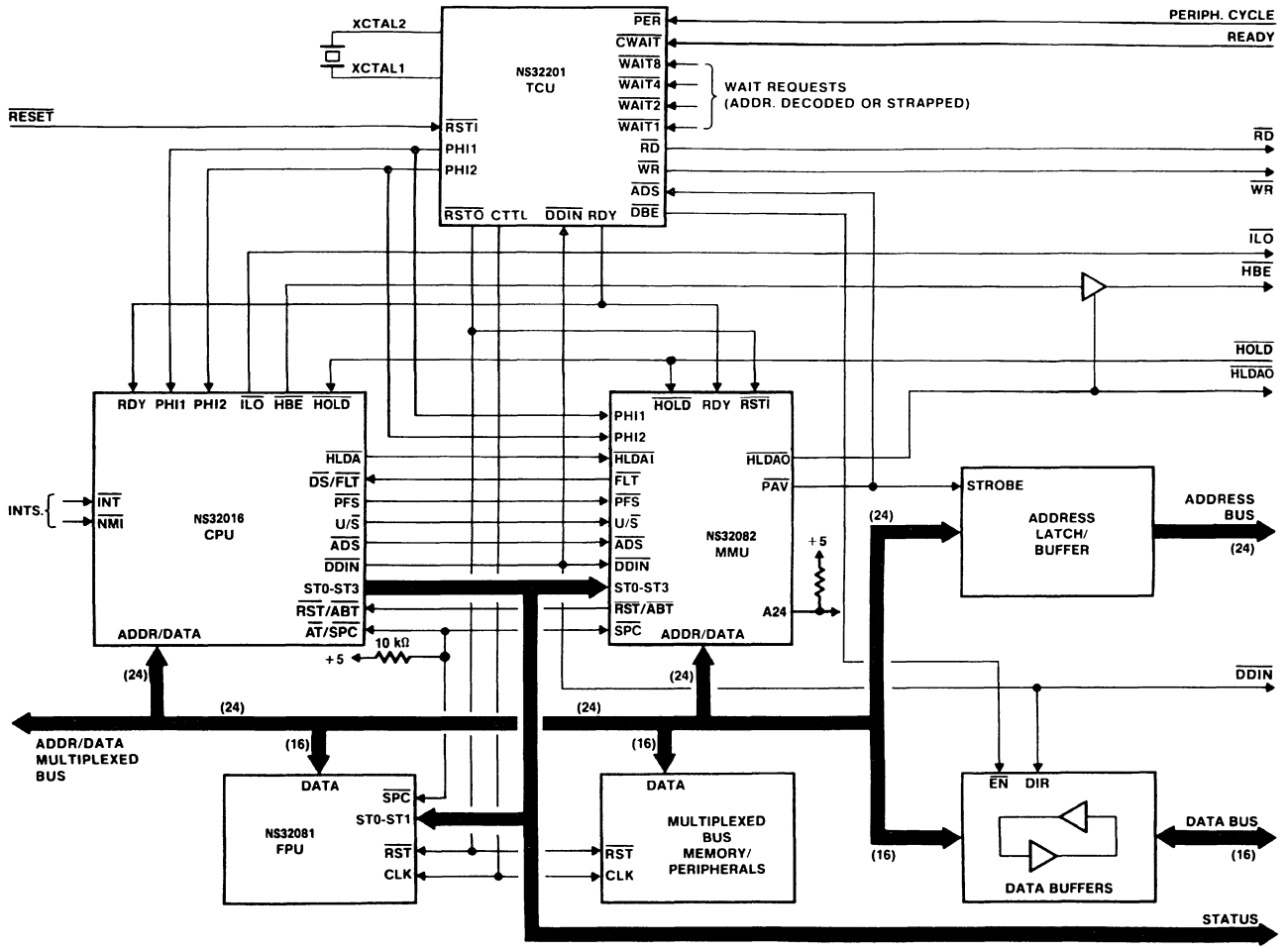


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FIGURE B-1. System Connection Diagram

National Semiconductor

NS32008-10 High-Performance 8-Bit Microprocessor

General Description

The NS32008 is a 32-bit microprocessor with a 16-MByte linear address space and a 8-bit external data bus. It has a 32-bit ALU, eight 32-bit general purpose registers, a four-byte prefetch queue, and a slave processor interface. The NS32008 is fabricated with National Semiconductor's advanced XMOS™ process, and is fully object code compatible with other Series 32000® processors. The Series 32000 instructions set is optimized for modular high-level languages (HLL). The set is very symmetric, it has a two address format, and it incorporates HLL oriented addressing modes. The capabilities of the NS32008 can be expanded with the use of the NS32081 floating point unit (FPU), which interfaces to the NS32008 as a slave processor. The NS32008 is a general purpose microprocessor that is ideal for a wide range of computational intensive applications.

Features

- 32-bit architecture and implementation
- 16-MByte linear address space
- 8-bit external data bus
- Powerful instruction set
  - — General 2-address capability
  - — High degree of symmetry
  - — Addressing modes optimized for high-level languages
- Series 32000 slave processor support
- High-speed XMOS technology
- 48-pin dual-in-line (DIP) package

Block Diagram

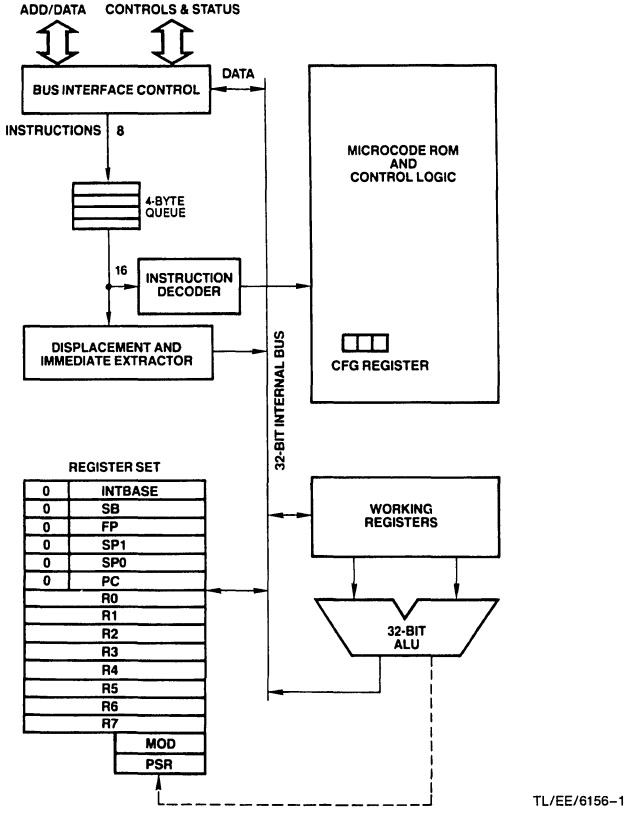

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Table of Contents

List of Illustrations

List of Illustrations (Continued)

List of Tables

1.0 Product Introduction

The Series 32000 Microprocessor family is a new generation of devices using National's XMOS and CMOS technologies. By combining state-of-the-art MOS technology with a very advanced architectural design philosophy, this family brings mainframe computer processing power to VLSI processors.

The Series 32000 family supports a variety of system configurations, extending from a minimum low-cost system to a powerful 4 gigabyte system. The architecture provides complete upward compatibility from one family member to another. The family consists of a selection of CPUs supported by a set of peripherals and slave processors that provide sophisticated interrupt and memory management facilities as well as high-speed floating-point operations. The architectural features of the Series 32000 family are described briefly below:

Powerful Addressing Modes. Nine addressing modes available to all instructions are included to access data structures efficiently.

Data Types. The architecture provides for numerous data types, such as byte, word, doubleword, and BCD, which may be arranged into a wide variety of data structures.

Symmetric Instruction Set. While avoiding special case instructions that compilers can't use, the Series 32000 family incorporates powerful instructions for control operations, such as array indexing and external procedure calls, which save considerable space and time for compiled code.

Memory-to-Memory Operations. The Series 32000 CPUs represent two-address machines. This means that each operand can be referenced by any one of the addressing modes provided. This powerful memory-to-memory architecture permits memory locations to be treated as registers for all useful operations. This is important for temporary operands as well as for context switching.

Memory Management. Either the NS32382 or the NS32082 Memory Management Unit may be added to the system to provide advanced operating system support functions, including dynamic address translation, virtual memory management, and memory protection.

Large, Uniform Addressing. The NS32008 has 24-bit address pointers that can address up to 16 megabytes without requiring any segmentation; this addressing scheme provides flexible memory management without added-on expense.

Modular Software Support. Any software package for the Series 32000 family can be developed independent of all other packages, without regard to individual addressing. In addition, ROM code is totally relocatable and easy to access, which allows a significant reduction in hardware and software cost.

Software Processor Concept. The Series 32000 architecture allows future expansions of the instruction set that can be executed by special slave processors, acting as extensions to the CPU. This concept of slave processors is unique to the Series 32000 family. It allows software compatibility even for future components because the slave hardware is transparent to the software. With future advances in semiconductor technology, the slaves can be physically integrated on the CPU chip itself.

To summarize, the architectural features cited above provide three primary performance advantages and characteristics:

- High-Level Language Support
- Easy Future Growth Path
- Application Flexibility

1.1 NS32008 DESIGN GOALS

The NS32008 is aimed at small to medium size systems, and is designed to bridge the gap between 8-bit CPUs and the higher-end members of the Series 32000 family. The NS32008 provides an 8-bit data bus and is the only CPU in the Series 32000 family that does not support virtual memory.

The NS32008 is most suitable for systems designed with 8-bit memory and peripherals.

2.0 Architectural Description

2.1 PROGRAMMING MODEL

The Series 32000 architecture includes 16 registers on the NS32008 CPU.

2.1.1 General Purpose Registers

There are eight registers for meeting high-speed general storage requirements, such as holding temporary variables and addresses. The general purpose registers are free for any use by the programmer. They are 32 bits in length. If a general register is specified for an operand that is 8 or 16 bits long, only the low part of the register is used; the high part is not referenced or modified.

2.1.2 Dedicated Registers

The eight dedicated registers of the NS32008 are assigned specific functions:

PC: The PROGRAM COUNTER register is a pointer to the first byte of the instruction currently being executed. The PC

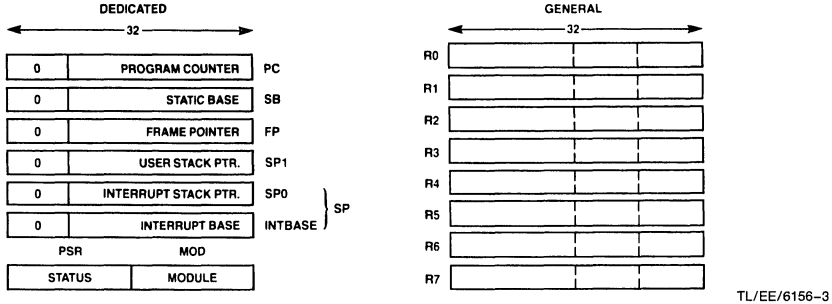

FIGURE 2-1. The General and Dedicated Registers

2.0 Architectural Description (Continued)

is used to reference memory in the program section. (In the NS32008, the upper eight bits of this register are always zero.)

SP0, SP1: The SP0 register points to the lowest address of the last item stored on the INTERRUPT STACK. This stack is normally used only by the operating system. It is used primarily for storing temporary data, and holding return information for operating system subroutines and interrupt and trap service routines. The SP1 register points to the lowest address of the last item stored on the USER STACK. This stack is used by normal user programs to hold temporary data and subroutine return information.

In this document, reference is made to the SP register. The terms "SP register" or "SP" refer to either SP0 or SP1, depending on the setting of the S bit in the PSR register. If the S bit in the PSR is 0, then SP refers to SP0. If the S bit in the PSR is 1, the SP refers to SP1. (In the NS32008, the upper eight bits of these registers are always zero.)

Stacks in the Series 32000 family grow downward in memory. A push operation pre-decrements the stack pointer by the operand length. A pop operation post-increments the stack pointer by the operand length.

FP: The FRAME POINTER register is used by a procedure to access parameters and local variables on the stack. The FP register is set up on procedure entry with the ENTER instruction and restored on procedure termination with the EXIT instruction.

The frame pointer holds the address in memory occupied by the old contents of the frame pointer. (In the NS32008, the upper eight bits of this register are always zero.)

SB: The STATIC BASE register points to the global variables of a software module. This register is used to support relocatable global variables for software modules. The SB register holds the lowest address in memory occupied by the global variables of a module. (In the NS32008, the upper eight bits of this register are always zero.)

INTBASE: The INTERRUPT BASE register holds the address of the dispatch table for interrupts and traps (Section 3.7). The INTBASE register holds the lowest address in memory occupied by the dispatch table. (In the NS32008, the upper eight bits of this register are always zero.)

MOD: The MODULE register holds the address of the module descriptor of the currently executing software module. The MOD register is 16 bits long, therefore the module table must be contained within the first 64K bytes of memory.

PSR: The PROCESSOR STATUS REGISTER holds the status codes for the NS32008 microprocessor.

The PSR is 16 bits long, divided into two 8-bit halves (*Figure 2-2*). The low order eight bits are accessible to all programs, but the high order eight bits are accessible only to programs executing in Supervisor Mode.

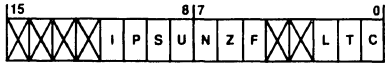

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FIGURE 2-2. The Processor Status Register

C: The C bit indicates that a carry or borrow occurred after an addition or subtraction instruction. It can be used with the ADDC and SUBC instructions to perform multiple-precision integer arithmetic calculations. It may have a setting of 0 (no carry or borrow) or 1 (carry or borrow).

T: The T bit causes program tracing. If this bit is a 1, a TRC trap is executed after every instruction (Section 3.7.5).

L: The L bit is altered by comparison instructions. In a comparison instruction, the L bit is set to "1" if the second operand is less than the first operand, when both operands are interpreted as unsigned integers. Otherwise, it is set to "0". In Floating-Point comparisons, this bit is always cleared.

F: The F bit is a general condition flag, which is altered by many instructions (e.g., integer arithmetic instructions use it to indicate overflow).

Z: The Z bit is altered by comparison instructions. In a comparison instruction, the Z bit is set to "1" if the second operand is equal to the first operand; otherwise it is set to "0".

N: The N bit is altered by comparison instructions. In a comparison instruction, the N bit is set to "1" if the second operand is less than the first operand, when both operands are interpreted as signed integers. Otherwise, it is set to "0".

U: If the U bit is "1", no privileged instructions may be executed. if the U bit is "0", then all instructions may be executed. When U=0, the NS32008 is said to be in Supervisor Mode; when U=1, the NS32008 is said to be in User Mode. A User Mode program is restricted from executing certain instructions and accessing certain registers which could interfere with the operating system. For example, a User Mode program is prevented from changing the setting of the flag used to indicate its own privilege mode. A Supervisor Mode program is assumed to be a trusted part of the operating system, hence it has no such restrictions.

S: The S bit specifies whether the SP0 register on SP1 register is used as the stack pointer. The bit is automatically cleared on interrupts and traps it. It may have a setting of 0 (use the SP0 register) or 1 (use the SP1 register).

P: The P bit prevents a TRC trap from occurring more than once for an instruction (Section 3.7.5). It may have a setting of 0 (no trace pending) or 1 (trace pending).

I: If I = 1, then all interrupts will be accepted (Section 3.7). If I = 0, only the $\overline{\text{NMI}}$ interrupt is accepted. Trap enables are not affected by this bit.

2.1.3 The Configuration Register (CFG)

Within the Control section of the NS32008 CPU is the 4-bit CFG Register, which declares the presence of certain external devices. It is referenced by only one instruction, SETCFG, which is intended to be executed only as part of system initialization after reset. The format of the CFG Register is shown in *Figure 2-3*.

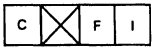

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FIGURE 2-3. CFG Register

The CFG I bit declares the presence of external interrupt vectoring circuitry (specifically, the NS32202 Interrupt Control Unit). If the CFG I bit is set, interrupts requested through the INT pin are "Vectored." If it is clear, these interrupts are "Non-Vectored." See Section 3.7.

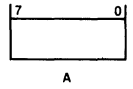
The F and C bits declare the presence of the FPU and Custom Slave Processors. If these bits are not set, the corresponding instructions are trapped as being undefined.

2.1.4 Memory Organization

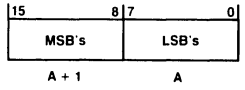
The main memory of the NS32008 is a uniform linear address space. Memory locations are numbered sequentially

2.0 Architectural Description (Continued)

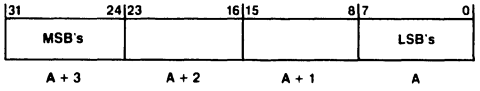
starting at zero and ending at $2^{24}-1$. The number specifying a memory location is called an address. The contents of each memory location is a byte consisting of eight bits (*Figure 2-4A*). Unless otherwise noted, diagrams in this document show data stored in memory with the lowest address on the right and the highest address on the left. Also, when data is shown vertically, the lowest address is at the top of a diagram and the highest address at the bottom of the diagram. When bits are numbered in a diagram, the least significant bit is given the number zero, and is shown at the right of the diagram. Bits are numbered in increasing significance and toward the left.



A. Byte at Address A



B. Word at Address A



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C. Double Word at Address A

FIGURE 2-4. Data Formats for NS32008 Memory

Two contiguous bytes are called a word (*Figure 2-4B*). Except where noted (Section 2.2.1), the least significant byte of a word is stored at the lower address, and the most significant byte of the word is stored at the next higher address. In memory, the address of a word is the address of its least significant byte, and a word may start at any address.

Two contiguous words are called a double word (*Figure 2-4C*). Except where noted (Section 2.2.1), the least significant word of a double word is stored at the lowest address and the most significant word of the double word is stored at the address two greater. In memory, the address of a double word is the address of its least significant byte, and a double word may start at any address.

2.1.5 Dedicated Tables

Two of the NS32008 dedicated registers (MOD and INTBASE) serve as pointers to dedicated tables in memory.

The INTBASE register points to the Interrupt Dispatch and Cascade tables. These are described in Section 3.7.

The MOD register contains a pointer into the Module Table, whose entries are called Module Descriptors. A Module Descriptor contains four pointers, three of which are used by the NS32008. The MOD register contains the address of the Module Descriptor for the currently running module. It is automatically updated by the Call External Procedure instructions (CXP and CXPD).

The format of a Module Descriptor is shown in *Figure 2-5*. The Static Base entry contains the address of static data assigned to the running module. It is loaded into the CPU Static Base register by the CXP and CXPD instructions. The Program Base entry contains the address of the first byte of instruction code in the module. Since a module may have multiple entry points, the Program Base pointer serves only as a reference to find them.

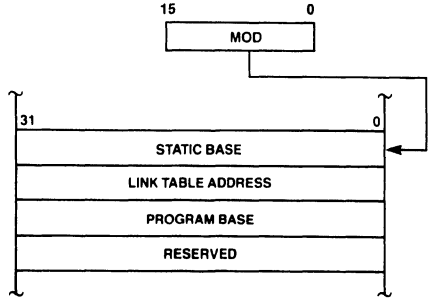

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FIGURE 2-5. Module Descriptor Format

The Link Table Address points to the Link Table for the currently running module. The Link Table provides the information needed for:

1. Sharing variables between modules. Such variables are accessed through the Link Table via the External addressing mode.
2. Transferring control from one module to another. This is done via the Call External Procedure (CXP) instruction.

The format of a Link Table is given in *Figure 2-6*. A Link Table Entry for an external variable contains the 32-bit address of that variable. An entry for an external procedure contains two 16-bit fields: Module and Offset. The Module field contains the new MOD register contents for the module being entered. The Offset field is an unsigned number giving the position of the entry point relative to the new module's Program Base pointer.

For further details of the functions of these tables, see the Series 32000 Instruction Set Reference Manual.

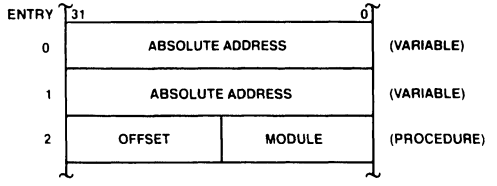

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FIGURE 2-6. A Sample Link Table

2.0 Architectural Description (Continued)

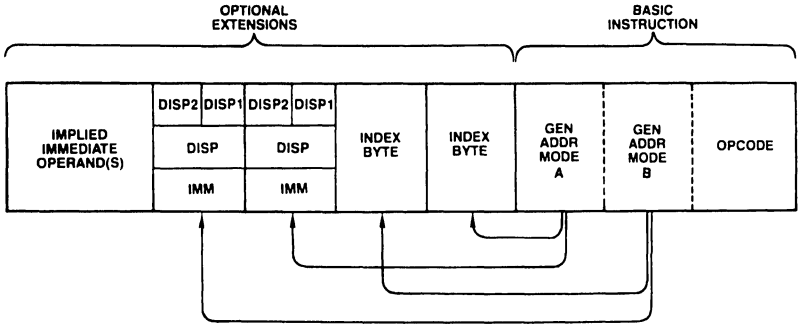

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FIGURE 2-7. General Instruction Format

2.2 INSTRUCTION SET

2.2.1 General Instruction Format

Figure 2-7 shows the general format of a Series 32000 instruction. The Basic Instruction is one to three bytes long and contains the opcode and up to two 5-bit General Addressing Mode ("Gen") fields. Following the Basic Instruction field is a set of optional extensions which may appear, depending on the instruction and the addressing modes selected.

Index Bytes appear when either or both Gen fields specify Scaled Index. In this case, the Gen field specifies only the Scale Factor (1, 2, 4 or 8), and the Index Byte specifies which General Purpose register to use as the index, and which addressing mode calculation to perform before indexing. See *Figure 2-8*.

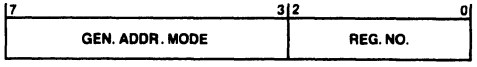

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FIGURE 2-8. Index Byte Format

Following Index Bytes come any displacements (addressing constants) or immediate values associated with the selected addressing modes. Each Displacement/Immediate field may contain one or two displacements, or one immediate value. The size of a Displacement field is encoded within the top bits of that field, as shown in *Figure 2-9*, with the remaining bits interpreted as a signed (two's complement) value. The size of an Immediate value is determined from the Opcode field. Both Displacement and Immediate fields are stored most-significant byte first. Note that this is different from the memory representation of data (Section 2.1.4.).

Some instructions require additional, "implied" immediates and/or displacements, apart from those associated with addressing modes. Any such extensions appear at the end of the instruction, in the order that they appear within the list of operands in the instruction definition (Section 2.2.3).

2.2.2 Addressing Modes

The NS32008 CPU generally accesses an operand by calculating its Effective Address based on information available when the operand is to be accessed. The method to be used in performing this calculation is specified by the programmer as an "addressing mode."

Addressing modes in the NS32008 are designed to optimally support high-level language accesses to variables. In nearly all cases, a variable access requires only one addressing mode, within the instruction that acts upon that variable. Extraneous data movement is therefore minimized.

NS32008 Addressing Modes fall into nine basic types:

Register: The operand is available in one of the eight General Purpose Registers. In certain Slave Processor instructions, an auxiliary set of eight registers may be referenced instead.

Register Relative: A General Purpose Register contains an address to which is added a displacement value from the instruction, yielding the effective address of the operand in memory.

Memory Space: Identical to Register Relative above, except that the register used is one of the dedicated registers PC, SP, SB or FP. These registers point to data areas generally needed by high-level languages.

Memory Relative: A pointer variable is found within the memory space pointed to by the SP, SB or FP register. A displacement is added to that pointer to generate the Effective Address of the operand.

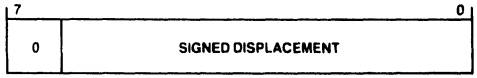
Immediate: The operand is encoded within the instruction. This addressing mode is not allowed if the operand is to be written.

Absolute: The address of the operand is specified by a displacement field in the instruction.

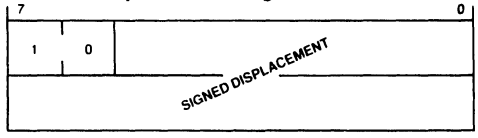
External: A pointer value is read from a specified entry of the current Link Table. To this pointer value is added a displacement, yielding the Effective Address of the operand.

2.0 Architectural Description (Continued)

Byte Displacement: Range −64 to +63



Word Displacement: Range −8192 to +8191



Double Word Displacement: Range (Entire Addressing Space)

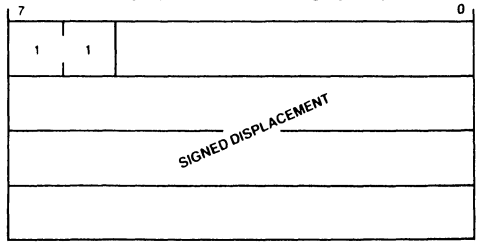


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FIGURE 2-9. Displacement Encodings

Top of Stack: The currently-selected Stack Pointer (SP0 or SP1) specifies the location of the operand. The operand is pushed or popped, depending on whether it is written or read.

Scaled Index: Although encoded as an addressing mode, Scaled Indexing is an option on any addressing mode except Immediate or another Scaled Index. It has the effect of calculating an Effective Address, then multiplying any General Purpose Register by 1, 2, 4 or 8 and adding it into the total, yielding the final Effective Address of the operand.

Table 2-1 is a brief summary of the addressing modes. For a complete description of their actions, see the Instruction Set Reference Manual.

2.2.3 Instruction Set Summary

Table 2-2 presents a brief description of the NS32008 instruction set. The Format column refers to the Instruction Format tables (Appendix A). The Instruction column gives the instruction as coded in assembly language, and the Description column provides a short description of the function provided by that instruction. Further details of the exact operations performed by each instruction may be found in the Instruction Set Reference Manual.

Notations:

i = Integer length suffix: B = Byte
W = Word
D = Double Word

f = Floating-Point length suffix: F = Standard Floating
L = Long Floating

gen = General operand. Any addressing mode can be specified.

short = A 4-bit value encoded within the Basic Instruction. (See Appendix A for encodings.)

imm = Immediate operand. An 8-bit value appended after any addressing extensions.

disp = Displacement (addressing constant): 8, 16, 32 bits. All three lengths legal.

reg = Any General Purpose Register: R0–R7.

areg = Any Dedicated/Address Register: SP, SB, FP, MOD, INTBASE, PSR, UPSR, (bottom eight PSR bits).

creg = A Custom Slave Processor Register (implementation dependent).

cond = Any condition code, encoded as a 4-bit field within the Basic Instruction. (See Appendix A for encodings.)

2.0 Architectural Description (Continued)

TABLE 2-1
NS32008 Addressing Modes

ENCODING	MODE	ASSEMBLER SYNTAX	EFFECTIVE ADDRESS
Register			
00000	Register 0	R0 or F0	None: Operand is in the specified register.
00001	Register 1	R1 or F1	
00010	Register 2	R2 or F2	
00011	Register 3	R3 or F3	
00100	Register 4	R4 or F4	
00101	Register 5	R5 or F5	
00110	Register 6	R6 or F6	
00111	Register 7	R7 or F7	
Register Relative			
01000	Register 0 relative	disp(R0)	Disp + Register.
01001	Register 1 relative	disp(R1)	
01010	Register 2 relative	disp(R2)	
01011	Register 3 relative	disp(R3)	
01100	Register 4 relative	disp(R4)	
01101	Register 5 relative	disp(R5)	
01110	Register 6 relative	disp(R6)	
01111	Register 7 relative	disp(R7)	
Memory Relative			
10000	Frame memory relative	disp2(disp1(FP))	Disp2 + Pointer; Pointer found at address Disp1 + Register. "SP" is either SP0 or SP1, as selected in PSR.
10001	Stack memory relative	disp2(disp1(SP))	
10010	Static memory relative	disp2(disp1(SB))	
Reserved			
10011	(Reserved for Future Use)		
Immediate			
10100	Immediate	value	None: Operand is input from instruction queue.
Absolute			
10101	Absolute	@disp	Disp.
External			
10110	External	EXT (disp1) + disp2	Disp2 + Pointer; Pointer is found at Link Table Entry number Disp1.
Top of Stack			
10111	Top of stack	TOS	Top of current stack, using either User or Interrupt Stack Pointer, as selected in PSR. Automatic Push/Pop included.
Memory Space			
11000	Frame memory	disp(FP)	Disp + Register; "SP" is either SP0 or SP1, as selected in PSR.
11001	Stack memory	disp(SP)	
11010	Static memory	disp(SB)	
11011	Program memory	* + disp	
Scaled Index			
11100	Index, bytes	mode[Rn:B]	EA (mode) + Rn.
11101	Index, words	mode[Rn:W]	EA (mode) + 2 × Rn.
11110	Index, double words	mode[Rn:D]	EA (mode) + 4 × Rn.
11111	Index, quad words	mode[Rn:Q]	EA (mode) + 8 × Rn. 'Mode' and 'n' are contained within the Index Byte. EA (mode) denotes the effective address generated using mode.

2.0 Architectural Description (Continued)

TABLE 2-2
NS32008 Instruction Set Summary

MOVES

Format	Operation	Operands	Description
4	MOVi	gen,gen	Move a value.
2	MOVQi	short,gen	Extend and move a signed 4-bit constant.
7	MOVMi	gen,gen,disp	Move multiple: disp bytes (1 to 16).
7	MOVZBW	gen,gen	Move with zero extension.
7	MOVZiD	gen,gen	Move with zero extension.
7	MOVXBW	gen,gen	Move with sign extension.
7	MOVXiD	gen,gen	Move with sign extension.
4	ADDR	gen,gen	Move effective address.

INTEGER ARITHMETIC

Format	Operation	Operands	Description
4	ADDi	gen,gen	Add.
2	ADDQi	short,gen	Add signed 4-bit constant.
4	ADDCi	gen,gen	Add with carry.
4	SUBi	gen,gen	Subtract.
4	SUBCi	gen,gen	Subtract with carry (borrow).
6	NEGi	gen,gen	Negate (2's complement).
6	ABSi	gen,gen	Take absolute value.
7	MULi	gen,gen	Multiply.
7	QUOi	gen,gen	Divide, rounding toward zero.
7	REMi	gen,gen	Remainder from QUO.
7	DIVi	gen,gen	Divide, rounding down.
7	MODi	gen,gen	Remainder from DIV (Modulus).
7	MEIi	gen,gen	Multiply to extended integer.
7	DEIi	gen,gen	Divide extended integer.

PACKED DECIMAL (BCD) ARITHMETIC

Format	Operation	Operands	Description
6	ADDPi	gen,gen	Add packed.
6	SUBPi	gen,gen	Subtract packed.

INTEGER COMPARISON

Format	Operation	Operands	Description
4	CMPi	gen,gen	Compare.
2	CMPQi	short,gen	Compare to signed 4-bit constant.
7	CMPMi	gen,gen,disp	Compare multiple: disp bytes (1 to 16).

LOGICAL AND BOOLEAN

Format	Operation	Operands	Description
4	ANDi	gen,gen	Logical AND.
4	ORi	gen,gen	Logical OR.
4	BICi	gen,gen	Clear selected bits.
4	XORi	gen,gen	Logical exclusive OR.
6	COMi	gen,gen	Complement all bits.
6	NOTi	gen,gen	Boolean complement: LSB only.
2	Scondi	gen	Save condition code (cond) as a Boolean variable of size i.

2.0 Architectural Description (Continued)

TABLE 2-2
Instruction Set Summary (Continued)

SHIFTS

Format	Operation	Operands	Description
6	LSHi	gen,gen	Logical shift, left or right.
6	ASHi	gen,gen	Arithmetic shift, left or right.
6	ROTi	gen,gen	Rotate, left or right.

BITS

Format	Operation	Operands	Description
4	TBITi	gen,gen	Test bit.
6	SBITi	gen,gen	Test and set bit.
6	SBITIi	gen,gen	Test and set bit, interlocked.
6	CBITi	gen,gen	Test and clear bit.
6	CBITIi	gen,gen	Test and clear bit, interlocked.
6	IBITi	gen,gen	Test and invert bit.
8	FFSi	gen,gen	Find first set bit.

BIT FIELDS

Bit fields are values in memory that are not aligned to byte boundaries. Examples are PACKED arrays and records used in Pascal. "Extract" instructions read and align a bit field. "Insert" instructions write a bit field from an aligned source.

Format	Operation	Operands	Description
8	EXTi	reg,gen,gen,disp	Extract bit field (array oriented).
8	INSi	reg,gen,gen,disp	Insert bit field (array oriented).
7	EXTSi	gen,gen,imm,imm	Extract bit field (short form).
7	INSSi	gen,gen,imm,imm	Insert bit field (short form).
8	CVTP	reg,gen,gen	Convert to bit field pointer.

ARRAYS

Format	Operation	Operands	Description
8	CHECKi	reg,gen,gen	Index bound check.
8	INDEXi	reg,gen,gen	Recursive indexing step for multiple-dimensional arrays.

STRINGS

String instructions assign specific functions to the General Purpose Registers:

R4 – Comparison Value
R3 – Translation Table Pointer
R2 – String 2 Pointer
R1 – String 1 Pointer
R0 – Limit Count

Options on all string instructions are:

B (Backward): Decrement string pointers after each step rather than incrementing.

U (Until match): End instruction if String 1 entry matches R4.

W (While match): End instruction if String 1 entry does not match R4.

All string instructions end when R0 decrements to zero.

Format	Operation	Operands	Description
5	MOVSi	options	Move String 1 to String 2.
	MOVST	options	Move string, translating bytes.
5	CMPSi	options	Compare String 1 to String 2.
	CMPST	options	Compare, translating String 1 bytes.
5	SKPSi	options	Skip over String 1 entries.
	SKPST	options	Skip, translating bytes for Until/While.

2.0 Architectural Description (Continued)

TABLE 2-2
Instruction Set Summary (Continued)

JUMPS AND LINKAGE

Format	Operation	Operands	Description
3	JUMP	gen	Jump.
0	BR	disp	Branch (PC Relative).
0	Bcond	disp	Conditional branch.
3	CASEi	gen	Multiway branch.
2	ACBi	short,gen,disp	Add 4-bit constant and branch if non-zero.
3	JSR	gen	Jump to subroutine.
1	BSR	disp	Branch to subroutine.
1	CXP	disp	Call external procedure.
3	CXPD	gen	Call external procedure using descriptor.
1	SVC		Supervisor call.
1	FLAG		Flag trap.
1	BPT		Breakpoint trap.
1	ENTER	[reg list],disp	Save registers and allocate stack frame. (Enter Procedure)
1	EXIT	[reg list]	Restore registers and reclaim stack frame. (Exit Procedure)
1	RET	disp	Return from subroutine.
1	RXP	disp	Return from external procedure call.
1	RETT	disp	Return from trap. (Privileged)
1	RETI		Return from interrupt. (Privileged)

CPU REGISTER MANIPULATION

Format	Operation	Operands	Description
1	SAVE	[reg list]	Save general purpose registers.
1	RESTORE	[reg list]	Restore general purpose registers.
2	LPRi	areg,gen	Load dedicated register. (Privileged if PSR or INTBASE)
2	SPRi	areg,gen	Store dedicated register. (Privileged if PSR or INTBASE)
3	ADJSPi	gen	Adjust stack pointer.
3	BISPSRi	gen	Set selected bits in PSR. (Privileged if not Byte length)
3	BICPSRi	gen	Clear selected bits in PSR. (Privileged if not Byte length)
5	SETCFG	[option list]	Set configuration register. (Privileged)

FLOATING POINT

Format	Operation	Operands	Description
11	MOVf	gen,gen	Move a floating point value.
9	MOVLF	gen,gen	Move and shorten a long value to standard.
9	MOVFL	gen,gen	Move and lengthen a standard value to long.
9	MOVif	gen,gen	Convert any integer to standard or long floating.
9	ROUNDfi	gen,gen	Convert to integer by rounding.
9	TRUNCfi	gen,gen	Convert to integer by truncating, toward zero.
9	FLOORfi	gen,gen	Convert to largest integer less than or equal to value.
11	ADDf	gen,gen	Add.
11	SUBf	gen,gen	Subtract.
11	MULf	gen,gen	Multiply.
11	DIVf	gen,gen	Divide.
11	CMPf	gen,gen	Compare.
11	NEGf	gen,gen	Negate.
11	ABSf	gen,gen	Take absolute value.
9	LFSR	gen	Load FSR.
9	SFSR	gen	Store FSR.

MISCELLANEOUS

Format	Operation	Operands	Description
1	NOP		No operation.
1	WAIT		Wait for interrupt.
1	DIA		Diagnose. Single-byte "Branch to Self" for hardware breakpointing. Not for use in programming.

2.0 Architectural Description (Continued)

TABLE 2-2
Instruction Set Summary (Continued)

CUSTOM SLAVE Format	Operation	Operands	Description
15.5	CCAL0c	gen,gen	Custom calculate.
15.5	CCAL1c	gen,gen	
15.5	CCAL2c	gen,gen	
15.5	CCAL3c	gen,gen	
15.5	CMOV0c	gen,gen	Custom move.
15.5	CMOV1c	gen,gen	
15.5	CMOV2c	gen,gen	
15.5	CMOV3c	gen,gen	
15.5	CCMP0c	gen,gen	Custom compare.
15.5	CCMP1c	gen,gen	
15.1	CCV0ci	gen,gen	Custom convert.
15.1	CCV1ci	gen,gen	
15.1	CCV2ci	gen,gen	
15.1	CCV3ic	gen,gen	
15.1	CCV4DQ	gen,gen	
15.1	CCV5QD	gen,gen	
15.1	LCSR	gen	Load custom status register.
15.1	SCSR	gen	Store custom status register.
15.0	CATST0	gen	Custom address/test. (Privileged)
15.0	CATST1	gen	(Privileged)
15.0	LCR	creg,gen	Load custom register. (Privileged)
15.0	SCR	creg,gen	Store custom register. (Privileged)

3.0 Functional Description

3.1 POWER AND GROUNDING

The NS32008 requires a single 5V power supply, applied on pin 48 (V_{CC}).

Grounding connections are made on two pins. Logic Ground (GNDL, pin 24) is the common pin for on-chip logic, and Buffer Ground (GNDB, pin 25) is the common pin for the output drivers. For optimal noise immunity, it is recommended that GNDL be attached through a single conductor directly to GNDB, and that all other grounding connections be made only to GNDB, as shown below (*Figure 3-1*).

In addition to V_{CC} and Ground, the NS32008 CPU uses an internally-generated negative voltage. It is necessary to filter this voltage externally by attaching a pair of capacitors (*Figure 3-1*) from the BBG pin to ground. Recommended values for these are:

C_1: 1 μF, Tantalum.

C_2: 1000 pF, low inductance. This should be either a disc or monolithic ceramic capacitor.

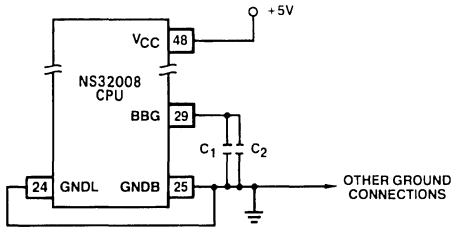

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FIGURE 3-1. Recommended Supply Connections

3.2 CLOCKING

The NS32008 inputs clocking signals from the NS32201 Timing Control Unit (TCU), which presents two non-overlapping phases of a single clock frequency. These phases are called PHI1 (pin 26) and PHI2 (pin 27). Their relationship to each other is shown in *Figure 3-2*.

Each rising edge of PHI1 defines a transition in the timing state ("T-State") of the CPU. One T-State represents the execution of one microinstruction within the CPU and/or one step of an external bus transfer. See Section 4 for complete specifications of PHI1 and PHI2.

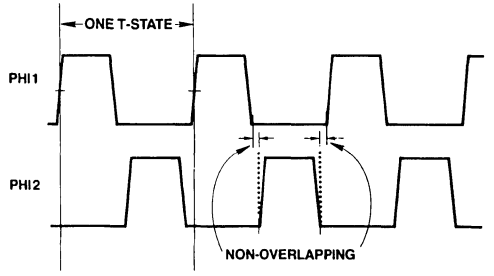

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FIGURE 3-2. Clock Timing Relationships

As the TCU presents signals with very fast transitions, it is recommended that the conductors carrying PHI1 and PHI2 be kept as short as possible, and that they not be

3.0 Functional Description (Continued)

connected anywhere except from the TCU to the CPU. A TTL clock signal (CTTL) is provided by the TCU for all other clocking.

3.3 RESETTING

The $\overline{RST}$ pin serves as a reset for on-chip logic. The CPU may be reset at any time by pulling the $\overline{RST}$ pin low for at least 64 clock cycles. Upon detecting a reset, the CPU terminates instruction processing, resets its internal logic, and clears the Program Counter (PC) and Processor Status Register (PSR) to all zeroes.

On application of power, $\overline{RST}$ must be held low for at least 50 μs after V_{CC} is stable. This is to ensure that all on-chip voltages are completely stable before operation. Whenever a Reset is applied, it must also remain active for not less than 64 clock cycles. The rising edge must occur while PHI1 is high. See *Figures 3-3* and *3-4*.

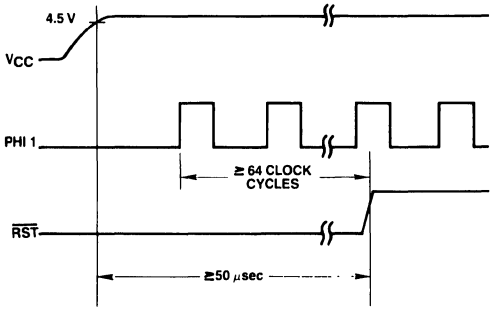

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FIGURE 3-3. Power-On Reset Requirements

The NS32201 Timing Contol Unit (TCU) provides circuitry to meet the Reset requirements of the NS32008 CPU. *Figure 3-5* shows the recommended connections.

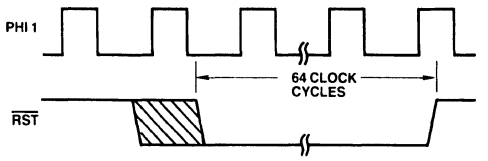

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FIGURE 3-4. General Reset Timing

3.4 BUS CYCLES

The NS32008 will perform a bus cycle for one of the following reasons:

1. To write or read data to or from memory or a peripheral interface device. Peripheral input and output are memory-mapped in the Series 32000 family.
2. To fetch instructions into the 4-byte instruction queue. This happens whenever the bus would otherwise be idle and the queue is not already full.
3. To acknowledge an interrupt and allow external circuitry to provide a vector number, or to acknowledge completion of an interrupt service routine.
4. To transfer information to or from a Slave Processor.

In terms of bus timing, cases 1 through 3 above are identical. For timing specifications, see Section 4. The only external difference between them is the 4-bit code placed on the Bus Status pins (ST0–ST3). Slave Processor cycles differ in that separate control signals are applied and transfers are performed 16 bits at a time (Section 3.4.6).

Figure 3-6 shows typical bus connections for the NS32008. The address, data, and control signals referenced in the following discussion are shown in this figure.

The sequence of events in a non-Slave Processor bus cycle is shown in *Figure 3-7* for a Read cycle and *Figure 3-8* for a Write cycle. The cases shown assume that the selected memory or interface device is capable of communicating with the CPU at full speed. If it is not, then cycle extension may be requested through the RDY line (Section 3.4.1).

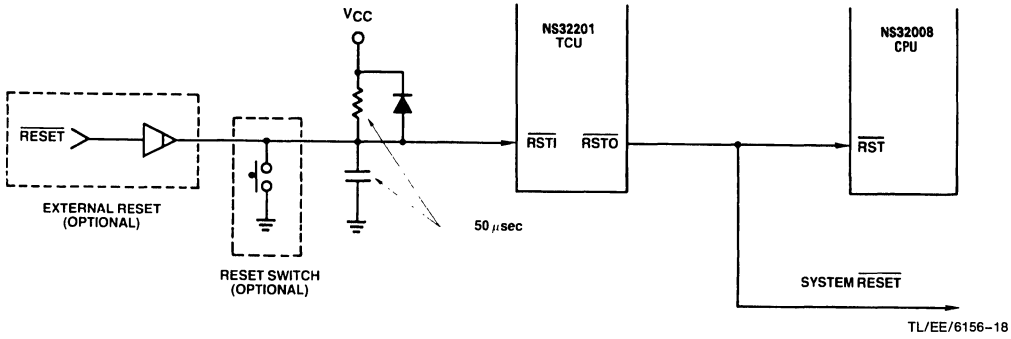

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FIGURE 3-5. Recommended Reset Connections

3.0 Functional Description (Continued)

A full-speed bus cycle is performed in four cycles of the PHI1 clock signal, labeled T1 through T4. Clock cycles not associated with a bus cycle are designated Ti (for "Idle").

During T1, the CPU applies an address on pins AD0–AD15 and A16–A23. It also provides a low-going pulse on the $\overline{ADS}$ pin, which serves the dual purpose of informing external circuitry that a bus cycle is starting and of providing control to an external latch for demultiplexing address bits 0–7 from the AD0–AD7 pins. See *Figure 3-6.* Also during this time the status signal $\overline{DDIN}$, indicating the direction of the transfer, becomes valid.

During T2, the CPU switches the Data Bus, AD0–AD7, to either accept or present data. Note that the signals AD8–AD15 and AD16–AD23 remain valid, and need not be latched. It also starts the Data Strobe ($\overline{DS}$), signaling the beginning of the data transfer. Associated signals from the NS32201 Timing Control Unit are also activated at this time: $\overline{RD}$ (Read Strobe) or $\overline{WR}$ (Write Strobe), $\overline{TSO}$ (Timing State Output, indicating that T2 has been reached) and $\overline{DBE}$ (Data Buffer Enable).

The T3 state provides for access time requirements, and it occurs at least once in a bus cycle. At the end of T2 or T3, on the falling edge of the PHI2 clock, the RDY (Ready) line is sampled to determine whether the bus cycle will be extended (Section 3.4.1).

If the CPU is performing a Read cycle, the Data Bus (AD0–AD7) is sampled at the falling edge of PHI2 of the last T3 state. See Timing Specification, Section 4. Data must, however, be held at least until the beginning of T4. $\overline{DS}$ and $\overline{RD}$ are guaranteed not to go inactive before this point, so the rising edge of either of them may safely be used to disable the device providing the input data.

The T4 state finishes the bus cycle. At the beginning of T4, the $\overline{DS}$, $\overline{RD}$ or $\overline{WR}$, and $\overline{TSO}$ signals go inactive, and at the rising edge of PHI2, $\overline{DBE}$ goes inactive, having provided for necessary data hold times. Data during Write cycles remains valid from the CPU throughout T4. Note that the Bus Status lines (ST0–ST3) change at the beginning of T4, anticipating the following bus cycle (if any).

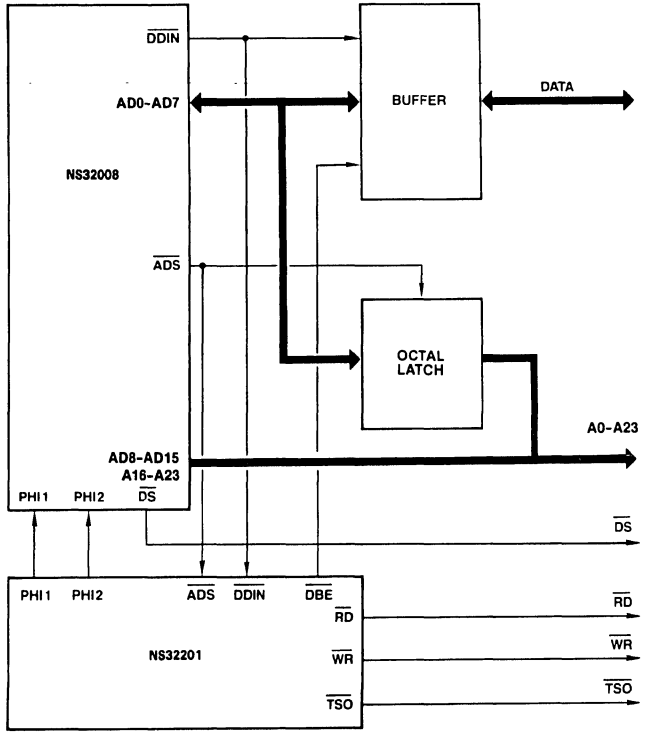

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FIGURE 3-6. Bus Connections

3.0 Functional Description (Continued)

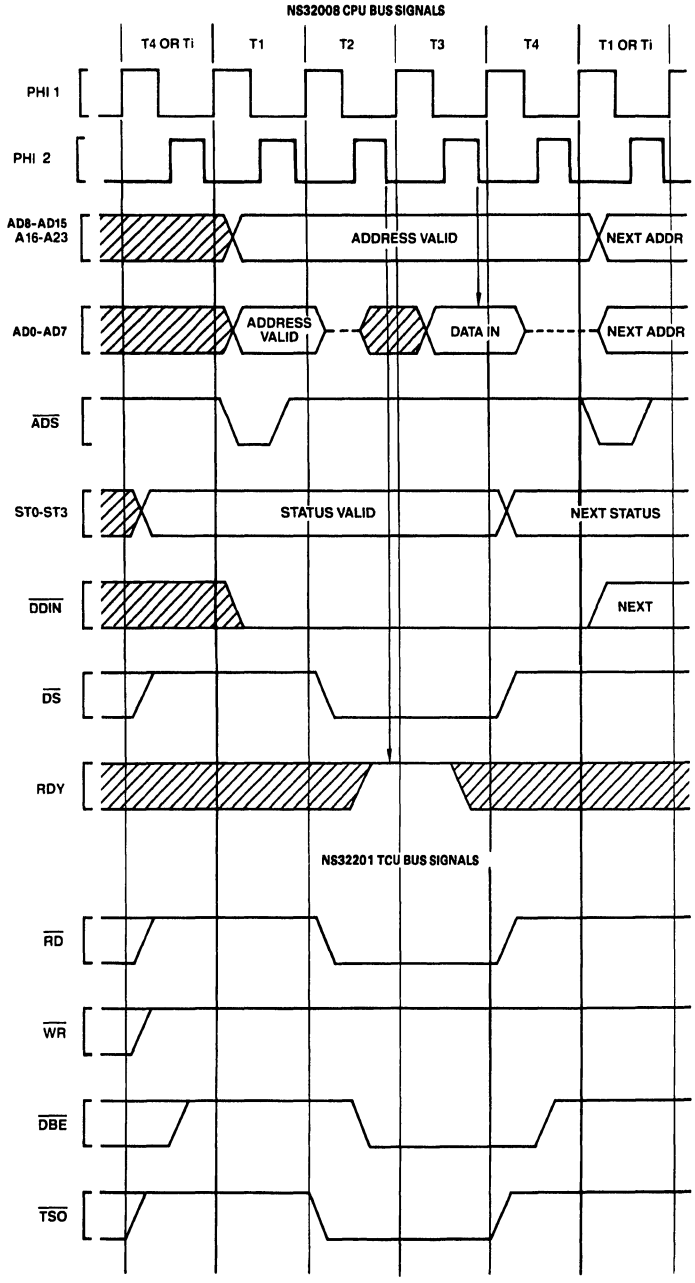

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FIGURE 3-7. Read Cycle Timing

3.0 Functional Description (Continued)

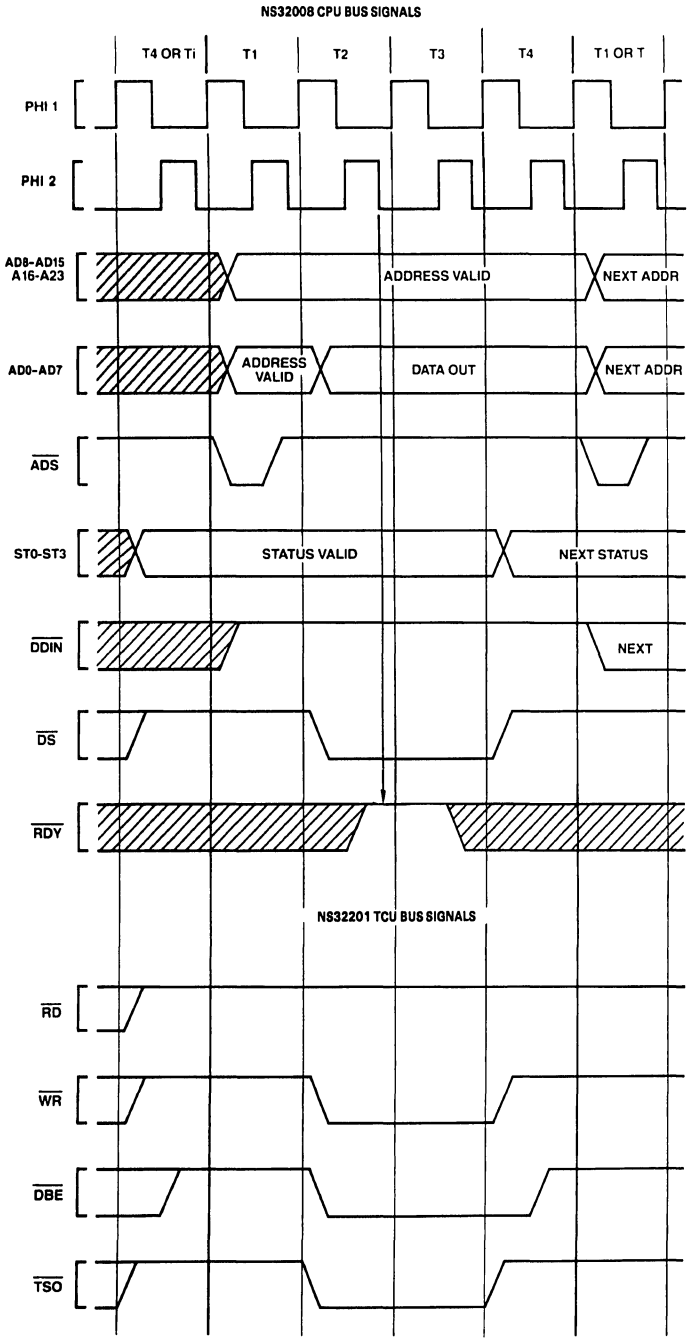

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FIGURE 3-8. Write Cycle Timing

3.0 Functional Description (Continued)

3.4.1 Cycle Extension

To allow sufficient strobe widths and access times for any speed of memory or peripheral device, the NS32008 provides for extension of a bus cycle. Any type of bus cycle except a Slave Processor cycle can be extended.

In *Figures 3-7* and *3-8*, note that during T3 all bus control signals from the CPU and TCU are flat. Therefore, a bus cycle can be cleanly extended by causing the T3 state to be repeated. This is the purpose of the RDY (Ready) pin.

At the end of T2 on the falling edge of PHI2, the RDY line is sampled by the CPU. If RDY is high, the next T-states will be T3 and T4, ending the bus cycle. If RDY is low, then another T3 state will be inserted after the next T-state and the RDY line will again be sampled on the falling edge of PHI2. Each additional T3 state after the first is referred to as a "WAIT STATE". See *Figure 3-9*.

The RDY pin is driven by the NS32201 Timing Control Unit, which applies WAIT States to the CPU as requested on three sets of pins:

1. $\overline{\text{CWAIT}}$ (Continuous WAIT), which holds the CPU in WAIT States until removed.
2. $\overline{\text{WAIT1}}$, $\overline{\text{WAIT2}}$, $\overline{\text{WAIT4}}$, $\overline{\text{WAIT8}}$ (collectively, $\overline{\text{WAITn}}$), which may be given a 4-bit binary value requesting a specific number of WAIT States from 0 to 15.
3. $\overline{\text{PER}}$ (Peripheral), which inserts five additional WAIT states and causes the TCU to reshape the $\overline{\text{RD}}$ and $\overline{\text{WR}}$ strobes. This provides the setup and hold times required by most MOS peripheral interface devices.

Combinations of these various WAIT requests are both legal and useful. For details of their use, see the NS32201 Data Sheet.

Figure 3-10 illustrates a typical Read cycle, with two WAIT states requested through the TCU $\overline{\text{WAITn}}$ pins.

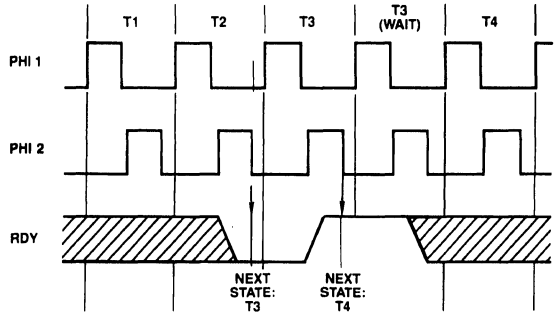

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FIGURE 3-9. RDY Pin Timing

3.4.2 Bus Status

The NS32008 CPU presents four bits of Bus Status information on pins ST0–ST3. The various combinations on these pins indicate why the CPU is performing a bus cycle, or, if it is idle on the bus, why it is idle.

Referring to *Figures 3-7* and *3-8*, note that Bus Status leads the corresponding Bus Cycle, going valid one clock cycle before T1, and changing to the next state at T4. This allows the system designer to fully decode the bus status and, if desired, latch the decoded signals before $\overline{\text{ADS}}$ initiates the Bus Cycle.

The Bus Status pins are interpreted as a 4-bit value, with ST0 the least significant bit. Their values decode as follows:

0000 The bus is idle because the CPU does not need to perform a bus access.

0001 The bus is idle because the CPU is executing the WAIT instruction.

0010 (Reserved for future use.)

0011 The bus is idle because the CPU is waiting for a Slave Processor to complete an instruction.

0100 Interrupt Acknowledge, Master.

The CPU is performing a Read cycle. To acknowledge receipt of a Non-Maskable Interrupt (on $\overline{\text{NMI}}$), it will read from address FFFF00_{16}, but will ignore any data provided. To acknowledge receipt of a Maskable Interrupt (on $\overline{\text{INT}}$), it will read from address FFFE00_{16}, expecting a vector number to be provided from the Master NS32202 Interrupt Control Unit. If the vectoring mode selected by the last SETCFG instruction was Non-Vectored, then the CPU will ignore the value it has read and will use a default vector instead, having assumed that no NS32202 is present. See Section 3.4.5.

0101 Interrupt Acknowledge, Cascaded.

The CPU is reading a vector number from a Cascaded NS32202 Interrupt Control Unit. The address provided is the address of the NS32202 Hardware Vector register. See Section 3.4.5.

0110 End of Interrupt, Master.

The CPU is performing a Read cycle to indicate that it is executing a Return from Interrupt (RETI) instruction. See Section 3.4.5.

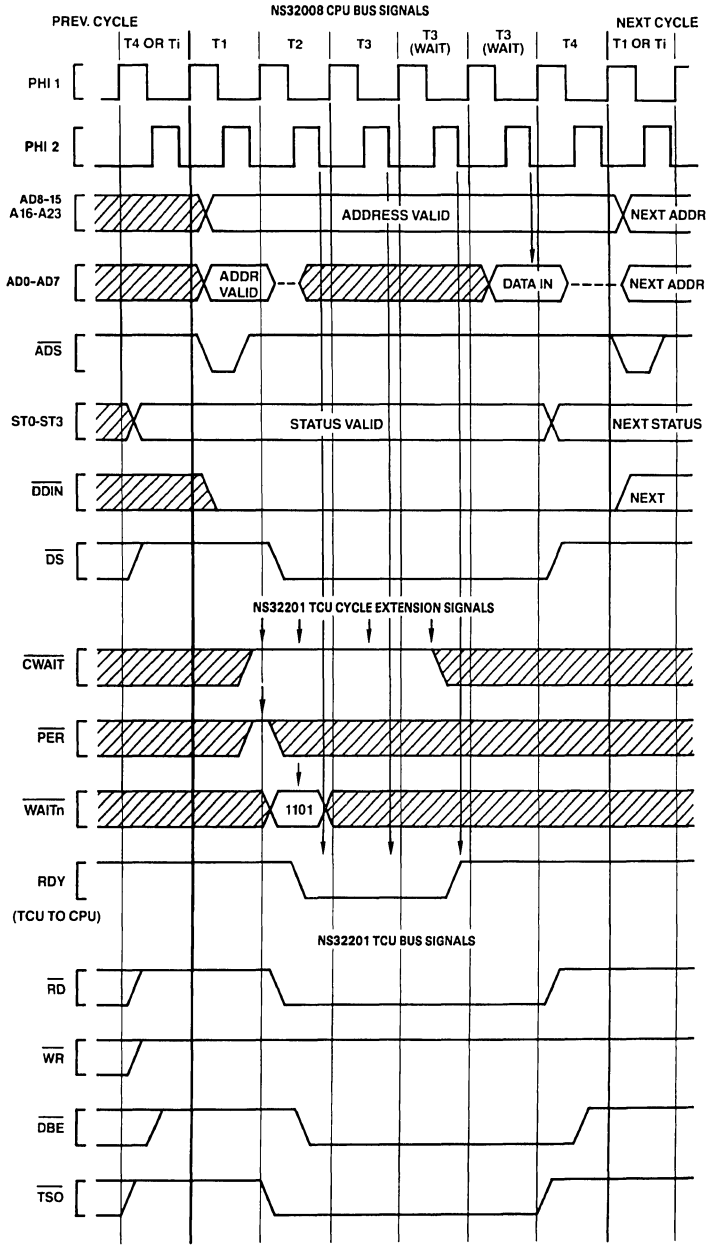
0111 End of Interrupt, Cascaded.

The CPU is reading from a Cascaded Interrupt Control Unit to indicate that it is returning (through RETI) from an interrupt service routine requested by that unit. See Section 3.4.5.

1000 Sequential Instruction Fetch.

The CPU is reading the next sequential word from the instruction stream into the Instruction Queue. It will do so whenever the bus would otherwise be idle and the queue is not already full.

3.0 Functional Description (Continued)



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Note: Arrows on $\overline{\text{CWAIT}}$, $\overline{\text{PER}}$, $\overline{\text{WAITn}}$ indicate points at which the TCU samples.
Arrows on AD0–AD7 and RDY indicate points at which the CPU samples.

FIGURE 3-10. Extended Cycle Example

3.0 Functional Description (Continued)

1001 Non-Sequential Instruction Fetch.

The CPU is performing the first fetch of instruction code after the Instruction Queue is purged. This will occur as a result of any jump or branch, or any interrupt or trap, or execution of certain instructions.

1010 Data Transfer.

The CPU is reading or writing an operand of an instruction.

1011 Read RMW Operand.

The CPU is reading an operand which will subsequently be modified and rewritten.

1100 Read for Effective Address Calculation.

The CPU is reading information from memory in order to determine the Effective Address of an operand. This will occur whenever an instruction uses the Memory Relative or External addressing mode.

1101 Transfer Slave Processor Operand.

The CPU is either transferring an instruction operand to or from a Slave Processor, or it is issuing the Operation Word of a Slave Processor instruction. See Section 3.8.1.

1110 Read Slave Processor Status.

The CPU is reading a status word from a Slave Processor. This occurs after the Slave Processor has signaled completion of an instruction. The transferred word tells the CPU whether a trap should be taken, and in some instructions, it presents new values for the CPU Processor Status Register bits N, Z, L or F. See Section 3.8.1.

1111 Broadcast Slave ID.

The CPU is initiating the execution of a Slave Processor instruction. The ID Byte (first byte of the instruction) is sent to all Slave Processors, one of which will recognize it. From this point, the CPU is communicating with only one Slave Processor. See Section 3.8.1.

3.4.3 Data Access Sequences

The NS32008 accesses all memory and peripheral devices in sequences of single-byte transfers. Transfer of values larger than bytes is performed from least-significant byte (lowest address) to most-significant byte.

3.4.3.1 Bit Accesses

The bit instructions access the byte containing the designated bit. The Test and Set Bit instruction (SBIT), for example, reads a byte, alters it, and rewrites it, having changed the contents of one bit.

3.4.3.2 Bit Field Accesses

An access to a Bit Field in memory always generates a Double Word transfer starting at the address containing the least-significant bit of the field. The Double Word is read by an Exact instruction; an Insert instruction reads a Double Word, modifies it, and rewrites it.

3.4.3.3 Extending Multiply Accesses

The extending multiply instruction (MEI) will return a result which is twice the size in bytes of the operand that it reads. If the multiplicand is in memory, the most-significant half of the result is written first (at the higher address), then the least-significant half.

3.4.4 Instruction Fetches

Instructions for the NS32008 CPU are "prefetched"; that is, they are input before being needed into the next available entry of the 4-byte Instruction Queue. The CPU performs two types of Instruction Fetch cycles: Sequential and Non-Sequential. These can be distinguished from each other by their differing status combinations on pins ST0–ST3 (Section 3.4.2).

A Sequential Fetch will be performed by the CPU whenever the Data Bus would otherwise be idle and the Instruction Queue is not currently full.

A Non-Sequential Fetch occurs as a result of any break in the normally sequential flow of a program. Any jump or branch instruction, a trap or an interrupt will cause the next Instruction Fetch cycle to be Non-Sequential. In addition, certain instructions flush the Instruction Queue, causing the next instruction fetch to display Non-Sequential status. Only the first bus cycle after a break displays Non-Sequential status.

3.4.5 Interrupt Control Cycles

Activating the $\overline{\text{INT}}$ or $\overline{\text{NMI}}$ pin on the CPU will initiate one or more bus cycles whose purpose is interrupt control rather than the transfer of instructions or data. Execution of the Return from Interrupt instruction (RETI) will also cause Interrupt Control bus cycles. These differ from instruction or data transfers only in the status presented on pins ST0–ST3. All Interrupt Control cycles are Read cycles. Table 3-1 summarizes NS32008 interrupt sequences.

This section describes only the Interrupt Control sequences associated with each interrupt and with the return from its service routine. For full details of the NS32008 interrupt structure, see Section 3.7.

3.0 Functional Description (Continued)

TABLE 3-1
Interrupt Sequences

Cycle	Status	Address	$\overline{DDIN}$	Bus
A. Nonmaskable Interrupt Control Sequences.				
Interrupt Acknowledge				
1	0100	$FFFF00_{16}$	0	Don't Care
Interrupt Return				
None: Performed through Return from Trap (RETT) instruction.				
B. Nonvectored Interrupt Control Sequences.				
Interrupt Acknowledge				
1	0100	$FFFE00_{16}$	0	Don't Care
Interrupt Return				
None. Performed through return from Trap (RETT) instruction.				
C. Vectored Interrupt Sequences: Noncascaded.				
Interrupt Acknowledge				
1	0100	$FFFE00_{16}$	0	Vector: Range 0–127
Interrupt Return				
1	0110	$FFFE00_{16}$	0	Vector: Same as in Previous Interrupt Acknowledge Cycle
D. Vectored Interrupt Sequences: Cascaded.				
Interrupt Acknowledge				
1	0100	$FFFE00_{16}$	0	Cascade Index: Range −16 to −1
(The CPU here uses the Cascade Index to find the Cascade Address.)				
2	0101	Cascade Address	0	Vector: Range 0–255
Interrupt Return				
1	0110	$FFFE00_{16}$	0	Cascade Index: Same as in Previous Interrupt Acknowledge Cycle
(The CPU here uses the Cascade Index to find the Cascade Address.)				
2	0111	Cascade Address	0	Don't Care

3.0 Functional Description (Continued)

3.4.6 Slave Processor Communication

The $\overline{SPC}$ pin is used as the data strobe for Slave Processor transfers. In a Slave Processor bus cycle, data is transferred 16 bits at a time on the Data Bus (AD0–AD15) and the status lines ST0–ST3 are monitored by each Slave Processor in order to determine the type of transfer being performed. *Figure 3-11* shows typical Slave Processor connections. $\overline{SPC}$ is bidirectional, but is driven by the CPU during all Slave Processor bus cycles. See Section 3.8 for full protocol sequences.

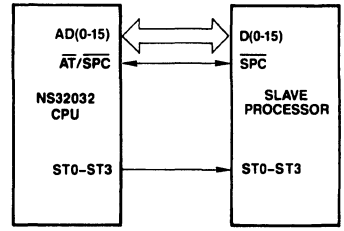

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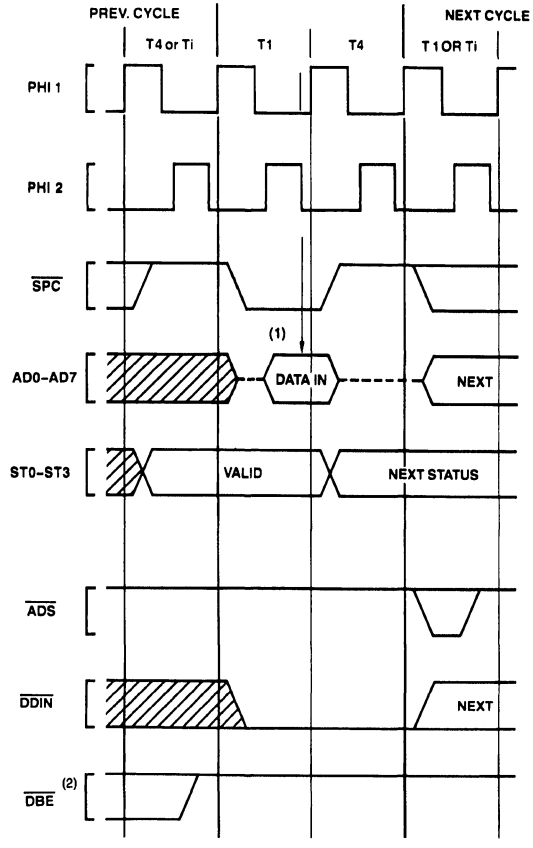
FIGURE 3-11. Slave Processor Connections



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Note 1. CPU samples Data Bus here.

Note 2. $\overline{DBE}$ and all other NS32201 TCU bus signals remain inactive because no $\overline{ADS}$ pulse is received from the CPU.

FIGURE 3-12. CPU Read from Slave Processor

3.0 Functional Description (Continued)

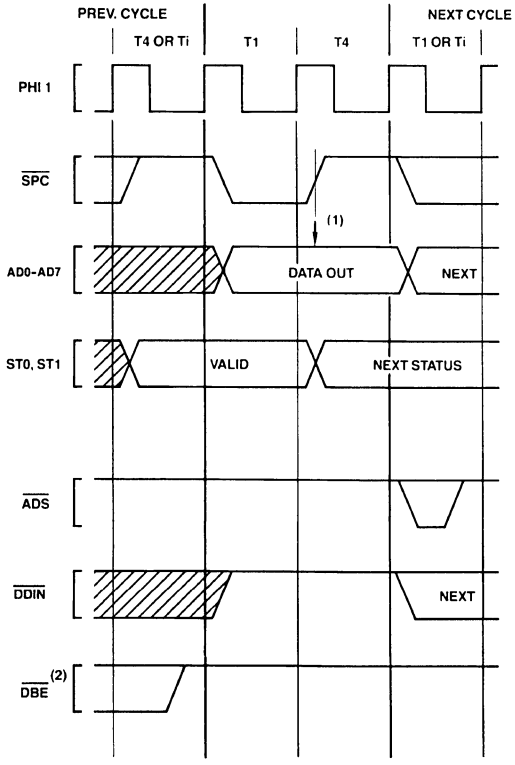
3.4.6.1 Slave Processor Bus Cycles

A Slave Processor bus cycle always takes exactly two clock cycles, labeled T1 and T4 (see *Figures 3-12* and *3-13*). During a Read cycle $\overline{SPC}$ is active from the beginning of T1 to the beginning of T4, and the data is sampled at the end of T1. The Cycle Status pins lead the cycle by one clock period, and are sampled at the leading edge of $\overline{SPC}$. During a Write cycle, the CPU applies data and activates $\overline{SPC}$ at T1, removing $\overline{SPC}$ at T4. The Slave Processor latches status on the leading edge of $\overline{SPC}$ and latches data on the trailing edge.

Since the CPU does not pulse the Address Strobe ($\overline{ADS}$), no bus signals are generated by the NS32201 Timing Control Unit. The direction of a transfer is determined by the sequence ("protocol") established by the instruction under execution; but the CPU indicates the direction on the $\overline{DDIN}$ pin for hardware debugging purposes.

3.4.6.2 Slave Operand Transfer Sequences

A Slave Processor operand is transferred in one or more Slave bus cycles. A Byte operand is transferred on the least-significant byte of the Data Bus (AD0–AD7), and a Word operand is transferred on the entire 16-bit bus (AD0–AD15). A Double Word is transferred in a consecutive pair of bus cycles, least-significant word first. A Quad Word is transferred in two pairs of Slave cycles, with other bus cycles possibly occurring between them. The word order is from least-significant to most-significant word.



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Note 1. Slave Processor samples Data Bus here.

Note 2. $\overline{DBE}$, being provided by the NS32201 TCU, remains inactive due to the fact that no pulse is presented on ADS, TCU signals $\overline{RD}$, $\overline{WR}$ and $\overline{TSO}$ also remain inactive.

FIGURE 3-13. CPU Write to Slave Processor

3.0 Functional Description (Continued)

3.5 BUS ACCESS CONTROL

The NS32008 CPU has the capability of relinquishing its access to the bus request from a DMA device or another CPU. This capability is implemented on the $\overline{\text{HOLD}}$ (Hold Request) and $\overline{\text{HLDA}}$ (Hold Acknowledge) pins. By asserting $\overline{\text{HOLD}}$ low, an external device requests access to the bus. On receipt of $\overline{\text{HLDA}}$ from the CPU, the device may perform bus cycles, as the CPU at this point has set the AD0–AD15, A16–A23, $\overline{\text{ADS}}$ and $\overline{\text{DDIN}}$ pins to the TRI-STATE® condition. To return control of the bus to the CPU, the device sets $\overline{\text{HOLD}}$ inactive, and the CPU acknowledges return of the bus by setting $\overline{\text{HLDA}}$ inactive.

How quickly the CPU releases the bus depends on whether it is idle on the bus at the time the $\overline{\text{HOLD}}$ request is made, as the CPU must always complete the current bus cycle. *Figure 3-14* shows the timing sequence when the CPU is idle. In this case, the CPU grants the bus during the immediately following clock cycle. *Figure 3-15* shows the sequence if the CPU is using the bus at the time that the $\overline{\text{HOLD}}$ request is made. If the request is made during or before the clock cycle shown (two clock cycles before T4), the CPU will release the bus during the clock cycle following T4. If the request occurs closer to T4, the CPU may already have decided to initiate another bus cycle. In that case, it will not grant the bus until after the next T4 state. Note that this situation will also occur if the CPU is idle on the bus, but has initiated a bus cycle internally.

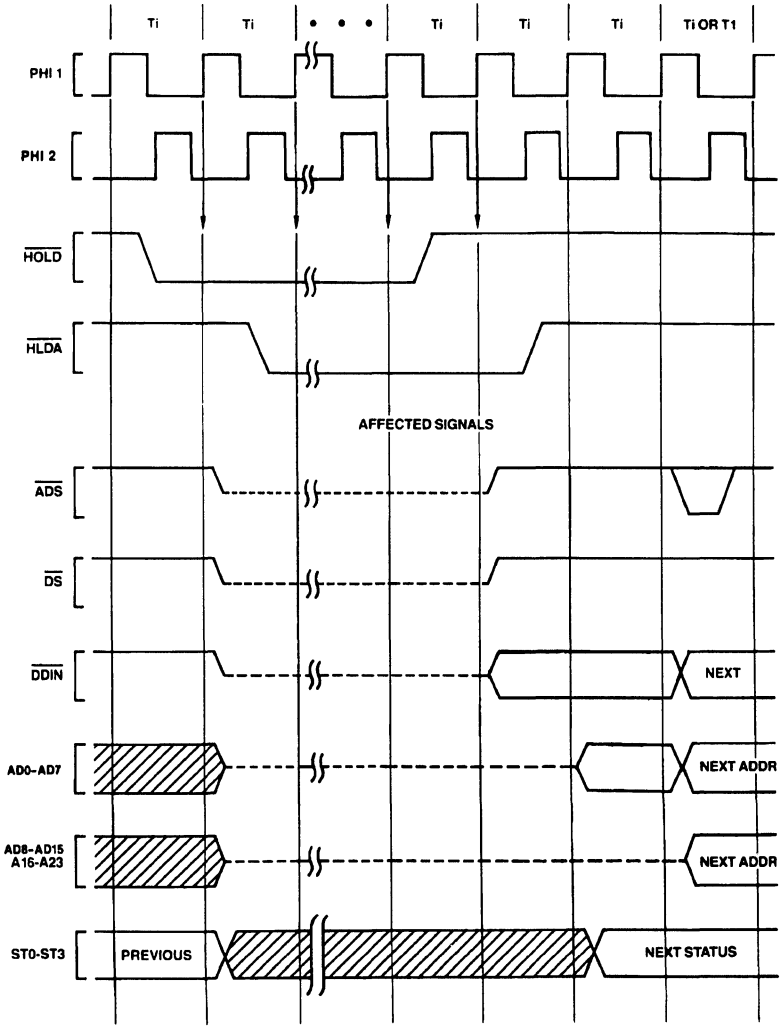

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FIGURE 3-14. $\overline{\text{HOLD}}$ Timing, Bus Initially Idle

3.0 Functional Description (Continued)

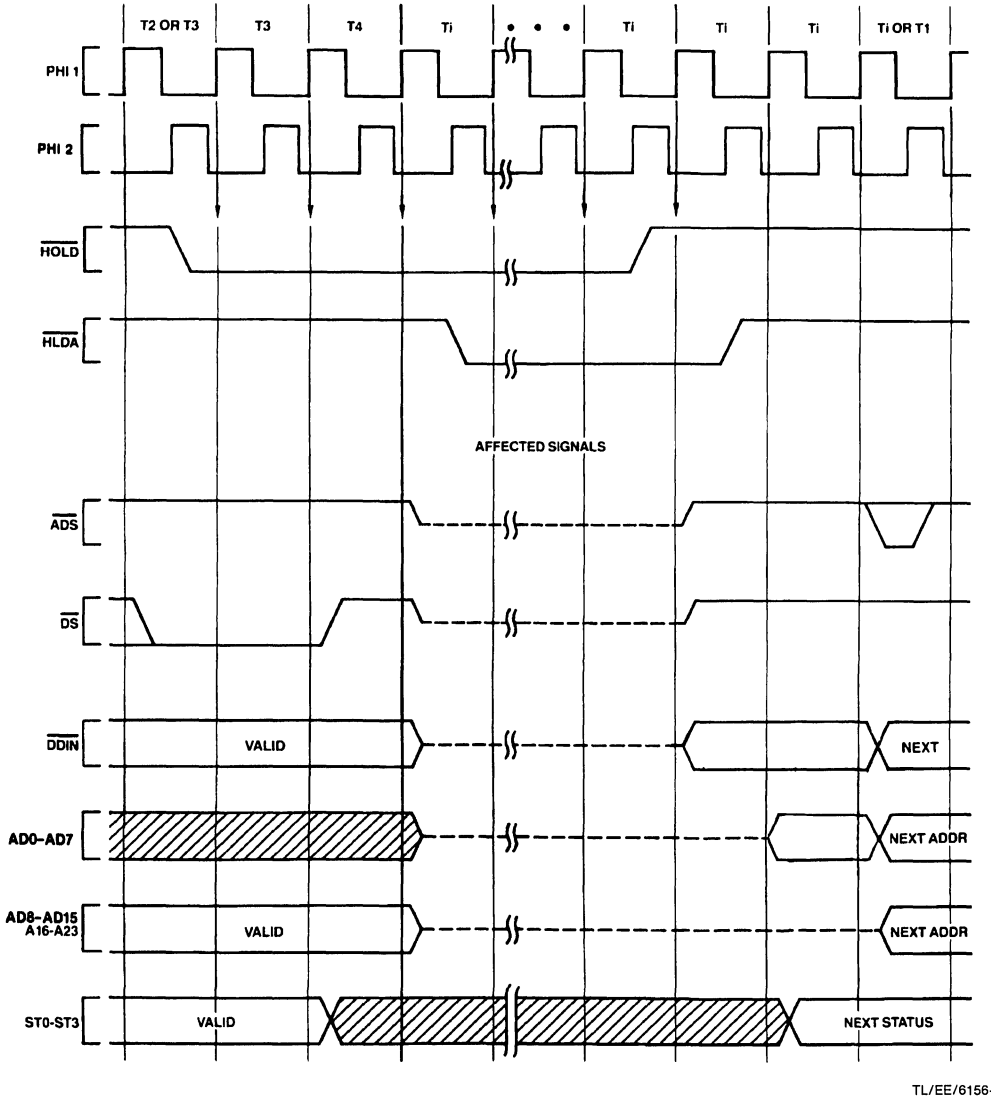

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FIGURE 3-15. $\overline{\text{HOLD}}$ Timing, Bus Initially Not Idle

3.0 Functional Description (Continued)

3.6 INSTRUCTION STATUS

In addition to the four bits of bus cycle status (ST0–ST3), the NS32008 CPU also presents Instruction Status information on three separate pins. These pins differ from ST0–ST3 in that they are synchronous to the CPU's internal instruction execution section rather than to its bus inerface section.

$\overline{PFS}$ (Program Flow Status) is pulsed low as each instruction begins execution. It is intended for debugging purposes.

U/$\overline{S}$ originates from the U bit of the Processor Status Register, and indicates whether the CPU is currently running in User or Supervisor mode. Although it is not synchronous to bus cycles, there are guarantees on its validity during any given bus cycle. See the Timing Specifications, *Figure 4-19*.

$\overline{ILO}$ (Interlocked Operation) is activated during an SBITI (Set Bit, Interlocked) or CBITI (Clear Bit, Interlocked) instruction. It is made available to external bus arbitration circuitry in order to allow these instructions to implement the semaphore primitive operations for multiprocessor communication and resource sharing. As with the U/$\overline{S}$ pin, there are guarantees on its validity during the operand accesses performed by the instructions. See the Timing Specification section, *Figures 4-16* and *4-17*.

3.7 NS32008 INTERRUPT STRUCTURE

The NS32008 CPU has two interrupt pins: INT, on which maskable interrupts may be requested, and NMI, on which nonmaskable interrupts may be requested.

In addition, there is a set of internally-generated "traps" which cause interrupt service to be performed as a result either of exceptional conditions (e.g., attempted division by zero) or of specific instructions whose purpose is to cause a trap to occur (e.g., the Supervisor Call instruction).

3.7.1 General Interrupt/Trap Sequence

Upon receipt of an interrupt or trap request, the CPU goes through three major steps:

1. Adjustment of Registers.

   Depending on the source of the interrupt or trap, the CPU may restore and/or adjust the contents of the Program Counter (PC), the Processor Status Register (PSR) and the currently-selected Stack Pointer (SP). A copy of the PSR is made, and the PSR is then set to reflect Supervisor Mode and selection of the Interrupt Stack.

2. Vector Acquisition.

   A Vector is either obtained from the Data Bus or is supplied by default.

3. Service Call.

   The Vector is used as an index into the Interrupt Dispatch Table, whose base address is taken from the CPU Interrupt Base (INTBASE) Register. See *Figure 3-16*. A 32-bit External Procedure Descriptor is read from the table entry, and an External Procedure Call is performed using it. The MOD Register (16 bits) and Program Counter (32 bits) are pushed on the Interrupt Stack.

This process is illustrated in *Figure 3-17*, from the viewpoint of the programmer.

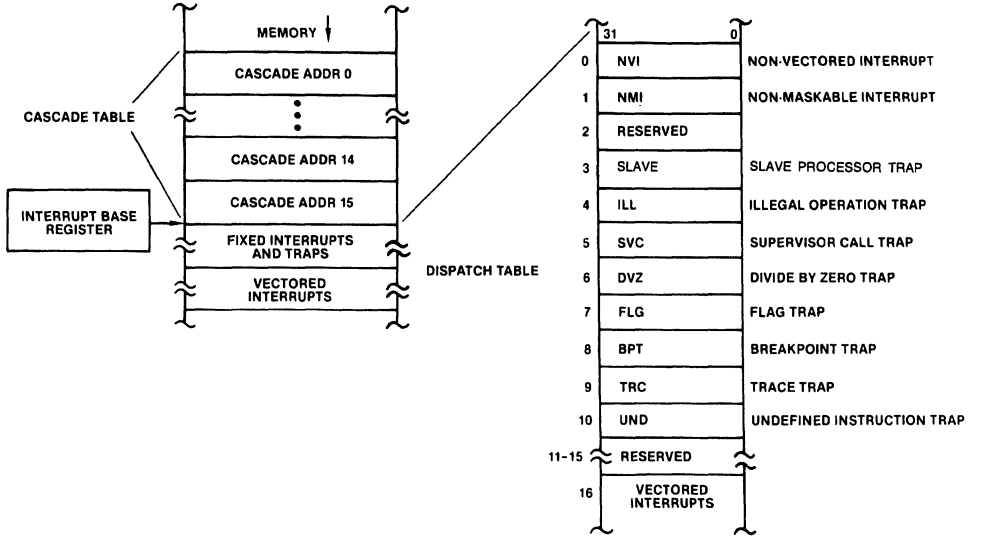

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FIGURE 3-16. Interrupt Dispatch and Cascade Tables

3.0 Functional Description (Continued)

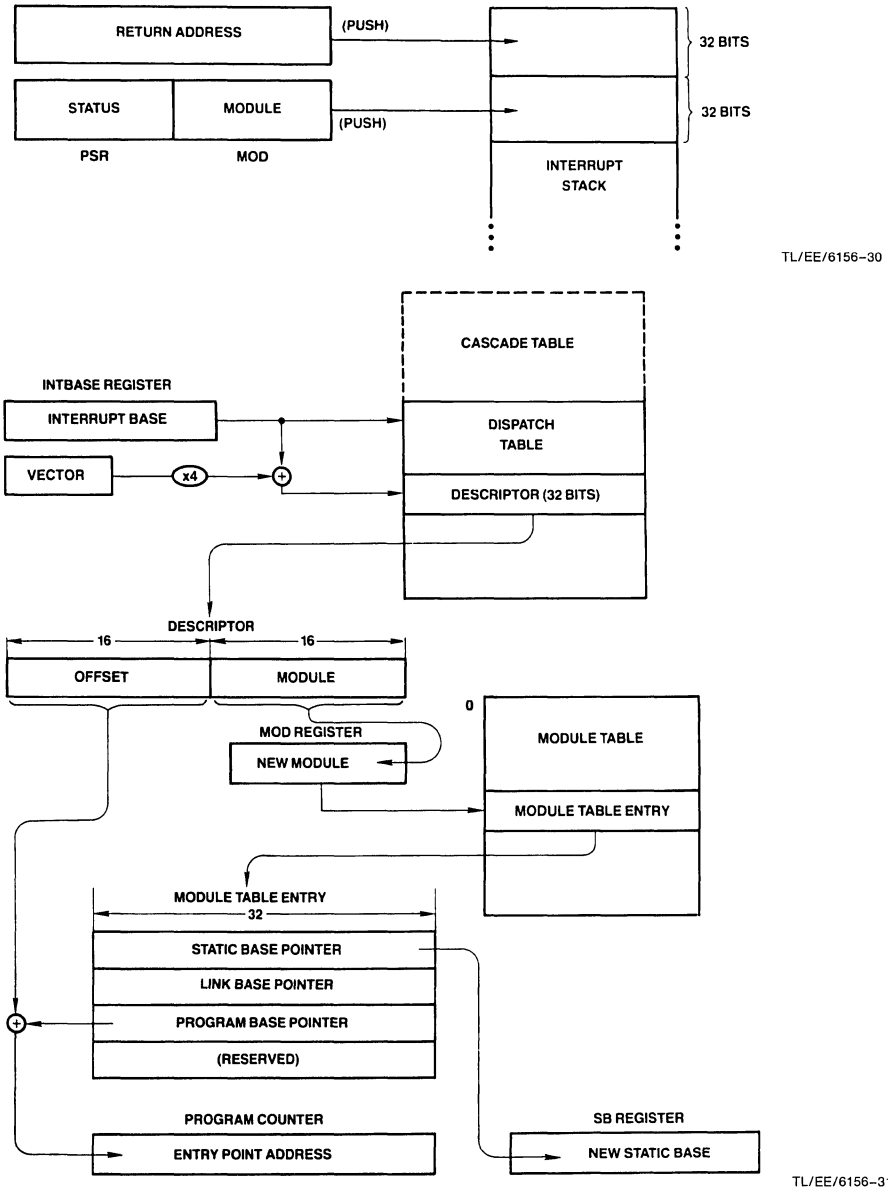

FIGURE 3-17. Interrupt/Trap Service Routine Calling Sequence

3.0 Functional Description (Continued)

3.7.2 Interrupt/Trap Return

To return control to an interrupted program, one of two instruction is used. The RETT (Return From Trap) instruction (*Figure 3-18*) restores the PSR, MOD, PC and SB registers to their previous contents and, since traps are often used deliberately as a call mechanism for Supervisor Mode procedures, it also discards a specified number of bytes from the original stack as surplus parameter space. RETT is used to return from any trap or interrupt except the Maskable Interrupt. For this, the RETI (Return from Interrupt) instruction is used, which also informs any external Interrupt Control Units that interrupt service has been completed. Since interrupts are generally asynchronous external events, RETI does not pop parameters. See *Figure 3-19*.

3.7.3 Maskable Interrupts (The $\overline{\text{INT}}$ Pin)

The $\overline{\text{INT}}$ pin is a level-sensitive input. A continuous low level is allowed for generating multiple interrupt requests. The input is maskable, and is therefore enabled to generate interrupt requests only while the Processor Status Register I bit is set. The I bit is automatically cleared during service of an $\overline{\text{INT}}$ or $\overline{\text{NMI}}$ request, and is restored to its original setting upon return from the interrupt service routine via the RETT or RETI instruction.

The $\overline{\text{INT}}$ pin may be configured via the SETCFG instruction as either Non-Vectored (CFG register bit I = 0) or Vectored (bit I = 1).

3.7.3.1 Non-Vectored Mode

In the Non-Vectored Mode, an interrupt request on the $\overline{\text{INT}}$ pin will cause an Interrupt Acknowledge bus cycle, but the CPU will ignore any value read from the bus and use instead a default vector of zero. This mode is useful for small systems in which hardware interrupt prioritization is unnecessary. The RETT instruction should be used to return from an interrupt in Non-Vectored Mode.

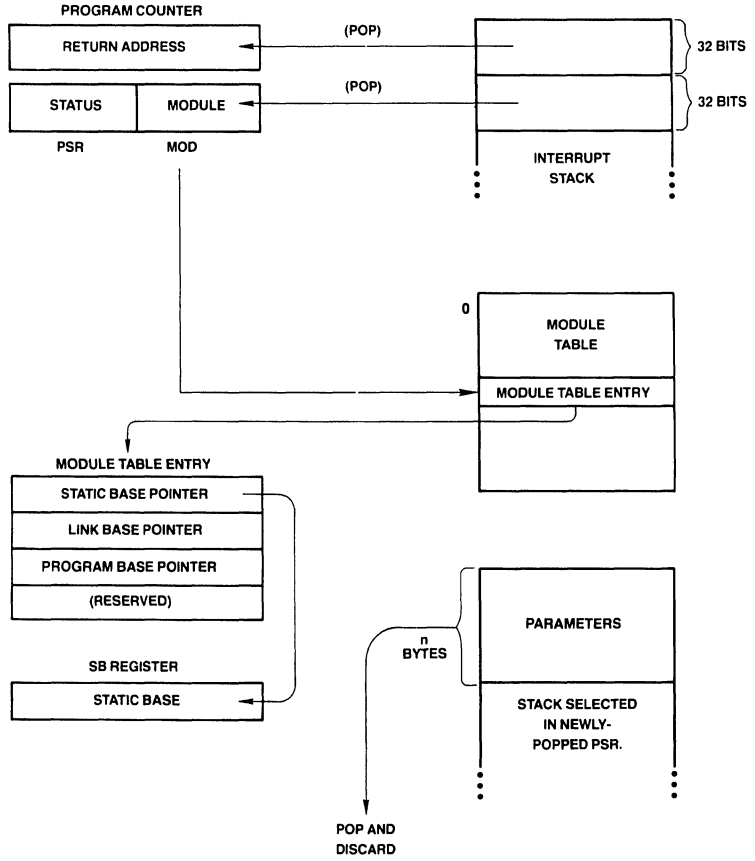

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FIGURE 3-18. Return from Trap (RETTn) Instruction Flow

3.0 Functional Description (Continued)

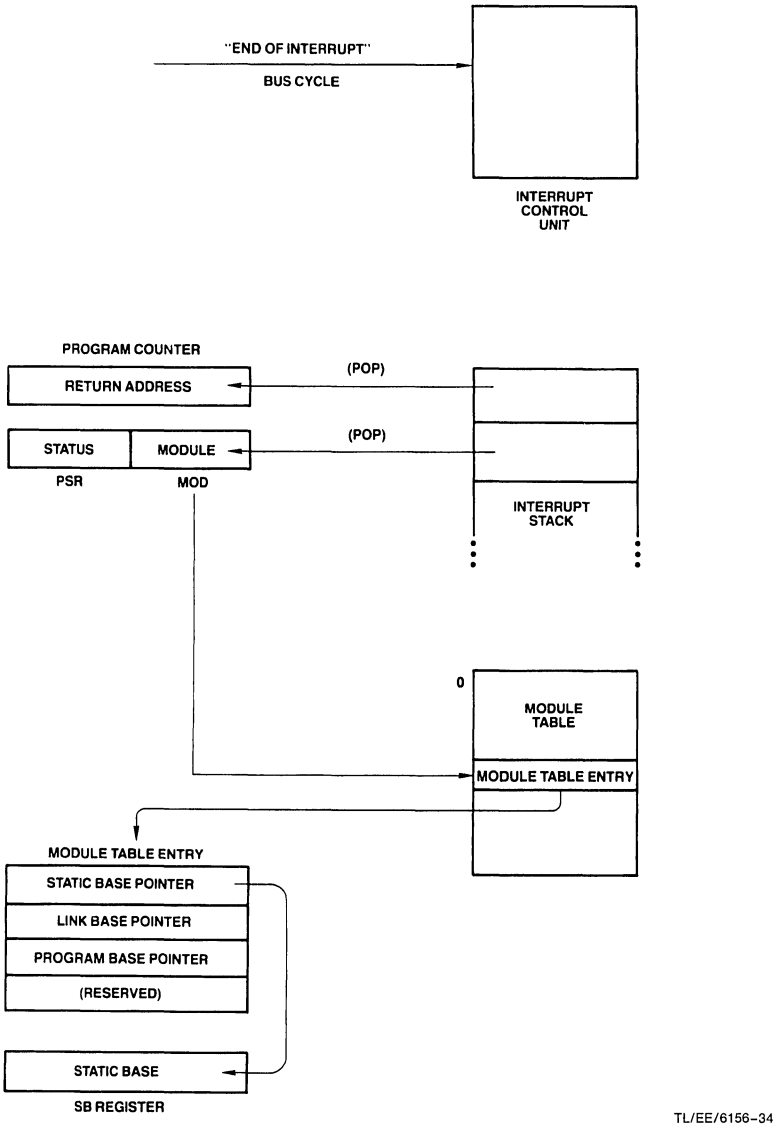

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FIGURE 3-19. Return from Interrupt (RETI) Instruction Flow

3.0 Functional Description (Continued)

3.7.3.2 Vectored Mode: Non-Cascaded Case

In the Vectored mode, the CPU uses an Interrupt Control Unit (ICU) to prioritize up to 16 interrupt requests. *Figure 3-20* shows the connections required for a single ICU. Upon receipt of an interrupt request on the $\overline{INT}$ pin, the CPU performs an "Interrupt Acknowledge, Master" bus cycle (Section 3.4.2) reading a vector value from the Data Bus. This vector is then used as an index into the Dispatch Table in order to find the External Procedure Descriptor for the proper interrupt service procedure. The service procedure eventually returns via the Return from Interrupt (RETI) instruction, which performs an End of Interrupt bus cycle, informing the ICU that it may reprioritize any interrupt requests still pending. The ICU provides the vector number again, which the CPU uses to determine whether it needs also to inform a Cascaded ICU (see below).

In a system with only one ICU (16 levels of interrupt), the vectors provided must be in the range of 0 through 127; that is, they must be positive numbers in eight bits. By providing a negative vector number, an ICU flags the interrupt source as being a Cascaded ICU (see below).

3.7.3.3 Vectored Mode: Cascaded Case

In order to allow up to 256 levels of interrupt, provision is made both in the CPU and in the NS32202 Interrupt Control Unit (ICU) to transparently support cascading. *Figure 3-21* shows a typical cascaded configuration. Note that the Interrupt output from a Cascaded ICU goes to an Interrupt Request input of the Master ICU, which is the only ICU which drives the CPU $\overline{INT}$ pin.

In a system which uses cascading, two tasks must be performed upon initialization:

1. For each Cascaded ICU in the system, the Master ICU must be informed of the line number (0 to 15) on which it receives the cascaded requests.
2. A Cascade Table must be established in memory. The Cascade Table is located in a *negative* direction from the location indicated by the CPU Interrupt Base (INTBASE) register. Its entries are 32-bit addresses, pointing to the Vector Registers of each of up to 16 Cascaded ICUs.

Figure 3-16 illustrates the position of the Cascade Table. To find the Cascade Table entry for a Cascaded ICU, take its Master ICU line number (0 to 15) and subtract 16 from it, giving an index in the range −16 to −1. Multiply this value by 4, and add the resulting negative number to the contents of the INTBASE Register. The 32-bit entry at this address must be set to the address of the Hardware Vector Register of the Cascaded ICU. This is referred to as the "Cascade Address."

Upon receipt of an interrupt request from a Cascaded ICU, the Master ICU interrupts the CPU and provides the negative Cascade Table index instead of a (positive) vector number. The CPU, seeing the negative value, uses it as an index into the Cascade Table and reads the Cascade Address from the referenced entry. Applying this address, the CPU performs an "Interrupt Acknowledge, Cascaded" bus cycle (Section 3.4.2), reading the final vector value. This vector is interpreted by the CPU as an unsigned byte, and can therefore be in the range of 0 through 255.

In returning from a Cascaded interrupt, the service procedure executes the Return from Interrupt (RETI) instruction, as it would for any Maskable Interrupt. The CPU performs an "End of Interrupt, Master" bus cycle (Section 3.4.2), whereupon the Master ICU again provides the negative Cascade Table index. The CPU, seeing a negative value, uses it to find the corresponding Cascade Address from the Cascade Table. Applying this address, it performs an "End of Interrupt, Cascaded" bus cycle (Section 3.4.2), informing the cascaded ICU of the completion of the service routine. The byte read from the Cascaded ICU is discarded.

Note: If an interrupt must be masked off, the CPU can do so by setting the corresponding bit in the interrupt mask register of the interrupt controller. However, if an interrupt is set pending during the CPU instruction that masks off that interrupt, the CPU may still perform an interrupt acknowledge cycle following that instruction since it might have sampled the $\overline{INT}$ line before the ICU deasserted it. This could cause the ICU to provide an invalid vector. To avoid this problem the above operation should be performed with the CPU interrupt disabled.

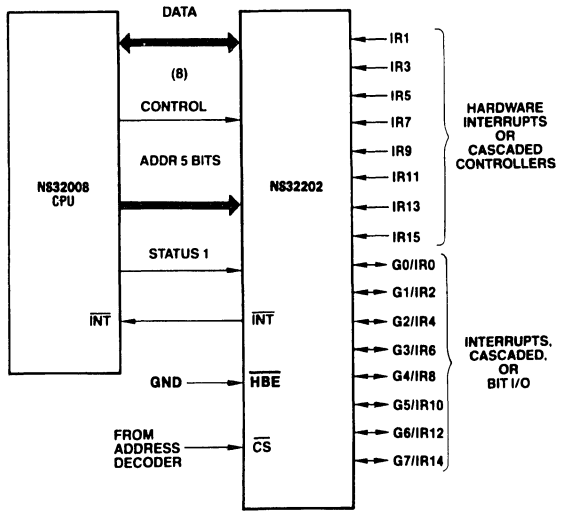

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FIGURE 3-20. Interrupt Control Unit Connections (16 Levels)

3.0 Functional Description (Continued)

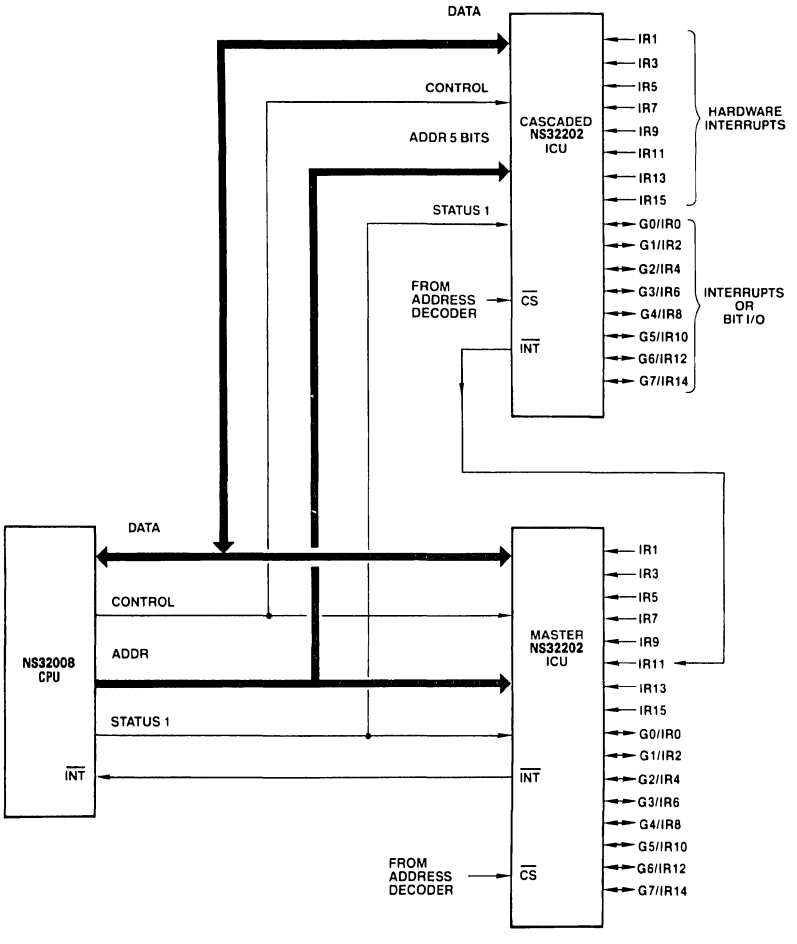

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FIGURE 3-21. Cascaded Interrupt Control Unit Connections

3.7.4 Non-Maskable Interrupt (The $\overline{\text{NMI}}$ Pin)

The Non-Maskable interrupt is triggered whenever a falling edge is detected on the $\overline{\text{NMI}}$ pin. The CPU performs an "Interrupt Acknowledge, Master" bus cycle (Section 3.4.2) when processing of this interrupt actually begins. The Interrupt Acknowledge cycle differs from that provided for Maskable Interrupts in that the address presented is $FFFF00_{16}$. The vector value used for the Non-Maskable Interrupt is taken as 1, regardless of the value read from the bus.

The service procedure returns from the Non-Maskable Interrupt using the Return from Trap (RETT) instruction. No special bus cycles occur on return.

For the full sequence of events in processing the Non-Maskable Interrupt, see Section 3.7.7.1.

3.7.5 Traps

A trap is an internally-generated interrupt request caused as a direct and immediate result of the execution of an instruction. The Return Address pushed by any trap except TRC is the address of the first byte of the instruction during which the trap occurred. Traps do not disable interrupts, as they are not associated with external events. Traps recognized by the NS32008 are:

Trap (Slave): An exceptional condition was detected by the Floating-Point unit or another Slave Processor during the execution of a Slave Instruction. This trap is requested via the Status Word returned as part of the Slave Processor Protocol (Section 3.8.1).

Trap (ILL): Illegal operation. A privileged operation was attempted while the CPU was in User Mode (PSR bit U = 1).

Trap (SVC): The Supervisor Call (SVC) instruction was executed.

Trap (DVZ): An attempt was made to divide an integer by zero. (The Slave Trap is used for Floating-Point division by zero.)

3.0 Functional Description (Continued)

Trap (FLG): The FLAG instruction detected a "1" in the CPU PSR F bit.

Trap (BPT): The Breakpoint (BPT) instruction was executed.

Trap (TRC): The instruction just completed is being traced. See below.

Trap (UND): An undefined opcode was encountered by the CPU.

A special case is the Trace Trap (TRC), which is enabled by setting the T bit in the Processor Status Register (PSR). At the beginning of each instruction, the T bit is copied into the PSR P (Trace "Pending") bit. If the P bit is set at the end of an instruction, then the Trace Trap is activated. If any other trap or interrupt request is made during a traced instruction, its entire service procedure is allowed to complete before the Trace Trap occurs. Each interrupt and trap sequence handles the P bit for proper tracing, guaranteeing one and only one Trace Trap per instruction, and guaranteeing that the Return Address pushed during a Trace Trap is always the address of the next instruction to be traced.

3.7.6 Prioritization

The NS32008 CPU internally prioritizes simultaneous interrupt and trap requests as follows:

1. Traps other than Trace (Highest priority)
2. Non-Maskable Interrupt
3. Maskable Interrupts
4. Trace Trap (Lowest priority)

3.7.7 Interrupt/Trap Sequences: Detailed Flow

For purposes of the following detailed discussion of interrupt and trap service sequences, a single sequence called "Service" is defined in *Figure 3-22*. Upon detecting any interrupt request or trap condition, the CPU first performs a sequence dependent upon the type of interrupt or trap. This sequence will include pushing the Processor Status Register and establishing a Vector and a Return Address. The CPU then performs the Service sequence.

For the sequence followed in processing either Maskable or Non-Maskable interrupts (on the $\overline{INT}$ or $\overline{NMI}$ pins, respectively), see Section 3.7.7.1. For the Trace Trap, see Section 3.7.7.3, and for all other traps, see Section 3.7.7.2.

3.7.7.1 Maskable/Non-Maskable Interrupt Sequence

This sequence is performed by the CPU when the $\overline{NMI}$ pin receives a falling edge, or the $\overline{INT}$ pin becomes active with the PSR I bit set. The interrupt sequence begins either at the next instruction boundary or, in the case of the String instructions, at the next interruptable point during its execution.

1. If a String instruction was interrupted and not yet completed:
   a. Clear the Processor Status Register P bit.
   b. Set "Return Address" to the address of the first byte of the interrupted instruction.

   Otherwise, set "Return Address" to the address of the next instruction.
2. Copy the Processor Status Register (PSR) into a temporary register, then clear PSR bits S, U, T, P and I.
3. If the interrupt is Non-Maskable:
   a. Read a byte from address $FFFF00_{16}$, applying Status Code 0100 (Interrupt Acknowledge, Master: Section 3.4.2). Discard the byte read.
   b. Set "Vector" to 1.
   c. Go to Step 8.
4. If the interrupt is Non-Vectored:
   a. Read a byte from address $FFFE00_{16}$, applying Status Code 0100 (Interrupt Acknowledge, Master: Section 3.4.2). Discard the byte read.
   b. Set "Vector" to 0.
   c. Go to Step 8.
5. Here the interrupt is Vectored. Read "Byte" from address $FFFE00_{16}$, applying Status Code 0100 (Interrupt Acknowledge, Master, Section 3.4.2).
6. If "Byte" ≥ 0, then set "Vector" to "Byte" and go to Step 8.
7. If "Byte" is in the range -16 through -1, then the interrupt source is Cascaded. (More negative values are reserved for future use.) Perform the following:
   a. Read the 32-bit Cascade Address from memory. The address is calculated as INTBASE $+4*$ Byte.
   b. Read "Vector," applying the Cascade Address just read and Status Code 0101 (Interrupt Acknowledge, Cascaded, Section 3.4.2).
8. Push the PSR copy (from Step 2) onto the Interrupt Stack as a 16-bit value.
9. Perform Service (Vector, Return Address), *Figure 3-22*.

Service (Vector, Return Address):

1) Read the 32-bit External Procedure Descriptor from the Interrupt Dispatch Table: address is Vector*4 + INTBASE Register contents.
2) Move the Module field of the Descriptor into the MOD Register.
3) Read the new Static Base pointer from the memory address contained in MOD, placing it into the SB Register.
4) Read the Program Base pointer from memory address MOD + 8, and add to it the Offset field from the Descriptor, placing the result in the Program Counter.
5) Flush queue: Non-sequentially fetch first instruction of Interrupt routine.
6) Push MOD Register onto the Interrupt Stack as a 16-bit value. (The PSR has already been pushed as a 16-bit value.)
7) Push the Return Address onto the Interrupt Stack as a 32-bit quantity.

FIGURE 3-22. Service Sequence
Invoked during all interrupt/trap sequences.

3.0 Functional Description (Continued)

3.7.7.2 Trap Sequence: Traps Other Than Trace

1. Restore the currently selected Stack Pointer and the Processor Status Register to their original values at the start of the trapped instruction.
2. Set "Vector" to the value corresponding to the trap type.
   SLAVE: Vector = 3
   ILL: Vector = 4
   SVC: Vector = 5
   DVZ: Vector = 6
   FLG: Vector = 7
   BPT: Vector = 8
   UND: Vector = 10
3. Copy the Processor Status Register (PSR) into a temporary register, then clear PSR bits S, U, T and P.
4. Push the PSR copy onto the Interrupt Stack as a 16-bit value.
5. Set "Return Address" to the address of the first byte of the trapped instruction.
6. Perform Service (Vector, Return Address), *Figure 3-22.*

3.7.7.3 Trace Trap Sequence

1. In the Processor Status Register (PSR), clear the P bit.
2. Copy the PSR into a temporary register, then clear PSR bits S, U and T.
3. Push the PSR copy onto the Interrupt Stack as a 16-bit value.
4. Set "Vector" to 9.
5. Set "Return Address" to the address of the next instruction.
6. Perform Service (Vector, Return Address), *Figure 3-22.*

3.8 SLAVE PROCESSOR INSTRUCTIONS

The NS32008 CPU recognizes two groups of instructions as being executable by external Slave Processors:

Floating-Point Instruction Set

Custom Instruction Set

Each Slave Instruction Set is validated by a bit in the Configuration Register (Section 2.1.3). Any Slave Instruction which does not have its corresponding Configuration Register bit set will trap as undefined, without any Slave Processor communication attempted by the CPU. This allows software simulation of a nonexistent Slave Processor. Slave Processor cycles use pins AD0–AD15 as a 16-bit data bus.

Status Combinations:

Send ID (ID): Code 1111
Xfer Operand (OP): Code 1101
Read Status (ST): Code 1110

Step	Status	Action
1	ID	CPU Send ID Byte.
2	OP	CPU Sends Operation Word.
3	OP	CPU Sends Required Operands.
4	—	Slave Starts Execution. CPU Pre-Fetches.
5	—	Slave Pulses $\overline{SPC}$ Low.
6	ST	CPU Reads Status Word. (Trap? Alter Flags?)
7	OP	CPU Reads Results (If Any).

FIGURE 3-23. Slave Processor Protocol

3.8.1 Slave Processor Protocol

Slave Processor instructions have a 3-byte Basic Instruction field, consisting of an ID Byte followed by an Operation Word. The ID Byte has three functions:

1. It identifies the instruction as being a Slave Processor instruction.
2. It specifies which Slave Processor will execute it.
3. It determines the format of the following Operation Word of the instruction.

Upon receiving a Slave Processor instruction, the CPU initiates the sequence outlined in *Figure 3-23.* While applying Status Code 1111 (Broadcast ID, Section 3.4.2), the CPU transfers the ID Byte on the least-significant half of the data bus (AD0–AD7). All Slave Processors input this Byte and decode it. The Slave Processor selected by the ID Byte is activated, and from this point the CPU is communicating only with it. If any other slave protocol was in progress (e.g., an aborted Slave instruction), this tranfer cancels it.

The CPU next sends the Operation Word while applying Status Code 1101 (Transfer Slave Operand, Section 3.4.2). Upon receiving it, the Slave Processor decodes it, and at this point both the CPU and the Slave Processor are aware of the number of operands to be transferred and their sizes. The Operation Word is swapped on the Data Bus; that is, bits 0–7 appear on pins AD8–AD15 and bits 8–15 appear on pins AD0–AD7.

Using the Addressing Mode fields within the Operation Word, the CPU starts fetching operands and issuing them to the Slave Processor. To do so, it references any Addressing Mode extensions which may be appended to the Slave Processor instruction. Since the CPU is solely responsible for memory accesses, these extensions are not sent to the Slave Processor. The Status Code applied is 1101 (Transfer Slave Processor Operand, Section 3.4.2).

After the CPU has issued the last operand, the Slave Processor starts the actual execution of the instruction. Upon completion, it will signal the CPU by pulsing $\overline{SPC}$ low. To allow for this, $\overline{SPC}$ is normally held high only by an internal pull-up device of approximately 5 kΩ.

While the Slave Processor is executing the instruction, the CPU is free to prefetch instructions into its queue. If it fills the queue before the Slave Processor finishes, the CPU will wait, applying Status Code 0011 (Waiting for Slave, Section 3.4.2).

Upon receiving the pulse on SPC, the CPU uses SPC to read a Status Word from the Slave Processor, applying Status Code 1110 (Read Slave Status, Section 3.4.2). This word has the format shown in *Figure 3-24.* If the Q bit ("Quit," Bit 0) is set, this indicates that an error was detected by the Slave Processor. The CPU will not continue the protocol, but will immediately trap through the Slave vector

3.0 Functional Description (Continued)

in the Interrupt Table. Certain Slave Processor instructions cause CPU PSR bits to be loaded from the Status Word.

The last step in the protocol is for the CPU to read a result, if any, and transfer it to the destination. The Read cycles from the Slave Processor are performed by the CPU while applying Status Code 1101 (Transfer Slave Operand, Section 3.4.2).

An exception to the protocol above is a Custom Slave instruction (LCR: Load Custom Register). In executing this instruction, the protocol ends after the CPU has issued the last operand. The CPU does not wait for an acknowledgement from the Slave Processor, and it does not read status.

3.8.2 Floating-Point Instructions

Table 3-2 gives the protocols followed for each Floating-Point instruction. The instructions are referenced by their mnemonics. For the bit encoding of each instruction, see Appendix A.

The Operand class columns give the Access Class for each general operand, defining how the addressing modes are interpreted (see Instruction Set Reference Manual).

The Operand Issued columns show the sizes of the operands issued to the Floating-Point Unit by the CPU. "D" indicates a 32-bit Double Word. "i" indicates that the instruction specifies an integer size for the operand (B=byte, W=word, D=double word). "f" indicates that the instruction specifies a Floating-Point size for the operand (F=32-bit standard floating, L=64-bit Long Floating).

The Returned Value type and Destination column gives the size of any returned value and where the CPU places it. The PSR Bits Affected column indicates which PSR bits, if any, are updated from the Slave Processor Status Word (*Figure 3-24*).

Any operand indicated as being of type "f" will not cause a transfer if the Register addressing mode is specified. This is because the Floating-Point Registers are physically on the Floating-Point Unit and are therefore available without CPU assistance.

TABLE 3-2
Floating-Point Instruction Protocols

Mnemonic	Operand 1 Class	Operand 2 Class	Operand 1 Issued	Operand 2 Issued	Returned Value Type and Dest.	PSR Bits Affected
ADDf	read.f	rmw.f	f	f	f to Op. 2	none
SUBf	read.f	rmw.f	f	f	f to Op. 2	none
MULf	read.f	rmw.f	f	f	f to Op. 2	none
DIVf	read.f	rmw.f	f	f	f to Op. 2	none
MOVf	read.f	write.f	f	N/A	f to Op. 2	none
ABSf	read.f	write.f	f	N/A	f to Op. 2	none
NEGf	read.f	write.f	f	N/A	f to Op. 2	none
CMPf	read.f	read.f	f	f	N/A	N,Z,L
FLOORfi	read.f	write.i	f	N/A	i to Op. 2	none
TRUNCfi	read.f	write.i	f	N/A	i to Op. 2	none
ROUNDfi	read.f	write.i	f	N/A	i to Op. 2	none
MOVFL	read.F	write.L	F	N/A	L to Op. 2	none
MOVLF	read.L	write.F	L	N/A	F to Op. 2	none
MOVif	read.i	write.f	i	N/A	f to Op. 2	none
LFSR	read.D	N/A	D	N/A	N/A	none
SFSR	N/A	write.D	N/A	N/A	D to Op. 2	none

Note:
D=Double word.
i=Integer size (B,W,D) specified in mnemonic.
f=Floating-point type (F,L) specified in mnemonic.
N/A=Not applicable to this instruction.

3.0 Functional Description (Continued)

3.8.3 Custom Slave Instruction

Provided in the NS32008 is the capability of communicating with a user-defined, "Custom" Slave Processor. The instruction set provided for a Custom Slave Processor defines the instruction formats, the operand classes and the communication protocol. Left to the user are the interpretations of the opcode fields, the programming model of the Custom Slave and the actual types of data transferred. The protocol specifies only the size of an operand, not its data type.

Table 3-3 lists the relevant information for the Custom Slave instruction set. The designation "c" is used to represent an operand which can be a 32-bit ("D") or 64-bit ("Q") quantity in any format; the size is determined by the suffix on the mnemonic. Similarly, an "i" indicates an integer size (Byte, Word, Double Word) selected by the corresponding mnemonic suffix.

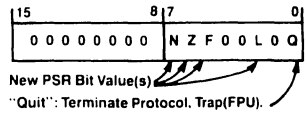

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FIGURE 3-24. Slave Processor Status Word Format

Any operand indicated as being of type "c" will not cause a transfer if the register addressing mode is specified. It is assumed in this case that the slave processor is already holding the operand internally.

For the instruction encodings, see Appendix A.

TABLE 3-3
Custom Slave Instruction Protocols

Mnemonic	Operand 1 Class	Operand 2 Class	Operand 1 Issued	Operand 2 Issued	Returned Value Type and Dest.	PSR Bits Affected
CCAL0c	read.c	rmw.c	c	c	c to Op. 2	none
CCAL1c	read.c	rmw.c	c	c	c to Op. 2	none
CCAL2c	read.c	rmw.c	c	c	c to Op. 2	none
CCAL3c	read.c	rmw.c	c	c	c to Op. 2	none
CMOV0c	read.c	write.c	c	N/A	c to Op. 2	none
CMOV1c	read.c	write.c	c	N/A	c to Op. 2	none
CMOV2c	read.c	write.c	c	N/A	c to Op. 2	none
CMOV3c	read.c	write.c	c	N/A	c to Op.2	none
CCMP0c	read.c	read.c	c	c	N/A	N,Z,L
CCMP1c	read.c	read.c	c	c	N/A	N,Z,L
CCV0ci	read.c	write.i	c	N/A	i to Op. 2	none
CCV1ci	read.c	write.i	c	N/A	i to Op. 2	none
CCV2ci	read.c	write.i	c	N/A	i to Op. 2	none
CCV3ic	read.i	write.c	i	N/A	c to Op. 2	none
CCV4DQ	read.D	write.Q	D	N/A	Q to Op. 2	none
CCV5QD	read.Q	write.D	Q	N/A	D to Op. 2	none
LCSR	read.D	N/A	D	N/A	N/A	none
SCSR	N/A	write.D	N/A	N/A	D to Op. 2	none
CATST0*	addr	N/A	D	N/A	N/A	F
CATST1*	addr	N/A	D	N/A	N/A	F
LCR*	read.D	N/A	D	N/A	N/A	none
SCR*	write.D	N/A	N/A	N/A	D to Op. 1	none

Note:

D = Double word.

i = Integer size (B, W, D) specified in mnemonic.

c = Custom size (D: 32 bits or Q: 64 bits) specified in mnemonic.

* = Privileged instruction; will trap if CPU is in User Mode.

N/A = Not applicable to this instruction.

4.0 Device Specifications

4.1 NS32008 PIN DESCRIPTIONS

The following is a brief description of all NS32008 pins. The descriptions reference portions of the Functional Description, Section 3.

4.1.1 Supplies

Power (V_{CC}): +5V Positive Supply. Section 3.1.

Logical Ground (GNDL): Ground reference for on-chip logic. Section 3.1.

Buffer Ground (GNDB): Ground reference for on-chip drivers connected to output pins. Section 3.1.

Back-Bias Generator (BBG): Output of on-chip substrate voltage generator. Section 3.1.

4.1.2 Input Signals

Clocks (PHI1, PHI2): Two-phase clocking signals. Section 3.2.

Ready (RDY): Active high. While RDY is inactive, the CPU extends the current bus cycle to provide for a slower memory or peripheral reference. Upon detecting RDY active, the CPU terminates the bus cycle. Section 3.4.1.

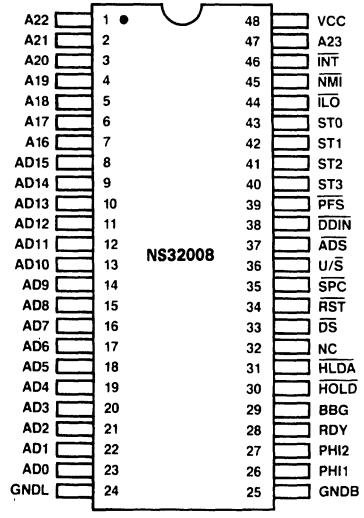
Hold Request ($\overline{\text{HOLD}}$): Active low. Causes the CPU to release the bus for DMA or multiprocessing purposes. Section 3.5.

Note: If the $\overline{\text{HOLD}}$ signal is generated asynchronously, it's set up and hold times may be violated. In this case it is recommended to synchronize it with CTTL to minimize the possibility of metastable states.

The CPU provides only one synchronization stage to minimize the $\overline{\text{HLDA}}$ latency. This is to avoid speed degradations in cases of heavy $\overline{\text{HOLD}}$ activity (i.e. DMA controller cycles interleaved with CPU cycles.)

Interrupt ($\overline{\text{INT}}$): Active low. Maskable Interrupt Request. Section 3.7.

Dual-In-Line Package



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Top View

Figure 4-1. NS32008 Connection Diagram

Order Number NS32008D or NS32008N
See NS Package Number D48A or N48A

Non-Maskable Interrupt ($\overline{\text{NMI}}$): Active low. Non-Maskable Interrupt Request. Section 3.7.

Reset ($\overline{\text{RST}}$): Active low. It initiates a Reset. Section 3.3.

4.1.3 Output Signals

Address Bits 16–23 (A16–A23): These are the most significant eight bits of the memory address bus. Section 3.4.

Address Strobe ($\overline{\text{ADS}}$): Active low. Controls address latches; indicates start of a bus cycle. Section 3.4.

Data Direction In ($\overline{\text{DDIN}}$): Active low. Status signal indicating direction of data transfer during a bus cycle. Section 3.4.

Status (ST0–ST3): Bus cycle status code, ST0 least significant. Section 3.4.2. Encodings are:

0000—Idle: CPU Inactive on Bus
0001—Idle: WAIT Instruction
0010—(Reserved)
0011—Idle: Waiting for Slave
0100—Interrupt Acknowledge, Master
0101—Interrupt Acknowledge, Cascaded
0110—End of Interrupt, Master
0111—End of Interrupt, Cascaded
1000—Sequential Instruction Fetch
1001—Nonsequential Instruction Fetch
1010—Data Transfer
1011—Read Read-Modify-Write Operand
1100—Read for Effective Address
1101—Transfer Slave Operand
1110—Read Slave Status Word
1111—Broadcast Slave ID.

Hold Acknowledge ($\overline{\text{HLDA}}$): Active low. Applied by the CPU in response to $\overline{\text{HOLD}}$ input, indicating that the bus has been released for DMA or multiprocessing purposes. Section 3.5.

User/Supervisor (U/$\overline{\text{S}}$): User or Supervisor Mode status. High state indicates User Mode, low indicates Supervisor Mode. Section 3.6.

Interlocked Operation ($\overline{\text{ILO}}$): Active low. Indicates that an interlocked instruction is being executed. Section 3.6.

Program Flow Status ($\overline{\text{PFS}}$): Active low. Pulse indicates beginning of an instruction execution. Section 3.6.

Data Strobe ($\overline{\text{DS}}$): Active low. Data strobe output. Section 3.4.

4.1.4 Input-Output Signals

Address/Data 0–15 (AD0–AD15): In all except Slave Processor bus cycles, pins AD0–AD7 serve as an 8-bit Multiplexed Address/Data bus, and pins AD8–AD15 hold address bits 8–15 throughout the bus cycle. Bit 0 is defined as the least-significant bit. Section 3.4.

In Slave Processor bus cycles, all 16 pins are used as a data bus (Section 3.4.6).

Slave Processor Control ($\overline{\text{SPC}}$): Active low. Used by the CPU as the data strobe output for Slave Processor transfers; used by Slave Processors to acknowledge completion of a slave instruction. Section 3.4.6 and Section 3.8. This pin should be pulled up to V_{CC} through a 10 kΩ resistor.

Data Strobe ($\overline{\text{DS}}$): Active low. Data Strobe output. Section 3.4.

4.0 Device Specifications (Continued)

4.2 ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias	0°C to +70°C
Storage Temperature	−65°C to +150°C
All Input or Output Voltages With Respect to GND	−0.5V to +7V
Power Dissipation	1.5 Watt

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Note: *Absolute maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended; operation should be limited to those conditions specified under Electrical Characteristics.*

4.3 ELECTRICAL CHARACTERISTICS T_A = 0 to + 70°C, V_{CC} = 5V ± 5%, GND = 0V

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High Level Input Voltage		2.0		V_{CC}+0.5	V
V_{IL}	Low Level Input Voltage		−0.5		0.8	V
V_{CH}	High Level Clock Voltage	PHI1, PHI2 pins only	V_{CC}−0.35		V_{CC}+0.5	V
V_{CL}	Low Level Clock Voltage	PHI1, PHI2 pins only	−0.5		0.3	V
V_{CLT}	Low Level Clock Voltage, Transient (ringing tolerance)	PHI1, PHI2 pins only	−0.5		0.6	V
V_{OH}	High Level Output Voltage	I_{OH} = −400 μA	2.4			V
V_{OL}	Low Level Output Voltage	I_{OL} = 2 mA			0.45	V
I_{ILS}	$\overline{SPC}$ Input Current (low)	V_{IN} = 0.4V, $\overline{SPC}$ in input mode	0.05		1.0	mA
I_I	Input Load Current	$0 \le V_{IN} \le V_{CC}$, All inputs except PHI1, PHI2, $\overline{SPC}$	−20		20	μA
I_L	Leakage Current Output and I/O Pins in TRI-STATE/Input Mode	$0.4 \le V_{IN} \le V_{CC}$	−20		30	μA
I_{CC}	Active Supply Current	I_{OUT}=0, T_A=25°C		180	300	mA

4.4 SWITCHING CHARACTERISTICS

4.4.1 Definitions

All the timing specifications given in this section refer to 2.0V on the rising or falling edges of the clock phases PHI1 and PHI2 and 0.8V or 2.0V on all other signals as illustrated in *Figures 4-2* and *4-3*, unless specifically stated otherwise.

Abbreviations:

L.E.—leading edge
T.E.—trailing edge
R.E.—rising edge
F.E.—falling edge

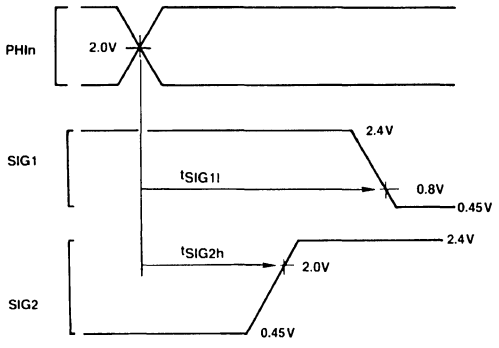

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FIGURE 4-2. Timing Specification Standard (Signal Valid After Edge)

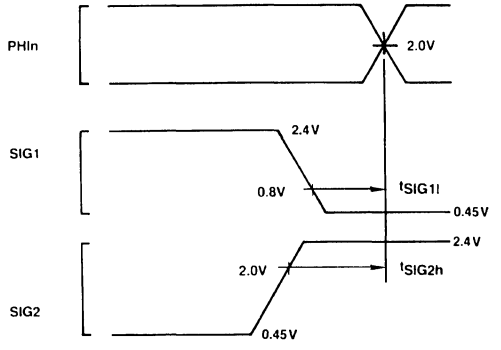

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FIGURE 4-3. Timing Specification Standard (Signal Valid Before Edge)

4.0 Device Specifications (Continued)

4.4.2 Timing Tables

4.4.2.1 Output Signals: Internal Propagation Delays, NS32008-10

Maximum times assume capacitive loading of 100 pF

Name	Figure	Description	Reference/Conditions	NS32008-10		Units
				Min	Max	
t_{ALv}	4-4	Address Bits 0–7 Valid	after R.E., PHI1 T1		50	ns
t_{ALh}	4-4	Address Bits 0–7 Hold	after R.E., PHI1 T2	5		ns
t_{Dv}	4-4	Data Valid (Write Cycle)	after R.E., PHI1 T2		50	ns
t_{Dh}	4-4	Data Hold (Write Cycle)	after R.E., PHI1 next T1 or Ti	0		ns
t_{AHv}	4-4	Address Bits 8–23 Valid	after R.E., PHI1 T1		50	ns
t_{AHh}	4-4	Address Bits 8–23 Hold	after R.E., PHI1 next T1 or Ti	0		ns
t_{ALADSs}	4-5	Address Bits 0–7 Set Up	before $\overline{ADS}$ T.E.	25		ns
t_{AHADSs}	4-5	Address Bits 8–23 Set Up	before $\overline{ADS}$ T.E.	25		ns
t_{ALADSh}	4-10	Address Bits 0–7 Hold	after $\overline{ADS}$ T.E.	15		ns
t_{ALf}	4-5	Address Bits 0–7 Floating	after R.E., PHI1 T2		25	ns
t_{STv}	4-4	Status (ST0–ST3) Valid	after R.E., PHI1 T4 (before T1, see note)		45	ns
t_{STh}	4-4	Status (ST0–ST3) Hold	after R.E., PHI1 T4 (after T1)	0		ns
t_{DDINv}	4-5	$\overline{DDIN}$ Signal Valid	after R.E., PHI1 T1		50	ns
t_{DDINh}	4-5	$\overline{DDIN}$ Signal Hold	after R.E., PHI1 next T1 or Ti	0		ns
t_{ADSa}	4-4	$\overline{ADS}$ Signal Active (Low)	after R.E., PHI1 T1		35	ns
t_{ADSia}	4-4	$\overline{ADS}$ Signal Inactive	after R.E., PHI2 T1		40	ns
t_{ADSw}	4-4	$\overline{ADS}$ Pulse Width	at 0.8V (both edges)	30		ns
t_{DSa}	4-4	$\overline{DS}$ Signal Active (Low)	after R.E., PHI1 T2		40	ns
t_{DSia}	4-4	$\overline{DS}$ Signal Inactive	after R.E., PHI1 T4		40	ns
t_{ALf}	4-6	AD0–AD7 Floating (Caused by $\overline{HOLD}$)	after R.E., PHI1 T1		25	ns
t_{AHf}	4-6	A8–A23 Floating (Caused by $\overline{HOLD}$)	after R.E., PHI1 T1		25	ns
t_{ADSf}	4-6	$\overline{ADS}$ Floating (Caused by $\overline{HOLD}$)	after R.E., PHI1 Ti		50	ns
t_{DDINf}	4-6	$\overline{DDIN}$ Floating (Caused by $\overline{HOLD}$)	after R.E., PHI1 Ti		50	ns
t_{HLDAa}	4-6	$\overline{HLDA}$ Signal Active (Low)	after R.E., PHI1 Ti		50	ns
t_{HLDAia}	4-8	$\overline{HLDA}$ Signal Inactive	after R.E., PHI1 Ti		50	ns
t_{ADSr}	4-8	$\overline{ADS}$ Signal Returns from Floating (Caused by $\overline{HOLD}$)	after R.E., PHI1 Ti		55	ns
t_{DDINr}	4-8	$\overline{DDIN}$ Signal Returns from Floating (Caused by $\overline{HOLD}$)	after R.E., PHI1 Ti		55	ns
t_{SPCa}	4-13	$\overline{SPC}$ Output Active (Low)	after R.E., PHI1 T1		35	ns
t_{SPCia}	4-13	$\overline{SPC}$ Output Inactive	after R.E., PHI1 T4		35	ns
t_{SPCnf}	4-15	$\overline{SPC}$ Output Nonforcing	after R.E., PHI2 T4		30	ns
t_{Dv}	4-11	Data Valid (Slave Processor Write)	after R.E., PHI1 T1		50	ns
t_{Dh}	4-11	Data Hold (Slave Processor Write)	after R.E., PHI1 next T1 or Ti	0		ns
t_{PFSw}	4-15	$\overline{PFS}$ Pulse Width	at 0.8V (both edges)	50		ns
t_{PFSa}	4-15	$\overline{PFS}$ Pulse Active (Low)	after R.E., PHI2		40	ns
t_{PFSia}	4-15	$\overline{PFS}$ Pulse Inactive	after R.E., PHI2		40	ns

4.0 Device Specifications (Continued)

4.4.2.1 Output Signals: Internal Propagation Delays, NS32008-10 (Continued)

Name	Figure	Description	Reference/ Conditions	NS32008-10		Units
				Min	Max	
t_{ILOs}	4-17	$\overline{ILO}$ Signal Setup	before R.E., PHI1 T1 of first interlocked read cycle	50		ns
t_{ILOh}	4-18	$\overline{ILO}$ Signal Hold	after R.E., PHI1 T3 of last interlocked write cycle	10		ns
t_{ILOa}	4-19	$\overline{ILO}$ Signal Active (Low)	after R.E., PHI1		40	ns
t_{ILOia}	4-19	$\overline{ILO}$ Signal Inactive	after R.E., PHI1		40	ns
t_{USv}	4-20	U/$\overline{S}$ Signal Valid	after R.E., PHI1 T4		45	ns
t_{USh}	4-20	U/$\overline{S}$ Signal Hold	after R.E., PHI1 T1	8		ns
t_{NSPF}	4-16b	Nonsequential Fetch to Next $\overline{PFS}$ Clock Cycle	after R.E., PHI1 T1	4		t_{Cp}
t_{PFNS}	4-16a	$\overline{PFS}$ Clock Cycle to Next Non-Sequential Fetch	before R.E., PHI1 T1	4		t_{Cp}
t_{LXPF}	4-25	Last Operand Transfer of an Instruction to Next $\overline{PFS}$ clock Cycle	before R.E., PHI1 T1 of first bus cycle of transfer	0		t_{Cp}

Note: Every memory cycle starts with T4, during which Cycle Status is applied. If the CPU was idling, the sequence will be: ". . .Ti, T4, T1. . .". If the CPU was not idling, the sequence will be: ". . .T4, T1. . .".

4.4.2.2 Input Signal Requirements: NS32008-10

Name	Figure	Description	Reference/ Conditions	NS32008-10		Units
				Min	Max	
t_{PWR}	4-21	Power Stable to $\overline{RST}$ R.E.	after V_{CC} reaches 4.5V	50		μs
t_{DIs}	4-5	Data in Setup (Read Cycle)	before F.E., PHI2 T3	15		ns
t_{DIh}	4-5	Data in Hold (Read Cycle)	after R.E., PHI1 T4	3		ns
t_{HLDa}	4-6	$\overline{HOLD}$ Active (Low) Setup Time (See Note)	before F.E., PHI2 TX1	25		ns
t_{HLDia}	4-8	$\overline{HOLD}$ Inactive Setup Time	before F.E., PHI2 Ti	25		ns
t_{HLDh}	4-6	$\overline{HOLD}$ Hold Time	after R.E., PHI1 TX2	0		ns
t_{RDYs}	4-9, 4-10	RDY Setup Time	before F.E., PHI2 T2 or T3	25		ns
t_{RDYh}	4-9, 4-10	RDY Hold Time	after F.E., PHI1 T3	5		ns
t_{RSTs}	4-21, 4-22	$\overline{RST}$ Setup Time	before F.E., PHI1	15		ns
t_{RSTw}	4-22	$\overline{RST}$ Pulse Width	at 0.8V (both edges)	64		t_{Cp}
t_{INTs}	4-23	$\overline{INT}$ Setup Time	before T.E., PHI1	20		ns
t_{NMIw}	4-28	$\overline{NMI}$ Pulse Width	at 0.8V (both edges)	70		ns
t_{DIs}	4-12	Data Setup (Slave Read Cycle)	before F.E., PHI2 T1	15		ns
t_{DIh}	4-12	Data Hold (Slave Read Cycle)	after R.E., PHI1 T4	3		ns
t_{SPCd}	4-13	$\overline{SPC}$ Pulse Delay from Slave	after R.E., PHI2 T4	25		ns
t_{SPCs}	4-13	$\overline{SPC}$ Setup Time	Before F.E., PHI1	30		ns
t_{SPCw}	4-13	SPC Pulse Width from Slave Processor (Async. Input)	at 0.8V (both edges)	20		ns

NOTE: This setup time is necessary to ensure prompt acknowledgement via $\overline{HLDA}$ and the ensuing floating of CPU off the buses. Note that the time from the receipt of the $\overline{HOLD}$ signal until the CPU floats is a function of the time $\overline{HOLD}$ signal goes low, and the state of the RDY input.

4.0 Device Specifications (Continued)

4.4.2.3 Clocking Requirements: NS32008-10

Name	Figure	Description	Reference/ Conditions	NS32008-10		Unit
				Min	Max	
t_{Cp}	4-14	Clock Period	R.E., PHI1, PHI2 to next R.E., PHI1, PHI2	100	250	ns
t_{CLw}	4-14	PHI1, PHI2 Pulse Width	at 2.0V on PHI1, PHI2 (both edges)	0.5 t_{Cp} −10 ns		
t_{CLh}	4-14	PHI1, PHI2 High Time	at V_{CC} − 0.9V on PHI1, PHI2 (both edges)	0.5t_{Cp} −15 ns		
t_{CLl}	4-14	PHI1, PHI2 Low Time	at 0.8V on PHI1, PHI2	0.5t_{Cp} −5 ns		
$t_{nOVL(1,2)}$	4-14	Non-Overlap Time	0.8V on F.E., PHI1, PHI2 to 0.8V on R.E., PHI1, PHI2	−2	5	ns
t_{nOVLas}		Non-Overlap Asymmetry ($t_{nOVL(1)} - t_{nOVL(2)}$)	at 0.8V on PHI1, PHI2	−4	4	ns
t_{CLwas}		PHI1, PHI2 Asymmetry ($t_{CLw(1)} - t_{CLw(2)}$)	at 2.0V on PHI1, PHI2	−5	5	ns

4.0 Device Specifications (Continued)

4.4.3 Timing Diagrams

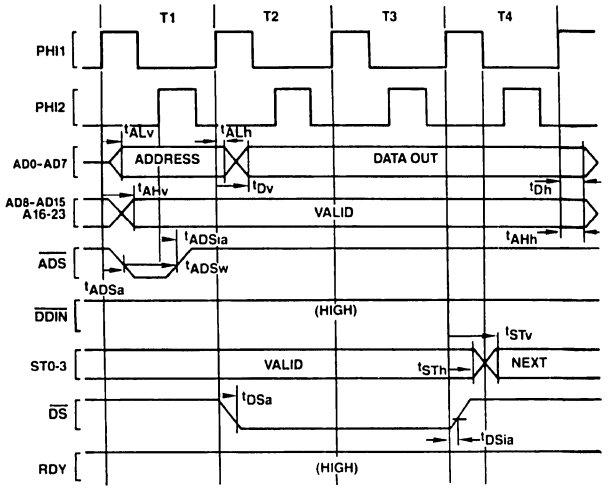

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FIGURE 4-4. Write Cycle

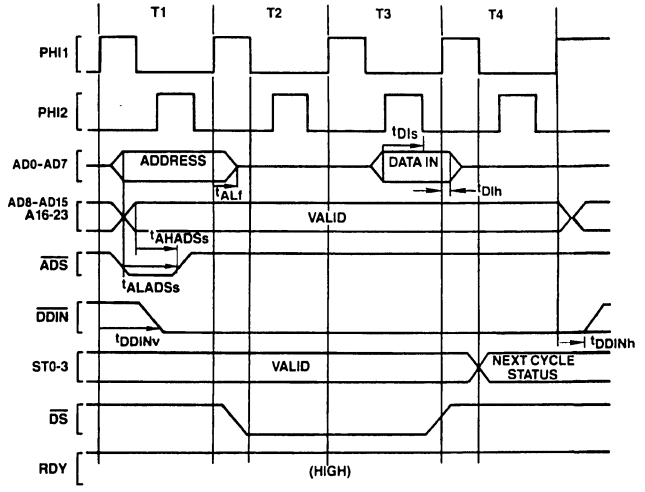

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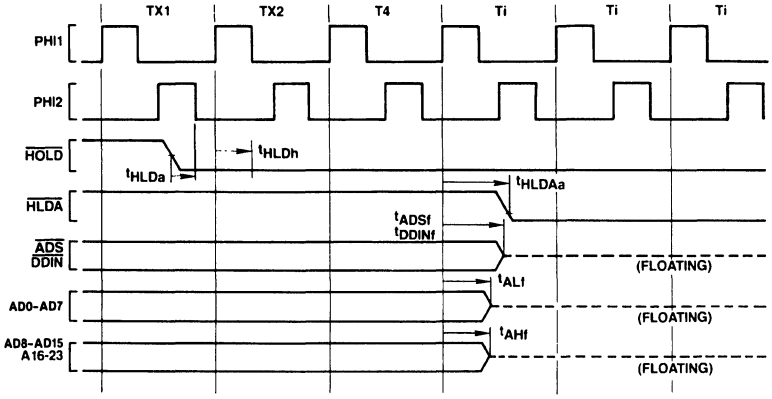
FIGURE 4-5. Read Cycle

4.0 Device Specifications (Continued)



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Note: Whenever the CPU is not idling (not in Ti), the $\overline{HOLD}$ request ($\overline{HOLD}$ low) must be active t_{HLDa} before the falling edge of PHI2 of the clock cycle that appears two clock cycles before T4(TX1) and stay low until t_{HLDh} after the rising edge of PHI1 of the clock cycle that precedes T4(TX2) for the request to be acknowledged.

FIGURE 4-6. Floating by $\overline{HOLD}$ Timing (CPU Not Idle Initially)

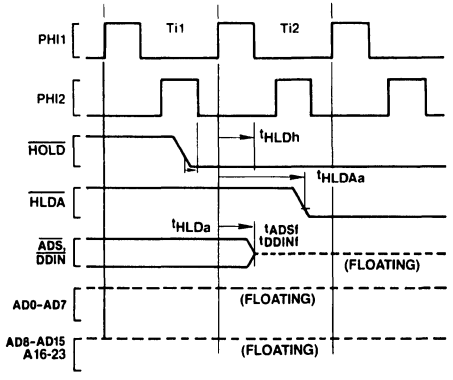

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FIGURE 4-7. Floating by $\overline{HOLD}$ Timing (CPU Initially Idle)

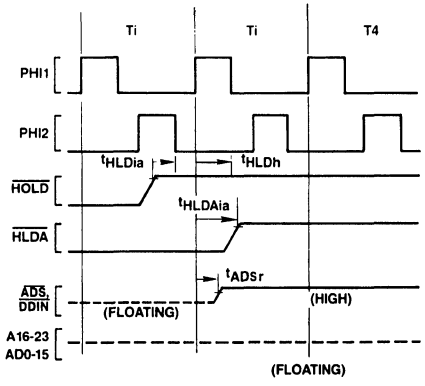

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FIGURE 4-8. Release from $\overline{HOLD}$

4.0 Device Specifications (Continued)

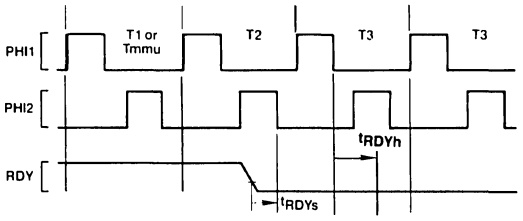

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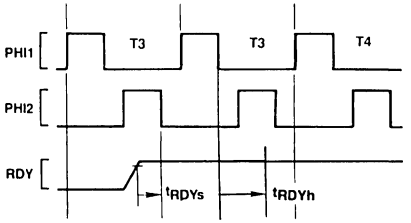
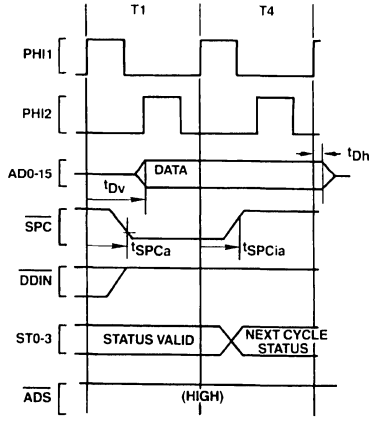
FIGURE 4-9. Ready Sampling (CPU Initially READY)



TL/EE/6156-46

FIGURE 4-10. Ready Sampling (CPU Initially NOT READY)



TL/EE/6156-47

FIGURE 4-11. Slave Processor Write Timing

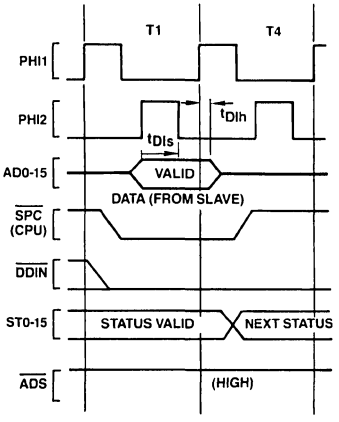


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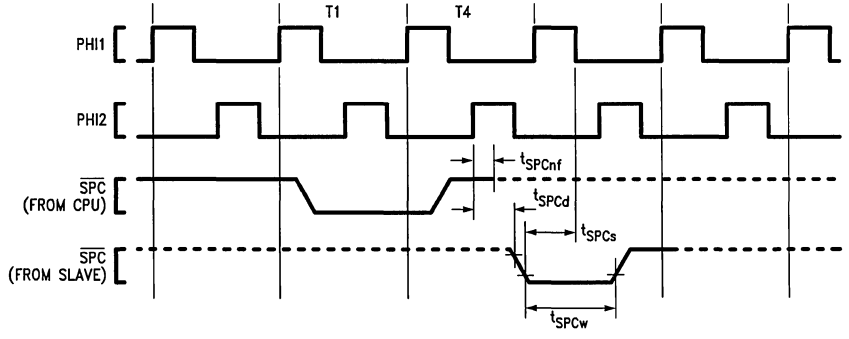
FIGURE 4-12. Slave Processor Read Timing



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Note: After transferring last operand to a Slave Processor, CPU turns OFF driver and holds $\overline{SPC}$ high with internal 5 kΩ pullup.

FIGURE 4-13. $\overline{SPC}$ Timing

4.0 Device Specifications (Continued)

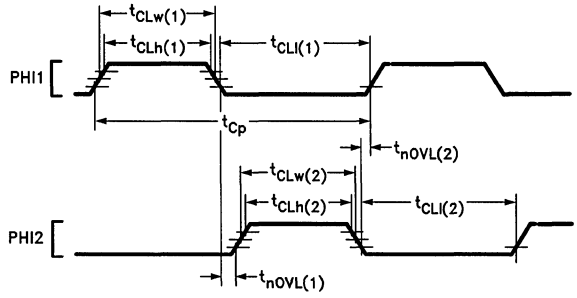

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FIGURE 4-14. Clock Waveforms

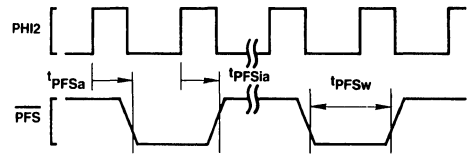

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FIGURE 4-15. Relationship of $\overline{PFS}$ to Clock Cycles

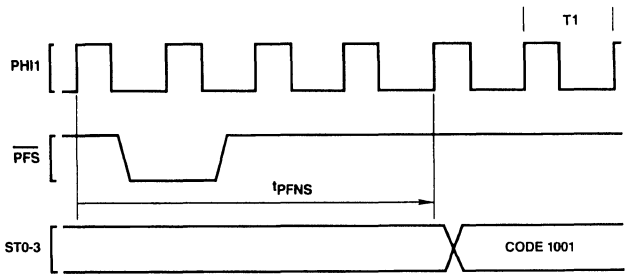

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FIGURE 4-16a. Guaranteed Delay, $\overline{PFS}$ to Non-Sequential Fetch

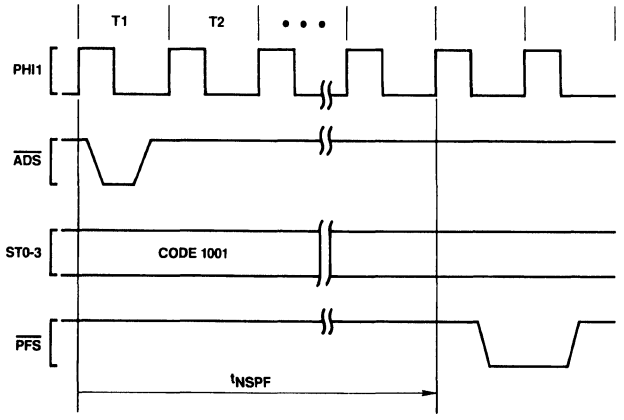

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FIGURE 4-16b. Guaranteed, Delay, Non-Sequential Fetch to $\overline{PFS}$

4.0 Device Specifications (Continued)

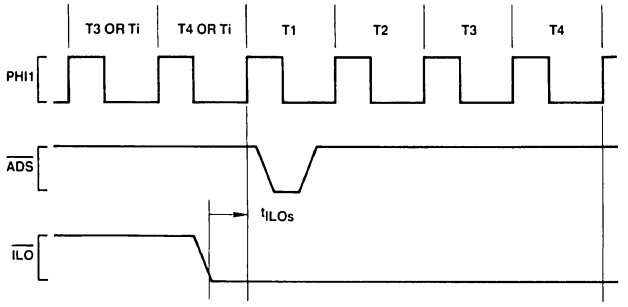

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FIGURE 4-17. Relationship of $\overline{ILO}$ to First Operand Cycle of an Interlocked Instruction

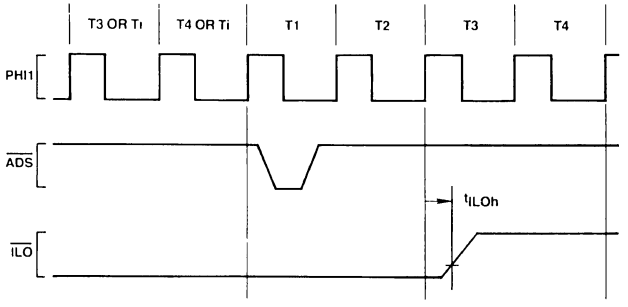

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FIGURE 4-18. Relationship of $\overline{ILO}$ to Last Operand Cycle of an Interlocked Instruction

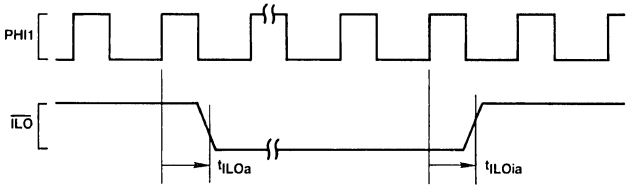

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FIGURE 4-19. Relationship of $\overline{ILO}$ to Any Clock Cycle

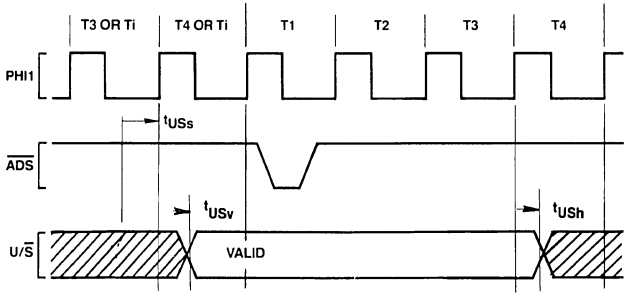

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FIGURE 4-20. U/$\overline{S}$ Relationship to Any Bus Cycle— Guarantee Valid Interval

4.0 Device Specifications (Continued)

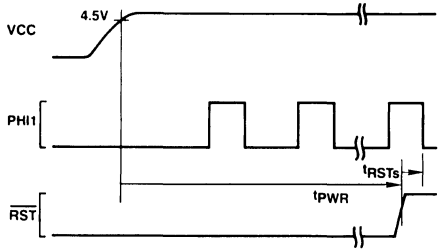

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FIGURE 4-21. Power-On Reset

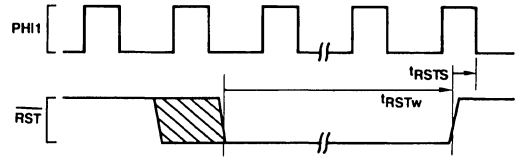

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FIGURE 4-22. Non-Power-On Reset

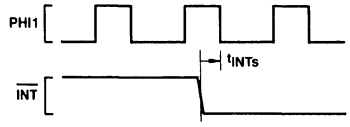

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FIGURE 4-23. $\overline{INT}$ Interrupt Signal Detection

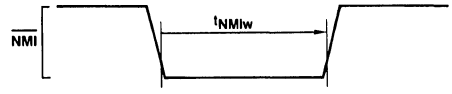

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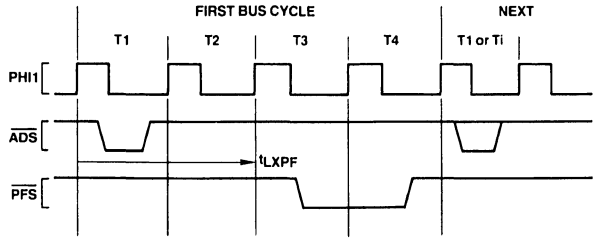
FIGURE 4-24. $\overline{NMI}$ Interrupt Signal Timing



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Note: In a transfer of a Read-Modify-Write type operand, this is the Read transfer, displaying RMW Status (Code 1011).

FIGURE 4-25. Relationship Between Last Data Transfer of an Instruction and $\overline{PFS}$ Pulse of Next Instruction

Appendix A: Instruction Formats

NOTATIONS

i ..... Integer Type Field
B=00 (Byte)
W=01 (Word)
D=11 (Double Word)

f ..... Floating-Point Type Field
F=1 (Standard Floating: 32 bits)
L=0 (Long Floating: 64 bits)

c ..... Custom Type Field
D=1 (Double Word)
Q=0 (Quad Word)

op ..... Operation Code
Valid encodings shown with each format.

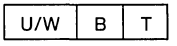
gen, gen1,
gen2 ..... General Addressing Mode Field.
See Section 2.2 for encodings.

reg ..... General Purpose Register Number

cond ..... Condition Code Field
0000=EQual: Z=1
0001=Not Equal: Z=0
0010=Carry Set: C=1
0011=Carry Clear: C=0
0100=Higher: L=1
0101=Lower or Same: L=0
0110=Greater Than: N=1
0111=Less or Equal: N=0
1000=Flag Set: F=1
1001=Flag Clear: F=0
1010=LOwer: L=0 and Z=0
1011=Higher or Same: L=1 or Z=1
1100=Less Than: N=0 and Z=0
1101=Greater or Equal: N=1 or Z=1
1110=(Unconditionally True)
1111=(Unconditionally False)

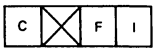
short ..... Short Immediate Value. May contain:
quick: Signed 4-bit value, in MOVQ, ADDQ, CMPQ, ACB
cond: Condition Code (above), in Scond.
areg: CPU Dedicated Register, in LPR, SPR.
0000=US
0001–0111=(Reserved)
1000=FP
1001=SP
1010=SB
1011=(Reserved)
1100=(Reserved)
1101=PSR
1110=INTBASE
1111=MOD

Options: in String Instructions



T=Translated
B=Backward
U/W=00: None
01: While Match
11: Until Match

Configuration bits, in SETCFG:



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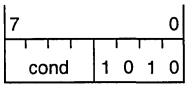
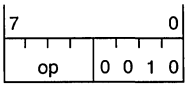


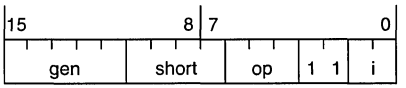
Format 0

Bcond (BR)



Format 1

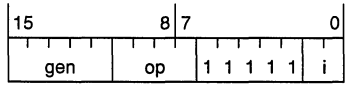
BSR	–0000	ENTER	–1000
RET	–0001	EXIT	–1001
CXP	–0010	NOP	–1010
RXP	–0011	WAIT	–1011
RETT	–0100	DIA	–1100
RETI	–0101	FLAG	–1101
SAVE	–0110	SVC	–1110
RESTORE	–0111	BPT	–1111



Format 2

ADDQ	–000	ACB	–100
CMPQ	–001	MOVQ	–101
SPR	–010	LPR	–110
Scond	–011		

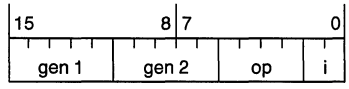
Appendix A: Instruction Formats (Continued)



Format 3

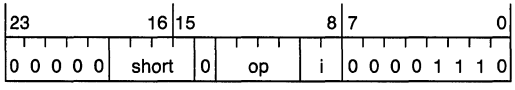
CXPD	−0000	ADJSP	−1010
BICPSR	−0010	JSR	−1100
JUMP	−0100	CASE	−1110
BISPSR	−0110		

Trap (UND) on XXX1, 1000



Format 4

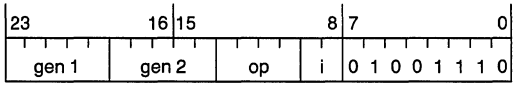
ADD	−0000	SUB	−1000
CMP	−0001	ADDR	−1001
BIC	−0010	AND	−1010
ADDC	−0100	SUBC	−1100
MOV	−0101	TBIT	−1101
OR	−0110	XOR	−1110



Format 5

MOVS	−0000	SETCFG	−0010
CMPS	−0001	SKPS	−0011

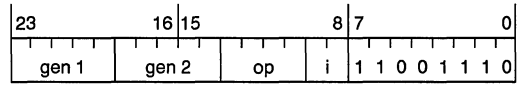
Trap (UND) on 1XXX, 01XX



Format 6

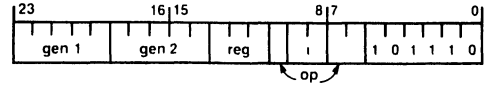
ROT	−0000	NEG	−1000
ASH	−0001	Trap (UND)	−1010
CBIT	−0010	SUBP	−1011
CBITI	−0011	ABS	−1100
Trap (UND)	−0100	COM	−1101
LSH	−0101	IBIT	−1110
SBIT	−0110	ADDP	−1111
SBITI	−0111		

Trap (UND) on all others



Format 7

MOVM	−0000	MUL	−1000
CMPM	−0001	MEI	−1001
INSS	−0010	Trap (UND)	−1010
EXTS	−0011	DEI	−1011
MOVXBW	−0100	QUO	−1100
MOVZBW	−0101	REM	−1101
MOVZiD	−0110	MOD	−1110
MOVXiD	−0111	DIV	−1111



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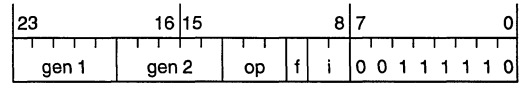
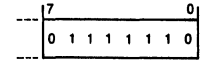
Format 8

EXT	−000	INDEX	−100
CVTP	−001	FFS	−101
INS	−010		
CHECK	−011		



Format 9

MOVif	−000	ROUND	−100
LFSR	−001	TRUNC	−101
MOVLF	−010	SFSR	−110
MOVFL	−011	FLOOR	−111



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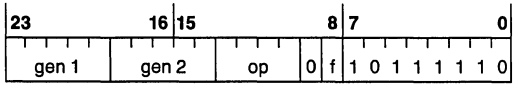
Format 10

Trap (UND) Always

Appendix A: Instruction Formats (Continued)



Format 11

ADDf	−0000	DIVf	−1000
MOVf	−0001	Trap (Slave)	−1001
CMPf	−0010	Trap (UND)	−1010
Trap (Slave)	−0011	Trap (UND)	−1011
SUBf	−0100	MULf	−1100
NEGf	−0101	ABSf	−1110
Trap (UND)	−0110	Trap (UND)	−1110
Trap (UND)	−0111	Trap (UND)	−1111

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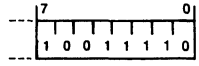
Format 12

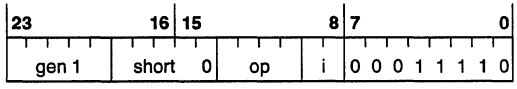
Trap (UND) Always



TL/EE/6156-77

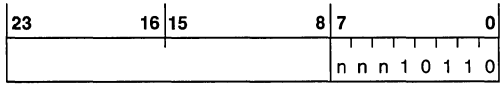
Format 13

Trap (UND) Always



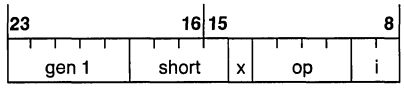
Format 14

Trap (UND) Always



Format 15
(Custom Slave)

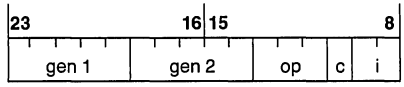
nnn **Operation Word Format**



000

Format 15.0

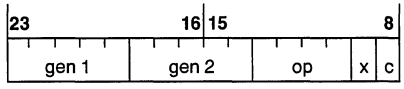
CATST0	−0000	LCR	−0010
CATST1	−0001	SCR	−0011



001

Format 15.1

CCV3	−000	CCV2	−100
LCSR	−001	CCV1	−101
CCV5	−010	SCSR	−110
CCV4	−011	CCV0	−111



101

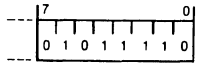
Format 15.5

CCAL0	−0000	CCAL3	−1000
CMOV0	−0001	CMOV3	−1001
CCMP0	−0010	Trap (UND)	−1010
CCMP1	−0011	Trap (UND)	−1011
CCAL1	−0100	CCAL2	−1100
CMOV2	−0101	CMOV1	−1101
Trap (UND)	−0110	Trap (UND)	−1110
Trap (UND)	−0111	Trap (UND)	−1111

If nnn=010, 011, 100, 110, 111, then Trap (UND) Always

2

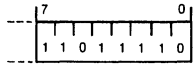
Appendix A: Instruction Formats (Continued)



TL/EE/6156-78

Format 16

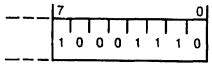
Trap (UND) Always



TL/EE/6156-79

Format 17

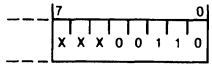
Trap (UND) Always



TL/EE/6156-80

Format 18

Trap (UND) Always

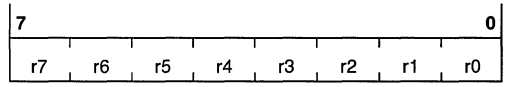


TL/EE/6156-81

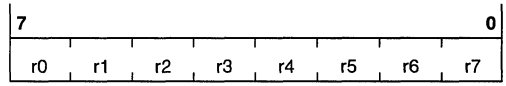
Format 19

Trap (UND) Always

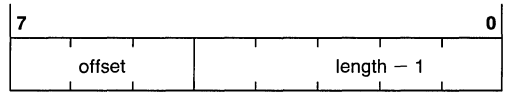
Implied Immediate Encodings:



Register Mask, appended to SAVE, ENTER



Register Mask, appended to RESTORE, EXIT



Offset/Length Modifier, appended to INSS, EXTS

Section 3

Slave Processors

Section 3 Contents

National Semiconductor

PRELIMINARY

NS32382-10/NS32382-15 Memory Management Units

General Description

The NS32382 Memory Management Unit (MMU) provides hardware support for demand-paged virtual memory implementations. The NS32382 functions as a slave processor in Series 32000 microprocessor-based systems. Its specific capabilities include fast dynamic translation, protection, and detailed status to assist an operating system in efficiently managing up to 4 Gbytes of physical memory. Support for multiple address spaces, virtual machines, and program debugging is provided.

High-speed address translation is performed on-chip through a 32-entry fully associative translation look-aside buffer (TLB), which maintains itself from tables in memory with no software intervention. Protection violations and page faults (references to non-resident pages) are automatically detected by the MMU, which invokes the instruction abort feature of the CPU.

Additional features for program debugging include three breakpoint registers which provide the programmer with powerful stand-alone debugging capability.

Features

- Compatible with the NS32332 CPU
- Totally automatic mapping of 4 Gbyte virtual address space using memory based tables
- On-chip translation look-aside buffer allows 97% of translations to occur in one clock for most applications
- Full hardware support for virtual memory and virtual machines
- Implements "referenced" bits for simple, efficient working set management
- Protection mechanisms implemented via access level checking and dual space mapping
- Program debugging support
- Dedicated 32-bit physical address bus
- Non-cacheable page support
- 125-pin PGA (Pin grid array) package

Conceptual Address Translation Model

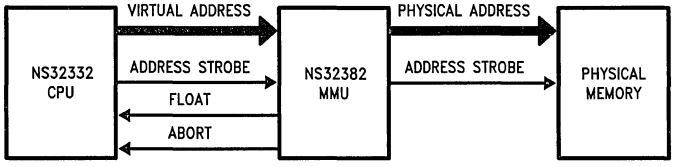


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Table Of Contents

List of Illustrations

List of Illustrations (Continued)

Tables

1.0 Product Introduction

The NS32382 MMU provides hardware support for three basic features of the Series 32000; dynamic address translation, access level checking and software debugging. Dynamic Address Translation is required to implement demand-paged virtual memory. Access level checking is performed during address translation, ensuring that unauthorized accesses do not occur. Because the MMU resides on the local bus and is in an ideal location to monitor CPU activity, debugging functions are also included.

The MMU is intended for use in implementing demand-paged virtual memory. The concept of demand-paged virtual memory is illustrated in *Figure 1-1.* At any point in time, a program sees a uniform addressing space of up to 4 gigabytes (the "virtual" space), regardless of the actual size of the memory physically present in the system (the "physical" space). The full virtual space is recorded as an image on a mass storage device. Portions of the virtual space needed by a running program are copied into physical memory when needed.

To make the virtual information directly available to a running program, a mapping must be established between the virtual addresses asserted by the CPU and the physical addresses of the data being referenced.

To perform this mapping, the MMU divides the virtual memory space into 4 Kbyte blocks called "pages". It interprets the 32-bit address from the CPU as a 20-bit "page number" followed by a 12-bit offset, which indicates the position of a byte within the selected page. Similarly, the MMU divides the physical memory into 4 Kbyte frames, each of which can hold a virtual page.

The translation process is therefore modeled as accepting a virtual page number from the CPU and substituting the corresponding physical page frame number for it, as shown in *Figure 1-2.* The offset is not changed. The translated page frame number is 20 bits long. Physical addresses issued by the MMU are 32 bits wide.

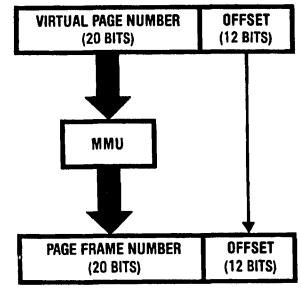

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FIGURE 1-2. NS32382 Address Translation Model

Generally, in virtual memory systems the available physical memory space is smaller than the maximum virtual memory space. Therefore, not all virtual pages are simultaneously resident. Nonresident pages are not directly addressable by the CPU. Whenever the CPU issues a virtual address for a nonresident or nonexistent page, a "page fault" will result. The MMU signals this condition by invoking the Abort feature of the CPU. The CPU then halts the memory cycle, restores its internal state to the point prior to the instruction being executed, and enters the operating system through the abort trap vector.

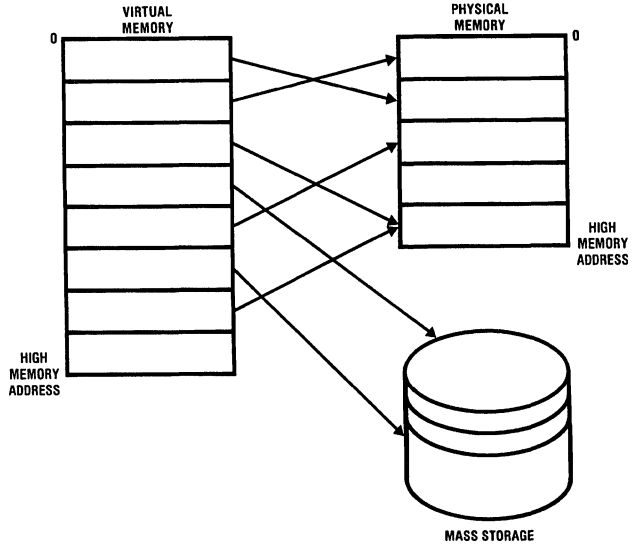

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FIGURE 1-1. The Virtual Memory Model

1.0 Product Introduction (Continued)

The operating system reads from the MMU the virtual address which caused the abort. It selects a page frame which is either vacant or not recently used and, if necessary, writes this frame back to mass storage. The required virtual page is then copied into the selected page frame.

The MMU is informed of this change by updating the page tables (Section 3.2), and the operating system returns control to the aborted program using the RETT instruction. Since the return address supplied by the abort trap is the address of the aborted instruction, execution resumes by retrying the instruction.

This sequence is called paging. Since a page fault encountered in normal execution serves as a demand for a given page, the whole scheme is called demand-paged virtual memory.

The MMU also provides debugging support. It may be programmed to monitor the CPU bus for a single or a range of virtual addresses in real time.

1.1 PROGRAMMING CONSIDERATIONS

When a CPU instruction is aborted as a result of a page fault, some memory resident data might have been already modified by the instruction before the occurrence of the abort.

This could compromise the restartability of the instruction when the CPU returns from the abort routine.

To guarantee correct results following the re-execution of the aborted instruction, the following actions should not be attempted:

a) No instruction should try to overlay part of a source operand with part of the result. It is, however, permissible to rewrite the result into the source operand exactly, if page faults are being generated only by invalid pages and not by write protection violations (for example, the instruction "ABSW X, X", which replaces X with its absolute value). Also, never write to any memory location which is necessary for calculating the effective address of either operand (i.e. the pointer in "Memory Relative" addressing mode; the Link Table pointer or Link Table Entry in "External" addressing mode).

b) No instruction should perform a conversion in place from one data type to another larger data type (Example: MOVWF X, X which replaces the 16-bit integer value in memory location X with its 32-bit floating-point value). The addressing mode combination "TOS, TOS" is an exception, and is allowed. This is because the least-significant part of the result is written to the possibly invalid page before the source operand is affected. Also, integer conversions to larger integers always work correctly in place, because the low-order portion of the result always matches the source value.

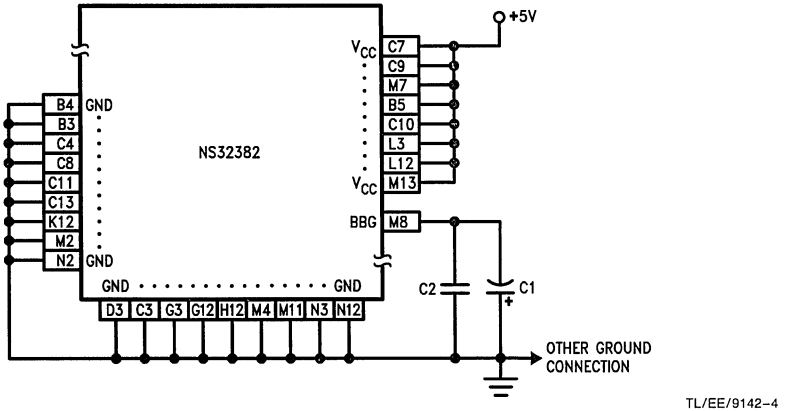
c) When performing the MOVM instruction, the entire source and destination blocks must be considered "operands" as above, and they must not overlap.

2.0 Functional Description

2.1 POWER AND GROUNDING

The NS32382 requires a single 5V power supply, applied on eight (V_{CC}) pins. These pins should be connected together by a power (V_{CC}) plane on the printed circuit board. See *Figure 2-1*.

The grounding connections are made on eighteen (GND) pins.



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C1 = 1 μF, Tantalum.

C2 = 1000 pF, low inductance. This should be either a disc or monolithic ceramic capacitor.

FIGURE 2-1. Recommended Supply Connections

2.0 Functional Description (Continued)

These pins should be connected together by a ground (GND) plane on the printed circuit board.

In addition to V_{CC} and Ground, the NS32382 MMU uses an internally-generated negative voltage (BBG), output of the on-chip substrate voltage generator. It is necessary to filter this voltage externally by attaching a pair of capacitors *(Figure 2-1)* from the BBG pin to ground.

2.2 CLOCKING

The NS32382 inputs clocking signals from the NS32301 Timing Control Unit (TCU), which presents two non-overlapping phases of a single clock frequency. These phases are called PHI1 (pin B8) and PHI2 (pin B9). Their relationship to each other is shown in *Figure 2-2.*

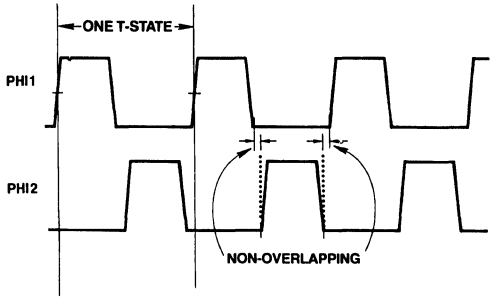

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FIGURE 2-2. Clock Timing Relationships

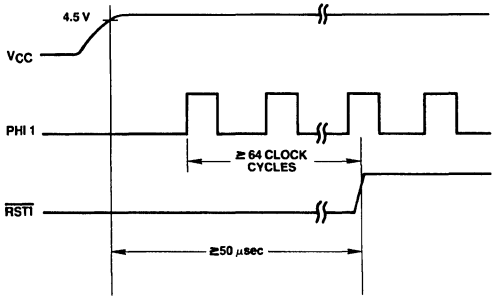

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FIGURE 2-3. Power-On Reset Requirements

Each rising edge of PHI1 defines a transition in the timing state ("T-State") of the MMU. One T-State represents one hardware cycle within the MMU, and/or one step of an external bus transfer. See Section 4 for complete specifications of PHI1 and PHI2.

As the TCU presents signals with very fast transitions, it is recommended that the conductors carrying PHI1 and PHI2 be kept as short as possible, and that they not be connected to any devices other than the CPU and MMU. A TTL Clock signal (CTTL) is provided by the TCU for all other clocking.

2.3 RESETTING

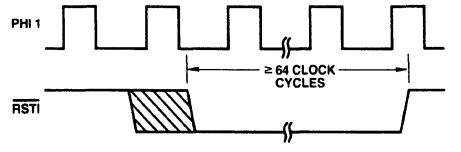
The $\overline{RSTI}$ input pin is used to reset the NS32382. The MMU responds to $\overline{RSTI}$ by terminating processing, resetting its internal logic and clearing the MCR and MSR registers.

Only the MCR and MSR registers are changed on reset. No other program accessible registers are affected.

The $\overline{RST}/\overline{ABT}$ signal is activated by the MMU on reset. This signal should be used to reset the CPU.

On application of power, $\overline{RSTI}$ must be held low for at least 50 μs after V_{CC} is stable. This is to ensure that all on-chip voltages are completely stable before operation. Whenever a Reset is applied, it must also remain active for not less than 64 clock cycles. See *Figures 2-3* and *2-4.*

The NS32C201 Timing Control Unit (TCU) provides circuitry to meet the Reset requirements of the NS32382 MMU. *Figure 2-5* shows the recommended connections.



TL/EE/9142-7

FIGURE 2-4. General Reset Timing

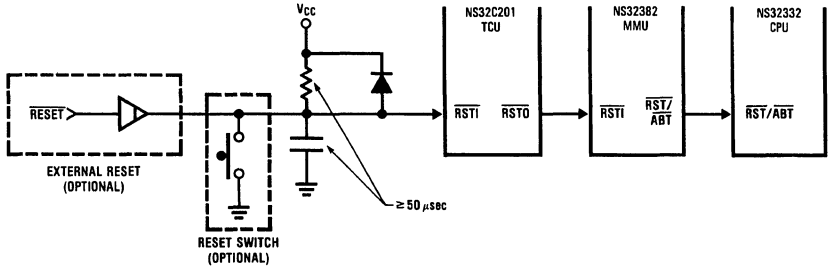


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FIGURE 2-5. Recommended Reset Connections, Memory-Managed System

2.0 Functional Description (Continued)

2.4 BUS OPERATION

2.4.1 Interconnections

The MMU runs synchronously with the CPU, sharing with it a single multiplexed address/data bus. The interconnections used by the MMU for bus control, when used in conjunction with the NS32332, are shown in *Figure A-1* (Appendix A).

The CPU issues 32-bit virtual addresses on the bus, and status information on other pins, pulsing the signal $\overline{ADS}$ low. These are monitored by the MMU. The MMU issues 32-bit physical addresses on the Physical Address bus, pulsing the $\overline{PAV}$ line low. The $\overline{PAV}$ pulse triggers the address latches and signals the NS32C201 TCU to begin a bus cycle. The TCU in turn generates the necessary bus control signals and synchronizes the insertion of WAIT states, by providing the signal RDY to the MMU and CPU. Note that it is the MMU rather than the CPU that actually triggers bus activity in the system.

The functions of other interface signals used by the MMU to control bus activity are described below.

The ST0–ST3 pins indicate the type of cycle being initiated by the CPU. ST0 is the least-significant bit of the code. Table 2-1 shows the interpretations of the status codes presented on these lines.

Status codes that are relevant to the MMU's function during a memory reference are:

1000, 1001 Instruction Fetch status, used by the debugging features to distinguish between data and instruction references.

1010 Data Transfer. A data value is to be transferred.

1011 Read RMW Operand. Although this is always a Read cycle, the MMU treats it as a Write cycle for purposes of protection and breakpointing.

1100 Read for Effective Address. Data used for address calculation is being transferred.

The MMU ignores all other status codes. The status codes 1101, 1110 and 1111 are also recognized by the MMU in conjunction with pulses on the $\overline{SPC}$ line while it is executing Slave Processor instructions, but these do not occur in a context relevant to address translation.

TABLE 2-1. ST0–ST3 Encodings (ST0 is the Least Significant)

0000 — Idle: CPU Inactive on Bus
0001 — Idle: WAIT Instruction
0010 — (Reserved)
0011 — Idle: Waiting for Slave
0100 — Interrupt Acknowledge, Master
0101 — Interrupt Acknowledge, Cascaded
0110 — End of Interrupt, Master
0111 — End of Interrupt, Cascaded
1000 — Sequential Instruction Fetch
1001 — Non-Sequential Instruction Fetch
1010 — Data Transfer
1011 — Read Read-Modify-Write Operand
1100 — Read for Effective Address
1101 — Transfer Slave Operand
1110 — Read Slave Status Word
1111 — Broadcast Slave ID and Operation Word

The $\overline{DDIN}$ line indicates the direction of the transfer: 0 = Read, 1 = Write.

$\overline{DDIN}$ is monitored by the MMU during CPU cycles to detect write operations, and is driven by the MMU during MMU-initiated bus cycles.

The U/$\overline{S}$ pin indicates the privilege level at which the CPU is making the access: 0 = Supervisor Mode, 1 = User Mode. It is used by the MMU to select the address space for translation and to perform protection level checking. Normally, the U/$\overline{S}$ pin is a direct reflection of the U bit in the CPU's Processor Status Register (PSR). The MOVUS and MOVSU CPU instructions, however, toggle this pin on successive operand accesses in order to move data between virtual spaces.

The MMU uses the $\overline{FLT}$ line to take control of the bus from the CPU. It does so as necessary for updating its internal TLB from the Page Tables in memory, and for maintaining the contents of the status bits (R and M) in the Page Table Entries.

The MMU also aborts invalid accesses attempted by the CPU. This is done by pulsing the $\overline{RST}/\overline{ABT}$ pin low for one clock period. (A pulse longer than one clock period is interpreted by the CPU as a Reset command.)

2.4.2 CPU-Initiated Bus Cycles

A CPU-initiated bus cycle is performed in a minimum of four clock cycles: T1, T2, T3 and T4, as shown in *Figure 2-6*.

During period T1, the CPU places the virtual address to be translated on the bus, and the MMU latches it internally and begins translation. The MMU also samples the $\overline{DDIN}$ pin, the status lines ST0–ST3, and the U/$\overline{S}$ pin in the previous T4 cycle to determine how the CPU intends to use the bus.

During period T2 the CPU removes the virtual address from the bus and the MMU takes one of three actions:

1) If the translation for the virtual address is resident in the MMU's TLB, and the access being attempted by the CPU does not violate the protection level of the page being referenced, the MMU presents the translated address on PA0–PA31 and generates a $\overline{PAV}$ pulse to trigger a bus cycle in the rest of the system. See *Figure 2-6*.

2) If the translation for the virtual address is resident in the MMU's TLB, but the access being attempted by the CPU is not allowed due to the protection level of the page being referenced, the MMU generates a pulse on the $\overline{RST}/\overline{ABT}$ pin to abort the CPU's access. No $\overline{PAV}$ pulse is generated. See *Figure 2-7*.

3) If the translation for the virtual address is not resident in the TLB, or if the CPU is writing to a page whose M bit is not yet set, the MMU takes control of the bus asserting the $\overline{FLT}$ signal as shown in *Figure 2-8*. This causes the CPU to float its bus and wait. The MMU then initiates a sequence of bus cycles as described in Section 2.4.3.

From state T2 through T4 data is transferred on the bus between the CPU and memory, and the TCU provides the strobes for the transfer.

Whenever the MMU generates an Abort pulse on the $\overline{RST}/\overline{ABT}$ pin, the CPU enters state T3 and then Ti (idle), ending the bus cycle. Since no $\overline{PAV}$ pulse is issued by the MMU, the rest of the system remains unaware that an access has been attempted.

2.0 Functional Description (Continued)

2.4.3 MMU-Initiated Cycles

Bus cycles initiated by the MMU are always nested within CPU-initiated bus cycles; that is, they appear after the MMU has accepted a virtual address from the CPU and has set the $\overline{FLT}$ line active. The MMU will initiate memory cycles in the following cases:

1) There is no translation in the MMU's TLB for the virtual address issued by the CPU, meaning that the MMU must reference the Page Tables in memory to obtain the translation.
2) There is a translation for that virtual address in the TLB, but the page is being written for the first time (the M bit in its Level-2 Page Table Entry is 0). The MMU treats this case as if there were no translation in the TLB, and performs a Page Table lookup in order to set the M bit in the Level-2 Page Table Entry as well as in the TLB.

Having made the necessary memory references, the MMU either aborts the CPU access or it provides the translated address and allows the CPU's access to continue to T3.

Figure 2-8 shows the sequence of events in a Page Table lookup. After asserting $\overline{FLT}$, the MMU waits for one additional clock cycle, then reads the Level-1 Page Table Entry and the Level-2 Page Table Entry in two consecutive memory Read cycles. There are no idle clock cycles between MMU-initiated bus cycles unless a bus request is made on the $\overline{HOLD}$ line (Section 2.6).

During the Page Table lookup the MMU drives the $\overline{DDIN}$ signal. The status lines ST0–ST3 and the U/$\overline{S}$ pin are not released by the CPU, and retain their original settings while the MMU uses the bus. The Byte Enable signals from the CPU, $\overline{BE0}$–$\overline{BE3}$, should be handled externally for correct memory referencing.

In the clock cycle immediately after T4 of the last lookup cycle, the MMU issues the translated address and pulses $\overline{MADS}$. In the subsequent cycle it removes $\overline{FLT}$ and pulses $\overline{PAV}$ to continue the CPU's access.

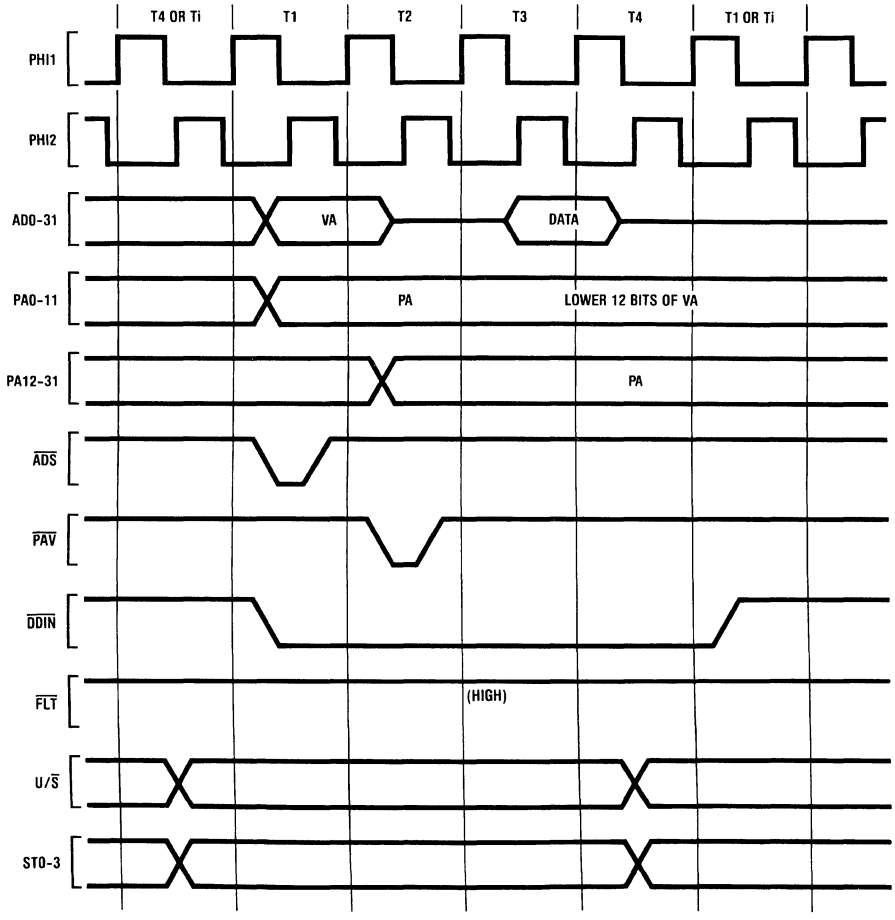

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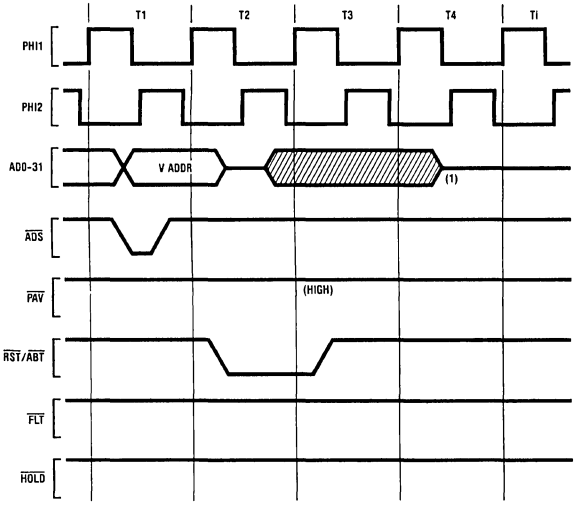
FIGURE 2-6. CPU Read Cycle; Translation in TLB (TLB Hit)

2.0 Functional Description (Continued)



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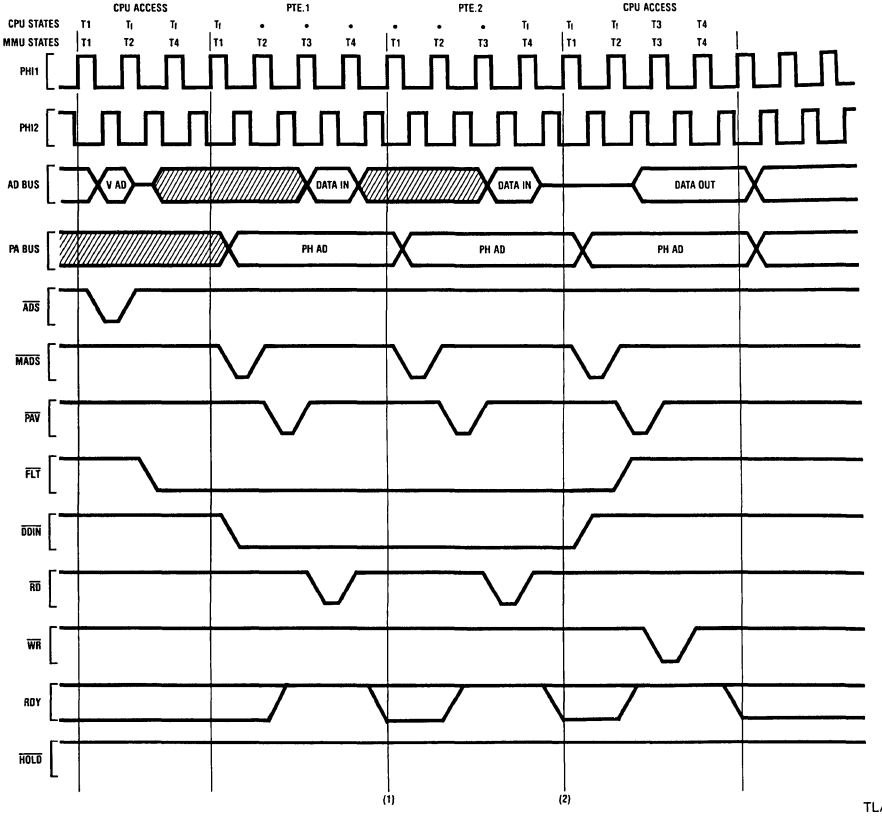
Note 1: The CPU drives the bus if a write cycle is aborted.

FIGURE 2-7. Abort Resulting from Protection Violation or a Breakpoint; Translation in TLB



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Note 1: If the R bit on the Level-1 PTE must be set, a write cycle is inserted here.

Note 2: If either the R or the M bit on the Level-2 PTE must be set, a write cycle is inserted here.

FIGURE 2-8. Page Table Lookup

2.0 Functional Description (Continued)

If the V bit (Bit 0) in any of the Page Table Entries is zero, or the protection level field PL (bits 1 and 2) indicates that the CPU's attempted access is illegal, the MMU does not generate any further memory cycles, but instead issues an Abort pulse during the clock cycle after T4 and removes the $\overline{FLT}$ signal.

If the R and/or M bit (bit 7 or 8) must be updated, the MMU does this immediately in a single Write cycle. All bits except those updated are rewritten with their original values.

At most, the MMU writes two double words to memory during a translation: the first to the Level-1 table to update the R bit, and the second to the Level-2 table to update the R and/or M bits.

2.4.4 Cycle Extension

To allow sufficient strobe widths and access time requirements for any speed of memory or peripheral device, the NS32382 provides for extension of a bus cycle. Any type of bus cycle, CPU-initiated or MMU-initiated, can be extended, except Slave Processor cycles, which are not memory or peripheral references.

In *Figures 2-6* and *2-8*, note that during T3 all bus control signals are flat. Therefore, a bus cycle can be cleanly extended by causing the T3 state to be repeated. This is the purpose of the RDY (Ready) pin.

In the middle of T3, on the falling edge of clock phase PHI1, the RDY line is sampled by the CPU and/or the MMU. If RDY is high, the next state after T3 will be T4, ending the bus cycle. If it is low, the next state after T3 will be another T3 and the RDY line will be sampled again. RDY is sampled in each following clock period, with insertion of additional T3 states, until it is sampled high. Each additional T3 state inserted is called a "WAIT state".

The RDY pin is driven by the NS32C201 Timing Control Unit, which applies WAIT states to the CPU and MMU as requested on its own WAIT request input pins.

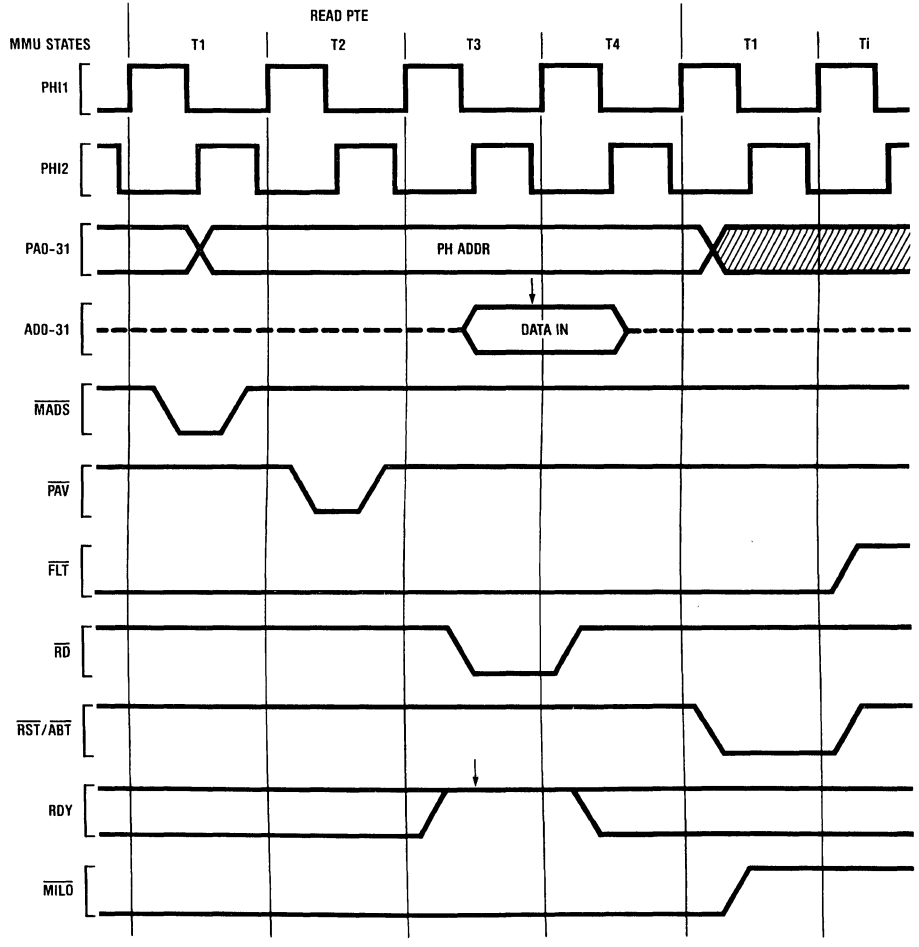

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FIGURE 2-9. Abort Resulting after a Page Table Lookup

2.0 Functional Description (Continued)

2.4.5 Bus Retry

The Bus Retry input signal ($\overline{BRT}$) provides a system with the capability of repeating a bus cycle upon the occurrence of a "soft" or correctable error. The system first determines that a correctable error has occurred and then activates the $\overline{BRT}$ input. The MMU then samples this input on the falling edge of PHI1 in both T3 and T4 of a bus cycle. A valid bus retry will be issued as a result of a low being sampled in both T3 and T4.

If the MMU gets a Bus Retry when it is controlling the bus, it will re-run the bus cycle until $\overline{BRT}$ is deactivated.

Any Pending Hold request will not be acknowledged by the MMU if a bus retry is detected and during Hold Acknowledge, the MMU will not recognize the Bus Retry signal.

2.4.6 Bus Error

The Bus Error input signal $\overline{BER}$ will be activated (low) when a "hard" or uncorrectable error occurs within the system (e.g. bus timeout, double ECC error). $\overline{BER}$ will be sampled on the falling edge of PHI1 in T4. If the MMU detects Bus Error while it is controlling the bus, it will store the virtual address which caused the error in the BEAR (Bus Error Address Register), and set the ME bit in the MSR to indicate MMU ERROR. An abort signal $\overline{ABT}$ will be generated and further memory accesses by the MMU will be inhibited. The 32382 then returns bus control to the CPU by releasing the $\overline{FLT}$ signal, ($\overline{FLT}$ = 1). Any pending Hold request will not be acknowledged by the MMU if a bus error is detected.

If the Bus Error signal is received when the CPU is controlling the bus, the MMU will store the virtual address in BEAR, and set the CE bit in the MSR to indicate CPU ERROR.

During the Hold Acknowledge, the MMU will ignore the $\overline{BER}$ signal.

2.4.7 Interlocked Bus Transfers

Both the 32332 CPU and the 32382 MMU are capable of executing interlocked cycles to access a stream of data from memory without intervention from other devices.

Before executing an interlocked access, the 32332 CPU performs a dummy read with Read-Modify-Write status (1011). The MMU handles the dummy read as if it were a real RMW access. The TLB entries will be searched and page table look-up will be performed if a miss occurs. The access level is checked and the CPU will be aborted if write privilege is not currently assigned. The Reference (R) and the Modify (M) bits in the first and second level PTEs, as well as those in the Translation look-aside Buffer, will be updated. By executing the dummy read, the CPU is assured of no MMU intervention when the actual interlocked access is performed.

The 32382 MMU executes interlocked Read-Modify-Write memory cycles to access Page Table Entries (PTEs) and update the Reference (R) and Modify (M) bit in the PTEs when necessary. If the R and/or M bit(s) do not require updating, the write portion of the RMW cycle will not be executed. The memory cycles to access PTEs during execution of RDVAL and WRVAL instructions are not interlocked since R and M bits are not updated.

During interlocked access cycles, the $\overline{MILO}$ signal from the MMU will be asserted. $\overline{MILO}$ has the same timing as $\overline{ILO}$ from the CPU. $\overline{MILO}$ is asserted in the clock cycle immediately before the Read-Modify-Write access and de-activated in the clock cycle following T4 of the write cycle.

The write portion of the Read-Modify-Write access will not be executed if any one of the following conditions occurs:

(1) A bus error has occurred in the read portion of the interlocked access.

(2) The R and/or M bit(s) in the PTE(s) do not require updating.

(3) A protection violation has occurred.

(4) An invalid PTE is detected.

If a bus retry is encountered in an interlocked access, $\overline{MILO}$ will continue to be asserted, and the access will be retried.

2.5 SLAVE PROCESSOR INTERFACE

The CPU and MMU execute four instructions cooperatively. These are LMR, SMR, RDVAL and WRVAL, as described in Section 2.5.2. The MMU takes the role of a Slave Processor in executing these instructions, accepting them as they are issued to it by the CPU. The CPU calculates all effective addresses and performs all operand transfers to and from memory and the MMU. The MMU does not take control of the bus except as necessary in normal operation; i.e., to translate and validate memory addresses as they are presented by the CPU.

The sequence of transfers ("protocol") followed by the CPU and MMU involves a special type of bus cycle performed by the CPU. This "Slave Processor" bus cycle does not involve the issuing of an address, but rather performs a fast data transfer whose purpose is pre-determined by the form of the instruction under execution and by status codes asserted by the CPU.

2.5.1 Slave Processor Bus Cycles

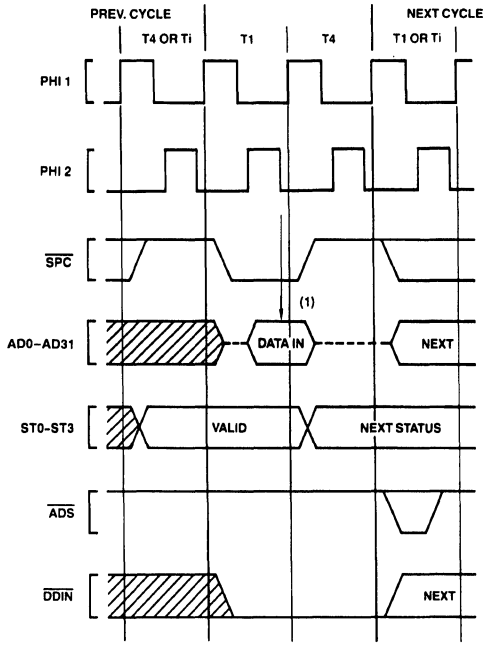
The interconnections between the CPU and MMU for Slave Processor communication are shown in *Figure A-1* (Appendix A). The $\overline{SPC}$ signal is pulsed by the CPU as a low-active data strobe for Slave Processor transfers. Since $\overline{SPC}$ is normally in a high-impedance state, it must be pulled high with a 10 kΩ resistor, as shown. The MMU also monitors the status lines ST0–ST3 to follow the protocol for the instruction being executed.

Data is transferred between the CPU and the MMU with Slave Processor bus cycles, illustrated in *Figures 2-10* and *2-11*. Each bus cycle transfers one double-word (32 bits) to or from the MMU.

Slave Processor bus cycles are performed by the CPU in two clock periods, which are labeled T1 and T4. During T1, the CPU activates $\overline{SPC}$ and, if it is writing to the MMU, it presents data on the bus. During T4, the CPU deactivates $\overline{SPC}$ and, if it is reading from the MMU, it latches data from the bus. The CPU guarantees that data written to the MMU is held through T4 to provide for the MMU's hold time requirements. The CPU also guarantees that the status code on ST0–ST3 becomes valid, at the latest, during the clock period preceding T1. The status code changes during T4 to anticipate the next bus cycle, if any.

Note that Slave Processor bus cycles are never extended with WAIT states. The RDY line is not sampled.

2.0 Functional Description (Continued)



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Note 1: CPU samples Data Bus here.

FIGURE 2-10. Slave Access Timing; CPU Reading from MMU

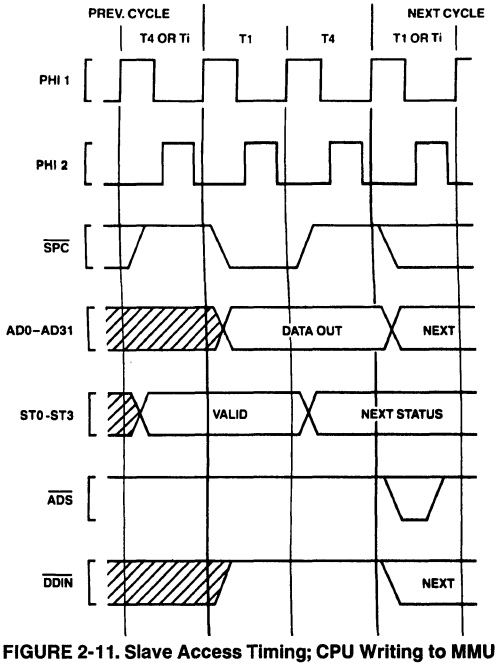

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FIGURE 2-11. Slave Access Timing; CPU Writing to MMU

2.0 Functional Description (Continued)

2.5.2 Instruction Protocols

MMU instructions have a three-byte Basic Instruction field consisting of an ID byte followed by an Operation Word. See *Figure 3-10* for the MMU instruction encodings. The ID Byte has three functions:

1) It identifies the instruction as being a Slave Processor instruction.
2) It specifies that the MMU will execute it.
3) It determines the format of the following Operation Word of the instruction.

The CPU initiates an MMU instruction by issuing the ID Byte and the Operation Word, using Slave Processor bus cycles. While applying status code IIII, the CPU transfers the ID byte on bits AD24–AD31, the operation word on bits AD8–AD23 in a swapped order of bytes and a non-used byte XXXXXXX1 (X = Don't Care) on bits AD0–AD7.

Other actions are taken by the CPU and the MMU according to the instruction under execution, as shown in Tables 2-2, 2-3 and 2-4.

In executing the LMR instruction (Load MMU Register, Table 2-2), the CPU issues the ID Byte, the Operation Word, and then the operand value to be loaded by the MMU. The register to be loaded is specified in a field within the Operation Word of the instruction.

The CPU then waits for the MMU to signal the completion of the instruction by pulsing $\overline{\text{SDONE}}$ low.

In executing the SMR instruction (Store MMU Register, Table 2-3), the CPU also issues the ID Byte and the Operation Word of the instruction to the MMU. It then waits for the MMU to signal (by pulsing $\overline{\text{SDONE}}$ low) that it is ready to present the specified register's contents to the CPU. Upon receiving this "Done" pulse, the CPU reads the contents of the selected register in one Slave Processor bus cycle, and places this result value into the instruction's destination (a CPU general-purpose register or a memory location).

In executing the RDVAL (Read-Validate) or WRVAL (Write-Validate) instruction, the CPU first performs the effective address calculation and obtains the address to be validated. It then issues the ID Byte and the Operation Word to the MMU. It initiates a one-byte Read cycle from the memory address whose protection level is being tested. It does so while presenting status code 1010; this being the only place that this status code appears during a RDVAL or WRVAL instruction. This memory access triggers a special address translation from the MMU. The translation is performed by the MMU using User-Mode mapping, and any protection violation occurring during this memory cycle does not cause an Abort. The MMU will, however, abort the CPU if the Level-1 Page Table Entry is invalid.

Upon completion of the address translation, the MMU pulses $\overline{\text{SDONE}}$ for two clock cycles to acknowledge that the instruction may continue execution and an MMU status read is required.

TABLE 2-2. LMR Instruction Protocol

CPU Action	Status	MMU Action
Issues ID Byte and Operation Word, pulsing $\overline{\text{SPC}}$.	1111	Accepts and decodes instruction.
Accesses memory for effective address calculation and operand fetching or instruction prefetching.	XXXX	Translates CPU addresses.
Issues operand value to MMU, pulsing $\overline{\text{SPC}}$.	1101	Accepts operand value from bus; places it into referenced MMU register.
Waits for $\overline{\text{SDONE}}$ pulse from MMU.	0011	Sends completion signal by pulsing $\overline{\text{SDONE}}$ low.

TABLE 2-3. SMR Instruction Protocol

CPU Action	Status	MMU Action
Issues ID Byte and Operation Word, pulsing $\overline{\text{SPC}}$.	1111	Accepts and decodes instruction.
Accesses memory for effective address calculation or instruction prefetching.	XXXX	Translates CPU addresses.
Waits for $\overline{\text{SDONE}}$ pulse from MMU.	0011	Sends completion signal by pulsing $\overline{\text{SDONE}}$ low.
Reads results from MMU, pulsing $\overline{\text{SPC}}$.	1101	Presents data value from referenced MMU register on bus.

TABLE 2-4. RDVAL/WRVAL Instruction Protocol

CPU Action	Status	MMU Action
Performs effective address calculation and obtains address to be validated.	XXXX	Translates CPU addresses.
Issues ID Byte and operation word, pulsing $\overline{\text{SPC}}$.	1111	Accepts and decodes instruction.
CPU may prefetch instructions.	XXXX	
Performs dummy one-byte memory read from operand's location.	1010	Translates CPU address, using User-Mode mapping, and performs requested test on the address presented by the CPU. Aborts the CPU if there is no protection violation and the level-1 page table entry is invalid. Aborts on protection violations are temporarily suppressed.
Waits for $\overline{\text{SDONE}}$ pulse from MMU	XXXX	Pulses $\overline{\text{SDONE}}$ low for two clock cycles.
Sends $\overline{\text{SPC}}$ pulse and reads Status Word from MMU; places bit 5 of this word into the F bit of the PSR register.	1110	Presents Status Word on bus, indicating in bit 5 the result of the test.

2.0 Functional Description (Continued)

The CPU then reads a status word from the MMU. Bit 5 of this Status Word indicates the result of the instruction:

0 if the CPU in User Mode could have made the corresponding access to the operand at the specified address (Read in RDVAL, Write in WRVAL),

1 if the CPU would have been aborted for a protection violation.

Bit 5 of the Status Word is placed by the CPU into the F bit of the PSR register, where it can be tested by subsequent instructions as a condition code.

2.6 BUS ACCESS CONTROL

The NS32382 MMU has the capability of relinquishing its access to the bus upon request from a DMA device. It does this by using $\overline{\text{HOLD}}$, $\overline{\text{HLDAI}}$ and $\overline{\text{HLDAO}}$.

Details on the interconnections of these pins are provided in *Figure A-1* (Appendix A).

Requests for DMA are presented in parallel to both the CPU and MMU on the $\overline{\text{HOLD}}$ pin of each. The component that currently controls the bus then activates its Hold Acknowledge output to grant bus access to the requesting device. When the CPU grants the bus, the MMU passes the CPU's $\overline{\text{HLDA}}$ signal to its own $\overline{\text{HLDAO}}$ pin. When the MMU grants the bus, it does so by activating its $\overline{\text{HLDAO}}$ pin directly, and the CPU is not involved. $\overline{\text{HLDAI}}$ in this case is ignored.

Refer to *Figures 4-15* and *4-16* for details on bus granting sequences.

2.7 BREAKPOINTING

The MMU provides the ability to monitor references to memory locations in real time, generating a Breakpoint trap on occurrence of any type of reference made by a program to a specified virtual address or range of addresses.

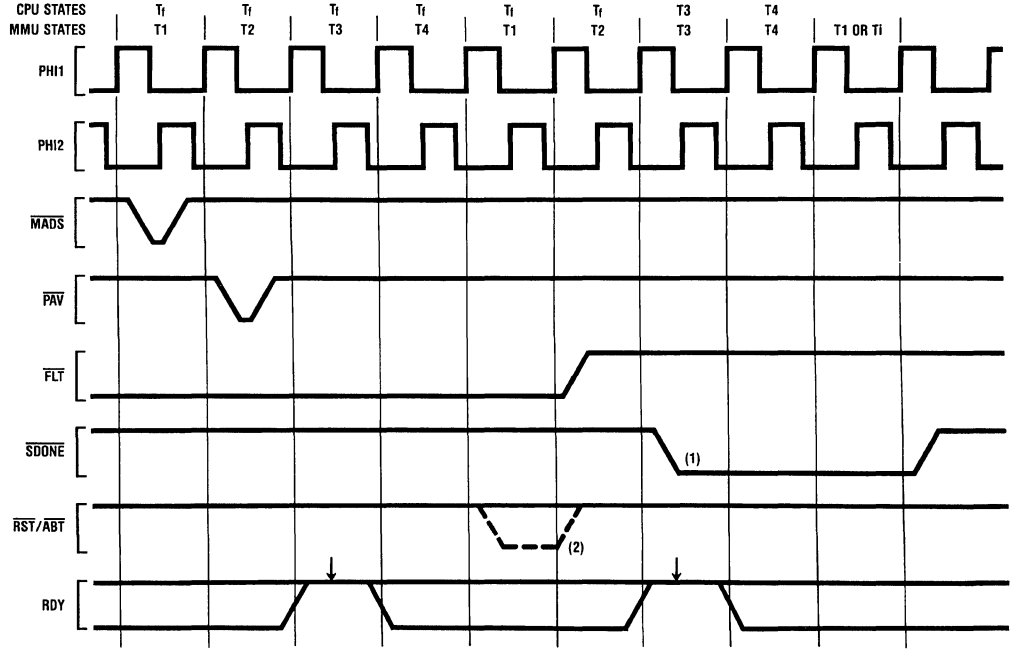
Breakpoint monitoring is enabled and regulated by the setting of appropriate bits in the BAR, BMR, BDR, MCR and MSR registers. See Sections 3.7 through 3.11.

The MMU compares the 32-bit address stored in the BAR register with the virtual address from the CPU. Selected bits can be masked off by the data pattern stored in the BMR register. Only those bit positions which are set in the BMR register will be used in the comparison process, bit positions which are cleared become "Don't Cares".

If a Breakpoint condition is detected, an abort will be issued to the CPU and the BP bit in the MSR register will be set. The virtual address that triggered the Breakpoint is then stored in the BDR register.

The dummy read addresses generated by the CPU during RDVAL/WRVAL operations, are not subject to Breakpoint address comparison. See Section 2.5.2.

When a Breakpoint is enabled, the NS32332 burst cycles should be inhibited by keeping the $\overline{\text{BIN}}$ signal high. The reason being that the CPU addresses are not incremented during burst. It is therefore possible for the CPU to skip over the address specified in the BAR register during burst cycle.



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Note 1: If there is a protection violation or an invalid Level-2 PTE then $\overline{\text{SDONE}}$ is issued two clock cycles earlier in T1.

Note 2: If there is no protection violation and the Level-1 PTE is not valid, an abort is generated and $\overline{\text{SDONE}}$ is not pulsed.

FIGURE 2-12. $\overline{\text{FLT}}$ Deassertion During RDVAL/WRVAL Execution

3.0 Architectural Description

3.1 PROGRAMMING MODEL

The MMU contains a set of registers through which the CPU controls and monitors management and debugging functions. These registers are not memory-mapped. They are examined and modified by executing the Slave Processor instructions LMR (Load Memory Management Register) and SMR (Store Memory Management Register). These instructions are explained in Section 3.14, along with the other Slave Processor instructions executed by the MMU.

A brief description of the MMU registers is provided below. Details on their formats and functions are provided in the following sections.

PTB0, PTB1—Page Table Base Registers. They hold the physical memory addresses of the LEVEL-1 Page Tables referenced by the MMU for address translation. See Section 3.3.

IVAR0, IVAR1—Invalidate Virtual Address Registers. These WRITE-ONLY registers are used to remove invalid Page Table Entries from the Translation Buffer.

TEAR—Translation Exception Address Registers. This register contains the virtual address which caused the translation exception.

BEAR—Bus Error Address Register. This register contains the virtual address which triggered the bus error.

BAR—Breakpoint Address Register. Used to hold a virtual address for breakpoint address comparison.

BMR—Breakpoint Mask Register. The contents of this register indicate which bit positions of the virtual address are to be compared.

BDR—Breakpoint Data Register. This register contains the virtual address that triggered a breakpoint.

MCR—Memory Management Control Register. Contains the control field for selecting the various features provided by the MMU.

MSR—Memory Management Status Register. Contains basic status fields for all MMU functions. See Section 3.11.

3.2 MEMORY MANAGEMENT FUNCTIONS

The NS32382 uses sets of tables in physical memory (the "Page Tables") to define the mapping from virtual to physical addresses. These tables are found by the MMU using one of its two Page Table Base registers: PTB0 or PTB1. Which register is used depends on the currently selected address space. See Section 3.2.2.

3.2.1. Page Tables Structure

The page tables are arranged in a two-level structure, as shown in *Figure 3-1*. Each of the MMU's PTBn registers may point to a Level-1 page table. Each entry of the Level-1 page table may in turn point to a Level-2 page table. Each Level-2 page table entry contains translation information for one page of the virtual space.

The Level-1 page table must remain in physical memory while the PTBn register contains its address and translation is enabled. Level-2 Page Tables need not reside in physical memory permanently, but may be swapped into physical memory on demand as is done with the pages of the virtual space.

The Level-1 Page Table contains 1024 32-bit Page Table Entries (PTE's) and therefore occupies 4 Kbyte. Each entry of the Level-1 Page Table contains fields used to construct the physical base address of a Level-2 Page Table. These fields are a 20-bit PFN field, providing bits 12-31 of the physical address. The remaining bits (0–11) are assumed zero, placing a Level-2 Page Table always on a 4 Kbyte (page) boundary.

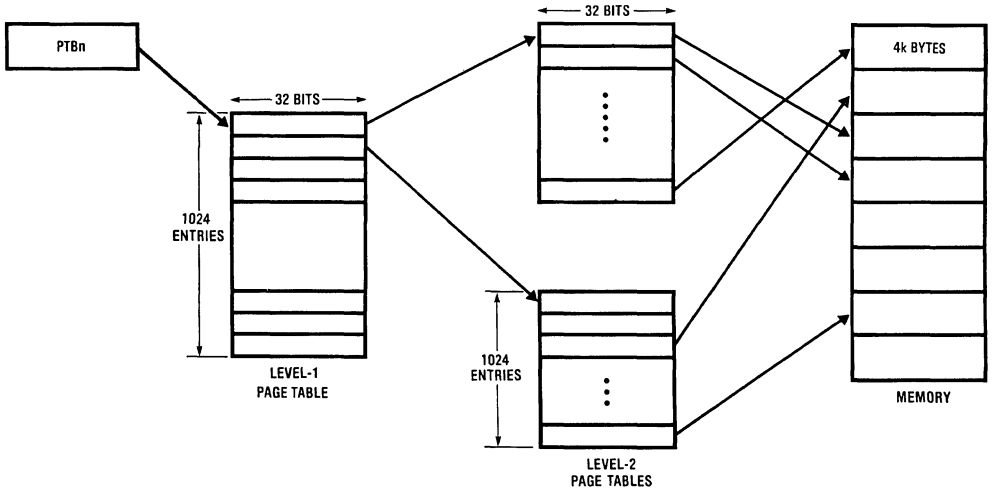

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FIGURE 3-1. Two-Level Page Tables

3.0 Architectural Description (Continued)

Level-2 Page Tables contain 1024 32-bit Page Table entries, and so occupy 4 Kbytes (1 page). Each Level-2 Page Table Entry points to a final 4 Kbyte physical page frame. In other words, its PFN provides the Page Frame Number portion (bits 12-31) of the translated address *(Figure 3-3)*. The OFFSET field of the translated address is taken directly from the corresponding field of the virtual address.

3.2.2 Virtual Address Spaces

When the Dual Space option is selected for address translation in the MCR (Sec. 3.10) the MMU uses two maps: one for translating addresses presented to it in Supervisor Mode and another for User Mode addresses. Each map is referenced by the MMU using one of the two Page Table Base registers: PTB0 or PTB1. The MMU determines the CPU's current mode by monitoring the state of the U/$\overline{S}$ pin and applying the following rules.

1) While the CPU is in Supervisor Mode (U/$\overline{S}$ pin = 0), the CPU is said to be presenting addresses belonging to Address Space 0, and the MMU uses the PTB0 register as its reference for looking up translations from memory.
2) While the CPU is in User Mode (U/$\overline{S}$ pin = 1), and the MCR DS bit is set to enable Dual Space translation, the CPU is said to be presenting addresses belonging to Address Space 1, and the MMU uses the PTB1 register to look up translations.
3) If Dual Space translation is not selected in the MCR, there is no Address Space 1, and all addresses presented in both Supervisor and User modes are considered by the MMU to be in Address Space 0. The privilege level of the CPU is used then only for access level checking.

Note: When the CPU executes a Dual-Space Move instruction (MOVUSi or MOVSUi), it temporarily enters User Mode by switching the state of the U/$\overline{S}$ pin. Accesses made by the CPU during this time are treated by the MMU as User-Mode accesses for both mapping and access level checking. It is possible, however, to force the MMU to assume Supervisor-Mode privilege on such accesses by setting the Access Override (AO) bit in the MCR (Sec. 3.10).

3.2.3 Page Table Entry Formats

Figure 3-2 shows the formats of Level-1 and Level-2 Page Table Entries (PTE's).

The bits are defined as follows:

V Valid. The V bit is set and cleared only by software.

V=1=> The PTE is valid and may be used for translation by the MMU.

V=0=> The PTE does not represent a valid translation. Any attempt to use this PTE will cause the MMU to generate an Abort trap.

PL Protection Level. This two-bit field establishes the types of accesses permitted for the page in both User Mode and Supervisor Mode, as shown in Table 3-1.

The PL field is modified only by software. In a Level-1 PTE, it limits the maximum access level allowed for all pages mapped through that PTE.

TABLE 3-1. Access Protection Levels

Mode	U/$\overline{S}$	Protection Level Bits (PL)			
		00	01	10	11
User	1	no access	no access	read only	full access
Supervisor	0	read only	full access	full access	full access

NU Not Used. These bits are reserved by National for future enhancements. Their values should be set to zero.

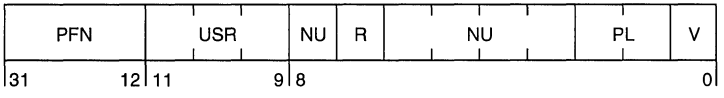
CI Cache Inhibit. This bit appears only in Level-2 PTE's. It is used to specify non-cacheable pages.

R Referenced. This is a status bit, set by the MMU and cleared by the operating system, that indicates whether the page mapped by this PTE has been referenced within a period of time determined by the operating system. It is intended to assist in implementing memory allocation strategies. In a Level-1 PTE, the R bit indicates only that the Level-2 Page Table has been referenced for a translation, without necessarily implying that the translation was successful. In a Level-2 PTE, it indicates that the page mapped by the PTE has been successfully referenced.

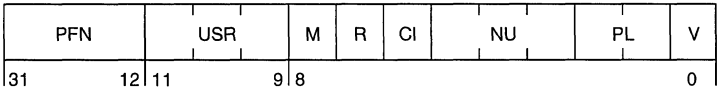
R=1=> The page has been referenced since the R bit was last cleared.

R=0=> The page has not been referenced since the R bit was last cleared.

M Modified. This is a status bit, set by the MMU whenever a write cycle is successfully performed to the page mapped by this PTE. It is initialized to zero by the operating system when the page is brought into physical memory.



First Level PTE



Second Level PTE

FIGURE 3-2. Page Table Entries (PTE's)

3.0 Architectural Description (Continued)

M=1=> The page has been modified since it was last brought into physical memory.

M=0=> The page has not been modified since it was last brought into physical memory.

In Level-1 Page Table Entries, this bit position is undefined, and is unaltered.

USR User bits. These bits are ignored by the MMU and their values are not changed.

They can be used by the user software.

PFN Page Frame Number. This 20-bit field provides bits 12-31 of the physical address. See *Figure 3-3.*

3.2.4 Physical Address Generation

When a virtual address is presented to the MMU by the CPU and the translation information is not in the TLB, the MMU performs a page table lookup in order to generate the physical address.

The Page Table structure is traversed by the MMU using fields taken from the virtual address. This sequence is diagrammed in *Figure 3-3.*

Bits 12–31 of the virtual address hold the 20-bit Page Number, which in the course of the translation is replaced with the 20-bit Page Frame Number of the physical address. The virtual Page Number field is further divided into two fields, INDEX 1 and INDEX 2.

Bits 0–11 constitute the OFFSET field, which identifies a byte's position within the accessed page. Since the byte position within a page does not change with translation, this value is not used, and is simply echoed by the MMU as bits 0–11 of the final physical address.

The 10-bit INDEX 1 field of the virtual address is used as an index into the Level-1 Page Table, selecting one of its 1024 entries. The address of the entry is computed by adding INDEX 1 (scaled by 4) to the contents of the current Page Table Base register. The PFN field of that entry gives the base address of the selected Level-2 Page Table.

The INDEX 2 field of the virtual address (10 bits) is used as the index into the Level-2 Page Table, by adding it (scaled by 4) to the base address taken from the Level-1 Page Table Entry. The PFN field of the selected entry provides the entire Page Frame Number of the translated address.

The offset field of the virtual address is then appended to this frame number to generate the final physical address.

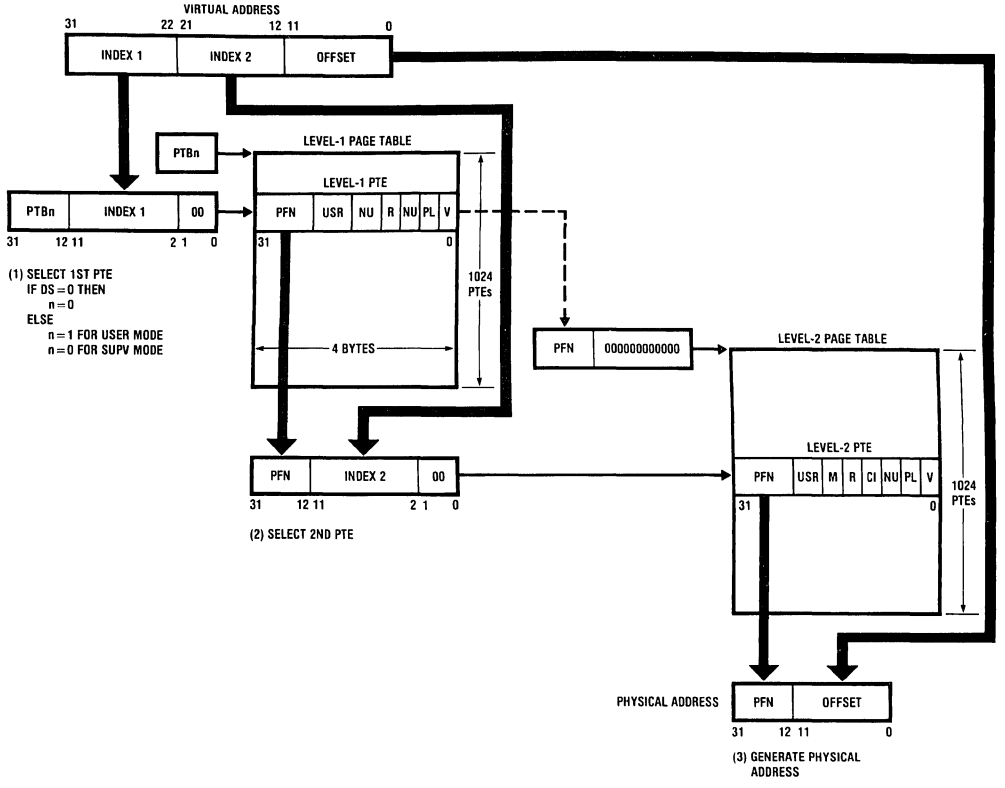


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FIGURE 3-3. Virtual to Physical Address Translation

3.0 Architectural Description (Continued)

3.3 PAGE TABLE BASE REGISTERS (PTB0, PTB1)

The PTBn registers hold the physical addresses of the Level-1 Page Tables.

The format of these registers is shown in *Figure 3-4.* The least-significant 12 bits are permanently zero, so that each register always points to a 4 Kbyte boundary in memory.

The PTBn registers may be loaded or stored using the MMU Slave Processor instructions LMR and SMR (Section 3.14).

3.4 INVALIDATE VIRTUAL ADDRESS REGISTERS (IVAR0, IVAR1)

The Invalidate Virtual Address registers are write-only registers. When a virtual address is written to IVAR0 or IVAR1 using the LMR instruction, the translation for that virtual address is purged, if present, from the TLB. This must be done whenever a Page Table Entry has been changed in memory, since the TLB might otherwise contain an incorrect translation value.

Another technique for purging TLB entries is to load a PTBn register. This automatically purges all entries associated with the addressing space mapped by that register. Turning off translation (clearing the MCR TU and/or TS bits) does not purge any entries from the TLB.

The format of the $IVAR_n$ registers is shown in *Figure 3-5.*

3.5 TRANSLATION EXCEPTION ADDRESS REGISTER (TEAR)

The TEAR Register is loaded when a translation exception occurs. It contains the 32-bit virtual address which caused the translation exception and is a read-only register. TEAR has the same format as the IVARn registers of *Figure 3-5.*

For more details on the updating of TEAR, refer to the note at the end of Section 3.11.

3.6 BUS ERROR ADDRESS REGISTER (BEAR)

The BEAR Register is loaded when a CPU or MMU bus error occurs. It contains the 32-bit virtual address which triggered the bus error and is a read-only register. BEAR has the same format as the IVARn registers of *Figure 3-5.*

3.7 BREAKPOINT ADDRESS REGISTER (BAR)

The Breakpoint Address Register is used to hold a virtual address for breakpoint address comparison during instruction and operand accesses. It is 32 bits in length and its format is shown in *Figure 3-6.*

3.8 BREAKPOINT MASK REGISTER (BMR)

The Breakpoint Mask Register provides corresponding bit positions for each of the virtual address bits that are to be compared when the Breakpoint Address Compare Function is enabled. Bits which are set in this register are used for matching virtual address bits while bits which are cleared are treated as "don't cares". This allows a breakpoint to be generated upon an access to any location within a block of addresses. The BMR Register format is shown in *Figure 3-6.*

3.9 BREAKPOINT DATA REGISTER (BDR)

The Breakpoint Data Register holds the virtual address that triggered the breakpoint.

It is a read-only register and its format is shown in *Figure 3-6.*

3.10 MEMORY MANAGEMENT CONTROL REGISTER (MCR)

The MCR Register controls the various features provided by the MMU. It is 32 bits in length and has the format shown in *Figure 3-7.* All bits will be cleared on reset. The bits 8 to 31 are RESERVED for future use and must be loaded with zeros.

When MCR is read as a 32-bit word, bits 8 to 31 will be returned as zeros. Details on the MCR bits are given below.

TU Translate User-Mode Addresses. While this bit is "1", the MMU translates all addresses presented while the CPU is in User Mode. While it is "0", the MMU echoes all User-Mode virtual addresses without performing translation or access level checking.

Note: Altering the TU bit has no effect on the contents of the TLB.

TS Translate Supervisor-Mode Addresses. While this bit is "1", the MMU translates all addresses presented while the CPU is in Supervisor Mode. While it is "0", the MMU echoes all Supervisor-Mode virtual addresses without translation or access level checking.

Note: Altering the TS bit has no effect on the contents of the TLB.

DS Dual-Space Translation. While this bit is "1", Supervisor Mode addresses and User Mode addresses are translated independently of each other, using separate mappings. While it is "0", both Supervisor Mode addresses and User Mode addresses are translated using the same mapping. See Section 3.2.2.

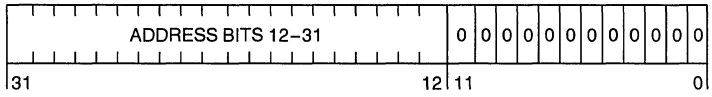

FIGURE 3-4. Page Table Base Registers (PTB0, PTB1)

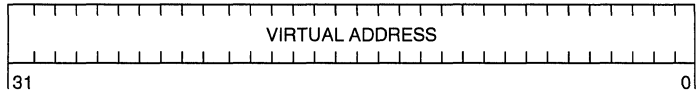

FIGURE 3-5. Address Registers (IVAR0, IVAR1, TEAR, BEAR)

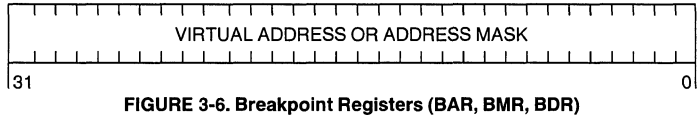

FIGURE 3-6. Breakpoint Registers (BAR, BMR, BDR)

3.0 Architectural Description (Continued)

AO Access Level Override. This bit may be set to temporarily cause User Mode accesses to be given Supervisor Mode privilege. See Section 3.13.

BR Break on Read. If BR is 1, a break is generated when data is read from the breakpoint address. Instruction fetches do not trigger a Read breakpoint. If BR is 0, this condition is disabled.

BW Break on Write. If BW is 1, a break is generated when data is written to the breakpoint address or when data is read from the breakpoint address as the first part of a read-modify-write access. If BW is 0, this condition is disabled.

BE Break on Execution. If BE is 1, a break is generated when the instruction at the breakpoint address is fetched. If BE is 0, this condition is disabled.

BAS Breakpoint Address Space. This bit selects the address space for breakpointing.

BAS = 0 Selects Address Space 0 (PTB0).

BAS = 1 Selects Address Space 1 (PTB1).

3.11 MEMORY MANAGEMENT STATUS REGISTER (MSR)

The Memory Management Status Register provides status information for translation exceptions as well as bus errors.

When either a translation exception or a bus error occurs, the corresponding bits in the MSR are updated.

The MSR register can be loaded with an LMR instruction. Its format is shown in *Figure 3-8*. Bits 19 through 31 are reserved for future use and are returned as zeros when read. Bits 8 and 18 are also reserved.

Upon reset, all MSR bits are cleared to zero. Details on the function of each bit are given below.

TEX Translation Exception. This 2-bit field specifies the cause of the current address translation exception. Combinations appearing in this field are summarized below.

00 No Translation Exception

01 First Level PTE Invalid

10 Second Level PTE Invalid

11 Protection Violation

Note: During address translation, if a protection violation and an invalid PTE are detected at the same time, the TEX field is set to indicate a protection violation.

DDT Data Direction. This bit indicates the direction of the transfer that the CPU was attempting when the translation exception occurred.

DDT = 0 = > Read Cycle

DDT = 1 = > Write Cycle

UST User/Supervisor. This is the state of the U/$\overline{S}$ pin from the CPU during the access cycle that triggered the translation exception.

STT CPU Status. This 4-bit field is set on an address translation exception to the value of the CPU Status Bus (ST0–ST3).

BP Break. This bit is set to indicate that a breakpoint condition has been detected by the MMU.

CE CPU Error. This bit is set when a bus error occurs while the CPU is in control of the bus.

ME MMU Error. This bit is set when a bus error occurs while the MMU is in control of the bus.

DDE Data Direction. This bit indicates the direction of the transfer that the CPU was attempting when the bus error occurred.

DDE = 0 = > Read Cycle

DDE = 1 = > Write Cycle

USE User/Supervisor. This is the state of the U/$\overline{S}$ pin from the CPU during the access cycle that triggered the bus error.

STE CPU Status. This 4-bit field is set to the value of the CPU status bus (ST0–ST3) when a bus error is detected.

Note: The MSR and TEAR registers are updated whenever a translation exception occurs, regardless of whether a CPU abort will result. As a consequence, after an abort is recognized, MSR and TEAR may be overwritten with new data and thus the original contents may be lost. This happens if the CPU, while executing the abort routine, performs instruction prefetch cycles from an invalid page. To ensure correct operation the reading of MSR and TEAR should be performed before any instruction prefetch crosses a page boundary, unless the next page is valid. This may place some restrictions in the relocation of the abort routine.

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FIGURE 3-7. Memory Management Control Register (MCR)

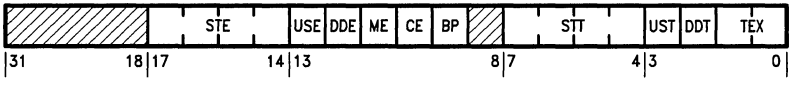

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FIGURE 3-8. Memory Management Status Register (MSR)

3.0 Architectural Description (Continued)

3.12 TRANSLATION LOOKASIDE BUFFER (TLB)

The Translation Lookaside Buffer is an on-chip fully associative memory. It provides direct virtual to physical mapping for the 32 most recently used pages, requiring only one clock period to perform the address translation.

The efficiency of the MMU is greatly increased by the TLB, which bypasses the much longer Page Table lookup in over 97% of the accesses made by the CPU.

Entries in the TLB are allocated and replaced by the MMU itself; the operating system is not involved. The TLB entries cannot be read or written by software; however, they can be purged from it under program control.

Figure 3-9 models the TLB. Information is placed into the TLB whenever the MMU performs a lookup from the Page Tables in memory. If the retrieved mapping is valid (V=1 in both levels of the Page Tables), and the access attempted is permitted by the protection level, an entry of the TLB is loaded from the information retrieved from memory. The recipient entry is selected by an on-chip circuit that implements a Least-Recently-Used (LRU) algorithm. The MMU places the virtual page number (20 bits) and the Address Space qualifier bit into the Tag field of the TLB entry.

The Value portion of the entry is loaded from the Page Tables as follows:

The Translation field (20 bits) is loaded from the PFN field of the Level-2 Page Table Entry.

The CI and M bits are loaded from the Level-2 Page Table Entry.

The PL field (2 bits) is loaded to reflect the net protection level imposed by the PL fields of the Level-1 and Level-2 Page Table Entries.

(Not shown in the figure are additional bits associated with each TLB entry which flag it as full or empty, and which select it as the recipient when a Page Table lookup is performed.)

When a virtual address is presented to the MMU for translation, the high-order 20 bits (page number) and the Address Space qualifier are compared associatively to the corresponding fields in all entries of the TLB. When the Tag portion of a TLB entry completely matches the input values, the Value portion is produced as output. If the protection level is not violated, and the M bit does not need to be changed, then the physical address Page Frame number is output in the next clock cycle. If the protection level is violated, the MMU instead activates the Abort output. If no TLB entry matches, or if the matching entry's M bit needs to be changed, the MMU performs a page-table lookup from memory.

Note that for a translation to be loaded into the TLB it is necessary that the Level-1 and Level-2 Page Table Entries be valid (V bit = 1). Also, it is guaranteed that in the process of loading a TLB entry (during a Page Table lookup) the Level-1 and Level-2 R bits will be set in memory if they were not already set. For these reasons, there is no need to replicate either the V bit or the R bit in the TLB entries.

Whenever a Page Table Entry in memory is altered by software, it is necessary to purge any matching entry from the TLB, otherwise the MMU would be translating the corresponding addresses according to obsolete information. TLB entries may be selectively purged by writing a virtual address to one of the IVARn registers using the LMR instruction. The TLB entry (if any) that matches that virtual address is then purged, and its space is made available for another translation. Purging is also performed by the MMU whenever an address space is remapped by altering the contents of the PTB0 or PTB1 register. When this is done, the MMU purges all the TLB entries corresponding to the address space mapped by that register. Turning translation on or off (via the MCR TU and TS bits) does not affect the contents of the TLB.

3.13 ADDRESS TRANSLATION ALGORITHM

The MMU either translates the 32-bit virtual address to a 32-bit physical address or reports a translation error. This process is described algorithmically in the following pages. See also *Figure 3-3*.

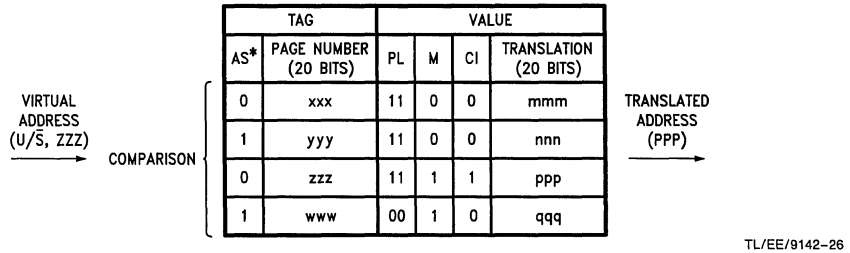

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FIGURE 3-9. TLB Model

*AS represents the virtual address space qualifier.

MMU Page Table Lookup and Access Validation Algorithm

```
Legend:
x = y           x is assigned the value y
x == y          Comparison expression, true if x is equal to y
x AND y         Boolean AND expression, true only if assertions x and y are both true
x OR y          Boolean inclusive OR expression, true if either of assertions x and y is true
;               Delimiter marking end of statement
{ . . . }       Delimiters enclosing a statement block
item(i)         Bit number i of structure "item"
item(i:j)       The field from bit number i through bit number j of structure "item"
item.x          The bit or field named "x" in structure "item"
DONE            Successful end of translation; MMU provides translated address
ABORT           Unsuccessful end of translation; MMU aborts CPU access
This algorithm represents for all cases a valid definition of address translation.
Bus activity implied here occurs only if the TLB does not contain the mapping,
or if the reference requires that the MMU alter the M bit of the Page Table Entry.
Otherwise, the MMU provides the translated address in one clock period.
Input (from CPU):
     U (1 if U/S is high)
     W (1 if DDIN input is high)
     VA  Virtual address consisting of:
        INDEX_1 (from pins A31-A22)
        INDEX_2 (from pins A21-A12)
        OFFSET  (from pins A11-A0)
     ACCESS_LEVEL       The access level of a reference is a 2-bit value synthesized by the MMU from CPU status:
        bit 1 = U AND NOT MCR.A0  (U from U/S input pin)
        bit 0 = 1 for Write cycle, or Read cycle of an "rmw" class operand access
                0 otherwise.

Output:
     PA Physical Address on pins PA0-PA31;
     CI Cache Inhibit Signal
     Abort pulse on RST/ABT pin.
Uses:
     MCR        Control Register:
                        fields TU, TS and DS
```

MMU Page Table Lookup and Access Validation Algorithm (Continued)

```
     PTB0       Page Table Base Register 0
     PTB1       Page Table Base Register 1
     PTE_1      Level-1 Page Table Entry:
                       fields PFN, PL, V and R
     PTEP_1     Pointer, holding address of PTE_1
     PTE_2      Level-2 Page Table Entry:
                       fields PFN, PL, V, M, R and CI
     PTEP_2     Pointer, holding address of PTE_2
IF ( (MCR.TU == 0) AND (U == 1) )  OR  ( (MCR.TS == 0) AND (U ==0) )  If translation not enabled then echo
     THEN  {  PA(0:31) = VA(0:31) ; CINH PIN = 0 ; DONE  }  ;              virtual address as physical address.
     ,

IF (MCR.DS == 1) AND (U == 1)                                        If Dual Space mode and CPU in User Mode
   THEN {  PTEP_1(31:12) = PTB1(31:12) ;                                  then form Level-1 PTE address
           PTEP_1(11:2) = VA.INDEX_1 ; PTEP_1(1:0)=0  }                         from PTB1 register,
   ELSE {  PTEP_1(31:12) = PTB0(31:12) ;                                  else form Level-1 PTE address
           PTEP_1(11:2) = VA.INDEX_1; PTEP_1(1:0) = 0                           from PTB0 register.
        } ;

                                          - - - LEVEL 1 PAGE TABLE LOOKUP - - -

IF ( ACCESS_LEVEL > PTE_1.PL ) OR (PTE_1.V == 0)                     If protection violation or invalid Level-2 page
   THEN ABORT ;                                                            table then abort the access.

IF PTE_1.R == 0 THEN PTE_1.R = 1 ;                                   Otherwise, set Reference bit if not already set,

PTEP_2(31:11) = PTE_1.PFN ;                                                    and form Level-2 PTE address.
PTEP_2(11:2) = VA.INDEX_2 ; PTEP_2(1:0) = 0 ;

                                          - - - LEVEL 2 PAGE TABLE LOOKUP - - -

IF ( ACCESS_LEVEL > PTE_2.PL ) OR ( PTE_2.V ==0 )                        If protection violation or invalid page
   THEN ABORT ;                                                          then abort the access.

IF PTE_2.R == 0 THEN PTE_2.R == 1 ;                                  Otherwise, set Referenced bit if not already set,
IF ( W == 1) AND ( PTE_2.M == 0 ) THEN PTE_2.M = 1 ;                     if Write cycle set Modified bit if not
                                                                               already set,
PA(31:11) = PTE_2.PFN ; PA(11:0) = VA.OFFSET ; CINH = PTE_2.CI ;                 and generate physical address.
DONE ;
```

3.0 Architectural Description (Continued)

3.14 INSTRUCTION SET

Four instructions of the Series 32000 instruction set are executed cooperatively by the CPU and MMU. These are:

LMR Load Memory Management Register
SMR Store Memory Management Register

RDVAL Validate Address for Reading
WRVAL Validate Address for Writing

The format of the MMU slave instructions is shown in *Figure 3-10*. Table 3-2 shows the encodings of the "short" field for selecting the various MMU internal registers.

TABLE 3-2. "Short" Field Encodings

"Short" Field	Register
0000	BAR
0001	RESERVED
0010	BMR
0011	BDR
0110	BEAR
1001	MCR
1010	MSR
1011	TEAR
1100	PTB0
1101	PTB1
1110	IVAR0
1111	IVAR1

Note: All other codes are illegal. They will cause unpredictable registers to be selected if used in an instruction.

For reasons of system security, all MMU instructions are privileged, and the CPU does not issue them to the MMU in User Mode. Any such attempt made by a User-Mode program generates the Illegal Operation trap, Trap (ILL). In addition, the CPU will not issue MMU instructions unless its CFG register's M bit has been set to validate the MMU instruction set. If this has not been done, MMU instructions are not recognized by the CPU, and an Undefined Instruction trap, Trap (UND), results.

The LMR and SMR instructions load and store MMU registers as 32-bit quantities to and from any general operand (including CPU General-Purpose Registers).

The RDVAL and WRVAL instructions probe a memory address and determine whether its current protection level would allow reading or writing, respectively, if the CPU were in User Mode. Instead of triggering an Abort trap, these instructions have the effect of setting the CPU PSR F bit if the type of access being tested for would be illegal. The PSR F bit can then be tested as a condition code.

Note: The Series 32000 Dual-Space Move instructions (MOVSUi and MOVUSi), although they involve memory management action, are not Slave Processor instructions. The CPU implements them by switching the state of its U/$\overline{S}$ pin at appropriate times to select the desired mapping and protection from the MMU.

For full architectural details of these instructions, see the Series 32000 Instruction Set Reference Manual.

4.0 Device Specifications

4.1 NS32382 PIN DESCRIPTIONS

The following is a brief description of all NS32382 pins. The descriptions reference portions of the Functional Description, Section 2.0.

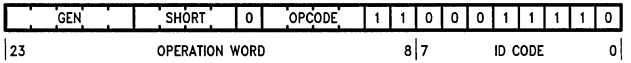

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FIGURE 3-10. MMU Slave Instruction Format

4.0 Device Specifications (Continued)

4.1.1 Supplies

Power (V_{CC}): Eight pins, connected to the +5V supply.

Back Bias Generator (BBG): Output of on-chip substrate voltage generator.

Ground (GND): Eighteen pins, connected to ground.

4.1.2 Input Signals

Clocks (PHI1, PHI2): Two-phase clocking signals. Section 2.2.

Ready (RDY): Active high. Used by slow memories to extend MMU originated memory cycles. Section 2.4.4.

Hold Request ($\overline{HOLD}$): Active low. Causes a release of the bus for DMA or multiprocessing purposes. Section 2.6.

Hold Acknowledge in ($\overline{HLDAI}$): Active low. Applied by the CPU in response to $\overline{HOLD}$ input, indicating that the CPU has released the bus for DMA or multiprocessing purposes. Section 2.6.

Reset Input ($\overline{RSTI}$): Active low. System reset. Section 2.3.

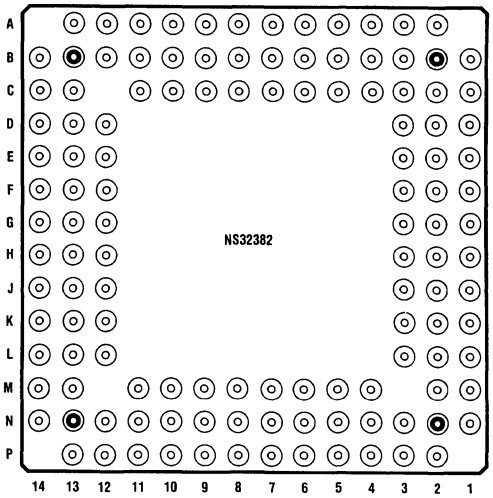
Status Lines (ST0–ST3): Status code input from the CPU. Active from T4 of previous bus cycle through T3 of current bus cycle. Section 2.4.

User/Supervisor Mode (U/$\overline{S}$): This signal is provided by the CPU. It is used by the MMU for protection and for selecting the address space (in dual address space mode only). Section 2.4.

Address Strobe Input ($\overline{ADS}$): Active low. Pulse indicating that a virtual address is present on the bus.

Bus Error ($\overline{BER}$): Active low. When active, indicates that an error occurred during a bus cycle. Not applicable for slave cycles.

Connection Diagram



Bottom View

FIGURE 4-1. Pin Grid Array Package

Order Number NS32382U-10 or NS32382U-15
See NS Package Number U125A

NS32382 Pinout Descriptions
125 Pin Grid Array

Desc	Pin	Desc	Pin	Desc	Pin	Desc	Pin
NC	A2	V_{CC}	C7	AD22	H1	PA4	M9
$\overline{SPC}$	A3	GND	C8	AD21	H2	PA7	M10
NC	A4	V_{CC}	C9	AD20	H3	GND	M11
$\overline{SDONE}$	A5	V_{CC}	C10	GND	H12	V_{CC}	M13
$\overline{MILO}$	A6	GND	C11	PA22	H13	PA13	M14
$\overline{HLDAI}$	A7	GND	C13	PA21	H14	NC	N1
$\overline{RSTI}$	A8	CINH	C14	AD19	J1	GND	N2
$\overline{BER}$	A9	AD29	D1	AD18	J2	GND	N3
$\overline{BRT}$	A10	AD31	D2	AD17	J3	AD9	N4
$\overline{RST/ABT}$	A11	GND	D3	PA20	J12	AD5	N5
ST0	A12	$\overline{ADS}$	D12	PA19	J13	AD2	N6
ST1	A13	RESERVED	D13	PA18	J14	AD0	N7
NC	B1	PA31	D14	AD14	K1	PA0	N8
NC	B2	AD27	E1	AD15	K2	PA3	N9
GND	B3	AD30	E2	AD16	K3	PA6	N10
GND	B4	U/$\overline{S}$	E3	GND	K12	PA9	N11
V_{CC}	B5	PA30	E12	PA17	K13	GND	N12
$\overline{HOLD}$	B6	PA29	E13	PA16	K14	NC	N13
RDY	B7	PA28	E14	AD13	L1	PA12	N14
PHI2	B8	AD25	F1	AD12	L2	AD11	P2
PHI1	B9	AD26	F2	V_{CC}	L3	AD10	P3
$\overline{PAV}$	B10	AD28	F3	V_{CC}	L12	AD8	P4
$\overline{FLT}$	B11	PA27	F12	PA14	L13	AD6	P5
ST2	B12	PA26	F13	PA15	L14	AD4	P6
ST3	B13	PA25	F14	NC	MI	AD1	P7
RESERVED	B14	AD23	G1	GND	M2	PA1	P8
NC	C1	AD24	G2	GND	M4	PA2	P9
$\overline{MADS}$	C2	GND	G3	AD7	M5	PA5	P10
GND	C3	GND	G12	AD3	M6	PA8	P11
GND	C4	PA24	G13	V_{CC}	M7	PA10	P12
$\overline{DDIN}$	C5	PA23	G14	BBG	M8	PA11	P13
$\overline{HLDAO}$	C6						

4.0 Device Specifications (Continued)

Bus Retry ($\overline{BRT}$): Active low. When active, the MMU will re-execute the last bus cycle. Not applicable for slave cycles.

Slave Processor Control ($\overline{SPC}$): Active low. Used as a data strobe for slave processor transfers.

4.1.3 Output Signals

Reset Output/Abort ($\overline{RST}/\overline{ABT}$): Active Low. Held active longer than one clock cycle to reset the CPU. Pulsed low during T2 to abort the current CPU instruction.

Float Output ($\overline{FLT}$): Active low. Floats the CPU from the bus when the MMU accesses page table entries. Section 2.4.3.

Physical Address Valid ($\overline{PAV}$): Active low. Pulse generated during T2 indicating that a physical address is present on the bus.

Hold Acknowledge Output ($\overline{HLDAO}$): Active low. When active, indicates that the bus has been released.

Cache Inhibit (CINH): This output signal reflects the state of the CI bit in the second level Page Table Entry (PTE). It is used to specify non-cacheable pages. During MMU generated bus cycles and when the MMU is in No-Translation mode, CINH will be held low.

Slave Done ($\overline{SDONE}$): Active low. Used by the MMU to inform the CPU of the completion of a slave instruction. It floats when it is not active.

MMU Address Strobe ($\overline{MADS}$): Active low. This signal is asserted in T1 of an MMU initiated cycle. It indicates that the physical address is available on the physical address bus. $\overline{MADS}$ is floated during hold acknowledge.

MMU Interlock ($\overline{MILO}$): Active low. This signal is asserted by the MMU when it performs a read-modify-write operation to up-date the R and/or the M bit in the Page Table Entry (PTE). It is inactive during Hold Acknowledge.

Physical Address Bus (PA0–PA31): These 32 signal lines carry the physical address. They float during Hold Acknowledge.

4.1.4 Input-Output Signals

Data Direction In ($\overline{DDIN}$): Active low. Status signal indicating direction of data transfer during a bus cycle. Driven by the MMU during a page-table lookup.

Address/Data 0–31 (AD0–AD31): Multiplexed Address/Data Information. Bit 0 is the least significant bit.

4.2 ABSOLUTE MAXIMUM RATINGS

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Temperature Under Bias	0°C to +70°C
Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to GND	−0.5V to +7V
Power Dissipation	2.5W

Note: *Absolute maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended; operation should be limited to those conditions specified under Electrical Characteristics.*

4.3 ELECTRICAL CHARACTERISTICS $T_A = 0$ to $+70°C$, $V_{CC} = 5V \pm 5\%$, GND = 0V

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High Level Input Voltage		2.0		$V_{CC} + 0.5$	V
V_{IL}	Low Level Input Voltage		−0.5		0.8	V
V_{CH}	High Level Clock Voltage	PHI1, PHI2 Pins Only	$V_{CC} - 0.5$		$V_{CC} + 0.5$	V
V_{CL}	Low Level Clock Voltage	PHI1, PHI2 Pins Only	−0.5		0.3	V
V_{CRT}	Clock Input Ringing Tolerance	PHI1, PHI2 Pins Only	−0.5		0.5	V
V_{OH}	High Level Output Voltage	$I_{OH} = -400\ \mu A$	2.4			V
V_{OL}	Low Level Output Voltage	$I_{OL} = 2$ mA			0.45	V
I_{ILS}	$\overline{SPC}$ Input Current (Low)	$V_{IN} = 0.4V$, $\overline{SPC}$ in Input Mode	0.05		1.0	mA
I_I	Input Load Current	$0 \le V_{IN} \le V_{CC}$, All Inputs Except PHI1, PHI2, $\overline{AT}/\overline{SPC}$	−20		20	μA
I_L	Leakage Current (Output and I/O Pins in TRI-STATE/Input Mode)	$0.4 \le V_{OUT} \le V_{CC}$	−20		20	μA
I_{CC}	Active Supply Current	$I_{OUT} = 0$, $T_A = 25°C$		350	500	mA

4.0 Device Specifications (Continued)

4.4 SWITCHING CHARACTERISTICS

4.4.1 Definitions

All the timing specifications given in this section refer to 2.0V on the rising or falling edges of the clock phases PHI1 and PHI2, and 0.8V or 2.0V on all other signals as illustrated in *Figures 4-2* and *4-3*, unless specifically stated otherwise.

ABBREVIATIONS:

L.E. — leading edge R.E. — rising edge
T.E. — trailing edge F.E. — falling edge

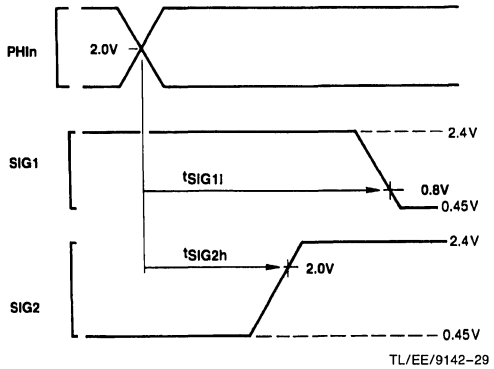


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FIGURE 4-2. Timing Specification Standard (Signal Valid after Clock Edge)

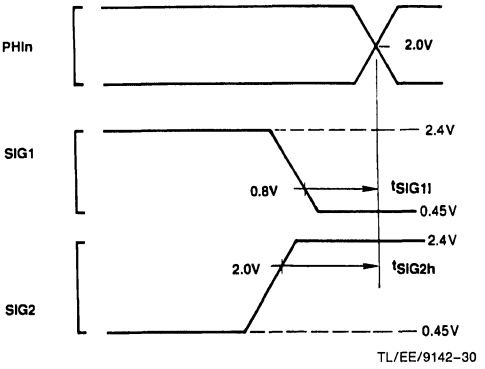

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FIGURE 4-3. Timing Specification Standard (Signal Valid before Clock Edge)

4.4.2 Timing Tables

4.4.2.1 Output Signals: Internal Propagation Delays, NS32382-10, NS32382-15.
Maximum times assume capacitive loading of 50 pF.

Name	Figure	Description	Reference/Conditions	NS32382-10		NS32382-15		Units
				Min	Max	Min	Max	
t_{PALv}	4–4	PA0–11 Valid ($\overline{FLT}$ = 1)	After R.E., PHI1 T1		75		50	ns
t_{PAHv}	4–4	PA12–31 Valid ($\overline{FLT}$ = 1)	After R.E., PHI1 T2		30		20	ns
t_{PAVa}	4–4	$\overline{PAV}$ Signal Active	After R.E., PHI1 T2		25		17	ns
t_{PAVia}	4–4	$\overline{PAV}$ Signal Inactive	After R.E., PHI2 T2		40		27	ns
t_{PAVw}	4–4	$\overline{PAV}$ Pulse Width	At 0.8V (Both Edges)	35		22		ns
t_{PALh}	4–4	PA0–11 Hold ($\overline{FLT}$ = 1)	After R.E., PHI1 (Next) T1	0		0		ns
t_{PAHh}	4–4	PA12–31 Hold ($\overline{FLT}$ = 1)	After R.E., PHI1 (Next) T2	0		0		ns
t_{CIv}	4–4, 4–15,	CINH Signal Valid ($\overline{FLT}$ = 1) ($\overline{FLT}$ = 0)	After R.E., PHI1 T2 After R.E., PHI1 T1		40		27	ns
t_{CIh}	4–4	CINH Signal Hold ($\overline{FLT}$ = 1)	After R.E., PHI1 (Next) T2	0		0		
t_{DDINv}	4–5, 4–7, 4–15	$\overline{DDIN}$ Signal Valid ($\overline{FLT}$ = 0)	After R.E., PHI1 T1		35		25	ns
t_{DDINh}	4–5	$\overline{DDIN}$ Signal Hold ($\overline{FLT}$ = 0)	After R.E., PHI1 (Next) T1	0		0		ns
t_{Dv}	4–6	AD0–AD31 Valid (Memory Write)	After R.E., PHI1 T2		50		38	ns
t_{Dh}	4–6	AD0–AD31 Hold (Memory Write)	After R.E., PHI1 (Next) T1	0		0		ns
t_{MAv}	4–6	PA0–31 Valid ($\overline{FLT}$ = 0)	After R.E., PHI1 T1		30		20	ns
t_{MAh}	4–6	PA0–31 Hold ($\overline{FLT}$ = 0)	After R.E., PHI1 (Next) T1	0		0		ns

4.0 Device Specifications (Continued)

4.4.2.1 Output Signals: Internal Propagation Delays, NS32382-10, NS32382-15.
Maximum times assume capacitive loading of 50 pF. (Continued)

Name	Figure	Description	Reference/Conditions	NS32382-10		NS32382-15		Units
				Min	Max	Min	Max	
t_{MADSa}	4–6, 15	$\overline{MADS}$ Signal Active ($\overline{FLT}$ = 0)	After R.E., PHI1 T1		25		17	ns
t_{MADSia}	4–6	$\overline{MADS}$ Signal Inactive	After R.E., PHI2 T1	5	35	5	25	ns
t_{MADSw}	4–6	$\overline{MADS}$ Pulse Width	At 0.8V (Both Edges)	35		22		ns
t_{DDINf}	4–7, 4–9, 11	$\overline{DDIN}$ Floating	After R.E., PHI1 T3 After R.E., PHI1 T1		25		25	ns
t_{MILOa}	4–5, 4–15	$\overline{MILO}$ Signal Active	After R.E., PHI1 T4		50		38	
t_{MILOia}	4–7, 4–15	$\overline{MILO}$ Signal Inactive	After R.E., PHI1 T1 or Ti		50		38	ns
t_{ABTa}	4–8	$\overline{RST}/\overline{ABT}$ Signal Active (Abort)	After R.E., PHI1 T1 or T2		50		40	ns
t_{ABTia}	4–8	$\overline{RST}/\overline{ABT}$ Signal Inactive (Abort)	After R.E., PHI1 T2 or T3	2	50	2	40	ns
t_{ABTw}	4–8	$\overline{RST}/\overline{ABT}$ Pulse Width (Abort)	At 0.8V (Both Edges)	60		40		ns
t_{FLTa}	4–5	$\overline{FLT}$ Signal Active	After R.E., PHI1 T2		50		40	ns
t_{FLTia}	4–7, 4–9	$\overline{FLT}$ Signal Inactive	After R.E., PHI1 T2		40		30	ns
t_{Df}	4–12	Data Bits Floating (Slave Processor Read)	After R.E., PHI1 T4		25		18	
t_{Dv}	4–12	AD0–AD31 Valid (CPU Slave Read)	After R.E., PHI1 T1		50		38	ns
t_{Dh}	4–12	AD0–AD31 Hold (CPU Slave Read)	After R.E., PHI1 T4	4		3		ns
t_{SDNa}	4–14	$\overline{SDONE}$ Signal Active	After R.E., PHI2		50		35	ns
t_{SDNia}	4–14	$\overline{SDONE}$ Signal Inactive	Ater R.E., PHI1		50		35	ns
t_{SDNw}	4–14	$\overline{SDONE}$ Pulse Width	At 0.8V (Both Edges)	25	90	17	60	ns
t_{SDNdw}	4–14	$\overline{SDONE}$ Double Pulse Width	At 0.8V (Both Edges)	225	275	140	180	ns
t_{SDNf}	4–14	$\overline{SDONE}$ Signal Floating	After R.E., PHI2		40		25	ns
t_{HLDAOa}	4–15	$\overline{HLDAO}$ Signal Active ($\overline{FLT}$ = 0)	After R.E., PHI1 Ti		60		40	ns
$t_{HLDAOia}$	4–15	$\overline{HLDAO}$ Signal Inactive ($\overline{FLT}$ = 0)	After R.E., PHI1 T4		60		40	ns
t_{MADSz}	4–15	$\overline{MADS}$ Signal Floated by $\overline{HOLD}$	After R.E., PHI1 Ti		40		25	ns
t_{PAVz}	4–15	$\overline{PAV}$ Signal Floated by $\overline{HOLD}$	After R.E., PHI1 Ti		40		25	ns
t_{PAVr}	4–15	$\overline{PAV}$ Return from Floating (Caused by $\overline{HOLD}$)	After R.E., PHI1 T1		40		25	ns
t_{Dz}	4–15	AD0–AD31 Floating (Caused by $\overline{HOLD}$)	After R.E., PHI1 Ti		25		18	ns
t_{MAz}	4–15	PA0–31 Floated by $\overline{HOLD}$	After R.E., PHI1 Ti		25		18	ns
t_{DDINz}	4–15	$\overline{DDIN}$ Signal Floated by $\overline{HOLD}$	After R.E., PHI1 Ti		40		25	ns
t_{CIz}	4–15	CINH Signal Floated by $\overline{HOLD}$	After R.E., PHI1 Ti		25		18	ns
t_{MILOia}	4–15	$\overline{MILO}$ Signal Inactive by $\overline{HOLD}$ ($\overline{FLT}$ = 0)	After R.E., PHI1 Ti		50		38	ns

4.0 Device Specifications (Continued)

4.4.2.1 Output Signals: Internal Propagation Delays, NS32382-10, NS32382-15.
Maximum times assume capacitive loading of 50 pF. (Continued)

Name	Figure	Description	Reference/Conditions	NS32382-10		NS32382-15		Units
				Min	Max	Min	Max	
t_{MILOa}	4–15	$\overline{MILO}$ Signal Active ($\overline{FLT}$ = 0)	After R.E., PHI1 T4		50		38	ns
t_{HLDAOa}	4–16	$\overline{HLDAO}$ Signal Active ($\overline{FLT}$ = 1)	After R.E., PHI1 Ti		45		30	ns
$t_{HLDAOia}$	4–16	$\overline{HLDAO}$ Signal Inactive ($\overline{FLT}$ = 1)	After R.E., PHI1 Ti or T4		45		30	ns
t_{MADSz}	4–16	$\overline{MADS}$ Signal Floated by $\overline{HLDAI}$ ($\overline{FLT}$ = 1)	After R.E., PHI1 Ti		25		18	ns
t_{MADSr}	4–16	$\overline{MADS}$ Return from Floating ($\overline{FLT}$ = 1)	After R.E., PHI1 Ti or T4		30		20	ns
t_{PAVz}	4–16	$\overline{PAV}$ Signal Floated $\overline{HLDAI}$ ($\overline{FLT}$ = 1)	After R.E., PHI1 Ti		25		18	ns
t_{PAVr}	4–16	$\overline{PAV}$ Return from Floating ($\overline{FLT}$ = 1)	After R.E., PHI1 Ti or T4		30		20	ns
t_{Dz}	4–16	AD0–AD31 Signals Floating ($\overline{FLT}$ = 1)	After R.E., PHI1 Ti		25		18	ns
t_{Dr}	4–16	AD0–AD31 Return from Floating ($\overline{FLT}$ = 1)	After R.E., PHI1 Ti or T4		30		20	ns
t_{MAz}	4–16	PA0–31 Signals Floated by $\overline{HLDAI}$ ($\overline{FLT}$ = 1)	After R.E., PHI1 T1		25		18	ns
t_{MAr}	4–16	PA0–31 Return from Floating ($\overline{FLT}$ = 1)	After R.E., PHI1 Ti or T4		30		20	ns
t_{Clz}	4–16	CINH Signal Floated by $\overline{HLDAI}$ ($\overline{FLT}$ = 1)	After R.E., PHI1 Ti		25		18	ns
t_{Clr}	4–16	CINH Return from Floating ($\overline{FLT}$ = 1)	After R.E., PHI1 Ti or T4		30		20	ns
t_{RSTOa}	4–18	$\overline{RST}/\overline{ABT}$ Signal Active (Reset)	After R.E., PHI2 Ti		50		40	ns
t_{RSTOia}	4–18	$\overline{RST}/\overline{ABT}$ Signal Inactive (Reset)	After R.E. PHI2 Ti		50		40	ns
t_{RSTOw}	4–18	$\overline{RST}/\overline{ABT}$ Pulse Width (Reset)	At 0.8V (Both Edges)	64		64		t_{cp}

4.4.2.2 Input Signal Requirements: NS32382-10, NS32382-15

Name	Figure	Description	Reference/Conditions	NS32382-10		NS32382-15		Units
				Min	Max	Min	Max	
t_{DIs}	4–5	Input Data Setup ($\overline{FLT}$ = 0)	Before F.E., PHI2 T3	12		10		ns
t_{DIh}	4–5	Input Data Hold ($\overline{FLT}$ = 0)	After R.E., PHI1 T4	3		3		ns
t_{RDYs}	4–5	RDY Setup	Before F.E., PHI1 T3	20		12		ns
t_{RDYh}	4–5	RDY Hold	After R.E., PHI2 T3	4		3		ns
t_{SPCs}	4-12	$\overline{SPC}$ Input Setup	Before F.E., PHI2 T1	45		35		ns
t_{SPCh}	4-12	$\overline{SPC}$ Input Hold	After R.E., PHI1 T4	0		0		ns
t_{USs}	4–4, 4-12	U/$\overline{S}$ Setup	Before F.E., PHI2 T4	25		20		ns
t_{USh}	4–4, 4–12	U/$\overline{S}$ Hold	After R.E., PHI1 (Next) T4	0		0		ns
t_{STs}	4–4, 4–12	ST0–3 Setup	Before F.E., PHI2 T4	40		25		ns
t_{STh}	4–4, 4–12	ST0–3 Hold	After R.E., PHI1 (Next) T4	0		0		ns
t_{DIs}	4–13	Data In Setup (Slave Processor Write)	Before F.E., PHI2 T1	40		22		ns

4.0 Device Specifications (Continued)

4.4.2.2 Input Signal Requirements: NS32382-10, NS32382-15 (Continued)

Name	Figure	Description	Reference/Conditions	NS32382-10		NS32382-15		Units
				Min	Max	Min	Max	
t_{DIh}	4–13	Data In Hold (Slave Processor Write)	After R.E., PHI1 (Next) Ti	3		3		ns
t_{HOLDs}	4-15	$\overline{HOLD}$ Setup ($\overline{FLT}$ = 0)	Before F.E., PHI2 T3	15		15		ns
t_{HOLDh}	4-15	$\overline{HOLD}$ Hold ($\overline{FLT}$ = 0)	After R.E., PHI1 T4	0		0		ns
t_{HLDAis}	4-16	$\overline{HLDAI}$ Signal Setup ($\overline{FLT}$ = 1)	Before F.E., PHI2 Ti	25		15		ns
t_{HLDAih}	4-16	$\overline{HLDAI}$ Signal Hold ($\overline{FLT}$ = 1)	After R.E., PHI1 Ti or T4	0		0		ns
t_{BRTs}	4-10	$\overline{BRT}$ Signal Setup ($\overline{FLT}$ = 0)	Before F.E., PHI1 T3 or T4	25		14		ns
t_{BRTh}	4-10	$\overline{BRT}$ Signal Hold ($\overline{FLT}$ = 0)	After R.E., PHI2 T3 or T4	0		0		ns
t_{BERs}	4-11	$\overline{BER}$ Signal Setup ($\overline{FLT}$ = 0)	Before F.E., PHI1 T4	25		14		ns
t_{BERh}	4-11	$\overline{BER}$ Signal Hold ($\overline{FLT}$ = 0)	After R.E., PHI2 T4	0		0		ns
t_{RSTIs}	4-18	Reset Input Setup	Before F.E., PHI1 Ti	20		10		ns
t_{RSTIw}	4–18	Reset Input Width	At 0.8V (Both Edges)	64		64		t_{cp}

4.4.2.3 Clocking Requirements: NS32382-10, NS32382-15

Name	Figure	Description	Reference/ Conditions	NS32382-10		NS32382-15		Units
				Min	Max	Min	Max	
t_{Cp}	4–17	Clock Period	R.E., PHI1, PHI2 to Next R.E., PHI1, PHI2	100	250	66	250	ns
$t_{CLw(1,2)}$	4–17	PHI1, PHI2 Pulse Width	At 2.0V on PHI1, PHI2 (Both Edges)	0.5 t_{cp} −10 ns		0.5 t_{cp} −6 ns		
$t_{CLh(1,2)}$	4–17	PHI1, PHI2 High Time	At V_{CC} − 0.9V on PHI1, PHI2 (Both Edges)	0.5 t_{cp} −15 ns		0.5 t_{cp} −10 ns		
t_{CLl}	4–17	PHI1, PHI2 Low Time	At 0.8V on PHI1, PHI2 (Both Edges)	0.5 t_{Cp} −5 ns		0.5 t_{Cp} −5 ns		
$t_{nOVL(1,2)}$	4–17	Non-Overlap Time	0.8V on F.E., PHI1, PHI2 to 0.8V on R.E., PHI2, PHI1	−2	5	−2	5	ns
t_{nOVLas}		Non-Overlap Asymmetry ($t_{nOVL(1)} - t_{nOVL(2)}$)	At 0.8V on PHI1, PHI2	−4	4	−3	3	ns
t_{CLhas}		PHI1, PHI2 Asymmetry $t_{CLh(1)} - t_{CLh(2)}$)	At V_{CC} − 0.9V on PHI1, PHI2	−5	5	−3	3	ns

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4.0 Device Specifications (Continued)

4.4.3 Timing Diagrams

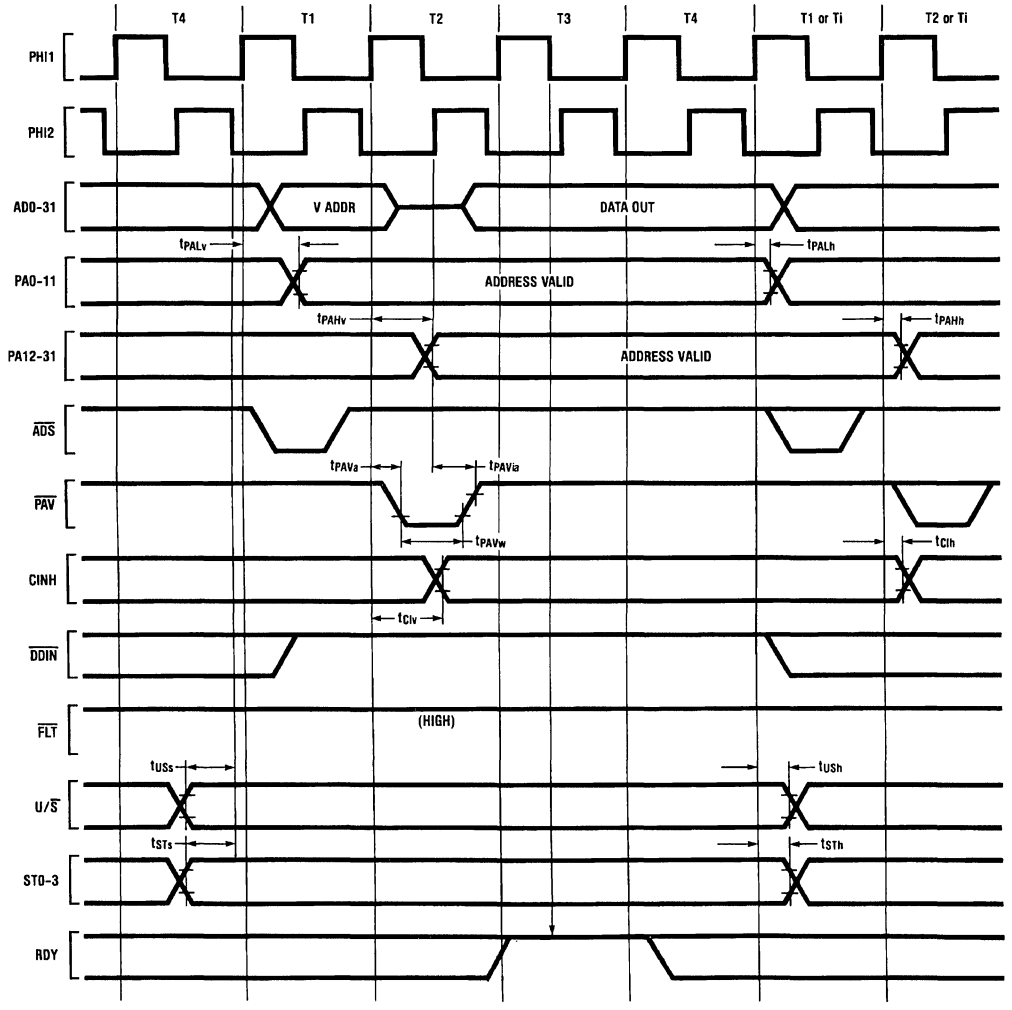

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FIGURE 4-4. CPU Write Cycle Timing; Translation in TLB

4.0 Device Specifications (Continued)

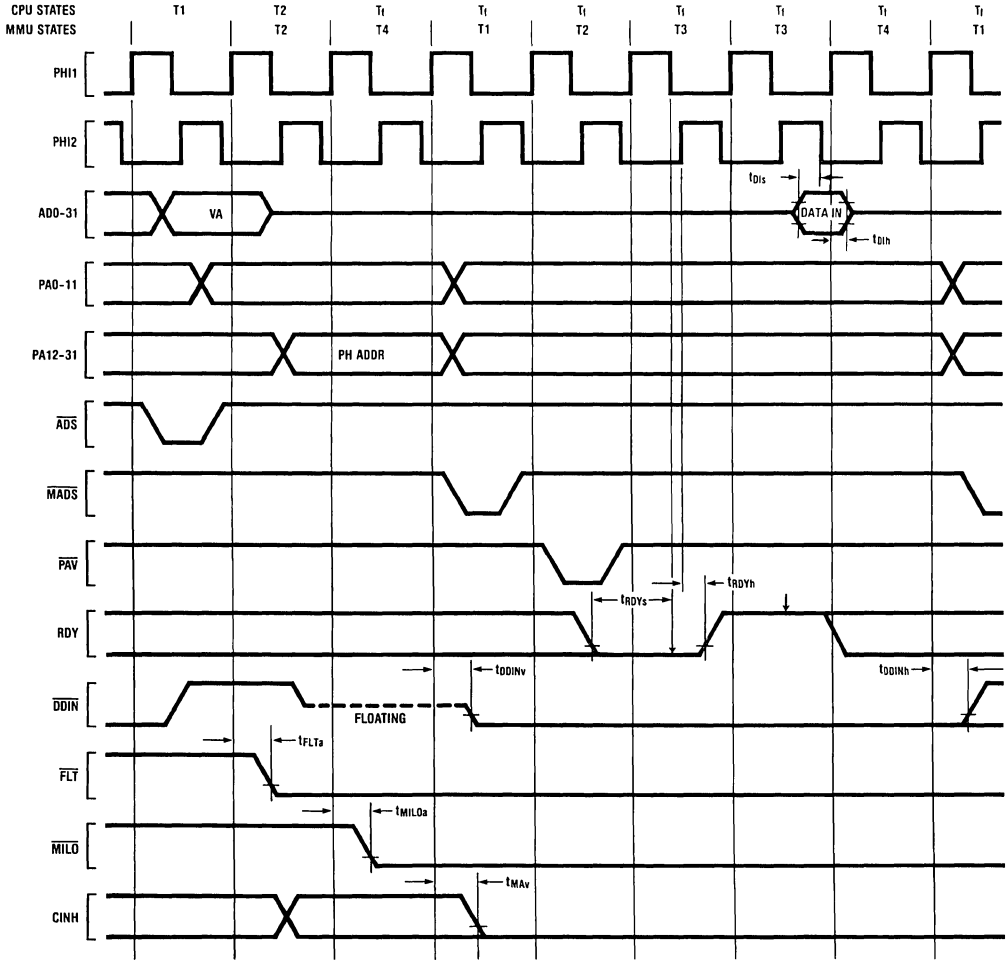

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FIGURE 4-5. MMU Read Cycle Timing (1-Wait State); After a TLB Miss

Note: After $\overline{FLT}$ is deasserted, $\overline{DDIN}$ may be driven temporarily by both CPU and MMU. This, however, does not cause any conflict. Since CPU and MMU force $\overline{DDIN}$ to the same logic level.

4.0 Device Specifications (Continued)

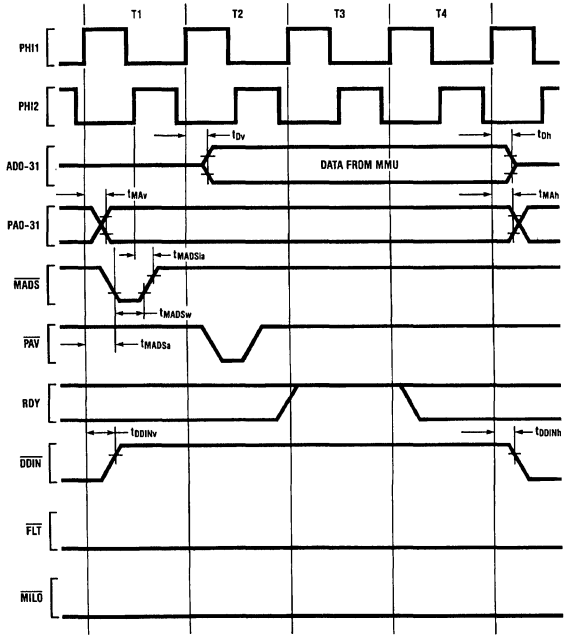

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FIGURE 4-6. MMU Write Cycle Timing; after a TLB Miss

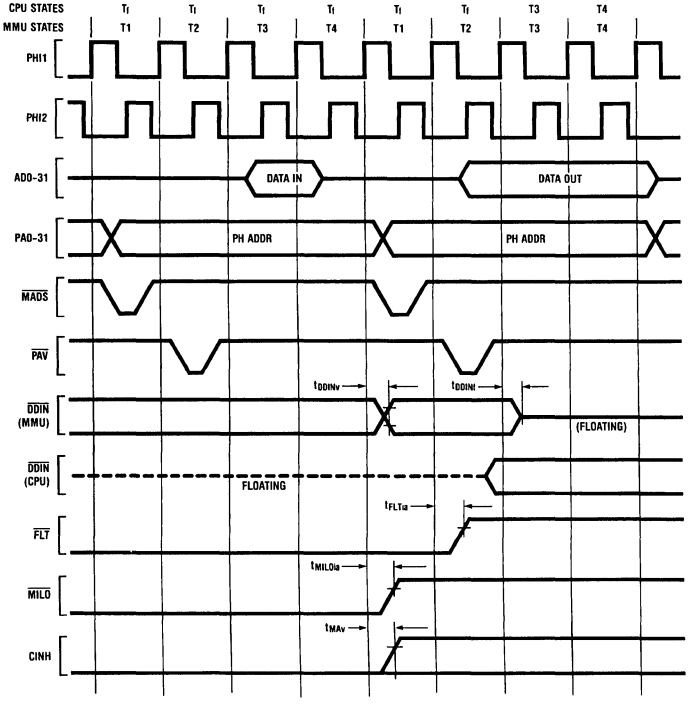

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FIGURE 4-7. $\overline{\text{FLT}}$ Deassertion Timing

Note: After $\overline{\text{FLT}}$ is deasserted, $\overline{\text{DDIN}}$ may be driven temporarily by both CPU and MMU. This, however, does not cause any conflict. Since CPU and MMU force $\overline{\text{DDIN}}$ to the same logic level.

4.0 Device Specifications (Continued)

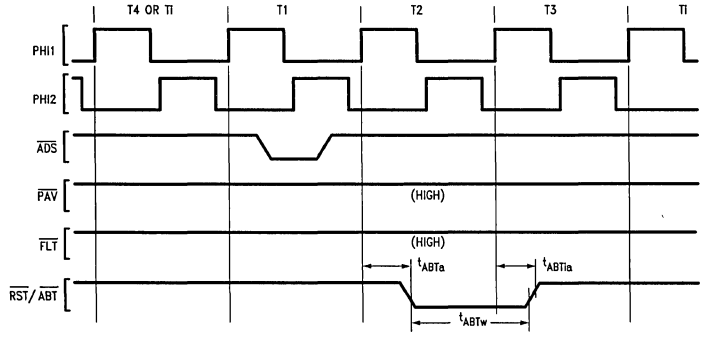

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FIGURE 4-8. Abort Timing ($\overline{FLT}$ = 1)

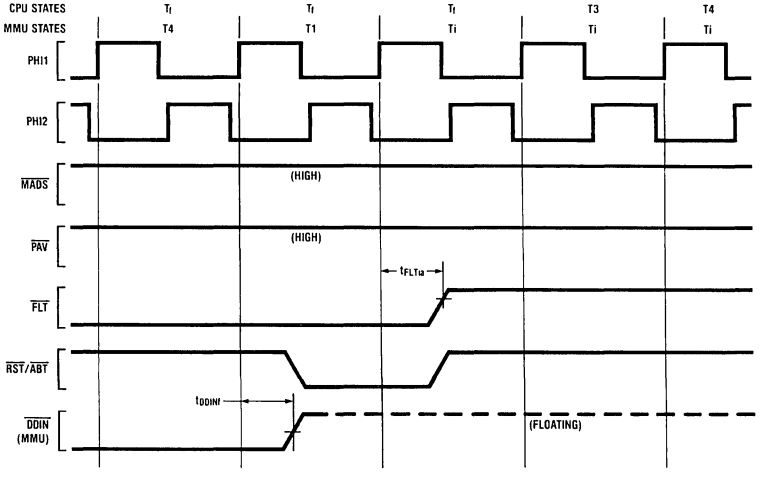

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FIGURE 4-9. Abort Timing ($\overline{FLT}$ = 0)

3

4.0 Device Specifications (Continued)

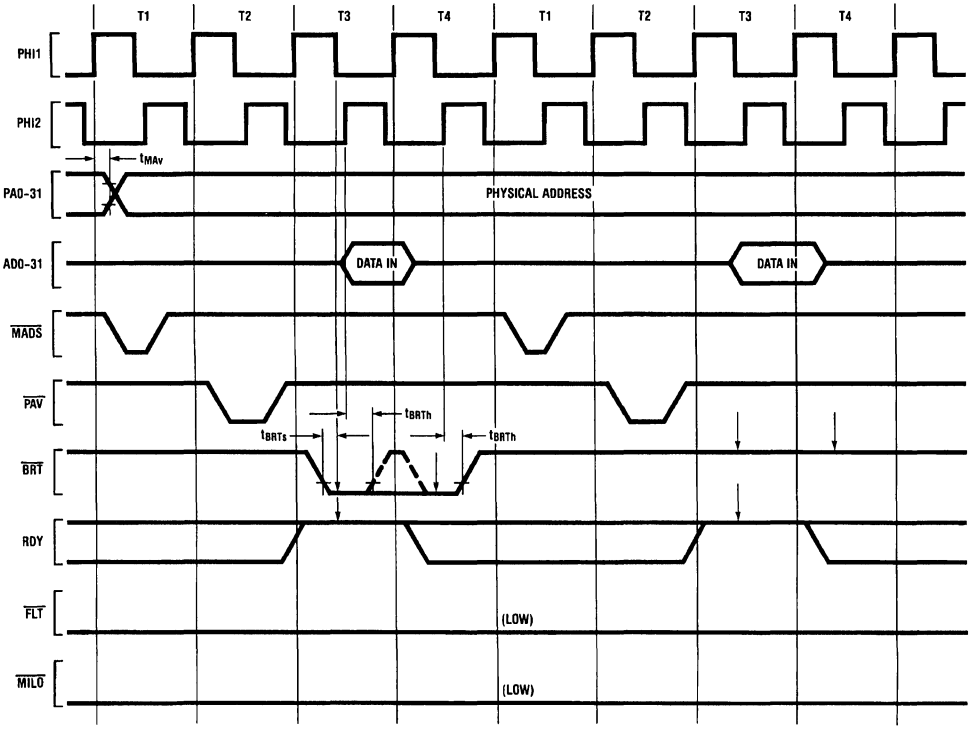

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FIGURE 4-10. MMU Bus Retry Timing

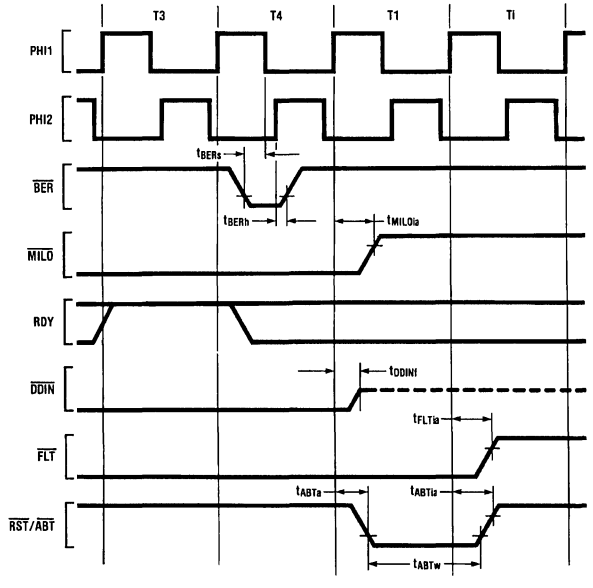

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FIGURE 4-11. Bus Error Timing

4.0 Device Specifications (Continued)

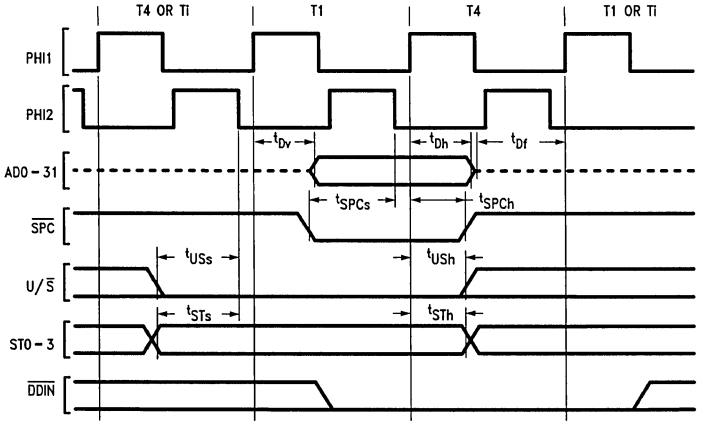

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FIGURE 4-12. Slave Access Timing; CPU Reading from MMU

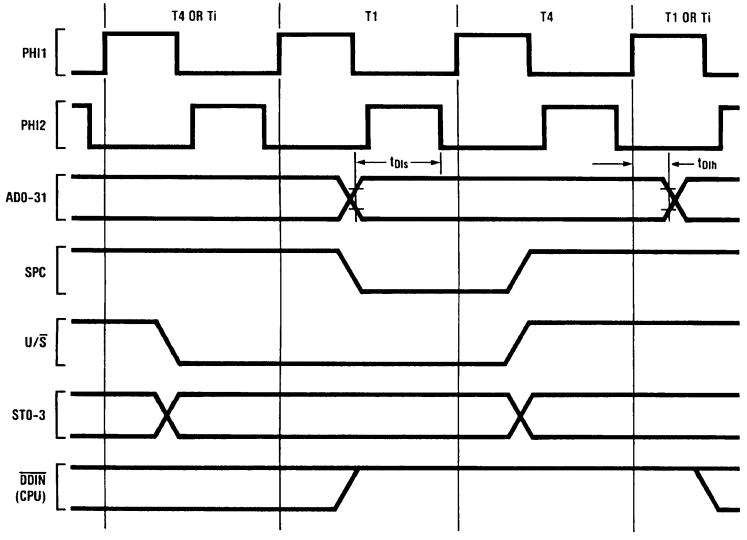

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FIGURE 4-13. Slave Access Timing; CPU Writing to MMU

3

4.0 Device Specifications (Continued)

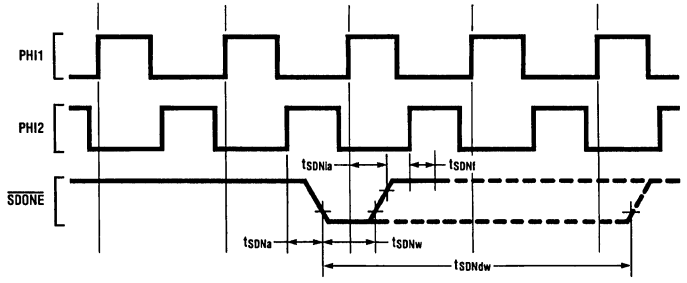

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FIGURE 4-14. $\overline{\text{SDONE}}$ Timing

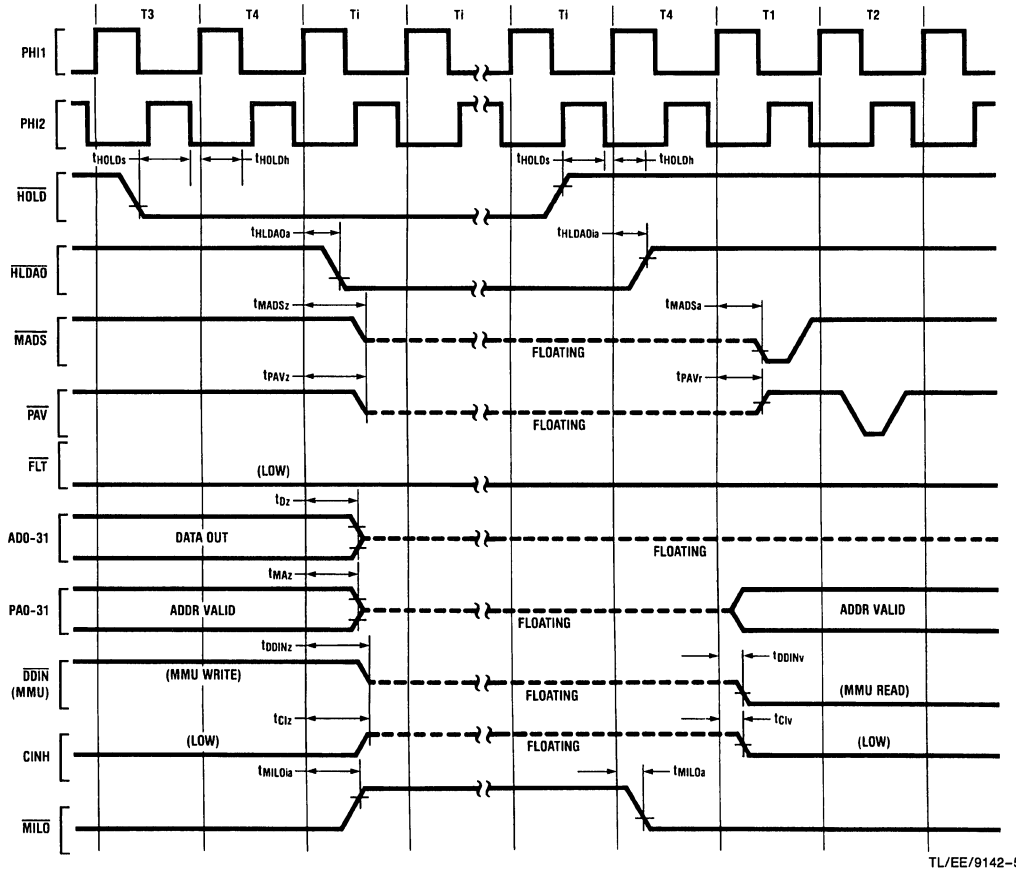

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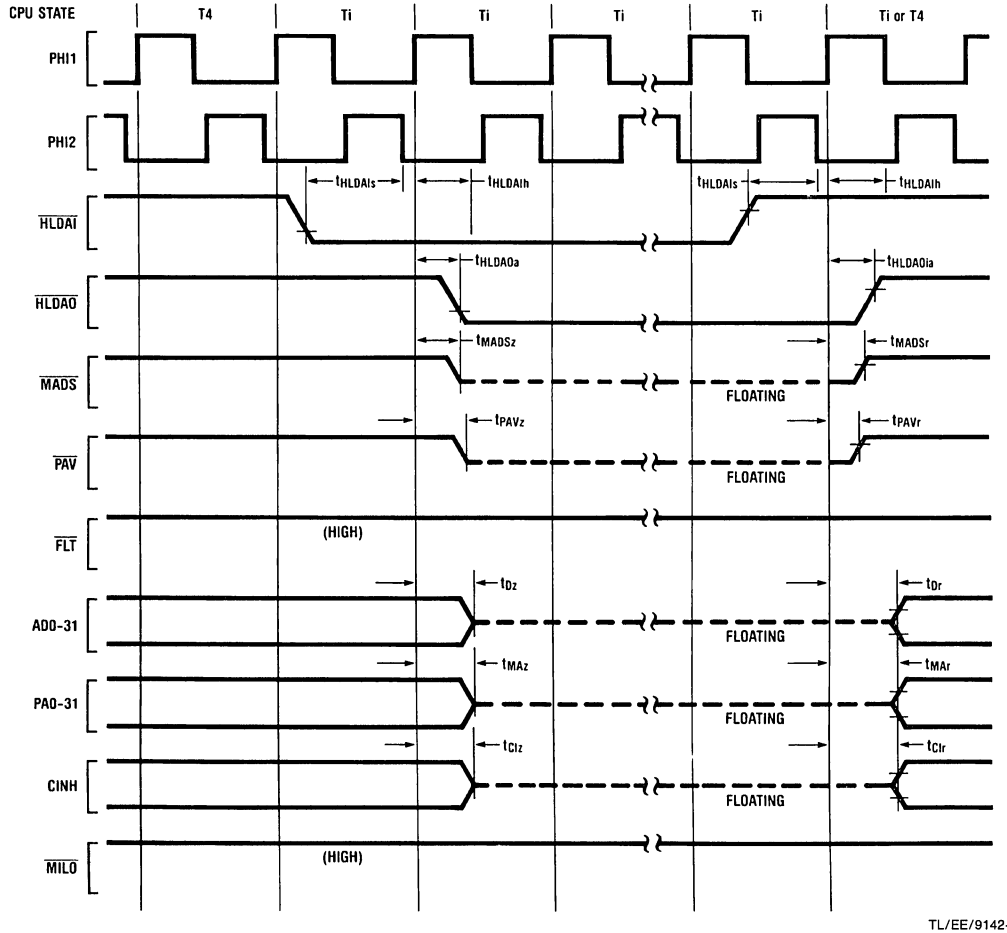
FIGURE 4-15. Hold Timing ($\overline{\text{FLT}}$ = 0)

4.0 Device Specifications (Continued)



TL/EE/9142-51

FIGURE 4-16. Hold Timing ($\overline{FLT}$ = 1)

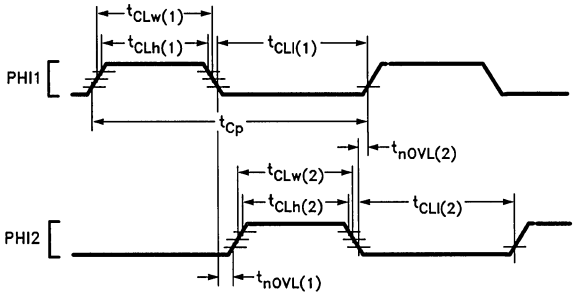


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FIGURE 4-17. Clock Waveforms

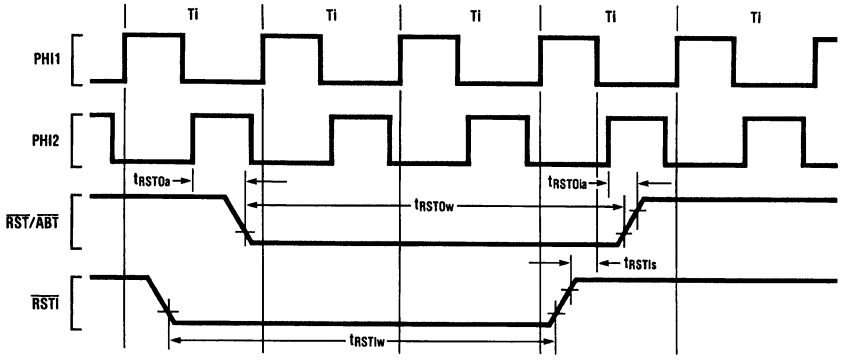

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FIGURE 4-18. Non Power-On Reset Timing

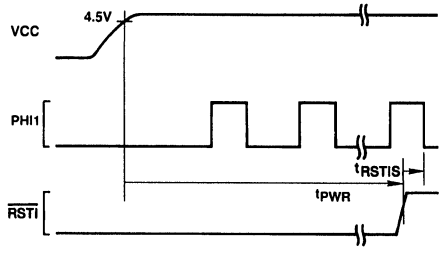

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FIGURE 4-19. Power-On Reset

Appendix A: Interfacing Suggestions

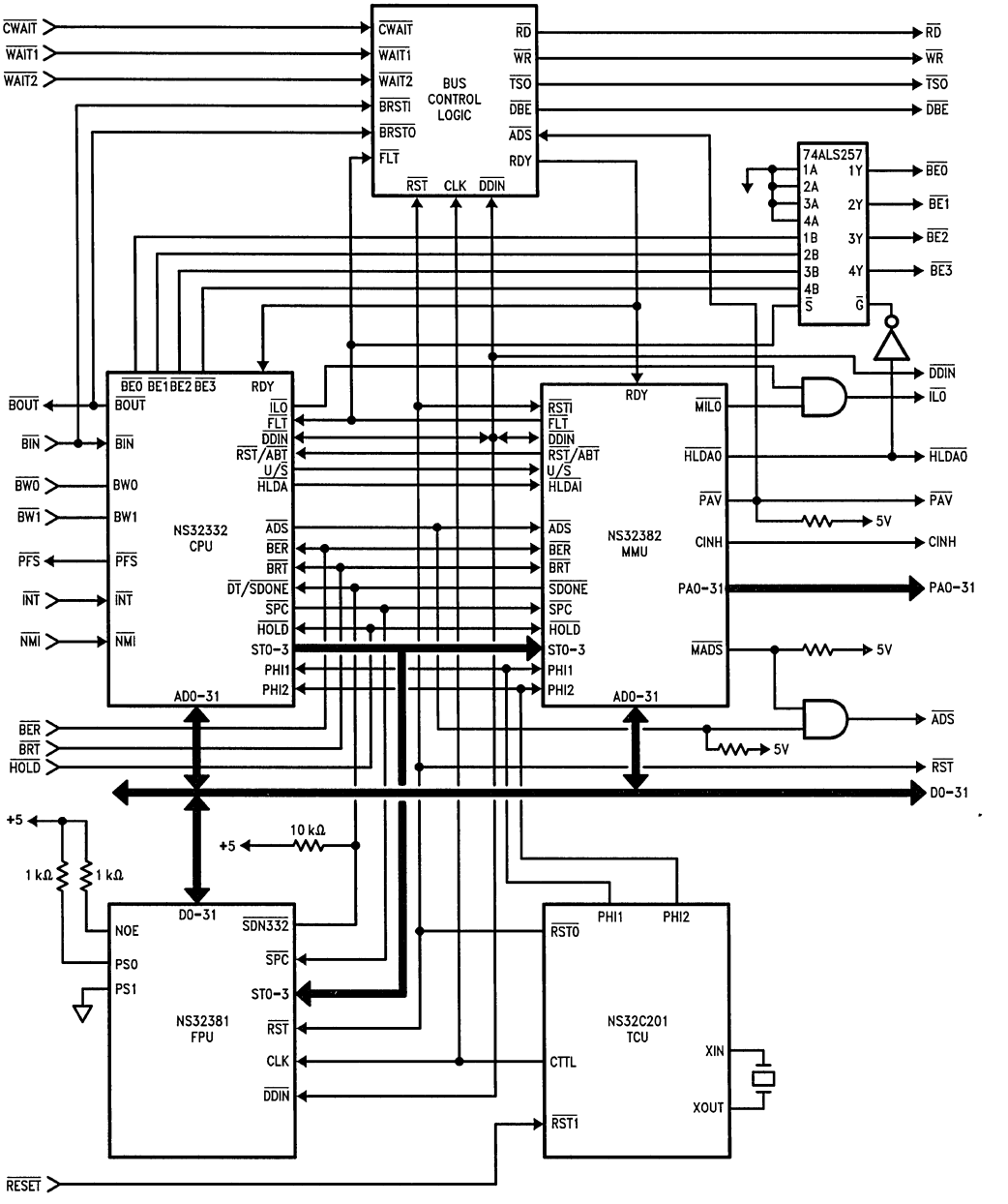

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FIGURE A-1. System Connection Diagram

National Semiconductor

NS32082-10 Memory Management Unit

General Description

The NS32082 Memory Management Unit (MMU) provides hardware support for demand-paged virtual memory implementations. The NS32082 functions as a slave processor in Series 32000 microprocessor-based systems. Its specific capabilities include fast dynamic translation, protection, and detailed status to assist an operating system in efficiently managing up to 32 Mbytes of physical memory. Support for multiple address spaces, virtual machines, and program debugging is provided.

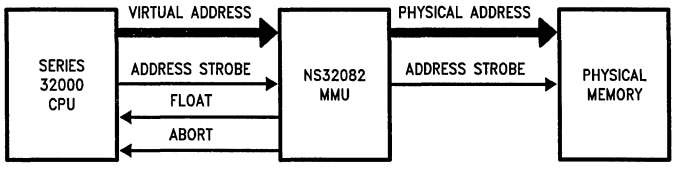
High-speed address translation is performed on-chip through a 32-entry fully associative translation look-aside buffer (TLB), which maintains itself from tables in memory with no software intervention. Protection violations and page faults (references to non-resident pages) are automatically detected by the MMU, which invokes the instruction abort feature of the CPU.

Additional features for program debugging include two breakpoint registers and a breakpoint counter, which provide the programmer with powerful stand-alone debugging capability.

Features

- Totally automatic mapping of 16 Mbyte virtual address space using memory based tables
- On-chip translation look-aside buffer allows 97% of translations to occur in one clock for most applications
- Full hardware support for virtual memory and virtual machines
- Implements "referenced" bits for simple, efficient working set management
- Protection mechanisms implemented via access level checking and dual space mapping
- Program debugging support
- Compatible with NS32016, NS32032 and NS32332 CPUs
- 48-pin dual-in-line package

Conceptual Address Translation Model



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List of Illustrations

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Tables

1.0 Product Introduction

The NS32082 MMU provides hardware support for three basic features of the Series 32000; dynamic address translation, access level checking and software debugging. Dynamic Address Translation is required to implement demand-paged virtual memory. Access level checking is performed during address translation, ensuring that unauthorized accesses do not occur. Because the MMU resides on the local bus and is in an ideal location to monitor CPU activity, debugging functions are also included.

The MMU is intended for use in implementing demand-paged virtual memory. The concept of demand-paged virtual memory is illustrated in *Figure 1-1*. At any point in time, a program sees a uniform addressing space of up to 16 megabytes (the "virtual" space), regardless of the actual size of the memory physically present in the system (the "physical" space). The full virtual space is recorded as an image on a mass storage device. Portions of the virtual space needed by a running program are copied into physical memory when needed.

To make the virtual information directly available to a running program, a mapping must be established between the virtual addresses asserted by the CPU and the physical addresses of the data being referenced.

To perform this mapping, the MMU divides the virtual memory space into 512-byte blocks called "pages." It interprets the 24-bit address from the CPU as a 15-bit "page number" followed by a 9-bit offset, which indicates the position of a byte within the selected page. Similarly, the MMU divides the physical memory into 512-byte frames, each of which can hold a virtual page.

The translation process is therefore modeled as accepting a virtual page number from the CPU and substituting the corresponding physical page frame number for it, as shown in *Figure 1-2*. The offset is not changed. The translated page frame number is 16 bits long, including an additional address bit (A24) intended for physical bank selection. Physical addresses issued by the MMU are 25 bits wide.

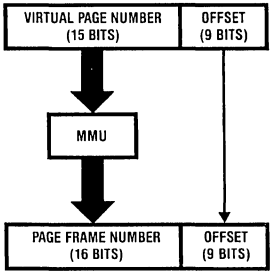

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FIGURE 1-2. NS32082 Address Translation Model

Generally, in virtual memory systems the available physical memory space is smaller than the maximum virtual memory space. Therefore, not all virtual pages are simultaneously resident. Nonresident pages are not directly addressable by the CPU. Whenever the CPU issues a virtual address for a nonresident or nonexistent page, a "page fault" will result. The MMU signals this condition by invoking the Abort feature of the CPU. The CPU then halts the memory cycle,

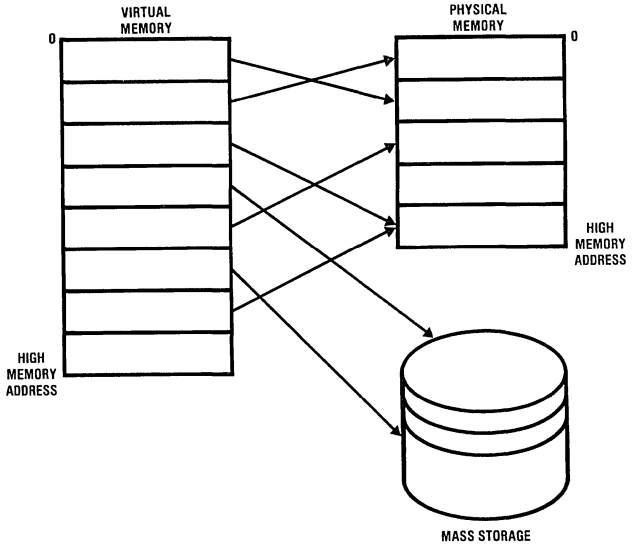

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FIGURE 1-1. The Virtual Memory Model

1.0 Product Introduction (Continued)

restores its internal state to the point prior to the instruction being executed, and enters the operating system through the abort trap vector.

The operating system reads from the MMU the virtual address which caused the abort. It selects a page frame which is either vacant or not recently used and, if necessary, writes this frame back to mass storage. The required virtual page is then copied into the selected page frame.

The MMU is informed of this change by updating the page tables (Section 3.2), and the operating system returns control to the aborted program using the RETT instruction. Since the return address supplied by the abort trap is the address of the aborted instruction, execution resumes by retrying the instruction.

This sequence is called paging. Since a page fault encountered in normal execution serves as a demand for a given page, the whole scheme is called demand-paged virtual memory.

The MMU also provides debugging support. It may be programmed to monitor the bus for two virtual or physical addresses in real time. A counter register is associated with one of these, providing a "break-on-N-occurrences" capability.

1.1 PROGRAMMING CONSIDERATIONS

When a CPU instruction is aborted as a result of a page fault, some memory resident data might have been already modified by the instruction before the occurrence of the abort.

This could compromise the restartability of the instruction when the CPU returns from the abort routine.

To guarantee correct results following the re-execution of the aborted instruction, the following actions should not be attempted:

a) No instruction should try to overlay part of a source operand with part of the result. It is, however, permissible to rewrite the result into the source operand exactly if page faults are being generated only by invalid pages and not by write protection violations (for example, the instruction "ABSW X, X", which replaces X with its absolute value). Also, never write to any memory location which is necessary for calculating the effective address of either operand (i.e. the pointer in "Memory Relative" addressing mode; the Link Table pointer or Link Table Entry in "External" addressing mode).

b) No instruction should perform a conversion in place from one data type to another larger data type (Example: MOVWF X, X which replaces the 16-bit integer value in memory location X with its 32-bit floating-point value). The addressing mode combination "TOS, TOS" is an exception, and is allowed. This is because the least-significant part of the result is written to the possibly invalid page before the source operand is affected. Also, integer conversions to larger integers always work correctly in place, because the low-order portion of the result always matches the source value.

c) When performing the MOVM instruction, the entire source and destination blocks must be considered "operands" as above, and they must not overlap.

2.0 Functional Description

2.1 POWER AND GROUNDING

The NS32082 requires a single 5V power supply, applied on pin 48 (V_{CC}).

Grounding connections are made on two pins. Logic Ground (GNDL, pin 24) is the common pin for on-chip logic, and Buffer Ground (GNDB, pin 25) is the common pin for the output drivers. For optimal noise immunity, it is recommended that GNDL be attached through a single conductor directly to GNDB, and that all other grounding connections be made only to GNDB, as shown below (*Figure 2-1*).

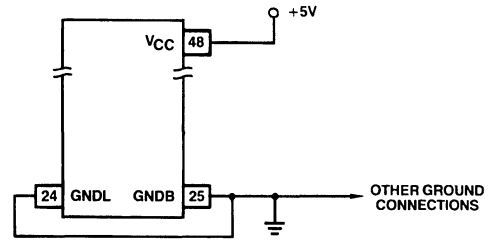

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FIGURE 2-1. Recommended Supply Connections

2.2 CLOCKING

The NS32082 inputs clocking signals from the NS32201 Timing Control Unit (TCU), which presents two non-overlapping phases of a single clock frequency. These phases are called PHI1 (pin 26) and PHI2 (pin 27). Their relationship to each other is shown in *Figure 2-2*.

Each rising edge of PHI1 defines a transition in the timing state ("T-State") of the MMU. One T-State represents one hardware cycle within the MMU, and/or one step of an external bus transfer. See Section 4 for complete specifications of PHI1 and PHI2.

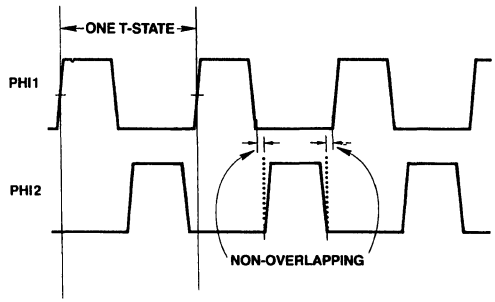

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FIGURE 2-2. Clock Timing Relationships

As the TCU presents signals with very fast transitions, it is recommended that the conductors carrying PHI1 and PHI2 be kept as short as possible, and that they not be connected to any devices other than the CPU and MMU. A TTL Clock signal (CTTL) is provided by the TCU for all other clocking.

2.0 Functional Description (Continued)

2.3 RESETTING

The $\overline{RSTI}$ input pin is used to reset the NS32082. The MMU responds to $\overline{RSTI}$ by terminating processing, resetting its internal logic and clearing the appropriate bits in the MSR register.

Only the MSR register is changed on reset. No other program accessible registers, including the TLB are affected.

The $\overline{RST}/\overline{ABT}$ signal is activated by the MMU on reset. This signal should be used to reset the CPU. $\overline{AT}/\overline{SPC}$ is held low for five clock cycles after the rising edge of $\overline{RSTI}$ to indicate to the CPU that the address translation mode must be selected.

The A24/$\overline{HBF}$ signal is sampled by the MMU on the rising edge of $\overline{RSTI}$. It indicates the bus size of the attached CPU. A24/$\overline{HBF}$ must be sampled high for a 16-bit bus and low for a 32-bit bus.

On application of power, $\overline{RSTI}$ must be held low for at least 50 μs after V_{CC} is stable. This is to ensure that all on-chip voltages are completely stable before operation. Whenever a Reset is applied, it must also remain active for not less than 64 clock cycles. The rising edge must occur while PHI1 is high. See *Figures 2-3* and *2-4*.

The NS32201 Timing Control Unit (TCU) provides circuitry to meet the Reset requirements of the NS32082 MMU. *Figure 2-5* shows the recommended connections.

2.4 BUS OPERATION

2.4.1 Interconnections

The MMU runs synchronously with the CPU, sharing with it a single multiplexed address/data bus. The interconnections used by the MMU for bus control, when used in conjunction with the NS32016, are shown in *Figure A-1* (Appendix A).

The CPU issues 24-bit virtual addresses on the bus, and status information on other pins, pulsing the signal $\overline{ADS}$ low. These are monitored by the MMU. The MMU issues 25-bit physical addresses on the bus, pulsing the $\overline{PAV}$ line low. The $\overline{PAV}$ pulse triggers the address latches and signals the NS32201 TCU to begin a bus cycle. The TCU in turn generates the necessary bus control signals and synchronizes the insertion of WAIT states, by providing the signal RDY to the MMU and CPU. Note that it is the MMU rather than the CPU that actually triggers bus activity in the system.

The functions of other interface signals used by the MMU to control bus activity are described below.

The ST0–ST3 pins indicate the type of cycle being initiated by the CPU. ST0 is the least-significant bit of the code. Table 2-1 shows the interpretations of the status codes presented on these lines.

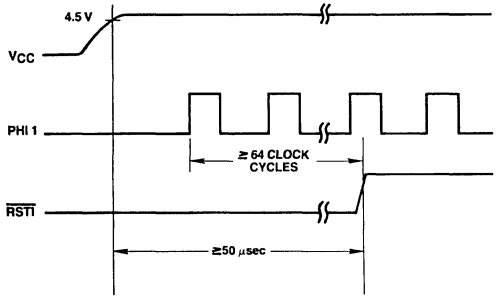

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FIGURE 2-3. Power-On Reset Requirements

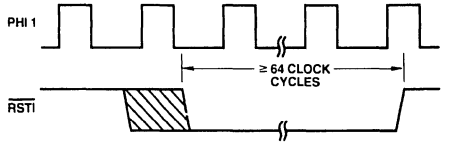

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FIGURE 2-4. General Reset Timing

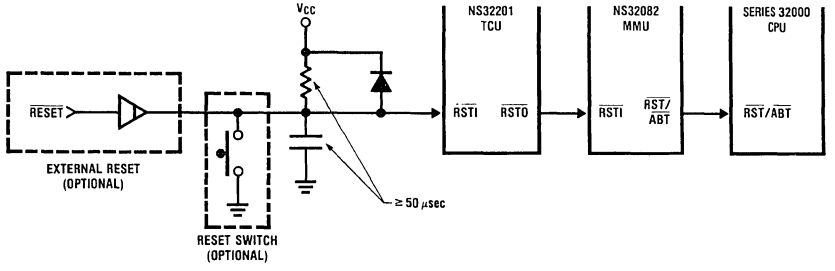

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FIGURE 2-5. Recommended Reset Connections, Memory-Managed System

2.0 Functional Description (Continued)

Status codes that are relevant to the MMU's function during a memory reference are:

1000, 1001 Instruction Fetch status, used by the debugging features to distinguish between data and instruction references.

1010 Data Transfer. A data value is to be transferred.

1011 Read RMW Operand. Although this is always a Read cycle, the MMU treats it as a Write cycle for purposes of protection and breakpointing.

1100 Read for effective address. Data used for address calculation is being transferred.

All other status codes are treated as data accesses if they occur in conjunction with a pulse on the $\overline{ADS}$ pin. Note that these include Interrupt Acknowledge and End of Interrupt cycles performed by the CPU. The status codes 1101, 1110 and 1111 are also recognized by the MMU in conjunction with pulses on the $\overline{SPC}$ line while it is executing Slave Processor instructions, but these do not occur in a context relevant to address translation.

TABLE 2-1. ST0–ST3 Encodings (ST0 is the Least Significant)

0000 — Idle: CPU Inactive on Bus
0001 — Idle: WAIT Instruction
0010 — (Reserved)
0011 — Idle: Waiting for Slave
0100 — Interrupt Acknowledge, Master
0101 — Interrupt Acknowledge, Cascaded
0110 — End of Interrupt, Master
0111 — End of Interrupt, Cascaded
1000 — Sequential Instruction Fetch
1001 — Non-Sequential Instruction Fetch
1010 — Data Transfer
1011 — Read Read-Modify-Write Operand
1100 — Read for Effective Address
1101 — Transfer Slave Operand
1110 — Read Slave Status Word
1111 — Broadcast Slave ID

The $\overline{DDIN}$ line indicates the direction of the transfer: 0 = Read, 1 = Write.

$\overline{DDIN}$ is monitored by the MMU during CPU cycles to detect write operations, and is driven by the MMU during MMU-initiated bus cycles.

The U/$\overline{S}$ pin indicates the privilege level at which the CPU is making the access: 0 = Supervisor Mode, 1 = User Mode. It is used by the MMU to select the address space for translation and to perform protection level checking. Normally, the U/$\overline{S}$ pin is a direct reflection of the U bit in the CPU's Processor Status Register (PSR). The MOVUS and MOVSU CPU instructions, however, toggle this pin on successive operand accesses in order to move data between virtual spaces.

The MMU uses the $\overline{FLT}$ line to take control of the bus from the CPU. It does so as necessary for updating its internal TLB from the Page Tables in memory, for maintaining the contents of the status bits (R and M) in the Page Table Entries, and for implementing bus timing adjustments needed by the debugging features.

The MMU also aborts invalid accesses attempted by the CPU. This is done by pulsing the $\overline{RST}/\overline{ABT}$ pin low for one clock period. (A pulse longer than one clock period is interpreted by the CPU as a Reset command).

Because the MMU performs only 16-bit transfers, some additional circuitry is needed to interface it to the 32-bit data bus of an NS32032-based system. However, since the MMU never writes to the most-significant word of a Page Table Entry, the only special requirement is that it must be able to read from the top half of the bus. This can be accomplished as shown in *Figure A-2* (Appendix A) by using a 16-bit unidirectional buffer and some gating circuitry that enables it whenever an MMU-initiated bus cycle accesses an address ending in binary "10".

The bus connections required in conjunction with the NS32332 CPU are somewhat more complex (see the NS32332 data sheet), but the sequences of events documented here still hold.

2.4.2 CPU-Initiated Bus Cycles

A CPU-initiated bus cycle is performed in a minimum of five clock cycles (four in the case of the NS32332): T1, TMMU, T2, T3 and T4, as shown in *Figure 2-6*.

During period T1, the CPU places the virtual address to be translated on the bus, and the MMU latches it internally and begins translation. The MMU also samples the $\overline{DDIN}$ pin, the status lines ST0–ST3, and the U/$\overline{S}$ pin to determine how the CPU intends to use the bus.

During period TMMU the CPU floats its bus drivers and the MMU takes one of three actions:

1) If the translation for the virtual address is resident in the MMU's TLB, and the access being attempted by the CPU does not violate the protection level of the page being referenced, the MMU presents the translated address and generates a $\overline{PAV}$ pulse to trigger a bus cycle in the rest of the system. See *Figure 2-6*.
2) If the translation for the virtual address is resident in the MMU's TLB, but the access being attempted by the CPU is not allowed due to the protection level of the page being referenced, the MMU generates a pulse on the $\overline{RST}/\overline{ABT}$ pin to abort the CPU's access. No $\overline{PAV}$ pulse is generated. See *Figure 2-7*.
3) If the translation for the virtual address is not resident in the TLB, or if the CPU is writing to a page whose M bit is not yet set, the MMU takes control of the bus asserting the $\overline{FLT}$ signal as shown in *Figure 2-8*. This causes the CPU to float its bus and wait. The MMU then initiates a sequence of bus cycles as described in Section 2.4.3.

From state T2 through T4 data is transferred on the bus between the CPU and memory, and the TCU provides the strobes for the transfer. During this time the MMU floats

2.0 Functional Description (Continued)

pins AD0–AD15, and handles pins A16–A24 according to the mode of operation (16-bit or 32-bit) selected during reset (Section 2.3).

In 16-bit bus mode, the MMU drives address lines A16–A24 from TMMU through T4 and they need not be latched externally. This is appropriate for the NS32016 CPU, which uses only AD0–AD15 for data transfers. In 32-bit bus mode, the MMU asserts the physical address on pins A16–A24 only during TMMU, and floats them from T2 through T4 because the CPU uses them for data transfer. In this case the physical address presented on these lines must be latched externally using $\overline{PAV}$.

Whenever the MMU generates an Abort pulse on the $\overline{RST}/\overline{ABT}$ pin, the CPU enters state T2 and then Ti (idle), ending the bus cycle. Since no $\overline{PAV}$ pulse is issued by the MMU, the rest of the system remains unaware that an access has been attempted. The MMU requires that no further memory references be attempted by the CPU for at least two clock cycles after the T2 state, as shown in *Figure 2-7*. This requirement is met by all Series 32000 CPU's. During this time, the RDY line must remain high. This requirement is met by the NS32201 TCU.

2.4.3 MMU-Initiated Cycles

Bus cycles initiated by the MMU are always nested within CPU-initiated bus cycles; that is, they appear after the MMU has accepted a virtual address from the CPU and has set the $\overline{FLT}$ line active. The MMU will initiate memory cycles in the following cases:

1) There is no translation in the MMU's TLB for the virtual address issued by the CPU, meaning that the MMU must reference the Page Tables in memory to obtain the translation.
2) There is a translation for that virtual address in the TLB, but the page is being written for the first time (the M bit in its Level-2 Page Table Entry is 0). The MMU treats this case as if there were no translation in the TLB, and performs a Page Table lookup in order to set the M bit in the Level-2 Page Table Entry as well as in the TLB.

Having made the necessary memory references, the MMU either aborts the CPU access or it provides the translated address and allows the CPU's access to continue to T2.

Figure 2-8 shows the sequence of events in a Page Table lookup. After asserting $\overline{FLT}$, the MMU waits for one additional clock cycle, then reads the Level-1 Page Table Entry and the Level-2 Page Table Entry in four consecutive memory Read cycles. Note that the MMU performs two 16-bit transfers to read each Page Table Entry, regardless of the width of the CPU's data bus. There are no idle clock cycles between MMU-initiated bus cycles unless a bus request is made on the $\overline{HOLD}$ line (Section 2.6).

During the Page Table lookup the MMU drives the $\overline{DDIN}$ signal. The status lines ST0–ST3 and the U/$\overline{S}$ pin are not released by the CPU, and retain their original settings while the MMU uses the bus. The Byte Enable signals from the CPU ($\overline{HBE}$ in 16-bit systems, $\overline{BE0}$–$\overline{BE3}$ in 32-bit systems) should in general be handled externally for correct memory referencing. (The current NS32016 CPU does, however, handle $\overline{HBE}$ in a manner that is acceptable in many systems at clock rates of 12.5 MHz or less.)

In the clock cycle immediately after T4 of the last lookup cycle, the MMU removes the $\overline{FLT}$ signal, issues the translated address, and pulses $\overline{PAV}$ to continue the CPU's access.

Note that when the MMU sets $\overline{FLT}$ active, the clock cycle originally called TMMU is redesignated Tf. Clock cycles in which the $\overline{PAV}$ pulse occurs are designated TMMU.

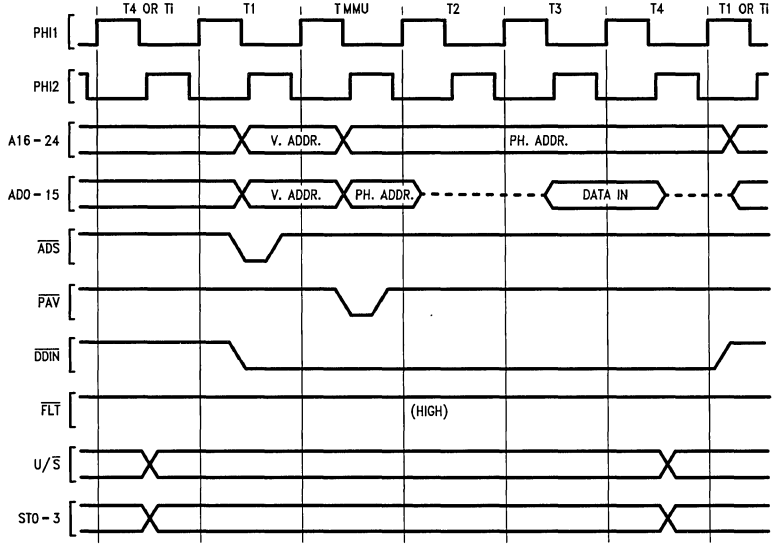

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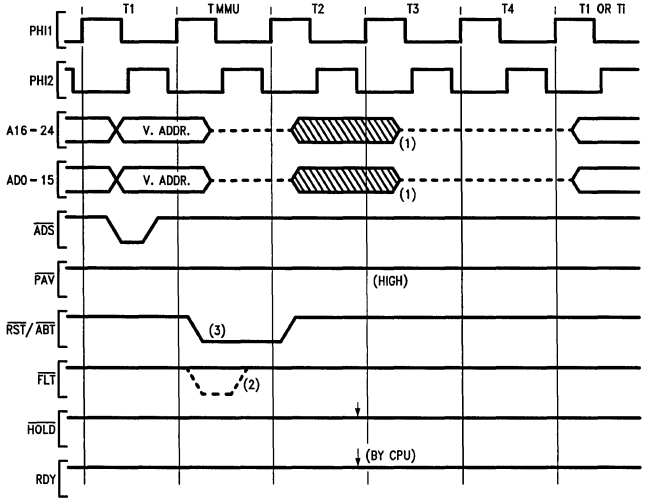
FIGURE 2-6. CPU Read Cycle; Translation in TLB (TLB Hit)

2.0 Functional Description (Continued)



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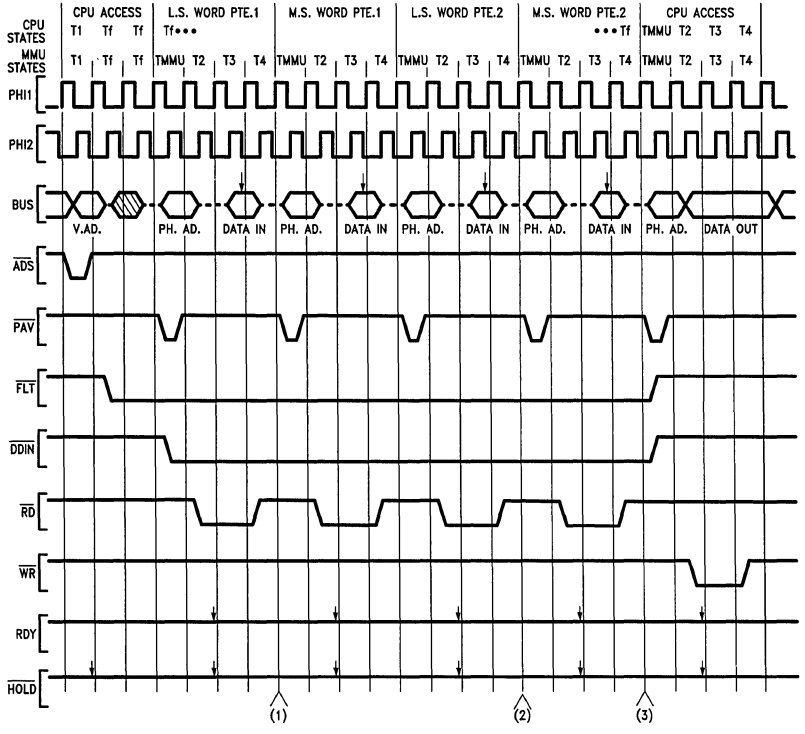
Note 1: The CPU drives the bus if a write cycle is aborted.

Note 2: FLT may be pulsed if a breakpoint on physical address is enabled or an execution breakpoint is triggered.

Note 3: If this bus cycle is a write cycle to a write-protected page, FLT is asserted for two clock cycles and the abort pulse is delayed by one clock cycle.

FIGURE 2-7. Abort Resulting from Protection Violation; Translation in TLB



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Note 1: If the R bit on the Level-1 PTE must be set, a write cycle is inserted here.

Note 2: If either the R or the M bit on the Level-2 PTE must be set, a write cycle is inserted here.

Note 3: If a breakpoint on physical address is enabled, an extra clock cycle is inserted here.

FIGURE 2-8. Page Table Lookup

2.0 Functional Description (Continued)

The Page Table Entries are read starting with the low-order word. If the V bit (bit 0) of the low-order word is zero, or the protection level field PL (bits 1 and 2) indicates that the CPU's attempted access is illegal, the MMU does not generate any further memory cycles, but instead issues an Abort pulse during the clock cycle after T4 and removes the $\overline{FLT}$ signal. The CPU continues to T2 and then becomes idle on the bus, as shown in *Figure 2-9*.

If the R and/or M bit (bit 3 or 4) of the low-order word must be updated, the MMU does this immediately in a single Write cycle, before reading the high-order word of the Page Table Entry. All bits except those updated are rewritten with their original values.

At most, the MMU writes two 16-bit words to memory during a translation: the first to the Level-1 table to update the R bit, and the second to the Level-2 table to update the R and/or M bits.

2.4.4 Cycle Extension

To allow sufficient strobe widths and access time requirements for any speed of memory or peripheral device, the NS32082 provides for extension of a bus cycle. Any type of bus cycle, CPU-initiated or MMU-initiated, can be extended, except Slave Processor cycles, which are not memory or peripheral references.

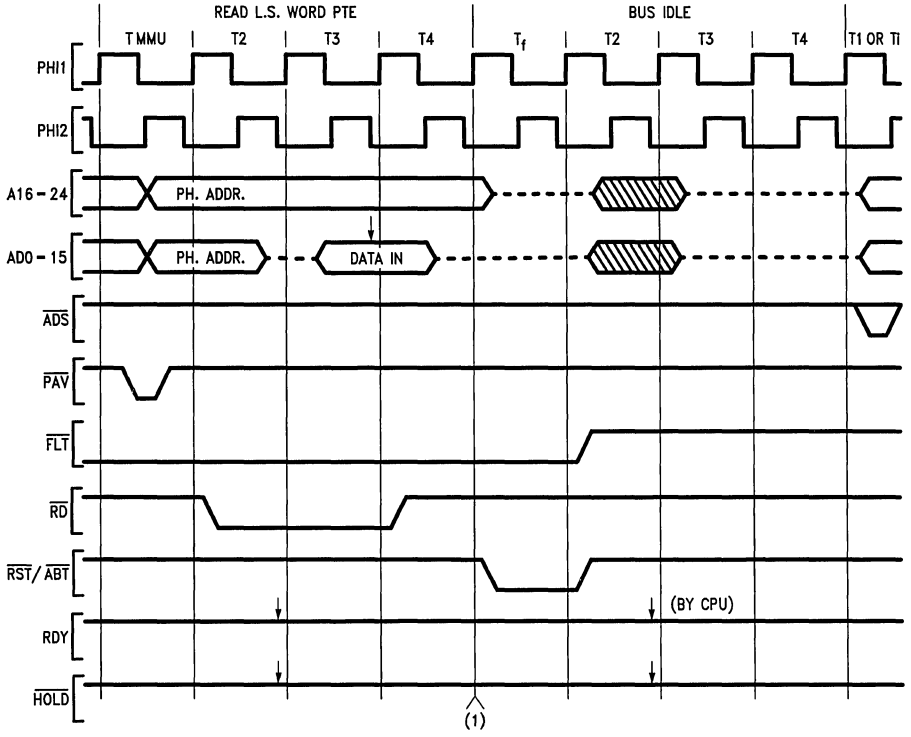
In *Figures 2-6* and *2-8*, note that during T3 all bus control signals are flat. Therefore, a bus cycle can be cleanly extended by causing the T3 state to be repeated. This is the purpose of the RDY (Ready) pin.

Immediately before T3 begins, on the falling edge of clock phase PHI2, the RDY line is sampled by the CPU and/or the MMU. If RDY is high, the next state after T3 will be T4, ending the bus cycle. If it is low, the next state after T3 will be another T3 and the RDY line will be sampled again. RDY is sampled in each following clock period, with insertion of additional T3 states, until it is sampled high. Each additional T3 state inserted is called a "WAIT state."

During CPU bus cycles, the MMU monitors the RDY pin only if the 16-bit mode is selected. This is necessary since the MMU drives the address lines A16–A24, and needs to detect the end of the bus cycle in order to float them.

If the 32-bit mode is selected, the above address lines are floated following the TMMU state. The MMU will be ready to perform another translation after three clock cycles, and the RDY line is ignored.

The RDY pin is driven by the NS32201 Timing Control Unit, which applies WAIT states to the CPU and MMU as requested on its own WAIT request input pins.



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Note 1: If a breakpoint on physical address is enabled, an extra clock cycle is inserted here.

FIGURE 2-9. Abort Resulting after a Page Table Lookup

2.0 Functional Description (Continued)

2.5 SLAVE PROCESSOR INTERFACE

The CPU and MMU execute four instructions cooperatively. These are LMR, SMR, RDVAL and WRVAL, as described in Section 2.5.2. The MMU takes the role of a Slave Processor in executing these instructions, accepting them as they are issued to it by the CPU. The CPU calculates all effective addresses and performs all operand transfers to and from memory and the MMU. The MMU does not take control of the bus except as necessary in normal operation; i.e., to translate and validate memory addresses as they are presented by the CPU.

The sequence of transfers ("protocol") followed by the CPU and MMU involves a special type of bus cycle performed by the CPU. This "Slave Processor" bus cycle does not involve the issuing of an address, but rather performs a fast data transfer whose purpose is pre-determined by the form of the instruction under execution and by status codes asserted by the CPU.

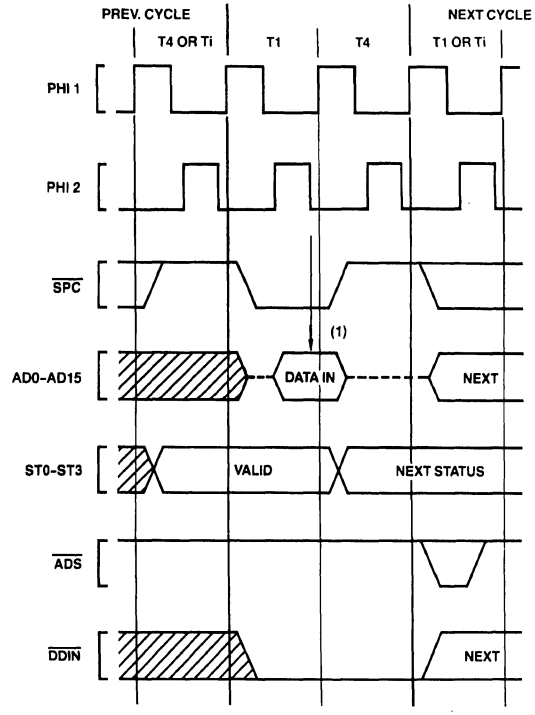
2.5.1 Slave Processor Bus Cycles

The interconnections between the CPU and MMU for Slave Processor communication are shown in *Figures A-1* and *A-2* (Appendix A). The low-order 16 bits of the bus are used for data transfers. The $\overline{SPC}$ signal is bidirectional. It is pulsed by the CPU as a low-active data strobe for Slave Processor transfers, and is also pulsed low by the MMU to acknowledge, when necessary, that it is ready to continue execution of an MMU instruction. Since $\overline{SPC}$ is normally in a high-impedance state, it must be pulled high with a 10 kΩ resistor, as shown. The MMU also monitors the status lines ST0–ST3 to follow the protocol for the instruction being executed.

Data is transferred between the CPU and the MMU with Slave Processor bus cycles, illustrated in *Figures 2-10* and *2-11*. Each bus cycle transfers one byte or one word (16 bits) to or from the MMU.

Slave Processor bus cycles are performed by the CPU in two clock periods, which are labeled T1 and T4. During T1, the CPU activates $\overline{SPC}$ and, if it is writing to the MMU, it presents data on the bus. During T4, the CPU deactivates $\overline{SPC}$ and, if it is reading from the MMU, it latches data from the bus. The CPU guarantees that data written to the MMU is held through T4 to provide for the MMU's hold time requirements. The CPU also guarantees that the status code on ST0–ST3 becomes valid, at the latest, during the clock period preceding T1. The status code changes during T4 to anticipate the next bus cycle, if any.

Note that Slave Processor bus cycles are never extended with WAIT states. The RDY line is not sampled.



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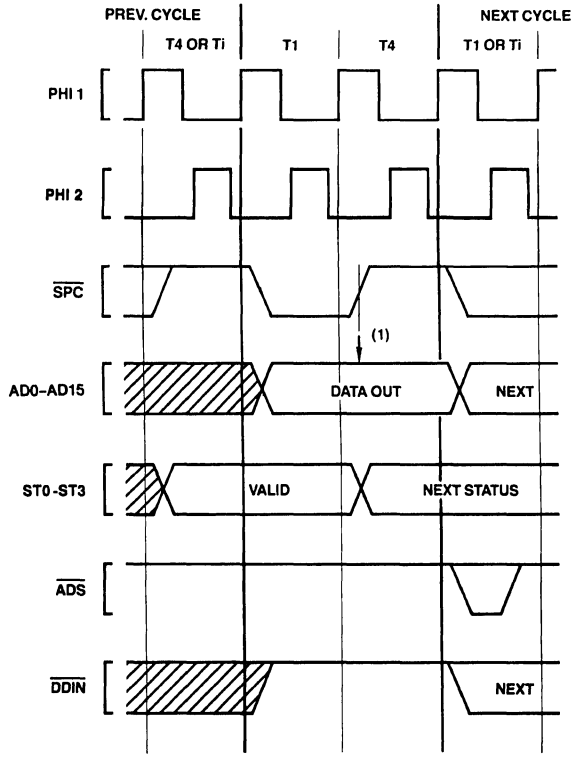
Note 1: CPU samples Data Bus here.

FIGURE 2-10. Slave Access Timing; CPU Reading from MMU

2.0 Functional Description (Continued)



Note 1: MMU samples Data Bus here.

FIGURE 2-11. Slave Access Timing; CPU Writing to MMU

2.5.2 Instruction Protocols

MMU instructions have a three-byte Basic Instruction field consisting of an ID byte followed by an Operation Word. See *Figure 3-10* for the MMU instruction encodings. The ID Byte has three functions:

1) It identifies the instruction as being a Slave Processor instruction.
2) It specifies that the MMU will execute it.
3) It determines the format of the following Operation Word of the instruction.

The CPU initiates an MMU instruction by issuing first the ID Byte and then the Operation Word, using Slave Processor bus cycles. The ID Byte is sent on the least-significant byte of the bus, in conjunction with status code 1111 (Broadcast ID Byte). The Operation Word is sent on the entire 16-bit data bus, with status code 1101 (Transfer Operation Word / Operand). The Operation Word is sent with its bytes swapped; i.e., its least-significant byte is presented to the MMU on the most-significant half of the 16-bit bus.

Other actions are taken by the CPU and the MMU according to the instruction under execution, as shown in Tables 2-2, 2-3 and 2-4.

In executing the LMR instruction (Load MMU Register, Table 2-2), the CPU issues the ID Byte, the Operation Word, and then the operand value to be loaded by the MMU. The register to be loaded is specified in a field within the Operation Word of the instruction.

In executing the SMR instruction (Store MMU Register, Table 2-3), the CPU also issues the ID Byte and the Operation Word of the instruction to the MMU. It then waits for the MMU to signal (by pulsing $\overline{SPC}$ low) that it is ready to present the specified register's contents to the CPU. Upon receiving this "Done" pulse, the CPU reads first a "Status Word" (dictated by the protocol for Slave Processor instructions) which the MMU provides as a word of all zeroes. The CPU then reads the contents of the selected register in two successive Slave Processor bus cycles, and places this result value into the instruction's destination (a CPU general-purpose register or a memory location).

In executing the RDVAL (Read-Validate) or WRVAL (Write-Validate) instruction, the CPU again issues the ID Byte and the Operation Word to the MMU. However, its next action is to initiate a one-byte Read cycle from the memory address whose protection level is being tested. It does so while presenting status code 1010; this being the only place that this status code appears during a RDVAL or WRVAL instruction. This memory access triggers a special address translation from the MMU. The translation is performed by the MMU using User-Mode mapping, and any protection violation occurring during this memory cycle does not cause an Abort. The MMU will, however, abort the CPU if the Level-1 Page Table Entry is invalid.

Upon completion of the address translation, the MMU pulses $\overline{SPC}$ to acknowledge that the instruction may continue execution.

2.0 Functional Description (Continued)

TABLE 2-2. LMR Instruction Protocol

CPU Action	Status	MMU Action
Issues ID Byte of instruction, pulsing $\overline{SPC}$.	1111	Accepts ID Byte.
Sends Operation Word of Instruction, pulsing $\overline{SPC}$.	1101	Decodes instruction.
Issues low-order word of new register value to MMU, pulsing $\overline{SPC}$.	1101	Accepts word from bus; places it into low-order half of referenced MMU register.
Issues high-order word of new register value to MMU, pulsing $\overline{SPC}$.	1101	Accepts word from bus; places it into high-order half of referenced MMU register.

TABLE 2-3. SMR Instruction Protocol

CPU Action	Status	MMU Action
Issues ID Byte of Instruction, pulsing $\overline{SPC}$.	1111	Accepts ID Byte.
Sends Operation Word of instruction, pulsing $\overline{SPC}$.	1101	Decodes instruction.
Waits for Done pulse from MMU.	xxxx	Sends Done pulse on $\overline{SPC}$.
Pulses $\overline{SPC}$ and reads Status Word from MMU.	1110	Presents Status Word (all zeroes) on bus.
Pulses $\overline{SPC}$, reading low-order word of result from MMU.	1101	Presents low-order word of referenced MMU register on bus.
Pulses $\overline{SPC}$, reading high-order word of result from MMU.	1101	Presents high-order word of referenced MMU register on bus.

TABLE 2-4. RDVAL/WRVAL Instruction Protocol

CPU Action	Status	MMU Action
Issues ID Byte of instruction, pulsing $\overline{SPC}$.	1111	Accepts ID Byte.
Sends Operation Word of instruction, pulsing $\overline{SPC}$.	1101	Decodes instruction.
Performs dummy one-byte memory read from operand's location.	1010	Translates CPU's address, using User-Mode mapping, and performs requested test on the address presented by the CPU. Aborts the CPU if the level-1 page table entry is invalid. Starts a Memory Cycle from the Translated Address if the translation is successful. Aborts on protection violations are temporarily suppressed.
Waits for Done pulse from MMU	xxxx	Sends Done pulse on $\overline{SPC}$.
Sends $\overline{SPC}$ pulse and reads Status Word from MMU; places bit 5 of this word into the F bit of the PSR register.	1110	Presents Status Word on bus, indicating in bit 5 the result of the test.

If the translation is successful the MMU will also start a dummy memory cycle from the translated address. See *Figure 2-12*. Note that, during this time the CPU will monitor the RDY line. Therefore, for proper operation, the RDY line must be kept high if the memory cycle is not performed.

The CPU then reads from the MMU a Status Word. Bit 5 of this Status Word indicates the result of the instruction:

0 if the CPU in User Mode could have made the corresponding access to the operand at the specified address (Read in RDVAL, Write in WRVAL),

1 if the CPU would have been aborted for a protection violation.

Bit 5 of the Status Word is placed by the CPU into the F bit of the PSR register, where it can be tested by subsequent instructions as a condition code.

Note: The MMU sets the R bit on RDVAL; R and M bits on WRVAL.

2.6 BUS ACCESS CONTROL

The NS32082 MMU has the capability of relinquishing its access to the bus upon rquest from a DMA device. It does this by using $\overline{HOLD}$, $\overline{HLDAI}$ and $\overline{HLDAO}$.

Details on the interconnections of these pins are provided in *Figures A-1* and *A-2* (Appendix A).

Requests for DMA are presented in parallel to both the CPU and MMU on the $\overline{HOLD}$ pin of each. The component that currently controls the bus then activates its Hold Acknowledge output to grant bus access to the requesting device. When the CPU grants the bus, the MMU passes the CPU's $\overline{HLDA}$ signal to its own $\overline{HLDAO}$ pin. When the MMU grants the bus, it does so by activating its $\overline{HLDAO}$ pin directly, and the CPU is not involved. $\overline{HLDAI}$ in this case is ignored.

Refer to *Figures 4-14, 4-15* and *4-16* for details on bus granting sequences.

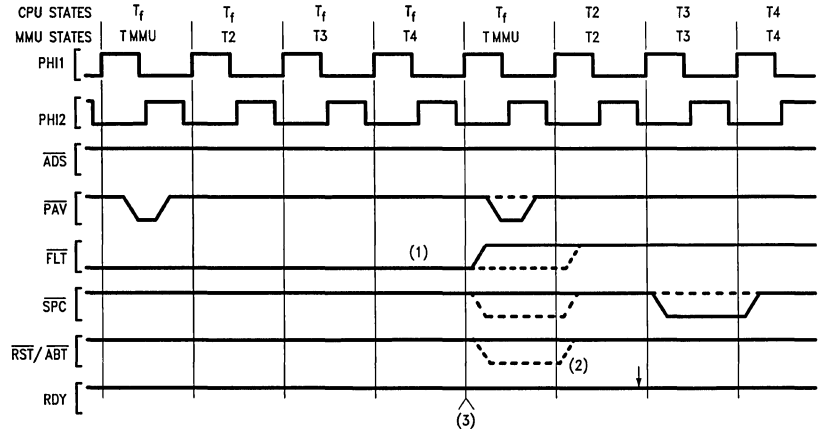
2.7 BREAKPOINTING

The MMU provides the ability to monitor references to two memory locations in real time, generating a Breakpoint trap on occurrence of any specified type of reference to either location made by a program. In addition, a Breakpoint trap may be inhibited until a specified number of such references have been performed.

Breakpoint monitoring is enabled and regulated by the setting of appropriate bits in the MSR and BPR0-1 registers. See Sections 3.5 and 3.7.

A Breakpoint trap is signalled to the CPU as either a Non-Maskable Interrupt or an Abort trap, depending on the setting of the AI bit in the MSR register.

2.0 Functional Description (Continued)



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Note 1: $\overline{FLT}$ is asserted if the translation is not in the TLB or a WRVAL instruction is executed and the M Bit is not set.

Note 2: If the Level-1 PTE is not valid, an abort is generated, $\overline{SPC}$ is issued in TMMU and $\overline{FLT}$ is deasserted in T_2.

Note 3: If a protection violation occurs or the Level-2 PTE is invalid, an Idle State is inserted here, $\overline{PAV}$ is not pulsed and $\overline{SPC}$ is pulsed during this Idle State.

FIGURE 2-12. $\overline{FLT}$ Deassertion During RDVAL/WRVAL Execution

The MSR register also indicates which breakpoint register triggered the break, and the direction (read or write) and type of memory cycle that was detected. The breakpoint address is not placed into the EIA register, as this register holds the addresses of address translation errors only. The breakpoint address is, however, available in the indicated Breakpoint register.

On occurrence of any trap generated by the MMU, including the Breakpoint trap, the BEN bit in the MSR register is immediately cleared, disabling any further Breakpoint traps.

Enabling breakpoints may cause variations in the bus timing given in the previous sections. Specifically:

1) While either breakpoint is enabled to monitor physical addresses, the MMU inserts an additional clock period into all bus cycles by asserting the $\overline{FLT}$ line for one clock. See *Figure 2-13.*

2) If the CPU initiates an instruction prefetch from a location at which a breakpoint is enabled on Execution, the MMU asserts the $\overline{FLT}$ line to the CPU, performs the memory cycle itself, and issues an edited instruction word to the CPU. See *Figure 2-14* and Section 2.7.1.

Note: Instructions which use two operands, a read-type and a write-type (e.g., MOVD 0(r1).0(r2), with the first operand valid and protected to allow user reads, and the second operand either invalid (page fault) or write protected, cause a read-type break event to occur for the first operand regardless of the outcome of the instruction. Each time the instruction is retried, the read-event is recorded. Hence, the breakpoint count register may reflect a different count than a casual assumption would lead one to. The same effect can occur on a RMW type operand with read only protection.

2.7.1 Breakpoints on Execution

The Series 32000 CPUs have an instruction prefetch which requires synchronization with execution breakpoints. In consideration of this, the MMU only issues an execution breakpoint when an instruction is prefetched with a nonsequential status code and the conditions specified in a breakpoint register are met. This guarantees that the instruction prefetch queue is empty and there are not pending instructions in the pipeline. There are three cases to consider:

Case 1: A nonsequential instruction prefetch is made to a breakpointed address.

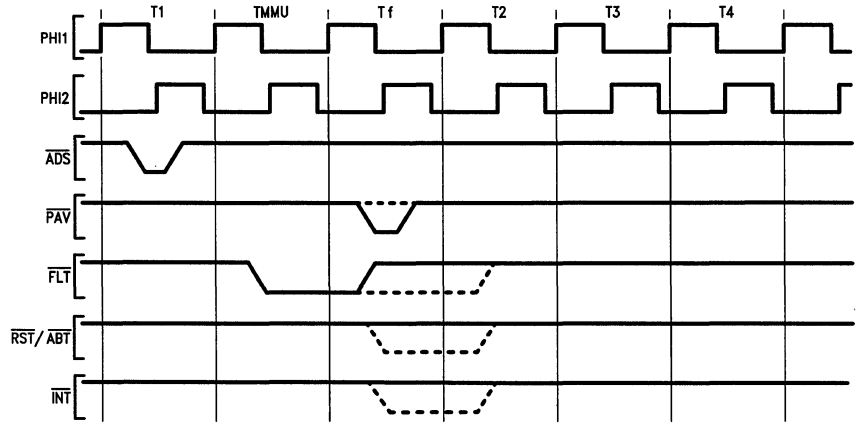
Response: The queue is necessarily empty. The breakpoint is issued.

Case 2, 3: A sequential prefetch is made to a breakpointed address OR a prefetch is made to an even address and the breakpoint is on the next odd address.

Response: In these cases, there may be instructions pending in the queue which must finish before the breakpoint is fired. Instead of putting the opcode byte (the one specified by the breakpointed address) in the queue, a DIA instruction is substituted for it. DIA is a single byte instruction which branches to itself, causing a queue flush. When the DIA executes, the breakpoint address is again issued, this time with nonsequential fetch status and the problem is reduced to case 1.

Note: Execution breakpoints cannot be used when the MMU is connected to either an NS32032 or an NS32332 CPU.

2.0 Functional Description (Continued)



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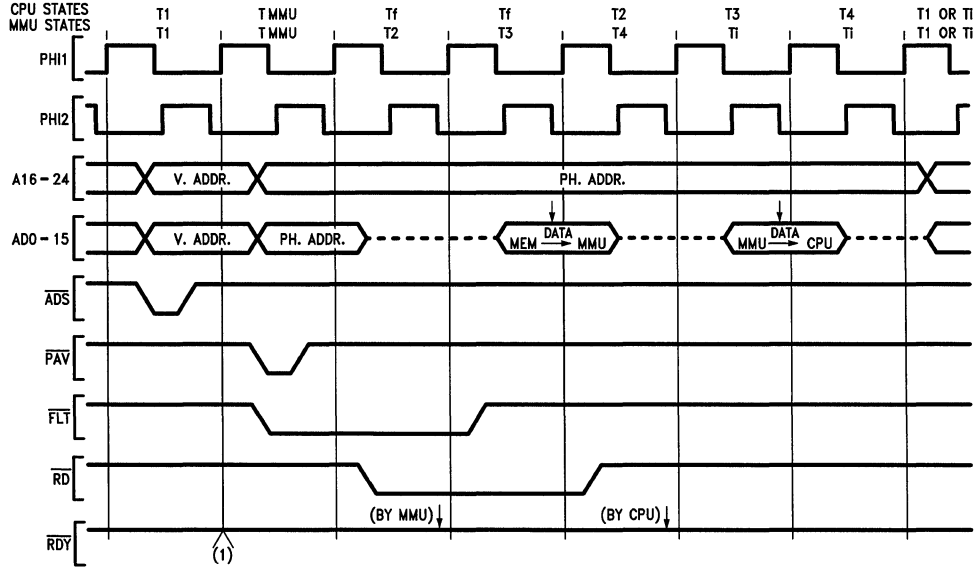
Note: If a breakpoint condition is met and abort on breakpoint is enabled, the bus cycle is aborted. In this case FLT is stretched by one clock cycle.

FIGURE 2-13. Bus Timing with Breakpoint on Physical Address Enabled



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Note 1: If a breakpoint on physical address is enabled, an extra clock cycle is inserted here.

FIGURE 2-14. Execution Breakpoint Timing; Insertion of DIA Instruction

3.0 Architectural Description

3.1 PROGRAMMING MODEL

The MMU contains a set of registers through which the CPU controls and monitors management and debugging functions. These registers are not memory-mapped. They are examined and modified by executing the Slave Processor instructions LMR (Load Memory Management Register) and SMR (Store Memory Management Register). These instructions are explained in Section 3.11, along with the other Slave Processor instructions executed by the MMU.

A brief description of the MMU registers is provided below. Details on their formats and functions are provided in the following sections.

PTB0, PTB1—Page Table Base Registers. They hold the physical memory addresses of the Page Tables referenced by the MMU for address translation. See Section 3.3.

EIA—Error/Invalidate Register. Dual-function register, used to display error addresses and also to purge cached translation information from the TLB. See Section 3.4.

BPR0, BPR1—Breakpoint Registers. Specify the conditions under which a breakpoint trap is generated. See Section 3.5.

BCNT—Breakpoint Counter Register. 24-bit counter used to count BPR0 events. Allows the breakpoint trap from the BPR0 register to be inhibited until a specified number of events have occurred. See Section 3.6.

MSR—Memory Management Status Register. Contains basic control and status fields for all MMU functions. See Section 3.7.

3.2 MEMORY MANAGEMENT FUNCTIONS

The NS32082 uses sets of tables in physical memory (the "Page Tables") to define the mapping from virtual to physical addresses. These tables are found by the MMU using one of its two Page Table Base registers: PTB0 or PTB1. Which register is used depends on the currently selected address space. See Section 3.2.2.

3.2.1. Page Table Structure

The page tables are arranged in a two-level structure, as shown in *Figure 3-1*. Each of the MMU's PTBn registers may point to a Level-1 page table. Each entry of the Level-1 page table may in turn point to a Level-2 page table. Each Level-2 page table entry contains translation information for one page of the virtual space.

The Level-1 page table must remain in physical memory while the PTBn register contains its address and translation is enabled. Level-2 Page Tables need not reside in physical memory permanently, but may be swapped into physical memory on demand as is done with the pages of the virtual space.

The Level-1 Page Table contains 256 32-bit Page Table Entries (PTE'S) and therefore occupies 1 Kbyte. Each entry of the Level-1 Page Table contains fields used to construct the physical base address of a Level-2 Page Table. These fields are a 15-bit PFN field, providing bits 9-23 of the physical address, and an MS bit providing bit 24. The remaining bits (0–8) are assumed zero, placing a Level-2 Page Table always on a 512-byte (page) boundary.

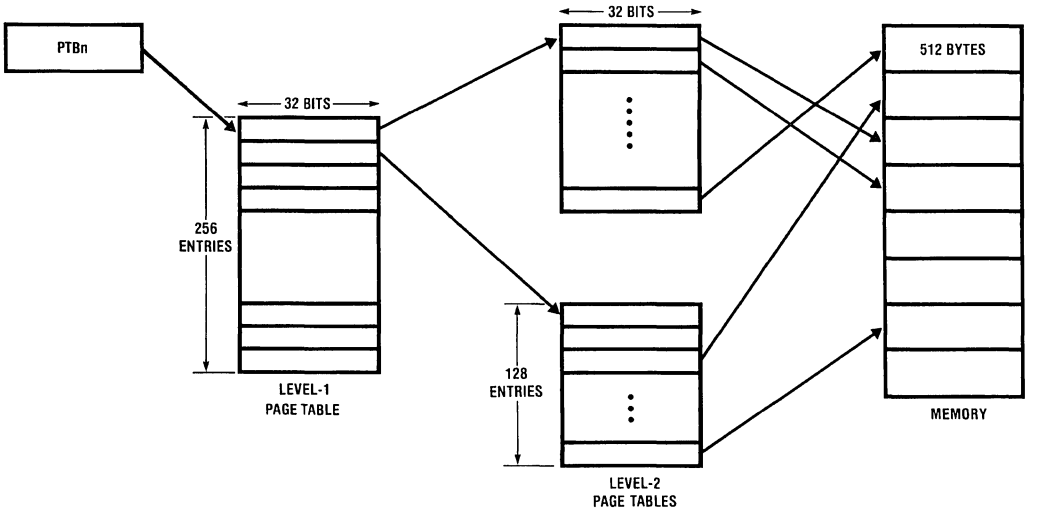

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FIGURE 3-1. Two-Level Page Tables

3.0 Architectural Description (Continued)

Level-2 Page Tables contain 128 32-bit Page Table entries, and so occupy 512 bytes (1 page). Each Level-2 Page Table Entry points to a final 512-byte physical page frame. In other words, its PFN and MS fields provide the Page Frame Number portion (bits 9-24) of the translated address (*Figure 3-3*). The OFFSET field of the translated address is taken directly from the corresponding field of the virtual address.

3.2.2 Virtual Address Spaces

When the Dual Space option is selected for address translation in the MSR (Sec. 3.7) the MMU uses two maps: one for translating addresses presented to it in Supervisor Mode and another for User Mode addresses. Each map is referenced by the MMU using one of the two Page Table Base registers: PTB0 or PTB1. The MMU determines the CPU's current mode by monitoring the state of the U/$\overline{S}$ pin and applying the following rules.

1) While the CPU is in Supervisor Mode (U/$\overline{S}$ pin = 0), the CPU is said to be presenting addresses belonging to Address Space 0, and the MMU uses the PTB0 register as its reference for looking up translations from memory.
2) While the CPU is in User Mode (U/$\overline{S}$ pin = 1), and the MSR DS bit is set to enable Dual Space translation, the CPU is said to be presenting addresses belonging to Address Space 1, and the MMU uses the PTB1 register to look up translations.
3) If Dual Space translation is not selected in the MSR, there is no Address Space 1, and all addresses presented in both Supervisor and User modes are considered by the MMU to be in Address Space 0. The privilege level of the CPU is used then only for access level checking.

Note: When the CPU executes a Dual-Space Move instruction (MOVUSi or MOVSUi), it temporarily enters User Mode by switching the state of the U/$\overline{S}$ pin. Accesses made by the CPU during this time are treated by the MMU as User-Mode accesses for both mapping and access level checking. It is possible, however, to force the MMU to assume Supervisor-Mode privilege on such accesses by setting the Access Override (AO) bit in the MSR (Sec. 3.7).

3.2.3 Page Table Entry Formats

Figure 3-2 shows the formats of Level-1 and Level-2 Page Table Entries (PTE's). Their formats are identical except for the "M" bit, which appears only in a Level-2 PTE.

The bits are defined as follows:

V Valid. The V bit is set and cleared only by software.

V=1=> The PTE is valid and may be used for translation by the MMU.

V=0=> The PTE does not represent a valid translation. Any attempt to use this PTE will cause the MMU to generate an Abort trap. While V=0, the operating system may use all other bits except the PL field for any desired function.

PL Protection Level. This two-bit field establishes the types of accesses permitted for the page in both User Mode and Supervisor Mode, as shown in Table 3-1.

The PL field is modified only by software. In a Level-1 PTE, it limits the maximum access level allowed for all pages mapped through that PTE.

TABLE 3-1. Access Protection Levels

Mode	U/$\overline{S}$	Protection Level Bits (PL)			
		00	01	10	11
User	1	no access	no access	read only	full access
Supervisor	0	read only	full access	full access	full access

R Referenced. This is a status bit, set by the MMU and cleared by the operating system, that indicates whether the page mapped by this PTE has been referenced within a period of time determined by the operating system. It is intended to assist in implementing memory allocation strategies. In a Level-1 PTE, the R bit indicates only that the Level-2 Page Table has been referenced for a translation, without necessarily implying that the translation was successful. In a Level-2 PTE, it indicates that the page mapped by the PTE has been successfully referenced.

R=1=> The page has been referenced since the R bit was last cleared.

R=0=> The page has not been referenced since the R bit was last cleared.

Note: The RDVAL and WRVAL instructions set the Level-1 and Level-2 bits for the page whose protection level is tested. See Sections 2.5.2 and 3.11.

M Modified. This is a status bit, set by the MMU whenever a write cycle is successfully performed to the page mapped by this PTE. It is initialized to zero by the operating system when the page is brought into physical memory.

M=1=> The page has been modified since it was last brought into physical memory.

M=0=> The page has not been modified since it was last brought into physical memory.

In Level-1 Page Table Entries, this bit position is undefined, and is altered in an undefined manner by the MMU while the V bit is 1.

Note: The WRVAL instruction sets the M bit for the page whose protection level is tested. See Sections 2.5.2 and 3.11.

NSC Reserved. These bits are ignored by the MMU and their values are not changed.

They are reserved by National, and therefore should not be used by the user software.

USR User bits. These bits are ignored by the MMU and their values are not changed.

They can be used by the user software.

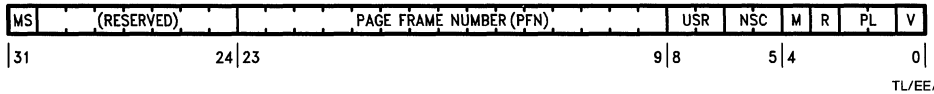

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FIGURE 3-2. A Page Table Entry

3.0 Architectural Description (Continued)

PFN Page Frame Number. This 15-bit field provides bits 9-23 of the Page Frame Number of the physical address. See *Figure 3-3.*

MS Memory System. This bit represents the most significant bit of the physical address, and is presented by the MMU on pin A24. This bit is treated by the MMU no differently than any other physical address bit, and can be used to implement a 32-Mbyte physical addressing space if desired.

3.2.4 Physical Address Generation

When a virtual address is presented to the MMU by the CPU and the translation information is not in the TLB, the MMU performs a page table lookup in order to generate the physical address.

The Page Table structure is traversed by the MMU using fields taken from the virtual address. This sequence is diagrammed in *Figure 3-3.*

Bits 9–23 of the virtual address hold the 15-bit Page Number, which in the course of the translation is replaced with the 16-bit Page Frame Number of the physical address. The virtual Page Number field is further divided into two fields, INDEX 1 and INDEX 2.

Bits 0–8 constitute the OFFSET field, which identifies a byte's position within the accessed page. Since the byte position within a page does not change with translation, this value is not used, and is simply echoed by the MMU as bits 0–8 of the final physical address.

The 8-bit INDEX 1 field of the virtual address is used as an index into the Level-1 Page Table, selecting one of its 256 entries. The address of the entry is computed by adding INDEX 1 (scaled by 4) to the contents of the current Page Table Base register. The PFN and MS fields of that entry give the base address of the selected Level-2 Page Table.

The INDEX 2 field of the virtual address (7 bits) is used as the index into the Level-2 Page Table, by adding it (scaled by 4) to the base address taken from the Level-1 Page Table Entry. The PFN and MS fields of the selected entry provide the entire Page Frame Number of the translated address.

The offset field of the virtual address is then appended to this frame number to generate the final physical address.

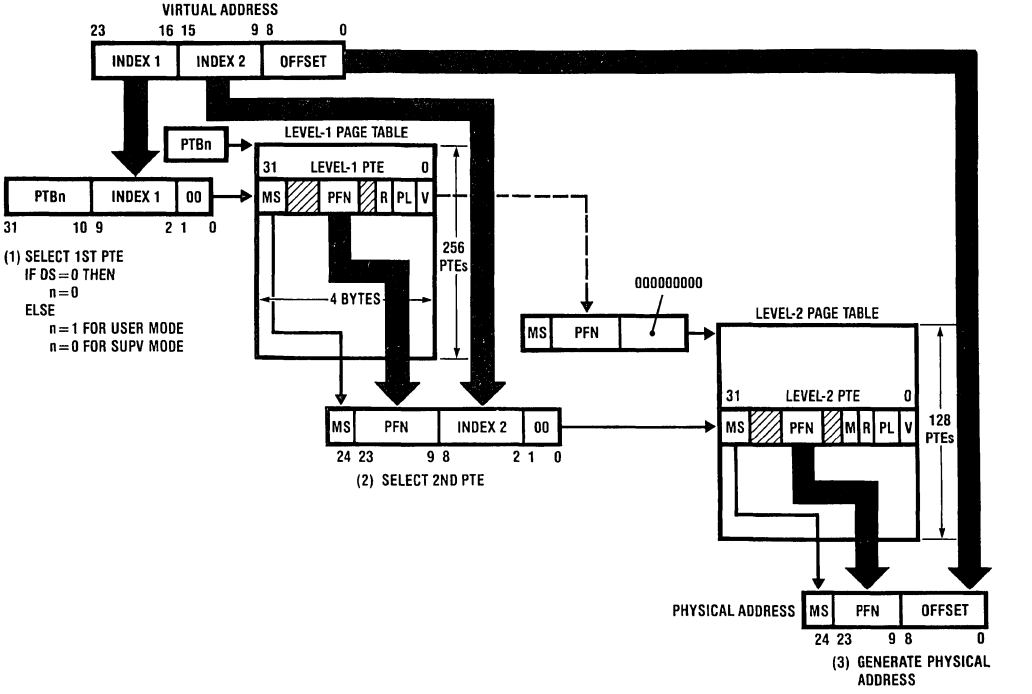

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FIGURE 3-3. Virtual to Physical Address Translation

3.0 Architectural Description (Continued)

3.3 PAGE TABLE BASE REGISTERS (PTB0, PTB1)

The PTBn registers hold the physical addresses of the Level-1 Page Tables.

The format of these registers is shown in *Figure 3-4.* The least-significant 10 bits are permanently zero, so that each register always points to a 1 Kbyte boundary in memory.

The PTBn registers may be loaded or stored using the MMU Slave Processor instructions LMR and SMR (Section 3.11).

3.4 ERROR/INVALIDATE ADDRESS REGISTER (EIA)

The Error/Invalidate Address register is a dual-purpose register.

1) When it is read using the SMR instruction, it presents the virtual address which last generated an address translation error.
2) When a virtual address is written into it using the LMR instruction, the translation for that virtual address is purged, if present, from the TLB. This must be done whenever a Page Table Entry has been changed in memory, since the TLB might otherwise contain an incorrect translation value.

The format of the EIA register is shown in *Figure 3-5.* When a translation error occurs, the cause of the error is reported by the MMU in the appropriate fields of the MSR register (Section 3.7). The ADDRESS field of the EIA register holds the virtual address at which the error occurred, and the AS bit indicates the address space that was in use.

In writing a virtual address to the EIA register, the virtual address is specified in the low-order 24 bits, and the AS bit specifies the address space. A TLB entry is purged only if it matches both the ADDRESS and AS fields.

Another technique for purging TLB entries is to load a PTBn register. This automatically purges all entries associated with the addressing space mapped by that register. Turning off translation (clearing the MSR TU and/or TS bits) does not purge any entries from the TLB.

3.5 BREAKPOINT REGISTERS (BPR0, BPR1)

The Breakpoint registers BPR0 and BPR1 specify the addresses and conditions on which a Breakpoint trap will be generated. They are each 32 bits in length and have the format shown in *Figure 3-6.* All implemented bits of BPR0 and BPR1 are readable and writable.

Bits 0 through 23 and bit 31 (AS) specify the breakpoint address. This address may be either virtual or physical, as specified in the VP bit.

Bits 24 and 25 are not implemented. Bit 26 (CE) is not implemented in register BPR1.

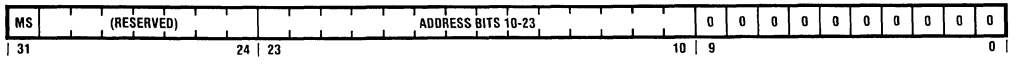

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FIGURE 3-4. Page Table Base Registers (PTB0, PTB1)

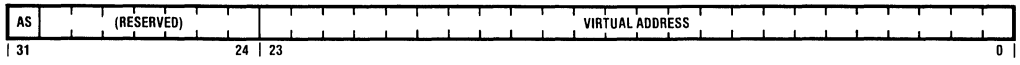

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FIGURE 3-5. EIA Register

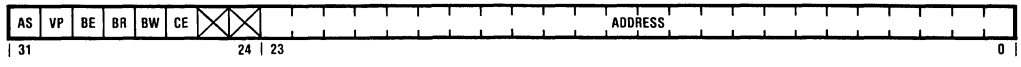

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FIGURE 3-6. Breakpoint Registers (BPR0, BPR1)

3.0 Architectural Description (Continued)

Bits 26 through 30 specify the breakpoint conditions. Breakpoint conditions define how the breakpoint address is compared and which conditions permit a break to be generated. A Breakpoint register can be selectively disabled by setting all of these bits to zero.

AS Address Space. This bit depends on the setting of the VP bit. For virtual addresses, this bit contains the AS (Address Space) qualifier of the virtual address (Section 3.2.2). For physical addresses, this bit contains the MS (Memory System) bit of the physical address.

VP Virtual/Physical. If VP is 0, the breakpoint address is compared against each referenced virtual address. If VP is 1, the breakpoint address is compared against each physical address that is referenced by the CPU (i.e. after translation).

BE Break on Execution. If BE is 1, a break is generated immediately before the instruction at the breakpoint address is executed. While this option is enabled, the breakpoint address must be the address of the first byte of an instruction. If BE is 0, this condition is disabled.

Note: This option cannot be used in systems based on any CPU with a 32-bit wide bus.

The BE bit should only be set when the CPU has a 16-bit bus (i.e. NS32016, NS32C016). In other systems, use instead the BPT instruction placed in memory, to signal a break.

BR Break on Read. If BR is 1, a break is generated when data is read from the breakpoint address. Instruction fetches do not trigger a Read breakpoint. If BR is 0, this condition is disabled.

BW Break on Write. If BW is 1, a break is generated when data is written to the breakpoint address or when data is read from the breakpoint address as the first part of a read-modify-write access. If BW is 0, this condition is disabled.

CE Counter Enable. This bit is implemented only in the BPR0 register. If CE is 1, no break is generated unless the Breakpoint Count register (BCNT, see below) is zero. The BCNT register decrements when the condition for the breakpoint in register BPR0 is met and the BCNT register is not already zero. If CE is 0, the BCNT register is disabled, and breaks from BPR0 occur immediately.

Note 1: The bits BR, BW and CE should not all be set. The counting performed by the MMU becomes inaccurate, and in Abort Mode (MSR AI bit set), it can trap a program in such a way as to make it impossible to retry the breakpointed instruction correctly.

Note 2: An execution breakpoint should not be counted (BE and CE bits both set) if it is placed at an address that is the destination of a branch, or if it follows a queue-flushing instruction. See Table 3-2. The counting performed by the MMU will be inaccurate if interrupts occur during the fetch of that address.

TABLE 3-2. Instructions Causing Non-Sequential Fetches

Branch	
ACBi	Add, Compare and Branch: unless result is zero
BR	Branch (Unconditional)
BSR	Branch to Subroutine
Bcond	Branch (Conditional): only if condition is met
CASEi	Case Branch
CXP	Call External Procedure
CXPD	Call External Procedure with Descriptor
DIA	Diagnose
JSR	Jump to Subroutine
JUMP	Jump
RET	Return from Subroutine
RXP	Return from External Procedure
BPT	Breakpoint Trap
FLAG	Trap on Flag
RETI	Return from Interrupt: if MSR loaded properly by supervisor
RETT	Return from Trap: if MSR loaded properly by supervisor
SVC	Supervisor Call

Also all traps or interrupts not generated by the MMU.

Branch to Following Instruction	
BICPSRi	Bit Clear in PSR
BISPSRi	Bit Set in PSR
LMR	Load Memory Management Register
LPRi	Load Processor Register: unless UPSR is the register specified
MOVSUi	Move Value from Supervisor to User Space
MOVUSi	Move Value from User to Supervisor Space
WAIT	Wait: fetches next instruction before waiting

3.6 BREAKPOINT COUNT REGISTER (BCNT)

The Breakpoint Count register (BCNT) permits the user to specify the number of breakpoint conditions given by register BPR0 that should be ignored before generating a Breakpoint trap. The BCNT register is 32 bits in length, containing a counter in its low-order 24 bits, as shown in *Figure 3-7.* The high-order eight bits are not used.

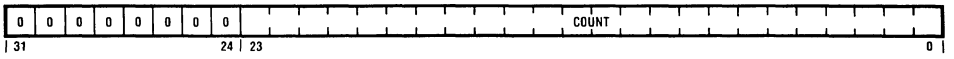

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FIGURE 3-7. Breakpoint Count Register (BCNT)

3.0 Architectural Description (Continued)

The BCNT register affects the generation of Breakpoint traps only when it is enabled by the CE bit in the BPR0 register. When the BPR0 breakpoint condition is encountered, and the BPR0 CE bit is 1, the contents of the BCNT register are checked against zero. If the BCNT contents are zero, a breakpoint trap is generated. If the contents are not equal to zero, no breakpoint trap is generated and the BCNT register is decremented by 1.

If the CE bit in the BPR0 register is 0, the BCNT register is ignored and the BPR0 condition breaks the program execution regardless of the BCNT register's contents. The BCNT register contents are unaffected.

3.7 MEMORY MANAGEMENT STATUS REGISTER (MSR)

The Memory Management Status Register (MSR) provides overall control and status fields for both address translation and debugging functions. The format of the MSR register is shown in *Figure 3-8*.

The MSR fields relevant to either of the above functions are described in the following sub-sections.

3.7.1 MSR Fields for Address Translation.

Control Functions

The address translation control bits in the MSR, ad exception of the R bit, are both readable (using the SMR instruction) and writable (using LMR).

R Reset. When read, this bit's contents are undefined. Whenever a "1" is written into it, MSR status fields TE, B, TET, ED, BD, EST and BST are cleared to all zeroes. (The BN bit is not affected.)

TU Translate User-Mode Addresses. While this bit is "1", the MMU translates all addresses presented while the CPU is in User Mode. While it is "0", the MMU echoes all User-Mode virtual addresses without performing translation or access level checking. This bit is cleared by a hardware Reset.

Note: Altering the TU bit has no effect on the contents of the TLB.

TS Translate Supervisor-Mode Addresses. While this bit is "1", the MMU translates all addresses presented while the CPU is in Supervisor Mode. While it is "0", the MMU echoes all Supervisor-Mode virtual addresses without translation or access level checking. This bit is cleared by a hardware Reset.

Note: Altering the TS bit has no effect on the contents of the TLB.

DS Dual-Space Translation. While this bit is "1", Supervisor Mode addresses and User Mode addresses are translated independently of each other, using separate mappings. While it is "0", both Supervisor Mode addresses and User Mode addresses are translated using the same mapping. See Section 3.2.2.

AO Access Level Override. This bit may be set to temporarily cause User Mode accesses to be given Supervisor Mode privilege. See Section 3.10.

Status Fields

The MSR status fields may be read using the MSR instruction, but are not writable. Instead, all status fields (except the BN bit) may be cleared by loading a "1" into the R bit using the LMR instruction.

TE Translation Error. This bit is set by the MMU to indicate that an address translation error has occurred. This bit is cleared by a hardware reset.

TET Translation Error Type. This three-bit field shows the reason(s) for the last address translation error reported by the MMU. The format of the TET field is shown below.

IL2	IL1	PL

PL Protection Level error. The access attempted by the CPU was not allowed by the protection level assigned to the page it attempted to access (forbidden by either of the Page Table Entry PL fields).

IL1 Invalid Level 1. The Level-1 Page Table Entry was invalid (V bit = 0).

IL2 Invalid Level 2. The Level-2 Page Table Entry was invalid (V bit = 0).

These error indications are not mutually exclusive. A protection level error and an invalid translation error can be reported simultaneously by the MMU.

ED Error Direction. This bit indicates the direction of the transfer that the CPU was attempting on the most recent address translation error.

ED = 0 => Write cycle.

ED = 1 => Read cycle.

EST Error Status. This 3-bit field is set on an address translation error to the low-order three bits of the CPU status bus. Combinations appearing in this field are summarized below.

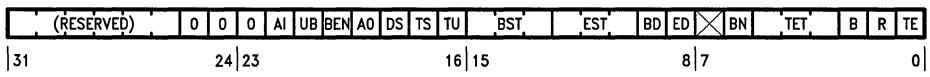
000 Sequential instruction fetch

001 Non-sequential instruction fetch

010 Operand transfer (read or write)

011 The Read action of a read-modify-write transfer (operands of access class "rmw" only: See the Series 32000 Instruction Set Reference Manual for further details).

100 A read transfer which is part of an effective address calculation (Memory Relative or External mode)



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Note: In some Series 32000 documentation, the bits TE, R and B are jointly referenced with the keyword "ERC".

FIGURE 3-8. Memory Management Status Register (MSR)

3.0 Architectural Description (Continued)

3.7.2 MSR Fields for Debugging

Control Functions

Breakpoint control bits in the MSR are both readable (using the SMR instruction) and writable (using LMR).

BEN Breakpoint Enable. Setting this bit enables both Breakpoint Registers (BPR0, BPR1) to monitor CPU activity. This bit is cleared by a hardware reset or whenever a Breakpoint trap or an address translation error occurs. If only one breakpoint register must be enabled, the other register should be disabled by clearing all of its control bits (bits 26–31) to zeroes.

Note: When the BEN bit is set (using the LMR instruction), the MMU enables breakpoints only after two non-sequential instruction fetch cycles have been completed by the CPU. See Section 3.9.

UB User-Only Breakpointing. When this bit is set in conjunction with the BEN bit, it limits the Breakpoint Registers to monitor addresses only while the CPU is in User Mode.

AI Abort/Interrupt. This bit selects the action taken by the MMU on a breakpoint. While AI is "0" the MMU generates a pulse on the $\overline{INT}$ pin (this can be used to generate a non-maskable interrupt). While AI is "1" the MMU generates an Abort pulse instead.

Status Fields

The MSR status fields may be read using the SMR instruction, but are not writable. Instead, all status fields (except the BN bit) may be cleared by loading a "1" into the R bit using the LMR instruction. See Section 3.7.1.

B Break. This bit is set to indicate that a breakpoint trap has been generated by the MMU.

BN Breakpoint Number. The BN bit contains the register number for the most recent breakpoint trap generated by the MMU. If BN is 1, the breakpoint was triggered by the BPR1 register. If BN is 0, the breakpoint was triggered by the BPR0 register. If both registers trigger a breakpoint simultaneously, the BN bit is set to 1.

BD Break Direction. This bit indicates the direction of the transfer that the CPU was attempting on the access that triggered the most recent breakpoint trap. It is loaded from the complement of the $\overline{DDIN}$ pin.

BD = 0 => Write cycle.

BD = 1 => Read cycle.

BST Breakpoint Status. This 3-bit field is loaded on a Breakpoint trap from the low-order three bits of the CPU status bus. Combinations appearing in this field are summarized below.

000 No break has occurred since the field was last reset.

001 Instruction fetch

010 Operand transfer (read or write)

011 The Read action of a read-modify-write transfer (operands of access class "rmw" only: See the Series 32000 Instruction Set Reference Manual for further details).

100 A read transfer which is part of an effective address calculation (Memory Relative or External mode)

Note: The BST field encodings 000 and 001 differ from those of the EST field (Section 3.7.1) because the MMU inserts a DIA instruction into the instruction stream in implementing Execution breakpoints (Section 2.7.1). One side effect of this is that a breakpoint trap is never triggered directly by a sequential instruction fetch cycle.

3.8 TRANSLATION LOOKASIDE BUFFER (TLB)

The Translation Lookaside Buffer is an on-chip fully associative memory. It provides direct virtual to physical mapping for the 32 most recently used pages, requiring only one clock period to perform the address translation.

The efficiency of the MMU is greatly increased by the TLB, which bypasses the much longer Page Table lookup in over 97% of the accesses made by the CPU.

Entries in the TLB are allocated and replaced by the MMU itself; the operating system is not involved. The TLB entries cannot be read or written by software; however, they can be purged from it under program control.

Figure 3-9 models the TLB. Information is placed into the TLB whenever the MMU performs a lookup from the Page Tables in memory. If the retrieved mapping is valid (V = 1 in both levels of the Page Tables), and the access attempted is permitted by the protection level, an entry of the TLB is loaded from the information retrieved from memory. The recipient entry is selected by an on-chip circuit that implements a Least-Recently-Used (LRU) algorithm. The MMU places the virtual page number (15 bits) and the Address Space qualifier bit into the Tag field of the TLB entry.

The Value portion of the entry is loaded from the Page Tables as follows:

The Translation field (16 bits) is loaded from the MS bit and PFN field of the Level-2 Page Table Entry.

The M bit is loaded from the Level-2 Page Table Entry.

The PL field (2 bits) is loaded to reflect the net protection level imposed by the PL fields of the Level-1 and Level-2 Page Table Entries.

(Not shown in the figure are additional bits associated with each TLB entry which flag it as full or empty, and which select it as the recipient when a Page Table lookup is performed.)

When a virtual address is presented to the MMU for translation, the high-order 15 bits (page number) and the Address Space qualifier are compared associatively to the corresponding fields in all entries of the TLB. When the Tag portion of a TLB entry completely matches the input values, the Value portion is produced as output. If the protection level is not violated, and the M bit does not need to be changed, then the physical address Page Frame number is output in the next clock cycle. If the protection level is violated, the MMU instead activates the Abort output. If no TLB entry matches, or if the matching entry's M bit needs to be changed, the MMU performs a page-table lookup from memory.

Note that for a translation to be loaded into the TLB it is necessary that the Level-1 and Level-2 Page Table Entries be valid (V bit = 1). Also, it is guaranteed that in

3.0 Architectural Description (Continued)

the process of loading a TLB entry (during a Page Table lookup) the Level-1 and Level-2 R bits will be set in memory if they were not already set. For these reasons, there is no need to replicate either the V bit or the R bit in the TLB entries.

Whenever a Page Table Entry in memory is altered by software, it is necessary to purge any matching entry from the TLB, otherwise the MMU would be translating the corresponding addresses according to obsolete information. TLB entries may be selectively purged by writing a virtual address to the EIA register using the LMR instruction. The TLB entry (if any) that matches that virtual address is then purged, and its space is made available for another translation. Purging is also performed by the MMU whenever an address space is remapped by altering the contents of the PTB0 or PTB1 register. When this is done, the MMU purges all the TLB entries corresponding to the address space mapped by that register. Turning translation on or off (via the MSR TU and TS bits) does not affect the contents of the TLB.

Note: If the value in the PTB0 register must be changed, it is strongly recommended that the translation be disabled before loading the new value, otherwise the purge performed may be incomplete. This is due to instruction prefetches and/or memory read cycles occurring during the LMR instruction which may restore TLB entries from the old map.

3.9 ENTRY/RE-ENTRY INTO PROGRAMS UNDER DEBUGGING

Whenever the MSR is written, breakpoints are disabled. After two non-sequential instruction fetch cycles have completed, they are again enabled if the new BEN bit value is '1'. The recommended sequence for entering a program under test is:

```
LMR     MSR, New_Value
RETT    n       ; or RETI
```

executed with interrupts disabled (CPU PSR I bit off).

This feature allows a debugger or monitor program to return control to a program being debugged without the risk of a false breakpoint trap being triggered during the return.

The LMR instruction performs the first non-sequential fetch cycle, in effect branching to the next sequential instruction. The RETT (or RETI) instruction performs the second non-sequential fetch as its last memory reference, branching to the first (next) instruction of the program under debug. The non-sequential fetch caused by the RETT instruction, which might not have occurred otherwise, is not monitored.

3.10 ADDRESS TRANSLATION ALGORITHM

The MMU either translates the 24-bit virtual address to a 25-bit physical address or reports a translation error. This process is described algorithmically in the following pages. See also *Figure 3-3*.

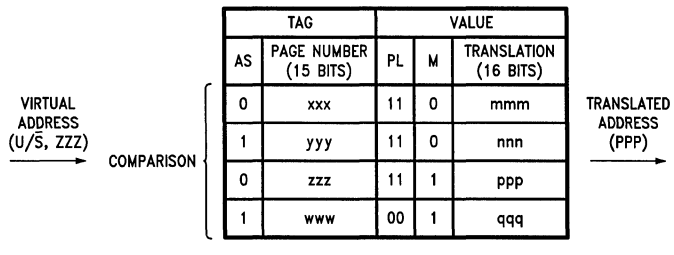

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FIGURE 3-9. TLB Model

MMU Page Table Lookup and Access Validation Algorithm

```
Legend:
x = y           x is assigned the value y
x == y          Comparison expression, true if x is equal to y
x AND y         Boolean AND expression, true only if assertions x and y are both true
x OR y          Boolean inclusive OR expression, true if either of assertions x and y is true
;               Delimiter marking end of statement
{ . . . }       Delimiters enclosing a statement block
item(i)         Bit number i of structure "item"
item(i:j)       The field from bit number i through bit number j of structure "item"
item.x          The bit or field named "x" in structure "item"
DONE            Successful end of translation; MMU provides translated address
ABORT           Unsuccessful end of translation; MMU aborts CPU access
This algorithm represents for all cases a valid definition of address translation.
Bus activity implied here occurs only if the TLB does not contain the mapping,
or if the reference requires that the MMU alter the M bit of the Page Table Entry.
Otherwise, the MMU provides the translated address in one clock period.
Input (from CPU):
     U (1 if U/S is high)
     W (1 if DDIN input is high)
     VA  Virtual address consisting of:
        INDEX_1 (from pins A23-A16)
        INDEX_2 (from pins AD15-AD9)
        OFFSET  (from pins AD8-AD0)
     ACCESS_LEVEL       The access level of a reference is a 2-bit value synthesized by the MMU from CPU status:
        bit 1 = U AND NOT MSR.A0  (U from U/S input pin)
        bit 0 = 1 for Write cycle, or Read cycle of an "rmw" class operand access
                0 otherwise.

Output:
     PA Physical Address on pins A24-A16, AD15-AD0;
        or
     Abort pulse on RST/ABT pin.
Uses:
     MSR        Status Register:
                        fields TU, TS and DS
```


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MMU Page Table Lookup and Access Validation Algorithm (Continued)

```
     PTB0       Page Table Base Register 0
     PTB1       Page Table Base Register 1
     PTE_1      Level-1 Page Table Entry:
                        fields PFN, PL, V, R and MS
     PTEP_1     Pointer, holding address of PTE_1
     PTE_2      Level-2 Page Table Entry:
                        fields PFN, PL, V, M, R and MS
     PTEP_2     Pointer, holding address of PTE_2
IF ( (MSR.TU == 0) AND (U == 1) )  OR  ( (MSR.TS == 0) AND (U ==0) )  If translation not enabled then echo
     THEN  {  PA(0:23) = VA(0:23) ; PA(24) = 0 ; DONE  }  ;                  virtual address as physical address.

IF (MSR.DS == 1) AND (U == 1)                                          If Dual Space mode and CPU in User Mode
   THEN {  PTEP_1(24) = PTB1.MS ; PTEP_1(23:10) = PTB1(23:10) ;             then form Level-1 PTE address
           PTEP_1(9:2) = VA.INDEX_1 ; PTEP_1(1:0)=0  }                             from PTB1 register,
   ELSE {  PTEP_1(24) = PTB0.MS ; PTEP_1(23:10) = PTB0(23:10) ;             else form Level-1 PTE address
           PTEP_1(9:2) = VA.INDEX_1; PTEP_1(1:0) = 0                               from PTB0 register.
        } ;

                                                  - - - LEVEL 1 PAGE TABLE LOOKUP - - -

IF ( ACCESS_LEVEL > PTE_1.PL ) OR (PTE_1.V == 0)                       If protection violation or invalid Level-2 page
   THEN ABORT ;                                                            table then abort the access.

IF PTE_1.R == 0 THEN PTE_1.R = 1 ;                                     Otherwise, set Reference bit if not already set,
PTE_1(4) = (undefined value);                                                  (the M bit position may be garbaged)

PTEP_2(24) = PTE_1.MS ; PTEP_2(23:9) = PTE_1.PFN ;                             and form Level-2 PTE address.
PTEP_2(8:2) = VA.INDEX_2 ; PTEP_2(1:0) = 0 ;

                                                  - - - LEVEL 2 PAGE TABLE LOOKUP - - -

IF ( ACCESS_LEVEL > PTE_2.PL ) OR ( PTE_2.V ==0 )                            If protection violation or invalid page
   THEN ABORT ;                                                              then abort the access.

IF PTE_2.R == 0 THEN PTE_2.R == 1 ;                                    Otherwise, set Referenced bit if not already set,
IF ( W == 1) AND ( PTE_2.M == 0 ) THEN PTE_2.M = 1 ;                         if Write cycle set Modified bit if not
                                                                                  already set,
PA(24) = PTE_2.MS ; PA(23:9) = PTE_2.PFN ; PA(8:0) = VA.OFFSET ;                  and generate physical address.
DONE ;
```

3.0 Architectural Description (Continued)

3.11 INSTRUCTION SET

Four instructions of the Series 32000 instruction set are executed cooperatively by the CPU and MMU. These are:

LMR	Load Memory Management Register
SMR	Store Memory Management Register
RDVAL	Validate Address for Reading
WRVAL	Validate Address for Writing

The format of the MMU slave instructions is shown in *Figure 3-10*. Table 3-3 shows the encodings of the "short" field for selecting the various MMU internal registers.

TABLE 3-3. "Short" Field Encodings

"Short" Field	Register
0000	BPR0
0001	BPR1
1010	MSR
1011	BCNT
1100	PTB0
1101	PTB1
1111	EIA

Note: All other codes are illegal. They will cause unpredictable registers to be selected if used in an instruction.

For reasons of system security, all MMU instructions are privileged, and the CPU does not issue them to the MMU in User Mode. Any such attempt made by a User-Mode program generates the Illegal Operation trap, Trap (ILL). In addition, the CPU will not issue MMU instructions unless its CFG register's M bit has been set to validate the MMU instruction set. If this has not been done, MMU instructions are not recognized by the CPU, and an Undefined Instruction trap, Trap (UND), results.

The LMR and SMR instructions load and store MMU registers as 32-bit quantities to and from any general operand (including CPU General-Purpose Registers).

The RDVAL and WRVAL instructions probe a memory address and determine whether its current protection level would allow reading or writing, respectively, if the CPU were in User Mode. Instead of triggering an Abort trap, these instructions have the effect of setting the CPU PSR F bit if the type of access being tested for would be illegal. The PSR F bit can then be tested as a condition code.

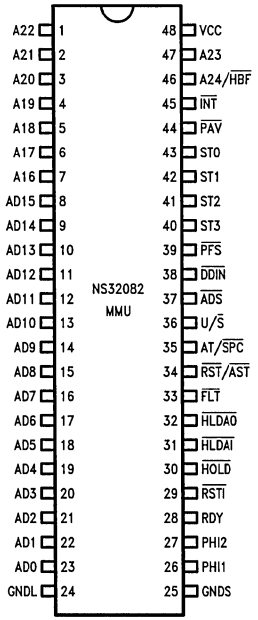
Note: The Series 32000 Dual-Space Move instructions (MOVSUi and MOVUSi), although they involve memory management action, are not Slave Processor instructions. The CPU implements them by switching the state of its U/$\overline{S}$ pin at appropriate times to select the desired mapping and protection from the MMU.

For full architectural details of these instructions, see the Series 32000 Instruction Set Reference Manual.

4.0 Device Specifications

4.1 NS32082 PIN DESCRIPTIONS

The following is a brief description of all NS32082 pins. The descriptions reference portions of the Functional Description, Section 2.0.



TL/EE/8692-28

Top View

Order Number NS16082D
See NS Package Number D48A

FIGURE 4-1. Dual-In-Line Package Connection Diagram

4.1.1 Supplies

Power (V_{CC}): +5V positive supply. Section 2.1.

Logic Ground (GNDL): Ground reference for on-chip logic. Section 2.1.

Buffer Ground (GNDB): Ground reference for on-chip drivers connected to output pins. Section 2.1.

4.1.2 Input Signals

Clocks (PHI1, PHI2): Two-phase clocking signals. Section 2.2.

Ready (RDY): Active high. Used by slow memories to extend MMU originated memory cycles. Section 2.4.4.

Hold Request ($\overline{HOLD}$): Active low. Causes a release of the bus for DMA or multiprocessing purposes. Section 2.6.

Hold Acknowledge in ($\overline{HLDAI}$): Active low. Applied by the CPU in response to $\overline{HOLD}$ input, indicating that the CPU has released the bus for DMA or multiprocessing purposes. Section 2.6.

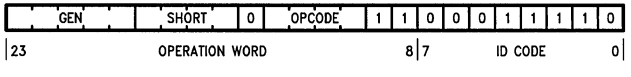


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FIGURE 3-10. MMU Slave Instruction Format

4.0 Device Specifications (Continued)

Reset Input ($\overline{RSTI}$): Active low. System reset. Section 2.3.

Status Lines (ST0–ST3): Status code input from the CPU. Active from T4 of previous bus cycle through T3 of current bus cycle. Section 2.4.

Program Flow Status ($\overline{PFS}$): Active low. Pulse issued by the CPU at the beginning of each instruction.

User/Supervisor Mode (U/$\overline{S}$): This signal is provided by the CPU. It is used by the MMU for protection and for selecting the address space (in dual address space mode only). Section 2.4.

Address Strobe Input ($\overline{ADS}$): Active low. Pulse indicating that a virtual address is present on the bus.

4.1.3 Output Signals

Reset Output/Abort ($\overline{RST}$/$\overline{ABT}$): Active Low. Held active longer than one clock cycle to reset the CPU. Pulsed low during T2 or TMMU to abort the current CPU instruction.

Interrupt Output ($\overline{INT}$): Active low. Pulse used by the debug functions to inform the CPU that a break condition has occurred.

Float Output ($\overline{FLT}$): Active low. Floats the CPU from the bus when the MMU accesses page table entries or performs a physical breakpoint check. Section 2.4.3.

Physical Address Valid ($\overline{PAV}$): Active low. Pulse generated during TMMU indicating that a physical address is present on the bus.

4.2 ABSOLUTE MAXIMUM RATINGS

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Temperature Under Bias	0°C to +70°C
Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to GND	−0.5V to +7V
Power Dissipation	1.5W

Hold Acknowledge Output ($\overline{HLDAO}$): Active low. When active, indicates that the bus has been released.

4.1.4 Input-Output Signals

Data Direction In ($\overline{DDIN}$): Active low. Status signal indicating direction of data transfer during a bus cycle. Driven by the MMU during a page-table lookup.

Address Translation/Slave Processor Control ($\overline{AT}$/ $\overline{SPC}$): Active low. Used by the CPU as the data strobe output for Slave Processor transfers; used by the MMU to acknowledge completion of an MMU instruction. Section 2.3 and 2.5. Held low during reset to select the address translation mode on the CPU.

M.S. Bit of Physical Address/High Byte Float (A24/ $\overline{HBF}$): Most significant bit of physical address. Sampled on the rising edge of the reset input to select 16 or 32-bit bus mode. This pin outputs a low level if address translation is not enabled. It is floated during T2–T4 if 32-bit bus mode is selected.

Address Bits 16–23 (A16–A23): High order bits of the address bus. These signals are floated by the MMU during T2–T4 if 32-bit bus mode is selected.

Address/Data 0–15 (AD0–AD15): Multiplexed Address/ Data Information. Bit 0 is the least significant bit.

Note: *Absolute maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended; operation should be limited to those conditions specified under Electrical Characteristics.*

4.3 ELECTRICAL CHARACTERISTICS T_A = 0 to +70°C, V_{CC} = 5V ±5%, GND = 0V

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High Level Input Voltage		2.0		V_{CC} + 0.5	V
V_{IL}	Low Level Input Voltage		−0.5		0.8	V
V_{CH}	High Level Clock Voltage	PHI1, PHI2 pins only	V_{CC} − 0.35		V_{CC} + 0.5	V
V_{CL}	Low Level Clock Voltage	PHI1, PHI2 pins only	−0.5		0.3	V
V_{CLT}	Low Level Clock Voltage, Transient (ringing tolerance)	PHI1, PHI2 pins only	−0.5		0.6	V
V_{OH}	High Level Output Voltage	I_{OH} = −400 μA	2.4			V
V_{OL}	Low Level Output Voltage	I_{OL} = 2 mA			0.45	V
I_{ILS}	$\overline{AT}$/$\overline{SPC}$ Input Current (low)	V_{IN} = 0.4V, $\overline{AT}$/$\overline{SPC}$ in input mode	0.05		1.0	mA
I_I	Input Load Current	0 ≤ V_{IN} ≤ V_{CC}, All inputs except PHI1, PHI2, $\overline{AT}$/$\overline{SPC}$	−20		20	μA
I_L	Leakage Current (Output and I/O Pins in TRI-STATE/Input Mode)	0.4 ≤ V_{IN} ≤ V_C	−20		30	μA
I_{CC}	Active Supply Current	I_{OUT} = 0, T_A = 25°C		200	300	mA

4.0 Device Specifications (Continued)

4.4 SWITCHING CHARACTERISTICS

4.4.1 Definitions

All the timing specifications given in this section refer to 2.0V on the rising or falling edges of the clock phases PHI1 and PHI2, and 0.8V or 2.0V on all other signals as illustrated in *Figures 4-2* and *4-3*, unless specifically stated otherwise.

ABBREVIATIONS:

L.E. — leading edge R.E. — rising edge
T.E. — trailing edge F.E. — falling edge

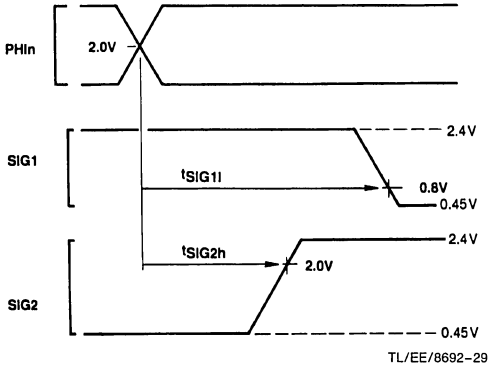

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FIGURE 4-2. Timing Specification Standard (Signal Valid after Clock Edge)

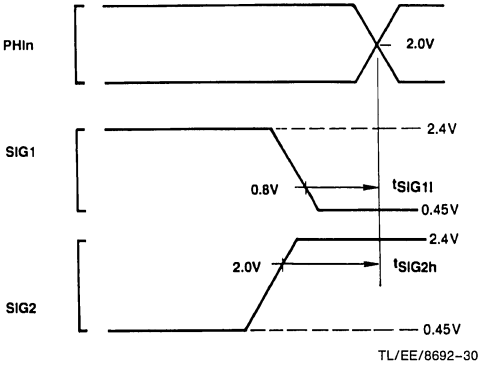

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FIGURE 4-3. Timing Specification Standard (Signal Valid before Clock Edge)

4.4.2 Timing Tables

4.4.2.1 Output Signals: Internal Propagation Delays, NS32082-10.
Maximum times assume capacitive loading of 100 pF.

Name	Figure	Description	Reference/Conditions	NS32082-10		Units
				Min	Max	
t_{ALv}	4–4	Address Bits 0–15 Valid	After R.E., PHI1 TMMU or T1		40	ns
t_{ALh}	4–4	Address Bits 0–15 Hold	After R.E., PHI1 T2	5		ns
t_{AHv}	4–4, 4–6	Address Bits 16–24 Valid	After R.E., PHI1 TMMU or T1		40	ns
t_{AHh}	4–4	Address Bits 16–24 Hold	After R.E., PHI1 T2	5		ns
t_{ALPAVs}	4–5	Address Bits 0–15 Set Up	Before $\overline{PAV}$ T.E.	25		ns
t_{AHPAVs}	4–5	Address Bits 16–24 Set Up	Before $\overline{PAV}$ T.E.	25		ns
t_{ALPAVh}	4–5	Address Bits 0–15 Hold	After $\overline{PAV}$ T.E.	15		ns
t_{AHPAVh}	4–5	Address Bits 16–24 Hold	After $\overline{PAV}$ T.E.	15		ns
t_{ALf}	4–10	AD0–AD15 Floating	After R.E., PHI1 T2		25	ns
t_{AHf}	4–7, 4–10	A16–A24 Floating	After R.E., PHI1 T2 or T1		25	ns
t_{ALz}	4–15, 4–16	AD0–AD15 Floating (Caused by $\overline{HOLD}$)	After R.E., PHI1 Ti		25	ns
t_{AHZ}	4–15, 4–16	A16–A24 Floating (Caused by $\overline{HOLD}$)	After R.E., PHI1 Ti		25	ns
t_{ALr}	4–15, 4–16	AD0–AD15 Return from Floating (Caused by $\overline{HOLD}$)	After R.E., PHI1 T1		50	ns

4.0 Device Specifications (Continued)

4.4.2.1 Output Signals: Internal Propagation Delays, NS32082-10. (Continued)

Name	Figure	Description	Reference/Conditions	NS32082-10		Units
				Min	Max	
t_{AHr}	4–15, 4–16	A16–A24 Return from Floating (Caused by $\overline{HOLD}$)	After R.E., PHI1 T1		50	ns
t_{Dv}	4–6	Data Valid (Memory Write)	After R.E., PHI1 T2		50	ns
t_{Dh}	4–6	Data Hold (Memory Write)	After R.E., PHI1 next T1 or Ti	0		ns
t_{Df}	4–11	Data Bits Floating (Slave Processor Read)	After R.E., PHI1 T1 or Ti		10	ns
t_{Dv}	4–11	Data Valid (Slave Processor Read)	After R.E., PHI1 T1		50	ns
t_{Dh}	4–11	Data Hold (Slave Processor Read)	After R.E., PHI1 next T1 or Ti	0		ns
t_{DDINv}	4–5, 4–7	$\overline{DDIN}$ Signal Valid	After R.E., PHI1 T1 or T_{MMU}		50	ns
t_{DDINh}	4–5	$\overline{DDIN}$ Signal Hold	After R.E., PHI1 T1 or Ti	0		ns
t_{DDINf}	4–7	$\overline{DDIN}$ Signal Floating	After R.E., PHI1 T2		25	ns
t_{DDINz}	4–16	$\overline{DDIN}$ Signal Floating (Caused by $\overline{HOLD}$)	After R.E., PHI1 Ti		50	ns
t_{DDINr}	4–16	$\overline{DDIN}$ Return from Floating (Caused by $\overline{HOLD}$)	After R.E., PHI1 T1 or Ti		50	ns
t_{DDINAf}	4–9	$\overline{DDIN}$ Floating after Abort ($\overline{FLT}$ = 0)	After R.E., PHI2 T2		25	ns
t_{PAVa}	4–4	$\overline{PAV}$ Signal Active	After R.E., PHI1 T_{MMU} or T1		35	ns
t_{PAVia}	4–4	$\overline{PAV}$ Signal Inactive	After R.E., PHI2 T_{MMU} or T1		40	ns
t_{PAVw}	4–4	$\overline{PAV}$ Pulse Width	At 0.8V (Both Edges)	30		ns
t_{PAVdz}	4–14, 4–15	$\overline{PAV}$ Floating Delay	After $\overline{HLDAI}$ F.E.		25	ns
t_{PAVdr}	4–14, 4–15	$\overline{PAV}$ Return from Floating	After $\overline{HLDAI}$ R.E.		25	ns
t_{PAVz}	4–16	$\overline{PAV}$ Floating (Caused by $\overline{HOLD}$)	After R.E., PHI2 T4		30	ns
t_{PAVr}	4–16	$\overline{PAV}$ Return from Floating (Caused by $\overline{HOLD}$)	After R.E., PHI2 Ti		30	ns
t_{FLTa}	4–5, 4–10	$\overline{FLT}$ Signal Active	After R.E., PHI1 T_{MMU}		55	ns
t_{FLTia}	4–7, 4–10	$\overline{FLT}$ Signal Inactive	After R.E., PHI1 T_{MMU}, T_f or T2		35	ns
t_{ABTa}	4–8, 4–10	Abort Signal Active	After R.E., PHI1 T_{MMU} or T1		55	ns
t_{ABTia}	4–8, 4–10	Abort Signal Inactive	After R.E., PHI1 T2		55	ns
t_{ABTw}	4–8, 4–10	Abort Pulse Width	At 0.8V (Both Edges)	70		ns
t_{INTa}	4–4, 4–10	$\overline{INT}$ Signal Active	After R.E., PHI1 T_{MMU} or T_f		55	ns
t_{INTia}	4–4, 4–10	$\overline{INT}$ Signal Inactive	After R.E., PHI1 T2		55	ns
t_{INTw}	4–10	$\overline{INT}$ Pulse Width	At 0.8V (Both Edges)	70		ns
t_{SPCa}	4–13	$\overline{SPC}$ Signal Active	After R.E., PHI1 T1		40	ns
t_{SPCia}	4–13	$\overline{SPC}$ Signal Inactive	After R.E., PHI1 T4		40	ns

4.0 Device Specifications (Continued)

4.4.2.1 Output Signals: Internal Propagation Delays, NS32082-10. (Continued)

Name	Figure	Description	Reference/Conditions	NS32082-10		Units
				Min	Max	
t_{SPCf}	4–13	$\overline{SPC}$ Signal Floating	After F.E., PHI1 T4		25	ns
t_{SPCw}	4–13	$\overline{SPC}$ Pulse Width	At 0.8V (Both Edges)	70		ns
t_{HLD0da}	4–14	$\overline{HLDA0}$ Assertion Delay	After $\overline{HLDAi}$ F.E.		50	ns
$t_{HLD0dia}$	4–14, 4–15	$\overline{HLDA0}$ Deassertion Delay	After $\overline{HLDAi}$ R.E.		50	ns
t_{HLD0a}	4–15, 4–16	$\overline{HLDA0}$ Signal Active	After R.E., PHI1 Ti		30	ns
t_{HLD0ia}	4–16	$\overline{HLDA0}$ Signal Inactive	After R.E, PHI1 Ti		30	ns
t_{ATa}	4–18	$\overline{AT}/\overline{SPC}$ Signal Active	After R.E., PHI1		35	ns
t_{ATia}	4–18	$\overline{AT}/\overline{SPC}$ Signal Inactive	After R.E., PHI1		35	ns
t_{ATf}	4–18	$\overline{AT}/\overline{SPC}$ Signal Floating	After F.E., PHI1		25	ns
t_{RST0a}	4–18	$\overline{RST}/\overline{ABT}$ Asserted (Low)	After R.E. PHI1		30	ns
t_{RST0ia}	4–18	$\overline{RST}/\overline{ABT}$ Deasserted (High)	After R.E. PHI1 Ti		30	ns

4.4.2.2 Input Signal Requirements: NS32082-10

Name	Figure	Description	Reference/Conditions	NS32082-10		Units
				Min	Max	
t_{DIs}	4–5	Data In Set Up (Memory Read)	Before F.E., PHI2 T3	15		ns
t_{DIh}	4–5	Data In Hold (Memory Read)	After R.E., PHI1 T4	3		ns
t_{DIs}	4–12	Data In Set Up (Slave Processor Write)	Before F.E., PHI2 T1	20		ns
t_{DIh}	4–12	Data In Hold (Slave Processor Write)	After R.E., PHI1 T4	3		ns
t_{RDYs}	4–5	RDY Signal Set Up	Before F.E., PHI2 T2 or T3	15		ns
t_{RDYh}	4–5	RDY Signal Hold	After F.E., PHI1 T3	5		ns
t_{USs}	4–4, 4-11	U/$\overline{S}$ Signal Set Up	Before F.E., PHI2 T4 or Ti	35		ns
t_{USh}	4–4, 4–11	U/$\overline{S}$ Signal Hold	After R.E., PHI1 Next T4	0		ns

4.0 Device Specifications (Continued)

4.4.2.2 Input Signal Requirements: NS32082-10 (Continued)

Name	Figure	Description	Reference/Conditions	NS32082-10		Units
				Min	Max	
t_{STs}	4–4, 4–11	Status Signals Set Up	Before F.E., PHI2 T4 or Ti	35		ns
t_{STh}	4–4, 4–11	Status Signals Hold	After R.E., PHI1 Next T4	0		ns
t_{SPCs}	4-11	$\overline{SPC}$ Input Set Up	Before F.E., PHI2 T1	45		ns
t_{SPCh}	4-11	$\overline{SPC}$ Input Hold	After R.E., PHI1 T4	0		ns
t_{HLDs}	4-16	$\overline{HOLD}$ Signal Set Up	Before F.E., PHI2 T4 or Ti	25		ns
t_{HLDh}	4-16	$\overline{HOLD}$ Signal Hold	After F.E., PHI2 T4 or Ti	0		ns
t_{HLDIs}	4-15	$\overline{HLDAi}$ Signal Set Up	Before F.E., PHI2 Ti	20		ns
t_{HLDIh}	4-15	$\overline{HLDAi}$ Signal Hold	After F.E., PHI2 Ti	0		ns
t_{HBFs}	4-18	A24/$\overline{HBF}$ Signal Set Up	Before F.E., PHI2	10		ns
t_{HBFh}	4-18	A24/$\overline{HBF}$ Signal Hold	After F.E., PHI2	0		ns
t_{RSTIs}	4-18	Reset Input Set Up	Before F.E., PHI1	20		ns
t_{PWR}	4-19	Power Stable to $\overline{RSTI}$ R.E.	After V_{CC} Reaches 4.5V	50		μs
t_{RSTIw}		$\overline{RSTI}$ Pulse Width	At 0.8V (Both Edges)	64		t_{cp}

4.4.2.3 Clocking Requirements: NS32082-10

Name	Figure	Description	Reference/ Conditions	NS32082-10		Units
				Min	Max	
t_{Cp}	4–17	Clock Period	R.E., PHI1, PHI2 to Next R.E., PHI1, PHI2	100	250	ns
t_{CLw}	4–17	PHI1, PHI2 Pulse Width	At 2.0V on PHI1, PHI2 (Both Edges)	$0.5t_{Cp}$ − 10 ns		
t_{CLh}	4–17	PHI1, PHI2 High Time	At V_{CC} − 0.9V on PHI1, PHI2 (Both Edges)	$0.5t_{Cp}$ − 15 ns		
t_{CLl}	4–17	PHI1, PHI2 Low Time	At 0.8V on PHI1, PHI2	$0.5t_{Cp}$ − 5 ns		
$t_{nOVL\,(1,2)}$	4–17	Non-overlap Time	0.8V on F.E. PHI1, PHI2 to 0.8V on R.E., PHI2, PHI1	−2	5	ns
t_{nOVLas}		Non-overlap Asymmetry ($t_{nOVL(1)} - t_{nOVL(2)}$)	At 0.8V on PHI1, PHI2	−4	4	ns
t_{CLwas}		PHI1, PHI2 Asymmetry $t_{CLw(1)} - t_{CLw(2)}$	At 2.0V on PHI1, PHI2	−5	5	ns

4.0 Device Specifications (Continued)

4.4.3 Timing Diagrams

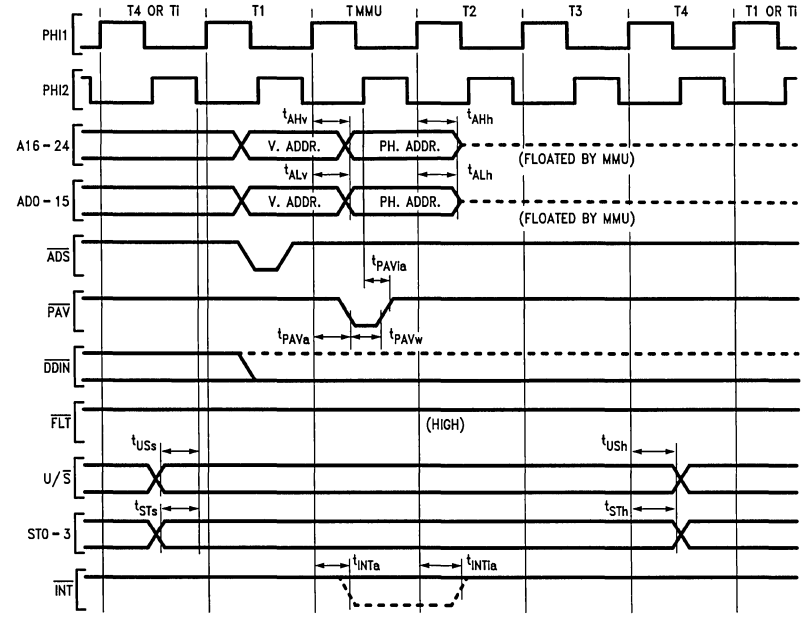

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FIGURE 4-4. CPU Read (Write) Cycle Timing (32-Bit Mode); Translation in TLB

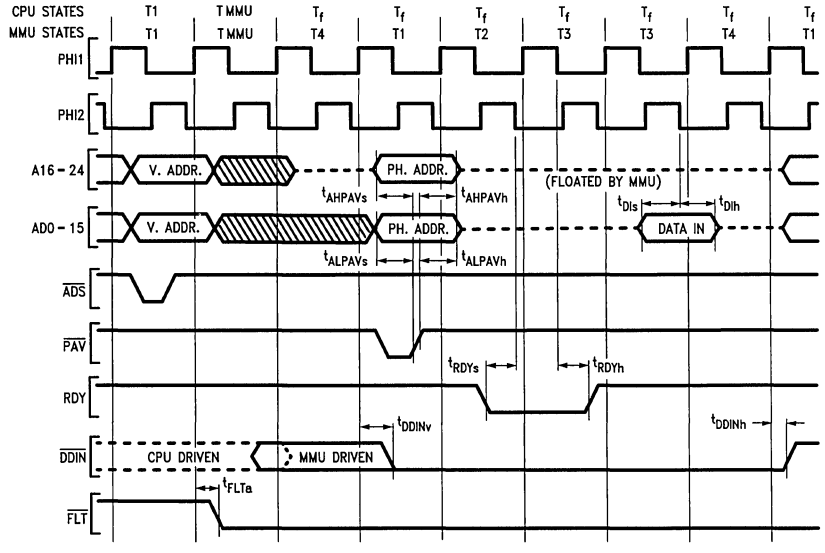

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FIGURE 4-5. MMU Read Cycle Timing (32-Bit Mode); After a TLB Miss

Note: After $\overline{FLT}$ is asserted, $\overline{DDIN}$ may be driven temporarily by both CPU and MMU. This, however, does not cause any conflict, since both CPU and MMU force $\overline{DDIN}$ to the same logic level.

4.0 Device Specifications (Continued)

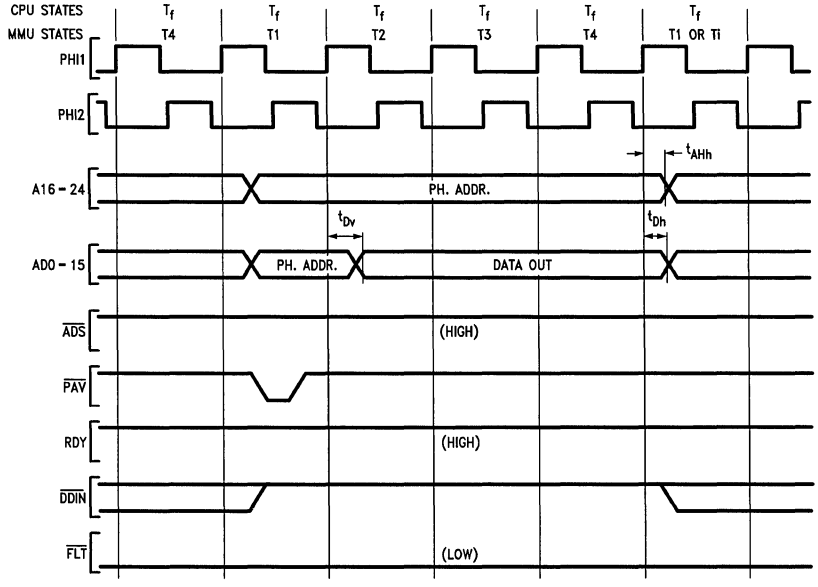

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FIGURE 4-6. MMU Write Cycle Timing; after a TLB Miss

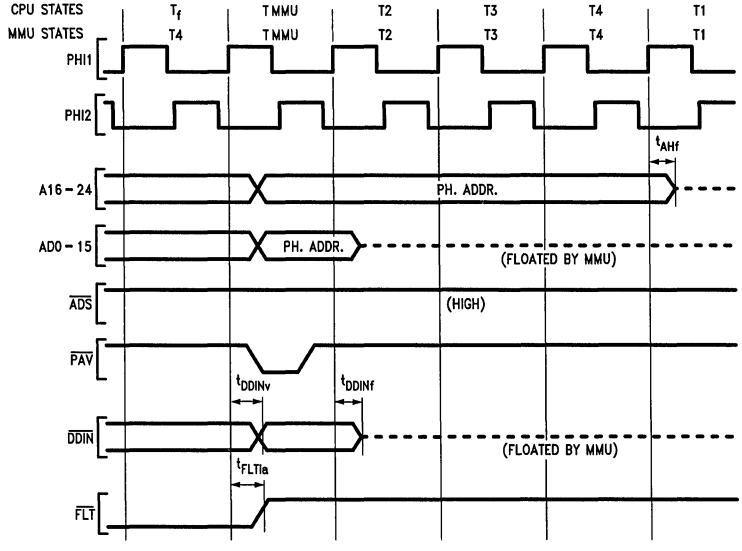

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FIGURE 4-7. $\overline{FLT}$ Deassertion Timing

Note: After $\overline{FLT}$ is deasserted, $\overline{DDIN}$ may be driven temporarily by both CPU and MMU. This, however, does not cause any conflict. Since CPU and MMU force $\overline{DDIN}$ to the same logic level.

4.0 Device Specifications (Continued)

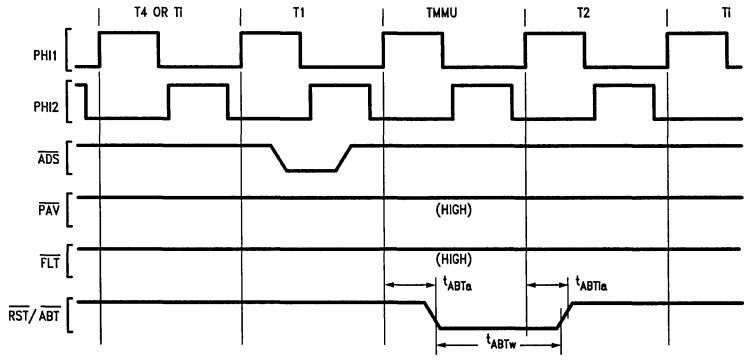

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FIGURE 4-8. Abort Timing ($\overline{FLT}$ = 1)

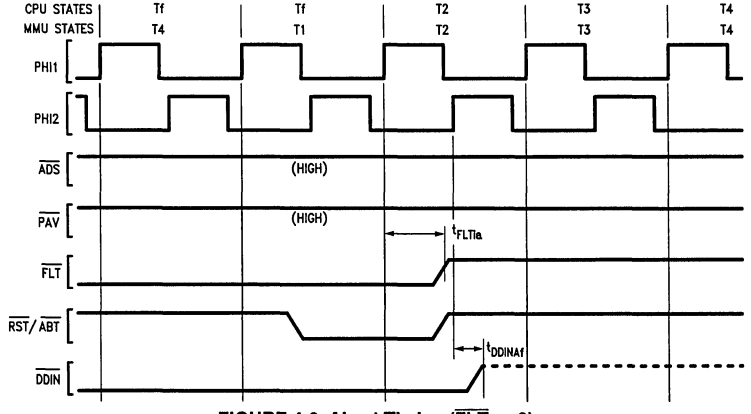

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FIGURE 4-9. Abort Timing ($\overline{FLT}$ = 0)

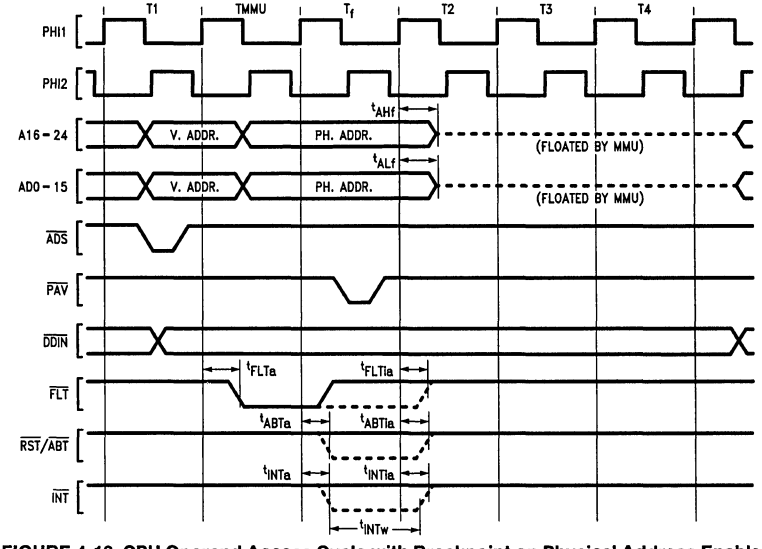

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FIGURE 4-10. CPU Operand Access Cycle with Breakpoint on Physical Address Enabled

Note: If a breakpoint condition is met and abort on breakpoint is enabled, the bus cycle is aborted. In this case $\overline{FLT}$ is stretched by one clock cycle.

4.0 Device Specifications (Continued)

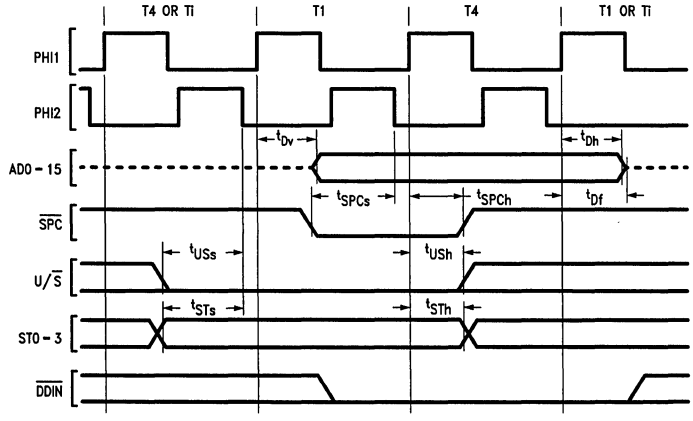

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FIGURE 4-11. Slave Access Timing; CPU Reading from MMU

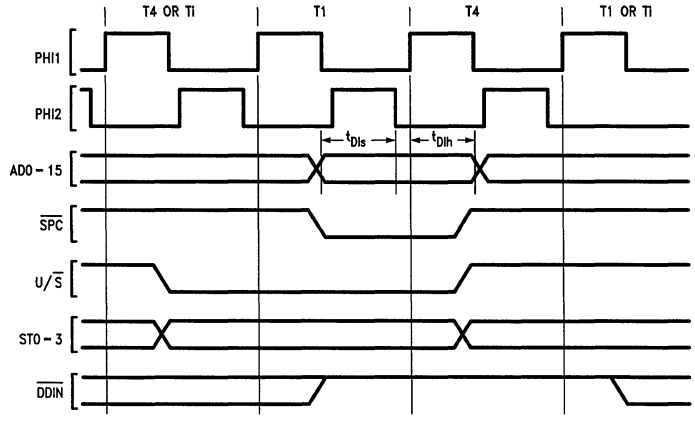

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FIGURE 4-12. Slave Access Timing; CPU Writing to MMU

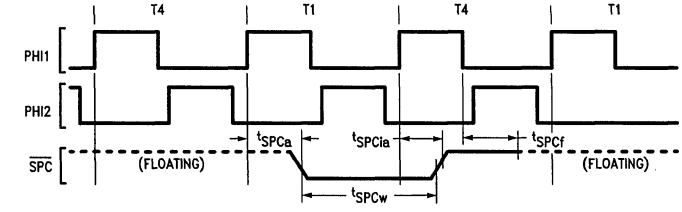

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FIGURE 4-13. $\overline{SPC}$ Pulse from the MMU

4.0 Device Specifications (Continued)

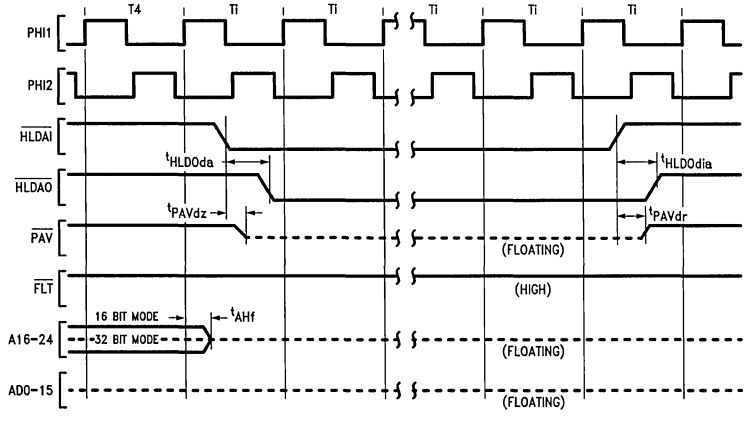

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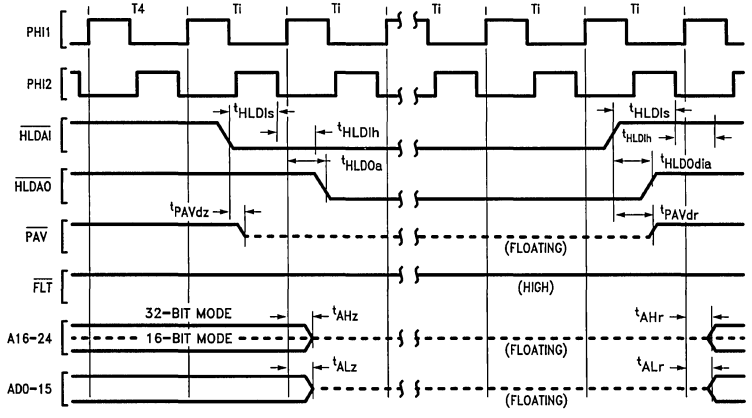
FIGURE 4-14. Hold Timing ($\overline{FLT}$ = 1); SMR Instruction Not Being Executed



TL/EE/8692-42

FIGURE 4-15. Hold Timing ($\overline{FLT}$ = 1); SMR Instruction Being Executed

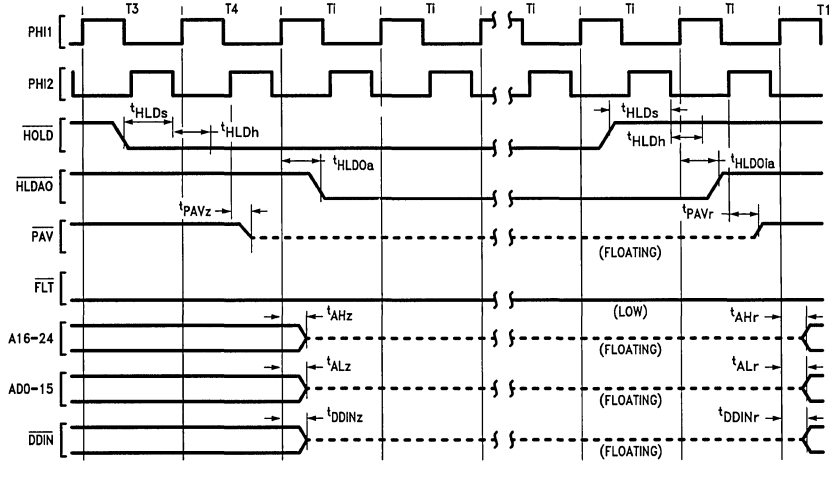


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FIGURE 4-16. Hold Timing ($\overline{FLT}$ = 0)

4.0 Device Specifications (Continued)

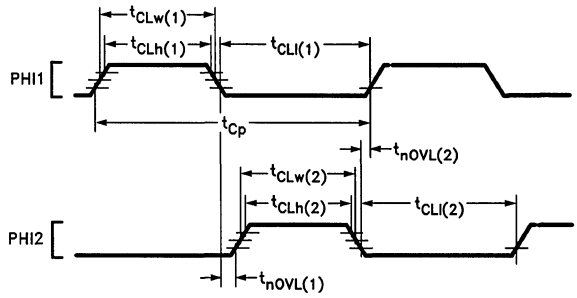

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FIGURE 4-17. Clock Waveforms

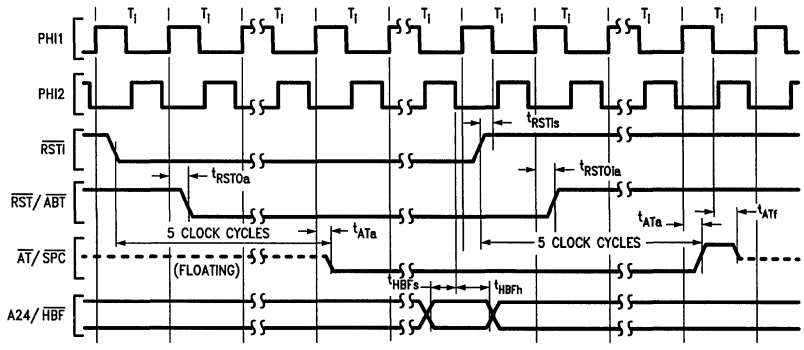

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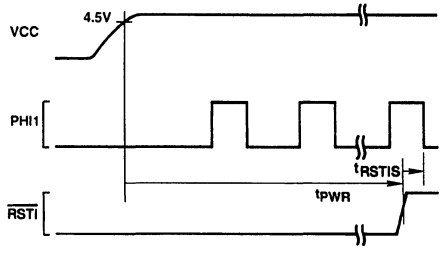
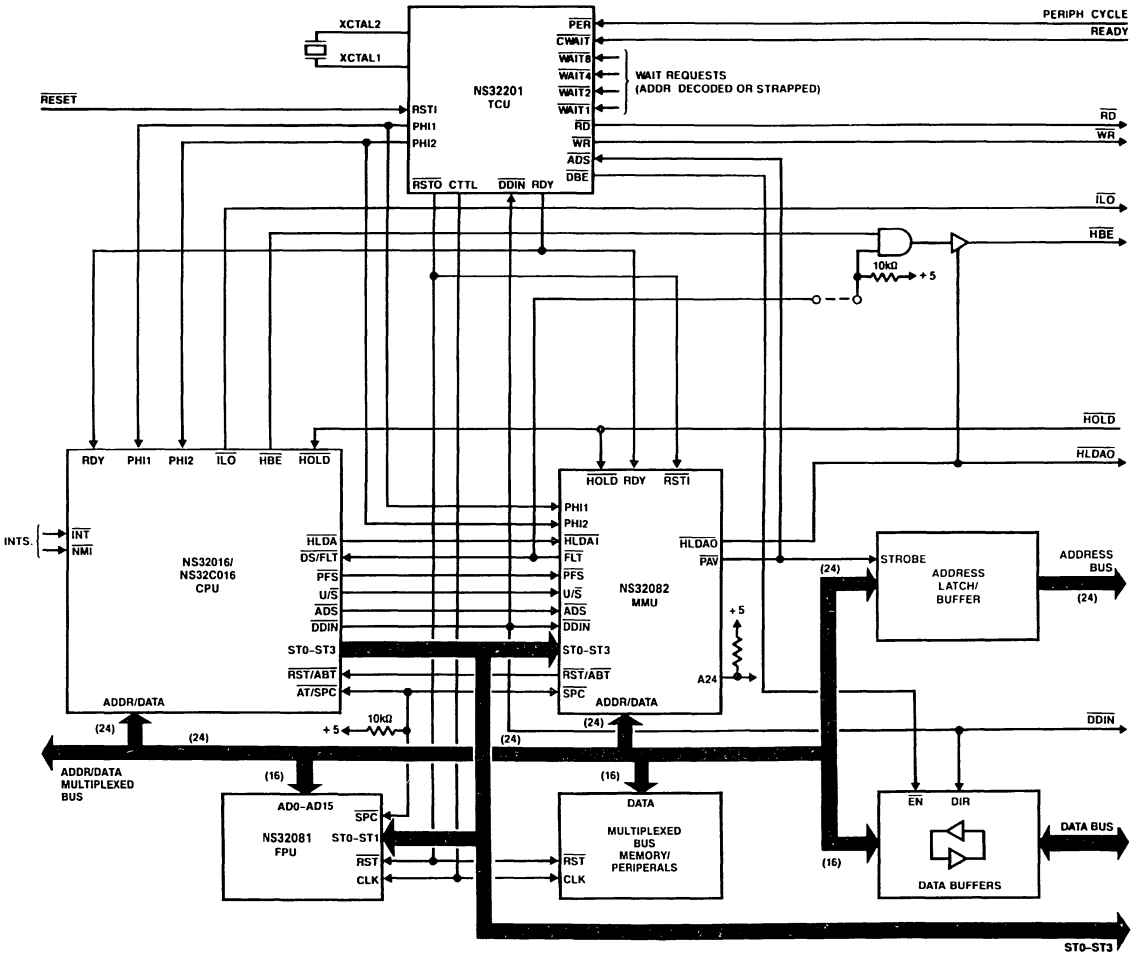
FIGURE 4-18. Reset Timing



TL/EE/8692-46

FIGURE 4-19. Power-On Reset



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Note: The "AND" gate on the $\overline{HBE}$ line is not needed when an NS32016 is used.

FIGURE A-1. System Connection Diagram

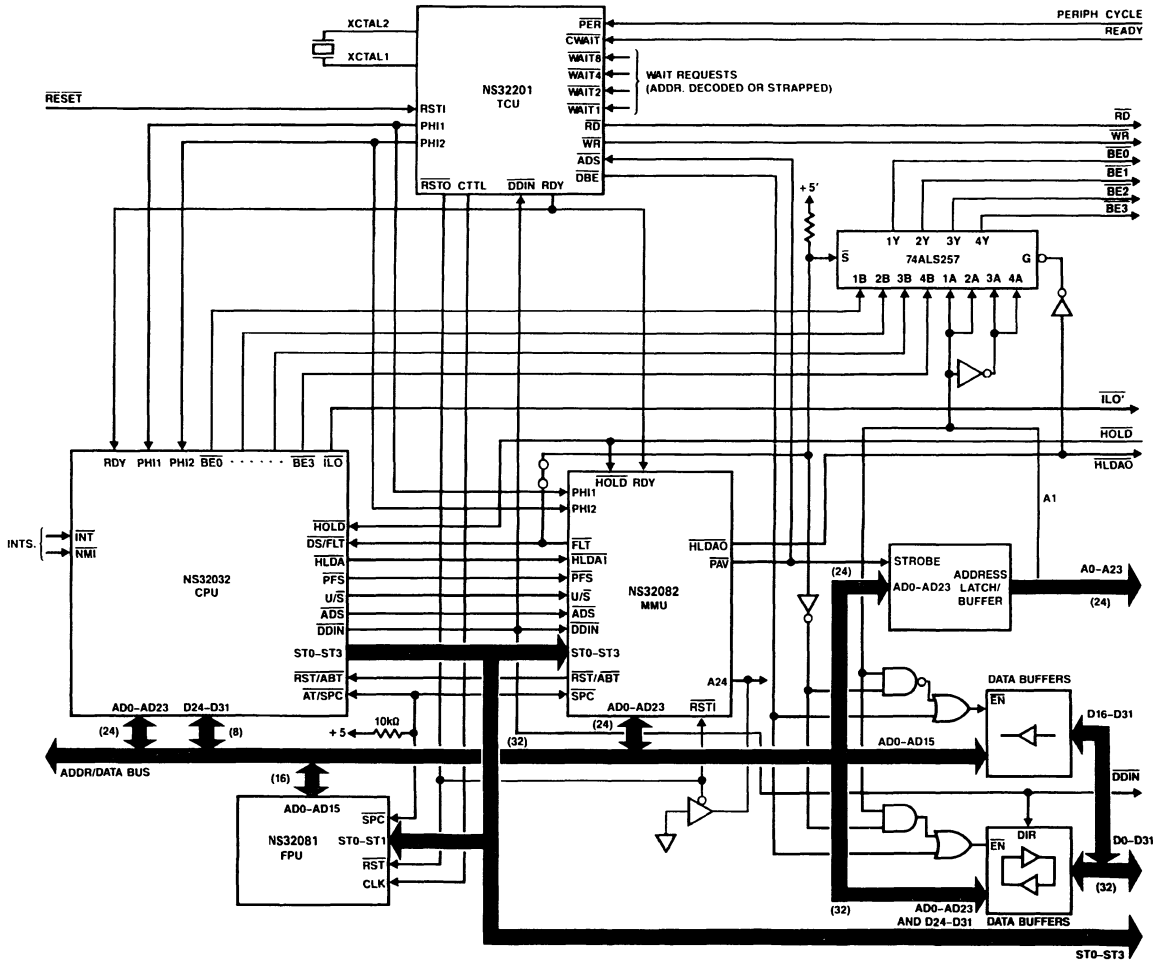

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FIGURE A-2. System Connection Diagram

National Semiconductor

PRELIMINARY

NS32381-15/NS32381-20 Floating-Point Unit

General Description

The NS32381 is a second generation, CMOS, floating-point slave processor that is fully software compatible with its forerunner, the NS32081 FPU. The NS32381 FPU functions with any Series 32000 CPU, from the NS32008 to the NS32532, in a tightly coupled slave configuration. The performance of the NS32381 has been increased over the NS32081 by architecture improvements, hardware enhancements, and higher clock frequencies. Key improvements include the addition of a 32-bit slave protocol, an early done algorithm to increase CPU/FPU parallelism, an expanded register set, an automatic power down feature, expanded math hardware, and additional instructions.

The NS32381 FPU contains eight 64-bit data registers and a Floating-Point Status Register (FSR). The FPU executes 20 instructions, and operates on both single and double-precision operands. Three separate processors in the NS32381 manipulate the mantissa, sign, and exponent. The NS32381 FPU conforms to IEEE standard 754-1985 for binary floating-point arithmetic.

When used with a Series 32000 CPU, the CPU and NS32381 FPU form a tightly coupled computer cluster. This cluster appears to the user as a single processing unit. All addressing modes, including two address operations, are available with the floating-point instructions. In addition, CPU and FPU communication is handled automatically, and is user transparent.

The FPU is fabricated with National's advanced double-metal CMOS process. It is available in a 68-pin Pin Grid Array (PGA) package.

Features

- Directly compatible with NS32008, NS32016, NS32C016, NS32032, NS32C032, NS32332 and NS32532 microprocessors
- Selectable 16-bit or 32-bit Slave Protocol
- Conforms to IEEE standard 754-1985 for binary floating-point arithmetic
- Early done algorithm
- Single (32-bit) and double (64-bit) precision operations
- Eight on-chip (64-bit) data registers
- (Automatic) power down mode
- Full upward compatibility with existing 32000 software
- High speed double-metal CMOS design
- 68-pin PGA package

FPU Block Diagram

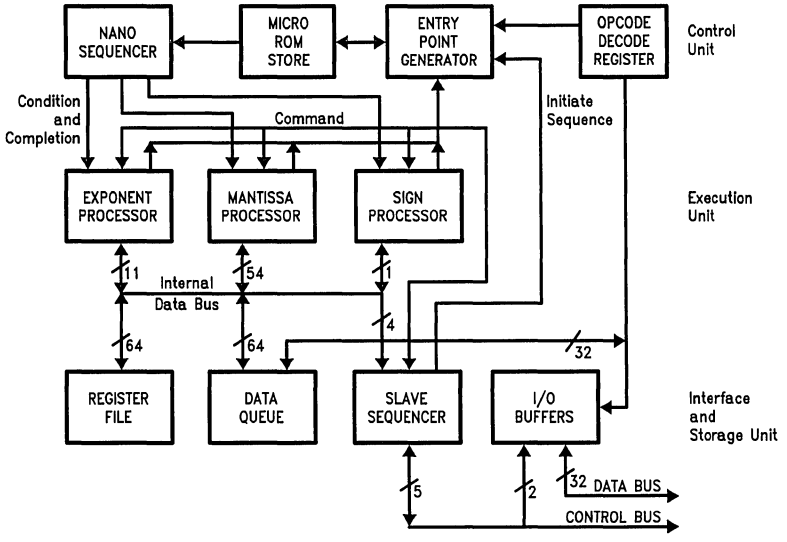

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FIGURE 1-1

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1.0 Product Introduction

The NS32381 Floating-Point Unit (FPU) provides high speed floating-point operations for the Series 32000 family, and is fabricated using National high-speed CMOS technology. It operates as a slave processor for transparent expansion of the Series 32000 CPU's basic instruction set. The FPU can also be used with other microprocessors as a peripheral device by using additional TTL and CMOS interface logic. The NS32381 is compatible with the IEEE Floating-Point Formats by means of its hardware and software features.

1.1 IEEE FEATURES SUPPORTED

a) Basic floating-point number formats

b) Add, subtract, multiply, divide and compare operations

c) Conversions between different floating-point formats

d) Conversions between floating-point and integer formats

e) Round floating-point number to integer (round to nearest, round toward negative infinity and round toward zero, in double or single-precision)

f) Exception signaling and handling (invalid operation, divide by zero, overflow, underflow and inexact)

The remaining IEEE features are supported in software. These items include:

a) Extended floating-point number formats

b) Positive and negative infinity, Not-a-Number (NaN), Denormalized numbers

c) Square root and conversions between basic formats, floating-point numbers and decimal strings

1.2 OPERAND FORMATS

The N32381 FPU operates on two floating-point data types—single precision (32 bits) and double precision (64 bits). Floating-point instruction mnemonics use the suffix F (Floating) to select the single precision data type, and the suffix L (Long Floating) to select the double precision data type.

A floating-point number is divided into three fields, as shown in *Figure 1-2*.

The F field is the fractional portion of the represented number. In Normalized numbers (Section 1.2.1), the binary point is assumed to be immediately to the left of the most significant bit of the F field, with an implied 1 bit to the left of the binary point. Thus, the F field represents values in the range $1.0 \leq x \leq 2.0$.

TABLE 1-1. Sample F Fields

F Field	Binary Value	Decimal Value
000...0	1.000...0	1.000...0
010...0	1.010...0	1.250...0
100...0	1.100...0	1.500...0
110...0	1.110...0	1.750...0

↑
Implied Bit

The E field contains an unsigned number that gives the binary exponent of the represented number. The value in the E field is biased; that is, a constant bias value must be subtracted from the E field value in order to obtain the true exponent. The bias value is $011\ldots11_2$, which is either 127 (single precision) or 1023 (double precision). Thus, the true exponent can be either positive or negative, as shown in Table 1-2.

TABLE 1-2. Sample E Fields

E Field	F Field	Represented Value
011...110	100...0	$1.5\times2^{-1} = 0.75$
011...111	100...0	$1.5\times2^{0} = 1.50$
100...000	100...0	$1.5\times2^{1} = 3.00$

Two values of the E field are not exponents. 11...11 signals a reserved operand (Section 1.2.3). 00...00 represents the number zero if the F field is also all zeroes, otherwise it signals a reserved operand.

The S bit indicates the sign of the operand. It is 0 for positive and 1 for negative. Floating-point numbers are in sign-magnitude form, that is, only the S bit is complemented in order to change the sign of the represented number.

1.2.1 Normalized Numbers

Normalized numbers are numbers which can be expressed as floating-point operands, as described above, where the E field is neither all zeroes nor all ones.

The value of a Normalized number can be derived by the formula:

$$(-1)^{S} \times 2^{(E\text{-}Bias)} \times (1 + F)$$

The range of Normalized numbers is given in Table 1-3.

1.2.2 Zero

There are two representations for zero—positive and negative. Positive zero has all-zero F and E fields, and the S bit is zero. Negative zero also has all-zero F and E fields, but its S bit is one.

1.2.3 Reserved Operands

The proposed IEEE Standard for Binary Floating-Point Arithmetic (Task P754) provides for certain exceptional forms of floating-point operands. The NS32381 FPU treats these forms as reserved operands. The reserved operands are:

- Positive and negative infinity
- Not-a-Number (NaN) values
- Denormalized numbers

Both Infinity and NaN values have all ones in their E fields. Denormalized numbers have all zeroes in their E fields and non-zero values in their F fields.

The NS32381 FPU causes an Invalid Operation trap (Section 2.1.2.2) if it receives a reserved operand, unless the operation is simply a move (without conversion). The FPU does not generate reserved operands as results.

1.0 Product Introduction (Continued)

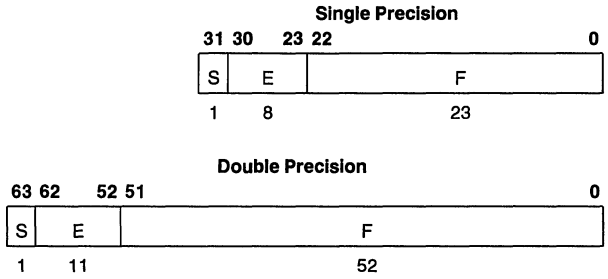

FIGURE 1-2. Floating-Point Operand Formats

TABLE 1-3. Normalized Number Ranges

	Single Precision	Double Precision
Most Positive	$2^{127} \times (2 - 2^{-23})$ $= 3.40282346 \times 10^{38}$	$2^{1023} \times (2 - 2^{-52})$ $= 1.7976931348623157 \times 10^{308}$
Least Positive	2^{-126} $= 1.17549436 \times 10^{-38}$	2^{-1022} $= 2.2250738585072014 \times 10^{-308}$
Least Negative	$-(2^{-126})$ $= -1.17549436 \times 10^{-38}$	$-(2^{-1022})$ $= -2.2250738585072014 \times 10^{-308}$
Most Negative	$-2^{127} \times (2 - 2^{-23})$ $= -3.40282346 \times 10^{38}$	$-2^{1023} \times (2 - 2^{-52})$ $= -1.7976931348623157 \times 10^{308}$

Note: The values given are extended one full digit beyond their represented accuracy to help in generating rounding and conversion algorithms.

1.2.4 Integers

In addition to performing floating-point arithmetic, the NS32381 FPU performs conversions between integer and floating-point data types. Integers are accepted or generated by the FPU as two's complement values of byte (8 bits), word (16 bits) or double word (32 bits) length.

See *Figure 1-3* for the Integer Format and Table 1-4 for the Integer Fields.

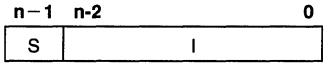

FIGURE 1-3. Integer Format

TABLE 1-4. Integer Fields

S	Value	Name
0	I	Positive Integer
1	$I - 2^n$	Negative Integer

Note: n represents n number of bits in the word, 8 for byte, 16 for word and 32 for double-word.

1.2.5 Memory Representations

The NS32381 FPU does not directly access memory. However, it is cooperatively involved in the execution of a set of two-address instructions with its Series 32000 Family CPU. The CPU determines the representation of operands in memory.

In the Series 32000 family of CPUs, operands are stored in memory with the least significant byte at the lowest byte address. The only exception to this rule is the Immediate addressing mode, where the operand is held (within the instruction format) with the most significant byte at the lowest address.

2.0 Architectural Description

2.1 PROGRAMMING MODEL

The Series 32000 architecture includes nine registers that are implemented on the NS32381 Floating-Point Unit (FPU).

2.0 Architectural Description (Continued)

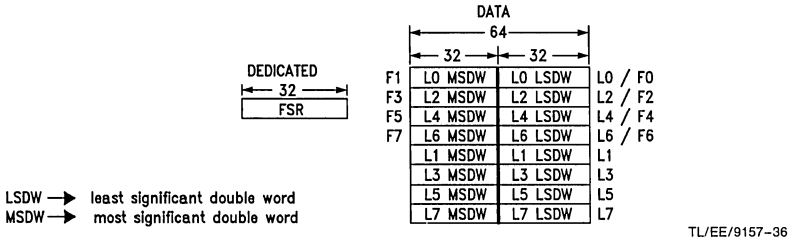

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FIGURE 2-1. Register Set

2.1.1 Floating-Point Registers

There are eight registers (L0–L7) on the NS32381 FPU for providing high-speed access to floating-point operands. Each is 64 bits long. A floating-point register is referenced whenever a floating-point instruction uses the Register addressing mode (Section 2.2.2) for a floating-point operand. All other Register mode usages (i.e., integer operands) refer to the General Purpose Registers (R0–R7) of the CPU, and the FPU transfers the operand as if it were in memory.

Note: These registers are all upward compatible with the 32-bit NS32081 registers, (F0–F7), such that when the Register addressing mode is specified for a double precision (64-bit) operand, a pair of 32-bit registers holds the operand. The programmer specifies the even register of the pair which contains the least significant half of the operand and the next consecutive register contains the most significant half.

2.1.2 Floating-Point Status Register (FSR)

The Floating-Point Status Register (FSR) selects operating modes and records any exceptional conditions encountered during execution of a floating-point operation. *Figure 2-2* shows the format of the FSR.

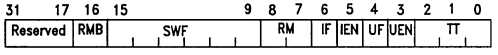

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FIGURE 2-2. The Floating-Point Status Register

2.1.2.1 FSR Mode Control Fields

The FSR mode control fields select FPU operation modes. The meanings of the FSR mode control bits are given below.

Rounding Mode (RM): Bits 7 and 8. This field selects the rounding method. Floating-point results are rounded whenever they cannot be exactly represented. The rounding modes are:

00 Round to nearest value. The value which is nearest to the exact result is returned. If the result is exactly halfway between the two nearest values the even value (LSB = 0) is returned.

01 Round toward zero. The nearest value which is closer to zero or equal to the exact result is returned.

10 Round toward positive infinity. The nearest value which is greater than or equal to the exact result is returned.

11 Round toward negative infinity. The nearest value which is less than or equal to the exact result is returned.

Underflow Trap Enable (UEN): Bit 3. If this bit is set, the FPU requests a trap whenever a result is too small in absolute value to be represented as a normalized number. If it is not set, any underflow condition returns a result of exactly zero.

Inexact Result Trap Enable (IEN): Bit 5. If this bit is set, the FPU requests a trap whenever the result of an operation cannot be represented exactly in the operand format of the destination. If it is not set, the result is rounded according to the selected rounding mode.

2.1.2.2 FSR Status Fields

The FSR Status Fields record exceptional conditions encountered during floating-point data processing. The meanings of the FSR status bits are given below:

Trap Type (TT): bits 0-2. This 3-bit field records any exceptional condition detected by a floating-point instruction. The TT field is loaded with zero whenever any floating-point instruction except LFSR or SFSR completes without encountering an exceptional condition. It is also set to zero by a hardware reset or by writing zero into it with the Load FSR (LFSR) instruction. Underflow and Inexact Result are always reported in the TT field, regardless of the settings of the UEN and IEN bits.

000 No exceptional condition occurred.

001 Underflow. A non-zero floating-point result is too small in magnitude to be represented as a normalized floating-point number in the format of the destination operand. This condition is always reported in the TT field and UF bit, but causes a trap only if the UEN bit is set. If the UEN bit is not set, a result of Positive Zero is produced, and no trap occurs.

010 Overflow. A result (either floating-point or integer) of a floating-point instruction is too great in magnitude to be held in the format of the destination operand. Note that rounding, as well as calculations, can cause this condition.

011 Divide by zero. An attempt has been made to divide a non-zero floating-point number by zero. Dividing zero by zero is considered an Invalid Operation instead (below).

100 Illegal Instruction. Any instruction forms not included in the NS32381 Instruction Set are detected by the FPU as being illegal.

3

2.0 Architectural Description (Continued)

101 Invalid Operation. One of the floating-point operands of a floating-point instruction is a Reserved operand, or an attempt has been made to divide zero by zero using the DIVf instruction.

110 Inexact Result. The result (either floating-point or integer) of a floating-point instruction cannot be represented exactly in the format of the destination operand, and a rounding step must alter it to fit. This condition is always reported in the TT field and IF bit unless any other exceptional condition has occurred in the same instruction. In this case, the TT field always contains the code for the other exception and the IF bit is not altered. A trap is caused by this condition only if the IEN bit is set; otherwise the result is rounded and delivered, and no trap occurs.

111 (Reserved for future use.)

Underflow Flag (UF): Bit 4. This bit is set by the FPU whenever a result is too small in absolute value to be represented as a normalized number. Its function is not affected by the state of the UEN bit. The UF bit is cleared only by writing a zero into it with the Load FSR instruction or by a hardware reset.

Inexact Result Flag (IF): Bit 6. This bit is set by the FPU whenever the result of an operation must be rounded to fit within the destination format. The IF bit is set only if no other error has occurred. It is cleared only by writing a zero into it with the Load FSR instruction or by a hardware reset.

Register Modify Bit (RMB): Bit 16. This bit is set by the FPU whenever writing to a floating point data register. The RMB bit is cleared only by writing a zero with the LFSR instruction or by a hardware reset. This bit can be used in context switching to determine whether the FPU registers should be saved.

2.1.2.3 FSR Software Field (SWF)

Bits 9-15 of the FSR hold and display any information written to them (using the LFSR and SFSR instructions), but are not otherwise used by FPU hardware. They are reserved for use with NSC floating-point extension software.

2.2 INSTRUCTION SET

2.2.1 General Instruction Format

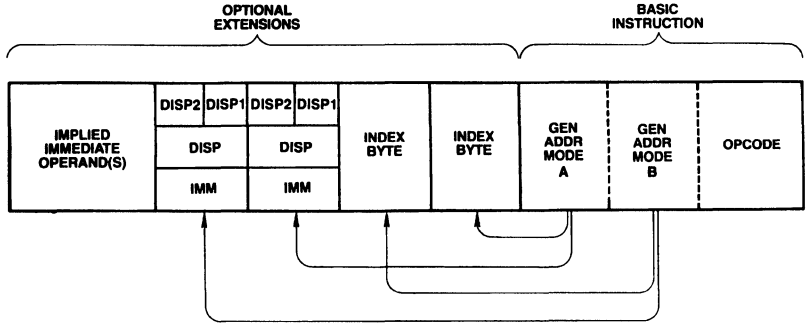
Figure 2-3 shows the general format of an Series 32000 instruction. The Basic Instruction is one to three bytes long and contains the opcode and up to two 5-bit General Addressing Mode (Gen) fields. Following the Basic Instruction field is a set of optional extensions, which may appear depending on the instruction and the addressing modes selected.

The only form of extension issued to the NS32381 FPU is an Immediate operand. Other extensions are used only by the CPU to reference memory operands needed by the FPU.

Index Bytes appear when either or both Gen fields specify Scaled Index. In this case, the Gen field specifies only the Scale Factor (1, 2, 4 or 8), and the Index Byte specifies which General Purpose Register to use as the index, and which addressing mode calculation to perform before indexing. See *Figure 2-4*.

Following Index Bytes come any displacements (addressing constants) or immediate values associated with the selected addressing modes. Each Disp/Imm field may contain one or two displacements, or one immediate value. The size of a Displacement field is encoded within the top bits of that field, as shown in *Figure 2-5*, with the remaining bits interpreted as a signed (two's complement) value. The size of an immediate value is determined from the Opcode field. Both Displacement and Immediate fields are stored most significant byte first.

Some non-FPU instructions require additional, "implied" immediates and/or displacements, apart from those associated with addressing modes. Any such extensions appear at the end of the instruction, in the order that they appear within the list of operands in the instruction definition.



TL/EE/9157-2

FIGURE 2-3. General Instruction Format

2.0 Architectural Description (Continued)

2.2.2 Addressing Modes

The Series 32000 Family CPUs generally access an operand by calculating its Effective Address based on information available when the operand is to be accessed. The method to be used in performing this calculation is specified by the programmer as an "addressing mode."

Addressing modes in the Series 32000 family are designed to optimally support high-level language accesses to variables. In nearly all cases, a variable access requires only one addressing mode within the instruction which acts upon that variable. Extraneous data movement is therefore minimized.

Series 32000 Addressing Modes fall into nine basic types:

Register: In floating-point instructions, these addressing modes refer to a Floating-Point Register (F0–F7) or (L0–L7) if the operand is of a floating-point type. Otherwise, a CPU General Purpose Register (R0–R7) is referenced. See Section 2.1.1.

Register Relative: A CPU General Purpose Register contains an address to which is added a displacement value from the instruction, yielding the Effective Address of the operand in memory.

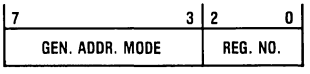


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FIGURE 2-4. Index Byte Format

Memory Space: Identical to Register Relative above, except that the register used is one of the dedicated CPU registers PC, SP, SB or FP. These registers point to data areas generally needed by high-level languages.

Memory Relative: A pointer variable is found within the memory space pointed to by the CPU SP, SB or FP register. A displacement is added to that pointer to generate the Effective Address of the operand.

Immediate: The operand is encoded within the instruction. This addressing mode is not allowed if the operand is to be written. Floating-point operands as well as integer operands may be specified using Immediate mode.

Absolute: The address of the operand is specified by a Displacement field in the instruction.

External: A pointer value is read from a specified entry of the current Link Table. To this pointer value is added a displacement, yielding the Effective Address of the operand.

Top of Stack: The currently-selected CPU Stack Pointer (SP0 or SP1) specifies the location of the operand. The operand is pushed or popped, depending on whether it is written or read.

Scaled Index: Although encoded as an addressing mode, Scaled Indexing is an option on any addressing mode except Immediate or another Scaled Index. It has the effect of calculating an Effective Address, then multiplying any General Purpose Register by 1, 2, 4 or 8 and adding it into the total, yielding the final Effective Address of the operand.

The following table, Table 2-1, is a brief summary of the addressing modes. For a complete description of their actions, see the Series 32000 Instruction Set Reference Manual.

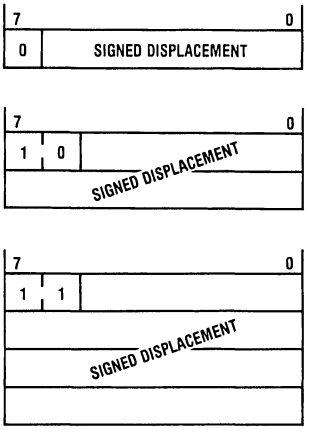

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FIGURE 2-5. Displacement Encodings

3

2.0 Architectural Description (Continued)

TABLE 2-1. Series 32000 Family Addressing Modes

Encoding	Mode	Assembler Syntax	Effective Address
REGISTER			
00000	Register 0	R0, F0 or L0	None: Operand is in the specified register.
00001	Register 1	R1, F1 or L1	
00010	Register 2	R2, F2 or L2	
00011	Register 3	R3, F3 or L3	
00100	Register 4	R4, F4 or L4	
00101	Register 5	R5, F5 or L5	
00110	Register 6	R6, F6 or L6	
00111	Register 7	R7, F7 or L7	
REGISTER RELATIVE			
01000	Register 0 relative	disp(R0)	Disp + Register.
01001	Register 1 relative	disp(R1)	
01010	Register 2 relative	disp(R2)	
01011	Register 3 relative	disp(R3)	
01100	Register 4 relative	disp(R4)	
01101	Register 5 relative	disp(R5)	
01110	Register 6 relative	disp(R6)	
01111	Register 7 relative	disp(R7)	
MEMORY SPACE			
11000	Frame memory	disp(FP)	Disp + Register; "SP" is either
11001	Stack memory	disp(SP)	SP0 or SP1, as selected in PSR.
11010	Static memory	disp(SB)	
11011	Program memory	*+disp	
MEMORY RELATIVE			
10000	Frame memory relative	disp2(disp1(FP))	Disp2+Pointer; Pointer found at
10001	Stack memory relative	disp2(disp1(SP))	address Disp1+Register. "SP" is
10010	Static memory relative	disp2(disp1(SB))	either SP0 or SP1, as selected in PSR.
IMMEDIATE			
10100	Immediate	value	None: Operand is issued from CPU instruction queue.
ABSOLUTE			
10101	Absolute	@disp	Disp.
EXTERNAL			
10110	External	EXT (disp1)+disp2	Disp2+Pointer; Pointer is found at Link Table Entry number Disp1.
TOP OF STACK			
10111	Top of Stack	TOS	Top of current stack, using either User or Interrupt Stack Pointer, as selected in PSR. Automatic Push/Pop included.
SCALED INDEX			
11100	Index, bytes	mode[Rn:B]	Mode + Rn.
11101	Index, words	mode[Rn:W]	Mode + 2 × Rn.
11110	Index, double words	mode[Rn:D]	Mode + 4 × Rn.
11111	Index, quad words	mode[Rn:Q]	Mode + 8 × Rn. "Mode" and "n" are contained within the Index Byte.
10011	(Reserved for Future Use)		

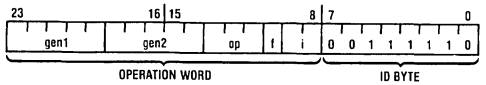
2.0 Architectural Description (Continued)

2.2.3 Floating-Point Instruction Set

The NS32381 FPU instructions occupy formats 9, 11 and 12 of the Series 32000 Family instruction set (*Figure 2-6*). A list of all Series 32000 family instruction formats is found in the applicable CPU data sheet.

Certain notations in the following instruction description tables serve to relate the assembly language form of each instruction to its binary format in *Figure 2-6*.

Format 9



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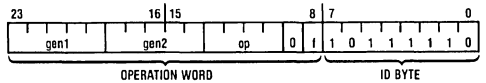
Format 11



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Format 12

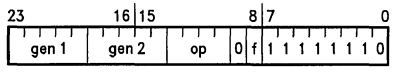

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FIGURE 2-6. Floating-Point Instruction Formats

The Format column indicates which of the three formats in *Figure 2-6* represents each instruction.

The Op column indicates the binary pattern for the field called "op" in the applicable format.

The Instruction column gives the form of each instruction as it appears in assembly language. The form consists of an instruction mnemonic in upper case, with one or more suffixes (i or f) indicating data types, followed by a list of operands (gen1, gen2).

An i suffix on an instruction mnemonic indicates a choice of integer data types. This choice affects the binary pattern in the i field of the corresponding instruction format (*Figure 2-6*) as follows:

Suffix i	Data Type	i Field
B	Byte	00
W	Word	01
D	Double Word	11

An f suffix on an instruction mnemonic indicates a choice of floating-point data types. This choice affects the setting of the f bit of the corresponding instruction format (*Figure 2-6*) as follows:

Suffix f	Data Type	f Bit
F	Single Precision	1
L	Double Precision (Long)	0

An operand designation (gen1, gen2) indicates a choice of addressing mode expressions. This choice affects the binary pattern in the corresponding gen1 or gen2 field of the instruction format (*Figure 2-6*). Refer to Table 2-1 for the options available and their patterns.

Further details of the exact operations performed by each instruction are found in the Series 32000 Instruction Set Reference Manual.

Movement and Conversion

The following instructions move the gen1 operand to the gen2 operand, leaving the gen1 operand intact.

Format	Op	Instruction		Description
11	0001	MOVf	gen1, gen2	Move without conversion
9	010	MOVLF	gen1, gen2	Move, converting from double precision to single precision.
9	011	MOVFL	gen1, gen2	Move, converting from single precision to double precision.
9	000	MOVif	gen1, gen2	Move, converting from any integer type to any floating-point type.
9	100	ROUNDfi	gen1, gen2	Move, converting from floating-point to the nearest integer.
9	101	TRUNCfi	gen1, gen2	Move, converting from floating-point to the nearest integer closer to zero.
9	111	FLOORfi	gen1, gen2	Move, converting from floating-point to the largest integer less than or equal to its value.

Note: The MOVLF instruction f bit must be 1 and the i field must be 10.
The MOVFL instruction f bit must be 0 and the i field must be 11.

Arithmetic Operations

The following instructions perform floating-point arithmetic operations on the gen1 and gen2 operands, leaving the result in the gen2 operand.

Format	Op	Instruction		Description
11	0000	ADDf	gen1, gen2	Add gen1 to gen2.
11	0100	SUBf	gen1, gen2	Subtract gen1 from gen2.
11	1100	MULf	gen1, gen2	Multiply gen2 by gen1.

2.0 Architectural Description (Continued)

	Format	Op	Instruction		Description
	11	1000	DIVf	gen1, gen2	Divide gen2 by gen1.
	11	0101	NEGf	gen1, gen2	Move negative of gen1 to gen2.
	11	1101	ABSf	gen1, gen2	Move absolute value of gen1 to gen2.
(N)	12	0100	SCALBf	gen1, gen2	Move gen2*2^{gen1} to gen2, for integral values of gen1 without computing 2^{gen1}.
(N)	12	0101	LOGBf	gen1, gen2	Move the unbiased exponent of gen1 to gen2.
(N)	12	0011	DOTf	gen1, gen2	Move (gen1*gen2) + L0 to L0.
(N)	12	0010	POLYf	gen1, gen2	Move (L0*gen1) + gen2 to L0.

(N): Indicates NEW instruction.

Comparison

The Compare instruction compares two floating-point values, sending the result to the CPU PSR Z and N bits for use as condition codes. See *Figure 3-11*. The Z bit is set if the gen1 and gen2 operands are equal; it is cleared otherwise. The N bit is set if the gen1 operand is greater than the gen2 operand; it is cleared otherwise. The CPU PSR L bit is unconditionally cleared. Positive and negative zero are considered equal.

Format	Op	Instruction		Description
11	0010	CMPf	gen1, gen2	Compare gen1 to gen2.

Floating-Point Status Register Access

The following instructions load and store the FSR as a 32-bit integer.

Format	Op	Instruction		Description
9	001	LFSR	gen1	Load FSR
9	110	SFSR	gen2	Store FSR

Note: All instructions support all of the NS32000 family data formats (for external operands) and all addressing modes are supported.

Rounding

The FPU supports all IEEE rounding options: Round toward nearest value or even significant if a tie. Round toward zero, Round toward positive infinity and Round toward negative infinity.

2.3 EXCEPTIONS/TRAPS

The FPU supports five types of traps: Invalid operation, Division by zero, Overflow, Underflow and Inexact (one trap can be signaled at a time). The user can disable the Inexact and the Underflow traps. If an undefined Floating-Point instruction is passed to the FPU an Illegal Instruction trap will occur. The user can't disable trap on Illegal Instruction.

Upon detecting an exceptional condition in executing a floating-point instruction, the FPU requests a TRAP by pulsing the $\overline{SPC}$ line for one clock cycle, pulsing the $\overline{SDN332}$ line for two and a half clock cycles and pulsing the $\overline{FSSR}$ line for one clock cycle. (The user will connect the correct lines according to the CPU being used).

In addition, the FPU sets the Q bit in the status word register. The CPU responds by reading the status word register while applying status h'E (transferring status word) on the status lines. A trapped instruction returns no result (also if the destination is FPU register) and does not affect the CPU PSR. The FPU displays the reason for the TRAP in the TRAP TYPE (TT) field of the FSR. If the CPU sends FPU ID with illegal opcode, the FPU generates TRAP(UND) by signaling TRAP and setting the T bit in the status word register.

3.0 Functional Description

3.1 POWER AND GROUNDING

The NS32381 requires a single 5V power supply, applied on seven (V_{CC}) pins. These pins should be connected together by a power (V_{CC}) plane on the printed circuit board. See *Figure 3-1*.

The grounding connections are made on eight (GND) pins. These pins should be connected together by a ground (GND) plane on the printed circuit board. See *Figure 3-1*.

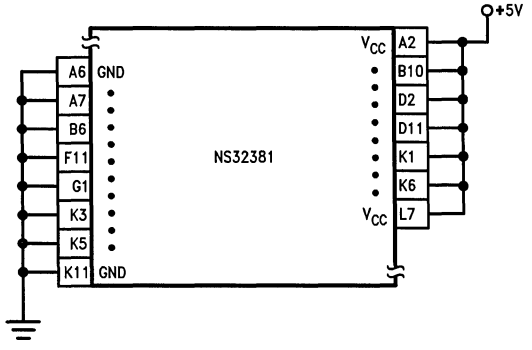

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FIGURE 3-1. Recommended Supply Connections

3.0 Functional Description (Continued)

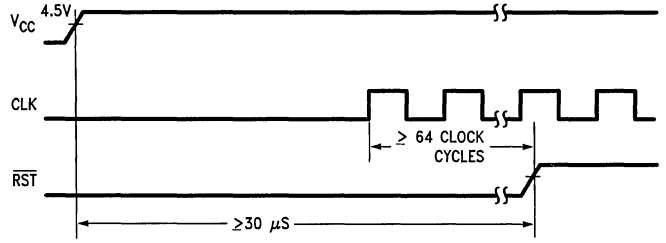

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FIGURE 3-2. Power-On Reset Requirements

3.2 AUTOMATIC POWER DOWN MODE

The NS32381 supports a power down mode in which the device consumes only 10% of its original power at 30 MHz. The NS32381 enters the power down mode (internal clocks are stopped with phase two high) if it does not receive an $\overline{SPC}$ pulse from the CPU within 256 clocks.

The FPU exits the power down mode and returns to normal operation after it receives an $\overline{SPC}$ from the CPU. There is no extra delay caused by the FPU being in the power down mode.

3.3 CLOCKING

The NS32381 FPU requires a single-phase TTL clock input on its CLK pin (pin A8). When the FPU is connected to a Series 32000 CPU, the CLK signal is provided from the CTTL pin of the NS32201 Timing Control Unit.

3.4 RESETTING

The $\overline{RST}$ pin serves as a reset for on-chip logic. The FPU may be reset at any time by pulling the $\overline{RST}$ pin low for at least 64 clock cycles. Upon detecting a reset, the FPU terminates instruction processing, resets its internal logic, and clears the FSR to all zeroes.

On application of power, $\overline{RST}$ must be held low for at least 30 μs after V_{CC} is stable. This ensures that all on-chip voltages are completely stable before operation. See *Figures 3-2* and *3-3*.

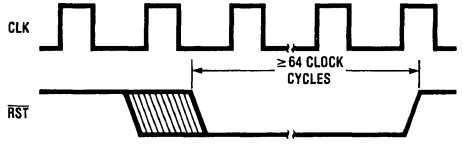

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FIGURE 3-3. General Reset Timing

3.5 BUS OPERATION

Instructions and operands are passed to the NS32381 FPU with slave processor bus cycles. Each bus cycle transfers either one byte (8 bits), one word (16 bits) or one double word (32 bits) to or from the FPU. During all bus cycles, the $\overline{SPC}$ line is driven by the CPU as an active low data strobe, and the FPU monitors pins ST0–ST3 to keep track of the sequence (protocol) established for the instruction being executed. This is necessary in a virtual memory environment, allowing the FPU to retry an aborted instruction.

3.5.1 Bus Cycles

A bus cycle is initiated by the CPU, which asserts the proper status on (ST0–ST3) and pulses $\overline{SPC}$ low. The status lines are sampled by the FPU on the leading (falling) edge of the $\overline{SPC}$ pulse except for the 32532 CPU. When used with the 32532 CPU, the status lines are sampled on the rising edge of CLK in the T2 state. If the transfer is from the FPU (a slave processor read cycle), the FPU asserts data on the data bus for the duration of the $\overline{SPC}$ pulse. If the transfer is to the FPU (a slave processor write cycle), the FPU latches data from the data bus on the trailing (rising) edge of the $\overline{SPC}$ pulse. *Figures 3-5, 3-6, 3-7* and *3-8* illustrate these sequences.

The direction of the transfer and the role of the bidirectional $\overline{SPC}$ line are determined by the instruction protocol being performed. $\overline{SPC}$ is always driven by the CPU during slave processor bus cycles. Protocol sequences for each instruction are given in Section 3.6.

3.5.2 Operand Transfer Sequences

An operand is transferred in one or more bus cycles. For the 16-Bit Slave Protocol a 1-byte operand is transferred on the least significant byte of the data bus (D0–D7). A 2-byte operand is transferred on the entire bus. A 4-byte or 8-byte operand is transferred in consecutive bus cycles, least significant word first.

For the 32-Bit Slave Protocol a 4-byte operand is transferred on the entire data bus in a single bus cycle and an 8-byte operand is transferred in two consecutive bus cycles with the most significant byte transferred on data bits (D0–D7). The complete operand transfer of bytes B0–B7 where B0 is the least significant byte would appear on the data bus as B4, B5, B6, B7 followed by B0, B1, B2, B3 in the second bus cycle.

3.0 Functional Description (Continued)

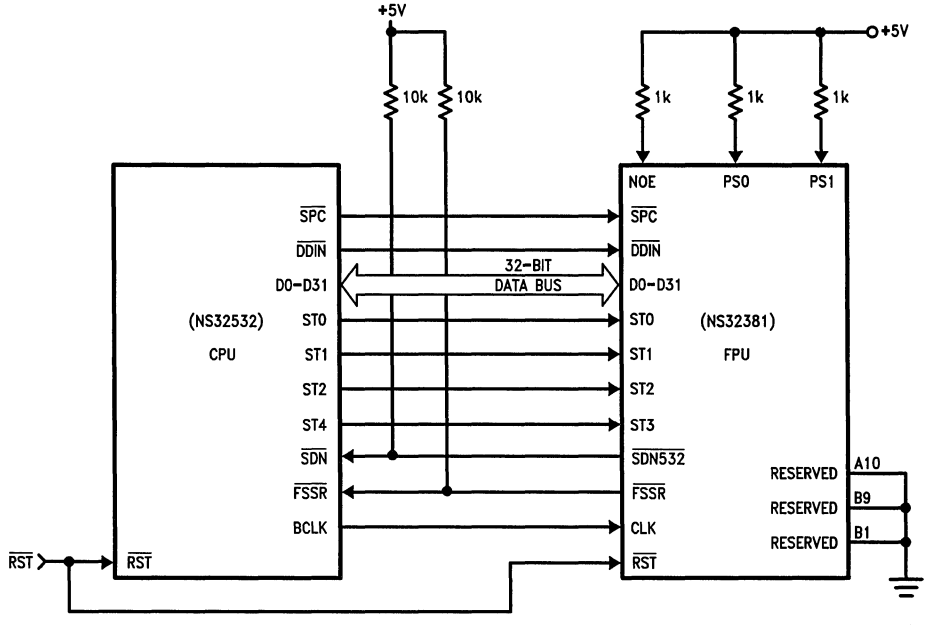

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FIGURE 3-4a. System Connection Diagram with the NS32532 CPU

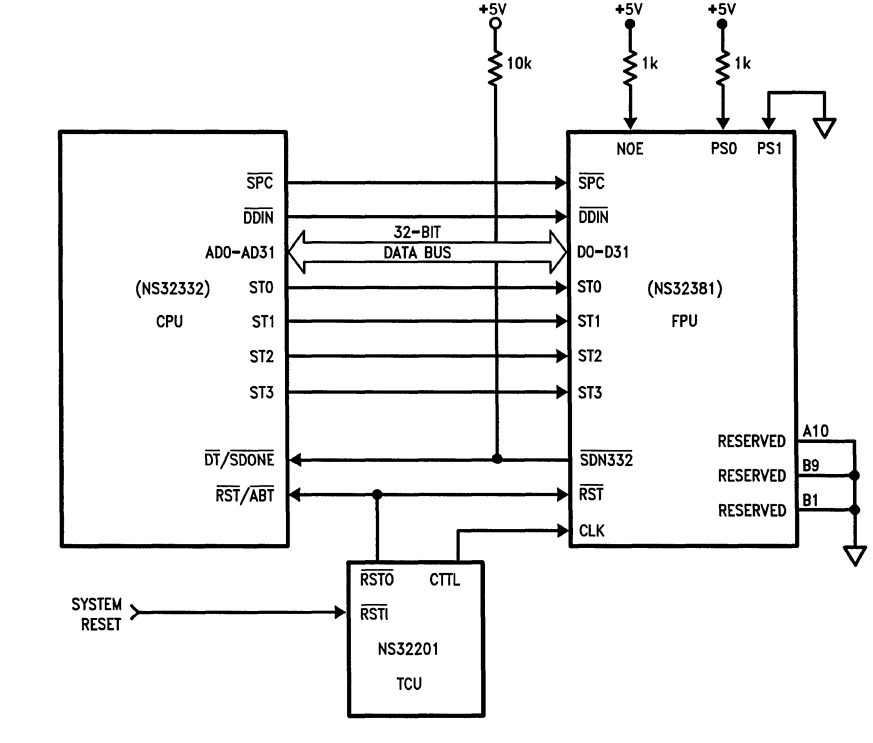

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FIGURE 3-4b. System Connection Diagram with the NS32332 CPU

3.0 Functional Description (Continued)

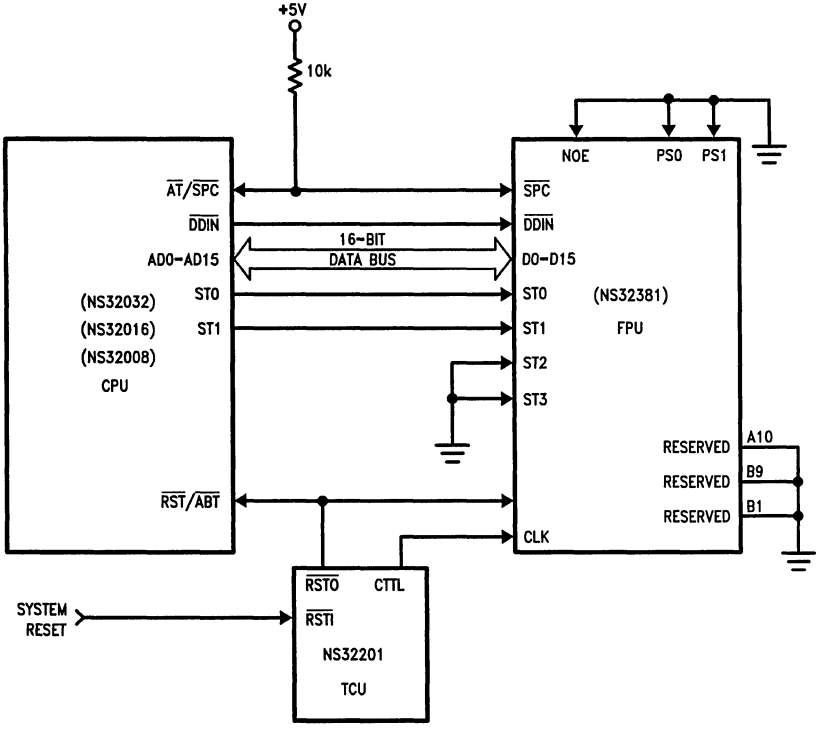

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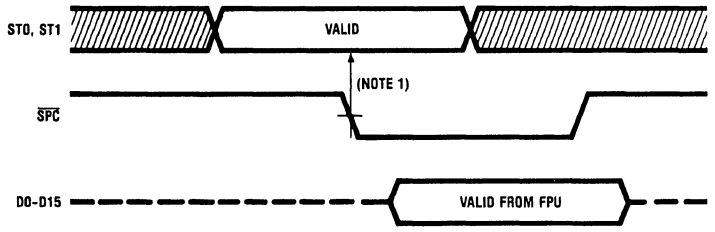
FIGURE 3-4c. System Connection Diagram with the NS32008, NS32016 or NS32032 CPU



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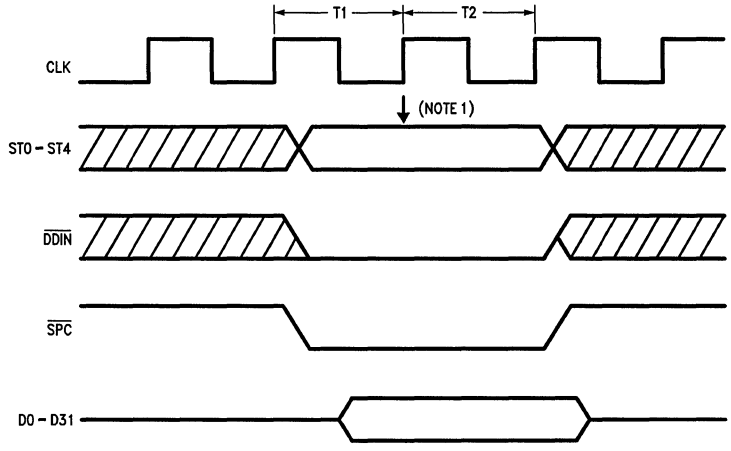
Note 1: FPU samples CPU status here.

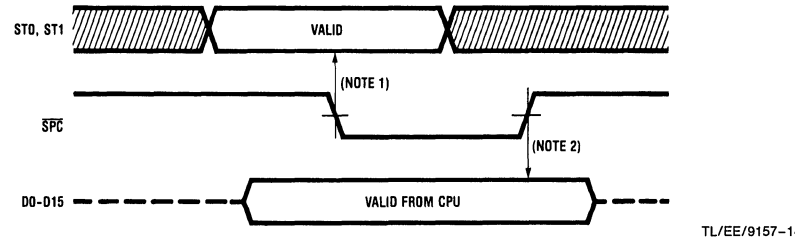
FIGURE 3-5. Slave Processor Read Cycle (NS32008, NS32016, NS32032 and NS32332 CPUs)

3.0 Functional Description (Continued)



Note 1: FPU samples CPU status here.

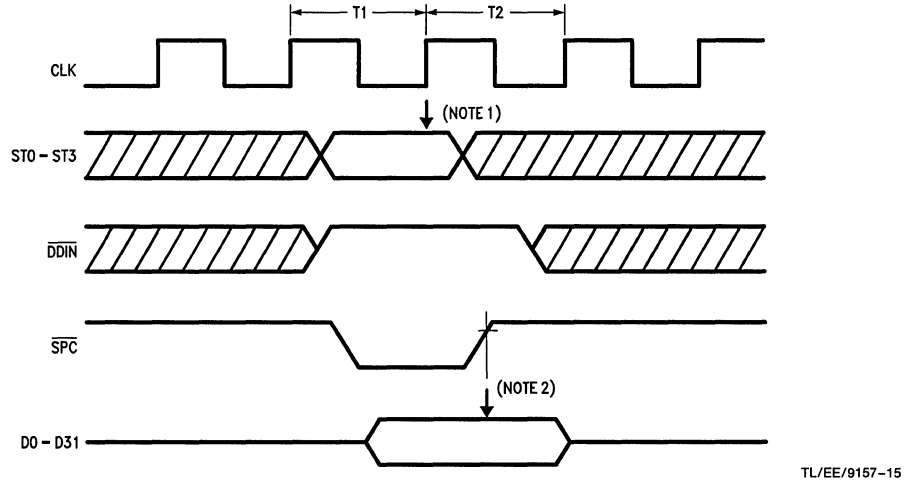
FIGURE 3-6. Slave Processor Read Cycle (NS32532 CPU)



Note 1: FPU samples CPU status here.

Note 2: FPU samples data bus here.

FIGURE 3-7. Slave Processor Write Cycle (NS32008, NS32016, NS32032 and NS32332 CPU)



Note 1: FPU samples CPU status here.

Note 2: FPU samples data bus here.

FIGURE 3-8. Slave Processor Write Cycle (NS32532 CPU)

3.0 Functional Description (Continued)

3.6 INSTRUCTION PROTOCOLS

3.6.1 General Protocol Sequences

The NS32381 supports both the 16-bit and 32-bit General Slave protocol sequences. See Tables 3-1, 3-2 and *Figures 3-12, 3-13* respectively.

Slave Processor instructions have a three-byte Basic Instruction field, consisting of an ID byte followed by an Operation Word. See *Figure 3-9* for the ID and Opcode format 16-bit Slave Protocol and *Figure 3-10* for the ID and Opcode Format 32-bit Slave Protocol. The ID Byte has three functions:

1) It identifies the instruction to the CPU as being a Slave Processor instruction.

2) It specifies which Slave Processor will execute it.

3) It determines the format of the following Operation Word of the instruction.

Upon receiving a Slave Processor instruction, the CPU initiates the sequence outlined in Table 3-3. Then depending on the state of the Protocol Select signals PS0 and PS1, either the 16-bit or a 32-bit Slave protocol is used. The NS32008, NS32016, NS32C016, NS32032 and the NS32C032 all communicate with the NS32381 using the 16-bit Slave Protocol. The NS32332 and NS32532 CPUs communicate with the NS32381 using a 32-bit Slave Protocol; a different version is provided for each CPU.

TABLE 3-1. 16-Bit General Slave Instruction Protocol

Step	Status	Action
1	ID (1111)	CPU sends ID Byte
2	OP (1101)	CPU sends Operation Word
3	OP (1101)	CPU sends required operands (if any)
4	—	Slaves starts execution (CPU prefetches)
5	—	Slave pulses $\overline{SPC}$ low
6	ST (1110)	CPU Reads Status Word
7	OP (1101)	CPU Reads Result (if destination is memory and if no TRAP occurred)

TABLE 3-2. 32-Bit General Slave Instruction Protocol

Step	Status	Action
1	ID (1111)	CPU sends ID and Operation Word
2	OP (1101)	CPU sends required operands (if any)
3	—	Slaves starts execution (CPU prefetches)
4	—	Slave signals DONE or TRAP or CMPf
5	ST (1110)	CPU Reads Status Word (If TRAP was signaled or a CMPf instruction was executed)
6	OP (1101)	CPU Reads Result (if destination is memory and if no TRAP occurred)

TABLE 3-3. Floating-Point Instruction Protocols

Mnemonic	Operand 1 Class	Operand 2 Class	Operand 1 Issued	Operand 2 Issued	Returned Value	PSR Bits Affected
ADDf	read.f	rmw.f	f	f	f to Op. 2	none
SUBf	read.f	rmw.f	f	f	f to Op. 2	none
MULf	read.f	rmw.f	f	f	f to Op. 2	none
DIVf	read.f	rmw.f	f	f	f to Op. 2	none
MOVf	read.f	write.f	f	N/A	f to Op. 2	none
ABSf	read.f	write.f	f	N/A	f to Op. 2	none
NEGf	read.f	write.f	f	N/A	f to Op. 2	none
CMPf	read.f	read.f	f	f	N/A	N,Z,L
FLOORfi	read.f	write.i	f	N/A	i to Op. 2	none
TRUNCfi	read.f	write.i	f	N/A	i to Op. 2	none
ROUNDfi	read.f	write.i	f	N/A	i to Op. 2	none
MOVFL	read.F	write.L	F	N/A	L to Op. 2	none
MOVLF	read.L	write.F	L	N/A	F to Op. 2	none
MOVif	read.i	write.f	i	N/A	f to Op. 2	none
LFSR	read.D	N/A	D	N/A	N/A	none
SFSR	N/A	write.D	N/A	N/A	D to Op. 2	none
SCALBf	read.f	rmw.f	f	f	f to Op.2	none
LOGBf	read.f	write.f	f	N/A	f to Op.2	none
DOTf	read.f	read.f	f	f	f to FO	none
POLYf	read.f	read.f	f	f	f to FO	none

D = Double Word

i = Integer size (B, W, D) specified in mnemonic.

f = Floating-Point type (F, L) specified in mnemonic.

N/A = Not Applicable to this instruction.

3.0 Functional Description (Continued)

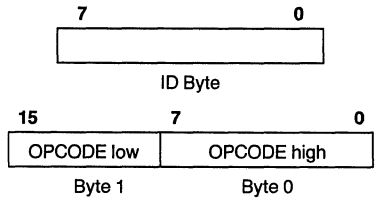


FIGURE 3-9. ID and OPCODE Format 16-Bit Slave Protocol

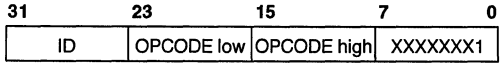


FIGURE 3-10. ID and OPCODE Format 32-Bit Slave Protocol

For the 16-bit Slave Protocol the CPU applies Status Code 1111 (Broadcast ID. Tables 3-1, 3-2), and sends the ID Byte on the least significant half of the Data Bus (D0–D7). The CPU next sends the Operation Word while applying Status Code 1101 (Transfer Slave Operand, Tables 3-1, 3-2). The Operation Word is swapped on the Data Bus; that is, bits 0–7 appear on pins D8–D15, and bits 8–15 appear on pins D0–D7.

For the 32-bit Slave Protocol the CPU applies Status Code 1111 and sends the ID Byte (different ID for each format) in byte 3 (D24–D31) and the Operation Word in bytes 1 and 2 in a single double word transfer. The Operation Word is swapped such that OPCODE low appears on byte 2 (D16–D23) and OPCODE high appears on byte 1 (D8–D15). Byte 0 (D0–D7) is not used.

All Slave Processors input and decode the data from these transfers. The Slave Processor selected by the ID Byte is activated and from this point the CPU is communicating only with it. If any other slave protocol is in progress (e.g., an aborted Slave instruction), this transfer cancels it. At this point also, both the CPU and FPU are aware of the number of operands to be transferred and their sizes.

Using the Addressing Mode fields within the Operation Word, the CPU starts fetching operands and issuing them to the FPU. To do so, it references any Addressing Mode extensions appended to the FPU instruction. Since the CPU is solely responsible for memory accesses, these extensions are not sent to the Slave Processor. The Status Code applied is 1101 (Transfer Slave Processor Operand, Tables 3-1, 3-2).

After the CPU has issued the last operand, the FPU starts the actual execution of the instruction. A one clock cycle $\overline{SPC}$ pulse is used to indicate the completion of the instruction and for the CPU to continue with the 16-Bit Slave Protocol by reading the FPU's status word.

For the 32-bit Slave Protocol, upon completion of the instruction, the FPU will signal the CPU by pulsing either $\overline{SDNXXX}$ or $\overline{FSSR}$ (Force Slave Status Read).

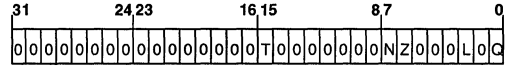
A half clock cycle $\overline{SDN332}$ pulse with a NS32332 CPU indicates a valid completion of the instruction and that there is no need for the CPU to read its Status Word.

A two and a half clock cycle $\overline{SDN332}$ pulse indicates that there is a need for the CPU to read its Status Word. In the case of the NS32532 CPU, a one clock cycle $\overline{SDN532}$ pulse indicates a valid completion of the instruction and that there is no need to read the Status Word.

A one clock cycle $\overline{FSSR}$ pulse is used to indicate the need for the CPU to read the Status Word.

In all cases and for both the 16-Bit and 32-Bit Slave Protocols the CPU will use $\overline{SPC}$ to read the Status Word from the FPU, while applying status code (1110). This word has the format shown in *Figure 3-11*. If the Q bit ("Quit", Bit 0) is set, this indicates that an error (TRAP) has been detected by the FPU. The CPU will not continue the protocol, but will immediately trap through the Slave vector in the Interrupt Table. If the instruction being performed is CMPf (Section 2.2.3) and the Q bit is not set, the CPU loads Processor Status Register (PSR) bits N, Z and L from the corresponding bits in the FPU Status Word. The FPU always sets the L bit to zero.

The last step in the Slave Protocol if no errors have occurred and the result's destination is memory will be for the CPU to read the result. Here again the CPU uses $\overline{SPC}$ to read the result from the FPU and transfer it to its destination. These Read cycles from the FPU are performed by the CPU while applying Status Code 1101 (Transfer Slave Operand).



Bit		Description
(0)	Q:	Set to "1" if an FPU TRAP (error) occurred. Cleared to '0" by a valid CMPf.
(2)	L:	Cleared to "0" by the FPU.
(6)	Z:	Set to "1" if the second operand is equal to the first operand. Otherwise it is cleared to "0".
(7)	N:	Set to "1" if the second operand is less than the first operand. Otherwise it is cleared to "0".
(15)	T:	Set to "1" if the TRAP is (UND) and cleared to "0" if the TRAP is (FPU).

FIGURE 3-11. FPU Status Word Format

3.0 Functional Description (Continued)

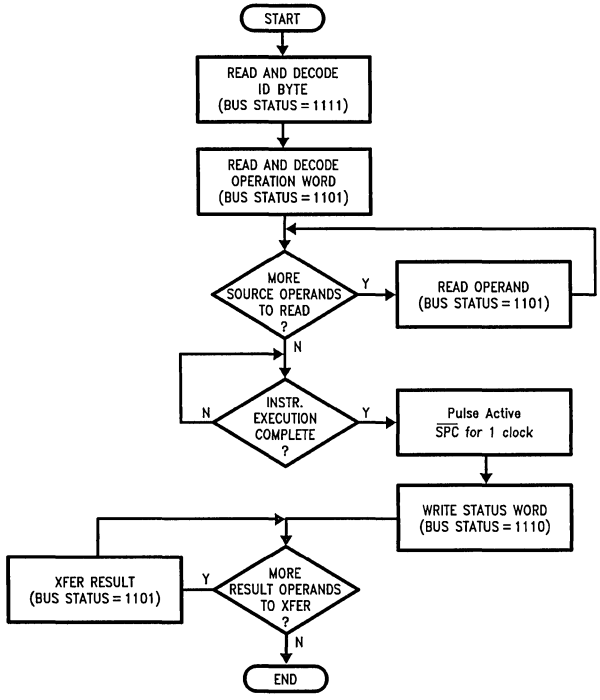


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FIGURE 3-12. 16-Bit General Slave Instruction Protocol: FPU Actions

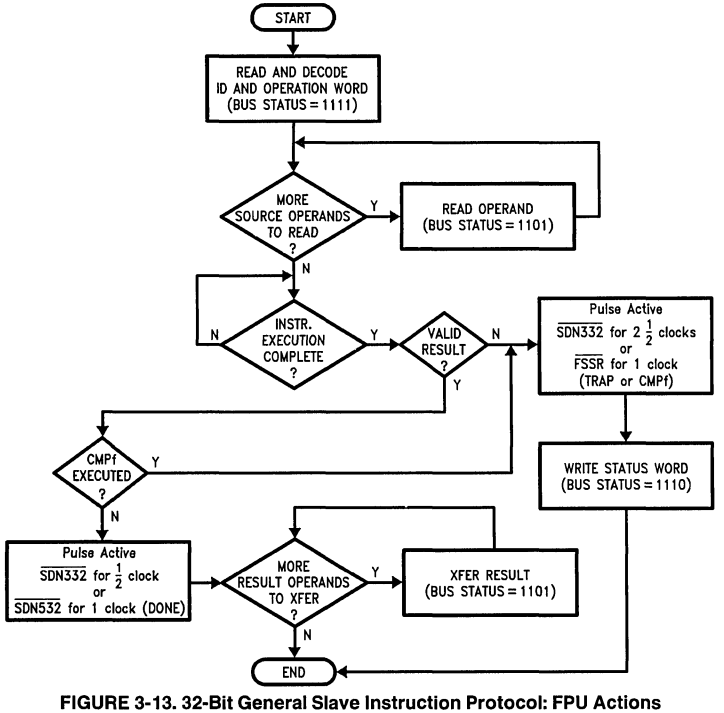

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FIGURE 3-13. 32-Bit General Slave Instruction Protocol: FPU Actions

3.0 Functional Description (Continued)

3.6.2 Early Done Algorithm

The NS32381 has the ability to modify the General Slave protocol sequences and to boost the performance of the FPU by 20% to 40%. This is called the Early Done Algorithm.

Early Done is defined by the fact that the destination of an instruction is an FPU register and that the instruction and range of operands cannot generate a TRAP (error). When these conditions are met the FPU will send a $\overline{\text{SDNXXX}}$ or $\overline{\text{SPC}}$ pulse after receiving all of the operands from the CPU and before executing the instruction, hence an early done as compared to the General Slave Protocols.

In the case of the 16-bit Slave Protocol in which the CPU always reads the slave status word, the FPU will force all zeroes to be read. The CPU can then send the next instruction to the FPU saving the general protocol overhead. The FPU will start the new instruction immediately after finishing the previous instruction.

SFSR, CMPF and CMPL do not generate an Early Done.

3.6.3 Floating-Point Protocols

Table 3-3 gives the protocols followed for each floating-point instruction. The instructions are referenced by their mnemonics. For the bit encodings of each instruction, see section 2.2.3.

The Operand Class columns give the Access Classes for each general operand, defining how the addressing modes are interpreted by the CPU (see Series 32000 Instruction Set Reference Manual).

The Operand Issued columns show the sizes of the operands issued to the Floating-Point Unit by the CPU. "D" indicates a 32-bit Double Word. "i" indicates that the instruction specifies an integer size for the operand (B = Byte, W = Word, D = Double Word). "f" indicates that the instruction specifies a floating-point size for the operand (F = 32-bit Standard Floating, L = 64-bit Long Floating).

The Returned Value Type and Destination column gives the size of any returned value and where the CPU places it. The PSR Bits Affected column indicates which PSR bits, if any, are updated from the FPU Status Word (*Figure 3-11*).

Any operand indicated as being of type "f" will not cause a transfer if the Register addressing mode is specified, because the Floating-Point Registers are physically on the Floating-Point Unit and are therefore available without CPU assistance.

4.0 Device Specifications

4.1 PIN DESCRIPTIONS

4.1.1 Supplies

The following is a brief description of all NS32381 pins.

V_{CC} — Power: +5V positive supply.

GND — Ground: Ground reference for both on-chip logic and drivers connected to output pins.

4.1.2 Input Signals

CLK — Clock: TTL-level clock signal.

$\overline{\text{DDIN}}$ — Data Direction In: Active low. Status signal indicating the direction of data transfers during a bus cycle.

ST0–ST3 — Status: Bus cycle status code from CPU. ST0 is the least significant and rightmost bit.

1100— Reserved

1101— Transferring Operation Word or Operand

1110— Reading Status Word

1111— Broadcasting Slave ID

Note: The NS32332 generates four status lines and the NS32532 generates five. The user should connect the status lines as shown below:

NS32381	NS32332	NS32532
ST0	ST0	ST0
ST1	ST1	ST1
ST2	ST2	ST2
ST3	ST3	ST4

$\overline{\text{RST}}$ — Reset: Active low. Resets the last operation and clears the FSR register.

NOE — New Opcode Enable: Active high. This signal enables the new opcodes available in the NS32381.

PS0, PS1 — Protocol Select: Selects the slave protocol to be used. PS0 is the least significant and rightmost bit.

00—Selects 16-bit protocol.
01—Selects 32-bit protocol for NS32332.
10—Reserved.
11—Selects 32-bit protocol for NS32532.

4.1.3 Output Signals

$\overline{\text{SDN332}}$ — Slave Done 332: Active low. This signal is for use with the NS32332 CPU only. If held active for a half clock cycle and released this pin indicates the successful completion by the FPU of a floating-point instruction. Holding this pin active for two and a half clock cycles indicates TRAP or that the CMPf instruction has been executed.

$\overline{\text{SDN532}}$ — Slave Done 532: Active low. This signal is for use with the NS32532 CPU only. When active it indicates successful completion by the FPU of a floating-point instruction.

$\overline{\text{FSSR}}$ — Force Slave Status Read: Active low. This signal is for use with the NS32532 CPU only. When active it indicates TRAP or that the CMPf instruction has been executed.

4.1.4 Input/Output Signals

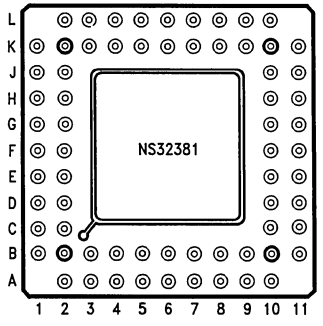
*D0–D31 — Data Bus: These are the 32 signal lines which carry data between the NS32381 and the CPU.

$\overline{\text{SPC}}$ — Slave Processor Control: Active low. This is the data strobe signal for slave transfers. For the 32-bit protocol, $\overline{\text{SPC}}$ is only an input signal.

*For the 16-bit Slave Protocol the upper sixteen data input signals (D16–D31) should be left floating.

4.0 Device Specifications (Continued)

Connection Diagram



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Bottom View

Order Number NS32381
See NS Package Number U68D

FIGURE 4-1. 68-Pin PGA Package
NS32381 Pinout Descriptions

Desc	Pin
V_{CC}	A2
D1	A3
D0	A4
PS1 (Note 1)	A5
GND	A6
GND	A7
CLK	A8
$\overline{RST}$	A9
Reserved (Note 2)	A10
Reserved (Note 2)	B1
D2	B2
D17	B3
D16	B4
PS0 (Note 1)	B5
GND	B6
NOE (Note 1)	B7
Reserved (Note 3)	B8
Reserved (Note 2)	B9
V_{CC}	B10
D15	B11
D18	C1
D3	C2
D31	C10
D14	C11
D19	D1
V_{CC}	D2
D30	D10
V_{CC}	D11
D4	E1
D20	E2
D13	E10
D29	E11
Reserved (Note 3)	F1
D5	F2

Desc	Pin
D28	F10
GND	F11
GND	G1
D21	G2
D12	G10
D27	G11
D6	H1
D22	H2
D11	H10
$\overline{SDN332}$	H11
D7	J1
D23	J2
$\overline{SPC}$	J10
$\overline{SDN532}$	J11
V_{CC}	K1
D8	K2
GND	K3
D26	K4
GND	K5
V_{CC}	K6
Reserved (Note 3)	K7
ST0	K8
ST1	K9
Reserved (Note 3)	K10
GND	K11
D24	L2
D25	L3
D9	L4
D10	L5
$\overline{DDIN}$	L6
V_{CC}	L7
ST2	L8
ST3	L9
$\overline{FSSR}$	L10

Note 1: CMOS input; never float.

Note 2: Pin should be grounded.

Note 3: Pin should be left floating.

4.0 Device Specifications (Continued)

4.2 ABSOLUTE MAXIMUM RATINGS

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Temperature Under Bias	0°C to +70°C
Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to GND	−0.5V to +7.0V
Power Dissipation	1.5W
Power Down Mode	0.15W

ESD Rating is to be determined.

Note: *Absolute maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended; operation should be limited to those conditions specified under Electrical Characteristics.*

4.3 ELECTRICAL CHARACTERISTICS T_A = 0°C to 70°C, V_{CC} = 5V ±5%, GND = 0V

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High Level Input Voltage*		2.0		V_{CC} +0.5	V
V_{IL}	Low Level Input Voltage*		−0.5		0.8	V
V_{OH}	High Level Output Voltage	I_{OH} = −400 μA	2.4			V
V_{OL}	Low Level Output Voltage	I_{OL} = 2 mA			0.4	V
I_I	Input Load Current*	0 ≤ V_{IN} ≤ V_{CC}	−10.0		10.0	μA
V_{IH}	High Level Input Voltage for PS0, PS1, NOE		3.5		V_{CC} +0.5	V
V_{IL}	Low Level Input Voltage for PS0, PS1, NOE		−0.5		1.5	V
I_I	Input Load Current for PS0, PS1, NOE	0 ≤ V_{IN} ≤ V_{CC}	−100		100	μA
I_L	Leakage Current (Output and I/O Pins in TRI-STATE®/Input Mode)	0.4 ≤ V_{OUT} ≤ 2.4V	−20.0		20.0	μA
I_{CC}	Active Supply Current	I_{OUT} = 0, T_A = 25°C			300	mA
I_{CC}	Power Down Current	I_{OUT} = 0, T_A = 25°C			30	mA
C_{IN}	Input Capacitance			6	10	pF
C_{OUT}	Output Capacitance			8	12	pF

*Except PS0, PS1, NOE and Reserved pins.

4.4 SWITCHING CHARACTERISTICS

4.4.1 Definitions

All the Timing Specifications given in this section refer to 0.8V and 2.0V on all the input and output signals as illustrated in *Figures 4.2* and *4.3,* unless specifically stated otherwise.

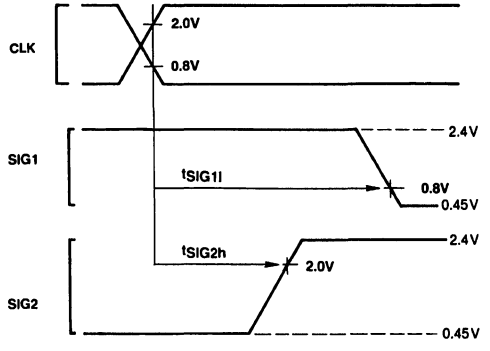

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FIGURE 4-2. Timing Specification Standard (Signal Valid after Clock Edge)

ABBREVIATIONS

L.E. — Leading Edge R.E. — Rising Edge

T.E. — Trailing Edge F.E. — Falling Edge

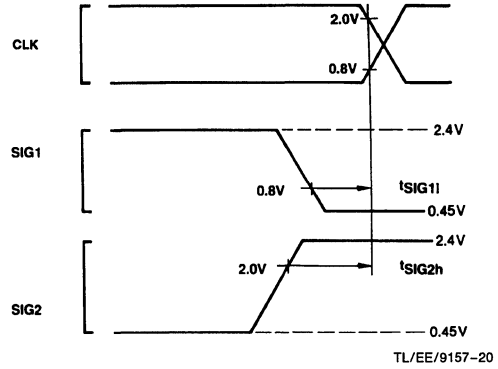

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FIGURE 4-3. Timing Specification Standard (Signal Valid before Clock Edge)

4.0 Device Specifications (Continued)

4.4.2 Timing Tables (Maximum times assume temperature range 0°C to 70°C)

4.4.2.1 Output Signal Propagation Delays for all CPUs
(Maximum times assume capacitive loading of 100 pF)

Symbol	Figure	Description	Reference/ Conditions	NS32381-15		NS32381-20		Units
				Min	Max	Min	Max	
t_{SPCF_w}	4-18	$\overline{SPC}$ Pulse Width from FPU	At 0.8V (Both Edges)	$\frac{1}{2}t_{CLK_p} - 10$	$\frac{1}{2}t_{CLK_p} + 10$	$\frac{1}{2}t_{CLK_p} - 10$	$\frac{1}{2}t_{CLK_p} + 10$	ns
t_{SPCF_a}	4-18	$\overline{SPC}$ Output Active	After CLK R.E.		38		33	ns
t_{SPCF_i}	4-18	$\overline{SPC}$ Output Inactive	After CLK R.E.	18	38	18	33	ns
$t_{SPCF_{nf}}$	4-18	$\overline{SPC}$ Output Nonforcing	After CLK F.E.		35		30	ns

4.4.2.2 Output Signal Propagation Delays for the NS32008, NS32016 and NS32032 CPUs
Maximum times assumes capacitive loading of 100 pF

Symbol	Figure	Description	Reference/ Conditions	NS32381-15		NS32381-20		Units
				Min	Max	Min	Max	
t_{D_v}	4-8	Data Valid (D0–D15)	After $\overline{SPC}$ L.E.		30			ns
t_{D_f}	4-8	D0–D15 Floating	After $\overline{SPC}$ T.E.		30			ns

4.4.2.3 Output Signal Propagation Delays for the 32-Bit Slave Protocol NS32332 CPU
Maximum times assume capacitive loading of 100 pF unless otherwise specified

Symbol	Figure	Description	Reference/ Conditions	NS32381-15		NS32381-20		Units
				Min	Max	Min	Max	
t_{D_v}	4-10	Data Valid	After $\overline{SPC}$ L.E.; 75 pF Cap. Loading		30		25	ns
$t_{D_{Iv}}$	4-10	Data Invalid	After $\overline{SPC}$ T.E.	18		18		ns
$t_{D_{nf}}$	4-10	Data Nonforcing	After $\overline{SPC}$ T.E.		30		30	ns
t_{SDN_a}	4-12, 13	Slave Done Active	After CLK F.E.	3	33	3	33	ns
t_{SDN_h}	4-13	Slave Done Hold	After CLK R.E.		33		33	ns
t_{SDN_w}	4-12	Slave Done Pulse Width	At 0.8V (Both Edges)	$\frac{1}{2}t_{CLK_p} - 10$	$\frac{1}{2}t_{CLK_p} + 10$	$\frac{1}{2}t_{CLK_p} - 10$	$\frac{1}{2}t_{CLK_p} + 10$	ns
$t_{SDN_{nf}}$	4-12, 13	Slave Done Nonforcing	After CLK R. E.		30		30	ns
t_{STRP_w}	4-13	Slave Done (TRAP) Pulse Width	At 0.8V (Both Edges)	$2\frac{1}{2}t_{CLK_p} - 10$	$2\frac{1}{2}t_{CLK_p} + 10$	$2\frac{1}{2}t_{CLK_p} - 10$	$2\frac{1}{2}t_{CLK_p} + 10$	ns

4.0 Device Specifications (Continued)

4.4.2.4 Output Signal Propagation Delays for the 32-Bit Slave Protocol NS32532 CPU

Maximum times assume capacitive loading of 75 pF

Symbol	Figure	Description	Reference/ Conditions	NS32381-								Units
				15		20		25		30		
				Min	Max	Min	Max	Min	Max	Min	Max	
t_{D_v}	4-14	Data Valid	After $\overline{SPC}$ L.E.		30		25		25		25	ns
$t_{D_{lv}}$	4-14	Data Invalid	After CLK R.E.	3		3		3		3		ns
$t_{D_{nf}}$	4-14	Data Nonforcing	After $\overline{SPC}$ T.E.		30		30		30		30	ns
t_{SD_a}	4-16	Slave Done Active	After CLK R.E.		40		35		25		25	ns
t_{SD_h}	4-16	Slave Done Hold	After CLK R.E.	2	38	2	33	2	25	2	25	ns
$t_{SD_{nf}}$	4-16	Slave Done Nonforcing	After CLK R. E.		35		30		30		30	ns
t_{FSSR_a}	4-17	Forced Slave Status Read Active	After CLK R.E.		40		35		25		25	ns
t_{FSSR_h}	4-17	Forced Slave Status Read Hold	After CLK R.E.	2	38	2	33	2	25	2	25	ns
$t_{FSSR_{nf}}$	4-17	Forced Slave Status Read Nonforcing	After CLK R.E.		35		30		30		30	ns

4.4.2.5 Input Signal Requirements with all CPUs

Symbol	Figure	Description	Reference/ Conditions	NS32381-								Units
				15		20		25		30		
				Min	Max	Min	Max	Min	Max	Min	Max	
t_{PWR}	4-5	Power-On Reset Duration	After CLK R.E.	30		30		30		30		μs
t_{RST_w}	4-6	Reset Pulse Width	At 0.8V (Both Edges)	64		64		64		64		t_{CLK_p}
t_{RST_s}	4-7	Reset Release	Before CLK F.E.	10		10		10		10		ns
t_{RST_h}	4-7	Reset Hold	After CLK R.E.	0		0		0		0		ns

4.4.2.6 Input Signal Requirements with the NS32008, NS32016, NS32032 CPUs

Symbol	Figure	Description	Reference/ Conditions	NS32381-15		NS32381-20		Units
				Min	Max	Min	Max	
t_{S_s}	4-8	Status (ST0–ST1) Setup	Before $\overline{SPC}$ L.E.	25		20		ns
t_{S_h}	4-8	Status (ST0–ST1) Hold	After $\overline{SPC}$ L.E.	20		20		ns
t_{D_s}	4-9	Data Setup (D0–D15)	Before $\overline{SPC}$ T.E.	25		20		ns
t_{D_h}	4-9	Data Hold (D0–D15)	After $\overline{SPC}$ T.E.	20		20		ns
t_{SPC_w}	4-8	$\overline{SPC}$ Pulse Width from CPU	At 0.8V (Both Edges)	35		35		ns

4.0 Device Specifications (Continued)

4.4.2.7 Input Signal Requirements with the 32-Bit Slave Protocol NS32332 CPU

Symbol	Figure	Description	Reference/ Conditions	NS32381-15		NS32381-20		Units
				Min	Max	Min	Max	
t_{ST_s}	4-11	Status Setup	Before $\overline{SPC}$ L.E.	25		20		ns
t_{ST_h}	4-11	Status Hold	After $\overline{SPC}$ L.E.	20		20		ns
t_{D_s}	4-11	Data Setup	Before $\overline{SPC}$ T.E.	25		20		ns
t_{D_h}	4-11	Data Hold	After $\overline{SPC}$ T.E.	20		20		ns
t_{SPC_w}	4-11	$\overline{SPC}$ Pulse Width	At 0.8V (Both Edges)	35		35		ns

4.4.2.8 Input Signal Requirements with the 32-Bit Slave Protocol NS32532 CPU

Symbol	Figure	Description	Reference/ Conditions	NS32381								Units
				15		20		25		30		
				Min	Max	Min	Max	Min	Max	Min	Max	
t_{ST_s}	4-15	Status Setup	Before CLK (T2) R.E.	25		25		20		15		ns
t_{ST_h}	4-15	Status Hold	After CLK (T2) R.E.	25		20		10		10		ns
t_{DDIN_s}	4-15	Data Direction In Setup	Before $\overline{SPC}$ L.E.	0		0		0		0		ns
t_{DDIN_h}	4-15	Data Direction In Hold	After $\overline{SPC}$ T.E.	10		10		10		10		ns
t_{D_s}	4-15	Data Setup	Before $\overline{SPC}$ T.E.	10		6		6		6		ns
t_{D_h}	4-15	Data Hold	After $\overline{SPC}$ T.E.	20		20		10		10		ns
t_{SPC_s}	4-15	$\overline{SPC}$ Setup	Before CLK (T2) R.E.	20		20		20		20		ns
t_{SPC_h}	4-15	$\overline{SPC}$ Hold	After CLK (T2) R.E.	0		0		0		0		ns
$t_{SPC_{ia}}$	4-14	$\overline{SPC}$ Inactive	After CLK (T1) R.E.					0		0		ns
t_{SPC_a}	4-14	$\overline{SPC}$ Active	After CLK (T1) R.E.					3		3		ns

4.4.2.9 Clocking Requirements with all CPUs

Symbol	Figure	Description	Reference/ Conditions	NS32381								Units
				15		20		25		30		
				Min	Max	Min	Max	Min	Max	Min	Max	
t_{CLK_h}	4-4	Clock High Time	At 2.0 V (Both Edges)	25	1000	20	1000	18	1000	16	1000	ns
t_{CLK_l}	4-4	Clock Low Time	At 0.8V (Both Edges)	25	DC	20	DC	18	DC	16	DC	ns
t_{CT_r}	4-4	Clock Rise Time	Between 0.8V and 2.0V		7		5		4		3	ns
t_{CT_d}	4-4	Clock Fall Time	Between 2.0V and 0.8V		7		5		4		3	ns
t_{CLK_p}	4-4	Clock Period	CLK R.E. to Next CLK R.E.	66	DC	50	DC	40	DC	33.3	DC	ns

4.0 Device Specifications (Continued)

4.4.3 Timing Diagrams

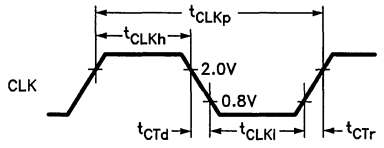

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FIGURE 4-4. Clock Timing

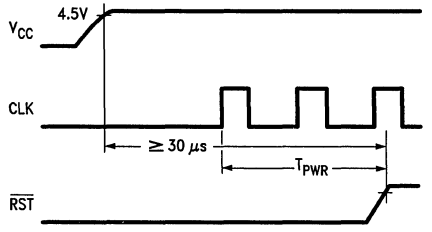

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FIGURE 4-5. Power-On Reset

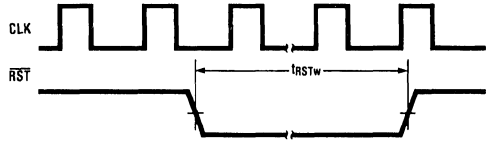

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FIGURE 4-6. Non-Power-On Reset

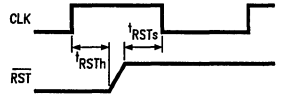

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FIGURE 4-7. $\overline{RST}$ Release Timing

Note: The rising edge of $\overline{RST}$ must occur while CLK is high, as shown.

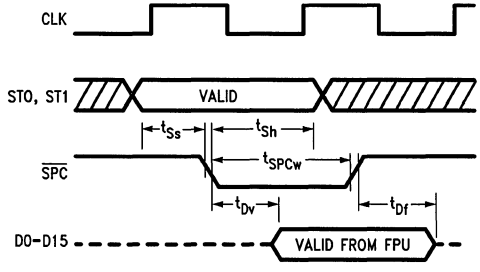

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FIGURE 4-8. Read Cycle from FPU (NS32008, NS32016, NS32032 CPUs)

4.0 Device Specifications (Continued)

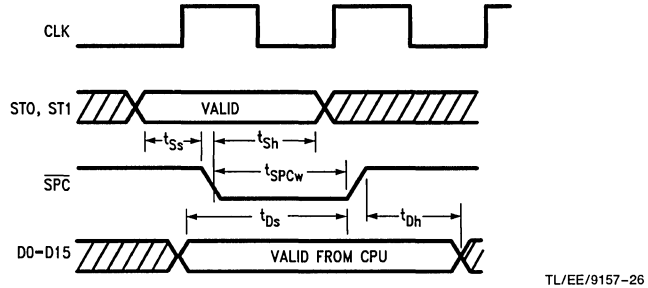

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FIGURE 4-9. Write Cycle to FPU (NS32008, NS32016, NS32032 CPUs)

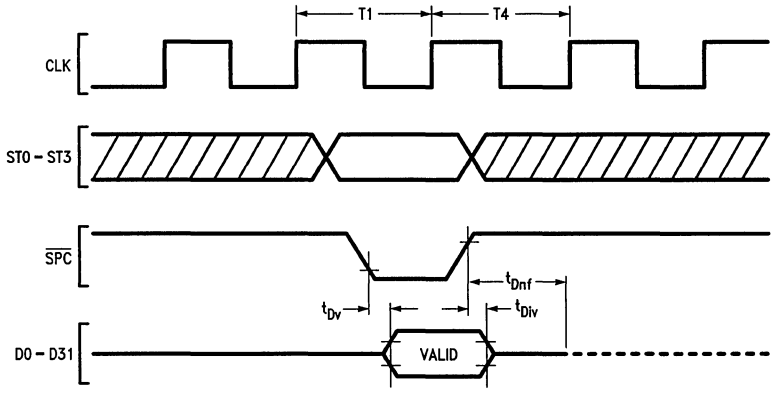

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FIGURE 4-10. Read Cycle from FPU (NS32332 CPU)

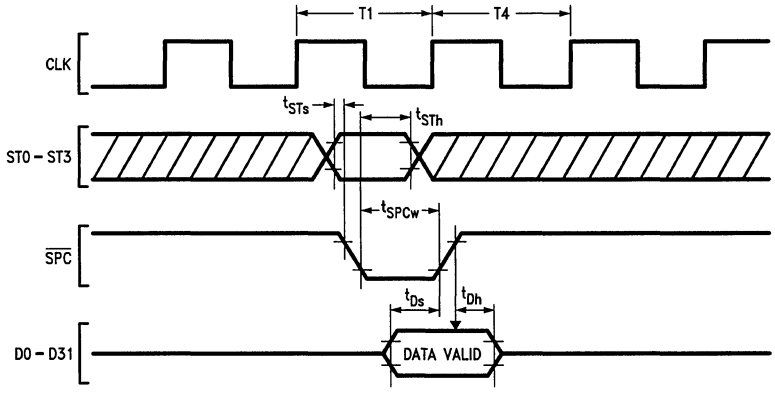

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FIGURE 4-11. Write Cycle to FPU (NS32332 CPU)

3

4.0 Device Specifications (Continued)

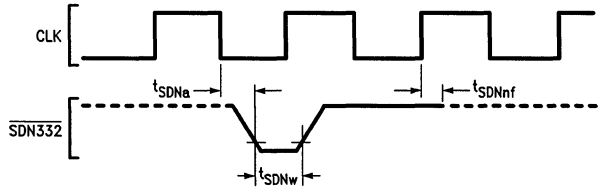

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FIGURE 4-12. $\overline{SDN332}$ Timing (NS32332 CPU)

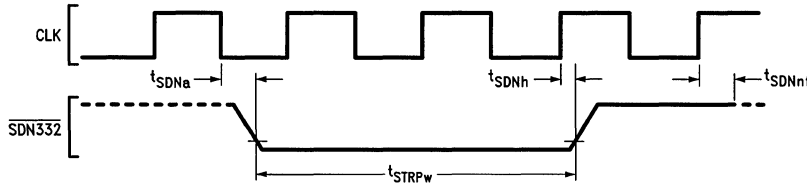

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FIGURE 4-13. $\overline{SDN332}$ (TRAP) Timing (NS32332 CPU)

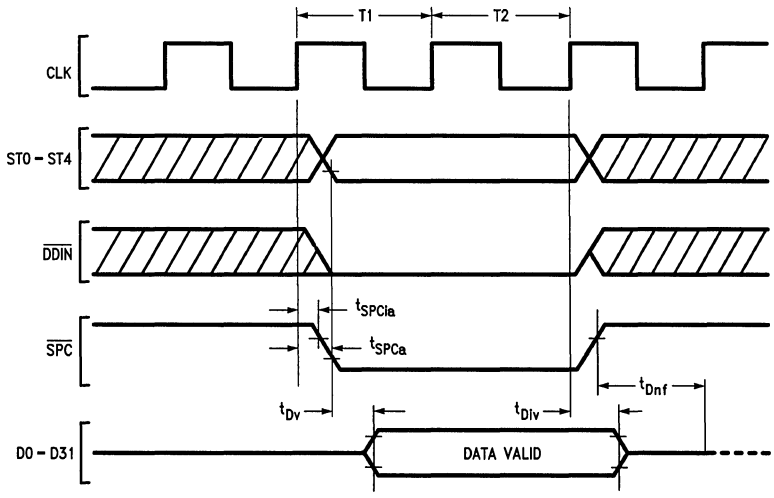

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FIGURE 4-14. Read Cycle from FPU (NS32532 CPU)

4.0 Device Specifications (Continued)

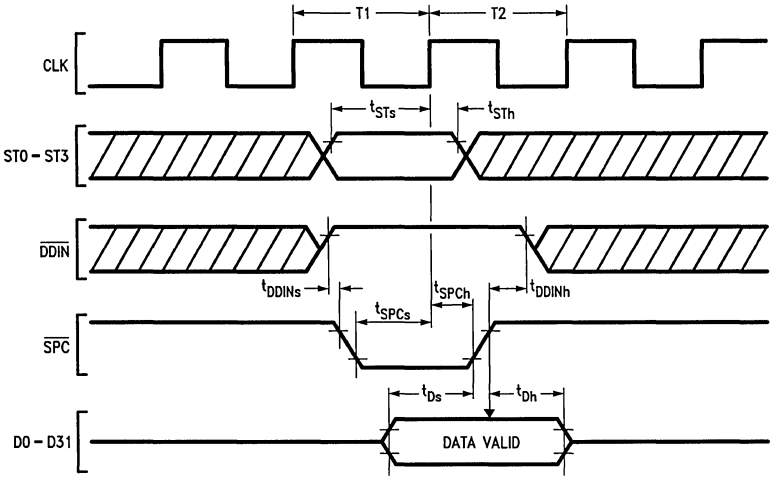

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FIGURE 4-15. Write Cycle to FPU (NS32532 CPU)

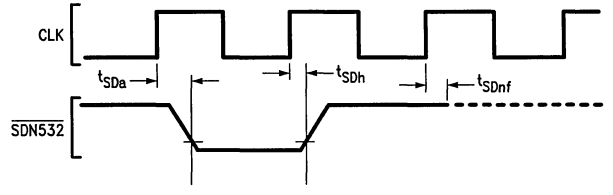

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FIGURE 4-16. SDN532 Timing (NS32532 CPU)

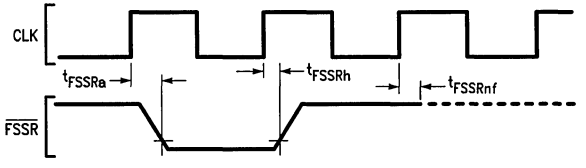

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FIGURE 4-17. FSSR Timing (NS32532 CPU)

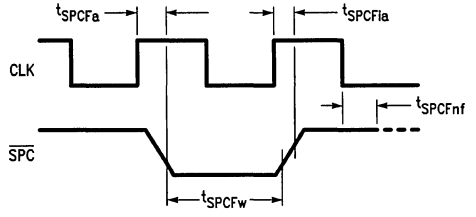

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FIGURE 4-18. SPC Pulse from FPU

Appendix A

NS32381 PERFORMANCE ANALYSIS

The following performance numbers were taken from simulations using the 381 SIMPLE model. The timing terms have been designed to provide performance numbers which are CPU independent. Numbers were obtained from SIMPLE simulations, taking the average execution times using 'typical' operands.

Listed below are definitions of the timing terms:

EXT — (EXecution Time) This is the time from the last data sent to the FPU, until the early DONE is issued. (FPU Pipe is empty)

EDD — (Early Done Delta) This is the time from when the early DONE is issued until the execution of the next instruction may start.

Provided that the CPU can transfer the ID/OPCODE and any operands to the FPU during the EDD time, the average system execution time for an instruction (keeping the FPU pipe filled) is: EXT + EDD.

The system execution time for a single FPU instruction with FPU register destination and early done is: EXT plus the protocol time. (FPU pipe is initially empty)

Instruction	EXT	EDD	Total
LFSR any, reg	5	8	13
MOVF any, reg	5	6	11
MOVL any, reg	5	8	13
MOVif any, reg	5	45	50
MOVFL any, reg	9	6	15
ADDF any, reg	11	31	42
ADDL any, reg	11	31	42
SUBF any, reg	11	31	42
SUBL any, reg	11	31	42
MULF any, reg	11	20	31
MULL any, reg	11	27	38
DIVF any, reg	11	45	56
DIVL any, reg	11	59	70
POLYF any, any	15	46	61
POLYL any, any	15	53	68
DOTF any, any	15	46	61
DOTL any, any	15	53	68

NS32381 PERFORMANCE ANALYSIS

The following instructions do not generate an early done. In this case, EXT is the time from the last data sent to the FPU, until the normal DONE is issued. (FPU Pipe is empty)

Instruction	EXT
SFSR reg, mem	7
MOVLF any, any	18
ROUNDfi any, mem	46
FLOORfi any, mem	46
TRUNCfi any, mem	46
CMPF any, any	17
CMPL any, any	17
ABSf any, any	9
NEGf any, any	9
SCALBf any, any	49
LOGBf any, any	36

National Semiconductor

NS32081-10/NS32081-15 Floating-Point Units

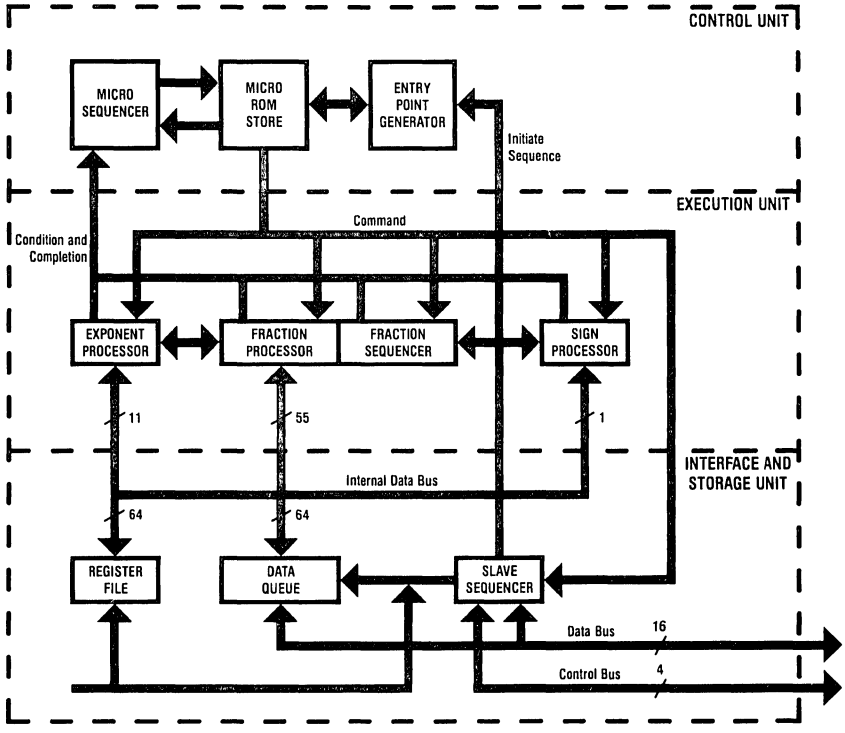
General Description

The NS32081 Floating-Point Unit functions as a slave processor in National Semiconductor's Series 32000® microprocessor family. It provides a high-speed floating-point instruction set for any Series 32000 family CPU, while remaining architecturally consistent with the full two-address architecture and powerful addressing modes of the Series 32000 micro-processor family.

Features

- Eight on-chip data registers
- 32-bit and 64-bit operations
- Supports proposed IEEE standard for binary floating-point arithmetic, Task P754
- Directly compatible with NS32016, NS32008 and NS32032 CPUs
- High-speed XMOS™ technology
- Single 5V supply
- 24-pin dual in-line package

Block Diagram



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1.0 Product Introduction

The NS32081 Floating-Point Unit (FPU) provides high speed floating-point operations for the Series 32000 family, and is fabricated using National high-speed XMOS technology. It operates as a slave processor for transparent expansion of the Series 32000 CPU's basic instruction set. The FPU can also be used with other microprocessors as a peripheral device by using additional TTL interface logic. The NS32081 is compatible with the IEEE Floating-Point Formats by means of its hardware and software features.

1.1 OPERAND FORMATS

The NS32081 FPU operates on two floating-point data types—single precision (32 bits) and double precision (64 bits). Floating-point instruction mnemonics use the suffix F (Floating) to select the single precision data type, and the suffix L (Long Floating) to select the double precision data type.

A floating-point number is divided into three fields, as shown in *Figure 1-1*.

The F field is the fractional portion of the represented number. In Normalized numbers (Section 1.1.1), the binary point is assumed to be immediately to the left of the most significant bit of the F field, with an implied 1 bit to the left of the binary point. Thus, the F field represents values in the range $1.0 \leq x \leq 2.0$.

TABLE 1-1. Sample F Fields

F Field	Binary Value	Decimal Value
000 . . . 0	1.000 . . . 0	1.000 . . . 0
010 . . . 0	1.010 . . . 0	1.250 . . . 0
100 . . . 0	1.100 . . . 0	1.500 . . . 0
110 . . . 0	1.110 . . . 0	1.750 . . . 0
	↑	
	Implied Bit	

The E field contains an unsigned number that gives the binary exponent of the represented number. The value in the E field is biased; that is, a constant bias value must be subtracted from the E field value in order to obtain the true exponent. The bias value is $011 \ldots 11_2$, which is either 127 (single precision) or 1023 (double precision). Thus, the true exponent can be either positive or negative, as shown in Table 1-2.

TABLE 1-2. Sample E Fields

E Field	F Field	Represented Value
011 . . . 110	100 . . . 0	$1.5 \times 2^{-1} = 0.75$
011 . . . 111	100 . . . 0	$1.5 \times 2^{0} = 1.50$
100 . . . 000	100 . . . 0	$1.5 \times 2^{1} = 3.00$

Two values of the E field are not exponents. 11 . . . 11 signals a reserved operand (Section 2.1.3). 00 . . . 00 represents the number zero if the F field is also all zeroes, otherwise it signals a reserved operand.

The S bit indicates the sign of the operand. It is 0 for positive and 1 for negative. Floating-point numbers are in sign-magnitude form, that is, only the S bit is complemented in order to change the sign of the represented number.

1.1.1 Normalized Numbers

Normalized numbers are numbers which can be expressed as floating-point operands, as described above, where the E field is neither all zeroes nor all ones.

The value of a Normalized number can be derived by the formula:

$$(-1)^{S} \times 2^{(E\text{-}Bias)} \times (1 + F)$$

The range of Normalized numbers is given in Table 1-3.

1.1.2 Zero

There are two representations for zero—positive and negative. Positive zero has all-zero F and E fields, and the S bit is zero. Negative zero also has all-zero F and E fields, but its S bit is one.

1.1.3 Reserved Operands

The proposed IEEE Standard for Binary Floating-Point Arithmetic (Task P754) provides for certain exceptional forms of floating-point operands. The NS32081 FPU treats these forms as reserved operands. The reserved operands are:

- Positive and negative infinity
- Not-a-Number (NaN) values
- Denormalized numbers

Both Infinity and NaN values have all ones in their E fields. Denormalized numbers have all zeroes in their E fields and non-zero values in their F fields.

The NS32081 FPU causes an Invalid Operation trap (Section 2.1.2.2) if it receives a reserved operand, unless the operation is simply a move (without conversion). The FPU does not generate reserved operands as results.

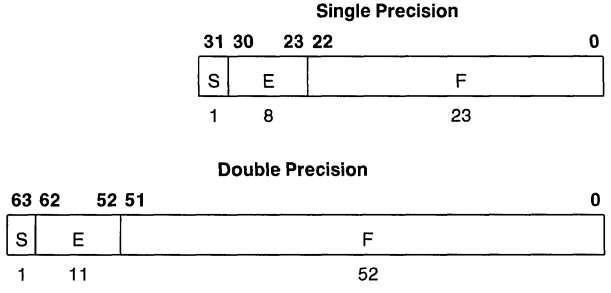

FIGURE 1-1. Floating-Point Operand Formats

1.0 Product Introduction (Continued)

TABLE 1-3. Normalized Number Ranges

	Single Precision	Double Precision
Most Positive	$2^{127}\times(2-2^{-23})$ $=3.40282346\times10^{38}$	$2^{1023}\times(2-2^{-52})$ $=1.7976931348623157\times10^{308}$
Least Positive	2^{-126} $=1.17549436\times10^{-38}$	2^{-1022} $=2.2250738585072014\times10^{-308}$
Least Negative	$-(2^{-126})$ $=-1.17549436\times10^{-38}$	$-(2^{-1022})$ $=-2.2250738585072014\times10^{-308}$
Most Negative	$-2^{127}\times(2-2^{-23})$ $=-3.40282346\times10^{38}$	$-2^{1023}\times(2-2^{-52})$ $=-1.7976931348623157\times10^{308}$

Note: The values given are extended one full digit beyond their represented accuracy to help in generating rounding and conversion algorithms.

1.1.4 Integers

In addition to performing floating-point arithmetic, the NS32081 FPU performs conversions between integer and floating-point data types. Integers are accepted or generated by the FPU as two's complement values of byte (8 bits), word (16 bits) or double word (32 bits) length.

1.1.5 Memory Representations

The NS32081 FPU does not directly access memory. However, it is cooperatively involved in the execution of a set of two-address instructions with its Series 32000 Family CPU. The CPU determines the representation of operands in memory.

In the Series 32000 family of CPUs, operands are stored in memory with the least significant byte at the lowest byte address. The only exception to this rule is the Immediate addressing mode, where the operand is held (within the instruction format) with the most significant byte at the lowest address.

2.0 Architectural Description

2.1 PROGRAMMING MODEL

The Series 32000 architecture includes nine registers that are implemented on the NS32081 Floating-Point Unit (FPU).

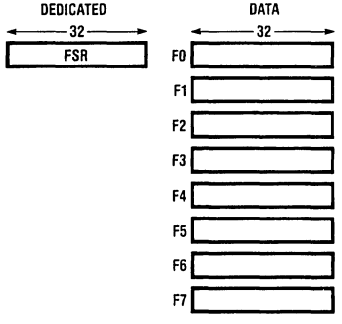

FIGURE 2-1. Register Set

2.1.1 Floating-Point Registers

There are eight registers (F0–F7) on the NS32081 FPU for providing high-speed access to floating-point operands. Each is 32 bits long. A floating-point register is referenced whenever a floating-point instruction uses the Register addressing mode (Section 2.2.2) for a floating-point operand. All other Register mode usages (i.e., integer operands) refer to the General Purpose Registers (R0–R7) of the CPU, and the FPU transfers the operand as if it were in memory. When the Register addressing mode is specified for a double precision (64-bit) operand, a pair of registers holds the operand. The programmer must specify the even register of the pair. The even register contains the least significant half of the operand and the next consecutive register contains the most significant half.

2.1.2 Floating-Point Status Register (FSR)

The Floating-Point Status Register (FSR) selects operating modes and records any exceptional conditions encountered during execution of a floating-point operation. *Figure 2-2* shows the format of the FSR.

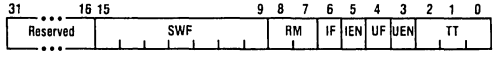

FIGURE 2-2. The Floating-Point Status Register

2.1.2.1 FSR Mode Control Fields

The FSR mode control fields select FPU operation modes. The meanings of the FSR mode control bits are given below.

Rounding Mode (RM): Bits 7 and 8. This field selects the rounding method. Floating-point results are rounded whenever they cannot be exactly represented. The rounding modes are:

00 Round to nearest value. The value which is nearest to the exact result is returned. If the result is exactly halfway between the two nearest values the even value (LSB=0) is returned.

01 Round toward zero. The nearest value which is closer to zero or equal to the exact result is returned.

2.0 Architectural Description (Continued)

10 Round toward positive infinity. The nearest value which is greater than or equal to the exact result is returned.

11 Round toward negative infinity. The nearest value which is less than or equal to the exact result is returned.

Underflow Trap Enable (UEN): Bit 3. If this bit is set, the FPU requests a trap whenever a result is too small in absolute value to be represented as a normalized number. If it is not set, any underflow condition returns a result of exactly zero.

Inexact Result Trap Enable (IEN): Bit 5. If this bit is set, the FPU requests a trap whenever the result of an operation cannot be represented exactly in the operand format of the destination. If it is not set, the result is rounded according to the selected rounding mode.

2.1.2.2 FSR Status Fields

The FSR Status Fields record exceptional conditions encountered during floating-point data processing. The meanings of the FSR status bits are given below:

Trap Type (TT): bits 0-2. This 3-bit field records any exceptional condition detected by a floating-point instruction. The TT field is loaded with zero whenever any floating-point instruction except LFSR or SFSR completes without encountering an exceptional condition. It is also set to zero by a hardware reset or by writing zero into it with the Load FSR (LFSR) instruction. Underflow and Inexact Result are always reported in the TT field, regardless of the settings of the UEN and IEN bits.

000 No exceptional condition occurred.

001 Underflow. A non-zero floating-point result is too small in magnitude to be represented as a normalized floating-point number in the format of the destination operand. This condition is always reported in the TT field and UF bit, but causes a trap only if the UEN bit is set. If the UEN bit is not set, a result of Positive Zero is produced, and no trap occurs.

010 Overflow. A result (either floating-point or integer) of a floating-point instruction is too great in magnitude to be held in the format of the destination operand. Note that rounding, as well as calculations, can cause this condition.

011 Divide by zero. An attempt has been made to divide a non-zero floating-point number by zero. Dividing zero by zero is considered an Invalid Operation instead (below).

100 Illegal Instruction. Two undefined floating-point instruction forms are detected by the FPU as being illegal. The binary formats causing this trap are:

xxxxxxxxxx0011xx10111110

xxxxxxxxxx1001xx10111110

101 Invalid Operation. One of the floating-point operands of a floating-point instruction is a Reserved operand, or an attempt has been made to divide zero by zero using the DIVf instruction.

110 Inexact Result. The result (either floating-point or integer) of a floating-point instruction cannot be represented exactly in the format of the destination operand, and a rounding step must alter it to fit. This condition is always reported in the TT field and IF bit unless any other exceptional condition has occurred in the same instruction. In this case, the TT field always contains the code for the other exception and the IF bit is not altered. A trap is caused by this condition only if the IEN bit is set; otherwise the result is rounded and delivered, and no trap occurs.

111 (Reserved for future use.)

Underflow Flag (UF): Bit 4. This bit is set by the FPU whenever a result is too small in absolute value to be represented as a normalized number. Its function is not affected by the state of the UEN bit. The UF bit is cleared only by writing a zero into it with the Load FSR instruction or by a hardware reset.

Inexact Result Flag (IF): Bit 6. This bit is set by the FPU whenever the result of an operation must be rounded to fit within the destination format. The IF bit is set only if no other error has occurred. It is cleared only by writing a zero into it with the Load FSR instruction or by a hardware reset.

2.1.2.3 FSR Software Field (SWF)

Bits 9-15 of the FSR hold and display any information written to them (using the LFSR and SFSR instructions), but are not otherwise used by FPU hardware. They are reserved for use with NSC floating-point extension software.

2.2 INSTRUCTION SET

2.2.1 General Instruction Format

Figure 2-3 shows the general format of an Series 32000 instruction. The Basic Instruction is one to three bytes long

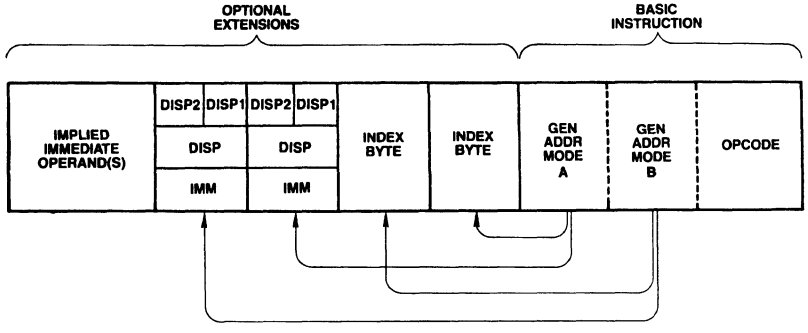

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FIGURE 2-3. General Instruction Format

2.0 Architectural Description (Continued)

and contains the opcode and up to two 5-bit General Addressing Mode (Gen) fields. Following the Basic Instruction field is a set of optional extensions, which may appear depending on the instruction and the addressing modes selected.

The only form of extension issued to the NS32081 FPU is an Immediate operand. Other extensions are used only by the CPU to reference memory operands needed by the FPU.

Index Bytes appear when either or both Gen fields specify Scaled Index. In this case, the Gen field specifies only the Scale Factor (1, 2, 4 or 8), and the Index Byte specifies which General Purpose Register to use as the index, and which addressing mode calculation to perform before indexing. See *Figure 2-4*.

Following Index Bytes come any displacements (addressing constants) or immediate values associated with the selected addressing modes. Each Disp/Imm field may contain one or two displacements, or one immediate value. The size of a Displacement field is encoded within the top bits of that field, as shown in *Figure 2-5*, with the remaining bits interpreted as a signed (two's complement) value. The size of an immediate value is determined from the Opcode field. Both Displacement and Immediate fields are stored most significant byte first.

Some non-FPU instructions require additional, "implied" immediates and/or displacements, apart from those associated with addressing modes. Any such extensions appear at the end of the instruction, in the order that they appear within the list of operands in the instruction definition.

2.2.2 Addressing Modes

The Series 32000 Family CPUs generally access an operand by calculating its Effective Address based on information available when the operand is to be accessed. The method to be used in performing this calculation is specified by the programmer as an "addressing mode."

Addressing modes in the Series 32000 family are designed to optimally support high-level language accesses to variables. In nearly all cases, a variable access requires only one addressing mode within the instruction which acts upon that variable. Extraneous data movement is therefore minimized.

Series 32000 Addressing Modes fall into nine basic types:

Register: In floating-point instructions, these addressing modes refer to a Floating-Point Register (F0–F7) if the operand is of a floating-point type. Otherwise, a CPU General Purpose Register (R0–R7) is referenced. See Section 2.1.1.

Register Relative: A CPU General Purpose Register contains an address to which is added a displacement value from the instruction, yielding the Effective Address of the operand in memory.

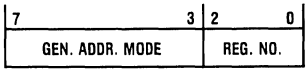

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FIGURE 2-4. Index Byte Format

Memory Space: Identical to Register Relative above, except that the register used is one of the dedicated CPU registers PC, SP, SB or FP. These registers point to data areas generally needed by high-level languages.

Memory Relative: A pointer variable is found within the memory space pointed to by the CPU SP, SB or FP register. A displacement is added to that pointer to generate the Effective Address of the operand.

Immediate: The operand is encoded within the instruction. This addressing mode is not allowed if the operand is to be written. Floating-point operands as well as integer operands may be specified using Immediate mode.

Absolute: The address of the operand is specified by a Displacement field in the instruction.

External: A pointer value is read from a specified entry of the current Link Table. To this pointer value is added a displacement, yielding the Effective Address of the operand.

Top of Stack: The currently-selected CPU Stack Pointer (SP0 or SP1) specifies the location of the operand. The operand is pushed or popped, depending on whether it is written or read.

Scaled Index: Although encoded as an addressing mode, Scaled Indexing is an option on any addressing mode except Immediate or another Scaled Index. It has the effect of calculating an Effective Address, then multiplying any General Purpose Register by 1, 2, 4 or 8 and adding it into the total, yielding the final Effective Address of the operand.

The following table, Table 2-1, is a brief summary of the addressing modes. For a complete description of their actions, see the Series 32000 Instruction Set Reference Manual.

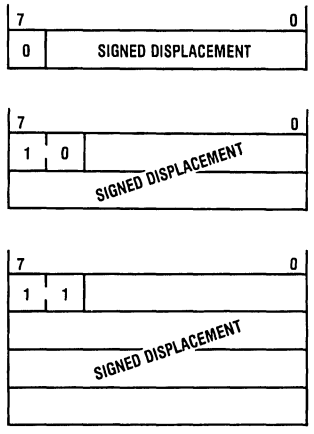

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FIGURE 2-5. Displacement Encodings

2.0 Architectural Description (Continued)

TABLE 2-1. Series 32000 Family Addressing Modes

Encoding	Mode	Assembler Syntax	Effective Address
REGISTER			
00000	Register 0	R0 or F0	None: Operand is in the specified register.
00001	Register 1	R1 or F1	
00010	Register 2	R2 or F2	
00011	Register 3	R3 or F3	
00100	Register 4	R4 or F4	
00101	Register 5	R5 or F5	
00110	Register 6	R6 or F6	
00111	Register 7	R7 or F7	
REGISTER RELATIVE			
01000	Register 0 relative	disp(R0)	Disp + Register.
01001	Register 1 relative	disp(R1)	
01010	Register 2 relative	disp(R2)	
01011	Register 3 relative	disp(R3)	
01100	Register 4 relative	disp(R4)	
01101	Register 5 relative	disp(R5)	
01110	Register 6 relative	disp(R6)	
01111	Register 7 relative	disp(R7)	
MEMORY SPACE			
11000	Frame memory	disp(FP)	Disp + Register; "SP" is either SP0 or SP1, as selected in PSR.
11001	Stack memory	disp(SP)	
11010	Static memory	disp(SB)	
11011	Program memory	*+disp	
MEMORY RELATIVE			
10000	Frame memory relative	disp2(disp1(FP))	Disp2+Pointer; Pointer found at address Disp1+Register. "SP" is either SP0 or SP1, as selected in PSR.
10001	Stack memory relative	disp2(disp1(SP))	
10010	Static memory relative	disp2(disp1(SB))	
IMMEDIATE			
10100	Immediate	value	None: Operand is issued from CPU instruction queue.
ABSOLUTE			
10101	Absolute	@disp	Disp.
EXTERNAL			
10110	External	EXT (disp1)+disp2	Disp2+Pointer; Pointer is found at Link Table Entry number Disp1.
TOP OF STACK			
10111	Top of Stack	TOS	Top of current stack, using either User or Interrupt Stack Pointer, as selected in PSR. Automatic Push/Pop included.
SCALED INDEX			
11100	Index, bytes	mode[Rn:B]	Mode + Rn.
11101	Index, words	mode[Rn:W]	Mode + 2 × Rn.
11110	Index, double words	mode[Rn:D]	Mode + 4 × Rn.
11111	Index, quad words	mode[Rn:Q]	Mode + 8 × Rn. "Mode" and "n" are contained within the Index Byte.
10011	(Reserved for Future Use)		

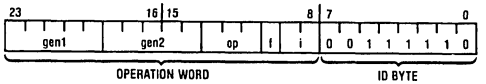
2.0 Architectural Description (Continued)

2.2.3 Floating-Point Instruction Set

The NS32081 FPU instructions occupy formats 9 and 11 of the Series 32000 Family instruction set (*Figure 2-6*). A list of all Series 32000 family instruction formats is found in the applicable CPU data sheet.

Certain notations in the following instruction description tables serve to relate the assembly language form of each instruction to its binary format in *Figure 2-6*.

Format 9



TL/EE/5234–11

Format 11

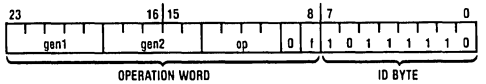


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FIGURE 2-6. Floating-Point Instruction Formats

The Format column indicates which of the two formats in *Figure 2-6* represents each instruction.

The Op column indicates the binary pattern for the field called "op" in the applicable format.

The Instruction column gives the form of each instruction as it appears in assembly language. The form consists of an instruction mnemonic in upper case, with one or more suffixes (i or f) indicating data types, followed by a list of operands (gen1, gen2).

An i suffix on an instruction mnemonic indicates a choice of integer data types. This choice affects the binary pattern in the i field of the corresponding instruction format (*Figure 2-6*) as follows:

Suffix i	Data Type	i Field
B	Byte	00
W	Word	01
D	Double Word	11

An f suffix on an instruction mnemonic indicates a choice of floating-point data types. This choice affects the setting of the f bit of the corresponding instruction format (*Figure 2-6*) as follows:

Suffix f	Data Type	f Bit
F	Single Precision	1
L	Double Precision (Long)	0

An operand designation (gen1, gen2) indicates a choice of addressing mode expressions. This choice affects the binary pattern in the corresponding gen1 or gen2 field of the instruction format (*Figure 2-6*). Refer to Table 2-1 for the options available and their patterns.

Further details of the exact operations performed by each instruction are found in the Series 32000 Instruction Set Reference Manual.

Movement and Conversion

The following instructions move the gen1 operand to the gen2 operand, leaving the gen1 operand intact.

Format	Op	Instruction		Description
11	0001	MOVf	gen1, gen2	Move without conversion
9	010	MOVLF	gen1, gen2	Move, converting from double precision to single precision.
9	011	MOVFL	gen1, gen2	Move, converting from single precision to double precision.
9	000	MOVif	gen1, gen2	Move, converting from any integer type to any floating-point type.
9	100	ROUNDfi	gen1, gen2	Move, converting from floating-point to the nearest integer.
9	101	TRUNCfi	gen1, gen2	Move, converting from floating-point to the nearest integer closer to zero.
9	111	FLOORfi	gen1, gen2	Move, converting from floating-point to the largest integer less than or equal to its value.

Note: The MOVLF instruction f bit must be 1 and the i field must be 10. The MOVFL instruction f bit must be 0 and the i field must be 11.

Arithmetic Operations

The following instructions perform floating-point arithmetic operations on the gen1 and gen2 operands, leaving the result in the gen2 operand.

Format	Op	Instruction		Description
11	0000	ADDf	gen1, gen2	Add gen1 to gen2.
11	0100	SUBf	gen1, gen2	Subtract gen1 from gen2.
11	1100	MULf	gen1, gen2	Multiply gen2 by gen1.
11	1000	DIVf	gen1, gen2	Divide gen2 by gen1.
11	0101	NEGf	gen1, gen2	Move negative of gen1 to gen2.
11	1101	ABSf	gen1, gen2	Move absolute value of gen1 to gen2.

2.0 Architectural Description (Continued)

Comparison

The Compare instruction compares two floating-point values, sending the result to the CPU PSR Z and N bits for use as condition codes. See *Figure 3-7*. The Z bit is set if the gen1 and gen2 operands are equal; it is cleared otherwise. The N bit is set if the gen1 operand is greater than the gen2 operand; it is cleared otherwise. The CPU PSR L bit is unconditionally cleared. Positive and negative zero are considered equal.

Format	Op	Instruction		Description
11	0010	CMPf	gen1, gen2	Compare gen1 to gen2.

Floating-Point Status Register Access

The following instructions load and store the FSR as a 32-bit integer.

Format	Op	Instruction		Description
9	001	LFSR	gen1	Load FSR
9	110	SFSR	gen2	Store FSR

2.3 TRAPS

Upon detecting an exceptional condition in executing a floating-point instruction, the NS32081 FPU requests a trap by setting the Q bit of the status word transferred during the slave protocol (Section 3.5). The CPU responds by performing a trap using a default vector value of 3. See the Series 32000 Instruction Set Reference Manual and the applicable CPU data sheet for trap service details.

A trapped floating-point instruction returns no result, and does not affect the CPU Processor Status Register (PSR). The FPU displays the reason for the trap in the Trap Type (TT) field of the FSR (Section 2.1.2.2).

3.0 Functional Description

3.1 POWER AND GROUNDING

The NS32081 requires a single 5V power supply, applied on pin 24 (V_{CC}). See DC Electrical Characteristics table.

Grounding connections are made on two pins. Logic Ground (GNDL, pin 12) is the common pin for on-chip logic, and Buffer Ground (GNDB, pin 13) is the common pin for the output drivers. For optimal noise immunity, it is recommended that GNDL be attached through a single conductor directly to GNDB, and that all other grounding connections be made only to GNDB, as shown below (*Figure 3-1*).

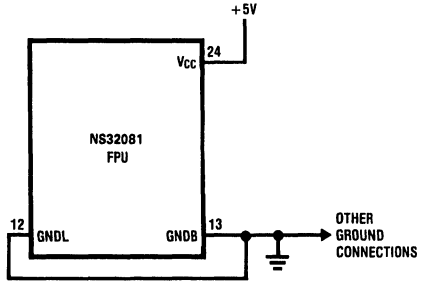

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FIGURE 3-1. Recommended Supply Connections

3.2 CLOCKING

The NS32081 FPU requires a single-phase TTL clock input on its CLK pin (pin 14). When the FPU is connected to a Series 32000 CPU, the CLK signal is provided from the CTTL pin of the NS32201 Timing Control Unit.

3.3 RESETTING

The $\overline{RST}$ pin serves as a reset for on-chip logic. The FPU may be reset at any time by pulling the $\overline{RST}$ pin low for at least 64 clock cycles. Upon detecting a reset, the FPU terminates instruction processing, resets its internal logic, and clears the FSR to all zeroes.

On application of power, $\overline{RST}$ must be held low for at least 50 μs after V_{CC} is stable. This ensures that all on-chip voltages are completely stable before operation. See *Figures 3-2* and *3-3*.

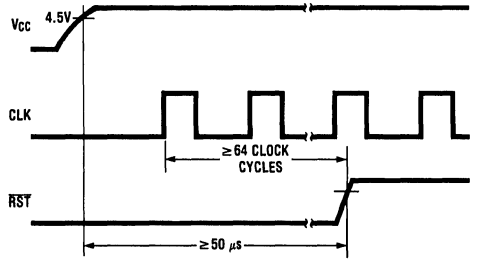

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FIGURE 3-2. Power-On Reset Requirements

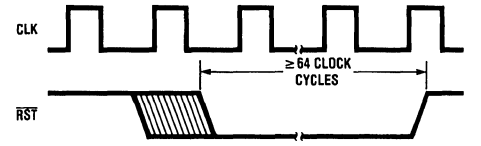

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FIGURE 3-3. General Reset Timing

3.4 BUS OPERATION

Instructions and operands are passed to the NS32081 FPU with slave processor bus cycles. Each bus cycle transfers either one byte (8 bits) or one word (16 bits) to or from the FPU. During all bus cycles, the $\overline{SPC}$ line is driven by the CPU as an active low data strobe, and the FPU monitors

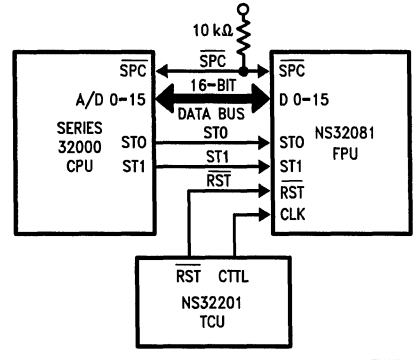

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FIGURE 3-4. System Connection Diagram

3.0 Functional Description (Continued)

pins ST0 and ST1 to keep track of the sequence (protocol) established for the instruction being executed. This is necessary in a virtual memory environment, allowing the FPU to retry an aborted instruction.

3.4.1 Bus Cycles

A bus cycle is initiated by the CPU, which asserts the proper status on ST0 and ST1 and pulses $\overline{SPC}$ low. ST0 and ST1 are sampled by the FPU on the leading (falling) edge of the $\overline{SPC}$ pulse. If the transfer is from the FPU (a slave processor read cycle), the FPU asserts data on the data bus for the duration of the $\overline{SPC}$ pulse. If the transfer is to the FPU (a slave processor write cycle), the FPU latches data from the data bus on the trailing (rising) edge of the $\overline{SPC}$ pulse. *Figures 3-5* and *3-6* illustrate these sequences.

The direction of the transfer and the role of the bidirectional $\overline{SPC}$ line are determined by the instruction protocol being performed. $\overline{SPC}$ is always driven by the CPU during slave processor bus cycles. Protocol sequences for each instruction are given in Section 3.5.

3.4.2 Operand Transfer Sequences

An operand is transferred in one or more bus cycles. A 1-byte operand is transferred on the least significant byte of the data bus (D0–D7). A 2-byte operand is transferred on the entire bus. A 4-byte or 8-byte operand is transferred in consecutive bus cycles, least significant word first.

3.5 INSTRUCTION PROTOCOLS

3.5.1 General Protocol Sequence

Slave Processor instructions have a three-byte Basic Instruction field, consisting of an ID byte followed by an Operation Word. See Section 2.2.3 for FPU instruction encodings. The ID Byte has three functions:

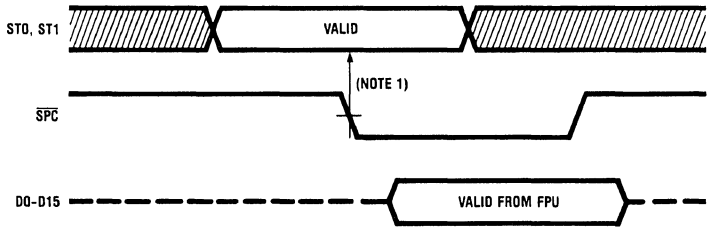
1) It identifies the instruction to the CPU as being a Slave Processor instruction.

2) It specifies which Slave Processor will execute it.

3) It determines the format of the following Operation Word of the instruction.

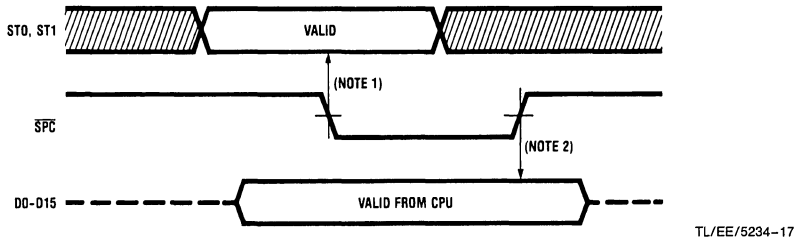
Upon receiving a Slave Processor instruction, the CPU initiates the sequence outlined in Table 3-2. While applying Status Code 11 (Broadcast ID. Table 3-1), the CPU transfers the ID Byte on the least significant half of the Data Bus (D0–D7). All Slave Processors input this byte and decode it. The Slave Processor selected by the ID Byte is activated, and from this point the CPU is communicating only with it. If any other slave protocol was in progress (e.g., an aborted Slave instruction), this transfer cancels it.

The CPU next sends the Operation Word while applying Status Code 01 (Transfer Slave Operand, Table 3-1). Upon receiving it, the FPU decodes it, and at this point both the CPU and the FPU are aware of the number of operands to be transferred and their sizes. The Operation Word is swapped on the Data Bus; that is, bits 0–7 appear on pins D8–D15, and bits 8–15 appear on pins D0–D7.



Note 1: FPU samples CPU status here.

FIGURE 3-5. Slave Processor Read Cycle



Note 1: FPU samples CPU status here.

Note 2: FPU samples data bus here.

FIGURE 3-6. Slave Processor Write Cycle

3.0 Functional Description (Continued)

Using the Addressing Mode fields within the Operation Word, the CPU starts fetching operands and issuing them to the FPU. To do so, it references any Addressing Mode extensions appended to the FPU instruction. Since the CPU is solely responsible for memory accesses, these extensions are not sent to the Slave Processor. The Status Code applied is 01 (Transfer Slave Processor Operand, Table 3-1).

After the CPU has issued the last operand, the FPU starts the actual execution of the instruction. Upon completion, it will signal the CPU by pulsing $\overline{SPC}$ low. To allow for this, the CPU releases the $\overline{SPC}$ signal, causing it to float. $\overline{SPC}$ must be held high by an external pull-up resistor.

Upon receiving the pulse on $\overline{SPC}$, the CPU uses $\overline{SPC}$ to read a Status Word from the FPU, applying Status Code 10. This word has the format shown in *Figure 3-7*. If the Q bit ("Quit", Bit 0) is set, this indicates that an error has been detected by the FPU. The CPU will not continue the protocol, but will immediately trap through the Slave vector in the Interrupt Table. If the instruction being performed is CMPf (Section 2.2.3) and the Q bit is not set, the CPU loads Processor Status Register (PSR) bits N, Z and L from the corresponding bits in the Status Word. The NS32081 FPU always sets the L bit to zero.

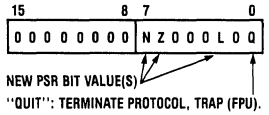


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FIGURE 3-7. FPU Protocol Status Word Format

The last step in the protocol is for the CPU to read a result, if any, and transfer it to the destination. The Read cycles from the FPU are performed by the CPU while applying Status Code 01 (Section 4.1.2).

TABLE 3-1. General Instruction Protocol

Step	Status	Action
1	11	CPU sends ID Byte.
2	01	CPU sends Operation Word.
3	01	CPU sends required operands.
4	XX	FPU starts execution.
5	XX	FPU pulses $\overline{SPC}$ low.
6	10	CPU reads Status Word.
7	01	CPU reads result (if any).

3.5.2 Floating-Point Protocols

Table 3-2 gives the protocols followed for each floating-point instruction. The instructions are referenced by their mnemonics. For the bit encodings of each instruction, see Section 2.2.3.

The Operand Class columns give the Access Classes for each general operand, defining how the addressing modes are interpreted by the CPU (see Series 32000 Instruction Set Reference Manual).

The Operand Issued columns show the sizes of the operands issued to the Floating-Point Unit by the CPU. "D" indicates a 32-bit Double Word. "i" indicates that the instruction specifies an integer size for the operand (B = Byte, W = Word, D = Double Word). "f" indicates that the instruction specifies a floating-point size for the operand (F = 32-bit Standard Floating, L = 64-bit Long Floating).

The Returned Value Type and Destination column gives the size of any returned value and where the CPU places it. The PSR Bits Affected column indicates which PSR bits, if any, are updated from the Slave Processor Status Word (*Figure 3-7*).

Any operand indicated as being of type "f" will not cause a transfer if the Register addressing mode is specified, because the Floating-Point Registers are physically on the Floating-Point Unit and are therefore available without CPU assistance.

TABLE 3-2. Floating Point Instruction Protocols

Mnemonic	Operand 1 Class	Operand 2 Class	Operand 1 Issued	Operand 2 Issued	Returned Value Type and Dest.	PSR Bits Affected
ADDf	read.f	rmw.f	f	f	f to Op. 2	none
SUBf	read.f	rmw.f	f	f	f to Op. 2	none
MULf	read.f	rmw.f	f	f	f to Op. 2	none
DIVf	read.f	rmw.f	f	f	f to Op. 2	none
MOVf	read.f	write.f	f	N/A	f to Op. 2	none
ABSf	read.f	write.f	f	N/A	f to Op. 2	none
NEGf	read.f	write.f	f	N/A	f to Op. 2	none
CMPf	read.f	read.f	f	f	N/A	N,Z,L
FLOORfi	read.f	write.i	f	N/A	i to Op. 2	none
TRUNCfi	read.f	write.i	f	N/A	i to Op. 2	none
ROUNDfi	read.f	write.i	f	N/A	i to Op. 2	none
MOVFL	read.F	write.L	F	N/A	L to Op. 2	none
MOVLF	read.L	write.F	L	N/A	F to Op. 2	none
MOVif	read.i	write.f	i	N/A	f to Op. 2	none
LFSR	read.D	N/A	D	N/A	N/A	none
SFSR	N/A	write.D	N/A	N/A	D to Op. 2	none

D = Double Word

i = Integer size (B, W, D) specified in mnemonic.

f = Floating-Point type (F, L) specified in mnemonic.

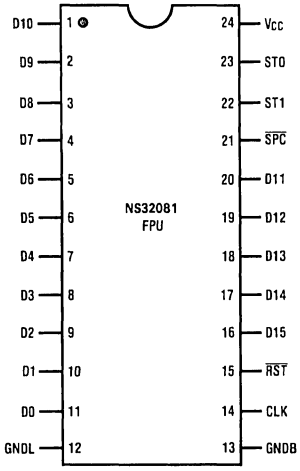
N/A = Not Applicable to this instruction.

4.0 Device Specifications

4.1 PIN DESCRIPTIONS

The following are brief descriptions of all NS32081 FPU pins. The descriptions reference the relevant portions of the Functional Description, Section 3.

Dual-In-Line Package



Top View

FIGURE 4-1. Connection Diagram

Order Number NS32081D-10 or NS32081D-15
See NS Package Number D24C

Order Number NS32081N-10 or NS32081N-15
See NS Package Number N24A

4.1.1 Supplies

Power (V_{CC}): +5V positive supply. Section 3.1.

Logic Ground (GNDL): Ground reference for on-chip logic. Section 3.1.

Buffer Ground (GNDB): Ground reference for on-chip drivers connected to output pins. Section 3.1.

4.1.2 Input Signals

Clock (CLK): TTL-level clock signal.

Reset ($\overline{RST}$): Active low. Initiates a Reset, Section 3.3.

Status (ST0, ST1): Input from CPU. ST0 is the least significant bit. Section 3.4 encodings are:

00—(Reserved)
01—Transferring Operation Word or Operand
10—Reading Status Word
11—Broadcasting Slave ID

4.1.3 Input/Output Signals

Slave Processor Control ($\overline{SPC}$): Active low. Driven by the CPU as the data strobe for bus transfers to and from the NS32081 FPU, Section 3.4. Driven by the FPU to signal completion of an operation, Section 3.5.1. Must be held high with an external pull-up resistor while floating.

Data Bus (D0–D15): 16-bit bus for data transfer. D0 is the least significant bit. Section 3.4.

4.2 ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias	0°C to +70°C
Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to GND	−0.5V to +7.0V
Power Dissipation	1.5W

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Note: *Absolute maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended; operation should be limited to those conditions specified under Electrical Characteristics.*

4.3 ELECTRICAL CHARACTERISTICS T_A = 0°C to 70°C, V_{CC} = 5V ±5%, GND = 0V

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	HIGH Level Input Voltage		2.0		V_{CC} +0.5	V
V_{IL}	LOW Level Input Voltage		−0.5		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −400 μA	2.4			V
V_{OL}	LOW Level Output Voltage	I_{OL} = 4 mA			0.45	V
I_I	Input Load Current	$0 \le V_{IN} \le V_{CC}$	−10.0		10.0	μA
I_L	Leakage Current Output and I/O Pins in TRI-STATE/Input Mode	$0.45 \le V_{IN} \le 2.4V$	−20.0		20.0	μA
I_{CC}	Active Supply Current	I_{OUT} = 0, T_A = 25°C			300	mA

4.0 Device Specifications (Continued)

4.4 SWITCHING CHARACTERISTICS

4.4.1 Definitions

All the Timing Specifications given in this section refer to 0.8V and 2.0V on all the input and output signals as illustrated in *Figures 4.2* and *4.3,* unless specifically stated otherwise.

ABBREVIATIONS

L.E. — Leading Edge
T.E. — Trailing Edge
R.E. — Rising Edge
F.E. — Falling Edge

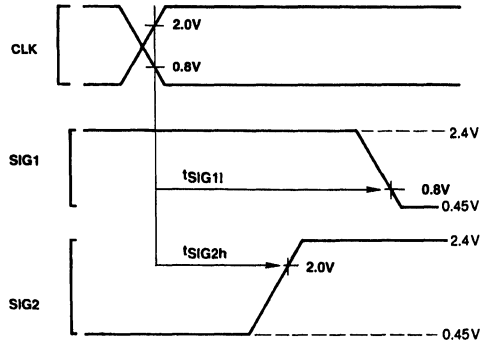


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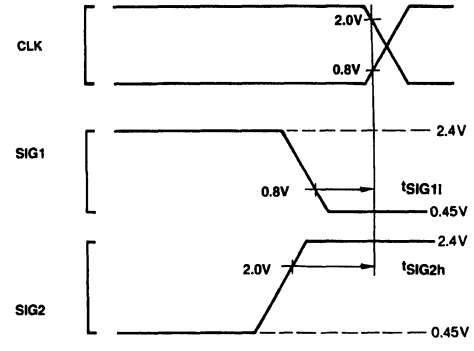
FIGURE 4-2. Timing Specification Standard (Signal Valid After Clock Edge)



TL/EE/5234–27

FIGURE 4-3. Timing Specification Standard (Signal Valid Before Clock Edge)

4.0 Device Specifications (Continued)

4.4.2 Timing Tables

4.4.2.1 Output Signal Propagation Delays

Maximum times assume capacitive loading of 100 pF.

Name	Figure	Description	Reference/ Conditions	NS32081-10		NS32081-15		Units
				Min	Max	Min	Max	
t_{Dv}	4-7	Data Valid	After $\overline{SPC}$ L.E.		45		30	ns
t_{Df}	4-7	D_0–D_{15} Floating	After $\overline{SPC}$ T.E.		50		35	ns
t_{SPCFw}	4-9	$\overline{SPC}$ Pulse Width from FPU	At 0.8V (Both Edges)	$t_{CLKp} - 50$	$t_{CLKp} + 50$	$t_{CLKp} - 40$	$t_{CLKp} + 40$	ns
t_{SPCFl}	4-9	$\overline{SPC}$ Output Active	After CLK R.E.		55		38	ns
t_{SPCFh}	4-9	$\overline{SPC}$ Output Inactive	After CLK R.E.		55		38	ns
t_{SPCFnf}	4-9	$\overline{SPC}$ Output Nonforcing	After CLK F.E.		45		35	ns

4.4.2.2 Input Signal Requirements

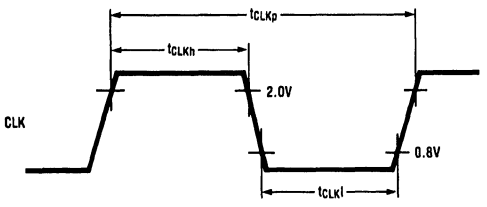
Name	Figure	Description	Reference/ Conditions	Min	Max	Min	Max	Units
t_{PWR}	4-5	Power Stable to $\overline{RST}$ R.E.	After V_{CC} Reaches 4.5V	50		50		μs
t_{RSTw}	4-6	$\overline{RST}$ Pulse Width	At 0.8V (Both Edges)	64		64		t_{CLKp}
t_{Ss}	4-7	Status (ST0–ST1) Setup	Before $\overline{SPC}$ L.E.	50		33		ns
t_{Sh}	4-7	Status (ST0–ST1) Hold	After $\overline{SPC}$ L.E.	40		35		ns
t_{Ds}	4-8	D0–D15 Setup Time	Before $\overline{SPC}$ T.E.	40		30		ns
t_{Dh}	4-8	D0–D15 Hold Time	After $\overline{SPC}$ T.E.	50		35		ns
t_{SPCw}	4-7	SPC Pulse Width from CPU	At 0.8V (Both Edges)	70		50		ns
t_{SPCs}	4-7	$\overline{SPC}$ Input Active	Before CLK R.E.	40		35		ns
t_{SPCh}	4-7	$\overline{SPC}$ Input Inactive	After CLK R.E.	0		0		ns
t_{RSTs}	4-10	$\overline{RST}$ Setup	Before CLK F.E.	10		10		ns
t_{RSTh}	4-10	$\overline{RST}$ R.E. Delay	After CLK R.E.	0		0		ns

4.4.2.3 Clocking Requirements

Name	Figure	Description	Reference/ Conditions	Min	Max	Min	Max	Units
t_{CLKh}	4-4	Clock High Time	At 2.0V (Both Edges)	42	1000	27	1000	ns
t_{CLKl}	4-4	Clock Low Time	At 0.8V (Both Edges)	42	1000	27	1000	ns
t_{CLKp}	4-4	Clock Period	CLK R.E. to Next CLK R.E.	100	2000	66		ns

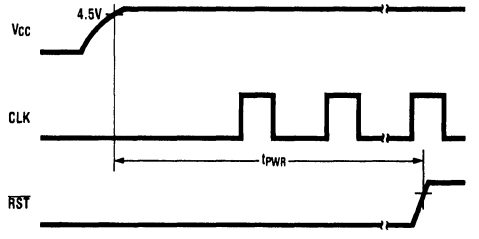
4.0 Device Specifications (Continued)

4.4.3 Timing Diagrams



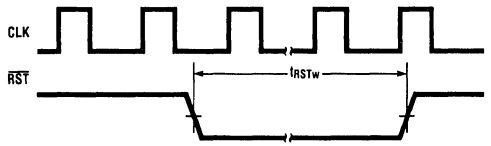
TL/EE/5234-19

FIGURE 4-4. Clock Timing



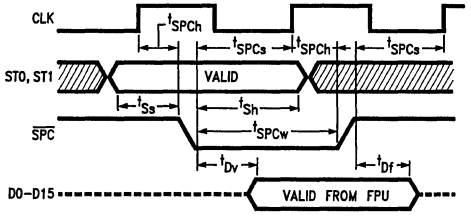
TL/EE/5234-20

FIGURE 4-5. Power-On Reset



TL/EE/5234-21

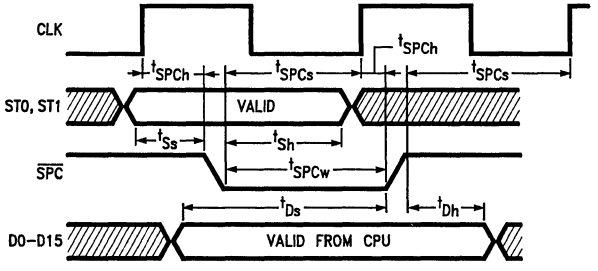
FIGURE 4-6. Non-Power-On Reset



TL/EE/5234-22

FIGURE 4-7. Read Cycle from FPU

Note: $\overline{SPC}$ pulse must be (nominally) 1 clock wide when writing into FPU.

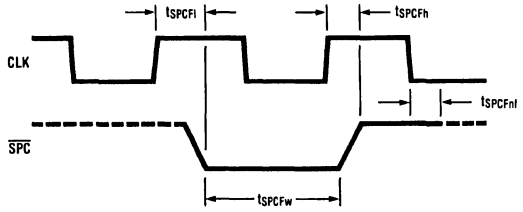


TL/EE/5234-23

FIGURE 4-8. Write Cycle to FPU

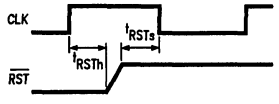
Note: $\overline{SPC}$ pulse may also be 2 clocks wide, but its edges must meet the t_{SPCs} and t_{SPCh} requirements with respect to CLK.

4.0 Device Specifications (Continued)



TL/EE/5234–24

FIGURE 4-9. $\overline{SPC}$ Pulse from FPU



TL/EE/5234–25

FIGURE 4-10. $\overline{RST}$ Release Timing

Note: The rising edge of $\overline{RST}$ must occur while CLK is high, as shown.

National Semiconductor

PRELIMINARY

NS32580-20/NS32580-25/NS32580-30 Floating Point Controller

General Description

The NS32580 Floating-Point Controller (FPC) is an interface controller designed to couple the NS32532 Microprocessor with the Weitek WTL 3164 Floating-Point Data Path (FPDP). It is a new member of the Series 32000® family and it is fully upward compatible with the existing NS32081 floating-point software. The performance of the NS32580 (FPC) and the WTL 3164 (FPDP) with the NS32532 has been significantly enhanced for high-performance floating-point applications. It reaches the peak performance of 15 Mflops when executing single and double precision ADD, SUB, MUL, and MAC instructions in a pipelined mode while maintaining precise exception handling.

The FPC/FPDP supports the IEEE 754—1985 standard for Binary Floating-Point Arithmetic. An improved exception handling scheme allows enabling or disabling of each of the IEEE defined traps. It supports Infinity and Not a Number (NaN) and can flush the result to zero or trap on underflowed instructions.

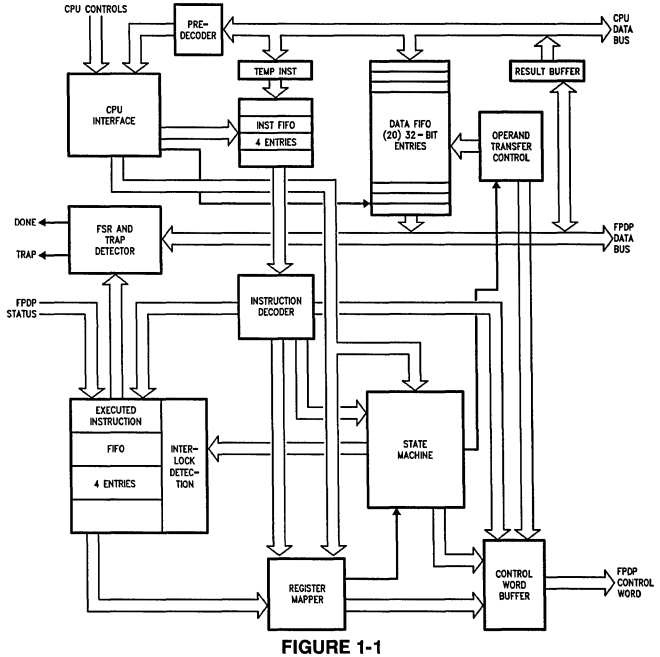
The NS32580 contains three FIFOs and a Floating-Point Status Register (FSR). It executes 18 instructions in conjunction with the WTL 3164 and with the NS32532 forms a tightly coupled computer cluster. The FPC/FPDP appears to the user as a single slave processing unit. All addressing modes, including two address operations, are available with the floating-point instructions. In addition, the CPU and FPC/FPDP communication is handled automatically, and is user transparent.

The FPC is fabricated with National's advanced double-metal CMOS process and can operate at a frequency of 30 MHz.

Features

- Provides the NS32532 CPU with a complete interface controller for high-speed floating-point arithmetic
- 15 Mflops peak performance for single and double precision ADD, SUB, MUL and MAC instructions with the Weitek WTL 3164 FPDP
- Conforms to IEEE 754—1985 standard for Binary Floating-Point Arithmetic
- Pipelined Slave Protocol with Data and Instruction FIFOs
- Improved exception handling including support of Infinities and Not a Number (NaN)
- Single (32-bit) and double (64-bit) precision operations
- Upward compatible with existing NS32081 software base
- 20 MHz, 25 MHz and 30 MHz operating frequencies
- 1 μm double-metal CMOS technology
- 172-pin PGA package

Block Diagram



TL/EE/9421–1

FIGURE 1-1

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1.0 Product Introduction

The NS32580 Floating-Point Controller (FPC) provides complete control for high speed floating-point operations between the NS32532 CPU and the Weitek WTL 3164 Floating-Point Data Path (FPDP). The FPC is fabricated using National high-speed CMOS technology and operates as a slave processor for transparent expansion of the Series 32000 CPU's basic instruction set. The NS32580 is compatible with the IEEE Floating-Point Formats by means of its hardware and software features.

1.1 IEEE FEATURES SUPPORTED

a. Basic floating-point number formats
b. Add, subtract, multiply, divide, sqrt, and compare operations
c. Conversions between different floating-point formats
d. Conversions between floating-point and integer formats
e. Round floating-point number to integer (round to nearest, round toward negative infinity and round toward zero, in double- or single-precision)
f. Exception signaling and handling (invalid operation, divide by zero, overflow, underflow and inexact)
g. Positive and negative infinity (Section 1.2.3)

Note: In addition to supporting the IEEE floating-point overflow, the NS32580 supports integer conversion overflow.

Also, the FPC-FPDP can accept Not-a-Number (NaN) as an operand and generate NaN as a result, but it does not conform to the IEEE 754-1985 Standard since it does not differentiate between signaling and quiet Not-a-Number.

The remaining IEEE features are supported in the software library. These items include:

a. Extended floating-point number formats
b. Mixed floating-point data formats
c. Conversions between basic formats, floating-point numbers and decimal strings
d. Remainder
e. Denormalized numbers

1.2 OPERAND FORMATS

The NS32580 FPC operates on two floating-point data types—single precision (32 bits) and double precision (64 bits). Floating-point instruction mnemonics use the suffix F (Floating) to select the single precision data type, and the suffix L (Long Floating) to select the double precision data type.

A floating-point number is divided into three fields, as shown in *Figure 1-2*.

The F field is the fractional portion of the represented number. In Normalized numbers (Section 1.2.1), the binary point is assumed to be immediately to the left of the most significant bit of the F field, with an implied 1 bit to the left of the binary point. Thus, the F field represents values in the range $1.0 \leq x \leq 2.0$, as shown in Table 1-1.

TABLE 1-1. Sample F Fields

F Field	Binary Value	Decimal Value
000 . . . 0	1.000 . . . 0	1.000 . . . 0
010 . . . 0	1.010 . . . 0	1.250 . . . 0
100 . . . 0	1.100 . . . 0	1.500 . . . 0
110 . . . 0	1.110 . . . 0	1.750 . . . 0
	↑	
	Implied Bit	

The E field contains an unsigned number that gives the binary exponent of the represented number. The value in the E field is biased; that is, a constant bias value must be subtracted from the E field value in order to obtain the true exponent. The bias value is $011 \ldots 11_2$, which is either 127 (single precision) or 1023 (double precision). Thus, the true exponent can be either positive or negative, as shown in Table 1-2.

TABLE 1-2. Sample E Fields

E Field	F Field	Represented Value
011 . . . 110	100 . . . 0	$1.5 \times 2^{-1} = 0.75$
011 . . . 111	100 . . . 0	$1.5 \times 2^{0} = 1.50$
100 . . . 000	100 . . . 0	$1.5 \times 2^{1} = 3.00$

Two values of the E field are not exponents. 11 . . . 11 signals Not-a-Number (NaN) or Infinity (Section 1.2.3). 00 . . . 00 represents the number zero (Section 1.2.2), if the F field is also all zeroes, otherwise it signals a reserved operand (Section 1.2.4).

The S bit indicates the sign of the operand. It is 0 for positive and 1 for negative. Floating-point numbers are in sign-magnitude form, that is, only the S bit is complemented in order to change the sign of the represented number.

1.2.1 Normalized Numbers

Normalized numbers are numbers which can be expressed as floating-point operands, as described above, where the E field is neither all zeroes nor all ones.

The value of a Normalized number can be derived by the formula:

$$(-1)^{S} \times 2^{(E\text{-}Bias)} \times (1 + F)$$

The range of Normalized numbers is given in Table 1-3.

1.2.2 Zero

There are two representatives for zero—positive and negative. Positive zero has all-zero F and E fields, and the S bit is zero. Negative zero also has all-zero F and E fields, but its S bit is one.

1.2.3 Reserved Operands

Infinity arithmetic is the limiting case of real arithmetic with operands of arbitrarily large magnitudes. The NS32580 does not treat infinity as a reserved operand and in ROUNDfi, TRUNCfi and FLOORfi instructions, when the operand is infinity, the FPC will return the TRAP "overflow" instead of TRAP "INVALID OPERATION" with the Integer Conversion Overflow Flag, IOF, set to "1".

Another special case regarding infinity occurs when dividing infinity by zero. In this case NO TRAP "DIVIDE BY ZERO" will be signaled and infinity will be returned as the result. See *Figures 1-3* and *1-4*.

The NS32580 FPC treats only Denormalized numbers as reserved operands if the Floating-Point Status Register ROE bit is set (Section 2.1.2). Denormalized numbers have all zeroes in their E fields and non-zero values in their F fields.

The NS32580 FPC causes an Invalid Operation Trap (Section 2.1.2.2) if it receives a reserved operand, unless the operation is simply a move (without conversion).

1.0 Product Introduction (Continued)

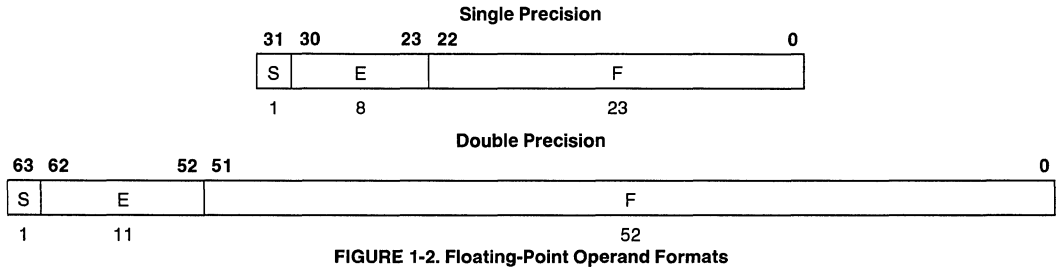

FIGURE 1-2. Floating-Point Operand Formats

TABLE 1-3. Normalized Number Ranges

	Single Precision	Double Precision
Most Positive	$2^{127} \times (2 - 2^{-23})$ $= 3.40282346 \times 10^{38}$	$2^{1023} \times (2 - 2^{-52})$ $= 1.7976931348623157 \times 10^{308}$
Least Positive	2^{-126} $= 1.17549436 \times 10^{-38}$	2^{-1022} $= 2.2250738585072014 \times 10^{-308}$
Least Negative	$-(2^{-126})$ $= -1.17549436 \times 10^{-38}$	$-(2^{-1022})$ $= -2.2250738585072014 \times 10^{-308}$
Most Negative	$-2^{127} \times (2 - 2^{-23})$ $= -3.40282346 \times 10^{38}$	$-2^{1023} \times (2 - 2^{-52})$ $= -1.7976931348623157 \times 10^{308}$

Note: The values given are extended one full digit beyond their represented accuracy to help in generating rounding and conversion algorithms.

E	F	Value	Name	Comments
255	Not 0	None	NaN	ROE = 0 → Reserved Operand ROE = 1 → NaN Returned as Result
255	0	$(-1)^s$ * Infinity	Infinity	Not a Reserved Operand
1–254	Any	$(-1)^s * 2^{e-127} * (1.f)$	Normalized Number	
0	Not 0	$(-1)^s * 2^{-126} * (0.f)$	Denormalized Number	Reserved Operand
0	0	$(-1)^s * 0$	Zero	

FIGURE 1-3. Single-Precision Operand E and F Fields

E	F	Value	Name	Comments
2047	Not 0	None	NaN	ROE = 0 → Reserved Operand ROE = 1 → NaN Returned as Result
2047	0	$(-1)^s$ * Infinity	Infinity	Not a Reserved Operand
1–2046	Any	$(-1)^s * 2^{e-1023} * (1.f)$	Normalized Number	
0	Not 0	$(-1)^s * 2^{-1022} * (0.f)$	Denormalized Number	Reserved Operand
0	0	$(-1)^s * 0$	Zero	

FIGURE 1-4. Double-Precision Operand E and F Fields

1.0 Product Introduction (Continued)

1.2.4 Integer Formats

The FPC-FPDP performs conversions between integer and floating point operands. Integers are accepted and generated by the FPC-FPDP as two's complement values of byte (8 bits), word (16 bits) or double-word (32 bits).

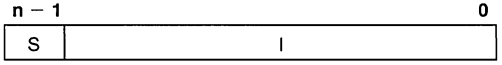

FIGURE 1-5. Integer Format

TABLE 1-4. Integer Fields

S	Value	Name
0	I	Positive Integer
1	$I - 2^n$	Negative Integer

n represents number of bits in the word, 8 for byte, 16 for word and 32 for double-word.

The FPDP supports only 32-bit integers, therefore, the FPC has to sign extend 8- and 16-bit integers prior to integer to floating-point number conversion.

In floating to integer conversion, FPC has to check possible integer overflow, in case of 8- and 16-bit integer formats.

1.2.5 Memory Representations

The NS32580 FPC does not directly access memory. However, it is cooperatively involved in the execution of a set of two-address instructions with the NS32532 CPU. The CPU determines the representation of operands in memory.

In the Series 32000 family of CPUs, operands are stored in memory with the least significant byte at the lowest byte address. The only exception to this rule is the Immediate addressing mode, where the operand is held (within the instruction format) with the most significant byte at the lowest address.

2.0 Architectural Description

2.1 PROGRAMMING MODEL

The Series 32000 architecture includes nine registers; eight data registers and one floating-point status register.

2.1.1 Floating-Point Data Registers (L0–L7)

There are eight registers (L0–L7) in the FPDP for providing high-speed access to floating-point operands. Each is 64 bits long. A floating-point register is referenced whenever a floating-point instruction uses the Register addressing mode (Section 2.2.2) for a floating-point operand. All other Register mode usages (i.e., integer operands) refer to the General Purpose Registers (R0–R7) of the CPU, and the FPU transfers the operand as if it were in memory.

Note: These registers are all upward compatible with the 32-bit NS32081 registers, (F0–F7), such that when the Register addressing mode is specified for a double precision (64-bit) operand, a pair of 32-bit registers holds the operand. The programmer specifies the even register of the pair which contains the least significant half of the operand and the next consecutive register contains the most significant half.

2.1.2 Floating-Point Status Register (FSR)

The Floating-Point Status Register selects operating modes and records any exceptional condition encountered during execution of a floating-point operation. The FPC FSR contains all the NS32081/NS32381 FSR bits and additional fields for better exception handling. The FSR is cleared to all zeros during reset.

DATA

	← 64 →		
	← 32 →	← 32 →	
F1	L0 MSDW	L0 LSDW	F0
	L1 MSDW	L1 LSDW	
F3	L2 MSDW	L2 LSDW	F2
	L3 MSDW	L3 LSDW	
F5	L4 MSDW	L4 LSDW	F4
	L5 MSDW	L5 LSDW	
F7	L6 MSDW	L6 LSDW	F6
	L7 MSDW	L7 LSDW	

LSDW → Least Significant Double Word

MSDW → Most Significant Double Word

FIGURE 2-1. Data Registers

2.1.2.1 FSR Mode Control Fields

The FSR mode control fields select FPC operation modes. The meanings of the FSR mode control bits are given below:

ROUNDING MODE (RM bit 8–7). This field selects the rounding method. Floating-point results are rounded whenever they cannot be represented exactly. The rounding modes are:

00 Round to nearest value. The value which is nearest to the exact result is returned. If the result is exactly halfway between the two nearest values the even value (lsb = 0) is returned.

01 Round toward zero. The nearest value which is closer to zero or equal to the exact result is returned.

10 Round toward positive infinity. The nearest value which is greater than or equal to the result is returned.

11 Round toward negative infinity. The nearest value which is less than or equal to the exact result is returned.

UNDERFLOW TRAP ENABLE (UEN bit 3). If this bit is set, the FPC requests a trap whenever a result is too small in absolute value to be presented as a Normalized number. If it is not set, FPC returns a result of exactly zero.

INEXACT RESULT TRAP ENABLE (IEN bit 5). If this bit is set, the FPC requests a trap whenever the result of an operation cannot be represented exactly in the operand format of the destination (and no other exception occurred in the same operation) or if the result of an operation overflows and the overflow trap is disabled. If IEN is not set, the result is rounded according to the selected rounding mode.

2.1.2.2 FSR Status Fields

The FSR Status Fields record exceptional conditions encountered during floating-point data processing. The meaning of the FSR status bits are given below:

TRAP TYPE (TT bits 2–0). This 3-bit field indicates the reason for TRAP (FPU) requested by the FPC. The TT field is loaded with zero whenever any floating-point instruction except LFSR or SFSR completes without exception. It is also set to zero by a reset or by writing zero into it with the LFSR instruction. The TT field is updated regardless of the setting of the exception enable bits.

2.0 Architectural Description (Continued)

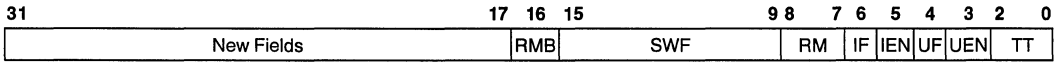

FIGURE 2-2. FSR (Compatible Fields)

000 No exceptional condition occurred.

001 Underflow. This condition occurs whenever a result is too close to zero to be represented as a Normalized number.

010 Overflow. This condition occurs whenever a result is too large in absolute value to be represented (float or integer).

011 Divide by Zero. This condition occurs whenever an attempt was made to divide a non-zero value by zero.

100 Illegal Instruction. An illegal or undefined Floating-Point instruction was passed to the FPC. If the T bit in the Status Word Register (SWR) is a "0", then it indicates that an illegal instruction was passed to the FPC. If the T bit in the SWR is a "1", then it indicates that an undefined instruction was passed to the FPC.

101 Invalid Operation. This condition occurs if:
1. NaN is used as a floating-point operand by any instruction except MOVf and the Reserved Operand Enable (ROE) bit in the FSR is disabled.
2. DNRM is used as a floating-point operand by any instruction except MOVf.
3. Both operands of the DIVf instruction are zero.
4. Sqrt when the floating-point number is negative.
5. Infinity plus negative infinity, infinity minus infinity.

110 Inexact Result. This condition occurs whenever the result of an operation cannot be exactly represented in the precision of the destination (and no other exception occurred in the same operation) or if the result of an operation overflows (floating-point or integer conversion overflow) and the overflow trap is disabled.

111 Reserved.

UNDERFLOW FLAG (UF bit 4). This bit is set by the FPC whenever a result is too small in absolute value to be represented as a Normalized number. Its function is not affected by the state of the UEN bit. The UF bit is "sticky" therefore it can be cleared only by writing a zero into it with the Load FSR instruction or by a hardware reset.

INEXACT RESULT FLAG (IF bit 6). This bit is set by the FPC whenever the result of an operation must be rounded to fit within the destination format (and no other exception occurred in the same operation) or if the result of an operation overflows and the overflow trap is disabled. This situation applies both to floating-point and integer destinations. The IF bit is "sticky" therefore it is cleared only by writing a zero into it with the Load FSR instruction or by a hardware reset.

REGISTER MODIFY BIT (RMB BIT 16). This bit is set by the FPC whenever writing to a floating-point data register. The RMB bit is cleared only by writing a zero with the LFSR instruction or by a hardware reset. This bit can be used in context switching to determine whether the FPC registers should be saved.

2.1.2.3 FSR Software Field (SWF)

Bits 15–9 of the FSR hold and display any information written to them using the LFSR and SFSR instructions, but are not otherwise used by FPC hardware. They are reserved for use with NSC floating-point extension software.

2.1.2.4 FSR New Fields

New fields were added to the FSR for better exception handling. In the FPC, the user can enable or disable each exception or combination of exceptions by using new "enable bits" implemented in the FSR. After reset the new fields are loaded to the default values (compatible with NS32081). Illegal Instruction always causes TRAP and can't be disabled.

CONTROL BITS

RESERVED OPERANDS ENABLE (ROE bit 17). If this bit is cleared, the FPC requests an Invalid Operation trap whenever a NaN has been detected by the FPC. Infinities are not reserved operands in the FPC. When ROE is disabled, the FPC does not generate reserved operands as results. Denormalized Numbers (DNRM) are always treated as reserved operands, except for the case of the SQRTf instruction. When calculating the square root of the negative denormalized number, the TRAP "INVALID OPERATION" will occur and the Reserved Operand Flag ROF will be "0" while Invalid Operation Flag IOF will be "1". If Invalid Operation exception is disabled, the ROE bit is overwritten internally (the FPC does not change the ROE bit in the FSR) and the FPC can generate NaN as a result. ROE bit does not affect MOVf instruction.

INVALID OPERATION ENABLE (IVE bit 18). If this bit is cleared, the FPC requests a trap whenever the operation is invalid. If this bit is set to "1", the trap is disabled and if invalid operation occurred, NaN will be delivered as result.

DIVIDE BY ZERO ENABLE (DZE bit 19). If this bit is cleared the FPC requests a trap whenever an attempt is made to divide by zero. If this bit is set the trap is disabled and if divide by zero occurred, infinity will be delivered as result.

OVERFLOW ENABLE (OVE bit 20). If this bit is cleared, the FPC requests a trap whenever a floating-point result is too big in absolute value to be represented. If this bit is set, the overflow trap is disabled and if overflow occurred, Infinity or Maximum Number will be delivered as result.

INTEGER CONVERSION OVERFLOW ENABLE (IOE bit 21). If this bit is cleared, the FPC requests a trap whenever an Integer result is too big to be represented. If this bit is set, the integer conversion overflow is disabled and if integer conversion overflow occurred, Max/Min integer will be delivered as result.

STATUS BITS

RESERVED OPERAND FLAG (ROF bit 22). This bit is set by the FPC whenever reserved operand DNRM or NaN (when ROE is cleared) is selected by the FPC. The ROF bit is "sticky" and can be cleared only by writing a zero with the Load FSR instruction or by a hardware reset.

INVALID FLAG (IVF bit 23). This bit is set by the FPC whenever the operation is invalid. The IVF bit is "sticky" and can be cleared only by writing a zero with the Load FSR instruction or by a hardware reset.

DIVIDE BY ZERO FLAG (DZF bit 24). This bit is set by the FPC whenever an attempt is made to divide a non-zero value by zero. The DZF bit is "sticky" and can be cleared only by writing a zero with the Load FSR instruction or by a hardware reset.

2.0 Architectural Description (Continued)

31 27	26	25	24	23	22	21	20	19	18	17	16
Reserved	IOF	OVF	DZF	IVF	ROF	IOE	OVE	DZE	IVE	ROE	RMB

FIGURE 2-3. New FSR Mode Control Fields

OVERFLOW FLAG (OVF bit 25). This bit is set by the FPC whenever a floating-point result is too large in absolute value to be represented. The OVF bit is "sticky" and can be cleared only by writing a zero with the Load FSR instruction or by a hardware reset.

INTEGER CONVERSION OVERFLOW FLAG (IOF bit 26). This bit is set by the FPC whenever an integer result is too large in absolute value to be represented. The IOF bit is "sticky" and can be cleared only by writing a zero with the Load FSR instruction or by a hardware reset.

RESERVED FIELD

Bits 31–27 in the FSR are reserved by NSC for future use. User should not use this field.

2.1.2.5 FSR Default Values

During Reset the FSR is loaded to a default value (see Table 2-1). The default values for the FSR represent upward compatibility of the FPC-FPDP with the NS32081. The user can change the default values by loading the FSR register with new values.

TABLE 2-1. FSR Default State Summary

Bit Name	Default Value	Default State
TT (bits 2–0)	0	No exceptional condition occurred.
UEN (bit 3)	0	Underflow trap disabled.
UF (bit 4)	0	Underflow flag is cleared.
IEN (bit 5)	0	Inexact result trap disabled.
IF (bit 6)	0	Inexact flag is cleared.
RM (bits 8–7)	0	Round to nearest.
SWF (bits 15–9)	0	Undefined
RMB (bit 16)	0	RMB flag is cleared.
ROE(bit 17)	0	FPC requests a trap whenever an attempt is made to use reserved operand except for MOVf instruction.
IVE (bit 18)	0	FPC requests a trap whenever the operation is invalid.
DZE (bit 19)	0	FPC requests a trap whenever an attempt is made to divide by zero.
OVE (bit 20)	0	FPC requests a trap whenever a floating-point result is too big to be represented.
IOE (bit 21)	0	FPC requests a trap whenever an integer conversion result is too big to be represented.
ROF (bit 22)	0	ROF flag is cleared.
IVF (bit 23)	0	IVF flag is cleared.
DZF (bit 24)	0	DZF flag is cleared.
OVF (bit 25)	0	OVF flag is cleared.
IOF (bit 26)	0	IOF flag is cleared.
RESERVED (bits 31–27)	0	Reserved field is cleared.

2.2 INSTRUCTION SET

2.2.1 General Instruction Format

Figure 2-4 shows the general format of a Series 32000 instruction. The Basic Instruction is one to three bytes long and contains the opcode and up to two 5-bit General Addressing Mode (Gen) fields. Following the Basic Instruction field is a set of optional extensions, which may appear depending on the instruction and the addressing modes selected.

The only form of extension issued to the NS32580 FPC is an Immediate operand. Other extensions are used only by the CPU to reference memory operands needed by the FPC.

Index Bytes appear when either or both Gen fields specify Scaled Index. In this case, the Gen field specifies only the Scale Factor (1, 2, 4 or 8), and the Index Byte specifies which General Purpose Register to use as the index, and which addressing mode calculation to perform before indexing. See *Figure 2-5*.

Following Index Bytes come any displacements (addressing constants) or immediate values associated with the selected addressing modes. Each Disp/Imm field may contain one or two displacements, or one immediate value. The size of a Displacement field is encoded within the top bits of that field, as shown in *Figure 2-6*, with the remaining bits interpreted as a signed (two's complement) value. The size of an immediate value is determined from the Opcode field. Both Displacement and Immediate fields are stored most significant byte first.

Some non-FPC instructions require additional, "implied" immediates and/or displacements, apart from those associated with addressing modes. Any such extensions appear at the end of the instruction, in the order that they appear within the list of operands in the instruction definition.

2.2.2 Addressing Modes

The Series 32000 Family CPUs generally access an operand by calculating its Effective Address based on information available when the operand is to be accessed. The method to be used in performing this calculation is specified by the programmer as an "addressing mode."

Addressing modes in the Series 32000 family are designed to optimally support high-level language accesses to variables. In nearly all cases, a variable access requires only

2.0 Architectural Description (Continued)

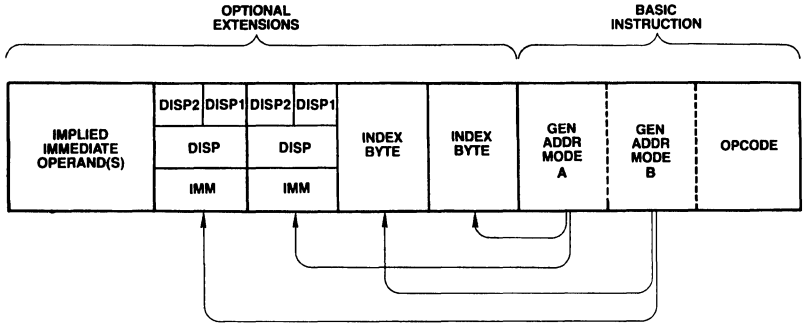

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FIGURE 2-4. General Instruction Format

one addressing mode within the instruction which acts upon that variable. Extraneous data movement is therefore minimized.

Series 32000 Addressing Modes fall into nine basic types:

Register: In floating-point instructions, these addressing modes refer to a Floating-Point Register (F0–F7) or (L0–L7) if the operand is of a floating-point type. Otherwise, a CPU General Purpose Register (R0–R7) is referenced. See Section 2.1.1.

Register Relative: A CPU General Purpose Register contains an address to which is added a displacement value from the instruction, yielding the Effective Address of the operand in memory.

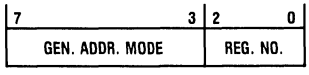

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FIGURE 2-5. Index Byte Format

Memory Space: Identical to Register Relative above, except that the register used is one of the dedicated CPU registers PC, SP, SB or FP. These registers point to data areas generally needed by high-level languages.

Memory Relative: A pointer variable is found within the memory space pointed to by the CPU SP, SB or FP register. A displacement is added to that pointer to generate the Effective Address of the operand.

Immediate: The operand is encoded within the instruction. This addressing mode is not allowed if the operand is to be written. Floating-point operands as well as integer operands may be specified using Immediate mode.

Absolute: The address of the operand is specified by a Displacement field in the instruction.

External: A pointer value is read from a specified entry of the current Link Table. To this pointer value is added a displacement, yielding the Effective Address of the operand.

Top of Stack: The currently-selected CPU Stack Pointer (SP0 or SP1) specifies the location of the operand. The operand is pushed or popped, depending on whether it is written or read.

Scaled Index: Although encoded as an addressing mode, Scaled Indexing is an option on any addressing mode except Immediate or another Scaled Index. It has the effect of calculating an Effective Address, then multiplying any General Purpose Register by 1, 2, 4 or 8 and adding it into the total, yielding the final Effective Address of the operand.

The following table, Table 2-2, is a brief summary of the addressing modes. For a complete description of their actions, see the Series 32000 Instruction Set Reference Manual.

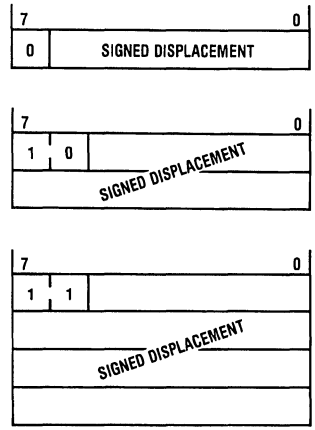

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FIGURE 2-6. Displacement Encodings

2.0 Architectural Description (Continued)

TABLE 2-2. Series 32000 Family Addressing Modes

Encoding	Mode	Assembler Syntax	Effective Address
REGISTER			
00000	Register 0	R0, F0 or L0	None: Operand is in the specified register.
00001	Register 1	R1, F1 or L1	
00010	Register 2	R2, F2 or L2	
00011	Register 3	R3, F3 or L3	
00100	Register 4	R4, F4 or L4	
00101	Register 5	R5, F5 or L5	
00110	Register 6	R6, F6 or L6	
00111	Register 7	R7, F7 or L7	
REGISTER RELATIVE			
01000	Register 0 relative	disp(R0)	Disp + Register.
01001	Register 1 relative	disp(R1)	
01010	Register 2 relative	disp(R2)	
01011	Register 3 relative	disp(R3)	
01100	Register 4 relative	disp(R4)	
01101	Register 5 relative	disp(R5)	
01110	Register 6 relative	disp(R6)	
01111	Register 7 relative	disp(R7)	
MEMORY SPACE			
11000	Frame memory	disp(FP)	Disp + Register; "SP" is either SP0 or SP1, as selected in PSR.
11001	Stack memory	disp(SP)	
11010	Static memory	disp(SB)	
11011	Program memory	* + disp	
MEMORY RELATIVE			
10000	Frame memory relative	disp2(disp1(FP))	Disp2 + Pointer; Pointer found at address Disp1 + Register. "SP" is either SP0 or SP1, as selected in PSR.
10001	Stack memory relative	disp2(disp1(SP))	
10010	Static memory relative	disp2(disp1(SB))	
IMMEDIATE			
10100	Immediate	value	None: Operand is issued from CPU instruction queue.
ABSOLUTE			
10101	Absolute	@disp	Disp.
EXTERNAL			
10110	External	EXT (disp1) + disp2	Disp2 + Pointer; Pointer is found at Link Table Entry number Disp1.
TOP OF STACK			
10111	Top of Stack	TOS	Top of current stack, using either User or Interrupt Stack Pointer, as selected in PSR. Automatic Push/Pop included.
SCALED INDEX			
11100	Index, bytes	mode[Rn:B]	Mode + Rn.
11101	Index, words	mode[Rn:W]	Mode + 2 × Rn.
11110	Index, double words	mode[Rn:D]	Mode + 4 × Rn.
11111	Index, quad words	mode[Rn:Q]	Mode + 8 × Rn. "Mode" and "n" are contained within the Index Byte.
10011	(Reserved for Future Use)		

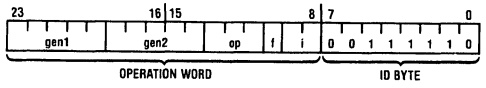
2.0 Architectural Description (Continued)

2.2.3 Floating-Point Instruction Set

The NS32580 FPC-FPDP instructions occupy formats 9, 11 and 12 of the Series 32000 Family instruction set *(Figure 2-7)*. A list of all Series 32000 family instruction formats is found in the applicable CPU data sheet.

Certain notations in the following instruction description tables serve to relate the assembly language form of each instruction to its binary format in *Figure 2-7*.

Format 9



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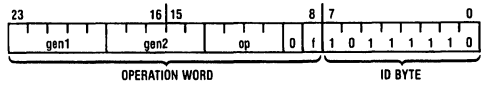
Format 11



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Format 12

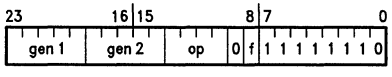

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FIGURE 2-7. Floating-Point Instruction Formats

The Format column indicates which of the three formats in *Figure 2-7* represents each instruction.

The Op column indicates the binary pattern for the field called "op" in the applicable format.

The Instruction column gives the form of each instruction as it appears in assembly language. The form consists of an instruction mnemonic in upper case, with one or more suffixes (i or f) indicating data types, followed by a list of operands (gen1, gen2).

An i suffix on an instruction mnemonic indicates a choice of integer data types. This choice affects the binary pattern in the i field of the corresponding instruction format *(Figure 2-7)* as follows:

Suffix i	Data Type	i Field
B	Byte	00
W	Word	01
D	Double Word	11

An f suffix on an instruction mnemonic indicates a choice of floating-point data types. This choice affects the setting of the f bit of the corresponding instruction format *(Figure 2-7)* as follows:

Suffix f	Data Type	f Bit
F	Single Precision	1
L	Double Precision (Long)	0

An operand designation (gen1, gen2) indicates a choice of addressing mode expressions. This choice affects the binary pattern in the corresponding gen1 or gen2 field of the instruction format *(Figure 2-7)*. Refer to Table 2-2 for the options available and their patterns.

Further details of the exact operations performed by each instruction are found in the Series 32000 Instruction Set Reference Manual.

Movement and Conversion

The following instructions move the gen1 operand to the gen2 operand, leaving the gen1 operand intact.

Format	Op	Instruction		Description
11	0001	MOVf	gen1, gen2	Move without conversion.
9	010	MOVLF	gen1, gen2	Move, converting from double precision to single precision.
9	011	MOVFL	gen1, gen2	Move, converting from single precision to double precision.
9	000	MOVif	gen1, gen2	Move, converting from any integer type to any floating-point type.
9	100	ROUNDfi	gen1, gen2	Move, converting from floating-point to the nearest integer.
9	101	TRUNCfi	gen1, gen2	Move, converting from floating-point to the nearest integer closer to zero.
9	111	FLOORfi	gen1, gen2	Move, converting from floating-point to the largest integer less than or equal to its value.

Note: The MOVLF instruction f bit must be 1 and the i field must be 10. The MOVFL instruction f bit must be 0 and the i field must be 11.

Arithmetic Operations

The following instructions perform floating-point arithmetic operations on the gen1 and gen2 operands, leaving the result in the gen2 operand.

Format	Op	Instruction		Description
11	0000	ADDf	gen1, gen2	Add gen1 to gen2.
11	0100	SUBf	gen1, gen2	Subtract gen1 from gen2.
11	1100	MULf	gen1, gen2	Multiply gen2 by gen1.
11	1000	DIVf	gen1, gen2	Divide gen2 by gen1.
11	0101	NEGf	gen1, gen2	Move negative of gen1 to gen2.
11	1101	ABSf	gen1, gen2	Move absolute value of gen1 to gen2.

2.0 Architectural Description (Continued)

	Format	Op	Instruction		Description
(N)	12	1010	MACf	gen1, gen2	Move (gen1*gen2) + L1 or F1 to L1 or F1 with two rounding errors.
(N)	12	0001	SQRTf	gen1, gen2	Move the square root of gen1 to gen2.

(N): Indicates NEW instruction.

Comparison

The compare instruction compares two floating-point operands, sending the result to the CPU PSR Z, N and L bits for use as condition codes.

Format	Opcode	Instruction		Description
11	0010	CMPf	gen1, gen2	Compare gen1 to gen2.

There are four possible results to the CMPf instruction (with normal operands):

Operands are equal	Z bit is set	N, L bits are cleared
Operand1 is less than Operand2		N, L, Z bits are cleared
Operand2 is less than Operand1	N bit is set	L, Z bits are cleared
Unordered (when at least one operand is NaN and ROE is set)	L bit is set	N, Z bits are cleared

Floating-Point Status Register Access

The following instructions load and store the FSR as a 32-bit integer. If the user specifies a register (gen1 in LFSR or gen2 in SFSR) it will be a general purpose register in the CPU.

Format	Opcode	Instruction		Description
9	001	LFSR	gen1	Load FSR with the content of gen1. (gen2 field = 0)
9	110	SFSR	gen2	Store FSR in gen2. (gen1 field = 0)

Note: All instructions support all of the NS32000 family data formats (for external operands) and all addressing modes are supported.

2.3 EXCEPTIONS/TRAPS

An exception for the FPC is a special floating-point condition with a default handling scheme. Seven types of exceptions are supported:

1) Underflows
2) Overflows
3) Divisions by zero
4) Illegal Instructions
5) Invalid Operations
6) Inexact results
7) Undefined Instructions

The FPC has improved exception handling. Except for Illegal and Undefined Instructions, the user can control all of the exception types. In addition, there are some specific exceptions that the user can control:

Overflows —Floating-Point overflow
Integer conversion overflow

Invalid Operations —Reserved Operands

Each exception or type that is controlled by the user can be set-up to cause an interrupt or to return a result without an interrupt on the occurrence of the exception. The interrupt is called a TRAP and is signaled by the FPC pulsing the $\overline{\text{FSSR}}$ line for one clock cycle. Illegal and Undefined instructions are not under control of the user and will always cause a TRAP if they are passed to the FPC.

Enabling an exception will cause a TRAP whenever the exception occurs and disabling an exception will return a result without a TRAP.

When the FPC TRAPS it sets the Q bit in the status word register. The CPU responds by reading the status word register while applying status (11110) on the status lines. If the CPU sent the FPC ID with an undefined opcode, the T bit in the status word register would also be set by the FPC indicating a TRAP (UND). If the T bit is clear after the TRAP it indicates a TRAP(FPU) and the reason for the TRAP resides in the FSR TRAP TYPE field. A trapped instruction returns no result (also if the destination is an FPDP register) and does not affect the CPU PSR.

In addition there is a flag bit, for each exception under user control, which will mark the occurrence of the exceptional condition whether or not the exception is enabled or disabled. These bits in the FSR can be used for polling the exception status while TRAPS are disabled.

Floating-point instructions that end with an enabled exception will trap, activating the $\overline{\text{FSSR}}$ signal, but will not update the destination register. In this case, the FPC will ABORT the instruction that ended with the exception to prevent destruction of the data in the destination register. Instructions that ended with a disabled exception update the destination register with the default result.

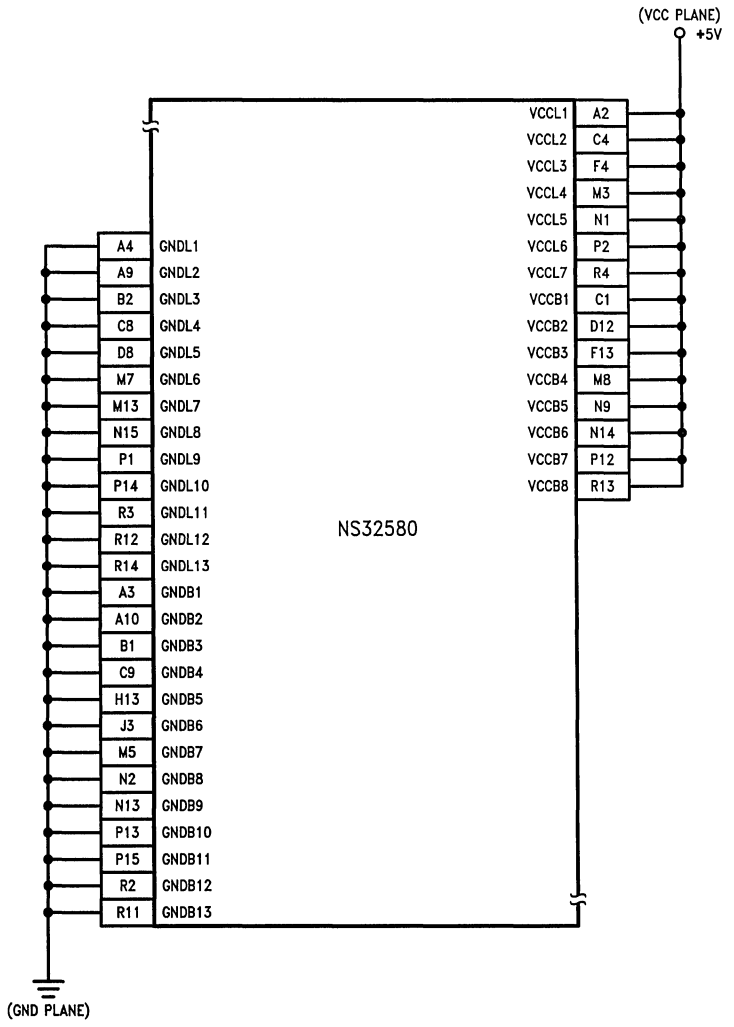
2.0 Architectural Description (Continued)

TABLE 2-3. Exception Enabled/Disabled Summary

Exception Occurred	Enabled By	Q = 1; Trap Type	Disabled By	Q = 0; Default Result Returned	Flag Bits
Underflow	UEN = 1	001	UEN = 0	Zero	UF = 1
Floating-Point Overflow	OVE = 0	010	OVE = 1 IEN = 0	Infinity or Max NRM Number	OVF = 1
	OVE = 1 IEN = 1	110			OVF = 1 IF = 1
Integer Conversion Ov.	IOE = 0	010	IOE = 1 IEN = 0	Max or Min Integer	IOF = 1
	IOE = 1 IEN = 1	110			IOF = 1 IF = 1
Divide by Zero	DZE = 0	011	DZE = 1	Infinity	DZF = 1
Illegal Instruction	Always Enabled	T bit = 0 and 100	Cannot be Disabled	No Result	No Flags Affected
Invalid Operation	IVE = 0	101	IVE = 1	NaN	IVF = 1
Reserved Op. (NaN)	ROE = 0 IVE = 0	101	ROE = 0 IVE = 1	NaN	ROF = 1 IVF = 1
Reserved Op. (NaN)		000	ROE = 1 IVE = X	NaN	No Flags
Reserved Op. (DNRM)	ROE = X IVE = 0	101	ROE = X IVE = 1	Undefined	ROF = 1 IVF = 1
Inexact Result	IEN = 1	110	IEN = 0	Correctly Rounded Result	IF = 1
Undefined Instruction	Always Enabled	T bit = 1 and 100	Cannot be Disabled	No Result	No Flags Affected
				Status Word Register	
CMPf (NaN)	ROE = 0 IVE = 0	101	ROE = 0 IVE = 1	L = 1, N = Z = 0	ROF = 1 IVF = 1
CMPf (NaN)		000	ROE = 1 IVE = X	L = 1, N = Z = 0	No Flags Affected
CMPf (DNRM)	ROE = X IVE = 0	101	ROE = X IVE = 1	N, L, Z Undefined	ROF = 1 IVF = 1

X = Don't Care

3.0 Functional Description



TL/EE/9421–8

FIGURE 3-1. Recommended Supply Connections

3.1 POWER AND GROUNDING

The NS32580 requires a single 5V power supply, applied on 15 pins. The logic voltage pins (VCCL1 to VCCL7) supply the power to the on-chip logic. The buffer voltage pins (VCCB1 to VCCB8) supply the power to the output drivers of the chip. All the voltage pins should be connected together by a power (V_{CC}) plane on the printed circuit board.

The NS32580 grounding connections are made on 26 pins. The logic ground pins (GNDL1 to GNDL13) are the ground pins for the on-chip logic. The buffer ground pins (GNDB1–GNDB13) are the ground pins for the output drivers of the chip. All the ground pins should be connected together by a ground plane on the printed circuit board.

Both power and ground connections are shown in *Figure 3-1.*

3.2 CLOCKING

The NS32580 FPC requires a single-phase TTL clock input on its BCLK pin (pin C10) and an inverted TTL clock input on its $\overline{\text{BCLK}}$ pin (pin B8). When the FPC is connected to a NS32532 CPU these signals are provided directly from the CPU's BCLK and $\overline{\text{BCLK}}$ output signals.

3.3 RESETTING

The $\overline{\text{RST}}$ pin serves as a reset for on-chip logic. The FPC may be reset at any time by pulling the $\overline{\text{RST}}$ pin low for at least 64 clock cycles. Upon detecting a reset, the FPC terminates instruction processing, resets its internal logic, clears the FSR to all zeroes, and clears the FIFOs.

On application of power, $\overline{\text{RST}}$ must be held low for at least 50 μs after V_{CC} is stable. This ensures that all on-chip voltages are completely stable before operation. See *Figures 3-2* and *3-3.*

3.0 Functional Description (Continued)

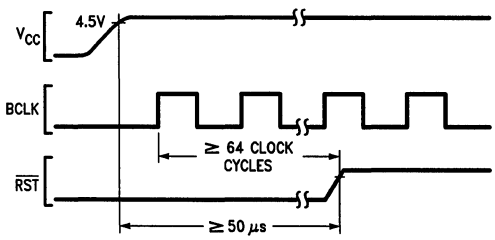


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FIGURE 3-2. Power-On Reset Requirements

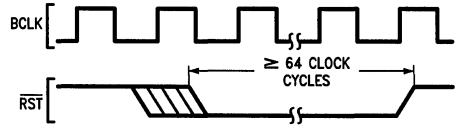

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FIGURE 3-3. General Reset Timing

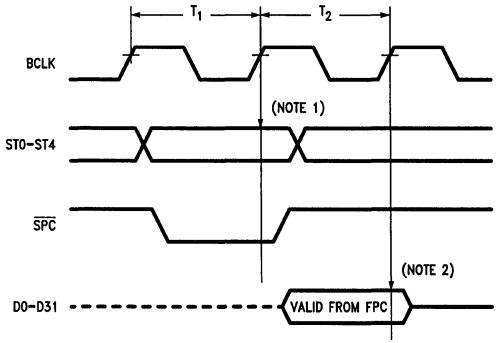
3.4 BUS OPERATION

Instructions and operands are passed to the NS32580 FPC with slave processor bus cycles. Each bus cycle transfers one double-word (32 bits) to or from the FPC. During all bus cycles, the $\overline{SPC}$ line is driven by the CPU as an active low data strobe, and the FPC monitors pins ST0–ST4 to keep track of the sequence (protocol) established for the instruction being executed. This is necessary in a virtual memory environment, allowing the FPC to retry an aborted instruction.

A bus cycle is initiated by the CPU, which asserts the proper status on ST0–ST4 and pulses $\overline{SPC}$ low. The status lines are sampled by the FPC on the rising edge of BCLK in the T2 state. *Figures 3-4* and *3-5* illustrate these sequences.

3.4.1 Operand Transfers

The CPU fetches operands from memory, aligns them (if needed) and sends them to the slave (with status h'1D) as a 32-bit transfer. If the operand is double-precision the Less significant half is transferred first (in 32000 mode). The FPC can not access the memory directly.



Note 1: FPC samples CPU status here.
Note 2: CPU samples FPC data here.

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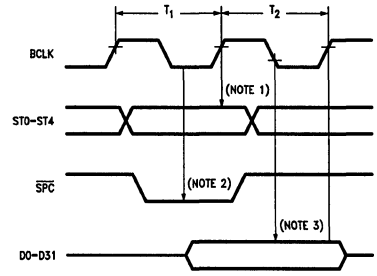
FIGURE 3-4. Slave Processor Read Cycle from FPC



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Note 1: FPC samples CPU status here.
Note 2: FPC samples $\overline{SPC}$ here.
Note 3: FPC samples data here.

FIGURE 3-5. Slave Processor Write Cycle to FPC

From the slave processor point of view there are four possible combinations of locations for operands: (For special cases see next paragraph.)

Register to Register Instructions—Both operands reside in the register file inside the FPDP. No operand fetch or transfer from memory is needed.

Memory to Register—The source operand is in memory, therefore the CPU will transfer the operand (one 32-bit transfer for single-precision and two 32-bit transfers for double-precision). The result is going to the floating-point register in the register file located inside the FPDP.

Register to Memory—The source operand resides inside the FPDP. If the instruction is monadic (one operand) the CPU will not transfer the operand to the FPC before the beginning of the instruction (all the information needed to start the operation resides inside the FPDP). For dyadic instructions, the CPU will fetch and transfer one operand from memory.

Memory to Memory—In monadic instructions the source operand is in memory and the CPU will transfer it to the FPC-FPDP. If the instruction is dyadic, two operands will be transferred from memory to the FPC-FPDP by the CPU (gen1 before gen2). The result in both cases is sent back to memory.

When the CPU transfers an operand from memory to the FPC-FPDP it is loaded into one of the registers that create the operand FIFO inside the FPDP. The FPC translates the incoming instruction (mem, reg or mem, mem) to a register-to-register instruction with the same register number. From the incoming instruction addressing mode it should know if the operands are coming from memory or already located in the register file.

The Data FIFO inside the FPC is 10 entries deep, single- or double-precision. If the destination of instruction is memory, the FPC will wait for completion of the instruction. Then, the result will be transferred to the FPC and $\overline{SDN}$ will be signaled. If the FPC receives a new ID and Opcode before the CPU finishes reading the result, (can happen if page fault has been detected on a write) the FPC will abort the last instruction and will start the execution of the new instruction. The NS32532 CPU can "reset" the FPC by issuing $\overline{SPC}$ and status h'1E when there was no $\overline{FSSR}$ from FPC. In this case FPC flushes the instructions currently being executed and the contents of the floating-point registers are undefined.

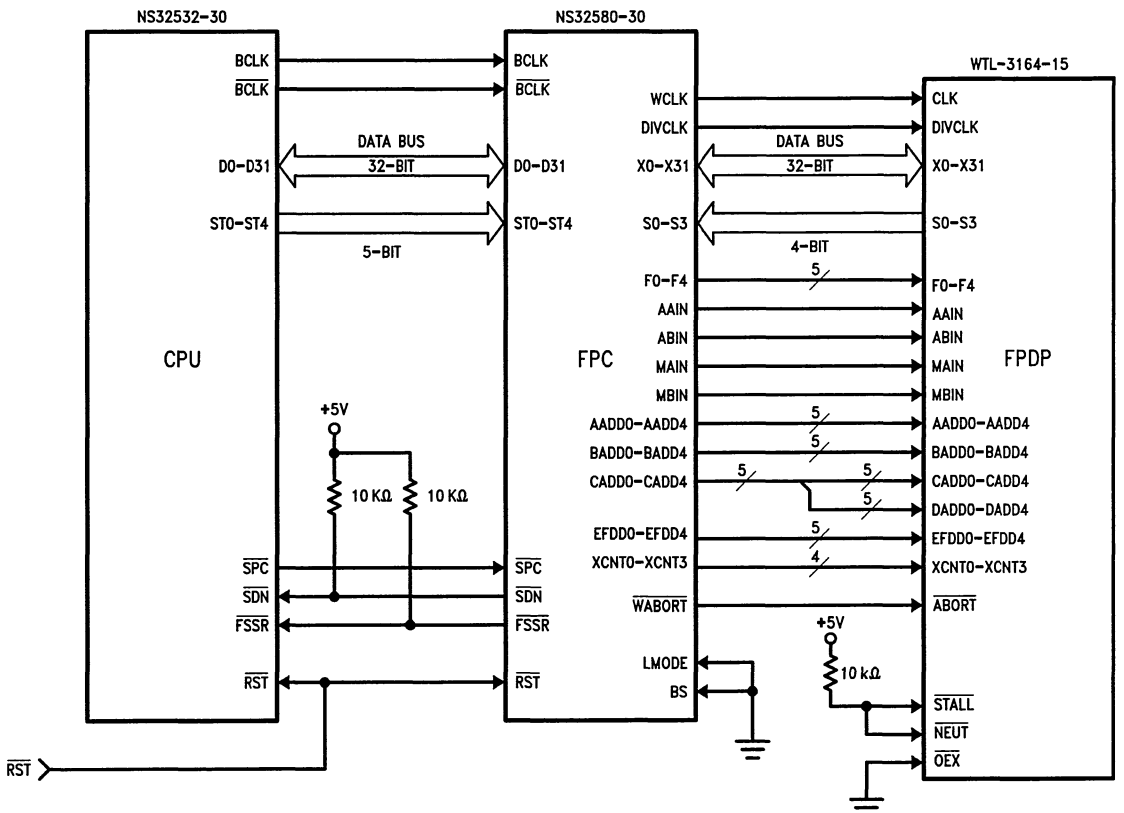

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FIGURE 3-6. System Connection Diagram

3.0 Functional Description (Continued)

3.5 INSTRUCTION PROTOCOLS

3.5.1 General Slave Protocol Sequence

The FPC interfaces with the CPU using the Slave-Protocol. The slave protocol is a well defined protocol for instruction and operand transfers between the CPU and the slave co-processors (FPC and Custom Slave). Only the CPU can initiate slave cycle or access memory to fetch operands. The communication between the CPU and the FPC occurs at the beginning of the floating-point instruction, when the CPU transfers the Opcode and possible operands. At the end of the instruction, the FPC signals successful or unsuccessful conclusion of floating-point instruction and the CPU transfers operands from the FPC, if applicable.

The CPU broadcasts the ID and Opcode to all slave processors, one of which will recognize it and from this point the CPU is communicating only with one slave processor.

The CPU puts the slave ID (different ID for each format) on byte 3 (D31–D24), puts the Opcode low on byte 2 (D23–D16) and puts the Opcode high on byte 1 (D15–D8). Byte 0 (D7–D0) is not used.

31	23	15	7	0
ID	OPCODE low	OPCODE high	XXXXXXXX	
Byte 3	Byte 2	Byte 1	Byte 0	

FIGURE 3-7. ID and Opcode Format

CPU Status Combinations

11101 (h'1D) Transfer Slave Processor Operands—The CPU is transferring an operand to or from a slave processor.

11110 (h'1E) Read Slave Processor Status—The CPU is reading the Status Word Register after the FPC signaled TRAP or is resetting the FPC when there was no $\overline{\text{FSSR}}$.

11111 (h'1F) Broadcast Slave ID—The CPU is initiating the execution of a slave processor instruction.

The floating-point unit has three different instruction formats:

Format 9

23	16	15	8	7							0
Gen 1	Gen 2	Op	f	i	0	0	1	1	1	1	1	0

MOVif —000 MOVLF —010 ROUND —100 SFSR —110
LFSR —001 MOVFL —011 TRUNC —101 FLOOR —111

Format 11

23	16	15	8	7							0
Gen 1	Gen 2	Op	0	f	1	0	1	1	1	1	1	0

ADDf	—0000	SUBf	—0100	DIVf	—1000	MULf	—1100
MOVf	—0001	NEGf	—0101	Trap(FPU)	—1001	ABSf	—1101
CMPf	—0010	Trap(UND)	—0110	Trap(UND)	—1010	Trap(UND)	—1110
Trap(FPU)	—0011	Trap(UND)	—0111	Trap(UND)	—1011	Trap(UND)	—1111

Format 12

23	16	15	8	7							0
Gen 1	Gen 2	Op	0	f	1	1	1	1	1	1	1	0

SREMf*	—0000	SCALBf*	—0100	Trap(UND)	—1000	Trap(UND)	—1100
SQRTf	—0001	LOGBf*	—0101	Trap(UND)	—1001	Trap(UND)	—1101
POLYf*	—0010	Trap(UND)	—0110	MACf	—1010	Trap(UND)	—1110
DOTf*	—0011	Trap(UND)	—0111	Trap(UND)	—1011	Trap(UND)	—1111

*All the marked instructions are not supported by the NS32580 and will cause Trap(UND).

TABLE 3-1. 32-Bit General Slave Instruction Protocol

Step	Status	Action
1	ID (11111)	CPU sends ID and Operation Word
2	OP (11101)	CPU sends required operands (if any)
3	—	Slaves starts execution (CPU prefetches)
4	—	Slave signals DONE, TRAP or CMPf
5	ST (11110)	CPU Reads Status Word (If TRAP was signaled or if a CMPf instruction was executed)
6	OP (11101)	CPU Reads Result (if destination is memory and if no TRAP occurred)

3.0 Functional Description (Continued)

TABLE 3-2. Floating-Point Instruction Protocols

Mnemonic	Operand 1 Class	Operand 2 Class	Operand 1 Issued	Operand 2 Issued	Returned Value	PSR Bits Affected
ADDf	read.f	rmw.f	f	f	f to Op. 2	none
SUBf	read.f	rmw.f	f	f	f to Op. 2	none
MULf	read.f	rmw.f	f	f	f to Op. 2	none
DIVf	read.f	rmw.f	f	f	f to Op. 2	none
MOVf	read.f	write.f	f	N/A	f to Op. 2	none
ABSf	read.f	write.f	f	N/A	f to Op. 2	none
NEGf	read.f	write.f	f	N/A	f to Op. 2	none
CMPf	read.f	read.f	f	f	N/A	N,Z,L
FLOORfi	read.f	write.i	f	N/A	i to Op. 2	none
TRUNCfi	read.f	write.i	f	N/A	i to Op. 2	none
ROUNDfi	read.f	write.i	f	N/A	i to Op. 2	none
MOVFL	read.F	write.L	F	N/A	L to Op. 2	none
MOVLF	read.L	write.F	L	N/A	F to Op. 2	none
MOVif	read.i	write.f	i	N/A	f to Op. 2	none
LFSR	read.D	N/A	D	N/A	N/A	none
SFSR	N/A	write.D	N/A	N/A	D to Op. 2	none
SQRTf	read.f	write.f	f	N/A	f to Op.2	none
MACf	read.f	read.f	f	f	f to L1/F1	none

D = Double Word

i = Integer size (B, W, D) specified in mnemonic.

f = Floating-Point type (F, L) specified in mnemonic.

N/A = Not Applicable to this instruction.

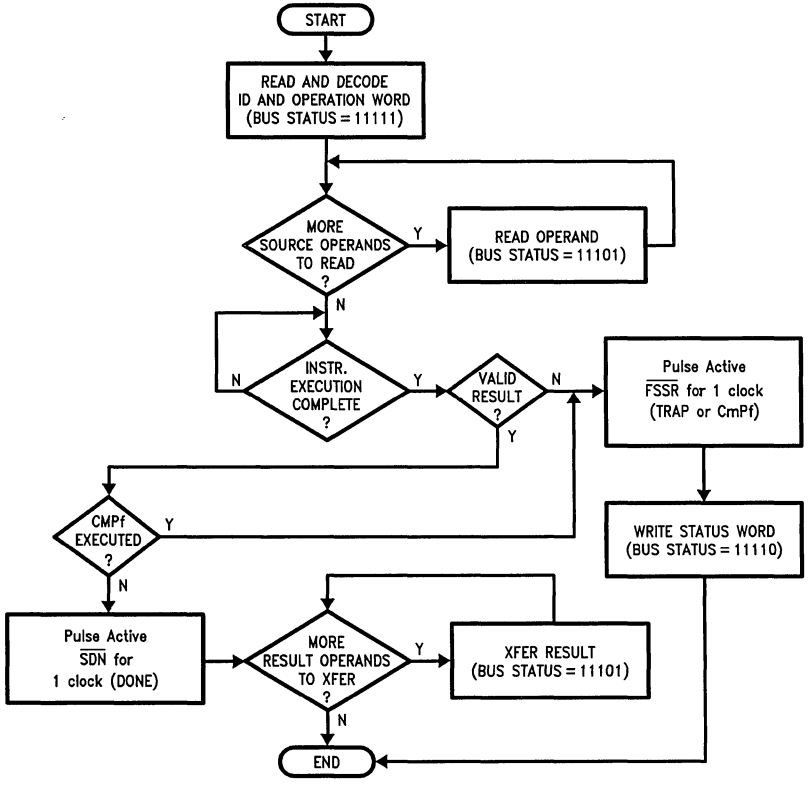

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FIGURE 3-8. 32-Bit General Slave Instruction Protocol

3.0 Functional Description (Continued)

3.5.2 Pipelined Slave Protocol Sequence

The NS32532 can communicate with the FPC using the pipelined Slave Protocol. In the pipelined slave protocol, the CPU proceeds to the next floating-point instruction if the destination of the current floating-point instruction is a register, without waiting for $\overline{SDN}$ signal. The FPC from the other end can receive new instructions before the end of the previous instruction. The FPC can internally store up to five new instructions, with up to 10 single- or double-precision operands. The CPU saves the PC of the floating-point instructions in the Floating-Point Instruction FIFO (FIF).

If exception occurs, the floating-point instruction can be reexecuted using the PC saved in the FIF (if exception occurs the CPU will flush the FIF and the FPC will flush the instruction and the operand's FIFOs).

The FPC-FPDP can start execution of a new floating-point instruction every two CPU clock cycles.

In the following example three floating-point instructions are being pipelined:

```
DIVF    O(RO), F1
ADDF    F2, F3
MULF    F4, F5
```

Step	Status	Action
1	ID (h'1F)	CPU sends ID and Opcode of DIVF instruction.
2	OP (h'1D)	CPU sends operand (R0).
3	—	Slave starts execution of DIVF instruction.
4	ID (h'1F)	CPU sends ID and Opcode of ADDF instruction.
5	—	Slave starts execution of ADDF instruction.
6	ID (h'1F)	CPU sends ID and Opcode of MULF instruction.
7	—	Slave starts execution of MULF instruction.
8	—	Slave pulses $\overline{SDN}$ or $\overline{FSSR}$ for the DIVF instruction. if TRAP occurred, the rest of the instructions will be aborted.
9	ST (h'1E)	CPU Reads Status Word (if TRAP was signaled).
10	—	Slave pulses $\overline{SDN}$ or $\overline{FSSR}$ for the ADDF instruction. If TRAP occurred, the rest of the instructions will be aborted.
11	ST (h'1E)	CPU Reads Status Word (if TRAP was signaled).
12	—	Slave pulses $\overline{SDN}$ or $\overline{FSSR}$ for the MULF instruction.
13	ST (h'1E)	CPU Reads Status Word (if TRAP was signaled).

3.5.3 Status Word Register

There is a Status Word Register (SWR) that holds the compare results and an exception flag, which indicates TRAP. This register can be read by the CPU by applying status code h'1E (read slave status) on the status line and $\overline{SPC}$ as a timing signal. The FPC updates the status word register after a compare float instruction or if TRAP has occurred. The content of SWR is valid only after the FPC signals $\overline{FSSR}$.

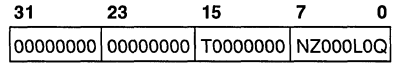

FIGURE 3-9. FPC Status Word Format (SWR)

Status Bits

N BIT: The N bit is set to "1" if the second operand is less than the first operand. Otherwise, it is set to "0".

Z BIT: The Z bit is set to "1" if the second operand is equal to the first operand. Otherwise, it is set to "0".

L BIT: The L bit is set to "1" if the operands in CMPf operation are "Unordered" (i.e., one of them is NaN). If ROE bit is cleared, the L bit is always cleared by the FPC.

Q BIT: The Q bit is set to "1" if TRAP occurred. The T bit will distinguish between TRAP(UND) and TRAP(FPU).

T BIT: The T bit is set to "1" if the TRAP is TRAP(UND) and "0" if the TRAP is TRAP(FPU). The CPU examines this bit whenever TRAP occurs.

3.5.4 Termination of Instruction (Not Including CMPf)

Floating-Point Instructions that ended without exception will signal done by pulsing the $\overline{SDN}$ line for one clock cycle. The CPU will read the result from the FPC if the destination is memory. The CPU can try to read the result immediately after detecting the $\overline{SDN}$ signal. Therefore, the DONE must be signaled after loading the result to the FPC. To read the result the CPU uses the Read from FPC cycle as shown in *Figure 3-4.* Upon detecting an exceptional condition in executing a floating point instruction, the FPC requests a TRAP by pulsing the $\overline{FSSR}$ line for one clock cycle. In addition, it sets the Q bit in the status word register. The CPU responds by reading the status word register while applying status h'1E (transferring status word) on the status lines. A trapped instruction returns no result (also if the destination is FPC register) and does not affect the CPU PSR.

The FPC displays the reason for the TRAP(FPU) in the TRAP TYPE (TT) field of the FSR. If the CPU sends FPC ID with illegal opcode, the FPC generates TRAP(UND) by signaling TRAP and setting the T bit in the status word register. The TT field in the FSR will be set to Illegal Instruction (h'100). POLYf, DOTf, SREMf, SCALBf, LOGBf and all the unused opcodes in formats 11 and 12 will cause a TRAP(UND).

3.5.5 Byte Sex

The FPC supports the VME or 32000 bus, depending on the state of the BS pin. In 32000 mode (BS = "0"), the FPC is ready to receive the less significant half of a double-precision operand first and the more significant half afterward. In VME mode (BS = "1"), the FPC is ready to receive the more significant half of a double-precision operand first and the less significant half afterward. The FPC will send the received operands to the correct destination registers inside the FPDP. In VME mode, the user must swap the data bus between the CPU and FPC. Byte 0 in the CPU should be connected to Byte 3 in the FPC, Byte 1 in the CPU should be connected to Byte 2 in the FPC, byte 2 in the CPU should be connected to Byte 1 in the FPC and Byte 3 in the CPU should be connected to Byte 0 in the FPC. The BS line is sampled by the FPC during Reset only.

3.0 Functional Description (Continued)

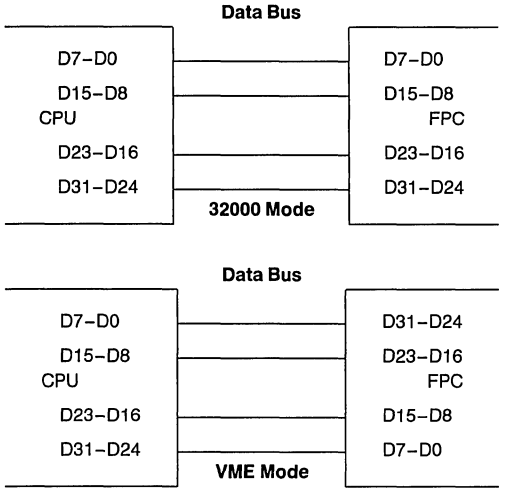

FIGURE 3-10. Byte Sex Connection Diagrams

3.5.6 Floating-Point Protocols

Table 3-2 gives the protocols followed for each floating-point instruction. The instructions are referenced by their mnemonics. For the bit encodings of each instruction, see Section 2.2.3.

The Operand Class columns give the Access Classes for each general operand, defining how the addressing modes are interpreted by the CPU (see Series 32000 Instruction Set Reference Manual).

The Operand Issued columns show the sizes of the operands issued to the Floating-Point Controller by the CPU. "D" indicates a 32-bit Double Word. "i" indicates that the instruction specifies an integer size for the operand (B = Byte, W = Word, D = Double Word). "f" indicates that the instruction specifies a floating-point size for the operand (F = 32-bit Standard Floating, L = 64-bit Long Floating).

The Returned Value Type and Destination column gives the size of any returned value and where the CPU places it. The PSR Bits Affected column indicates which PSR bits, if any, are updated from the FPC Status Word *(Figure 3-9)*.

Any operand indicated as being of type "f" will not cause a transfer if the Register addressing mode is specified, because the Floating-Point Registers are physically in the Floating-Point Data Path and are therefore available without CPU assistance.

3.6 FPDP INTERFACE

The FPC uses the Weitek WTL 3164 Floating-Point Data Path (FPDP) as the computational unit.

The FPDP is capable of supporting 32-bit and 64-bit IEEE floating-point operations. The FPDP consists of a Multiplier, ALU, Divide/Sqrt unit, 32 x 64-bit, Six-Port Register file, I/O port and control unit. There are six major internal 64-bit wide data buses used for data transfers between the different blocks inside the FPDP.

Using six data buses allows an input of two double-precision operands to a selected unit and to output one double-precision result in one WCLK cycle, supporting pipelining of a new double-precision instruction every WCLK cycle. (WCLK is half the frequency of BCLK.)

3.6.1 Controlling the FPDP

The FPC controls the FPDP on an instruction by instruction basis and not clock by clock. The instruction's control signals are delayed in the FPDP to match the pipeline stages inside the FPDP.

This allows the specifying of all the controls for a Reg to Reg instruction in a single control word. There are two types of operations that can be executed concurrently on the FPDP. The first operation is a floating-point arithmetic operation done on operands from the register file. The second operation is a Load/Store operation using the X port of the FPDP.

3.6.2 Instruction Control

The FPC controls the FPDP using a 33-bit control word. The control word contains all the information needed for the execution of an instruction including the function to be executed, source operands and destination of the result. The controls are pipelined along with the instruction and affect the operation at the appropriate times. The control word is sampled with the rising edge of the WCLK (system clock divided by two).

There are three functional fields in the control word:

1. The FUNC bits define the arithmetic operation to be executed.
2. The AAIN, ABIN, MAIN, MBIN, A ADD, B ADD, C ADD, D ADD bits specify the source and destination for arithmetic operation. Both C ADD and D ADD fields of the FPDP are connected to the D ADD field in the FPC control (C) word.
3. The E/F ADD and XCNT control the Load and Store operations.

FUNC, AAIN, ABIN, MAIN, MBIN Fields

The five-bit FUNC field specifies the arithmetic operation to be executed. The MAIN and AAIN control the muxes on the A inputs to the MULT and ALU respectively. MBIN and ABIN control the muxes on the B inputs to the MULT and ALU.

Aain, Main: A = "1", X = "0"
Abin, Mbin: B = "1", Y = "0"

5	1	1	1	1	5	5	5	5	5	4
FUNC	AAIN	ABIN	MAIN	MBIN	A ADD	B ADD	C ADD	D ADD	E/F ADD	XCNT
C41										C4

FIGURE 3-11. FPDP Control Word

3.0 Functional Description (Continued)

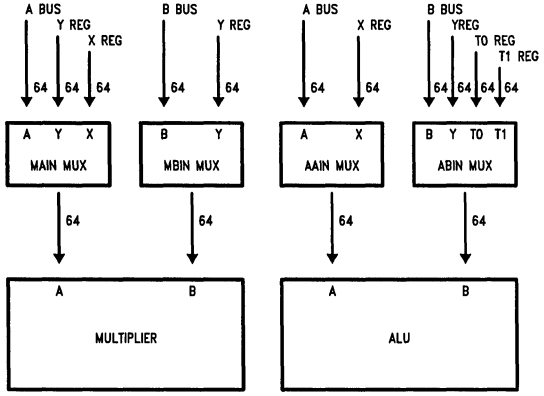

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FIGURE 3-12. FPDP Multiplier and ALU Bus Control

XCNT Field

The XCNT field specifies the I/O operation to be executed.

Code	Operation	Description
H'0	NOP	No Operation
H'1	EREG LS → XPAD	Transfer the Less Significant half of the register specified by EREG to the X-port (Store LS).
H'2	EREG MS → XPAD	Transfer the More Significant half of the register specified by EREG to the X-port (Store MS).
H'3	EREG INT → XPAD	Transfer Integer operand in the register specified by EREG to the X-port (Store Int).
H'5	XPAD → XREG/FREG LS	Load the Less Significant half of the data in the X-port into the XREG LS and into the register specified by FREG.
H'6	XPAD → XREG/FREG MS	Load the More Significant half of the data in the X-port into the XREG MS and into the register specified by FREG.
H'7	XPAD → XREG/FREG INT	Load the Integer operand in X-port into the XREG and into the register specified by FREG.

Data from FPC is transferred to the FPDP through the XPAD (32-bit I/O Port). The data is loaded into the XREG and into a register in the register file specified by the E/F ADD.

Loading the data to both locations allows the immediate use of the data by the ALU and MULT, bypassing the register file. Loading the data to register in the register file prevents data from being lost if the data from memory is needed a few cycles later.

The FPDP I/O Mode is determined by the control bits in the control register SR1 bits 4–0. The FPDP is being used in Undelayed Single-Pump mode (code 00000).

3.6.3 "2 Cycle Mode" and "3 Cycle Mode"

The FPDP has two timing modes, "Two cycle latency" and "Three cycle latency". In "Two cycle latency" single- and double-precision operations have latency of two cycles. In "Three cycle latency", double-precision multiply has a three cycle latency, single-precision multiplies and single- or double-precision ALU operations have latency of two cycles.

When using the "Three cycle latency" the Divide/Sqrt block uses the same clock as the FPDP (can not use the 2× clock). Although the "Three cycle latency" is not optimized for double-precision multiply it may be very useful if the system speed divided by two (WCLK output from FPC) is faster than the FPDP speed rating.

The FPC has a pin to specify the desired mode. In "Three cycle latency" the LMODE pin should be connected to V_{CC} and in "Two cycle latency" it should be connected to GND. The LMODE line is sampled during reset. After reset, as part of the initialization cycle, the FPC updates the Multiply Latency bit in the FPDP control register SR0 bit-7 (0 = "Two cycle latency", 1 = "Three cycle latency").

In "Three cycle latency" Divide/Sqrt block uses the DCLK3 (same as WCLK), in "Two cycle latency" it uses the DCLK2 (2 × WCLK). FPC uses the latency pin to determine the length of some instructions (number of cycles before FPC can signal DONE or TRAP).

This feature allows the CPU to run at more than twice the maximum FPDP speed.

3.0 Functional Description (Continued)

FPDP Speed Grade	WCLK "Two Cycle Latency"	WCLK "Three Cycle Latency"	Max System Speed
120 ns	120 ns	90 ns	45 ns
100 ns	100 ns	75 ns	38 ns
80 ns	80 ns	60 ns	30 ns
60 ns	60 ns	50 ns	25 ns

3.6.4 FPDP Mode Control Registers SR0, SR1

There are few options in the FPDP like Rounding, I/O, IEEE handling, Latency and other options that can be controlled by writing into the control registers SR0 and SR1.

After reset and whenever the user changes the relevant fields in the FSR, the FPC updates the FPDP control registers.

Fast/IEEE Mode SR0 bit 0

"1" Set to Fast mode. An underflowed instruction with disabled underflow exception delivers zero to the destination register.

Rounding

SR0 Bit-2	SR0 Bit-1	Rounding Mode
0	0	Round toward nearest value, if tie round toward even significant
0	1	Round toward zero
1	0	Round toward positive infinity
1	1	Round toward negative infinity

IntAbortOn SR0 Bit-3

"0" Internal abort off.

SR0 Bit-4

"0"

IlokOn SR0 Bit-5

"0" Disables Interlocks.

FpexSticky SR0 Bit-6

"0" FPEX is "Pulsed". In this mode, FPEX is asserted for one clock cycle.

Multiply Latency SR0 Bit-7

The FPDP has two multiply latency modes: Two cycle latency mode and Three cycle latency mode. (See separate paragraph on Latency Modes.)

SR0 Bit-7	Latency Mode
0	Two Cycle Latency Mode
1	Three Cycle Latency Mode

I/O Mode SR1 Bits 4–0

0 0 0 0 0 Single-Pump Undelayed

The FPDP is being used in the undelayed single-pump mode for load and store operations.

FpexDelay SR1 Bit-5

"1" Delayed FPEX- Mode.

BypassOn SR1 Bit-6

"1" Enables bypassing of operands between instructions.

SR1 Bit-7

"0"

3.6.5 IEEE Enables Register SR2

The SR2 register has enable bits for each of the exception conditions. The FPC updates the enable bits after Reset and whenever the user changes the relevant bits in the FSR. (See LFSR Instruction.)

	7							0
SR2 ENABLES	NaN	Inv	Dvz	Dnrm	Ovf	Unf	Inx	Iovf

FIGURE 3-13. IEEE Enables Register (FPDP)

FPC updates the Inv, Dvz, Ovf and Iovf, Unf, Inx enable bits to reflect those enable bits in the FSR.

The NaN bit is affected by the ROE bit in the FSR. If the ROE is cleared then NaN should be enabled (signal exception upon detection of NaN). If ROE is set NaN will be disabled.

The Dnrm bit is always enabled and detection of Dnrm as operand for operation will cause source exception.

Whenever the user changes the enable bit in the FSR, the same bit will be updated in the exception enable register in the FPDP.

Registers SR3–SR11 are not used by the FPC.

3.6.5.1 FPDP Status Lines (S3–S0)

The status of operation in the FPDP can be obtained by using the FPDP status lines (S3–S1). The status is not "sticky", therefore, the FPC has to sample the status lines in the correct timing. If ALU and MULT instructions end in the same cycle, the ALU status is valid at the end of the cycle and the MULT status is valid at the beginning of the following cycle.

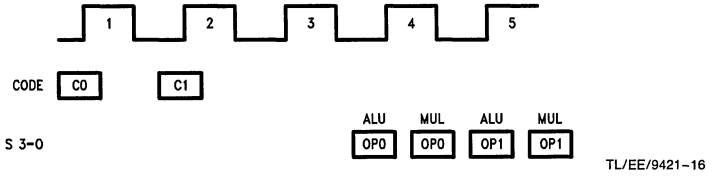

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FIGURE 3-14. FPDP Status Timing

3.0 Functional Description (Continued)

3.6.6 FPC-FPDP Clocks

FPC runs off BCLK and $\overline{BCLK}$, which is generated by the CPU. FPDP uses two clock signals, one clock signal for most of the chip and a special clock for the Divide unit. Both FPDP clock signals are supplied by the FPC.

3.6.6.1 FPC Clock

The FPC uses the system clocks (BCLK and $\overline{BCLK}$) generated by the NS32532. All the timing for signals between the CPU and the FPC are referenced to the BCLK. BCLK is a 30 MHz, TTL level clock (for timing characteristics refer to the timing chapter).

3.6.6.2 FPDP Main Clock (WCLK)

The FPDP uses a TTL level clock supplied by the FPC. The FPC generates the WCLK by dividing the BCLK by two. All the FPDP control signal times are specified relative to the rising edge of the WCLK.

3.6.6.3 Divide/Sqrt Unit Clock (DIVCLK)

The Divide/Sqrt unit in "Two cycle latency" mode uses a clock signal that is twice the WCLK (DCLK2). If the FPDP is in "three cycle latency", the Divide/Sqrt unit uses a clock signal that has the same frequency as WCLK (DCLK3). The FPC generates the correct DCLK automatically using the LMODE pin.

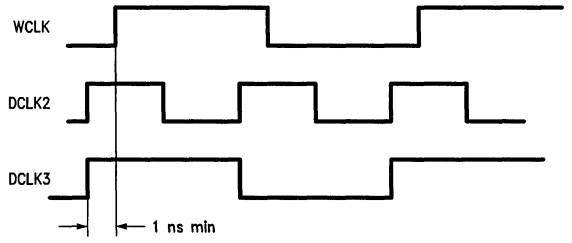

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FIGURE 3-15. Divide/Sqrt Clock DCLK2/DCLK3

4.0 Device Specifications

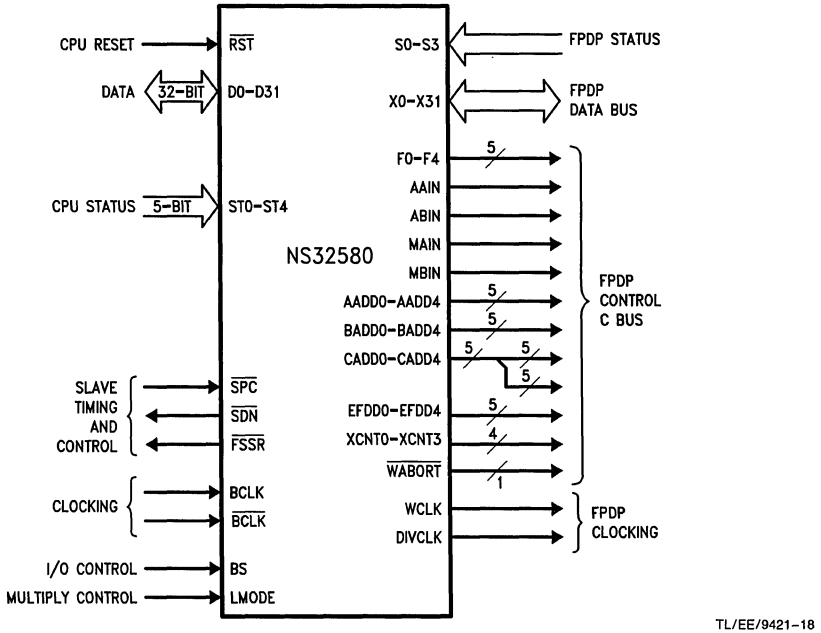

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FIGURE 4-1. NS32580 Interface Signals

4.0 Device Specifications (Continued)

4.1 NS32580 PIN DESCRIPTIONS

Descriptions of the NS32580 pins are given in the following sections. *Figure 4-1* shows the NS32580 interface signals grouped according to related functions.

4.1.1 Supplies

VCCL1–7 **Logic Power**—+5V positive supplies for on-chip logic.

VCCB1–8 **Buffers Power**—+5V positive supplies for on-chip buffers.

GNDL1–13 **Logic Ground**—Ground references for on-chip logic.

GNDB1–13 **Buffers Ground**—Ground references for on-chip buffers.

4.1.2 Input Signals

BCLK **Bus Clock**—Input clock for CPU bus timing; NS32532 system clock.

$\overline{\text{BCLK}}$ **Bus Clock Inverse**—Inverted input clock from NS32532.

BS **Byte Sex**—Specifies the I/O byte ordering of the FPC. If connected to GND the FPC is in 32000 mode. If connected to V_{CC} the FPC is in VME mode. The BS line must be valid during and after Reset. See Section 3.6.5.

LMODE **Latency Mode**—Specifies the latency mode of the FPC-FPDP. If connected to GND the FPC-FPDP is in the "Two cycle latency", if connected to V_{CC} the FPC-FPDP is in the "Three cycle latency". LMODE line must be valid during and after Reset.

$\overline{\text{RST}}$ **Reset**—Active low. Resets the last operation, clears the FIFOs and the FSR register to its default state.

S0–S3 **FPDP Status**—Indicates any exceptions or conditions that resulted from operations performed by the WTL 3164 floating-point data path.

$\overline{\text{SPC}}$ **Slave Processor Control**—Active low. Data strobe for slave transfers between the CPU and the FPC.

ST0–ST4 **CPU Status**—Bus cycle status code from CPU. ST0 is the least significant and rightmost bit.

1 1 1 0 0 —Reserved

1 1 1 0 1 —Transferring Operand

1 1 1 1 0 —Reading Status Word

1 1 1 1 1 —Broadcasting Slave ID

AADD0–AADD4 **A Read Port Register Address**—Chooses the inputs to the A bus of the FPDP.

AAIN **ALU A Input Select**—Controls the A input multiplexers of the FPDP ALU.

ABIN **ALU B Input Select**—Controls the B input multiplexers of the FPDP ALU.

BADD0–BADD4 **B Read Port Register Address**—Chooses the inputs to the B bus of the FPDP.

CADD0–CADD4 **C Write Port Register Address**—C/D Bus Control. Chooses the destinations of C and D buses. These signals should be connected to both the (CADD0–CADD4) and the (DADD0–DADD4) lines of the FPDP.

4.1.3 Output Signals

DIVCLK **Divide/Square Root Clock**—Clock signal for the Divide/Sqrt unit in the FPDP.

EFDD0–EFDD4 **E and/or F Port Register Address**—Chooses the source and destination for the Load/Store operations of the FPDP.

F0–F4 **Function Code**—Specifies the operation to be performed by the FPDP.

$\overline{\text{FSSR}}$ **Forced Slave Status Read**—Active low. When active, indicates that the slave status word should be read by the CPU. It is floating before and after being active.

MAIN **Multiplier A Input Select**—Controls the A input multiplexers of the multiplier of the FPDP.

MBIN **Multiplier B Input Select**—Controls the B input multiplexers of the multiplier of the FPDP.

$\overline{\text{SDN}}$ **Slave Done**—Active low. When active, indicates successful completion by the FPC-FPDP of a floating-point instruction. It is floating before and after being active.

$\overline{\text{WABORT}}$ **FPDP Abort**—Aborts the current and previous instructions in the FPDP.

WCLK **FPDP Clock**—Clock signal for the FPDP. It is BCLK divided by two. i.e., if BCLK is 30 MHz, WCLK will be 15 MHz.

XCNT0–XCNT3 **X Port Control**—They are the Load/Store controls for the FPDP.

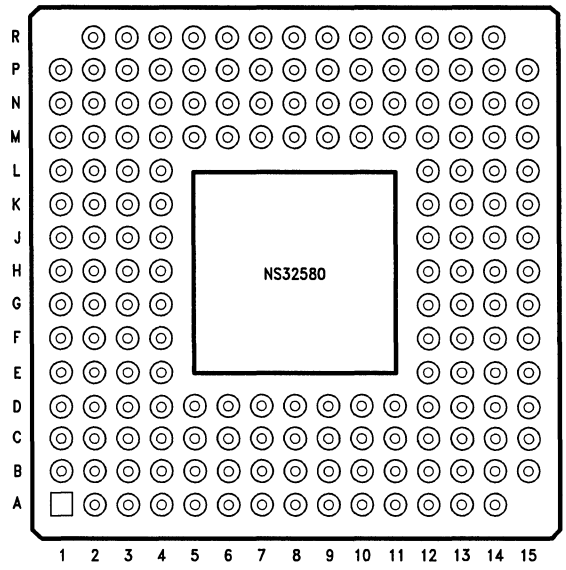
4.1.4 Input/Output Signals

D0–D31 **CPU Data Bus**—Data bus between FPC and the CPU.

X0–X31 **FPDP Data Bus**—Data bus between FPC and the FPDP X port.

4.0 Device Specifications (Continued)

Connection Diagram



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Bottom View

FIGURE 4-2. 172-Pin PGA Package

Order Number NS32580-20, NS32580-25 or NS32580-30
See NS Package Number U172B

4.0 Device Specifications (Continued)

NS32580 Pinout Descriptions

Desc	Pin
VCCL1	A2
GNDB1	A3
GNDL1	A4
XCNT0	A5
XCNT3	A6
EFADD1	A7
EFADD2	A8
GNDL2	A9
GNDB2	A10
CADD0	A11
CADD2	A12
CADD3	A13
BADD0	A14
GNDB3	B1
GNDL3	B2
X0	B3
XCNT1	B4
XCNT2	B5
EFADD0	B6
EFADD3	B7
$\overline{\text{BCLK}}$	B8
WCLK	B9
DIVCLK	B10
EFADD4	B11
CADD1	B12
CADD4	B13
BADD1	B14
BADD2	B15
VCCB1	C1
X2	C2
X1	C3
VCCL2	C4
D1	C5
D0	C6
NC	C7
GNDL4	C8
GNDB4	C9
BCLK	C10
$\overline{\text{RST}}$	C11
NC	C12
BADD3	C13
AADD0	C14
BADD4	C15

Desc	Pin
X3	D1
X4	D2
NC	D3
D2	D4
D17	D5
D16	D6
NC	D7
GNDL5	D8
NC	D9
NC	D10
NC	D11
VCCB2	D12
D15	D13
AADD1	D14
AADD2	D15
X5	E1
X7	E2
D18	E3
D3	E4
D31	E12
D14	E13
AADD3	E14
AADD4	E15
X6	F1
X9	F2
D19	F3
VCCL3	F4
D30	F12
VCCB3	F13
MAIN	F14
MBIN	F15
X8	G1
X10	G2
D4	G3
D20	G4
D13	G12
D29	G13
AAIN	G14
ABIN	G15
X11	H1
X12	H2
NC	H3
D5	H4

Desc	Pin
D28	H12
GNDB5	H13
F0	H14
F1	H15
X13	J1
X15	J2
GNDB6	J3
D21	J4
D12	J12
D27	J13
F2	J14
F3	J15
X14	K1
X17	K2
D6	K3
D22	K4
D11	K12
NC	K13
SO	K14
F4	K15
X16	L1
X18	L2
D7	L3
D23	L4
$\overline{\text{SPC}}$	L12
$\overline{\text{SDN}}$	L13
S2	L14
S1	L15
X19	M1
Reserved	M2
VCCL4	M3
D8	M4
GNDB7	M5
D26	M6
GNDL6	M7
VCCB4	M8
NC	M9
ST0	M10
ST1	M11
NC	M12
GNDL7	M13
$\overline{\text{WABORT}}$	M14
S3	M15

Desc	Pin
VCCL5	N1
GNDB8	N2
Reserved	N3
D24	N4
D25	N5
D9	N6
D10	N7
NC	N8
VCCB5	N9
ST2	N10
ST4	N11
$\overline{\text{FSSR}}$	N12
GNDB9	N13
VCCB6	N14
GNDL8	N15
GNDL9	P1
VCCL6	P2
X21	P3
X23	P4
X25	P5
X26	P6
X28	P7
X31	P8
X30	P9
BS	P10
ST3	P11
VCCB7	P12
GNDB10	P13
GNDL10	P14
GNDB11	P15
GNDB12	R2
GNDL11	R3
VCCL7	R4
X20	R5
X22	R6
X24	R7
X27	R8
X29	R9
LMODE	R10
GNDB13	R11
GNDL12	R12
VCCB8	R13
GNDL13	R14

Note: NC = No Connection

4.0 Device Specifications (Continued)

4.2 ABSOLUTE MAXIMUM RATINGS

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Temperature Under Bias	0°C to +70°C
Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to GND	−0.5V to +7V
Power Dissipation	1.5W

ESD Rating is to be determined.

Note: *Absolute maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended; operation should be limited to those conditions specified under Electrical Characteristics.*

4.3 ELECTRICAL CHARACTERISTICS T_A = 0°C to 70°C, V_{CC} = 5V ±10%, GND = 0V

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High Level Input Voltage		2.0		V_{CC} + 0.5	V
V_{IL}	Low Level Input Voltage		−0.5		0.8	V
V_{OH}	High Level Output Voltage	I_{OH} = −400 μA	2.4			V
V_{OL}	Low Level Output Voltage	I_{OL} = 2 mA			0.4	V
I_I	Input Load Current	0 ≤ V_{IN} ≤ V_{CC}				
I_L	Leakage Current (Output and I/O Pins in TRI-STATE®/Input Mode)	0.4 ≤ V_{OUT} ≤ 2.4V				
I_{CC}	Active Supply Current	I_{OUT} = 0, T_A = 25°C			300	mA
C_{IN}	Input Capacitance					pF
C_{OUT}	Output Capacitance					pF

4.4 SWITCHING CHARACTERISTICS

4.4.1 Definitions

All the Timing Specifications given in this section refer to 0.8V and 2.0V on all the input and output signals as illustrated in *Figures 4.2* and *4.3*, unless specifically stated otherwise.

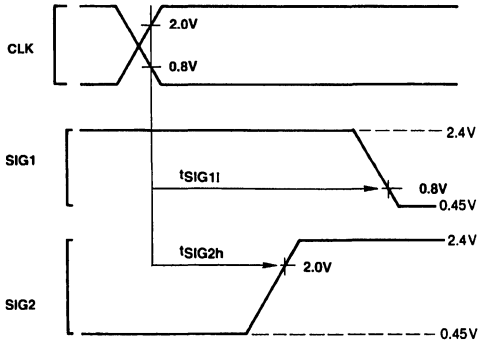

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FIGURE 4-3. Timing Specification Standard (Signal Valid after Clock Edge)

ABBREVIATIONS

L.E. — Leading Edge
T.E. — Trailing Edge
R.E. — Rising Edge
F.E. — Falling Edge

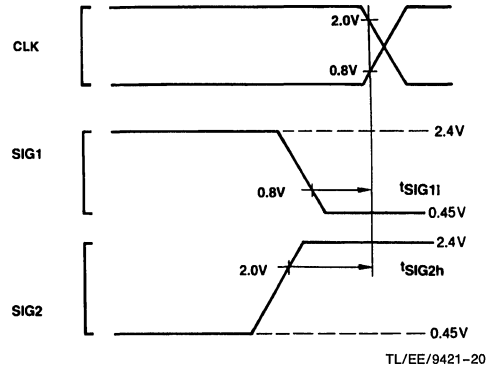

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FIGURE 4-4. Timing Specification Standard (Signal Valid before Clock Edge)

4.0 Device Specifications (Continued)

4.4.2 Timing Tables Maximum times assume temperature range 0°C to 70°C

4.4.2.1 Output Signal Propagation Delays Maximum times assume capacitive loading of 100 pF

Symbol	*Figure*	Description	Reference/ Conditions	NS32580-20		NS32580-25		NS32580-30		Units
				Min	Max	Min	Max	Min	Max	
t_{Dv}	*4-8*	CPU Data Valid	After R.E., BCLK T2		35		27		23	ns
t_{Doh}	*4-8*	CPU Data Hold	After R.E., BCLK Next T1/Ti	2		2		2		ns
t_{Dnf}	*4-8*	CPU Data Not Floating	After R.E., BCLK Next T1/Ti		28		23		19	ns
t_{SDa}	*4-10*	$\overline{SDN}$ Signal Active	After R.E., BCLK		35		28		22	ns
t_{SDia}	*4-10*	$\overline{SDN}$ Signal Inactive	After R.E., Next BCLK	2		2		2		ns
t_{SDnf}	*4-10*	$\overline{SDN}$ Signal Not Floating	After R.E., BCLK		25		20		17	ns
t_{FSSRa}	*4-11*	$\overline{FSSR}$ Signal Active	After R.E., BCLK		35		28		22	ns
t_{FSSRia}	*4-11*	$\overline{FSSR}$ Signal Inactive	After R.E., Next BCLK	2		2		2		ns
t_{FSSRnf}	*4-11*	$\overline{FSSR}$ Signal Not Floating	After R.E., BCLK		25		20		17	ns
t_{Cv}	*4-14*	C Bus and $\overline{WABORT}$ Valid	After R.E., WCLK		83		63		50	ns
t_{Ch}	*4-14*	C BUS and $\overline{WABORT}$ Hold Time	After R.E., WCLK	2		2		2		ns
t_{XLv}	*4-14*	FPDP Data Valid	After R.E., WCLK		83		63		50	ns
t_{XLh}	*4-14*	FPDP Data Hold Time	After R.E., WCLK	2		2		2		ns
t_{D2p}	*4-13*	DCLK2 Period	From 1.5V R.E., to 1.5V R.E.	50		40		33.3		ns
t_{D2h}	*4-13*	DCLK2 High Time	From 1.5V R.E., to 1.5V F.E.	22		17		14.5		ns
t_{D2l}	*4-13*	DCLK2 Low Time	From 1.5V F.E. to 1.5V R.E.	22		17		14.5		ns
t_{D3p}	*4-13*	DCLK3 Period	From 1.5V R.E., to 1.5V R.E.	100		80		66.6		ns
t_{D3h}	*4-13*	DCLK3 High Time	From 1.5V R.E., to 1.5V F.E.	45		36		30		ns
t_{D3l}	*4-13*	DCLK3 Low Time	From 1.5V F.E., to 1.5V R.E.	45		36		30		ns
t_{WCLKp}	*4-13*	WCLK Period	From 1.5V R.E., to 1.5V R.E.	100		80		66.6		ns
t_{WCLKh}	*4-13*	WCLK High Time	From 1.5V R.E., to 1.5V F.E.	45		36		30		ns
t_{WCLKl}	*4-13*	WCLK Low Time	From 1.5V F.E. to 1.5V R.E.	45		36		30		ns
t_{DWd}	*4-13*	DCLK2/DCLK3 to WCLK Delay	From 1.5V R.E., to 1.5V R.E.	2.5	8	2.5	8	2.5	8	ns
t_{Wr}	*4-13*	FPDP Clock Rise Time	From 0.4V R.E., to 2.4V R.E.		2		2		2	ns
t_{Wf}	*4-13*	FPDP Clock Fall Time	From 2.4V F.E. to 0.4V F.E.		2		2		2	ns

4.4.2.2 Input Signal Requirements NS32580–20, NS32580–25, NS32580–30

Symbol	*Figure*	Description	Reference/ Conditions	NS32580-20		NS32580-25		NS32580-30		Units
				Min	Max	Min	Max	Min	Max	
t_{BCp}	*4-5*	BCLK Period	R.E., BCLK to Next R.E., BLCK	50	100	40	100	33.3	100	ns
t_{BCh}	*4-5*	BCLK High Time	At 2.0V on BCLK (Both Edges)	0.5 t_{BCp} −5		0.5 t_{BCp} −4		0.5 t_{BCp} −3		
t_{BCl}	*4-5*	BCLK Low Time	At 0.8V on BCLK (Both Edges)	0.5 t_{BCp} −5		0.5 t_{BCp} −4		0.5 t_{BCp} −3		
t_{BCr}	*4-5*	BCLK Rise Time	0.8V to 2.0V on R.E., BCLK		5		4		3	ns
t_{BCf}	*4-5*	BCLK Fall Time	2.0V to 0.8V on F.E., BCLK		5		4		3	ns
t_{NBCp}	*4-5*	$\overline{BCLK}$ Period	R.E., $\overline{BCLK}$ to Next R.E., $\overline{BCLK}$	50	100	40	100	33.3	100	ns
t_{NBCh}	*4-5*	$\overline{BCLK}$ High Time	At 2.0V on $\overline{BCLK}$ (Both Edges)	0.5 t_{NBCp} −5		0.5 t_{NBCp} −4		0.5 t_{NBCp} −3	120	ns

4.0 Device Specifications (Continued)

4.4.2 Timing Tables Maximum times assume temperature range 0°C to 70°C (Continued)

4.4.2.2 Input Signal Requirements NS32580–20, NS32580–25, NS32580–30 (Continued)

Symbol	*Figure*	Description	Reference/ Conditions	NS32580-20		NS32580-25		NS32580-30		Units
				Min	Max	Min	Max	Min	Max	
t_{NBCl}	*4-5*	$\overline{BCLK}$ Low Time	At 0.8V on $\overline{BCLK}$ (Both Edges)	0.5 t_{NBCp} −5		0.5 t_{NBCp} −4		0.5 t_{NBCp} −3	120	ns
t_{NBCr}	*4-5*	$\overline{BCLK}$ Rise Time	0.8V to 2.0V on R.E., $\overline{BCLK}$		5		4		3	ns
t_{NBCf}	*4-5*	$\overline{BCLK}$ Fall Time	2.0V to 0.8V on F.E., $\overline{BCLK}$		5		4		3	ns
$t_{BCNBCrf}$	*4-5*	Bus Clock Skew	2.0V on R.E., BCLK to 0.8V on F.E., $\overline{BCLK}$	−2	+2	−2	+2	−1	+1	ns
$t_{BCNBCfr}$	*4-5*	Bus Clock Skew	0.8V on F.E., BCLK to 2.0V on R.E., $\overline{BCLK}$	−2	+2	−2	+2	−1	+1	ns
t_{PWR}	*4-6*	Power Stable to R.E. of $\overline{RST}$	After V_{CC} Reaches 4.5V	50		40		30		μs
t_{RSTs}	*4-6, 4-7*	$\overline{RST}$ Setup Time	Before R.E., BCLK	14		12		11		ns
t_{RSTw}	*4-7*	$\overline{RST}$ Pulse Width	At 0.8V (Both Edges)	64		64		64		t_{BCp}
t_{STs}	*4-8, 4-9*	CPU Status Setup Time	Before R.E., BCLK T2	36		30	24	24		ns
t_{STh}	*4-8, 4-9*	CPU Status Hold Time	After R.E., BCLK T2	15		12	10	10		ns
t_{SPCs}	*4-8, 4-9*	$\overline{SPC}$ Setup Time	Before R.E., BCLK T2	30		23	20	20		ns
t_{SPCh}	*4-8, 4-9*	$\overline{SPC}$ Hold Time	After R.E., BCLK T2	0	t_{BCp} +19	0	t_{BCp} +15	0	t_{BCp} +12	ns
t_{Ds}	*4-9*	Data Setup Time	Before R.E., BCLK T2	7		5		3		ns
t_{Dh}	*4-9*	Data Hold Time	After R.E., BCLK Next T1 or Ti	−4		−4		−4		ns
t_{SAs}	*4-12*	FPDP ALU Status Setup Time	Before R.E., WCLK	9		9		8		ns
t_{SAh}	*4-12*	FPDP ALU Status Hold Time	After R.E., WCLK	2		2		2		ns
t_{SMs}	*4-12*	FPDP Multiplier Status Setup Time	Before F.E., WCLK	9		9		8		ns
t_{SMh}	*4-12*	FPDP Multiplier Status Hold Time	After F.E., WCLK	2		2		2		ns
t_{XSs}	*4-14*	FPDP Data Setup Time	Before R.E., WCLK	9		9		9		ns
t_{XSh}	*4-14*	FPDP Data Hold Time	After R.E., WCLK	2		2		2		ns

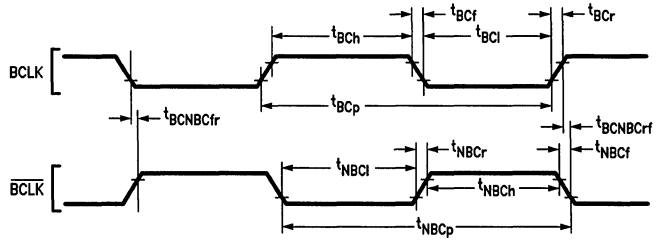

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FIGURE 4-5. Clock Waveforms

4.0 Device Specifications (Continued)

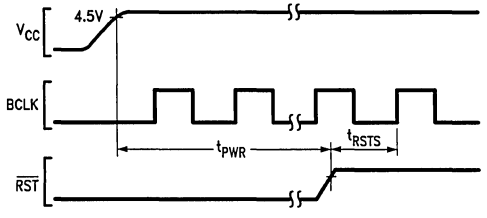

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FIGURE 4-6. Power-On Reset

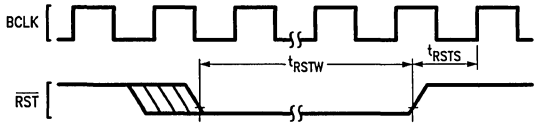

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FIGURE 4-7. Non-Power-On Reset

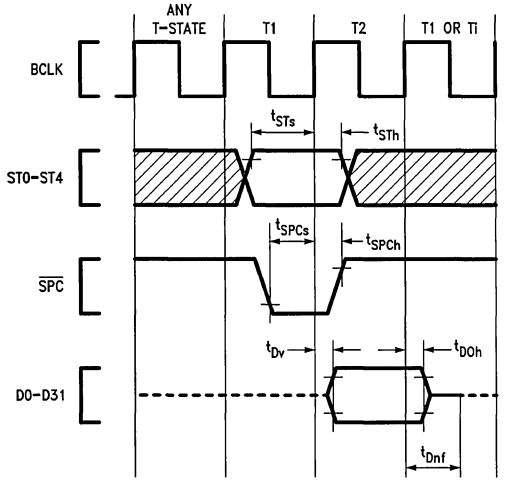

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FIGURE 4-8. Read Cycle from FPC

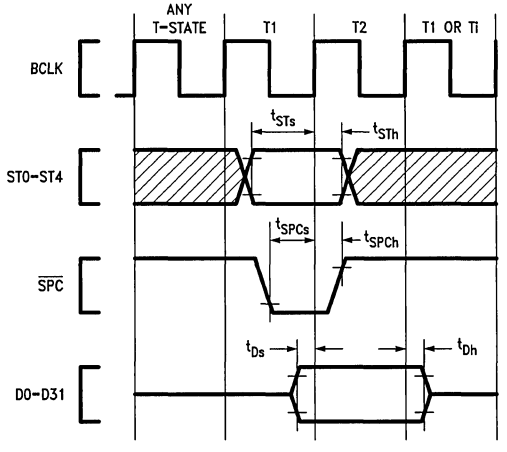

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FIGURE 4-9. Write Cycle to FPC

3

4.0 Device Specifications (Continued)

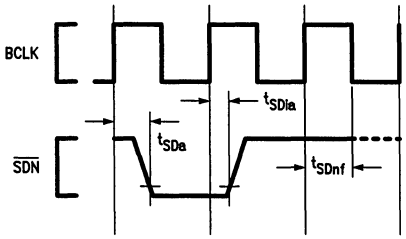

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FIGURE 4-10. Slave Processor Done Timing

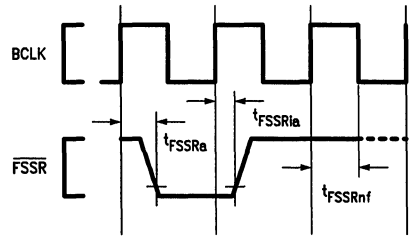

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FIGURE 4-11. $\overline{FSSR}$ Signal Timing

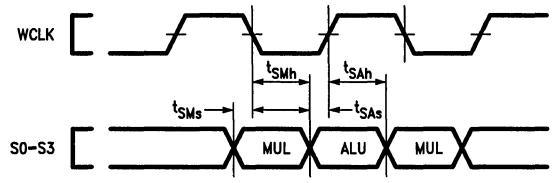

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FIGURE 4-12. FPDP Status Signal Timing

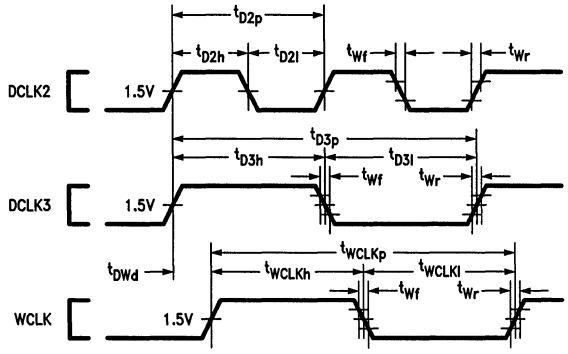

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FIGURE 4-13. FPDP Clock Signal Timing

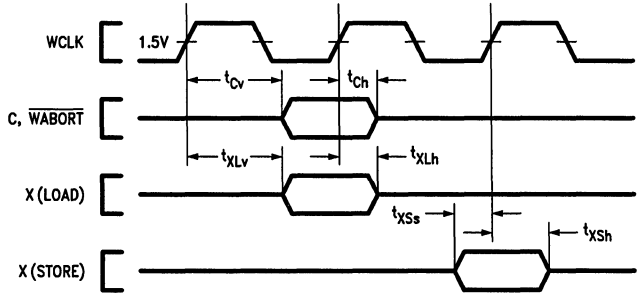

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FIGURE 4-14. FPDP Output Signal Timing

Appendix A

COMPATIBILITY OF FPC-FPDP WITH NS32081/NS32381

NS32081	NS32381	NS32580
INSTRUCTIONS		
	NS32081 +	NS32081 +
	DOTf	MACf
	POLYf	SQRTf
	SCALBf	
	LOGBf	
REGISTERS		
8 x 32 Bit	8 x 64 Bit	8 x 64 Bit
RESERVED OPERANDS		
DNRM	DNRM	DNRM
NaN	NaN	NaN can be enabled or Disable.
Infinity	Infinity	Infinity is NOT a reserved operand.

NS32081	NS32381	NS32580
FSR		
	NS32081 FSR +	NS32081 FSR +
	RMB	RMB
		ROE
		IVE
		DZE
		OVE
		IOE
		ROF
		IVF
		DZF
		OVF
		IOF

Appendix B

PERFORMANCE ANALYSIS

The execution time is calculated from $\overline{SPC}$ (T1, T2 included) to $\overline{SDN}$ (including the $\overline{SDN}$ pulse)

Instruction	Latency reg, reg 2 cycles mode	Latency reg, reg 3 cycles mode	Throughput reg, reg 2 cycles mode	Throughput reg, reg 3 cycles mode	Pipe Break
ADDf/I	13	13	2	2	No
SUBf/I	13	13	2	2	No
MULf	13	13	2	2	No
MULI	13	15	2	4	No
DIVf	29	43	Up to 29	Up to 43	No
DIV1	43	71	Up to 43	Up to 71	No
MOVf/I	13	13	2	2	No
ABSf/I	13	13	2	2	No
NEGf/I	13	13	2	2	No
CMPf/I	13 + CPU	13 + CPU	—	—	Yes
FLOORfi	13 + CPU	13 + CPU	—	—	Yes
TRUNCfi	13 + CPU	13 + CPU	—	—	Yes
ROUNDfi	13 + CPU	13 + CPU	—	—	Yes
MOVFL	13 + CPU	13 + CPU	—	—	Yes
MOVLF	13 + CPU	13 + CPU	—	—	Yes
MOVif	17 + CPU	17 + CPU	—	—	Yes
MOVil	13 + CPU	13 + CPU	—	—	Yes
LFSR	13	13	—	—	Yes
SFSR	13 + CPU	13 + CPU	—	—	Yes
MACf	15	15	6	6	No
MACI	15	17	6	8	No
SQRTf	41	65	Up to 41	Up to 65	No
SQRTI	69	123	Up to 69	Up to 123	No

Appendix B (Continued)

Add the following CPU cycles to the base (reg, reg) number of cycles for the different cases:

Instruction	Latency 2 Cycles Mode	Latency 3 Cycles Mode	Throughput 2 Cycles Mode	Throughput 3 Cycles Mode	Pipe Break
MONADIC FLOAT (One Operand)					
mem, reg	0	0	2	2	see reg, reg
reg, mem	0 + CPU	0 + CPU	—	—	Yes
mem, mem	0 + CPU	0 + CPU	—	—	Yes
DYADIC FLOAT (Two Operands)					
mem, reg	0	0	2	2	see reg, reg
reg, mem	0 + CPU	0 + CPU	—	—	Yes
mem, mem	2 + CPU	2 + CPU	—	—	Yes
MONADIC LONG (One Operand)					
mem, reg	2	2	4	4	see reg, reg
reg, mem	2 + CPU	2 + CPU	—	—	Yes
mem, mem	2 + CPU	2 + CPU	—	—	Yes
DYADIC LONG (Two Operands)					
mem, reg	2	2	4	4	see reg, reg
reg, mem	6 + CPU	6 + CPU	—	—	Yes
mem, mem	6 + CPU	6 + CPU	—	—	Yes

Note: CPU stands for the time it takes the CPU to take the result from the FPC and resume operation.

Section 4

Peripherals

Section 4 Contents

National Semiconductor

PRELIMINARY

NS32C201-10/NS32C201-15 Timing Control Units

General Description

The NS32C201 Timing Control Unit (TCU) is a 24-pin device fabricated using National's microCMOS technology. It provides a two-phase clock, system control logic and cycle extension logic for the Series 32000® microprocessor family. The TCU input clock can be provided by either a crystal or an external clock signal whose frequency is twice the system clock frequency.

In addition to the two-phase clock for the CPU and MMU (PHI1 and PHI2), it also provides two system clocks for general use within the system (FCLK and CTTL). FCLK is a fast clock whose frequency is the same as the input clock, while CTTL is a replica of PHI1 clock.

The system control logic and cycle extension logic make the TCU very attractive by providing extremely accurate bus control signals, and allowing extensive control over the bus cycle timing.

Features

- Oscillator at twice the CPU clock frequency
- 2 phase full V_{CC} swing clock drivers (PHI1 and PHI2)
- 4-bit input ($\overline{WAITn}$) allowing precise specification of 0 to 15 wait states
- Cycle Hold for system arbitration and/or memory refresh
- System timing (FCLK, CTTL) and control ($\overline{RD}$, $\overline{WR}$, and $\overline{DBE}$) outputs
- General purpose Timing State Output ($\overline{TSO}$) that identifies internal states
- Peripheral cycle to accommodate slower MOS peripherals
- Provides "ready" (RDY) output for the Series 32000 CPUs
- Synchronous system reset generation from Schmitt trigger input
- Phase synchronization to a reference signal
- High-speed CMOS technology
- TTL compatible inputs
- Single 5V power supply
- 24-pin dual-in-line package

Block Diagram

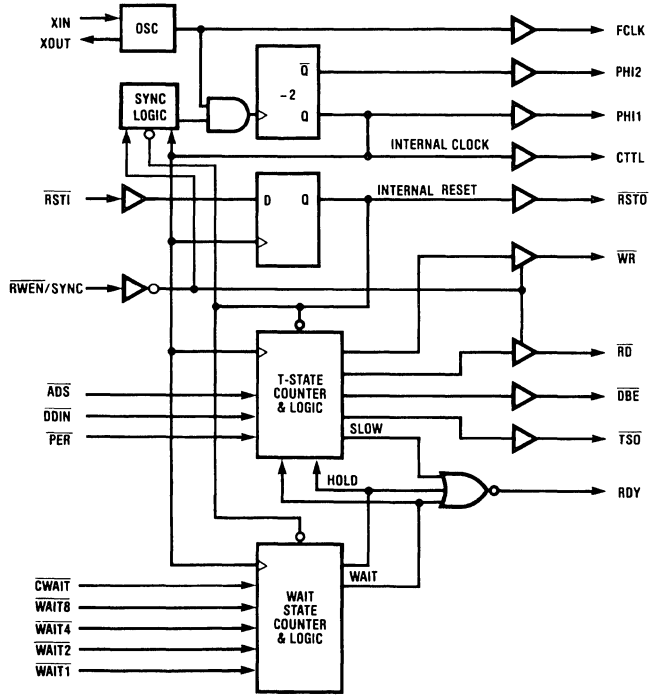

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Table of Contents

List of Illustrations

1.0 Functional Description

1.1 POWER AND GROUNDING

The NS32C201 requires a single +5V power supply, applied to pin 24 (V_{CC}). See Electrical Characteristics. The Logic Ground on pin 12 (GND), is the common pin for the TCU.

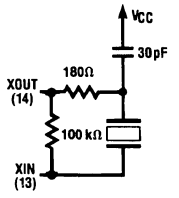
A 0.1 μF, ceramic decoupling capacitor must be connected across V_{CC} and GND, as close to the TCU as possible.

1.2 CRYSTAL OSCILLATOR CHARACTERISTICS

The NS32C201 has an internal oscillator that requires connections of the crystal and bias components to XIN and XOUT as shown in *Figure 1-1.* It is important that the crystal and the RC components be mounted in close proximity to the XIN, XOUT and V_{CC} pins to keep printed circuit trace lengths to an absolute minimum.

Typical Crystal Specifications:

Type ..... At-Cut
Tolerance ..... 0.005% at 25°C
Stability ..... 0.01% from 0° to 70°C
Resonance ..... Fundamental (parallel)
Capacitance ..... 20 pF
Maximum Series Resistance 50Ω



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CRYSTAL FREQUENCY (MHz)	R (OHM)
6-12	470
12-18	220
18-24	100
24-30	47

FIGURE 1-1. Crystal Connection Diagram

1.3 CLOCKS

The NS32C201 TCU has four clock output pins. The PHI1 and PHI2 clocks are required by the Series 32000 CPUs. These clocks are non-overlapping as shown in *Figure 1-2.*

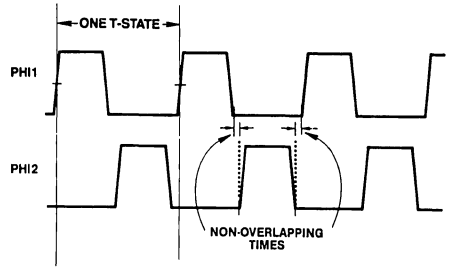

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FIGURE 1.2. PHI1 and PHI2 Clock Signals

Each rising edge of PHI1 defines a transition in the timing state of the CPU.

As the TCU generates the various clock signals with very short transition timings, it is recommended that the conductors carrying PHI1 and PHI2 be kept as short as possible. It is also recommended that only the Series 32000 CPU and, if used, the MMU (Memory Management Unit) be connected to the PHI1 and PHI2 clocks.

CTTL is a clock signal which runs at the same frequency as PHI1 and is closely balanced with it.

FCLK is a clock, running at the frequency of XIN input. This clock has a frequency that is twice the CTTL clock frequency. The exact phase relationship between PHI1, PHI2, CTTL and FLCK can be found in Section 2.

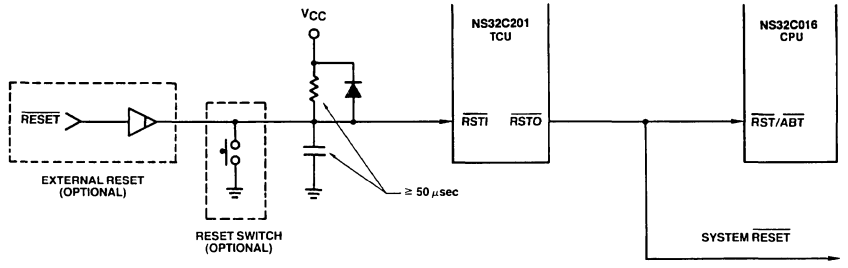

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FIGURE 1-3a. Recommended Reset Connections (Non Memory-Managed System)

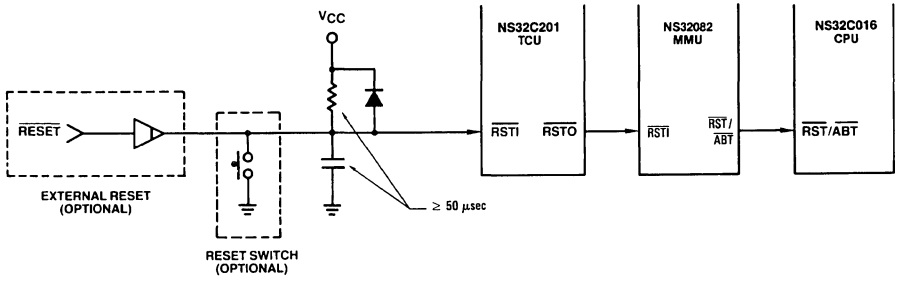

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FIGURE 1-3b. Recommended Reset Connections (Memory-Managed System)

1.0 Functional Description (Continued)

1.4 RESETTING

The NS32C201 TCU provides circuitry to meet the reset requirements of the Series 32000 CPUs. If the Reset Input line, $\overline{RSTI}$ is pulled low, the TCU asserts $\overline{RSTO}$ which resets the Series 32000 CPU. This Reset Output may also be used as a system reset signal. *Figure 1-3a* illustrates the reset connections for a non Memory-Managed system. *Figure 1-3b* illustrates the reset connections for a Memory-Managed system.

1.5 SYNCHRONIZING TWO OR MORE TCUs

During reset, (when $\overline{RSTO}$ is low), one or more TCUs can be synchronized with a reference (Master) TCU. The $\overline{RWEN}$/SYNC input to the slave TCU(s) is used for synchronization. The Slave TCU samples the $\overline{RWEN}$/SYNC input on the rising edge of XIN. When $\overline{RSTO}$ is low and CTTL is high (see *Figure 1-5*), if $\overline{RWEN}$/SYNC is sampled high, the phase of CTTL of the Slave TCU is shifted by one XIN clock cycle.

Two possible circuits for TCU synchronization are illustrated in *Figures 1-4a* and *1-4b*. It should be noted that when $\overline{RWEN}$/SYNC is high, the $\overline{RD}$ and $\overline{WR}$ signals will be TRI-STATE on the slave TCU.

Note: $\overline{RWEN}$/SYNC should not be kept constantly high during reset, otherwise the clock will be stopped and the device will not exit reset when $\overline{RSTI}$ is deasserted.

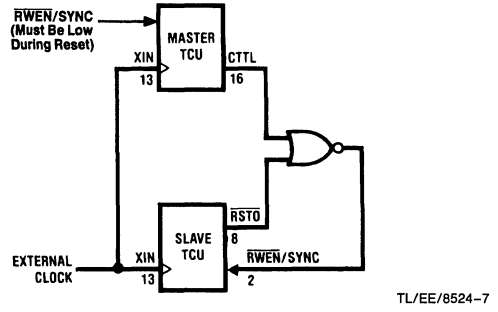

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FIGURE 1-4a. Slave TCU Does Not Use $\overline{RWEN}$ During Normal Operation

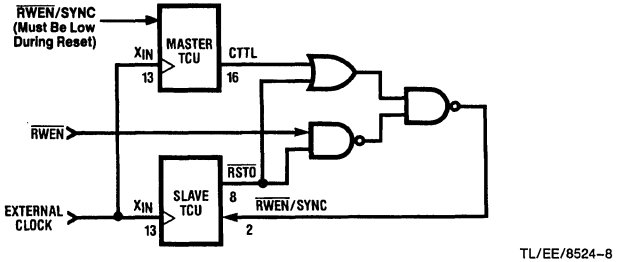

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FIGURE 1-4b. Slave TCU Uses Both SYNC and $\overline{RWEN}$

Note: When two or more TCUs are to be synchronized, the XIN of all the TCUs should be connected to an external clock source. For details on the external clock, see Switching Specifications in Section 2.

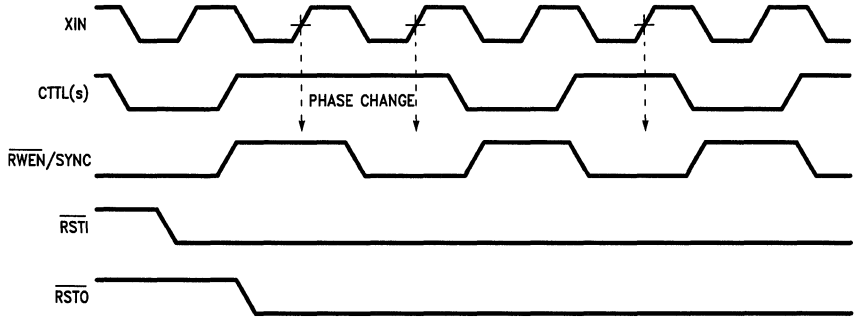

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FIGURE 1-5. Synchronizing Two TCUs

1.0 Functional Description (Continued)

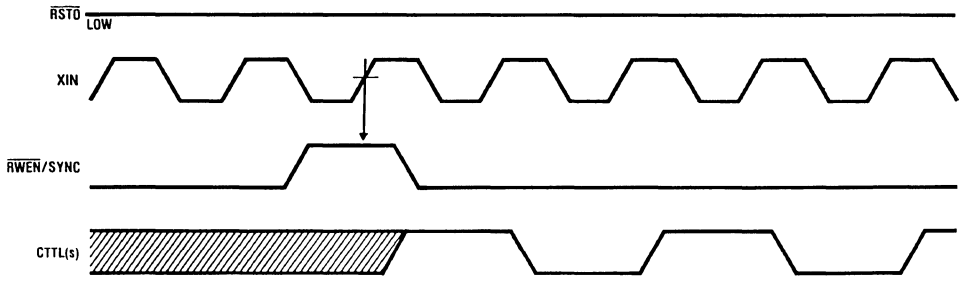

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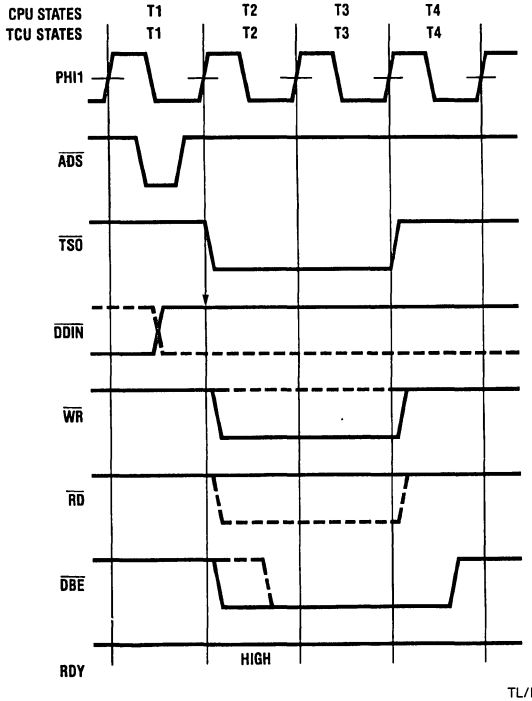
FIGURE 1-6. Synchronizing One TCU to An External Pulse

In addition to synchronizing two or more TCUs, the RWEN/SYNC input can be used to "fix" the phase of one TCU to an external pulse. The pulse to be used must be high for only one rising edge of XIN. Independent of CTTL's state at the XIN rising edge, the CTTL state following the XIN rising edge will be high. *Figure 1-6* shows the timing of this sequence.

1.6 BUS CYCLES

In addition to providing all the necessary clock signals, the NS32C201 TCU provides bus control signals to the system. The TCU senses the ADS signal from the CPU or MMU to start a bus cycle. The DDIN input signal is also sampled to determine whether a Read or Write cycle is to be generated. In addition to RD and WR, other signals are provided: DBE and TSO. DBE is used to enable data buffers. The leading edge of DBE is delayed a half clock period during Read cycles to avoid bus conflicts between data buffers and either the CPU or the MMU. This is shown in *Figure 1-7*.

The Timing State Output (TSO) is a general purpose signal that may be used by external logic for synchronizing to a System cycle. TSO is activated at the beginning of state T2 and returns to the high level at the beginning of state T4 of the CPU cycle. TSO can be used to gate the CWAIT signal when continuous waits are required. Another application of TSO is the control of interface circuitry for dynamic RAMs.



Notes:

1. The CPU and TCU view some timing states (T-states) differently. For clarity, references to T-states will sometimes be followed by (TCU) or (CPU). (CPU) also implies (MMU).
2. Arrows indicate when the TCU samples the input.
3. RWEN is assumed low (RD and WR enabled) unless specified differently.
4. For clarity, T-states for both the TCU and CPU are shown above the diagrams. (See Note 1.)

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FIGURE 1-7. Basic TCU Cycle (Fast Cycle)

1.0 Functional Description (Continued)

1.7 BUS CYCLE EXTENSION

The NS32C201 TCU uses the Wait input signals to extend normal bus cycles. A normal bus cycle consists of four PHI1 clock cycles. Whenever one or more Wait inputs to the TCU are activated, a bus cycle is extended by at least one PHI1 clock cycle. The purpose is to allow the CPU to access slow memories or peripherals. The TCU responds to the Wait signals by pulling the RDY signal low as long as Wait States are to be inserted in the Bus cycle.

There are three basic cycle extension modes provided by the TCU, as described below.

1.7.1 Normal Wait States

This is a normal Wait State insertion mode. It is initiated by pulling $\overline{\text{CWAIT}}$ or any of the $\overline{\text{WAITn}}$ lines low in the middle of T2. *Figure 1-8* shows the timing diagram of a bus cycle when $\overline{\text{CWAIT}}$ is sampled high at the end of T1 and low in the middle of T2.

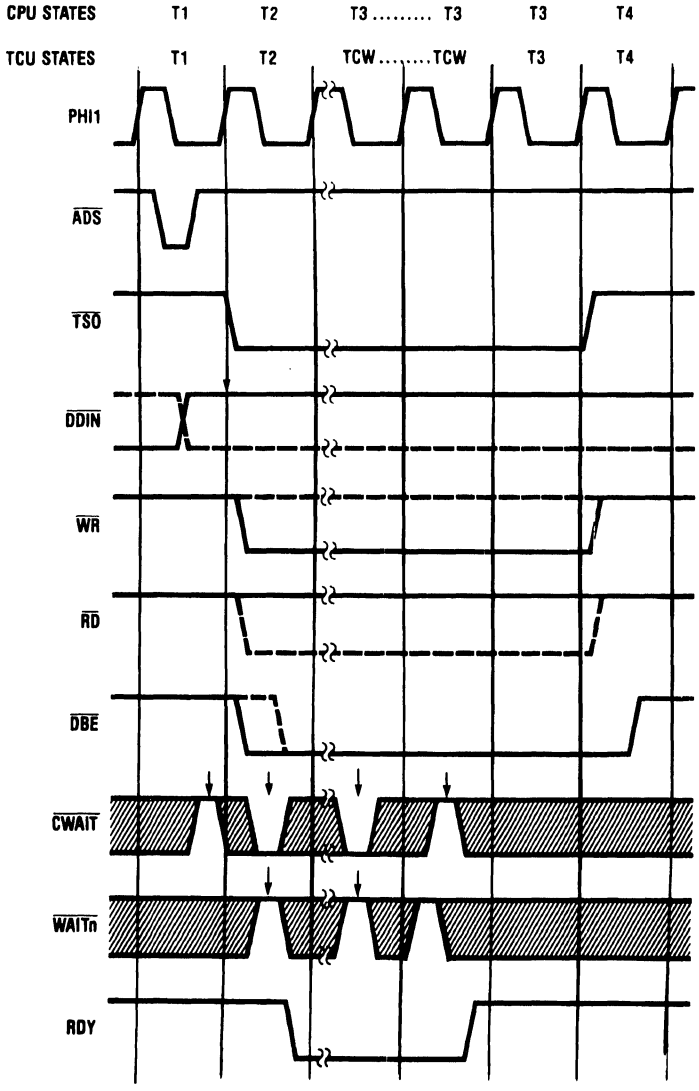

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FIGURE 1-8. Wait State Insertion Using $\overline{\text{CWAIT}}$ (Fast Cycle)

1.0 Functional Description (Continued)

The RDY signal goes low during T2 and remains low until $\overline{CWAIT}$ is sampled high by the TCU. RDY is pulled high by the TCU during the same PHI1 cycle in which the $\overline{CWAIT}$ line is sampled high.

If any of the $\overline{WAITn}$ signals are sampled low during T2 and $\overline{CWAIT}$ is high during the entire bus cycle, then the RDY line goes low for 1 to 15 clock cycles, depending on the binary weighted value of $\overline{WAITn}$. If, for example, $\overline{WAIT1}$ and $\overline{WAIT4}$ are sampled low, then five wait states will be inserted. This is shown in *Figure 1-9*.

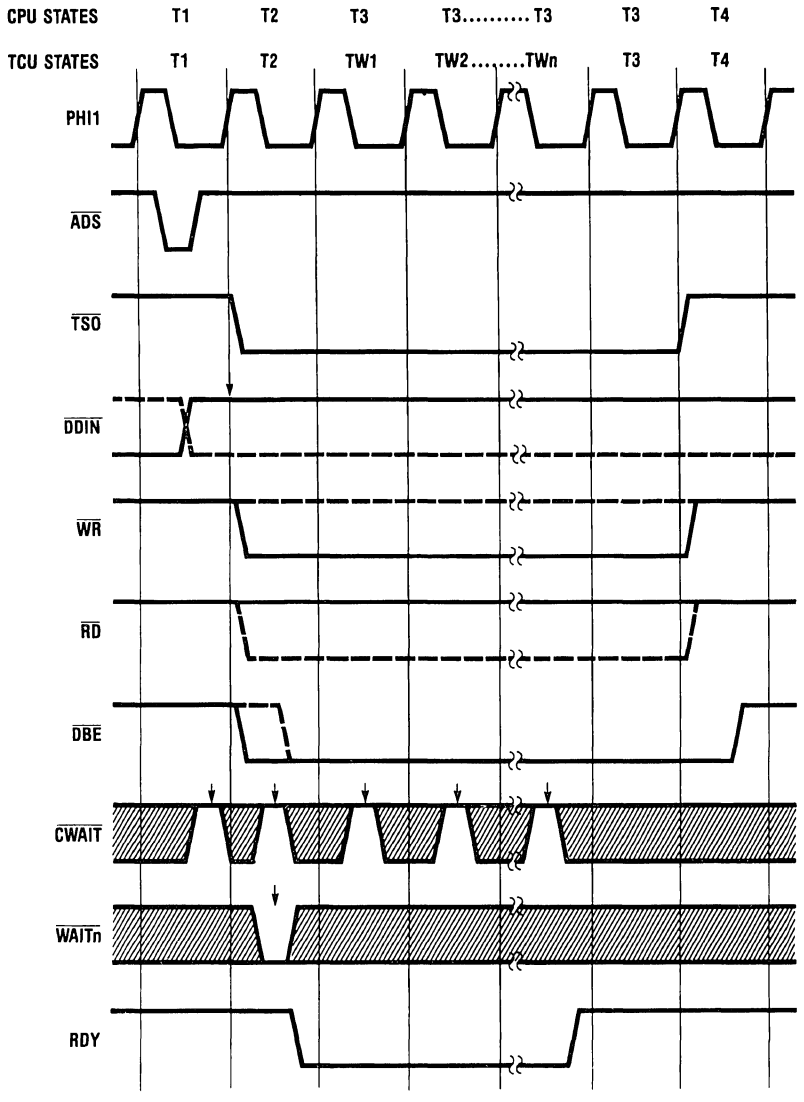

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FIGURE 1-9. Wait State Insertion Using $\overline{WAITn}$ (Fast Cycle)

1.0 Functional Description (Continued)

1.7.2 Peripheral Cycle

This cycle is entered when the $\overline{PER}$ signal line is sampled low at the beginning of T2. The TCU adds five wait states identified as TD0–TD4 into a normal bus cycle. The $\overline{RD}$ and $\overline{WR}$ signals are also re-shaped so the setup and hold times for address and data will be increased.

This may be necessary when slower peripherals must be accessed.

Figure 1-10 shows the timing diagram of a peripheral cycle.

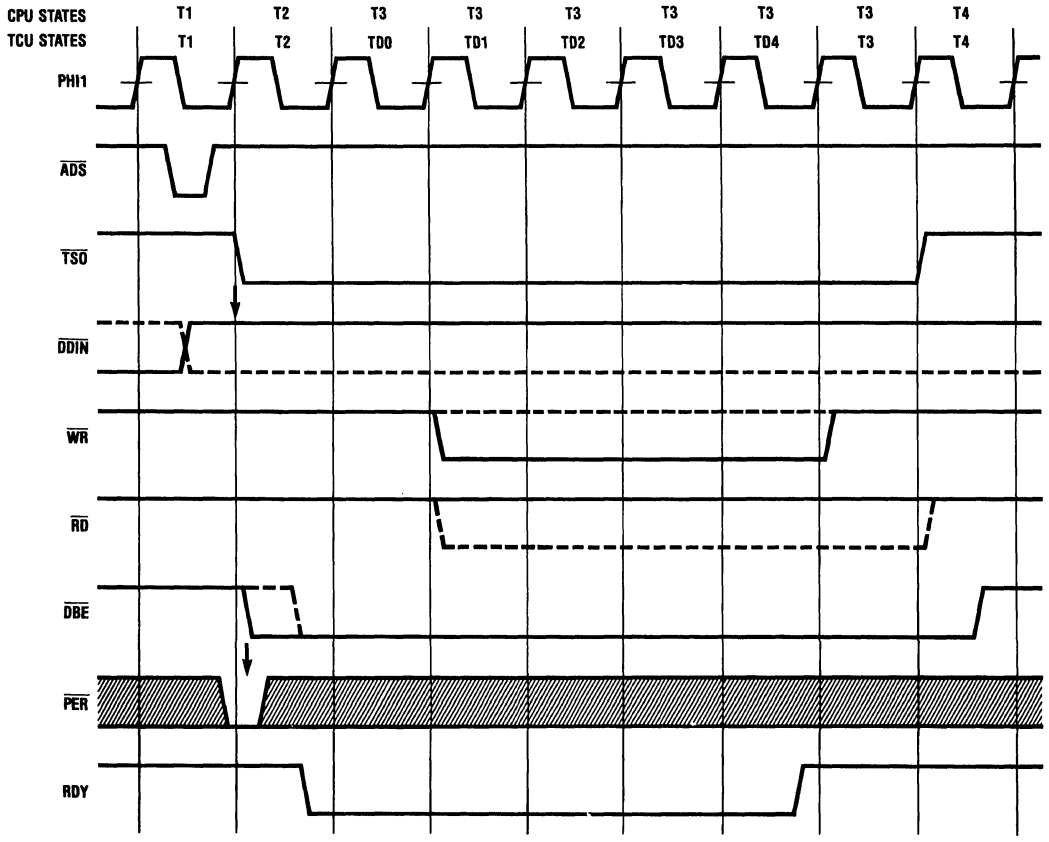

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FIGURE 1-10. Peripheral Cycle

1.0 Functional Description (Continued)

1.7.3 Cycle Hold

If the $\overline{CWAIT}$ input is sampled low at the end of state T1, the TCU will go into cycle hold mode and stay in this mode for as long as $\overline{CWAIT}$ is kept low. During this mode the control signals $\overline{RD}$, $\overline{WR}$, $\overline{TSO}$ and $\overline{DBE}$ are kept inactive; RDY is pulled low, thus causing wait states to be inserted into the bus cycle. The cycle hold feature can be used in applications involving dynamic RAMs. A timing diagram showing the cycle hold feature is shown in *Figure 1-11*.

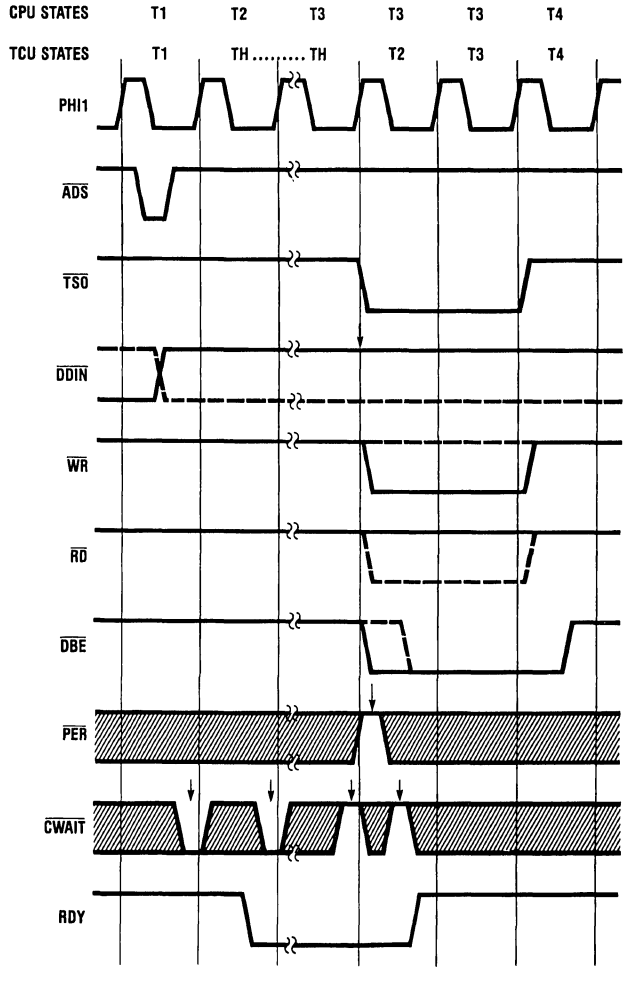

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FIGURE 1-11. Cycle Hold Timing Diagram

1.8 BUS CYCLE EXTENSION COMBINATIONS

Any combination of the TCU input signals used for extending a bus cycle can be activated at one time. The TCU will honor all of the requests according to a certain priority scheme. A cycle hold request is assigned top priority. It follows a peripheral cycle request, and then $\overline{CWAIT}$ and $\overline{WAITn}$ respectively.

If, for example, all the input signals $\overline{CWAIT}$, $\overline{PER}$ and $\overline{WAITn}$ are asserted at the beginning of the cycle, the TCU will enter the cycle hold mode. As soon as $\overline{CWAIT}$ goes high, the input signal $\overline{PER}$ is sampled to determine whether a peripheral cycle is requested.

Next, the TCU samples $\overline{CWAIT}$ again and $\overline{WAITn}$ to check whether additional wait states have to be inserted into the bus cycle. This sampling point depends on whether $\overline{PER}$ was sampled high or low. If $\overline{PER}$ was sampled high, then the sampling point will be in the middle of the TCU state T2, (*Figure 1-14*), otherwise it will occur three clock cycles later (*Figure 1-15*). *Figures 1-12* to *1-15* show the timing diagrams for different combinations of cycle extensions.

1.0 Functional Description (Continued)

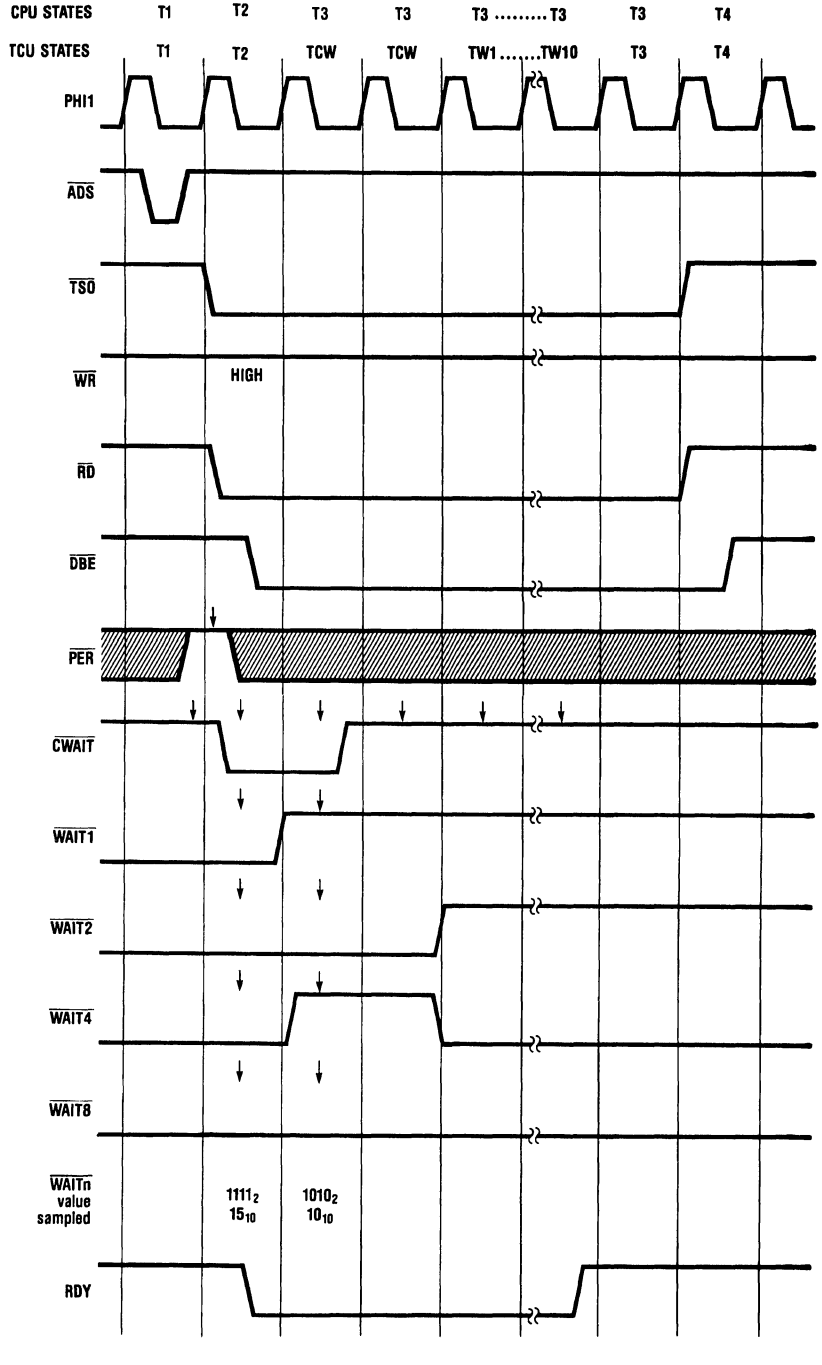

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FIGURE 1-12. Fast Cycle With 12 Wait States (2 $\overline{\text{CWAIT}}$ and $\overline{\text{WAIT10}}$) (Read Cycle)

1.0 Functional Description (Continued)

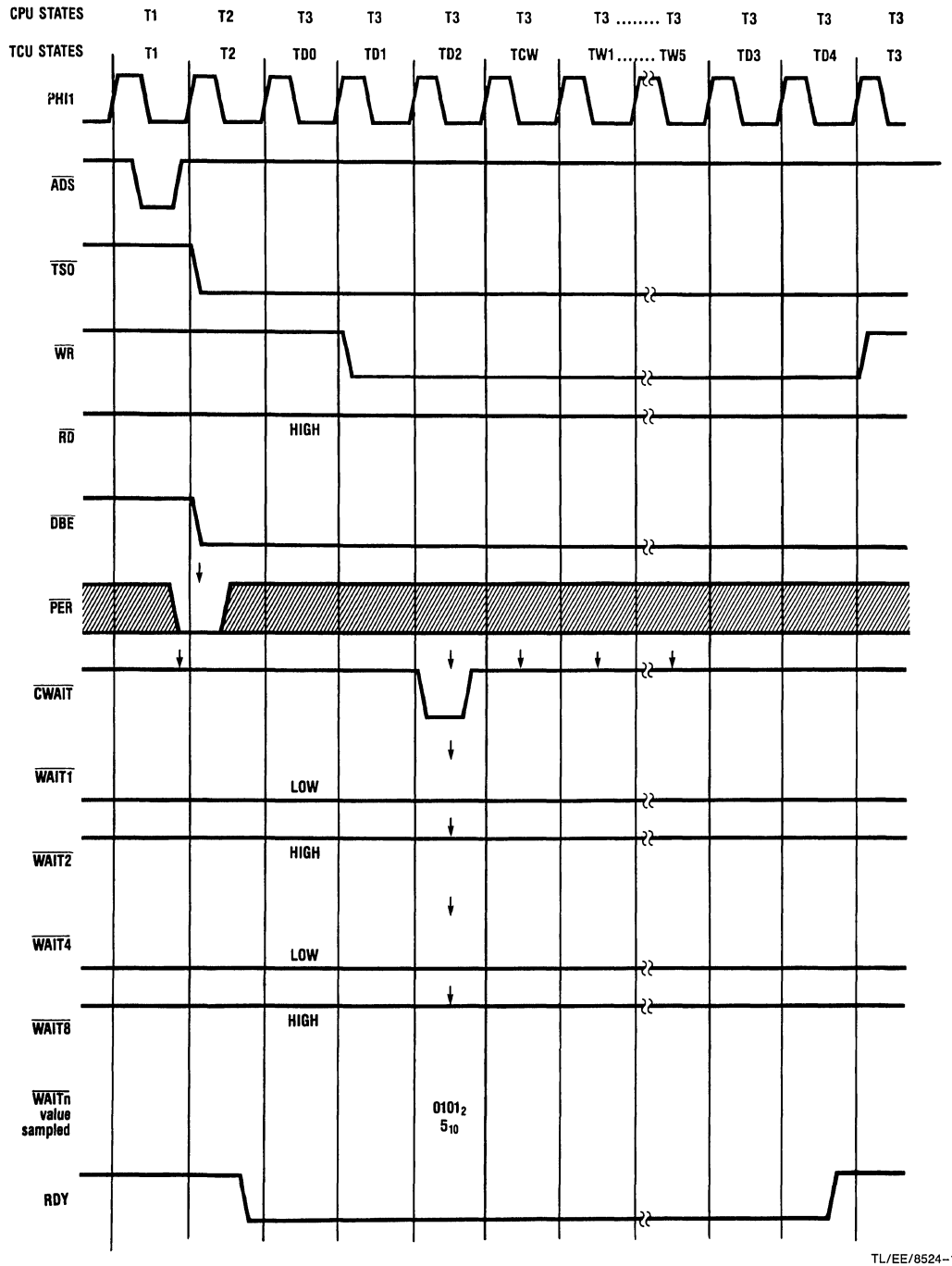

FIGURE 1-13. Peripheral Cycle with Six Wait States (1 $\overline{\text{CWAIT}}$ and $\overline{\text{WAIT5}}$) (Write Cycle)

1.0 Functional Description (Continued)

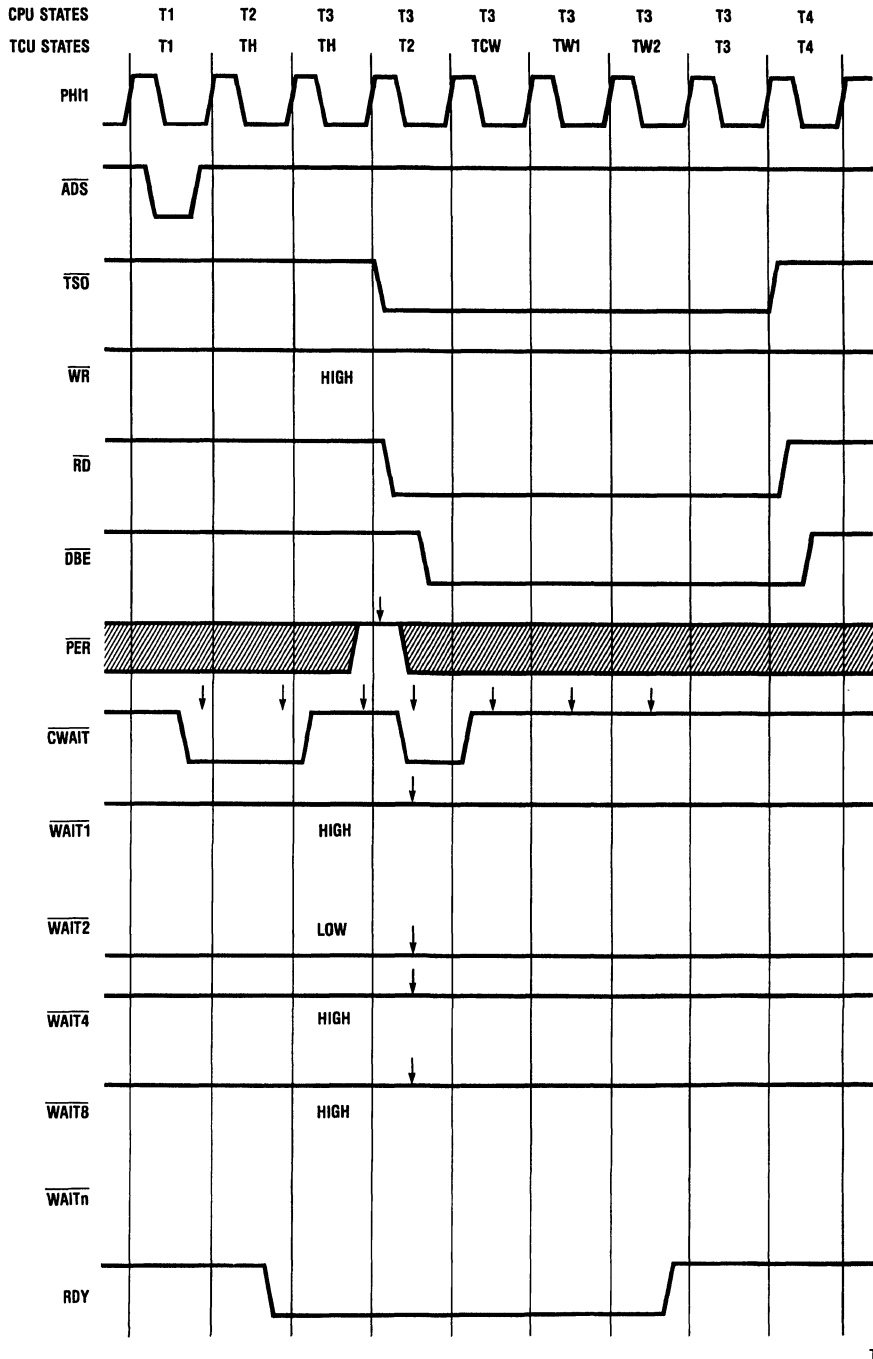

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FIGURE 1-14. Cycle Hold with Three Wait States (1 $\overline{\text{CWAIT}}$ and $\overline{\text{WAIT2}}$) (Read Cycle)

1.0 Functional Description (Continued)

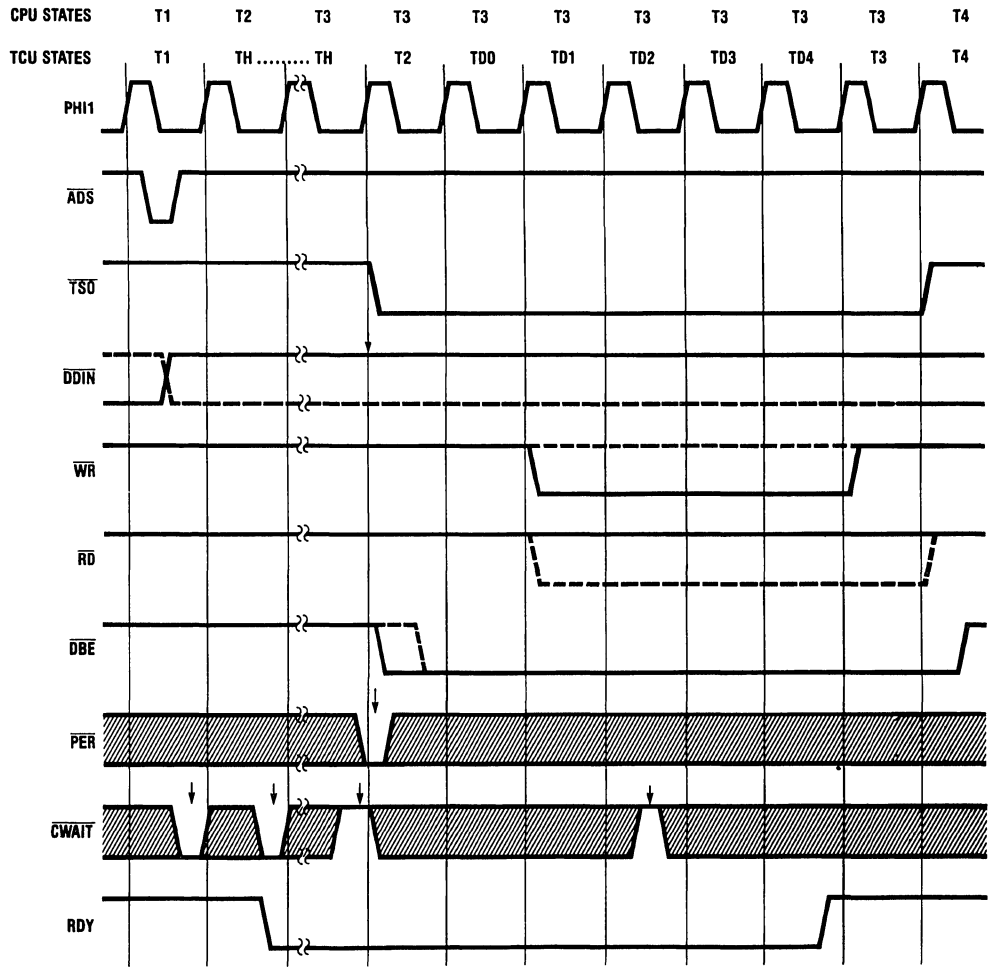

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FIGURE 1-15. Cycle Hold of a Peripheral Cycle

1.9 OVERRIDING WAITn WAIT STATES

The TCU handles the WAITn Wait States by means of an internal counter that is reloaded with the binary value corresponding to the state of the WAITn inputs each time CWAIT is sampled low, and is decremented when CWAIT is high.

This allows to either extend a bus cycle of a predefined number of clock cycles, or prematurely terminate it. To terminate a bus cycle, for example, CWAIT must be asserted for at least one clock cycle, and the WAITn inputs must be forced to their inactive state.

At least one wait state is always inserted when using this procedure as a result of CWAIT being sampled low. *Figure 1-16* shows the timing diagram of a prematurely terminated bus cycle where eleven wait states were being inserted.

1.0 Functional Description (Continued)

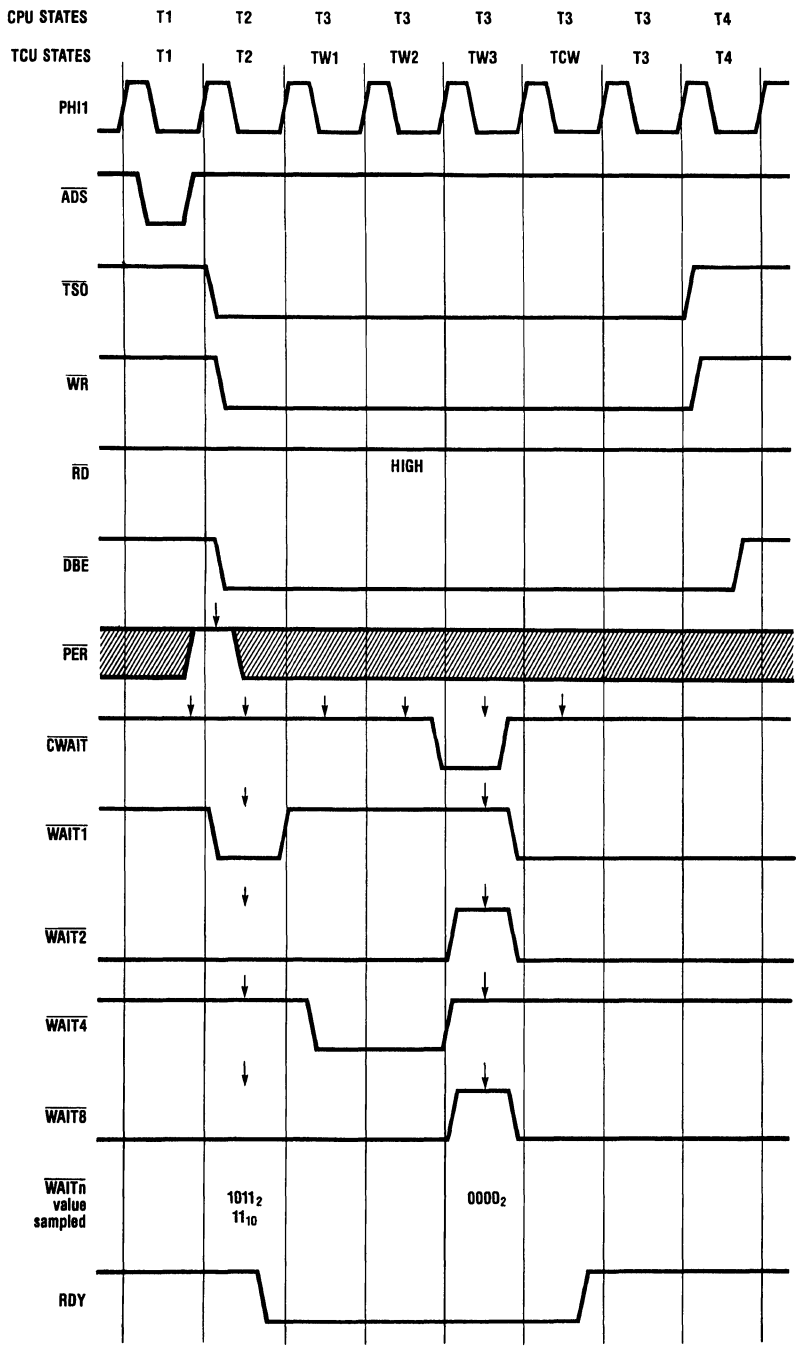

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FIGURE 1-16. Overriding $\overline{\text{WAITn}}$ Wait States (Write Cycle)

2.0 Device Specifications

2.1 PIN DESCRIPTIONS

The following is a description of all NS32C201 pins. The descriptions reference portions of the Functional Description, Section 1.

2.1.1 Supplies

Power (V_{CC}): +5V positive supply. Section 1.1.

Ground (GND): Power supply return. Section 1.1.

2.1.2 Input Signals

Reset Input ($\overline{RSTI}$): Active low. Schmitt triggered, asynchronous signal used to generate a system reset. Section 1.4.

Address Strobe ($\overline{ADS}$): Active low. Identifies the first timing state (T1) of a bus cycle.

Data Direction Input ($\overline{DDIN}$): Active low. Indicates the direction of the data transfer during a bus cycle. Implies a Read when low and a Write when high.

Note: In Rev. A of the NS32C201 this signal is CMOS compatible. In later revisions it is TTL compatible.

Read/Write Enable and Synchronization ($\overline{RWEN}$/SYNC): TRI-STATE® the $\overline{RD}$ and the $\overline{WR}$ outputs when high and enables them when low. Also used to synchronize the phase of the TCU clock signals, when two or more TCUs are used. Section 1.5.

Crystal or External Clock Source (XIN): Input from a crystal or an external clock source. Section 1.3.

Continuous Wait ($\overline{CWAIT}$): Active low. Initiates a continuous wait if sampled low in the middle of T2 during a Fast cycle, or in the middle of TD2, during a peripheral cycle. If $\overline{CWAIT}$ is low at the end of T1, it initiates a Cycle Hold. Section 1.7.1.

Four-Bit Wait State Inputs ($\overline{WAIT1}$, $\overline{WAIT2}$, $\overline{WAIT4}$ and $\overline{WAIT8}$): Active low. These inputs, (collectively called $\overline{WAITn}$), allow from zero to fifteen wait states to be specified. They are binary weighted. Section 1.7.1.

Peripheral Cycle ($\overline{PER}$): Active low. If active, causes the TCU to insert five wait states into a normal bus cycle. It also causes the Read and Write signals to be re-shaped to meet the setup and hold timing requirement of slower MOS peripherals. Section 1.7.2.

2.1.3 Output Signals

Reset Output ($\overline{RSTO}$): Active low. This signal becomes active when $\overline{RSTI}$ is low, initiating a system reset. $\overline{RSTO}$ goes high on the first rising edge of PHI1 after $\overline{RSTI}$ goes high. Section 1.4.

Read Strobe ($\overline{RD}$): (TRI-STATE) Active low. Identifies a Read cycle. It is decoded from $\overline{DDIN}$ and TRI-STATE by $\overline{RWEN}$/SYNC. Section 1.6.

Write Strobe ($\overline{WR}$): (TRI-STATE) Active low. Identifies a Write cycle. It is decoded from $\overline{DDIN}$ and TRI-STATE by $\overline{RWEN}$/SYNC. Section 1.6.

Note: $\overline{RD}$ and $\overline{WR}$ are mutually exclusive in any cycle. Hence they are never low at the same time.

Data Buffer Enable ($\overline{DBE}$): Active low. This signal is used to control the data bus buffers. It is low when the data buffers are to be enabled. Section 1.6.

Timing State Output ($\overline{TSO}$): Active low. The falling edge of $\overline{TSO}$ signals the beginning of state T2 of a bus cycle. The rising edge of $\overline{TSO}$ signals the beginning of state T4. Section 1.6.

Ready (RDY): Active high. This signal will go low and remain low as long as wait states are to be inserted in a bus cycle. It is normally connected to the RDY input of the CPU. Section 1.7.

Fast Clock (FCLK): This is a clock running at the same frequency as the crystal or the external source. Its frequency is twice that of the CPU clocks. Section 1.3.

CPU Clocks (PHI1 and PHI2): These outputs provide the Series 32000 CPU with two phase, non-overlapping clock signals. Their frequency is half that of the crystal or external source. Section 1.3.

System Clock (CTTL): This is a system version of the PHI1 clock. Hence, it operates at the CPU clock frequency. Section 1.3.

Crystal Output (XOUT): This line is used as the return path for the crystal (if used). It must be left open when an external clock source is used to drive XIN. Section 1.2.

2.0 Device Specifications (Continued)

2.2 ABSOLUTE MAXIMUM RATINGS (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltages	−0.5V to V_{CC} + 0.5V
Output Voltages	−0.5V to V_{CC} + 0.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C
Continous Power Dissipation	1W

Note: *Absolute maximum ratings indicate limits beyond which permament damage may occur. Continuous operation at these limits is not intended; operation should be limited to those conditions specified under Electrical Characteristics.*

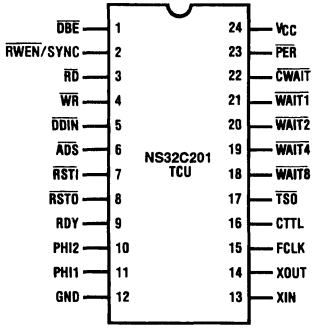
2.3 ELECTRICAL CHARACTERISTICS T_A = −40°C to +85°C, V_{CC} = 5V ±5%, GND = 0V

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IL}	Input Low Voltage	All Inputs Except $\overline{RSTI}$ & XIN			0.8	V
V_{IH}	Input High Voltage	All Inputs Except $\overline{RSTI}$ & XIN	2.0			V
V_{T+}	$\overline{RSTI}$ Rising Threshold Voltage	V_{CC} = 5.0V	2.5		3.5	V
V_{HYS}	$\overline{RSTI}$ Hysteresis Voltage	V_{CC} = 5.0V	0.8		1.9	V
V_{XL}	XIN Input Low Voltage				0.20 V_{CC}	V
V_{XH}	XIN Input High Voltage		0.80 V_{CC}			V
I_{IL}	Input Low Current	V_{IN} = 0V			−10	μA
I_{IH}	Input High Current	V_{IN} = V_{CC}			10	μA
V_{OL}	Output Low Voltage	PHI1 & PHI2, I = 1 mA All Other Outputs Except XOUT, I = 2 mA			0.10 V_{CC}	V
V_{OH}	Output High Voltage	All Outputs Except XOUT, I = −1 mA	0.90 V_{CC}			V
I_L	Leakage Current on $\overline{RD}/\overline{WR}$	0.4V ≤ V_{IN} ≤ V_{CC}	−20		+20	μA
I_{CC}	Supply Current	f_{xin} = 20 MHz		100	120	mA

Note 1: All typical values are for V_{CC} = 5V and T_A = 25°C.

Connection Diagram

Dual-In-Line Package



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Top View

Order Number NS32C201D or NS32C201N
See NS Package Number D24C or N24A

FIGURE 2.1

2.0 Device Specifications (Continued)

2.4 SWITCHING CHARACTERISTICS

2.4.1 Definitions

All the timing specifications given in this section refer to 2.0V on the rising or falling edges of the clock phases PHI1 and PHI2; to 15% or 85% of V_{CC} on all the CMOS output signals, and to 0.8V or 2.0V on all the TTL input signals, unless specifically stated otherwise.

2.4.2 Output Loading

Capacitive loading on output pins for the NS32C201.

RDY, $\overline{DBE}$, $\overline{TSO}$ ..... 50 pF
$\overline{RD}$, $\overline{WR}$ ..... 75 pF
CTTL ..... 50 ÷ 100 pF
FCLK ..... 100 pF
PHI1, PHI2 ..... 170 pF

ABBREVIATIONS

L.E.—Leading Edge
T.E.—Trailing Edge
R.E.—Rising Edge
F.E.—Falling Edge

2.4.3 Timing Tables

Symbol	Figure	Description	Reference/Conditions	NS32C201-10		NS32C201-15		Units
				Min	Max	Min	Max	
CLOCK-SIGNALS (XIN, FCLK, PHI1 & PHI2) TIMING								
t_{Cp}	2.2	Clock Period	PHI1 R.E. to Next PHI1 R.E.	100		66		ns
t_{CLh}	2.2	Clock High Time	At 90% V_{CC} on PHI1 (Both Edges)	0.5 t_{Cp} −15 ns	0.5 t_{Cp} −7 ns	0.5 t_{Cp} −10 ns	0.5 t_{Cp} −3 ns	
t_{CLl}	2.2	Clock Low Time	At 15% V_{CC} on PHI1	0.5 t_{Cp} −5 ns	0.5 t_{Cp} +10 ns	0.5 t_{Cp} −5 ns	0.5t_{CP} +6 ns	
$t_{CLw(1,2)}$	2.2	Clock Pulse Width	At 2.0V on PHI1, PHI2 (Both Edges)	0.5 t_{CP} −10 ns	0.5 t_{CP} −4 ns	0.5 t_{CP} −6 ns	0.5 t_{CP} −4 ns	
t_{CLwas}		PHI1, PHI2 Asymmetry (t_{CLw} (1) − t_{CLw} (2))	At 2.0V on PHI1, PHI2	−5	5	−3	3	ns
t_{CLR}	2.2	Clock Rise Time	15% to 90% V_{CC} on PHI1 R.E.		8		6	ns
t_{CLF}	2.2	Clock Fall Time	90% to 15% V_{CC} on PHI1 F.E.		8		6	ns
$t_{nOVL\,(1,2)}$	2.2	Clock Non-Overlap Time	At 15% V_{CC} on PHI1, PHI2	−2	+2	−2	+2	ns
t_{nOVLas}		Non-Overlap Asymmetry (t_{nOVL} (1) − t_{nOVL} (2))	At 15% V_{CC} on PHI1, PHI2	−4	4	−3	3	ns
t_{Xh}	2.2	XIN High Time (External Input)	At 80% V_{CC} on XIN (Both Edges)	16		10		ns
t_{Xl}	2.2	XIN Low Time (External Input)	At 15% V_{CC} on XIN (Both Edges)	16		10		ns
t_{XFr}	2.2	XIN to FCLK R.E. Delay	80% V_{CC} on XIN R.E. to FCLK R.E.	6	29	6	25	ns
t_{XFf}	2.2	XIN to FCLK F.E. Delay	15% V_{CC} on XIN F.E. to FCLK F.E.	6	29	6	25	ns
t_{XCr}	2.2	XIN to CTTL R.E. Delay	80% V_{CC} on XIN R.E. to CTTL R.E.	6	34	6	25	ns
t_{XPr}	2.2	XIN to PHI1 R.E. Delay	80% V_{CC} on XIN R.E. to PHI1 R.E.	6	32	6	25	ns
t_{FCr}	2.2	FCLK to CTTL R.E. Delay	FCLK R.E. to CTTL R.E.	0	6	0	6	ns
t_{FCf}	2.2	FCLK to CTTL F.E. Delay	FCLK R.E. to CTTL F.E.	−3	4	−3	4	ns
t_{FPr}	2.3	FCLK to PHI1 R.E. Delay	FCLK R.E. to PHI1 R.E.	−3	4	−3	4	ns
t_{FPf}	2.3	FCLK to PHI1 F.E. Delay	FCLK R.E. to PHI1 F.E.	−5	2	−5	2	ns
t_{Fw}	2.3	FCLK Pulse Width with Crystal	At 50% V_{CC} on FCLK (Both Edges)	0.25 t_{Cp} −5 ns	0.25 t_{Cp} +5 ns	0.25 t_{Cp} −5 ns	0.25 t_{Cp} +5 ns	
t_{PCf}	2.3	PHI2 R.E.to CTTL F.E. Delay	PHI2 R.E. to CTTL F.E.	−3	4	−3	3	ns
t_{CTw}	2.3	CTTL Pulse Width	At 50% V_{CC} on CTTL (Both Edges)	0.5 t_{Cp} −7 ns	0.5 t_{Cp} +1 ns	0.5 t_{Cp} −5 ns	0.5 t_{Cp} +1 ns	

Note 1: t_{XCr}, t_{FCr}, t_{FCf}, t_{PCf}, t_{CTh} are measured with 100 pF load on CTTL.

Note 2: PHI1 and PHI2 are interchangeable for the following parameters: t_{Cp}, t_{CLh}, t_{CLl}, t_{CLw}, t_{CLR}, t_{CLF}, t_{nOVL}, t_{XPr}, t_{FPr}, t_{FPf}.

2.0 Device Specifications (Continued)

2.4.3 Timing Tables (Continued)

Symbol	Figure	Description	Reference/Conditions	NS32C201-10		NS32C201-15		Units
				Min	Max	Min	Max	
CTTL TIMING (CL = 50 pF)								
t_{PCr}	2.3	PHI1 to CTTL R.E. Delay	PHI1 R.E. to CTTL R.E.	−2	5	−2	3	ns
t_{CTR}	2.3	CTTL Rise Time	10% to 90% V_{CC} on CTTL R.E.		7		6	ns
t_{CTF}	2.3	CTTL Fall Time	90% to 10% V_{CC} on CTTL F.E.		7		6	ns
CTTL TIMING (CL = 100 pF)								
t_{PCr}	2.3	PHI1 to CTTL R.E. Delay	PHI1 R.E. to CTTL R.E.	−2	6	−2	4	ns
t_{CTR}	2.3	CTTL Rise Time	10% to 90% V_{CC} on CTTL R.E.		8		7	ns
t_{CTF}	2.3	CTTL Fall Time	90% to 10% V_{CC} on CTTL F.E.		8		7	ns
CONTROL INPUTS ($\overline{RST1}$, $\overline{ADS}$, $\overline{DDIN}$) TIMING								
t_{RSTs}	2.4	$\overline{RSTI}$ Setup Time	Before PHI1 R.E.	20		15		
t_{ADs}	2.4	$\overline{ADS}$ Setup Time	Before PHI1 R.E.	25		20		ns
t_{ADw}	2.4	$\overline{ADS}$ Pulse Width	$\overline{ADS}$ L.E. to $\overline{ADS}$ T.E.	25		20		ns
t_{DDs}	2.4	$\overline{DDIN}$ Setup Time	Before PHI1 R.E.	15		13		ns
CONTROL OUTPUTS ($\overline{RSTO}$, $\overline{TSO}$, $\overline{RD}$, $\overline{WR}$, $\overline{DBE}$ & $\overline{RWEN}$/SYNC) TIMING								
t_{RSTr}	2.4	$\overline{RSTO}$ R.E. Delay	After PHI1 R.E.		21		10	ns
t_{Tf}	2.5	$\overline{TSO}$ L.E. Delay	After PHI1 R.E.		12		8	ns
t_{Tr}	2.5	$\overline{TSO}$ T.E. Delay	After PHI1 R.E.	3	18	3	10	ns
$t_{RWf(F)}$	2.5	$\overline{RD}$/$\overline{WR}$ L.E. Delay (Fast Cycle)	After PHI1 R.E.		30		21	ns
$t_{RWf(S)}$	2.6	$\overline{RD}$/$\overline{WR}$ L.E. Delay (Peripheral Cycle)	After PHI1 R.E.		25		15	ns
t_{RWr}	2.5/6	$\overline{RD}$/$\overline{WR}$ T.E. Delay	After PHI1 R.E.	3	20	3	15	ns
$t_{DBf(W)}$	2.5/6	$\overline{DBE}$ L.E. Delay (Write Cycle)	After PHI1 R.E.		25		15	ns
$t_{DBf(R)}$	2.5/6	$\overline{DBE}$ L.E. Delay (Read Cycle)	After PHI2 R.E.		20		11	ns
t_{DBr}	2.5/6	$\overline{DBE}$ T.E. Delay	After PHI2 R.E.		20		15	ns
t_{pLZ}	2.7	$\overline{RD}$,$\overline{WR}$ Low Level to TRI-STATE	After $\overline{RWEN}$/SYNC R.E.		25		20	ns
t_{pHZ}	2.7	$\overline{RD}$,$\overline{WR}$ High Level to TRI-STATE	After $\overline{RWEN}$/SYNC R.E.		20		15	ns
t_{pZL}	2.7	$\overline{RD}$,$\overline{WR}$ TRI-STATE to Low Level	After $\overline{RWEN}$/SYNC F.E.		25		18	ns
t_{pZH}	2.7	$\overline{RD}$,$\overline{WR}$ TRI-STATE to High Level	After $\overline{RWEN}$/SYNC F.E.		25		18	ns
WAIT STATES & CYCLE HOLD ($\overline{CWAIT}$, $\overline{WAITn}$, $\overline{PER}$ & $\overline{RDY}$) TIMING								
$t_{CWs(H)}$	2.8	$\overline{CWAIT}$ Setup Time (Cycle Hold)	Before PHI1 R.E.	30		20		ns
$t_{CWh(H)}$	2.8	$\overline{CWAIT}$ Hold Time (Cycle Hold)	After PHI1 R.E.	0		0		ns
$t_{CWs(W)}$	2.8/9	$\overline{CWAIT}$ Setup Time (Wait States)	Before PHI2 R.E.	10		6		ns
$t_{CWh(W)}$	2.9	$\overline{CWAIT}$ Hold Time (Wait States)	After PHI2 R.E.	20		10		ns
t_{Ws}	2.9	$\overline{WAITn}$ Setup Time	Before PHI2 R.E.	7		6		ns
t_{Wh}	2.9	$\overline{WAITn}$ Hold Time	After PHI2 R.E.	15		10		ns
t_{Ps}	2.10	$\overline{PER}$ Setup Time	Before PHI1 R.E.	7		5		ns
t_{Ph}	2.10	$\overline{PER}$ Hold Time	After PHI1 R.E.	30		20		ns
t_{Rd}	2.8/9/10	$\overline{RDY}$ Delay	After PHI2 R.E.		25		12	ns
SYNCHRONIZATION (SYNC) TIMING								
t_{Sys}	2.11	SYNC Setup Time	Before XIN R.E.	6		6		ns
t_{Syh}	2.11	SYNC Hold Time	After XIN R.E.	5		5		ns
t_{CS}	2.11	CTTL/SYNC Inversion Delay	CTTL (master) to $\overline{RWEN}$/SYNC (slave)		10		7	ns

2.0 Device Specifications (Continued)

2.4.4 Timing Diagrams

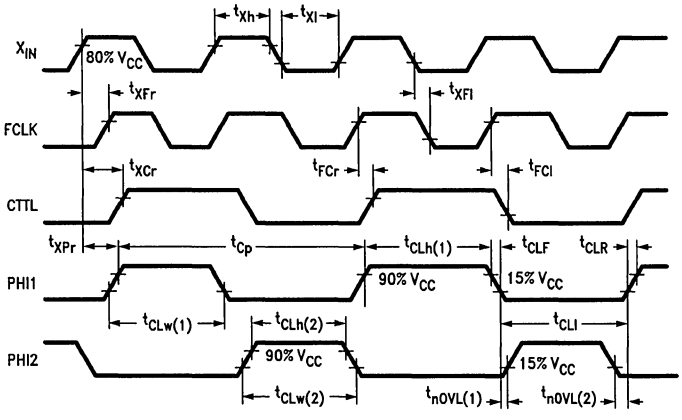

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FIGURE 2-2. Clock Signals (a)

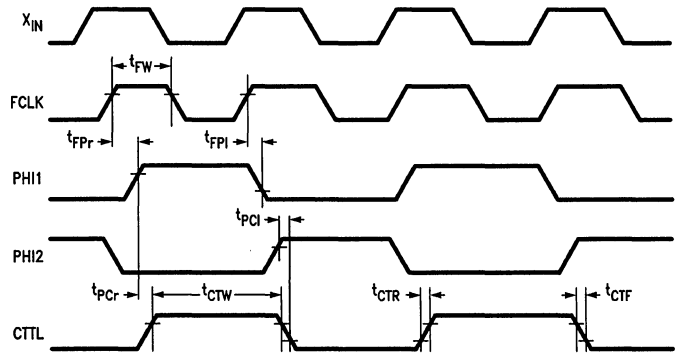

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FIGURE 2-3. Clock Signals (b)

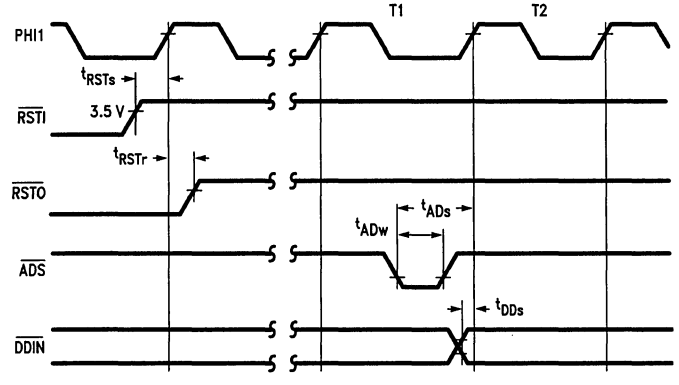

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FIGURE 2-4. Control Inputs

4

2.0 Device Specifications (Continued)

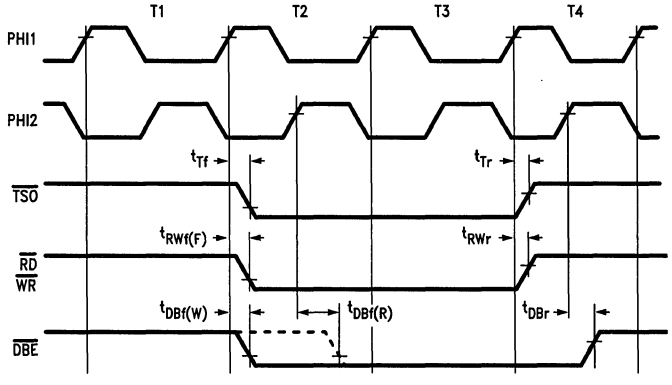

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FIGURE 2-5. Control Outputs (Fast Cycle)

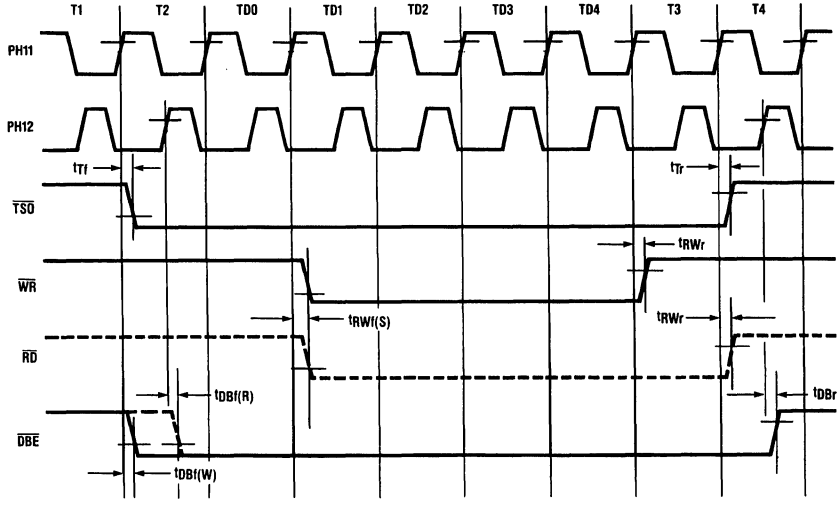

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FIGURE 2-6. Control Outputs (Peripheral Cycle)

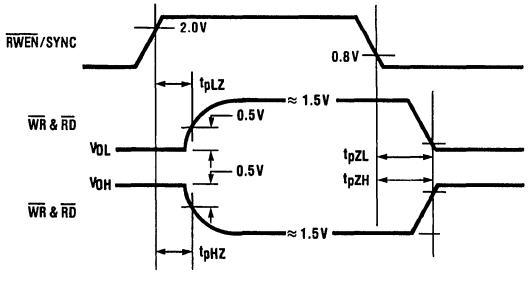

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FIGURE 2-7. Control Outputs (TRI-STATE Timing)

2.0 Device Specifications (Continued)

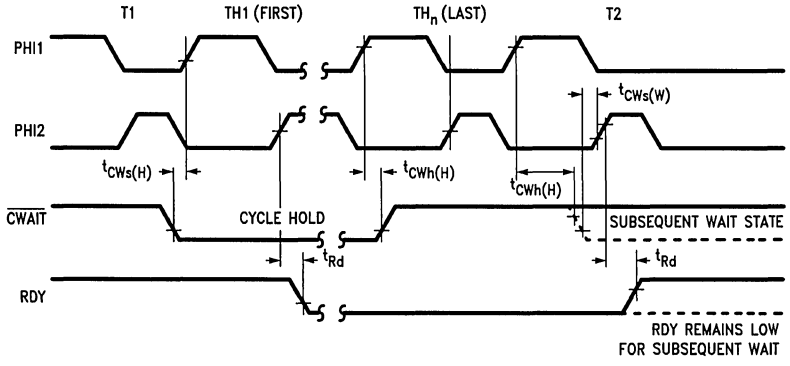

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FIGURE 2-8. Cycle Hold

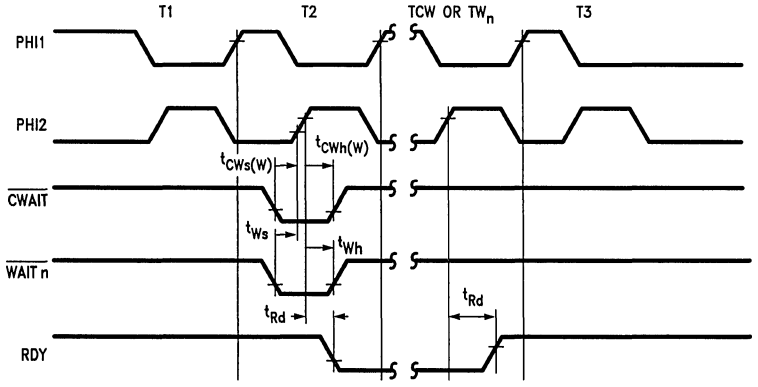

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FIGURE 2-9. Wait State (Fast Cycle)

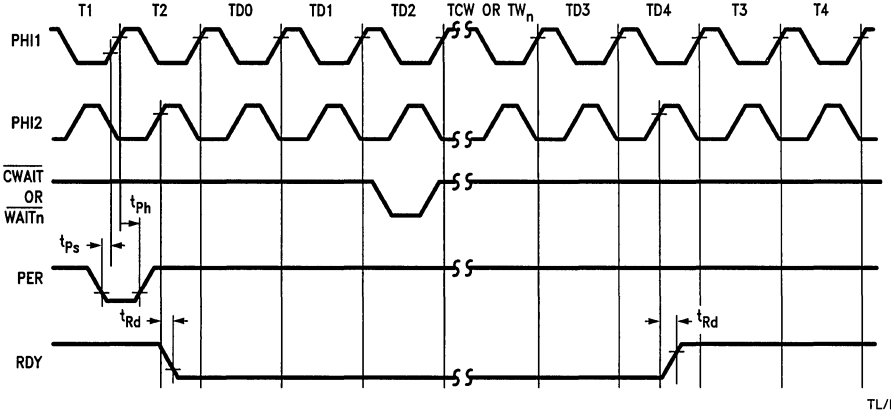

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FIGURE 2-10. Wait State (Peripheral Cycle)

4

2.0 Device Specifications (Continued)

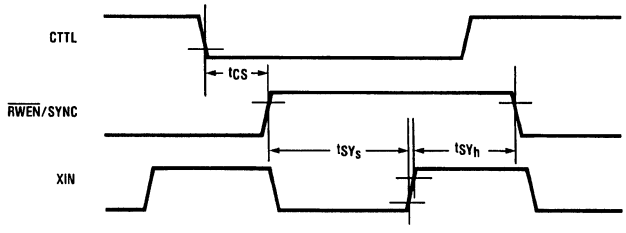

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FIGURE 2-11. Synchronization Timing

National Semiconductor

NS32202-10 Interrupt Control Unit

General Description

The NS32202 Interrupt Control Unit (ICU) is the interrupt controller for the Series 32000® microprocessor family. It is a support circuit that minimizes the software and real-time overhead required to handle multi-level, prioritized interrupts. A single NS32202 manages up to 16 interrupt sources, resolves interrupt priorities, and supplies a single-byte interrupt vector to the CPU.

The NS32202 can operate in either of two data bus modes: 16-bit or 8-bit. In the 16-bit mode, eight hardware and eight software interrupt positions are available. In the 8-bit mode, 16 hardware interrupt positions are available, 8 of which can be used as software interrupts. In this mode, up to 16 additional ICUs may be cascaded to handle a maximum of 256 interrupts.

Two 16-bit counters, which may be concatenated under program control into a single 32-bit counter, are also available for real-time applications.

Features

- 16 maskable interrupt sources, cascadable to 256
- Programmable 8- or 16-bit data bus mode
- Edge or level triggering for each hardware interrupt with individually selectable polarities
- 8 software interrupts
- Fixed or rotating priority modes
- Two 16-bit, DC to 10 MHz counters, that may be concatenated into a single 32-bit counter
- Optional 8-bit I/O port available in 8-bit data bus mode
- High-speed XMOS™ technology
- Single, +5V supply
- 40-pin, dual in-line package

Basic System Configuration

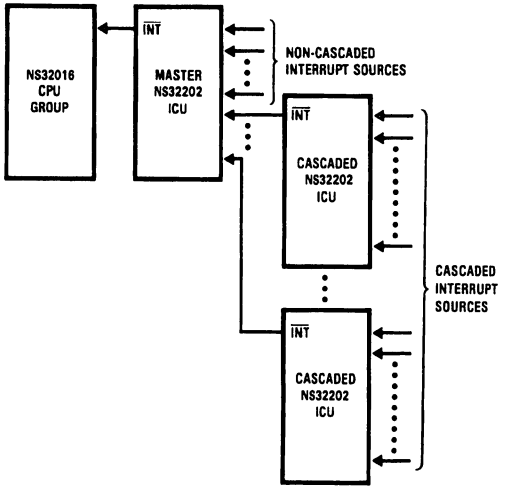

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Table of Contents

List of Illustrations

1.0 Product Introduction

The NS32202 ICU functions as an overall manager in an interrupt-oriented system environment. Its many features and options permit the design of sophisticated interrupt systems.

Figure 1–1 shows the internal organization of the NS32202. As shown, the NS32202 is divided into five functional blocks. These are described in the following paragraphs:

1.1 I/O BUFFERS AND LATCHES

The I/O Buffers and Latches block is the interface with the system data bus. It contains bidirectional buffers for the data I/O pins. It also contains registers and logic circuits that control the operation of pins G0/IR0, . . . ,G7/IR14 when the ICU is in the 8-bit bus mode.

1.2 READ/WRITE LOGIC AND DECODERS

The Read/Write Logic and Decoders manage all internal and external data transfers for the ICU. These include Data, Control, and Status Transfers. This circuit accepts inputs from the CPU address and control buses. In turn, it issues commands to access the internal registers of the ICU.

1.3 TIMING AND CONTROL

The Timing and Control Block contains status elements that select the ICU operating mode. It also contains state machines that generate all the necessary sequencing and control signals.

1.4 PRIORITY CONTROL

The Priority Control Block contains 16 units, one for each interrupt position. These units provide the following functions.

- Sensing the various forms of hardware interrupt signals e.g. level (high/low) or edge (rising/falling)
- Resolving priorities and generating an interrupt request to the CPU
- Handling cascaded arrangements
- Enabling software interrupts
- Providing for an automatic return from interrupt
- Enabling the assignment of any interrupt position to the internal counters
- Providing for rearrangement of priorities by assigning the first priority to any interrupt position
- Enabling automatic rotation of priorities

1.5 COUNTERS

This block contains two 16-bit counters, called the H-counter and the L-counter. These are down counters that count from an initial value to zero. Both counters have a 16-bit register (designated HCSV and LCSV) for loading their restarting values. They also have registers containing the current count values (HCCV and LCCV). Both sets of registers are fully described in Section 3.

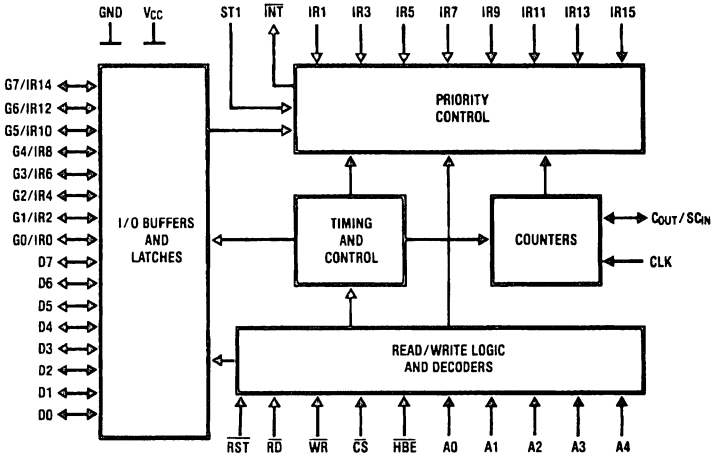

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FIGURE 1–1. NS32202 ICU Block Diagram

1.0 Product Introduction (Continued)

The counters are under program control and can be used to generate interrupts. When the count reaches zero, either counter can generate an interrupt request to any of the 16 interrupt positions. The counter then reloads the start value from the appropriate registers and resumes counting. *Figure 1–2* shows typical counter output signals available from the NS32202.

The maximum input clock frequency is 2.5 MHz.

A divide-by-four prescaler is also provided. When the prescaler is used, the input clock frequency can be up to 10 MHz.

When intervals longer than provided by a 16-bit counter are needed, the L- and H-counters can be concatenated to form a 32-bit counter. In this case, both counters are controlled by the H-counter control bits. Refer to the discussion of the Counter Control Register in Section 3 for additional information. *Figure 1-3* summarizes counter read/write operations.

2.0 Functional Description

2.1 RESET

The ICU is reset when a logic low signal is present on the $\overline{RST}$ pin. At reset, most internal ICU registers are affected, and the ICU becomes inactive.

2.2 INITIALIZATION

After reset, the CPU must initialize the NS32202 to establish its configuration. Proper initialization requires knowledge of the ICU register's formats. Therefore, a flowchart of a recommended initialization sequence is shown in (*Figure 3–3*) after the discussion of the ICU registers.

The operation sequence shown in *Figure 3–3* ensures that all counter output pins remain inactive until the counters are completely initialized.

2.3 VECTORED INTERRUPT HANDLING

For details on the operation of the vectored interrupt mode for a particular Series 32000 CPU, refer to the data sheet for

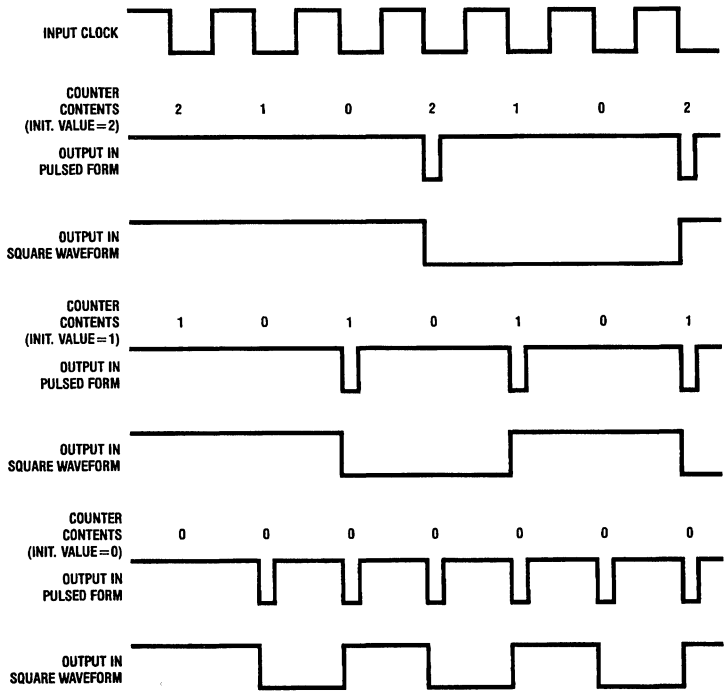
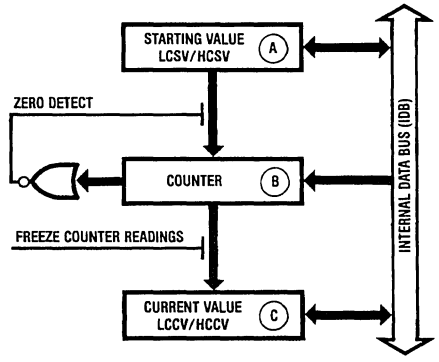


FIGURE 1–2. Counter Output Signals in Pulsed Form and Square Waveform for Three Different Initial Values

2.0 Functional Description (Continued)

that CPU. In this discussion, it is assumed that the NS32202 is working with a CPU in the vectored interrupt mode. Several ICU applications are discussed, including non-cascaded and cascaded operation. *Figures 2–1, 2–2,* and *2–3* show typical configurations of the ICU used with the NS32016 CPU.

A peripheral device issues an interrupt request by sending the proper signal to one of the NS32202 interrupt inputs. If the interrupt input is not masked, the ICU activates its Interrupt Output ($\overline{INT}$) pin and generates an interrupt vector byte. The interrupt vector byte identifies the interrupt source in its four least significant bits. When the CPU detects a low level on its Interrupt Input pin, it performs one or two interrupt acknowledge cycles depending on whether the interrupt request is from the master ICU or a cascaded ICU. *Figure 2–4* shows a flowchart of a typical CPU Interrupt Acknowledge sequence.



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BASIC OPERATIONS:

WRITING TO LCSV/HCSV	[A] ← (IDB)
READING LCSV/HCSV	[A] → (IDB)
WRITING TO LCCV/HCCV	[B] ← (IDB)
(only possible when counters are halted)	[C] ← (IDB)
READING LCCV/HCCV	[C] → (IDB)
(only possible when counter readings are frozen)	
COUNTER COUNTS AND READINGS ARE NOT FROZEN	[C] ← [B]
COUNTER RELOADS STARTING VALUE	[B] ← [A]
(occurs on the clock cycle following the one in which it reaches zero)	

FIGURE 1–3. Counter Configuration and Basic Operations

2.0 Functional Description (Continued)

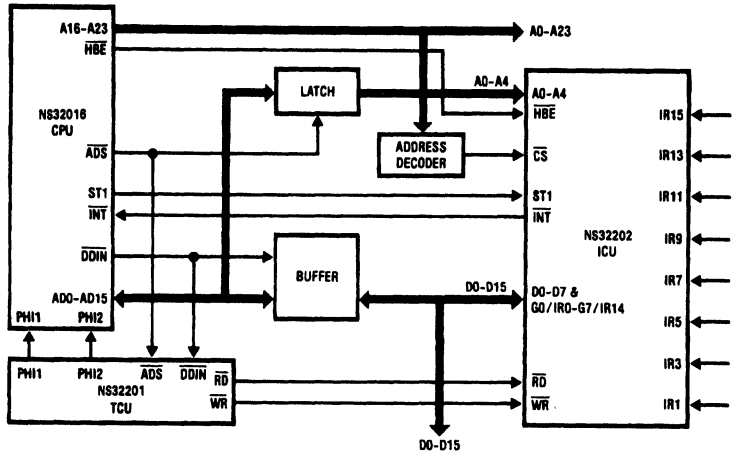

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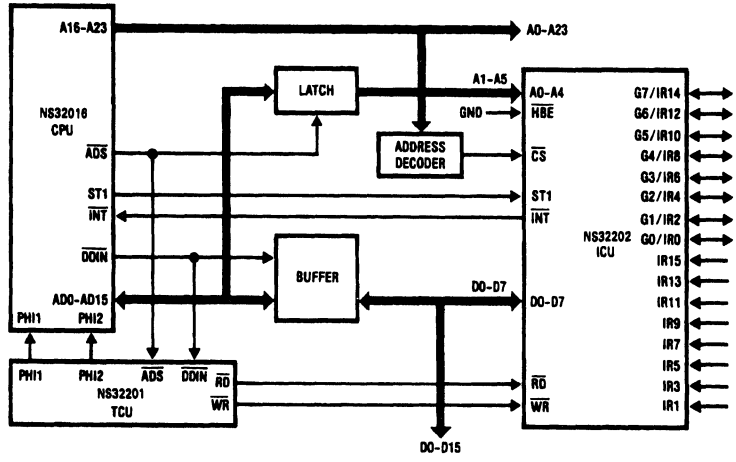
FIGURE 2-1. Interrupt Control Unit Connections in 16-Bit Bus Mode



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NOTE: In the 8-Bit Bus Mode the Master ICU Registers appear at even addresses (A0 = 0) since the ICU communicates with the least significant byte of the CPU data bus.

FIGURE 2-2. Interrupt Control Unit Connections in 8-Bit Bus Mode

2.0 Functional Description (Continued)

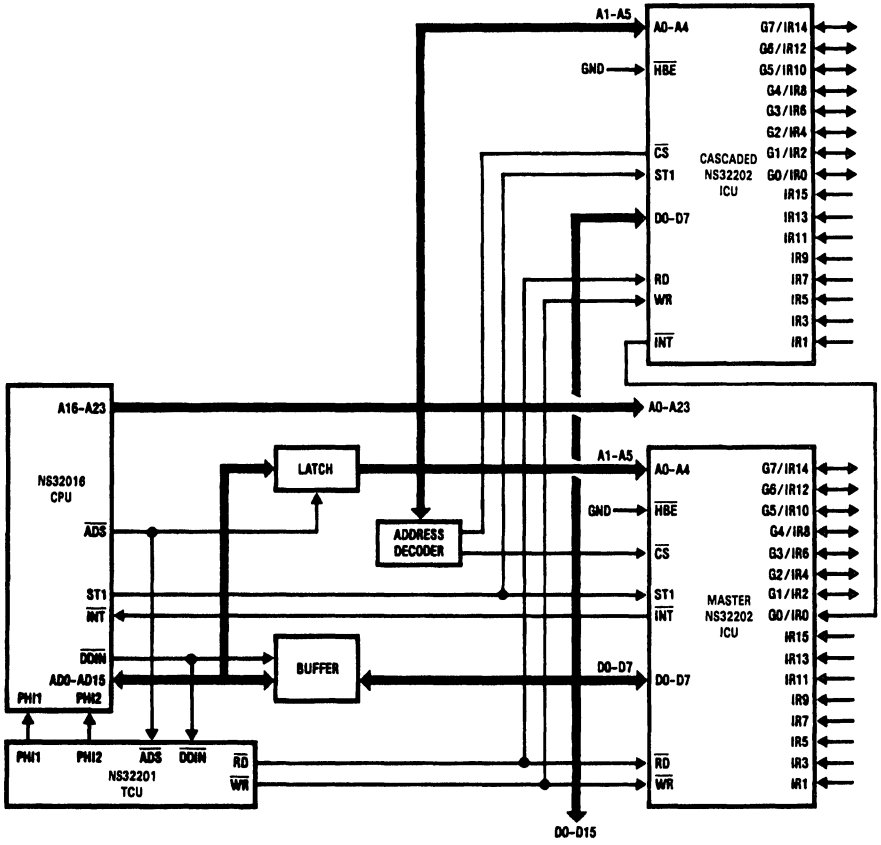

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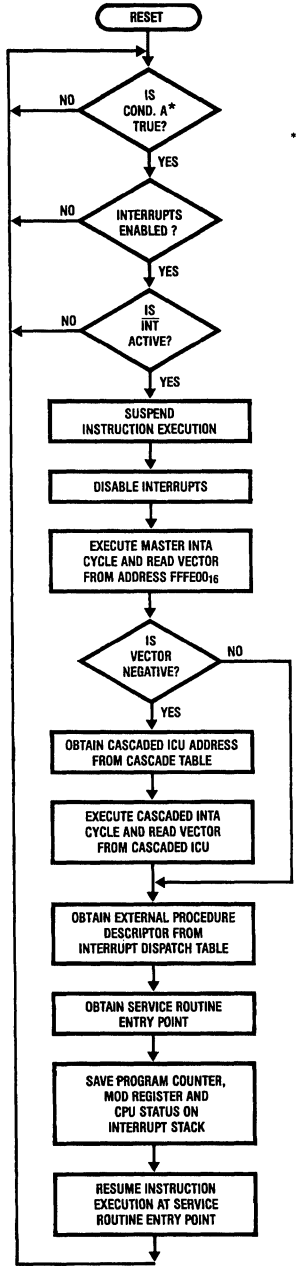
FIGURE 2-3. Cascaded Interrupt Control Unit Connections in 8-Bit Bus Mode

2.0 Functional Description (Continued)



* Cond. A is true if current instruction is terminated or an interruptible point in a string instruction is reached.

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FIGURE 2–4. CPU Interrupt Acknowledge Sequence

2.0 Functional Description (Continued)

In general, vectored interrupts are serviced by interrupt routines stored in system memory. The Dispatch Table stores up to 256 external procedure descriptors for the various service procedures. The CPU INTBASE register points to the top of the Dispatch Table. *Figure 2-5* shows the layout of the Dispatch Table. This figure also shows the layout of the Cascade Table, which is discussed with ICU cascaded operation.

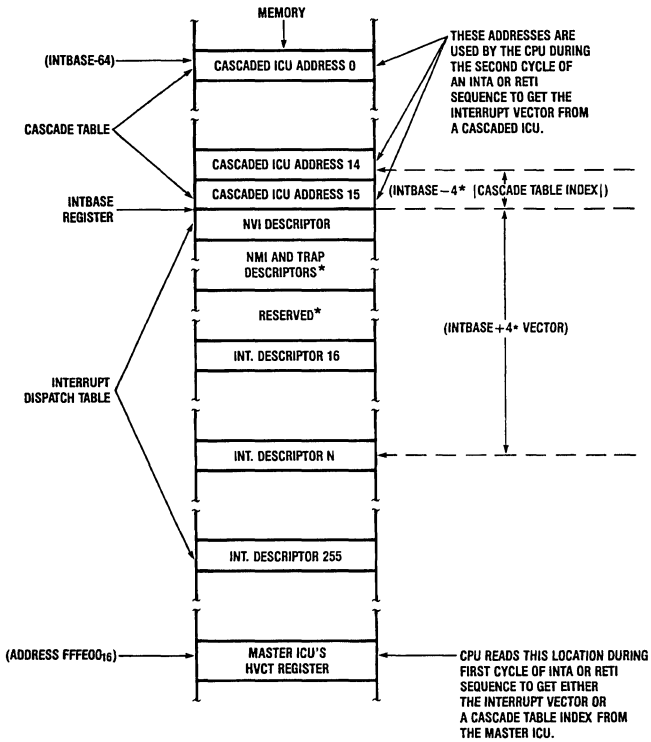
2.3.1 Non-Cascaded Operation. Whenever an interrupt request from a peripheral device is issued directly to the master ICU, a non-cascaded interrupt request to the CPU results. In a system using a single NS32202, up to 16 interrupt requests can be prioritized. Upon receipt of an interrupt request on the $\overline{INT}$ pin, the CPU performs a Master Interrupt-Acknowledge bus cycle, reading a vector byte from address $FFFE00_{16}$. This vector is then used as an index into the dispatch table in order to find the External Procedure Descriptor for the proper interrupt service procedure. The service procedure eventually returns via the Return-from-Interrupt (RET) instruction, which performs a Return-from-Interrupt bus cycle, informing the ICU that it may re-prioritize any interrupt requests still pending. *Figure 2-6* shows a typical CPU RETI sequence. In a system with only one ICU, the vectors provided must be in the range of 0 through 127; this can be ensured by writing 0XXXXXXX into the SVCT register. By providing a negative vector value, the master ICU flags the interrupt source as a cascaded ICU (see below).

2.3.2 Cascaded Operation. In cascaded operation, one or more of the interrupt inputs of the master ICU are connected to the Interrupt Output pin of one or more cascaded ICUs. Up to 16 cascaded ICUs may be used, giving a system total of 256 interrupts.

Note: The number of cascaded ICUs is practically limited to 15 because the Dispatch Table for the NS32016 CPU is constructed with entries 1 through 15 either used for NMI and Trap descriptors, or reserved for future use. Interrupt position 0 of the master ICU should not be cascaded, so it can be vectored through Dispatch Table entry 0, reserved for non-vectored interrupts. In this case, the non-vectored interrupt entry (entry 0) is also available for vectored interrupt operation, since the CPU is operating in the vectored interrupt mode.

The address of the master ICU should be $FFFE00_{16}$. (*) Cascaded ICUs can be located at any system address. A list of cascaded ICU addresses is maintained in the Cascade Table as a series of sixteen 32-bit entries.

(*)Note: The CPU status corresponding to both, master interrupt acknowledge and return from interrupt bus cycles, as well as address bit A8, could be used to generate the chip select ($\overline{CS}$) signal for accessing the master ICU during one of the above cycles. In this case the master ICU can reside at any system address. The only limitation is that the least significant 5 or 6 address bits (6 in the 8-bit bus mode) must be zero. The address bit A8 must be decoded to prevent an NMI bus cycle from reading the hardware vector register of the ICU. This could happen, since the NS32016 CPU performs a dummy read cycle from address $FFFF00_{16}$, with the same status as a master INTA cycle, when a non-maskable-interrupt is acknowledged.



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* Table entries 1 to 15 should not be used by the ICU since they contain NMI and Trap Descriptors or are reserved for future use. (For more details refer to NS32016 data sheet.)

FIGURE 2-5. Interrupt Dispatch and Cascade Tables

2.0 Functional Description (Continued)

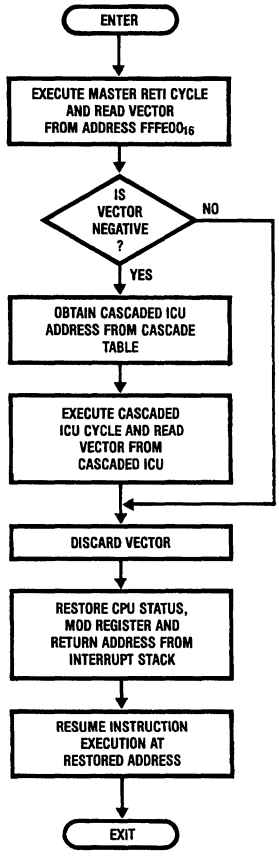

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FIGURE 2–6. CPU Return from Interrupt Sequence

The master ICU maintains a list (in the CSRC register pair) of its interrupt positions that are cascaded. It also provides a 4-bit (hidden) counter (in-service counter) for each interrupt position to keep track of the number of interrupts being serviced in the cascade ICUs. When a cascaded interrupt input is active, the master ICU activates its interrupt output and the CPU responds with a Master Interrupt Acknowledge Cycle. However, instead of generating a positive interrupt vector, the master ICU generates a negative Cascade Table index.

The CPU interprets the negative number returned from the master ICU as an index into the Cascade Table. The Cascade Table is located in a negative direction from the Dispatch Table, and it contains the virtual addresses of the hardware vector registers for any cascaded NS32202s in the system. Thus, the Cascade Table index supplied by the master ICU identifies the cascaded ICU that requested the interrupt.

Once the cascaded ICU is identified, the CPU performs a Cascaded Interrupt Acknowledge cycle. During this cycle, the CPU reads the final vector value directly from the cascaded ICU, and uses it to access the Dispatch Table. Each cascaded ICU, of course, has its own set of 16 unique interrupt vectors, one vector for each of its 16 interrupt positions.

The CPU interprets the vector value read during a Cascaded Interrupt Acknowledge cycle as an unsigned number. Thus, this vector can be in the range 0 through 255.

When a cascaded interrupt service routine completes its task, it must return control to the interrupted program with the same RETI instruction used in non-cascaded interrupt service routines. However, when the CPU performs a Master Return From Interrupt cycle, the CPU accesses the master ICU and reads the negative Cascade Table index identifying the cascaded ICU that originally received the interrupt request. Using the cascaded ICU address, the CPU now performs a Cascaded Return From Interrupt cycle, informing the cascaded ICU that the service routine is over. The byte provided by the cascaded ICU during this cycle is ignored.

2.4 INTERNAL ICU OPERATING SEQUENCE

The NS32202 ICU accepts two interrupt types, software and hardware.

Software interrupts are initiated when the CPU sets the proper bit in the Interrupt Pending (IPND) registers (R6, R7), located in the ICU. Bits are set and reset by writing the proper byte to either R6 or R7. Software interrupts can be masked, by setting the proper bit in the mask registers (R10, R11).

Hardware interrupts can be either internal or external to the ICU. Internal ICU hardware interrupts are initiated by the on-chip counter outputs. External hardware interrupts are initiated by devices external to the ICU, that are connected to any of the ICU interrupt input pins.

Hardware interrupts can be masked by setting the proper bit in the mask registers (R10, R11). If the Freeze bit (FRZ), located in the Mode Control Register (MCTL), is set, all incoming hardware interrupts are inhibited from setting their corresponding bits in the IPND registers. This prevents the ICU from recognizing any hardware interrupts.

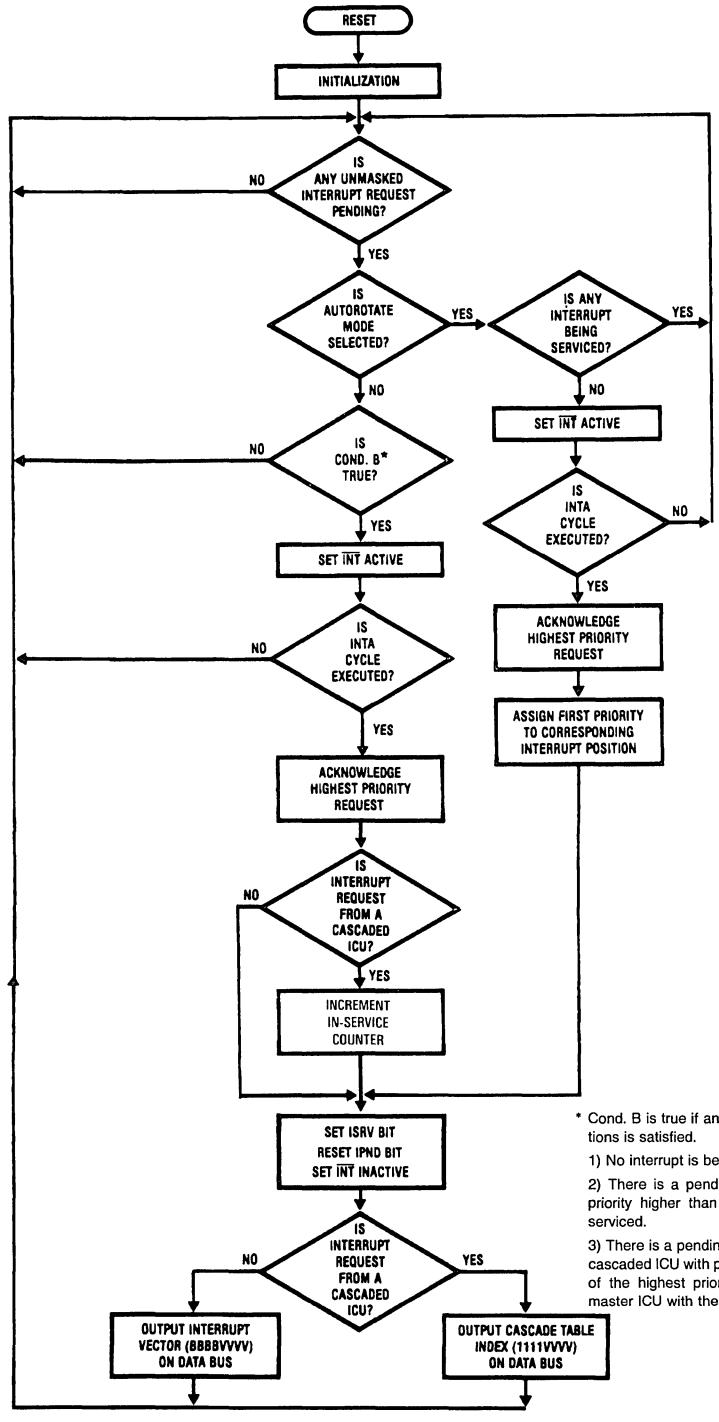
Once the ICU is initialized, it is enabled to accept interrupts. If an active interrupt is not masked, and has a higher priority than any interrupt currently being serviced, the ICU activates its Interrupt Output ($\overline{INT}$). *Figure 2–7* is a flowchart showing the ICU interrupt acknowledge sequence.

The CPU responds to the active $\overline{INT}$ line by performing an Interrupt Acknowledge bus cycle. During this cycle, the ICU clears the IPND bit corresponding to the active interrupt position and sets the corresponding bit in the Interrupt In-Service Registers (ISRV). The 4-bit in-service counter in the master ICU is also incremented by one if the fixed priority mode is selected and the interrupt is from a cascaded ICU. The ISRV bit remains set until the CPU performs a RETI bus cycle and the 4-bit in-service counter is decremented to zero. *Figure 2–8* is a flowchart showing ICU operation during a RETI bus cycle.

When the ISRV bit is set, the $\overline{INT}$ output is disabled. This output remains inactive until a higher priority interrupt position becomes active, or the ISRV bit is cleared.

An exception to the above occurs in the master ICU when the fixed priority mode is selected, and the interrupt input is connected to the $\overline{INT}$ output of a cascaded ICU. In this case the ISRV bit does not inhibit an interrupt of the same priority. This is to allow nesting of interrupts in a cascaded ICU.

2.0 Functional Description (Continued)



* Cond. B is true if any one of the following conditions is satisfied.

1) No interrupt is being serviced

2) There is a pending unmasked interrupt with priority higher than that of the interrupt being serviced.

3) There is a pending unmasked interrupt from a cascaded ICU with priority higher or same as that of the highest priority interrupt position in the master ICU with the ISRV bit set.

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FIGURE 2–7. ICU Interrupt Acknowledge Sequence

2.0 Functional Description (Continued)

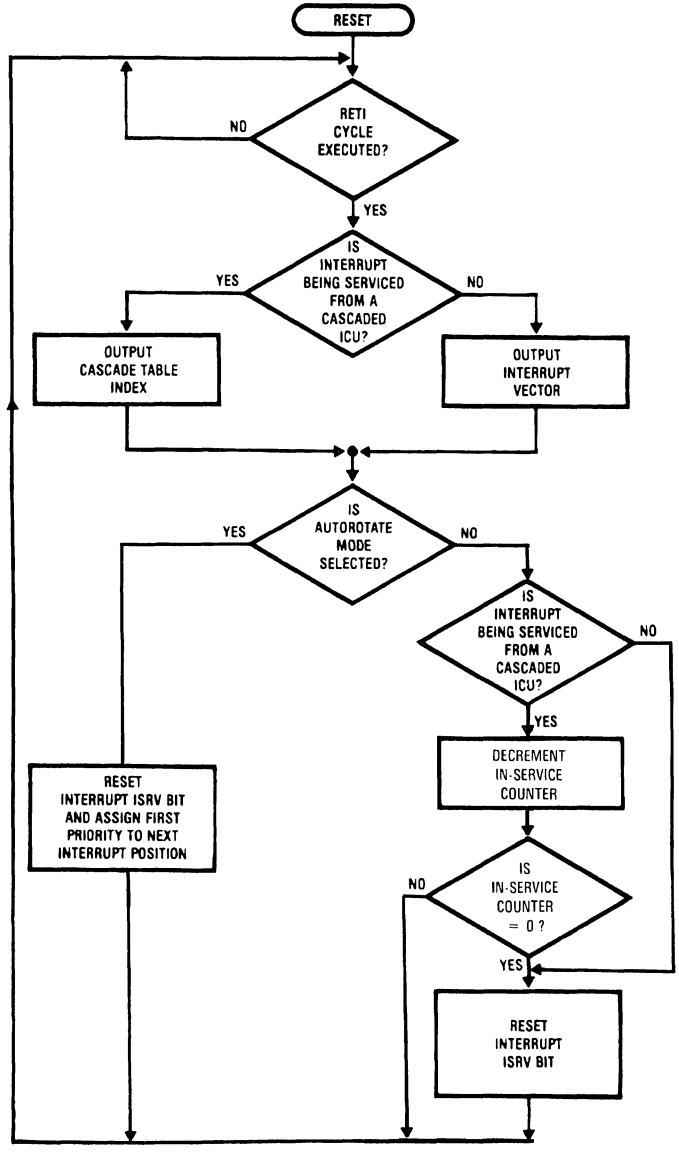

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FIGURE 2–8. ICU Return from Interrupt Sequence

2.0 Functional Description (Continued)

2.5 INTERRUPT PRIORITY MODES

The NS32202 ICU can operate in one of four interrupt priority modes: Fixed Priority; Auto-Rotate; Special Mask; and Polling. Each mode is described below.

2.5.1 Fixed Priority Mode

In the Fixed Priority Mode (also called Fully Nested Mode), each interrupt position is ranked in priority from 0 to 15, with 0 being the highest priority. In this mode, the processing of lower priority interrupts is nested with higher priority interrupts. Thus, while an interrupt is being serviced, any other interrupts of the same or lower priority are inhibited. The ICU does, however, recognize higher priority interrupt requests.

When the interrupt service routine executes its RETI instruction, the corresponding ISRV bit is cleared. This allows any lower priority interrupt request to be serviced by the CPU.

At reset, the default priority assignment gives interrupt IR0 priority 0 (highest priority), interrupt IR1 priority 1, and so forth. Interrupt IR15 is, of course, assigned priority 15, the lowest priority. The default priority assignment can be altered by writing an appropriate value into register FPRT (L) as explained in Section 3.9.

Note: When the ICU generates an interrupt request to the CPU for a higher priority interrupt while a lower priority interrupt is still being serviced by the CPU, the CPU responds to the interrupt request only if its internal interrupt enable flag is set. Normally, this flag is reset at the beginning of an interrupt acknowledge cycle and set during the RETI cycle. If the CPU is to respond to higher priority interrupts during any interrupt service routine, the service routine must set the internal CPU interrupt enable flag, as soon during the service routine as desired.

2.5.2 Auto-Rotate Mode

The Auto Rotate Mode is selected when the NTAR bit is set to 0, and is automatically entered after Reset. In this mode an interrupt source position is automatically assigned lowest priority after a request at that position has been serviced. Highest priority then passes to the next lower priority position. For example, when servicing of the interrupt request at position 3 is completed (ISRV bit 3 is cleared), interrupt position 3 is assigned lowest priority and position 4 assumes highest priority. The nesting of interrupts is inhibited, since the interrupt being serviced always has the highest priority.

This mode is used when the interrupting devices have to be assigned equal priority. A device requesting an interrupt, will have to wait, in the worst case, until each of the 15 other devices has been serviced at most once.

2.5.3 Special Mask Mode

The Special Mask Mode is used when it is necessary to dynamically alter the ICU priority structure while an interrupt is being serviced. For example, it may be desired in a particular interrupt service routine to enable lower priority interrupts during a part of the routine. To do so, the ICU must be programmed in fixed priority mode and the interrupt service routine must control its own in-service bit in the ISRV registers.

The bits of the ISRV registers are changed with either the Set Bit Interlocked or Clear Bit Interlocked instructions (SBITIW or CBITIW). The in-service bit is cleared to enable lower priority interrupts and set to disable them.

Note: For proper operation of the ICU, an interrupt service routine must set its ISRV bit before executing the RETI instruction. This prevents the RETI cycle from clearing the wrong ISRV bit.

2.5.4 Polling Mode

The Polling Mode gives complete control of interrupt priority to the system software. Either some or all of the interrupt positions can be assigned to the polling mode. To assign all interrupt positions to the polling mode, the CPU interrupt enable flag is reset. To assign only some of the interrupt positions to the polling mode, the desired interrupt positions are masked in the Interrupt Mask registers (IMSK). In either case, the polling operation consists of reading the Interrupt Pending (IPND) registers.

If necessary, the IPND read can be synchronized by setting the Freeze (FRZ) bit in the Mode Control register (MCTL). This prevents any change in the IPND registers during the read. The FRZ bit must be reset after the polling operation so the IPND contents can be updated. If an edge-triggered interrupt occurs while the IPND registers are frozen, the interrupt request is latched, and transferred to the IPND registers as soon as FRZ is reset.

The polling mode is useful when a single routine is used to service several interrupt levels.

3.0 Architectural Description

The NS32202 has thirty-two 8-bit registers that can be accessed either individually or in pairs. In 16-bit data bus mode, register pairs can be accessed with the CPU word or double-word reference instructions. *Figure 3–1* shows the ICU internal registers. This figure summarizes the name, function, and offset address for each register.

Because some registers hold similar data, they are grouped into functional pairs and assigned a single name. However, if a single register in a pair is referenced, either an L or an H is appended to the register name. The letters are placed in parentheses and stand for the low order 8 bits (L) and the high order 8 bits (H). For example, register R6, part of the Interrupt Pending (IPND) register pair, is referred to individually as IPND(L).

The following paragraphs give detailed descriptions of the registers shown in *Figure 3–1.*

3.1 HVCT — HARDWARE VECTOR REGISTER (R0)

The HVCT register is a single register that contains the interrupt vector byte supplied to the CPU during an Interrupt Acknowledge (INTA) or Return From Interrupt (RETI) cycle. The HVCT bit map is shown below:

7	6	5	4	3	2	1	0
B	B	B	B	V	V	V	V

3.0 Architectural Description (Continued)

REG. NUMBER AND ADDRESS IN HEX.		REG. NAME	REG. FUNCTION
	R0 (00_{16})	HVCT —	HARDWARE VECTOR
	R1 (01_{16})	SVCT —	SOFTWARE VECTOR
R3 (03_{16})	R2 (02_{16})	ELTG —	EDGE/LEVEL TRIGGERING
R5 (05_{16})	R4 (04_{16})	TPL —	TRIGGERING POLARITY
R7 (07_{16})	R6 (06_{16})	IPND —	INTERRUPTS PENDING
R9 (09_{16})	R8 (08_{16})	ISRV —	INTERRUPTS IN-SERVICE
R11 ($0B_{16}$)	R10 ($0A_{16}$)	IMSK —	INTERRUPT MASK
R13 ($0D_{16}$)	R12 ($0C_{16}$)	CSRC —	CASCADED SOURCE
R15 ($0F_{16}$)	R14 ($0E_{16}$)	FPRT —	FIRST PRIORITY
	R16 (10_{16})	MCTL —	MODE CONTROL
	R17 (11_{16})	OCASN —	OUTPUT CLOCK ASSIGNMENT
	R18 (12_{16})	CIPTR —	COUNTER INTERRUPT POINTER
	R19 (13_{16})	PDAT —	PORT DATA
	R20 (14_{16})	IPS —	INTERRUPT/PORT SELECT
	R21 (15_{16})	PDIR —	PORT DIRECTION
	R22 (16_{16})	CCTL —	COUNTER CONTROL
	R23 (17_{16})	CICTL —	COUNTER INTERRUPT CONTROL
R25 (19_{16})	R24 (18_{16})	LCSV —	L-COUNTER STARTING VALUE
R27 ($1B_{16}$)	R26 ($1A_{16}$)	HCSV —	H-COUNTER STARTING VALUE
R29 ($1D_{16}$)	R28 ($1C_{16}$)	LCCV —	L-COUNTER CURRENT VALUE
R31 ($1F_{16}$)	R30 ($1E_{16}$)	HCCV —	H-COUNTER CURRENT VALUE

FIGURE 3–1. ICU Internal Registers

3.0 Architectural Description (Continued)

The BBBB field is the bias which is programmed by writing $BBBB0000_2$ to the SVCT register (R1). The VVVV field identifies one of the 16 interrupt positions. The contents of the HVCT register provide various information to the CPU, as shown in *Figure 3-2*.

Note 1: The ICU always interprets a read of the HVCT register as either an INTA or RETI cycle. Since these cycles cause internal changes to the ICU, normal programs must never read the ICU HVCT register.

Note 2: If the HVCT register is read with ST1 = 0 (INTA cycle) and no unmasked interrupt is pending, the binary value BBBB1111 is returned and any pending edge-triggered interrupt in position 15 is cleared.

If the auto-rotate priority mode is selected, the FPRT register is also cleared, thus preventing any interrupt from being acknowledged. In this case a re-intialization of the FPRT register is required for the ICU to acknowledge interrupts again.

If a read of the HVCT register is performed with ST1 = 1 (RETI cycle), the binary value BBBB1111 is returned.

If the auto-rotate mode is selected, a priority rotation is also performed.

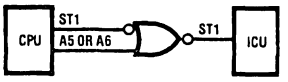
3.2 SVCT — SOFTWARE VECTOR REGISTER (R1)

The SVCT register is a copy of the HVCT register. It allows the programmer to read the contents of the HVCT register without initiating a INTA or RETI cycle in the ICU. It also allows a programmer to change the BBBB field of the HVCT register. The bit map of the SVCT register is the same as for the HVCT register.

During a write to SVCT, the four least significant bits are unaffected while the four most significant bits are written into both SVCT and HVCT (R1 and R0).

The SVCT register is updated dynamically by the ICU. The four least significant bits always contain the vector value that would be returned to the CPU if a INTA or RETI cycle were executed. Therefore, when reading the SVCT register, the state of the CPU ST1 pin is used to select either pending interrupt data or in-service interrupt data. For example, if the SVCT register is read with ST1 = 0 (as for an INTA cycle), the VVVV field contains the encoded value of the highest priority pending interrupt. On the other hand, if the SVCT register is read with ST1 = 1, the VVVV field contains the encoded value of the highest priority in-service interrupt.

Note: If the CPU ST1 output is connected directly to the ICU ST1 input, the vector read from SVCT is always the RETI vector. If both the INTA and RETI vectors are desired, additional logic must be added to drive the ICU ST1 input. A typical circuit is shown below. In this circuit, the state of the ICU ST1 input is controlled by both the CPU ST1 output and the selected address bit.



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3.3 ELTG — EDGE/LEVEL TRIGGERING REGISTERS (R2, R3)

The ELTG registers determine the input trigger mode for each of the 16 interrupt inputs. Each input is assigned a bit in this register pair. An interrupt input is level-triggered if its bit in ELTG is set to 1. The input is edge-triggered if its bit is cleared. At reset, all bits in ELTG are set to 1.

If odd-numbered interrupt positions must be used for software interrupts, the edge triggering mode must be selected and the corresponding interrupt inputs should be prevented from changing state.

3.4 TPL — TRIGGERING POLARITY REGISTERS (R4, R5)

The TPL registers determine the polarity of either the active level or the active edge for each of the 16 interrupt inputs. As with the ELTG registers, each input is assigned a bit. Possible triggering modes for the various combinations of ELTG and TPL bits are shown below.

ELTG BIT	TPL BIT	TRIGGERING MODE
0	0	Falling Edge
0	1	Rising Edge
1	0	Low Level
1	1	High Level

Software interrupt positions are not affected by their TPL bits. At reset, all TPL bits are set to 0.

Note 1: If edged-triggered interrupts are to be handled, the TPL register should be programmed before the ELTG register.

This prevents spurious interrupt requests from being generated during the ICU initialization from edge-triggered interrupt positions.

Note 2: Hardware interrupt inputs connected to cascaded ICUs must have their TPL bits set to 0.

3.5 IPND — INTERRUPT PENDING REGISTERS (R6, R7)

The IPND registers track interrupt requests that are pending but not yet serviced. Each interrupt position is assigned a bit in IPND. When an interrupt is pending, the corresponding bit in IPND is set. The IPND data are used by the ICU to generate interrupts to the CPU. These data are also used in polling operations.

	INTA CYCLE (ST1 = 0)		RETI CYCLE (ST1 = 1)	
	Highest priority pending interrupt is from:		Highest priority in-service interrupt was from:	
BBBB	cascaded ICU	any other source	cascaded ICU	any other source
	1111	programmed bias*	1111	programmed bias*
VVVV	encoded value of the highest priority pending interrupt		encoded value of the highest priority in-service interrupt	

*The Programmed bias for the master ICU must range from 0000 to 0111_2 because the CPU interprets a one in the most significant bit position as a Cascade Table Index indicator for a cascaded ICU.

FIGURE 3-2. HVCT Register Data Coding

3.0 Architectural Description (Continued)

The IPND registers are also used for requesting software interrupts. This is done by writing specially formatted data bytes to either IPND(L) or IPND(H). The formats differ for registers R6 and R7. These formats are shown below:

IPND(L) (R6) — S0000PPP

IPND(H) (R7) — S0001PPP

Where: S = Set (S = 1) or Clear (S = 0)

PPP = is a binary number identifying one of eight bits

Note: The data read from either R6 or R7 are different from that written to the register because the ICU returns the register contents, rather than the formatted byte used to set the register bits.

The ICU automatically clears a set IPND bit when the pending interrupt request is serviced. All pending interrupts in a register can be cleared by writing the pattern 'X1XXXXXX' to it (X = don't care). To avoid conflicts with asynchronous hardware interrupt requests, the IPND registers should be frozen before pending interrupts are cleared. Refer to the Mode Control Register description for details on freezing the IPND registers.

At reset, all IPND bits are set to 0.

Note: The edge sensing mechanism used for hardware interrupts in the NS32202 ICU is a latching device that can be cleared only by acknowledging the interrupt or by changing the trigger mode to level sensing. Therefore, before clearing pending interrupts in the IPND registers, any edge-triggered interrupt inputs must first be switched to the level-triggered mode. This clears the edge-triggered interrupts; the remaining interrupts can then be cleared in the manner described above. This applies to clearing the interrupts only. Edge-triggered interrupts can be set without changing the trigger mode.

3.6 ISRV — INTERRUPT IN-SERVICE REGISTERS (R8, R9)

The ISRV registers track interrupt requests that are currently being serviced. Each interrupt position is assigned a bit in ISRV. When an interrupt request is serviced by the ICU, its corresponding bit is set in the ISRV registers. Before generating an interrupt to the CPU, the ICU checks the ISRV registers to ensure that no higher priority interrupt is currently being serviced.

Each time the CPU executes an RETI instruction, the ICU clears the ISRV bit corresponding to the highest priority interrupt in service. The ISRV registers can also be written into by the CPU. This is done to implement the special mask priority mode.

At reset, the ISRV registers are set to 0.

Note: If the ICU initialization does not follow a hardware reset, the ISRV register should be cleared during initialization by writing zeroes into it.

3.7 IMSK — INTERRUPT MASK REGISTERS (R10, R11)

Each NS32202 interrupt position can be individually masked. A masked interrupt source is not acknowledged by the ICU. The IMSK registers store a mask bit for each of the ICU interrupt positions. If an interrupt position's IMSK bit is set to 1, the position is masked.

The IMSK registers are controlled by the system software. At reset, all IMSK bits are set to 1, disabling all interrupts.

Note: If an interrupt must be masked off, the CPU can do so by setting the corresponding bit in the IMSK register. However, if an interrupt is set pending during the CPU instruction that masks off that interrupt, the CPU may still perform an interrupt acknowledge cycle following that instruction since it might have sampled the $\overline{INT}$ line before the ICU deasserted it. This could cause the ICU to provide an invalid vector. To avoid this problem, the above operation should be performed with the CPU interrupt disabled.

3.8 CSRC — CASCADED SOURCE REGISTERS (R12, R13)

The CSRC registers track any cascaded interrupt positions. Each interrupt position is assigned a bit in the CSRC registers. If an interrupt position's CSRC bit is set, that position is connected to the $\overline{INT}$ output of another NS32202 ICU, i.e., it is a cascaded interrupt.

At reset, the CSRC registers are set to 0.

Note 1: If any cascaded ICU is used, the CSRC register should be cleared during initialization (if the initialization does not follow a hardware reset) by writing zeroes into it. This should be done before setting the bits corresponding to the cascaded interrupt positions. This operation ensures that the 4-bit in-service counters (associated with each interrupt position to keep track of cascaded interrupts) always get cleared when the ICU is re-initialized.

Note 2: Only the Master ICU should have any CSRC bits set. If CSRC bits are set in a cascaded ICU, incorrect operation results.

3.9 FPRT — FIRST PRIORITY REGISTERS (R14, R15)

The FPRT registers track the ICU interrupt position that currently holds first priority. Only one bit of the FPRT registers is set at one time. The set bit indicates the interrupt position with first (highest) priority.

The FPRT registers are automatically updated when the ICU is in the auto-rotate mode. The first priority interrupt can be determined by reading the FPRT registers. This operation returns a 16-bit word with only one bit set. An interrupt position can be assigned first priority by writing a formatted data byte to the FPRT(L) register. The format is shown below:

7	6	5	4	3	2	1	0
X	X	X	X	F	F	F	F

Where: XXXX = Don't Care

FFFF = A binary number from 0 to 15 indicating the interrupt position assigned first priority.

Note: The byte above is written only to the FPRT(L) register. Any data written to FPRT(H) is ignored.

At reset the FFFF field is set to 0, thus giving interrupt position 0 first priority.

3.10 MCTL — MODE CONTROL REGISTER (R16)

The contents of the MCTL set the operating mode of the NS32202 ICU. The MCTL bit map is shown below.

7	6	5	4	3	2	1	0
CFRZ	COUTD	COUTM	CLKM	FRZ	unused	NTAR	T16N8

3.0 Architectural Description (Continued)

CFRZ Determines whether or not the NS32202 counter readings are frozen. When frozen, the counters continue counting but the LCCV and HCCV registers are not updated. Reading of the true value of LCCV and HCCV is possible only while they are frozen.

CFRZ = 0 => LCCV and HCCV Not Frozen

CFRZ = 1 => LCCV and HCCV Frozen

COUTD Determines whether the COUT/SCIN pin is an input or an output. COUT/SCIN should be used as an input only for testing purposes. In this case an external sampling clock must be provided otherwise hardware interrupts will not be recognized.

COUTD = 0 => COUT/SCIN is Output

COUTD = 1 => COUT/SCIN is Input

COUTM When the COUT/SCIN pin is programmed as an output (COUTD=0), this bit determines whether the output signal is in pulsed form or in square wave form.

COUTM = 0 => Square Wave Form

COUTM = 1 => Pulsed Form

CLKM Used only in the 8-bit Bus Mode. This bit controls the clock wave form on any of the pins G0/IR0, . . . ,G3/IR6 programmed as counter output.

CLKM = 0 => Square Wave Form

CLKM = 1 => Pulsed Form

FRZ Freeze Bit. In order to allow a synchronous reading of the interrupt pending registers (IPND), their status may be frozen, causing the ICU to ignore incoming requests. This is of special importance if a polling method is used.

FRZ = 0 => IPND Not Frozen

FRZ = 1 => IPND Frozen

NTAR Determines whether the ICU is in the AUTO-ROTATE or FIXED Priority Mode. In AUTO-ROTATE mode, the interrupt source at the highest priority position, after being serviced, is assigned automatically lowest priority. In this mode, the interrupt in service always has highest priority and nesting of interrupts is therefore inhibited.

NTAR = 0 => Auto-Rotate Mode

NTAR = 1 => Fixed Mode

T16N8 Controls the data bus mode of operation.

T16N8 = 0 => 8-Bit Bus Mode

T16N8 = 1 => 16-Bit Bus Mode

At reset, all MCTL bits except COUTD, are reset to 0. COUTD is set to 1.

3.11 OCASN — OUTPUT CLOCK ASSIGNMENT REGISTER (R17)

Used only in the 8-bit Bus Mode. The four least significant bits of this register control the output clock assignments on pins G0/IR0, . . . ,G3/IR6. If any of these bits is set to 1, the clock generated by either the H-Counter or the H+L-Counter will be output to the corresponding pin. The four most significant bits of OCASN are not used. At Reset the four least significant bits are set to 0.

Note: The interrupt sensing mechanism on pins G0/IR0, . . . ,G3/IR6 is not disabled when any of these pins is programmed as clock output. Thus, to avoid spurious interrupts, the corresponding bits in register IPS should also be set to zero.

3.12 CIPTR — COUNTER INTERRUPT POINTER REGISTER (R18)

The CIPTR register tracks the assignment of counter outputs to interrupt positions. A bit map of this register is shown below.

7	6	5	4	3	2	1	0
H	H	H	H	L	L	L	L

Where: HHHH = A 4-bit binary number identifying the interrupt position assigned to the H-Counter (or the H+L-counter if the counters are concatenated).

LLLL = A 4-bit binary number identifying the interrupt position assigned to the L-counter.

Note: Assignment of a counter output to an interrupt position also requires control bits to be set in the CICTL register. If a counter output is assigned to an interrupt position, external hardware interrupts at that position are ignored.

At reset, all bits in the CIPTR are set to 1. (This means both counters are assigned to interrupt position 15.)

3.13 PDAT — PORT DATA REGISTER (R19)

Used only in the 8-bit Bus Mode. This register is used to input or output data through any of the pins G0/IR0, . . . ,G7/IR14 programmed as I/O ports by the IPS register. Any pin programmed as an output delivers the data written into PDAT. The input pins ignore it. Reading PDAT provides the logical value of all I/O pins, INPUT and OUTPUT.

3.14 IPS — INTERRUPT/PORT SELECT REGISTER (R20)

Used only in the 8-bit Bus Mode. This register controls the function of the pins G0/IR0, . . . ,G7/IR14. Each of these pins is individually programmed as an I/O port, if the corresponding bit of IPS is 0; as an interrupt source, if the corresponding bit is 1. The assignment of the H-Counter output to G0/IR0, . . . ,G3/IR6 by means of reg. OCASN overrides the assignment to these pins as I/O ports or interrupt inputs.

At Reset, all the IPS bits are set to 1.

Note: Whenever a bit in the IPS register is set to zero, to program the corresponding pin as an I/O port, any pending interrupt on the corresponding interrupt position will be cleared.

3.15 PDIR — PORT DIRECTION REGISTER (R21)

Used only in the 8-bit Bus Mode. This register determines the direction of any of the pins G0/IR0, . . . ,G7/IR14 programmed as I/O ports by the IPS register. A logic 1 indicates an input, while a logic 0 indicates an output.

At Reset, all the PDIR bits are set to 1.

3.16 CCTL — COUNTER CONTROL REGISTER (R22)

The CCTL register controls the operating modes of the counters. A bit map of CCTL is shown below.

7	6	5	4	3	2	1	0
CCON	CFNPS	COUT1	COUT0	CRUNH	CRUNL	CDCRH	CDCRL

CCON Determines whether the counters are independent or concatenated to form a single 32-bit counter (H+L-Counter). If a 32-bit counter is selected, the bits corresponding to the H-

3.0 Architectural Description (Continued)

Counter will control the H+L-Counter, while the bits corresponding to the L-Counter are not used.

CCON = 0 => Two 16-bit Counters

CCON = 1 => One 32-bit Counter

CFNPS Determines whether the external clock is prescaled or not.

CFNPS = 0 => Clock Prescaled (divided by 4)

CFNPS = 1 => Clock Not Prescaled.

COUT1 & COUT0 These bits are effective only when the COUT/SCIN pin is programmed as an OUTPUT (COUTD bit in reg. MCTL is 0). Their logic levels are decoded to provide different outputs for COUT/SCIN, as detailed in the table below:

COUT1	COUT0	COUT/SCIN Output Signal
0	0	Internal Sampling Oscillator
0	1	Zero Detect Of L-Counter
1	0	Zero Detect Of H-Counter
1	1	Zero Detect Of H+L-Counter*

*If the H- and L-Counters are not concatenated and COUT1/COUT0 are both 1, the COUT/SCIN pin is active when either counter reaches zero.

CRUNH Determines the state of either the H-Counter or the H+L-Counter, depending upon the status of CCON.

CRUNH = 0 => H-Counter or H+L-Counter Halted

CRUNH = 1 => H-Counter or H+L-Counter Running

CRUNL Effective only when CCON = 0. This bit determines whether the L-Counter is running or halted.

CRUNL = 0 => L-Counter Halted

CRUNL = 1 => L-counter Running

CDCRH Effective only when CRUNH = 0 (Counter Halted). This bit is the single cycle decrement signal for either the H-Counter or the H+L-Counter.

CDCRH = 0 => No Effect

CDCRH = 1 => Decrement H-Counter or H+L-Counter

CDCRL Effective only when CRUNL = 0 and CCON = 0. This bit is the single cycle decrement signal for the L-Counter.

CDCRL = 0 => No Effect

CDCRL = 1 => Decrement L-Counter

Note: The bits CDCRL and CDCRH are set when a logic 1 is written into them, but, they are automatically cleared after the end of the write operation. This is needed to accomplish the decrement operation. Therefore, these bits always contain 0 when read.

Reset does not affect the CCTL bits.

3.17 CICTL — COUNTER INTERRUPT CONTROL REGISTER (R23)

The CICTL register controls the counter interrupts and records counter interrupt status. Interrupts can be generated from either of the 16-bit counters. When the counters are concatenated, the interrupt control is through the H-Counter control bits. In this case the CIEL bit should be set to zero to avoid spurious interrupts from the L-Counter. A bit map of the CICTL register is shown following.

7	6	5	4	3	2	1	0
CERH	CIRH	CIEH	WENH	CERL	CIRL	CIEL	WENL

CERH H-Counter Error Flag. This bit is set (1) when a second interrupt request from the H-Counter (or H+L-Counter) occurs before the first request is acknowledged.

CIRH H-Counter Interrupt Request. It is set (1) when an interrupt is pending from the H-Counter (or H+L-Counter). It is automatically reset when the interrupt is acknowledged.

CIEH H-Counter Interrupt Enable. When it is set, the H-Counter (or H+L-Counter) interrupt is enabled.

WENH H-Counter Control Write Enable. When WEHN is set (1), bits CERH, CIRH, and CIEH can be written.

CERL L-Counter Error Flag. This bit is set (1) when a second interrupt request from the L-Counter occurs before the first request is acknowledged.

CIRL L-Counter Interrupt Request. It is set (1) when an interrupt is pending from the L-Counter. It is automatically reset when the interrupt is acknowledged.

CIEL L-Counter Interrupt Enable. When it is set (1), the L-Counter interrupt is enabled.

WENL L-Counter Control Write Enable. When WENL is set (1), bits CERL, CIRL, and CIEL can be written.

Note: Setting the write enable bits (WENH or WENL) and writing any of the other CICTL bits are concurrent operations. That is, the ICU will ignore any attempt to alter CICTL bits if the proper write enable bit is not set in the data byte.

At reset, all CICTL bits are set to 0. However, if the counters are running, the bits CIRL, CERL, CIRH and CERH may be set again after the reset signal is removed.

3.18 LCSV/HCSV — L-COUNTER STARTING VALUE/ H-COUNTER STARTING VALUE REGISTERS (R24, R25, R26, AND R27)

The LCSV and HCSV registers store the start values for the L-Counter and H-Counter, respectively. Each time a counter reaches zero, the start value is automatically reloaded from either LCSV or HCSV, one clock cycle after zero count is reached. Loading LCSV or HCSV from the CPU must be synchronized to avoid writing the registers while the reloading of the counters is occurring. One method is to halt the counters while the registers are loaded.

When the 16-bit counters are concatenated, the LCSV and HCSV registers hold the 32-bit start count, with the least significant byte in R24 and the most significant byte in R27.

3.19 LCCV/HCCV — L-COUNTER CURRENT VALUE/ H-COUNTER CURRENT VALUE REGISTERS (R28, R29, R30, AND R31)

The LCCV and HCCV registers hold the current value of the counters. If the CFRZ bit in the MCTL register is reset (0), these registers are updated on each clock cycle with the current value of the counters. LCCV and HCCV can be read only when the counter readings are frozen (CFRZ bit in the

3.0 Architectural Description (Continued)

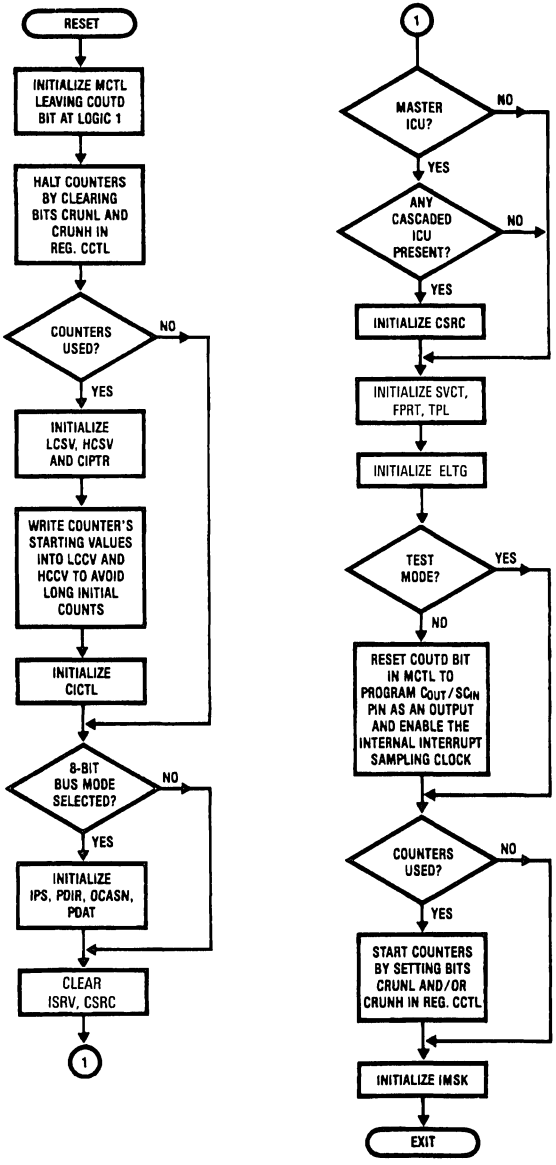

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FIGURE 3–3. Recommended ICU's Initialization Sequence

3.0 Architectural Description (Continued)

MCTL register is 1). They can be written only when the counters are halted (CRUNL and/or CRUNH bits in the CCTL register are 0). This last feature allows new initial count values to be loaded immediately into the counters, and can be used during initialization to avoid long initial counts.

When the 16-bit counters are concatenated, the LCCV and HCCV registers hold the 32-bit current value, with the least significant byte in R28 and the most significant byte in R31.

3.20 REGISTER INITIALIZATION

Figure 3-3 shows a recommended initialization procedure for the ICU that sets up all the ICU registers for proper operation.

4.0 Device Specifications

4.1 NS32202 PIN DESCRIPTIONS

4.1.1 Power Supply

Power (V_{CC}): +5V DC Supply

Ground (GND): Power Supply Return

4.1.2 Input Signals

Reset ($\overline{RST}$): Active low. This signal initializes the ICU. (The ICU initializes to the 8-bit bus mode.)

Chip Select ($\overline{CS}$): Active low. This signal enables the ICU to respond to address, data, and control signals from the CPU.

Addresses (A0 through A4): Address lines used to select the ICU internal registers for read/write operations.

High Byte Enable ($\overline{HBE}$): Active low. Enables data transfers on the most-significant byte of the Data Bus. If the ICU is in the 8-bit Bus Mode, this signal is not used and should be connected to either GND or V_{CC}.

Read ($\overline{RD}$): Active low. Enables data to be read from the ICU's internal registers.

Write ($\overline{WR}$): Active low. Enables data to be written into the ICU's internal registers.

Status (ST1): Status signal from the CPU. When the Hardware Vector Register is read, this signal differentiates an INTA cycle from an RETI cycle. If ST1 = 0 the ICU initiates an INTA cycle. If ST1 = 1 an RETI cycle will result.

Interrupt Requests (IR1, IR3..., IR15): These eight inputs are used for hardware interrupts. Each may be individually triggered in one of four modes: Rising Edge, Falling Edge, Low Level, or High Level.

Counter Clock (CLK): External clock signal to drive the ICU internal counters.

4.1.3 Output Signals

Interrupt Output ($\overline{INT}$): Active low. This signal indicates that an interrupt is pending.

4.1.4 Input/Output Signals

Data Bus 0-7 (D0 through D7): Eight low-order data bus lines used in both 8-bit and 16-bit bus modes.

General Purpose I/O Lines (G0/IR0, G1/IR2,...,G7/IR14): These pins are the high-order data bits when the ICU is in the 16-bit bus mode. When the ICU is in the 8-bit bus mode, each of these can be individually assigned one of the following functions:

- Additional Hardware Interrupt Input (IR0 through IR14)
- General Purpose Data Input
- General Purpose Data Output
- Clock Output from H-Counter (Pins G0/IR0 through G3/IR6 only)

It should be noted that, for maximum flexibility in assigning interrupt priorities, the interrupt positions corresponding to pins G0/IR0,...,G7/IR14 and IR1,...,IR15 are interleaved.

Counter or Oscillator Output/Sampling Clock Input (COUT/SCIN): As an output, this pin provides either a clock signal generated by the ICU internal oscillator, or a zero detect signal from one or both of the ICU counters. As an input, it is used for an external clock, to override the internal oscillator used for interrupt sampling. This is done only for testing purposes.

4.0 Device Specifications (Continued)

4.2 ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias	0°C to +70°C
Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to GND	−0.5V to +7.0V
Power Dissipation	1.5 Watt

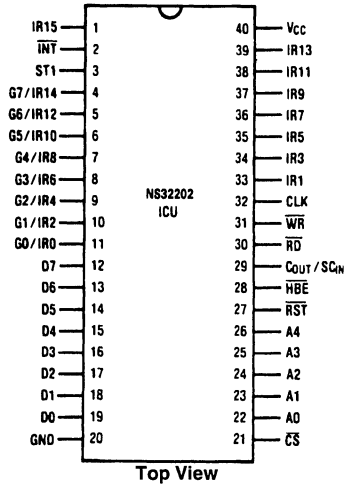
Note: *Absolute maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended; operation should be limited to those conditions specified under Electrical Characteristics.*

4.3 ELECTRICAL CHARACTERISTICS

T_A = 0° to 70°C, V_{CC} = +5V ± 5%, GND = 0V

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage		2.0			V
V_{OL}	Output Low Voltage	I_{OL} = 2 mA			0.45	V
V_{OH}	Output High Voltage	I_{OH} = −400 μA	2.4			V
I_L	Leakage Current (Output and I/O Pins in TRI-STATE/Input mode)	0.4 ≤ V_{IN} ≤ V_{CC}	−20		20	μA
I_I	Input Load Current	V_{in} = 0 to V_{CC}	−20		20	μA
I_{CC}	Power Supply Current	I_{out} = 0, T = 0°C			300	mA

Connection Diagram



Top View

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Order Number NS32202D-6, NS32202D-10
See NS Package Number D40C

FIGURE 4–1

4.0 Device Specifications (Continued)

4.4 SWITCHING CHARACTERISTICS

4.4.1 Definitions

All the timing specifications given in this section refer to 0.8V or 2.0V on the input and output signals as illustrated in *Figure 1*, unless specifically stated otherwise.

Abbreviations:

L.E.—leading edge R.E.—rising edge
T.E.—trailing edge F.E.—falling edge

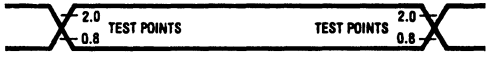

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FIGURE 4–2. Timing Specification Standard

4.4.1.1 Timing Tables

Symbol	Figure	Description	Reference/Conditions	NS32202-10		Units
				Min	Max	
READ CYCLE						
t_{AhRDia}	4-3	Address Hold Time	After $\overline{RD}$ T.E.	10		ns
t_{AsRDa}	4-3	Address Setup Time	Before $\overline{RD}$ L.E.	35		ns
$t_{CShRDia}$	4-3	$\overline{CS}$ Hold Time	After $\overline{RD}$ T.E.	15		ns
t_{CSsRDa}	4-3	$\overline{CS}$ Setup Time	Before $\overline{RD}$ L.E.	30		ns
t_{DhRDia}	4-3	Data Hold Time	After $\overline{RD}$ T.E.	5	50	ns
t_{RDaDv}	4-3	Data Valid	After $\overline{RD}$ L.E.		150	ns
t_{RDw}	4-3	$\overline{RD}$ Pulse Width	At 0.8V (Both Edges)	160		ns
t_{SsRDa}	4-3	ST1 Setup Time	Before $\overline{RD}$ L.E.	35		ns
t_{ShRDia}	4-3	ST1 Hold Time	After $\overline{RD}$ T.E.	−30		ns
WRITE CYCLE						
t_{AhWRia}	4-4	Address Hold Time	After $\overline{WR}$ T.E.	10		ns
t_{AsWRa}	4-4	Address Setup Time	Before $\overline{WR}$ L.E.	35		ns
$t_{CShWRia}$	4-4	$\overline{CS}$ Hold Time	After $\overline{WR}$ T.E.	15		ns
t_{CSsWRa}	4-4	$\overline{CS}$ Setup Time	Before $\overline{WR}$ L.E.	30		ns
t_{DhWRia}	4-4	Data Hold Time	After $\overline{WR}$ T.E.	10		ns
t_{DsWRia}	4-4	Data Setup Time	Before $\overline{WR}$ T.E.	70		ns
t_{WRiaPf}	4-4	Port Output Floating	After $\overline{WR}$ T.E. (To PDIR)		200	ns
t_{WRiaPv}	4-4	Port Output Valid	After $\overline{WR}$ T.E.		200	ns
t_{WRw}	4-4	$\overline{WR}$ Pulse Width	At 0.8V (Both Edges)	160		ns

4.0 Device Specifications (Continued)

4.4.1.1 Timing Tables (Continued)

Symbol	Figure	Description	Reference/Conditions	NS32202-10		Units
				Min	Max	
OTHER TIMINGS						
t_{COUTl}	4-8	Internal Sampling Clock Low Time	At 0.8V (Both Edges)	50		ns
t_{COUTp}	4-8	Internal Sampling Clock Period		400		ns
t_{SCINh}	4-7	External Sampling Clock High Time	At 2.0V (Both Edges)	100		ns
t_{SCINl}	4-7	External Sampling Clock Low Time	At 0.8V (Both Edges)	100		ns
t_{SCINp}	4-7	External Sampling Clock Period		800		ns
t_{Ch}	4-9	External Clock High Time (Without Prescaler)	At 2.0V (Both Edges)	100		ns
t_{Chp}	4-9	External Clock High Time (With Prescaler)	At 2.0V (Both Edges)	40		ns
t_{Cl}	4-9	External Clock Low Time (Without Prescaler)	At 0.8V (Both Edges)	100		ns
t_{Clp}	4-9	External Clock Low Time (With Prescaler)	At 0.8V (Both Edges)	40		ns
t_{Cy}	4-9	External Clock Period (Without Prescaler)		400		ns
t_{Cyp}	4-9	External Clock Period (With Prescaler)		100		ns
t_{GCOUTl}	4-9	Counter Output Transition Delay	After CLK F.E.		300	ns
t_{COUTw}	4-9	Counter Output Pulse Width in Pulsed Form	At 0.8V (Both Edges)	50		ns
t_{ACKIR}	4-5	Interrupt Request Delay	After Previous Interrupt Acknowledge	500		ns
t_{IRld}	4-5	$\overline{INT}$ Output Delay	After Interrupt Request Active		800	ns
t_{IRw}	4-5	Interrupt Request Pulse Width in Edge Trigger	At 0.8V (Both Edges)	50		ns
t_{RSTw}		$\overline{RST}$ Pulse Width	At 0.8V (Both Edges)	400		ns

4.4.1.2 Timing Diagrams

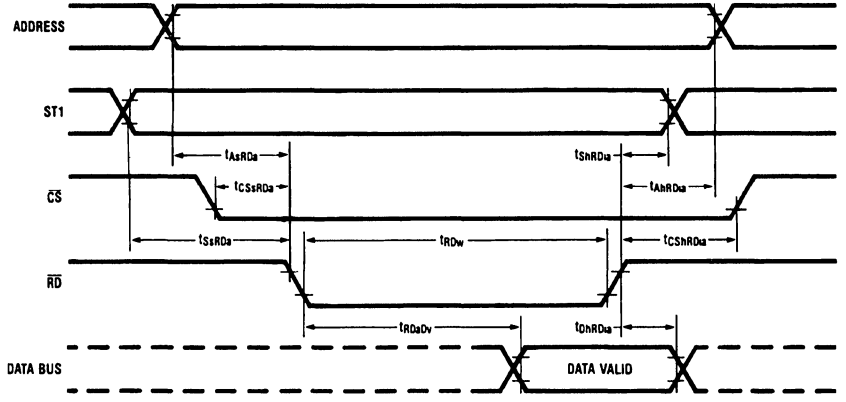

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FIGURE 4–3. READ/INTA Cycle

4.0 Device Specifications (Continued)

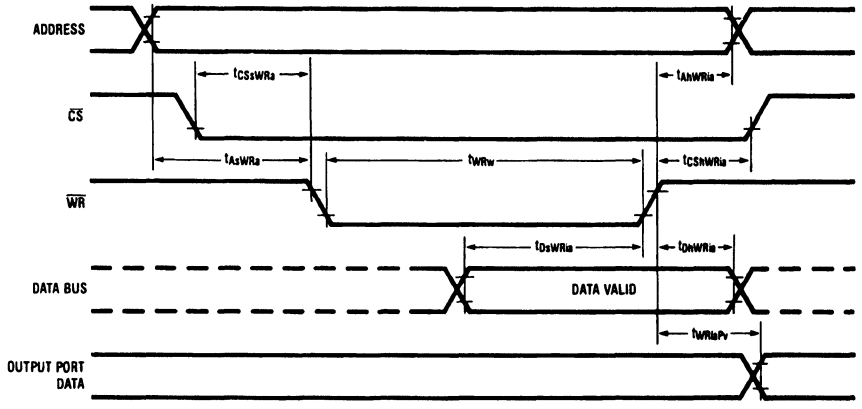

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FIGURE 4–4. Write Cycle

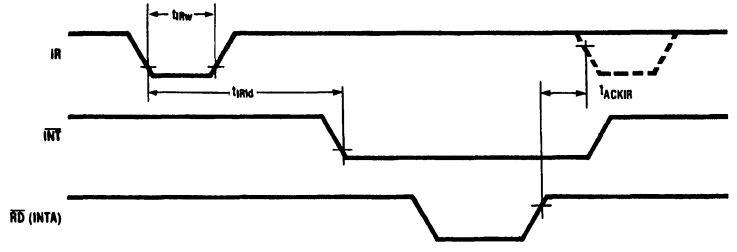

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FIGURE 4–5. Interrupt Timing in Edge Triggering Mode

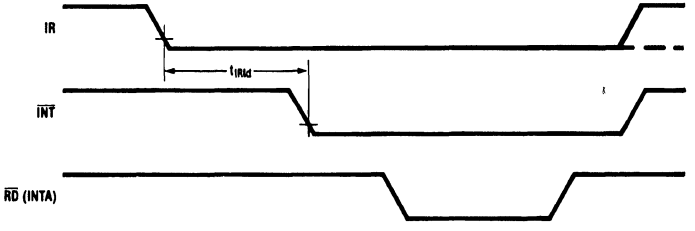

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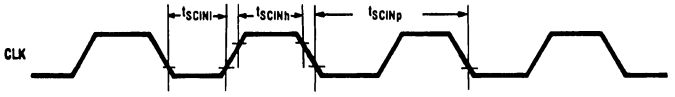
FIGURE 4–6. Interrupt Timing in Level Triggering Mode

4.0 Device Specifications (Continued)



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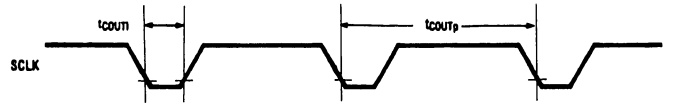
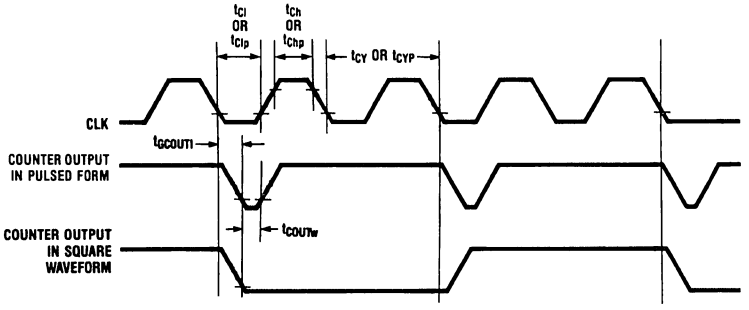
Note: Interrupts are sampled on the rising edge of CLK.

FIGURE 4–7. External Interrupt-Sampling-Clock to be Provided at Pin COUT/SCIN When in Test Mode



TL/EE/5117–22

FIGURE 4–8. Internal Interrupt-Sampling-Clock Provided at Pin COUT/SCIN



TL/EE/5117–23

FIGURE 4–9. Relationship Between Clock Input at Pin CLK and Counter Output Signals at Pins COUT/SCIN or G0/R0,...,G3/R6, in Both Pulsed Form and Square Waveform

National Semiconductor

PRELIMINARY

NS32203-10 Direct Memory Access Controller

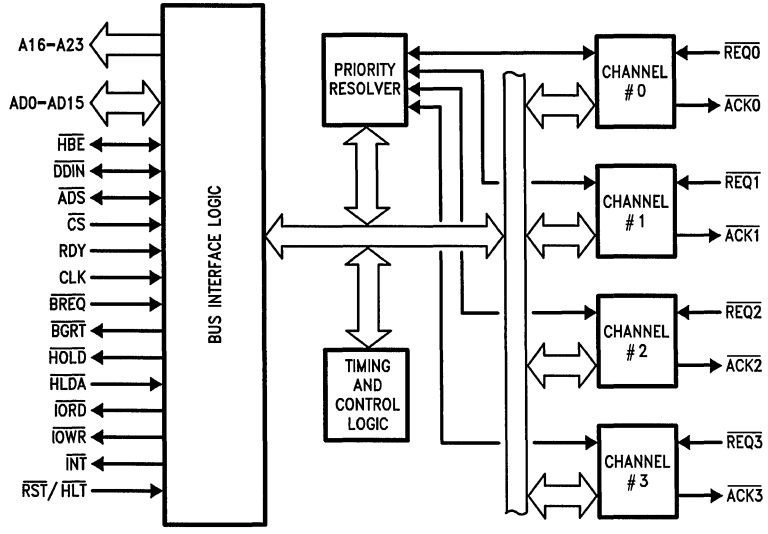
General Description

The NS32203 Direct Memory Access Controller (DMAC) is a support chip for the Series 32000® microprocessor family designed to relieve the CPU of data transfers between memory and I/O devices. The device is capable of packing data received from 8-bit peripherals into 16-bit words to reduce system bus loading. It can operate in local and remote configurations. In the local configuration it is connected to the multiplexed Series 32000 bus and shares with the CPU, the bus control signals from the NS32201 Timing Control Unit (TCU). In the remote configuration, the DMAC, in conjunction with its own TCU, communicates with I/O devices and/or memory through a dedicated bus, enabling rapid transfers between memory and I/O devices. The DMAC provides 4 16-bit I/O channels which may be configured as two complementary pairs to support chaining.

Features

- Direct or Indirect data transfers
- Memory to Memory, I/O to I/O or Memory to I/O transfers
- Remote or Local configurations
- 8-Bit or 16-Bit transfers
- Transfer rates up to 5 Megabytes per second
- Command Chaining on complementary channels
- Wide range of channel commands
- Search capability
- Interrupt Vector generation
- Simple interface with the Series 32000 Family of Microprocessors
- High Speed XMOS™ Technology
- Single +5V Supply
- 48-Pin Dual-In-Line Package

Block Diagram



TL/EE/8701–1

Table of Contents

List of Illustrations

1.0 Product Introduction

The NS32203 Direct Memory Access Controller (DMAC) is specifically designed to minimize the time required for high speed data transfers in a Series 32000-based computer system. It includes a wide variety of options and operating modes to enhance data throughput and system optimization, and to allow dynamic reconfiguration under program control.

The NS32203 can operate in two basic system configurations: local and remote. In the local configuration, the DMAC and the CPU share the same bus (address, data and control) and only one of them can perform data transfers on the bus at any one time. In this configuration, the DMAC and the CPU also share a Timing Control Unit (TCU) and a single set of address latches. Since this configuration yields a minimum part-count system, it offers a good cost/performance trade-off in many situations.

The remote configuration is intended to minimize the CPU bus use. In this configuration, the NS32203 I/O devices and optional buffer memory have their own dedicated bus (remote bus) so that an I/O transfer may be performed without loading the CPU bus (local bus).

Communication between the dedicated bus and the CPU bus may be initiated at any time by either the CPU or the NS32203. The DMAC accesses the CPU bus whenever a data transfer to/from memory or any I/O device residing on this bus is to be performed. The CPU, in turn, accesses the dedicated bus for reading status data or for programming either the DMAC or its I/O devices.

The NS32203 internal organization consists of seven functional blocks as illustrated in the block diagram. Descriptions of these blocks are given below.

DMA Channels. The NS32203 provides four channels. Each channel accepts a request from a peripheral I/O device and informs it when data transfer cycles are about to begin. A set of registers is provided for each channel to control the type of operation for that channel.

Bus Interface Unit. The bus interface unit controls all data transfers between peripheral I/O devices and memory whenever the DMAC is in control of the bus. This unit also controls the transfer of data between the CPU and the DMAC internal registers.

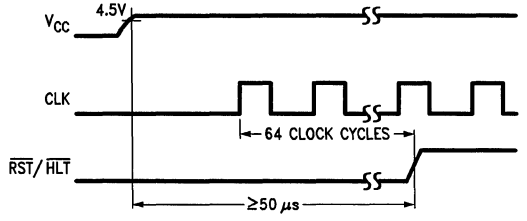
Timing and Control Logic. This block generates all the sequencing and control signals necessary for the operation of the DMAC.

Priority Resolver. This block resolves contentions among channels requesting service simultaneously.

2.0 Functional Description

2.1 RESETTING

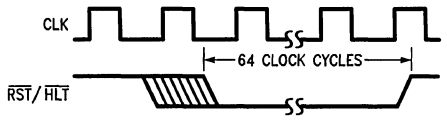
The $\overline{RST}/\overline{HLT}$ line serves both as a reset input for the on-chip logic and as a DMAC HALT input. Resetting is accomplished by pulling $\overline{RST}/\overline{HLT}$ low for at least 64 clock cycles. Upon detecting a Reset, the DMAC terminates any Data transfer in progress, resets its internal logic and enters an inactive state. On application of power, $\overline{RST}/\overline{HLT}$ must be held low for at least 50 μs after V_{CC} is stable. This is to ensure that all on-chip voltages are stable before operation. Whenever reset is applied, the rising edge must occur while the clock signal on the CLK pin is high (see *Figure 2-1* and *2-2*). The NS32201 TCU provides circuitry to meet the reset requirements. *Figure 2-3* shows the recommended connections. The HALT function is accomplished when $\overline{RST}/\overline{HLT}$ is activated for 1 or 2 clock cycles and then released. It can be used to stop any data transfer in progress in case of a bus error. As soon as HALT is acknowledged by the NS32203, the current transfer operation is terminated. See *Figure 4-18*.



TL/EE/8701–2

FIGURE 2-1. Power-On Reset Requirements

2.0 Functional Description (Continued)



TL/EE/8701-3

FIGURE 2-2. General Reset Timing

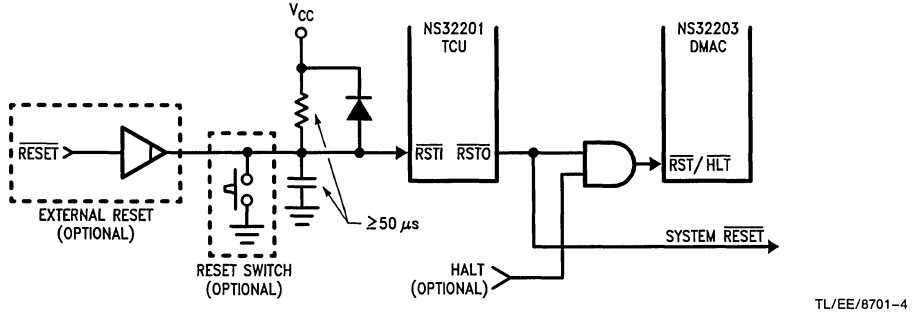


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FIGURE 2-3. Recommended Reset Connections

2.2 DATA TRANSFER OPERATIONS

After the NS32203 has been initialized by software, it is ready to transfer blocks of data, containing up to 64 kbytes, between memory and I/O devices, without further intervention required of the CPU. Upon receiving a transfer request from an I/O device, the DMAC performs the following operations:

1) Acquires control of the bus
2) Acknowledge the requesting I/O device which is connected to the highest priority channel.
3) Starts executing data transfer cycles according to the values stored into the control registers of the channel being serviced.
4) Terminates data transfers and relinquishes control of the bus as soon as one of the programmed conditions is met.

Each channel can be programmed for indirect or direct data transfers. Detailed descriptions of these transfer types are provided in the following sub-sections.

2.2.1 Indirect Data Transfers

In this mode of operation, each byte or word transfer between source and destination requires at least two bus cycles. The data is first read into the DMAC and subsequently it is written into the destination. The bus cycles in this case are similar to the CPU bus cycles when the MMU is not used. This mode is slower than the direct mode, but is the only one that allows some data manipulation like Byte Search or Word Assembly/Disassembly. *Figure 2-4* and *2-5* show the read and write cycle timing diagrams related to indirect data transfers. If a search operation is specified, extra clock cycles may be added following each read cycle.

2.0 Functional Description (Continued)

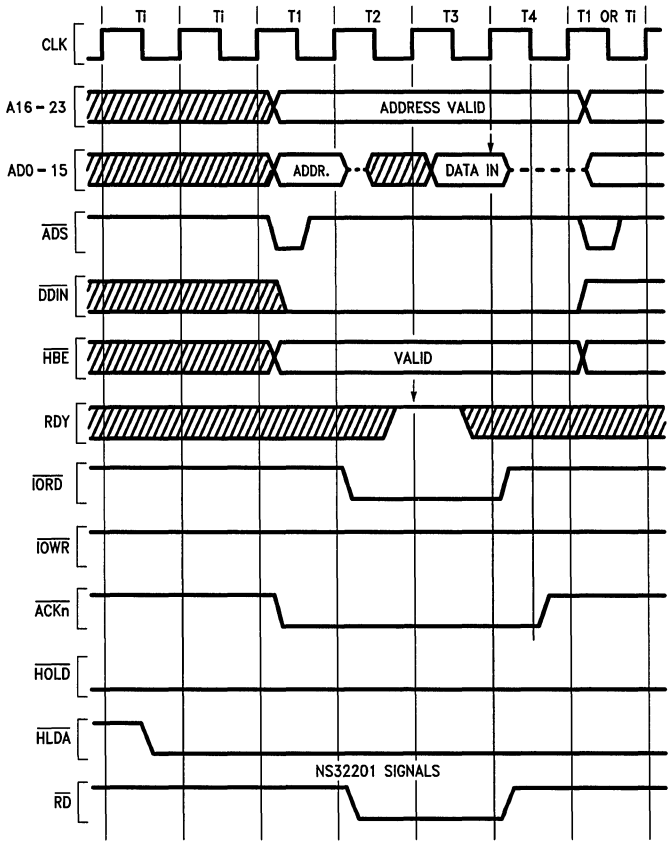

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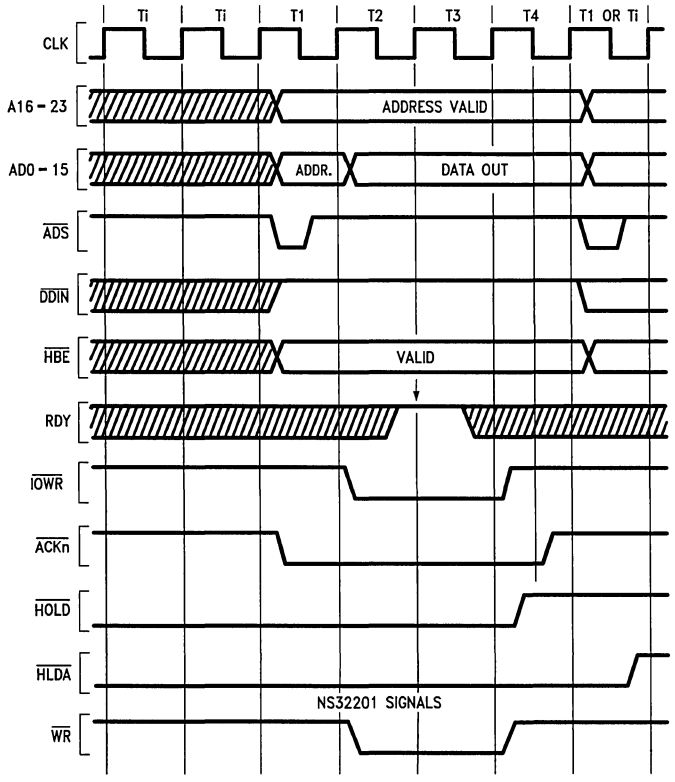
FIGURE 2-4. Indirect Read Cycle

2.0 Functional Description (Continued)



TL/EE/8701-6

FIGURE 2-5. Indirect Write Cycle (Single Transfer Mode)

Note: If burst mode is selected, $\overline{\text{HOLD}}$ is released at the end of the transfer operation.

2.0 Functional Description (Continued)

2.2.2 Direct (Flyby) Data Transfers

This mode of operation allows a very high data transfer rate between source and destination. Each data byte or word to be transferred requires only a single bus cycle instead of two separate read and write cycles, which are typical of the indirect mode. The DMAC accomplishes direct data transfers by activating $\overline{IORD}$, during memory write cycles, and $\overline{IOWR}$, during memory read cycles.

An I/O device, in the direct mode, is usually enabled by the proper acknowledge signal ($\overline{ACKn}$) from the DMAC. No search or word assembly/disassembly are possible during direct data transfers. *Figures 2-6* and *2-7* show the timing diagrams of direct memory-to-I/O and I/O-to-memory transfers respectively.

Note 1: In the direct mode each channel can control only one I/O device because the I/O device is hardwired to the $\overline{ACKn}$ output of the corresponding channel. in the indirect mode, a channel can control multiple devices as long as each device is selected through its own address rather than the $\overline{ACKn}$ output. However, the possiblity of selecting a single I/O device by the $\overline{ACKn}$ output is maintained in the indirect mode as well.

Note 2: Whenever the DMAC is either idle or is performing indirect transfers, it generates the $\overline{IORD}$ and $\overline{IOWR}$ signals as a replica of $\overline{RD}$ and $\overline{WR}$. This simplifies the logic required to access I/O devices wired for direct data transfers.

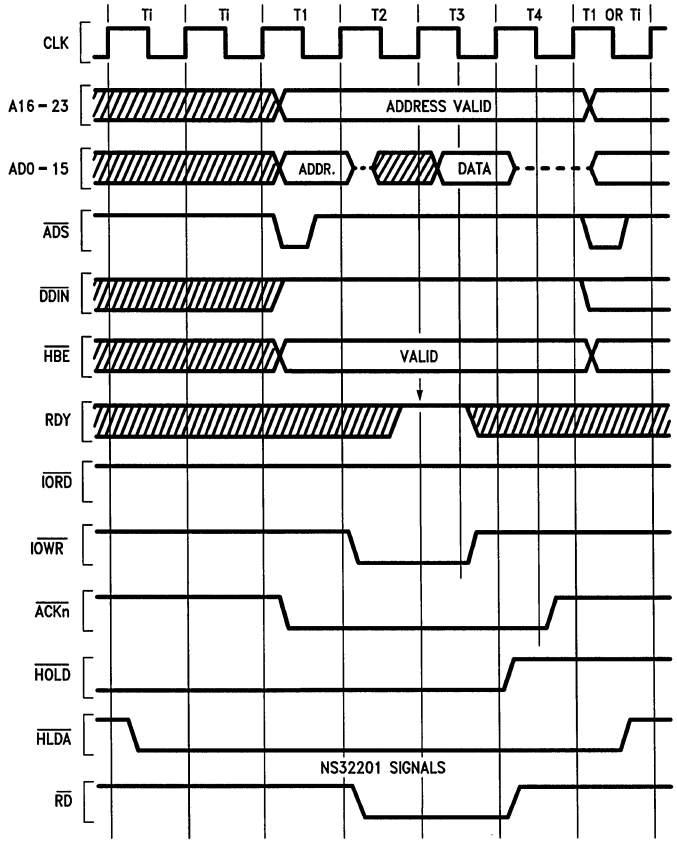


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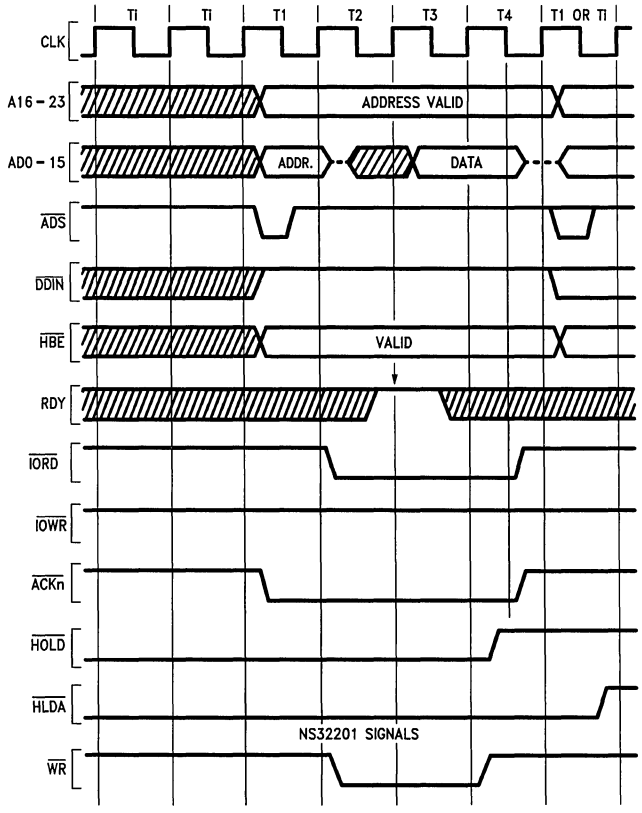
FIGURE 2-6. Direct Memory-To-I/O Data Transfer (Single Transfer Mode)

2.0 Functional Description (Continued)

2.3 LOCAL CONFIGURATION

As previously mentioned, in the local configuration the DMAC shares with CPU and MMU the multiplexed address/data bus as well as the control signals from the NS32201 TCU. A typical local configuration is shown in *Figure 2-8*. The DMAC, in the local configuration, must gain control of the bus whenever a data transfer cycle is to be performed, even though it is directed to an I/O device and is related to an indirect data transfer. This causes the system to be quite sensitive to the volume of data handled by the DMAC. Thus, the overall system performance decreases as the volume of data increases. A possible solution to this problem is to use the remote configuration, described in the following section. A significant advantage of the local configuration is its simplicity.



TL/EE/8701–8

FIGURE 2-7. Direct I/O-To-Memory Data Transfer (Single Transfer Mode)

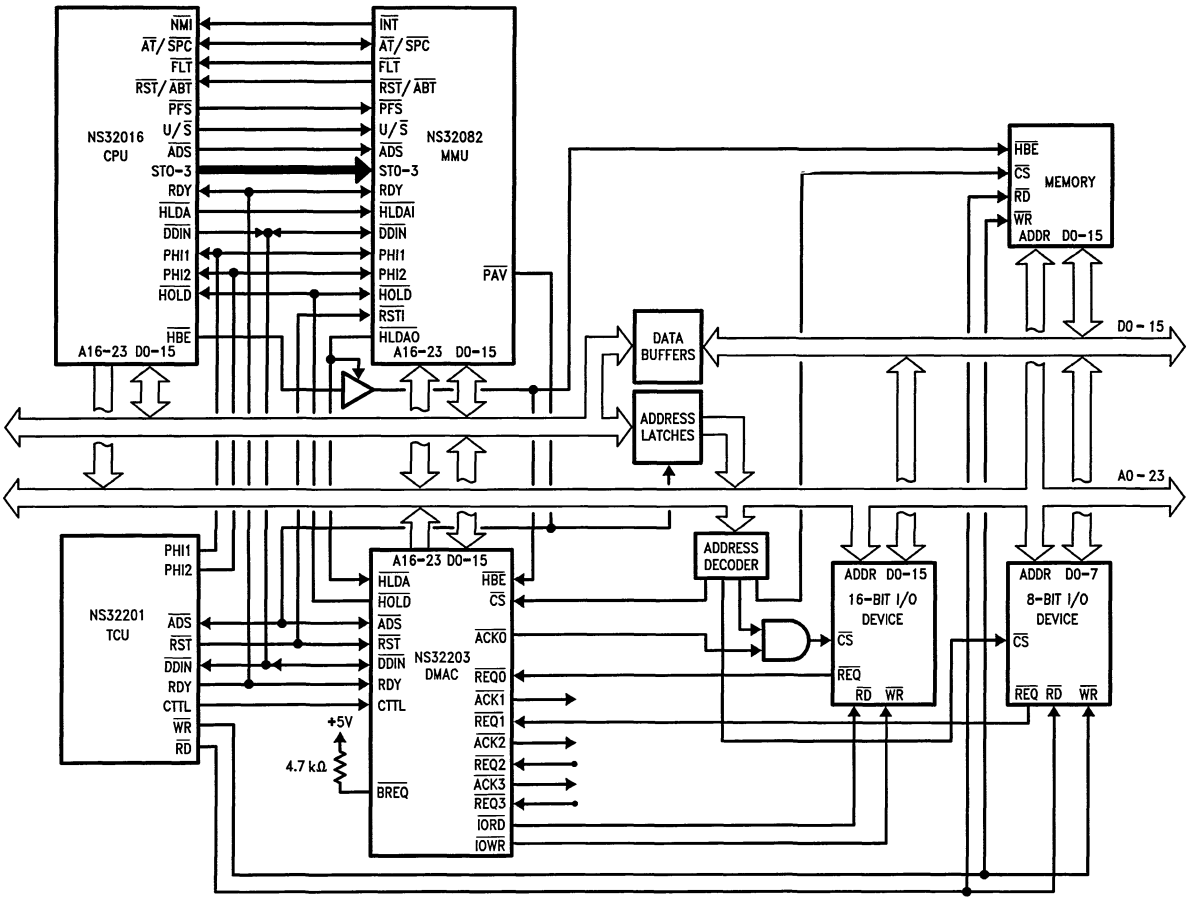


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FIGURE 2-8. NS32203 Interconnections In Local Configuration

Note 1: The 16 Bit I/O device is wired for direct transfers.
Note 2: The data buffers should not be enabled during direct data transfers or CPU accesses to the DMAC registers.

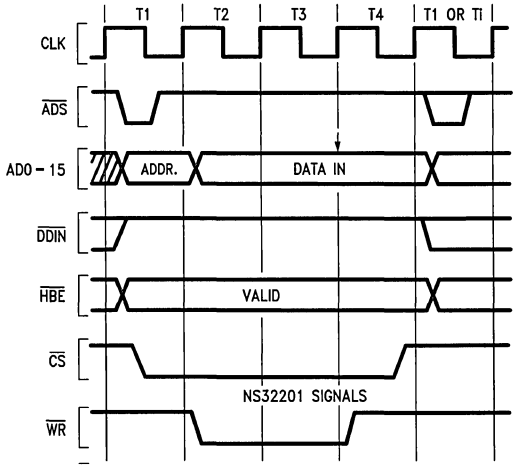
2.0 Functional Description (Continued)

2.4 REMOTE CONFIGURATION

The remote configuration is intended to minimize CPU Bus usage. In this configuration, the DMAC, buffer memory and I/O devices reside on a dedicated bus. Communication between the dedicated bus and the CPU bus is achieved by means of TRI-STATE buffers. Whenever the CPU needs to access the dedicated bus, it issues a bus request to the NS32203 by activating the $\overline{BREQ}$ signal. As the dedicated bus becomes idle, the DMAC pulls off the bus and acknowledges the CPU request by activating $\overline{BGRT}$. This output is also used as a control signal for the interconnection logic of the two buses.

The CPU can either be interrupted by $\overline{BGRT}$ or it can poll $\overline{BGRT}$ to determine when the dedicated bus can be accessed. The DMAC, in turn, before accessing the CPU bus, has to gain control of it. This is accomplished through the usual request-acknowledge mechanism performed by means of the $\overline{HOLD}$ and $\overline{HLDA}$ signals.

Figure A-1 in Appendix A shows an interconnection diagram of a basic remote configuration. Both TCUs are clocked by the same clock signal. They are synchronized during reset by the $\overline{RWEN}$/SYNC signal so that their output clocks are in phase. *Figures 2-9* and *2-10* show the timing diagrams for read and write accesses to the NS32203 internal registers.



TL/EE/8701–10

FIGURE 2-9. Write to NS32203 Internal Registers

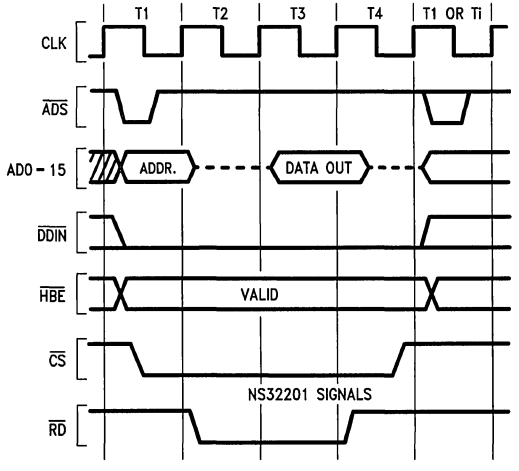


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FIGURE 2-10. Read from NS32203 Internal Registers

2.0 Functional Description (Continued)

2.5 DATA SOURCE (DESTINATION) ATTRIBUTES

Two types of data source (destination) are recognized: I/O device and memory. If the source (destination) is an I/O device, its address register is not changed after a data transfer; if it is memory, its address register is either incremented or decremented after any data transfer, according to the value of the corresponding direction bit. In the remote configuration, any data source (destination) may reside either on the CPU bus or on the dedicated bus. If it resides on the dedicated bus, the NS32203 does not activate the $\overline{HOLD}$ request line when an access to the source (destination) is performed, unless a direct transfer with a data destination (source) residing on the CPU bus is required.

Data can be transferred in either 8 bit or 16 bit units. The DMAC always considers the memory to be 16 bits wide. Thus, if an 8 bit transfer is specified, address bit A0 will determine the byte of the data-bus where the transfer takes place. If A0 = 0, the transfer occurs on the low order byte. If A0 = 1, it occurs on the high order byte. Different transfer widths can be specified for source and destination. However, some limitations exist in specifying these transfer widths when certain operations must be performed. These limitations are explained below.

1) If a transfer block has an odd number of bytes or is not word aligned, an 8 bit width for source and destination should be selected.
2) 16-bit I/O transfers can not be specified with 8 bit memory transfers.
3) Memory to memory transfers should have the same width.

Note 1: If source and destination are both memory, DMAC transfers can only be performed in indirect mode.

Note 2: If source and destination are both I/O devices and direct mode is being used, the source device is accessed by $\overline{IORD}$ and $\overline{ACK}$n; the destination device is accessed by $\overline{WR}$ (from the NS32201) and $\overline{CS}$ (from the address decoder). This allows a one direction data transfer only from one I/O device (source) to another. If data is to be transferred in both directions in direct mode between two I/O devices, two channels must be used (one for each direction of transfer), and extra hardware is required to control the read and write signals to the two I/O devices.

Note 3: When an 8-bit transfer is related to an I/O device, the other half of the 16-bit data bus is considered as DON'T CARE, and the $\overline{HBE}$/ signal may be activated.

2.6 WORD ASSEMBLY/DISASSEMBLY

This feature is automatically enabled when indirect transfers are selected, with data transferred between an 8-bit wide I/O device and a 16-bit I/O device or memory. For every 16-bit I/O device or memory access, the DMAC accesses the 8-bit I/O device twice, assembling two data bytes into a 16-bit word or breaking a 16-bit word into two data bytes, depending on the direction of transfer. The word assembly/disassembly feature allows a significant increase in the transfer speed and minimizes the CPU bus usage when the transfer occurs between an 8-bit I/O device residing on the dedicated bus, and a 16-bit I/O device or memory residing on the CPU bus. Word assembly/disassembly is not possible during direct data transfers.

Note: Requests from other channels are not acknowledged in the middle of a word assembly/disassembly. If this is unacceptable, 8 bit transfers should be specified for both source and destination.

2.7 AUTO TRANSFER

The NS32203 initiates a data transfer as a result of a request from an I/O device. In some cases a data transfer may be necessary without the corresponding request signal being asserted. This can happen, for example, when a block of data is to be moved from one memory region to another. In such cases, the auto transfer mode can be selected by setting an appropriate bit in the command register. The DMAC will initiate a data transfer regardless of the $\overline{REQ}$n signal for that channel.

Note: For proper operation, when auto transfer is required, the low order byte of the command register (containing the auto-transfer enable bit) should be written into after the other registers controlling the channel operation have been initialized.

2.8 SEARCH

The NS32203 provides a search capability that can be used to detect the occurrence of a certain data pattern. The search is performed by comparing each data byte with the search register, in conjunction with the mask register. An appropriate bit in the command register indicates whether the search continues 'UNTIL' a match occurs, or 'WHILE' a match exists. The search operation does not necessarily involve a data transfer. The DMAC allows a block of data to be searched without requiring any data transfer between source and destination. When performing a search, the user can specify whether or not the matched byte will be transferred. If 'INCLUSIVE SEARCH' is specified (INC = 1), the matched byte will be transferred, and the channel parameters will be updated accordingly. In this case, if a 16 bit word has been read from the data source and the search condition is satisfied by the low order byte, then the high order byte is transferred as well. If 'EXCLUSIVE SEARCH' is specified (INC = 0), the transfer will terminate with the last byte before the search condition was satisfied, and the parameters will point to the last transferred byte.

Search is not possible during direct transfers.

2.9 INTERRUPTS

The NS32203 provides interrupt circuitry that can be used to generate an interrupt whenever a data transfer is completed or a search condition is met. If an NS32202 ICU is used, the $\overline{INT}$ signal from the DMAC should be connected to an interrupt input of the ICU. When an interrupt occurs and the corresponding interrupt acknowledge (INTA) or return from interrupt (RETI) cycle is executed by the CPU, the NS32203 supplies its own vector as if it were a cascaded ICU. For such operation the virtual address of the interrupt vector register should be placed in the ICU cascade table, described in the NS32016 and NS32202 data sheets. See section 3.1.2.

2.10 TRANSFER MODES

When the NS32203 is in the inactive state and a channel requests service, the DMAC gains control of the bus and enters the active state. It is in this state that the data transfer takes place in one of the following modes:

SINGLE TRANSFER MODE

In single transfer mode, the NS32203 makes a single byte or word transfer for each $\overline{HOLD}$/$\overline{HLDA}$ handshake sequence.

In this case the request signal from the I/O device is edge sensitive, that is, a single transfer is performed each time a

2.0 Functional Description (Continued)

falling edge on $\overline{REQn}$ occurs. To perform multiple transfers, it is therefore necessary to temporarily deassert $\overline{REQn}$ after each transfer is initiated. If auto transfer mode is selected, the bus is released between two transfers for at least one clock cycle.

BURST (DEMAND) TRANSFER MODE

In burst transfer mode the DMAC will continue making data transfers until $\overline{REQn}$ goes inactive. Thus, the I/O device requesting service may suspend data transfer by bringing $\overline{REQn}$ inactive. Service may be resumed by asserting $\overline{REQn}$ again. If the auto transfer mode is selected, the DMAC will perform a single burst of data transfers until the end-transfer condition is reached.

Note 1: In either of the transfer modes described above, data transfers can only occur as long as the byte count is not zero or a search condition is not met. Whenever any of these conditions occur, the NS32203 terminates the current operation and releases the bus for at least one clock cycle.

Note 2: Whenever the DMAC releases $\overline{HOLD}$, it waits for $\overline{HLDA}$ to go inactive for at least one clock cycle before reasserting $\overline{HOLD}$ again to continue the transfer operation.

2.11 CHAINING

The NS32203 provides a chaining feature that allows the four DMAC channels to be regarded as two complementary pairs. Channels 0 and 1 form the first pair, while channels 2 and 3 form the second pair. Each pair is programmed independently by setting the corresponding bit in the configuration register. When two channels are complementary, only the even channel can perform transfer operations, while the odd one serves as temporary storage for the new control values and parameters loaded for the chaining operation. If an operation is being performed by the even channel of a pair and an end-condition is reached, the channel is not returned to the inactive state; rather, a new set of control values with or without parameters is loaded from the complementary channel and a new operation is started. During the reload operation the bus is released for at least two clock cycles. At the end of the second operation the channel returns to the inactive state, unless a new set of values has been loaded into the complementary channel by the CPU.

The chaining feature can be used to transfer blocks of data to/from non-contiguous memory segments. For example, the CPU can load channel 0 and 1 with control values and parameters for the first two blocks. After the operation for the first block is completed by channel 0, the control values and parameters stored in channel 1 are transferred to channel 0, during an update cycle, and a second operation is started. The CPU, being notified by an interrupt, can load channel 1 registers with control values and parameters for the third data block.

Note 1: Whenever a reload operation occurs, the register values of the complementary channel are affected. Thus, the CPU must always load a new set of values into the complementary channel if another chaining operation is required.

Note 2: When the chain option is selected, the CPU must be given the opportunity to acquire the bus for enough time between DMAC operations, in order for the complementary channel to be updated.

2.12 CHANNEL PRIORITIES

The NS32203 has four I/O channels, each of which can be connected to an I/O device. Since no dependency exists between the different I/O devices, a priority level is assigned to each I/O channel, and a priority resolver is provided to resolve multiple requests activated simultaneously.

The priority resolver checks the priorities on every cycle. If a channel is being serviced and a higher priority request is received, the channel operation is suspended and control passes to the higher priority channel, unless the lock bit for the lower priority channel is set. If the lock bit is set, that channel operation is continued until completion before control passes to the higher priority channel. The bus is always released for at least two clock cycles when control passes from one channel to another.

Two types of priority encodings are available as software selectable options.

The first is fixed priority which fixes the channels in priority order based on the decreasing values of their numbers. Channel 3 has the lowest priority, while channel 0 has the highest.

The second option is variable priority. The last channel that receives service becomes the lowest priority channel among all other channels with variable priority, while the channels which previously had lower priority will get their priorities increased. If variable priority is selected for all four channels, any I/O device requesting service is guaranteed to be acknowledged after no more than three higher priority services have occurred. This prevents any channel from monopolizing the system. Priority types can be intermixed for different channels.

As an example, let channels 0, 2 and 3 have variable priority and channel 1 fixed priority. Channel 2 receives service first, followed by channel 0. The priority levels among all channels will change as follows.

Priority	Initial Order	Next Order	Final Order
High 3		ch.0 ACK → ch.0	ch.3
2		ch.1	ch.1 ch.1 → fixed priority
1	ACK → ch.2	ch.3	ch.2
Low 0		ch.3	ch.2	ch.0

Whenever the PT bit (priority type) in the command register is changed, the priority levels of all the channels are reset to the initial order. If only one channel has variable priority, then no change in priority will occur from the initial order.

Note: If the lock bit is not set, three idle states are inserted between the write cycle of a previous burst indirect transfer and the next read cycle.

3.0 Architectural Description

The NS32203 has 128 8-bit registers that can be addressed either individually or in pairs, using the 7 least significant bits of the address bus and the high byte enable signal $\overline{HBE}$. Seventy-one of these registers are reserved, while the rest are accessible by the CPU for read/write operations. *Figure 3-1* shows the NS32203 internal registers together with their address offsets. Detailed descriptions of these registers are given in the following sections.

3.1 GLOBAL REGISTERS

The global registers consist of one configuration, one status and two interrupt vector registers. They are shared by all channels, and they control the overall operation of the NS32203.

3.1.1 CONF—Configuration Register

This register controls the hardware configuration of the NS32203 as well as the chaining feature.

3.0 Architectural Description (Continued)

The CONF register format is shown below:

7	6	5	4	3	2	1	0
XXXXX					C1	C0	CNF

CNF — Configuration Bit. Determines whether the NS32203 is in local or remote configuration.
CNF = 0 = > Local Configuration
CNF = 1 = > Remote Configuration

C0 — Chaining bit for channels 0 and 1. Determines whether or not channel 0 and 1 are complementary.
C0 = 0 = > Channels not complementary
C0 = 1 = > Channel 1 complementary to channel 0

C1 — Chaining bit for channels 2 and 3. Determines whether or not channels 2 and 3 are complementary.
C1 = 0 = > Channels not complementary
C1 = 1 = > Channel 3 complementary to channel 2

XXXXX — Reserved. These bits should be set to 0.

At reset, all CONF bits are reset to zero.

Note: The CNF bit should never be set by the software if the DMAC is wired for local configuration, otherwise bus conflicts will result.

	23 16	15 8	7 0	
Channel 0 Control Registers	COM(H) (02_{16})	COM(M) (01_{16})	COM(L) (00_{16})	Command
			SRCH (04_{16})	Search Pattern
			MSK (08_{16})	Search Mask
Channel 0 Parameter Registers	SRC(H) ($0E_{16}$)	SRC(M) ($0D_{16}$)	SRC(L) ($0C_{16}$)	Source Address
	DST(H) (12_{16})	DST(M) (11_{16})	DST(L) (10_{16})	Destination Address
		LNGT(H) (15_{16})	LNGT(L) (14_{16})	Block Length
Channel 1 Control Registers	COM(H) (22_{16})	COM(M) (21_{16})	COM(L) (20_{16})	Command
			SRCH (24_{16})	Search Pattern
			MSK (28_{16})	Search Mask
Channel 1 Parameter Registers	SRC(H) ($2E_{16}$)	SRC(M) ($2D_{16}$)	SRC(L) ($2C_{16}$)	Source Address
	DST(H) (32_{16})	DST(M) (31_{16})	DST(L) (30_{16})	Destination Address
		LNGT(H) (35_{16})	LNGT(L) (34_{16})	Block Length
Channel 2 Control Registers	COM(H) (42_{16})	COM(M) (41_{16})	COM(L) (40_{16})	Command
			SRCH (44_{16})	Search Pattern
			MSK (48_{16})	Search Mask
Channel 2 Parameters Registers	SRC(H) ($4E_{16}$)	SRC(M) ($4D_{16}$)	SRC(L) ($4C_{16}$)	Source Address
	DST(H) (52_{16})	DSC(M) 51_{16})	DST(L) (50_{16})	Destination Address
		LNGT(H) (55_{16})	LNGT(L) (54_{16})	Block Length
Channel 3 Control Registers	COM(H) (62_{16})	COM(M) (61_{16})	COM(L) (60_{16})	Command
			SRCH (64_{16})	Search Pattern
			MSK (68_{16})	Search Mask
Channel 3 Parameter Registers	SRC(H) ($6E_{16}$)	SRC(M) ($6D_{16}$)	SRC(L) ($6C_{16}$)	Source Address
	DST(H) (72_{16})	DST(M) (71_{16})	DST(L) (70_{16})	Destination Address
		LNGT(H) (75_{16})	LNGT(L) (74_{16})	Block Length
Global Registers			CONF (78_{16})	Configuration
			SVCT ($5C_{16}$)	Software Vector
			HVCT ($7C_{16}$)	Hardware Vector
		STAT(H) ($7F_{16}$)	STAT(L) ($7E_{16}$)	Status

FIGURE 3-1. NS32203 Internal Registers

3.0 Architectural Description (Continued)

3.1.2 HVCT — Hardware Vector Register

This register contains the interrupt vector byte that is supplied to the CPU during an interrupt acknowledge (INTA) or return from interrupt (RETI) cycle. The HVCT register format is shown below.

7	6	5	4	3	2	1	0
BIAS					E	CN	

CN — Channel number. Represents the number of the interrupting channel

E — Error code. Determines whether a normal operation completion or an error condition has occurred on the interrupting channel.

E = 0 => Normal Operation Completion

E = 1 => A second interrupt was generated by the same channel before the first interrupt was serviced.

BIAS — Programmable bias. This field is programmed by writing the pattern BBBBB000 into the HVCT register.

The NS32203 always interprets a read of the HVCT register as either an interrupt acknowledge (INTA) cycle or a return from interrupt (RETI) cycle. Since these cycles cause internal changes to the DMAC, normal programs should never read the HVCT register (see next section). The DMAC distinguishes an INTA cycle from a RETI cycle by the state of an internal flip-flop, called Interrupt Service Flip-Flop, that toggles every time the HVCT register is read. This flip-flop is cleared on reset or when the HVCT register is written into. When an interrupt is acknowledged by the CPU, the $\overline{INT}$ signal is deasserted unless another interrupt from a lower priority channel is pending. In this case the $\overline{INT}$ signal is deasserted when the acknowledge cycle for the second interrupt is performed.

For this reason, if the $\overline{INT}$ signal is connected to an interrupt input of the NS32202 ICU, the triggering mode of that interrupt position should be 'low level'.

Furthermore, if that ICU interrupt input is programmed for cascaded operation and nesting of interrupts from other devices connected to the ICU is to be allowed, then the ICU interrupt input connected to the DMAC should be masked off during the interrupt service routine, before the CPU interrupt is reenabled. This is because the DMAC does not provide interrupt nesting capability.

An interrupt from a certain channel can be acknowledged only after the return from interrupt from a previously acknowledged interrupt is performed.

3.1.3 SVCT — Software Vector Register

The SVCT register is an image of the HVCT register. It is a read-only register used for diagnostics. It allows the programmer to read the interrupt vector without affecting the interrupt logic of the NS32203. The format of the SVCT register is the same as that of the HVCT register.

3.1.4 STAT — Status Register

The status register contains status information of the NS32203, and can be used when the interrupts are not enabled. Each set bit is automatically cleared when a read operation is performed. The format of this register is shown in the following figure.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ME	CH	MN	TC	ME	CH	MN	TC	ME	CH	MN	TC	ME	CH	MN	TC
channel #3				channel #2				channel #1				channel #0			

The status of each channel is defined in a four-bit field as described below:

TC — Transfer Complete.

Indicates the completion of a channel operation, regardless of the state of the length register or whether a match/no match condition occurred.

MN — Match/No Match Bit.

This bit is set when a match/no match condition occurs.

CH — Channel Halted.

Set when a channel operation is halted by pulling the $\overline{RST}/\overline{HLT}$ pin.

ME — Multiple events. This bit is set when more than one of the above conditions have occurred.

Note: If an interrupt is enabled, the corresponding bit in the status register is not cleared upon read, unless the interrupt is acknowledged.

3.2 CONTROL REGISTERS

Each of the four channels has three control registers, consisting of a 24-bit command register, an 8-bit search register and an 8-bit mask register.

3.2.1 COM — Command Register

The command register controls the operation of the associated channel. It is divided into three separately addressable parts: COM(L), COM(M) and COM(H). The format of each part and bit functions are shown below.

COM(L) — Command Register (Low-Byte)

7	6	5	4	3	2	1	0
AT	LK	PT	UW	INC	DI	CC	

CC — Command Code

CC = 00 => Channel Disabled.

CC = 01 => Search

CC = 10 => Data Transfer

CC = 11 => Data Transfer and Search

DI — Direct/Indirect Transfers

DI = 0 => Indirect Transfers

DI = 1 => Direct Transfers

INC — Inclusive/Exclusive Search

INC = 0 => Exclusive Search

INC = 1 => Inclusive Search

UW — Search type

UW = 0 => Search UNTIL

UW = 1 => Search WHILE

PT — Priority type

PT = 0 => Fixed

PT = 1 => Variable

LK — Priority lock

LK = 0 => Priority Unlocked

LK = 1 => Priority Locked

3.0 Architectural Description (Continued)

AT — Auto transfer
AT = 0 => Auto Transfer Disabled
AT = 1 => Auto Transfer Enabled

At Reset, the CC bits in COM(L) are cleared, disabling the channel.

Note: The CC bits can be cleared by software during an indirect data transfer to stop the transfer. This, however, should not be done during direct data transfers. See section 3.3.3.

COM(M) - Command Register (Middle-Byte)

7	6	5	4	3	2	1	0
DD	DW	DL	DT	SD	SW	SL	ST

ST — Source Type
ST = 0 => I/O Device
ST = 1 => Memory

SL — Source Location
(Effective only in the remote configuration)
SL = 0 => Local
SL = 1 => Remote

SW — Source Width
SW = 0 => 8 Bits
SW = 1 => 16 Bits

SD — Source Direction
SD = 0 => Up
SD = 1 => Down

DT — Destination Type
DT = 0 => I/O Device
SD = 1 => Memory

DL — Destination Location
(Effective only in the remote configuration)
DL = 0 => Local
DL = 1 => Remote

DW — Destination Width
DW = 0 => 8 Bits
DW = 1 => 16 Bits

DD — Destination Direction.
DD = 0 => Up
DD = 1 => Down

COM(H) - Command Register (High-Byte)

7	6	5	4	3	2	1	0
HLI	MNI	TCI	AMN		ATC	DM	X

X — Reserved. (Should be set to 0)

TM — Transfer Mode
DM = 0 => Single Transfer
DM = 1 => Burst Transfer

ATC — Action after Transfer Complete
ATC = 0 => Disable Channel
ATC = 1 => Load Control Values and Parameters from Complementary Channel and Continue

AMN — Action after Match/No Match
AMN = 00 => Disable Channel
AMN = 01 => Continue
AMN = 10 => Load Control Values from Complementary Channel and Continue
AMN = 11 => Load Control Values and Parameters from Complementary Channel and Continue

TCI — Interrupt Mask on "Transfer Complete"
TCI = 0 => No Interrupt
TCI = 1 => Interrupt

MNI — Interrupt Mask on "Match/No Match"
MNI = 0 => No Interrupt
MNI = 1 => Interrupt

HLI — Interrupt Mask on "Channel Halted"
HLI = 0 => No Interrupt
HLI = 1 => Interrupt

3.2.2 SRCH — Search Register

This 8-bit register holds the value to be compared with the data transferred during the channel operation.

3.2.3 MSK — Mask Register

The 8-bit mask register determines which bits of the transferred data are compared with corresponding search register bits. If a mask register bit is set to 0, the corresponding search register bit is ignored in the compare operation. At reset, all the MSK bits are set to 0.

3.3 PARAMETER REGISTERS

Each channel has three parameter registers, consisting of a 24-bit source address register, a 24-bit destination address register and a 16-bit block length register.

3.3.1 SRC — Source Address Register

The source address register points to the physical address of the data source. When the data source is an I/O device, the register does not change during the transfer operation. When the data source is memory, the register is incremented or decremented by either one or two after each transfer.

3.3.2 DST — Destination Address Register

The destination address register points to the physical address of the data destination. When the data destination is an I/O device, the register does not change during the transfer operation. When the data destination is memory, the register is incremented or decremented by either one or two after each transfer.

3.3.3 LNGT — Block Length Register

The block length register holds the number of bytes in the block to be transferred. It is decremented by either one or two after each transfer.

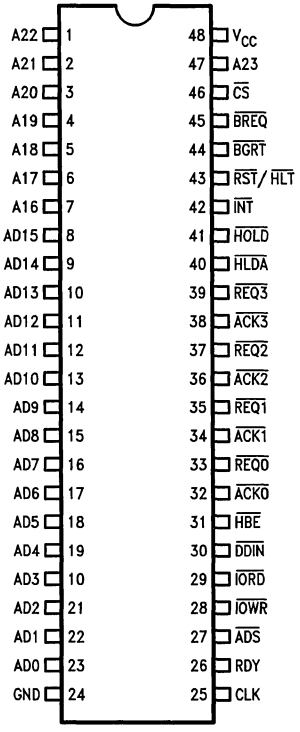
Note: A direct data transfer can be stopped by writing zeroes into the LNGT register. The number of bytes transferred can be determined in this case, from the value of either the SRC or the DST register.

4.0 Device Specifications

4.1. NS32203 PIN DESCRIPTIONS

The following is a brief description of all NS32203 pins. The descriptions reference portions of the Functional Description, Section 2.0.

Connection Diagram



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Top View

FIGURE 4-1. NS32203 Dual-In-Line Package

Order Number NS32203D or NS32203N
See NS Package Number D48A or N48A

4.1.1 SUPPLIES

Power (V_{CC}): +5V positive supply.

Ground (GND): Ground reference for on-chip logic.

4.1.2 INPUT SIGNALS

Reset/Halt ($\overline{RST}/\overline{HLT}$): Active low. If held active for 1 or 2 clock cycles and released, this signal halts the DMAC operation on the active channel. If held longer, it resets the DMAC. Section 2.1.

Chip Select ($\overline{CS}$): When low, the device is selected, enabling CPU access to the DMAC internal registers.

Ready (RDY): Active high. When inactive, the DMA Controller extends the current bus cycle for synchronization with slow memory or peripherals. Upon detecting RDY active, the DMAC terminates the bus cycle.

Channel Request 0–3 ($\overline{REQ0}$ - $\overline{REQ3}$): Active low. These lines are used by peripheral devices to request DMAC service.

Bus Request ($\overline{BREQ}$): Used only in the remote configuration. This signal, when asserted, forces the DMAC to stop transferring data and to release the bus. It must be activated by the CPU before any CPU access to the remote bus is performed. In the local configuration this signal should be connected to V_{CC} via a 4.7k resistor. Section 2.4.

Hold Acknowledge ($\overline{HLDA}$): Active low. When asserted, indicates that control of the system bus has been relinquished by the current bus master and the DMAC can take control of the bus.

Clock (CLK): Clock signal supplied by the CTTL output of the NS32201 TCU.

4.1.3 OUTPUT SIGNALS

Address Bits 16–23 (A16–A23): Most significant 8 bits of the address bus.

Hold Request ($\overline{HOLD}$): Active low. Used by the DMAC to request control of the system bus.

Channel Acknowledge 0–3 ($\overline{ACK0}$ - $\overline{ACK3}$): These lines indicate that a channel is active. When a channel's request is honored, the corresponding acknowledge line is activated to notify the peripheral device that it has been selected for a transfer cycle. Section 2.2.2.

Bus Grant ($\overline{BGRT}$): Used only in the remote configuration. This signal is used by the DMAC to inform the CPU that the remote bus has been relinquished by the DMAC and can be accessed by the CPU. Section 2.4.

I/O Read ($\overline{IORD}$): Active low. Enables data to be read from a peripheral device. Section 2.2.2.

I/O Write ($\overline{IOWR}$): Active low. Enables data to be written to a peripheral device. Section 2.2.2.

Interrupt ($\overline{INT}$): Active low. Used to generate an interrupt request when a programmed condition has occurred. Section 2.9.

4.1.4 INPUT/OUTPUT SIGNALS

Address/Data 0–15 (AD0–AD15): Multiplexed Address/Data bus lines. Also used by the CPU to access the DMAC internal registers.

High Byte Enable ($\overline{HBE}$): Active low. Enables data transfers on the most significant byte of the data bus.

Address Strobe ($\overline{ADS}$): Active low. Controls address latches and indicates the start of a bus cycle.

Data Direction in ($\overline{DDIN}$): Active low. Status signal indicating the direction of data flow in the current bus cycle.

4.0 Device Specifications (Continued)

4.2 ABSOLUTE MAXIMUM RATINGS

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Temperature Under Bias	0°C to +70°C
Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to GND	−0.5V to +7V
Power Dissipation	1.1 Watt

Note: *Absolute maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended; operation should be limited to those conditions specified under Electrical Characteristics.*

4.3 ELECTRICAL CHARACTERISTICS T_A = 0 to +70°C, V_{CC} = 5V ±5%, GND = 0V

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High Level Input Voltage		2.0		V_{CC} + 0.5	V
V_{IL}	Low Level Input Voltage		−0.5		0.8	V
V_{OH}	High Level Output Voltage	I_{OH} = −400 μA	2.4			V
V_{OL}	Low Level Output Voltage	I_{OL} = 2 mA			0.45	V
I_I	Input Load Current	0 < V_{IN} ≤ V_{CC}	−20		20	μA
I_L	Leakage Current Output and I/O Pins in TRI-STATE/Input Mode	0.4 ≤ V_{IN} ≤ V_{CC}	−20		20	μA
I_{CC}	Active Supply Current	I_{OUT} = 0, T_A = 25°C		180	300	mA

4.4 SWITCHING CHARACTERISTICS

4.4.1 Definitions

All the timing specifications given in this section refer to 0.8V and 2.0V on all the input and output signals as illustrated in *Figures 4-2* and *4-3*, unless specifically stated otherwise.

ABBREVIATIONS:

L.E. — leading edge R.E. — rising edge
T.E. — trailing edge F.E. — falling edge

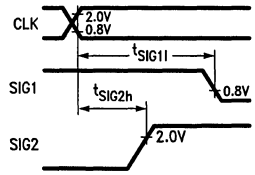

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FIGURE 4-2. Timing Specification Standard (Signal Valid after Clock Edge)

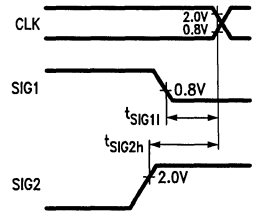

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FIGURE 4-3. Timing Specification Standard (Signal Valid before Clock Edge)

4.0 Device Specifications (Continued)

4.4.2 Timing Tables

4.4.2.1 Output Signals: Internal Propagation Delays, NS32203-10

Maximum Times Assume Capacitive Loading of 100 pF.

Name	Figure	Description	Reference/ Conditions	NS32203-10		Units
				Min	Max	
t_{ALv}	4-7	Address Bits 0–15 Valid	After R.E., CLK T1		50	ns
t_{ALh}	4-9	Address Bits 0–15 Hold Time	After R.E., CLK T2	5		ns
t_{AHv}	4-7	Address Bits 16–23 Valid	After R.E., CLK T1		50	ns
t_{AHh}	4-7	Address Bits 16–23 Hold	After R.E., CLK T1 or Ti	5		ns
t_{ALADSs}	4-8	Address Bits 0–15 Set Up	Before $\overline{ADS}$ T.E.	25		ns
t_{AHADSs}	4-8	Address Bits 16–23 Set Up	Before $\overline{ADS}$ T.E.	25		ns
t_{ALADSh}	4-9	Address Bits 0–15 Hold Time	After $\overline{ADS}$ T.E.	15		μs
t_{ALf}	4-8	Address Bits 0–15 Floating	After R.E., CLK T2		25	ns
t_{Dv}	4-7	Data Valid (Write Cycle)	After R.E., CLK T2		50	ns
t_{Dh}	4-7	Data Hold (Write Cycle)	After R.E., CLK T1 or Ti	0		ns
t_{DOv}	4-5	Data Valid (Reading DMAC Registers)	After R.E., CLK T3		50	
t_{DOh}	4-5	Data Hold (Reading DMAC Registers)	After R.E., CLK T4	10		
t_{HBEv}	4-7	$\overline{HBE}$ Signal Valid	After R.E., CLK T1		50	ns
t_{HBEh}	4-7	$\overline{HBE}$ Signal Hold	After R.E., CLK T1 or Ti	0		ns
t_{DDINv}	4-8	$\overline{DDIN}$ Signal Valid	After R.E., CLK T1		65	ns
t_{DDINh}	4-8	$\overline{DDIN}$ Signal Hold	After R.E., CLK T1 or Ti	0		ns
t_{ADSa}	4-7	$\overline{ADS}$ Signal Active	After R.E., CLK T1		35	ns
t_{ADSia}	4-7	$\overline{ADS}$ Signal Inactive	After R.E., CLK T1		40	ns
t_{ADSw}	4-7	$\overline{ADS}$ Pulse Width	at 0.8V (Both Edges)	30		ns
t_{ALz}	4-12. 4-13	AD0–AD15 Floating	After R.E., CLK Ti		55	ns
t_{AHz}	4-12, 4-13	A16–A23 Floating	After R.E., CLK Ti		55	ns
t_{ADSz}	4-12, 4-13	$\overline{ADS}$ Floating	After R.E., CLK Ti		55	ns
t_{HBEz}	4-12, 4-13	$\overline{HBE}$ Floating	After R.E., CLK Ti		55	ns
t_{DDINz}	4-12, 4-13	$\overline{DDIN}$ Floating	After R.E., CLK Ti		55	ns
t_{HLDa}	4-11	$\overline{HOLD}$ Signal Active	After R.E., CLK Ti		50	ns
t_{HLDia}	4-12	$\overline{HOLD}$ Signal Inactive	After R.E., CLK Ti or T4		50	ns
t_{INTa}	4-19, 4-21	$\overline{INT}$ Signal Active	After R.E., CLK Ti		40	ns
t_{ACKa}	4-16, 4-17, 4-7	$\overline{ACKn}$ Signal Active	After R.E., CLK T1		50	ns
t_{ACKia}	4-16, 4-17, 4-7	$\overline{ACKn}$ Signal Inactive	After F.E., CLK T4		35	ns

4.0 Device Specifications (Continued)

Name	Figure	Description	Reference/ Conditions	NS32203-10		Units
				Min	Max	
t_{BGRTa}	4-13	$\overline{BGRT}$ Signal Active	After R.E., CLK		65	ns
t_{BGRTia}	4-14	$\overline{BGRT}$ Signal Inactive	After R.E., CLK		65	ns
t_{IORDa}	4-8, 4-9	$\overline{IORD}$ Active	After R.E., CLK T2		40	ns
t_{IORDia}	4-8	$\overline{IORD}$ Inactive (During Indirect Transfers)	After R.E., CLK T4		40	ns
t_{IORDia}	4-9	$\overline{IORD}$ Inactive (During Direct Transfers)	After F.E., CLK T4		40	ns
t_{IOWRa}	4-7, 4-10	$\overline{IOWR}$ Active	After R.E., CLK T2		40	ns
t_{IOWRia}	4-7	$\overline{IOWR}$ Inactive (During Indirect Transfers)	After R.E., CLK T4		40	ns
$t_{IOWRdia}$	4-10	$\overline{IOWR}$ Inactive (During Direct Transfers)	After F.E., CLK T3		40	ns
4.4.2.2 Input Signal Requirements: NS32203-10						
t_{PWR}	4-22	Power Stable to $\overline{RST}/\overline{HLT}$ R.E.	After V_{CC} Reaches 4.75V	50		μs
t_{RSTw}	4-23	$\overline{RST}/\overline{HLT}$ Pulse Width (Resetting the DMAC)	at 0.8V (Both Edges)	64		tCp
t_{RSTs}	4-24	$\overline{RST}/\overline{HLT}$ Set Up Time (Resetting the DMAC)	Before F.E., CLK	15		ns
t_{HLTs}	4-18	$\overline{RST}/\overline{HLT}$ Setup Time (Halting a DMAC Transfer)	Before R.E., CLK T3	25		ns
t_{HLTh}	4-19	$\overline{RST}/\overline{HLT}$ Hold Time (Halting a DMAC Transfer)	After R.E., CLK T4	10		ns
t_{DIs}	4-6	Data in Setup Time	Before R.E., CLK T3	15		ns
t_{DIh}	4-6	Data in Hold	After R.E., CLK T4	3		ns
t_{DIs}	4-6	Data in Setup Time (Writing to DMAC Registers)	After R.E., CLK T3	15		ns
t_{DIh}	4-6	Data in Hold (Writing to DMAC Registers)	After R.E., CLK T4	3		ns
t_{HLDAs}	4-11, 4-12	$\overline{HOLDA}$ Setup Time	Before R.E., CLK	25		ns
t_{HLDAh}	4-11	$\overline{HLDA}$ Hold Time	After R.E., CLK	10		ns
t_{RDYs}	4-15	RDY Setup Time	Before R.E., CLK T2 or T3	20		ns
t_{RDYh}	4-15	RDY Hold Time	After R.E., CLK T3	5		ns
t_{REQs}	4-16, 4-17	$\overline{REQn}$ Setup Time	Before R.E., CLK	50		ns
t_{REQh}	4-16, 4-17	$\overline{REQn}$ Hold Time	After R.E., CLK	10		
t_{BREQs}	4-13	$\overline{BREQ}$ Setup Time	Before R.E., CLK	25		ns

4.0 Device Specifications (Continued)

Name	Figure	Description	Reference/ Conditions	NS32203-10		Units
				Min	Max	
t_{BREQh}	4-13	$\overline{BREQ}$ Hold Time	After R.E., CLK	10		ns
$t_{ALADSis}$	4-6	Address Bits 0–5 Setup	Before $\overline{ADS}$ T.E.	20		ns
$t_{ALADSih}$	4-6	Address Bits 0–5 Hold	After $\overline{ADS}$ T.E.	20		ns
t_{HBEs}	4-6	$\overline{HBE}$ Setup Time	Before R.E., CLK T1	10		ns
t_{HBEih}	4-6	$\overline{HBE}$ Hold Time	After R.E., CLK T4	40		ns
t_{ADSs}	4-6	$\overline{ADS}$ L.E. Setup Time	Before R.E., CLK T1	40		ns
t_{ADSiw}	4-6	$\overline{ADS}$ Pulse Width	$\overline{ADS}$ L.E. to $\overline{ADS}$ T.E.	35		ns
t_{CSs}	4-6	$\overline{CS}$ Setup Time	Before R.E., CLK T1	15		ns
t_{CSh}	4-6	$\overline{CS}$ Hold Time	After R.E., CLK T4	40		ns
t_{DDINs}	4-6	$\overline{DDIN}$ Setup Time	Before R.E., CLK T2	30		ns
t_{DDINh}	4-6	$\overline{DDIN}$ Hold Time	After R.E., CLK T4	40		ns

4.4.2.3 Clocking Requirements: NS32203-10

Name	Figure	Description	Reference/ Conditions	NS32203-10		Units
				Min	Max	
t_{CLKh}	4-4	Clock High Time	At 2.0V (Both Edges)	42		ns
t_{CLK1}	4-4	Clock Low Time	At 0.8V (Both Edges)	42		ns
t_{CLKp}	4-4	Clock Period	R.E., CLK to Next R.E. CLK	100		ns

4.4.3 Timing Diagrams

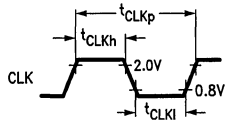

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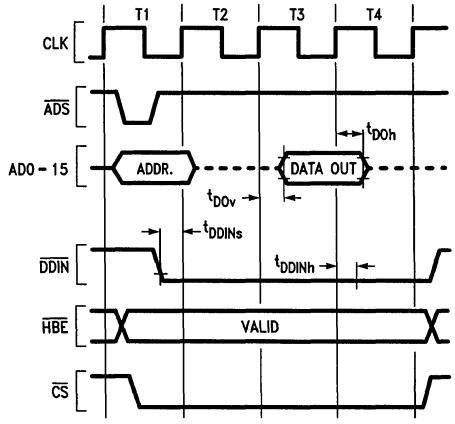
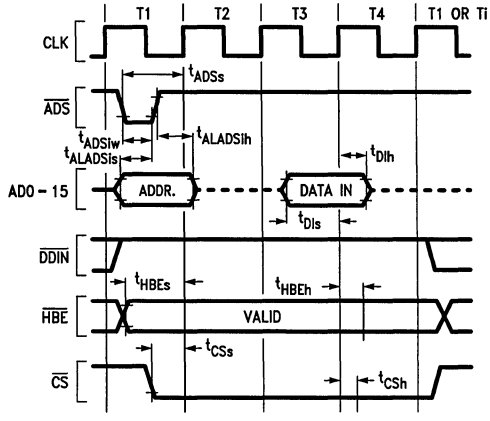
FIGURE 4-4. Clock Timing

4.0 Device Specifications (Continued)



TL/EE/8701-16

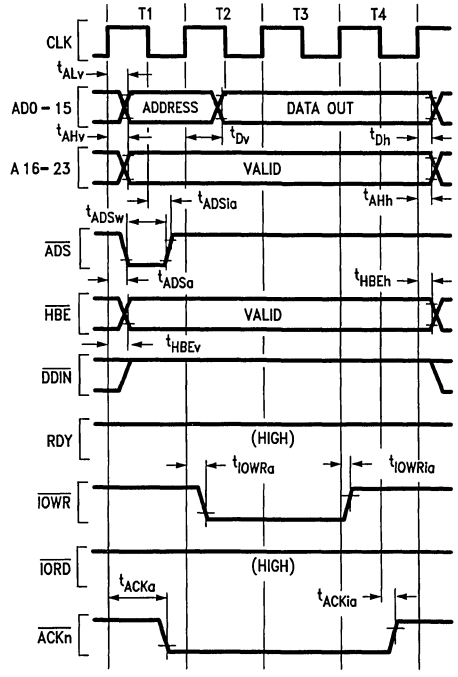
FIGURE 4-5. Read from DMAC Registers



TL/EE/8701-15

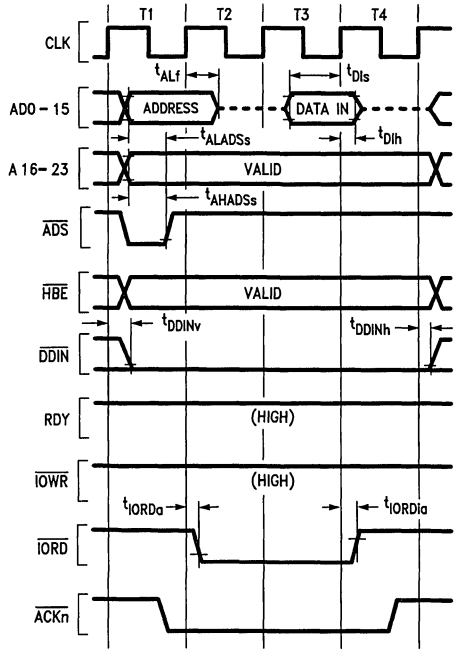
FIGURE 4-6. Write to DMAC Registers

4.0 Device Specifications (Continued)



TL/EE/8701–18

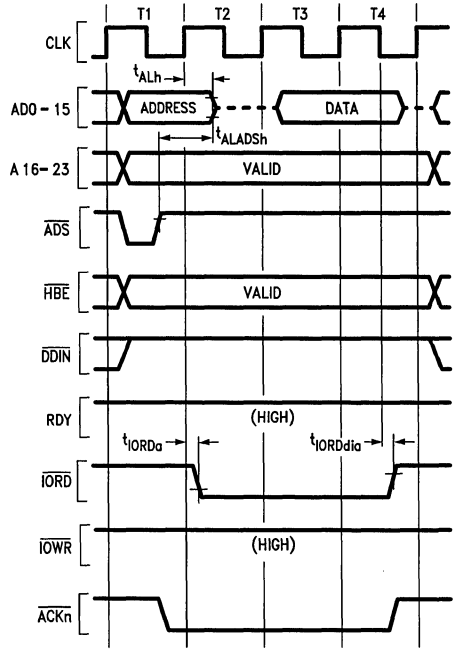
FIGURE 4-7. Indirect Write Cycle



TL/EE/8701–19

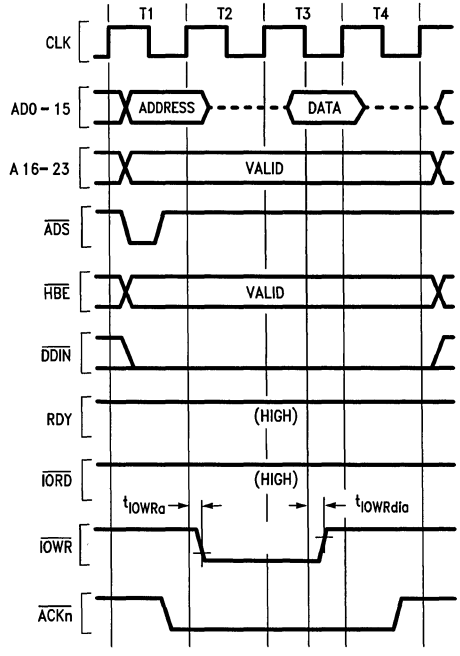
FIGURE 4-8. Indirect Read Cycle

4.0 Device Specifications (Continued)



TL/EE/8701-20

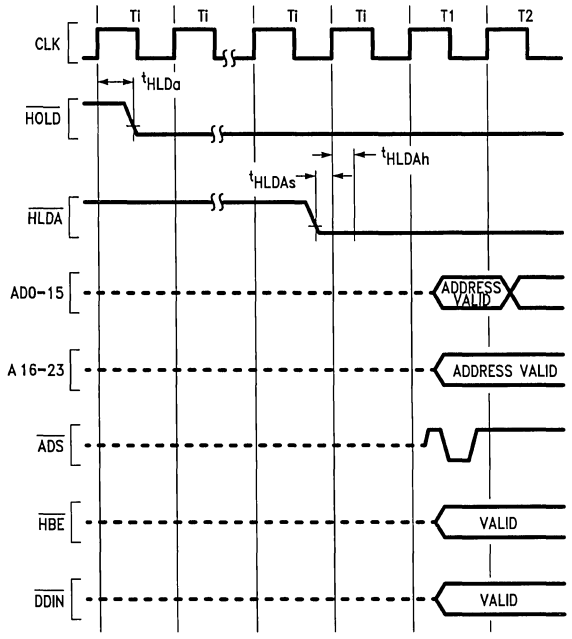
FIGURE 4-9. Direct I/O to Memory Transfer



TL/EE/8701-21

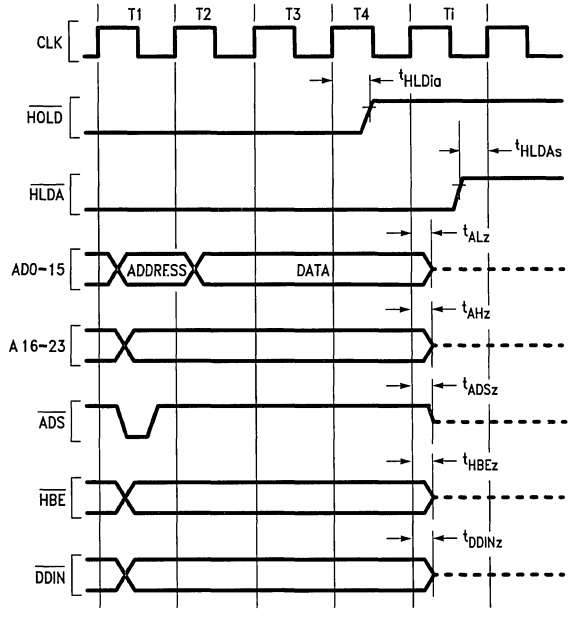
FIGURE 4-10. Direct Memory to I/O Transfer

4.0 Device Specifications (Continued)



TL/EE/8701-22

FIGURE 4-11. HOLD/HOLDA Sequence Start



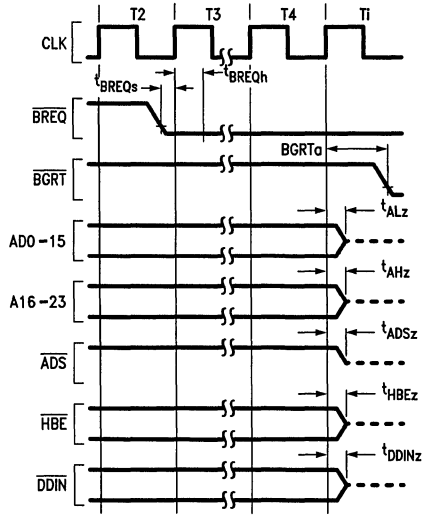
TL/EE/8701-23

FIGURE 4-12. HOLD/HOLDA Sequence End

Note 1: DMAC in local configuration.

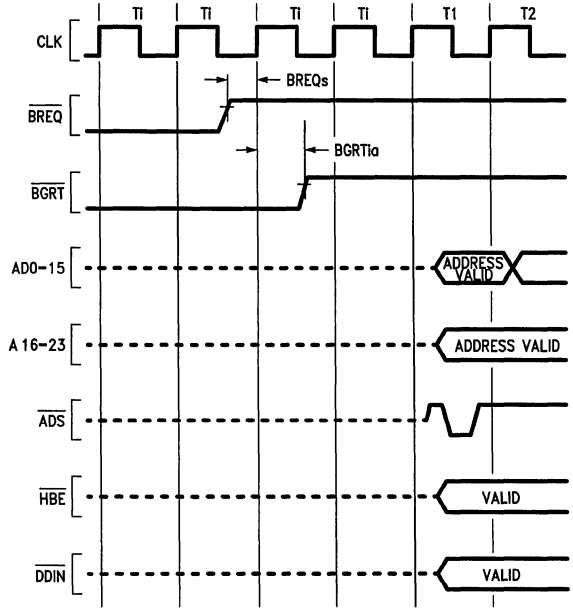
Note 2: The HOLD/HOLDA sequence shown above is related to the single transfer mode.
In burst transfer mode HOLD is deactivated two cycles later.

4.0 Device Specifications (Continued)



TL/EE/8701-24

FIGURE 4-13. Bus Request/Grant Sequence Start



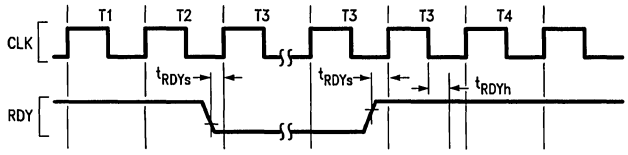
TL/EE/8701-25

FIGURE 4-14. Bus Request/Grant Sequence End

Note 1: DMAC in remote configuration.

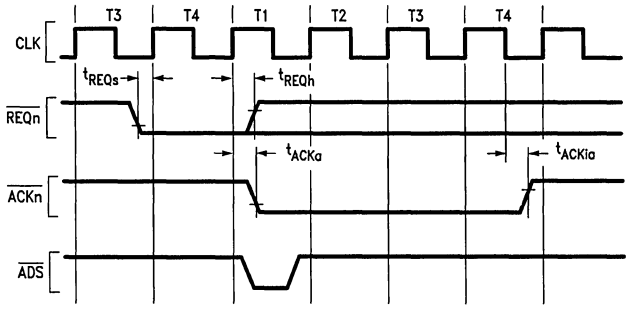
Note 2: If $\overline{\text{BREQ}}$ is asserted in the middle of a DMAC transfer, the transfer will always be completed.

4.0 Device Specifications (Continued)



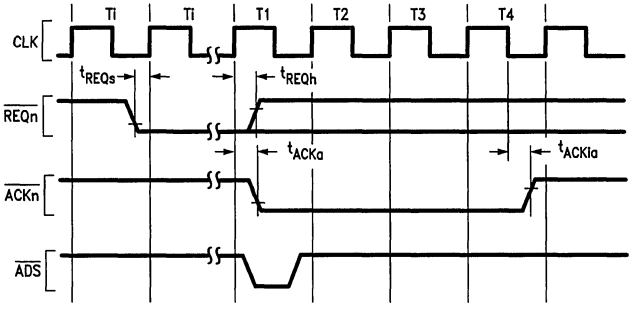
TL/EE/8701-26

FIGURE 4-15. Ready Sampling



TL/EE/8701-27

FIGURE 4-16. REQn/ACKn Sequence (DMAC Initially Not Idle)

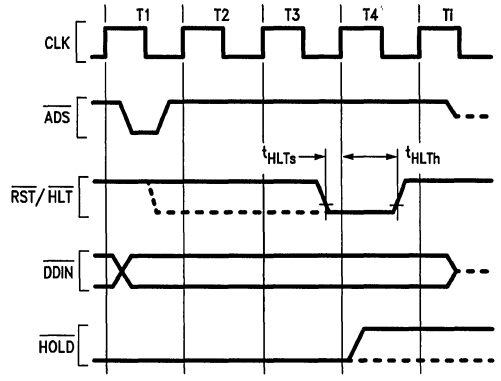


TL/EE/8701-28

FIGURE 4-17. REQn/ACKn Sequence (DMAC Initially Idle)

4

4.0 Device Specifications (Continued)

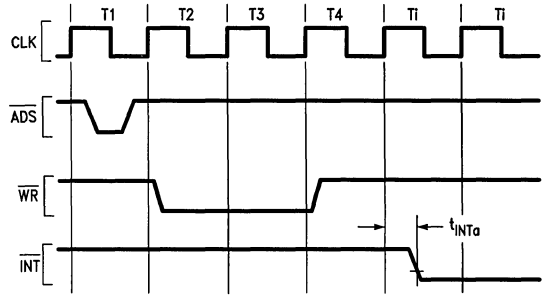


TL/EE/8701-29

FIGURE 4-18. Halted Cycle

Note 1: Halt may occur in previous T-States. It must be applied for 1 or 2 clock cycles.

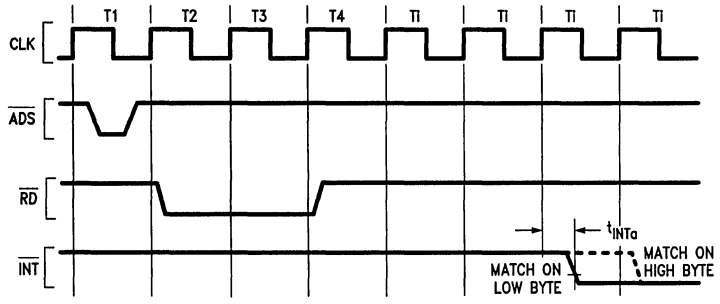
Note 2: If BREQ is asserted in the middle of a DMAC transfer, the transfer will always be completed.



TL/EE/8701-30

FIGURE 4-19. Interrupt on Transfer Complete

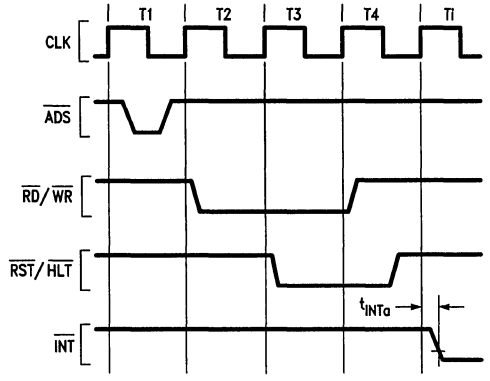
4.0 Device Specifications (Continued)



TL/EE/8701-31

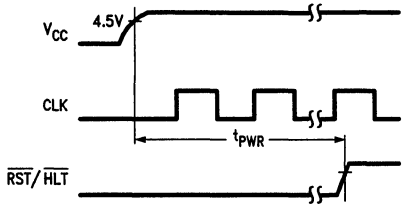
FIGURE 4-20. Interrupt on Match/No Match

Note: If inclusive search is specified a write cycle is performed before $\overline{INT}$ is activated.



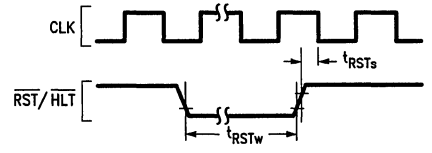
TL/EE/8701-32

FIGURE 4-21. Interrupt on Halt



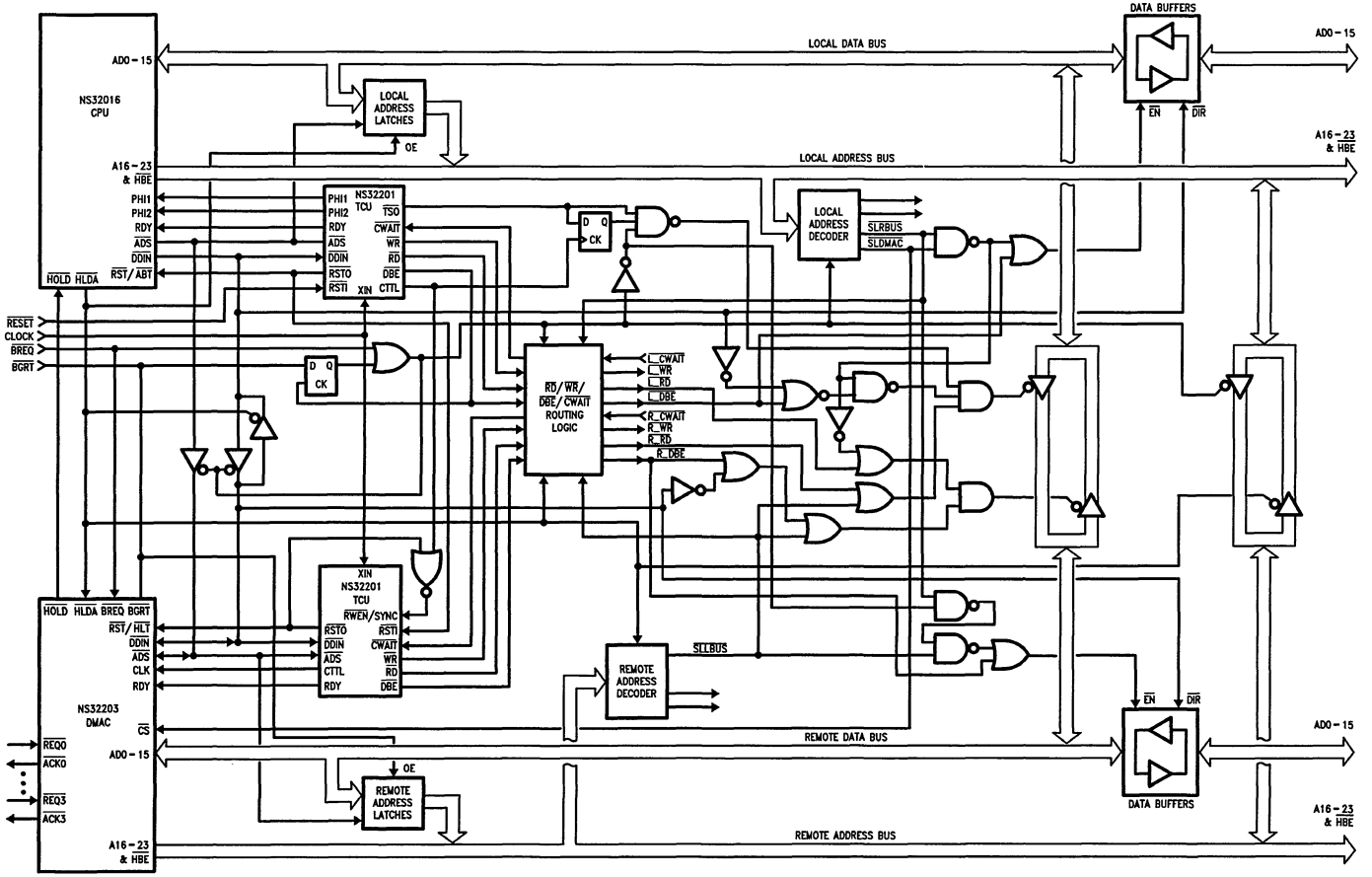
TL/EE/8701-33

FIGURE 4-22. Power on Reset



TL/EE/8701-34

FIGURE 4-23. Non Power on Reset



TL/EE/8701-35

FIGURE A-1. NS32203 Interconnections in Remote Configuration.

Note: This logic does not support direct (flyby) DMAC transfers.

Section 5

Board Level Products

Section 5 Contents

National Semiconductor

VME532
High Performance 32-Bit CPU VME Board with Cache, Memory Management and Floating Point

Features

- NS32532 Central Processing Unit (CPU) with internal cache and on-chip Memory Management Unit (MMU)
- NS32381 Floating Point Unit (FPU)
- Optional 32580 FPC+ Weitek WTL3164
- NS32202 Interrupt Control Unit (ICU)
- 20, 25 or 30 MHz operating frequency
- Cache—64 kbytes of direct-mapped zero wait-state cache
- Conforms to all VME Revision C.1 specifications
- Supports multiprocessing system applications
- 4–16 Mbytes of on-board Dual Port DRAM with parity, expandable to 256 Mbytes of cacheable address space over the VME bus
- 64 kbytes of EPROM in one socket
- Two RS-232C serial ports (2681 DUART) with adjustable baud rate
- MON532 monitor firmware with power on diagnostics

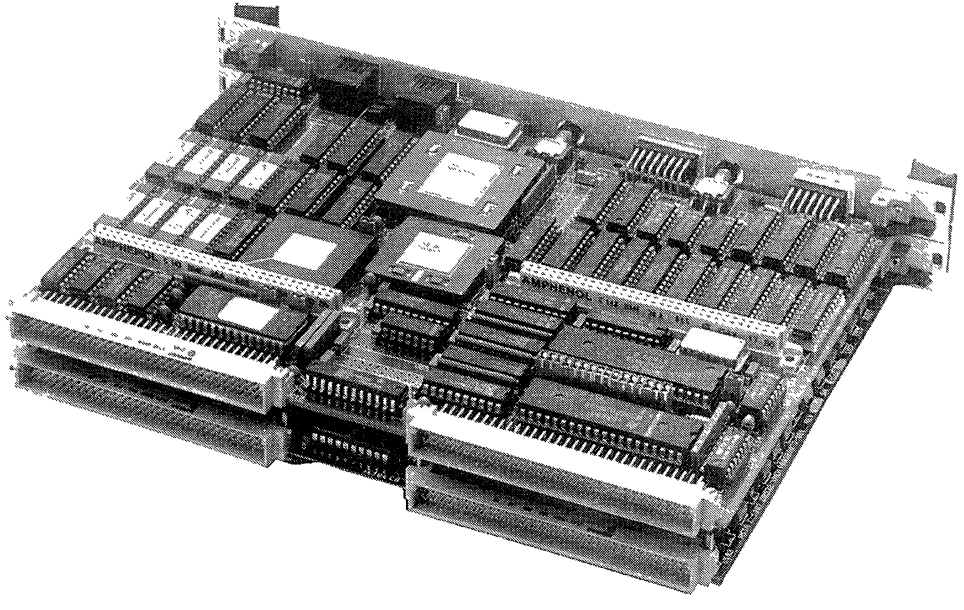
Product Overview

The VME532 is National Semiconductor's VME based board featuring the high-end Series 32000® family cluster. The cluster consists of the NS32532 CPU with on-chip Memory Management Unit, and the NS32381 Floating Point Unit (FPU).

Available in 20, 25 and 30 MHz operating speeds, the 2-board set includes a 64 kbyte external cache with an average hit rate of over 90%. Expandable to ½ gigabyte of memory, and with up to 16 Mbytes of DRAM on-board, the VME532 provides cacheable memory address range of up to 256 Mbytes.

The VME532 is a powerful CPU designed for systems demanding high performance in any environment, including UNIX®, real time operating systems, e.g., VRTX32®, and multiprocessing.

The VME532 may also be used to evaluate the NS32532 and NS32381 architecture, instruction set, timing, and performance. In addition, the board provides a native debug and execution environment for programs developed on a host computer and is compatible with National's GNX™ software package.



TL/EE/9380–1

FIGURE 1

Hardware Description

CENTRAL PROCESSING UNIT

The NS32532 microprocessor is National Semiconductor's most powerful Central Processing Unit (CPU) that is compatible with other members of the Series 32000 family. The NS32532 CPU contains an on-chip Memory Management Unit (MMU) with a 64-entry translation buffer and is software compatible with the NS32382 MMU.

Features of the NS32532 include 4 gigabytes of addressing capability, a 512-byte instruction cache, a 1024-byte data cache, 4-stage instruction pipeline, and dynamic bus sizing.

FLOATING POINT UNIT

The NS32381 Floating Point Unit (FPU) is a second generation CMOS, floating point slave processor, conforming to IEEE standard 754–1985 for binary floating point arithmetic. Functioning in a tightly coupled slave configuration with the NS32532 CPU, the NS32381 FPU operates significantly faster than the NS32081 FPU. Additionally, the NS32381 and has an expanded floating point instruction repertoire, while preserving upward compatability. The NS32381 FPU operates on 2 floating point data types: single-precision (32-bit) and double-precision (64-bit).

OPTIONAL FLOATING POINT ACCELERATOR

The VME532 is also available with a higher-performance (15 MFLOPS peak) floating point alternative. This floating point accelerator comprises the NS32580 Floating Point Controller (FPC) and Weitek WTL3164 Floating Point Data Path to create a compatible replacement for the standard NS32381 FPU.

FOUR-LEVEL MEMORY HIERARCHY

CPU Cache

The VME532 employs a 4-level memory hierarchy design. The first level includes the 512-byte instruction cache and the 1-kbyte data cache, integrated within the NS32532 CPU. This provides the CPU with an 80% internal cache hit rate minimizing external memory accesses.

External Cache

The second level memory hierarchy structure is composed of a 64-kbyte direct-mapped, zero wait-state external cache, allowing up to 256 Mbytes of cacheable address space. With the addition of the external cache, the overall cache hit rate increases to over 90%, allowing the NS32532 CPU to nearly operate at full performance. In case a cache miss occurs, no time is wasted accessing local or external memory because memory accesses occur simultaneously with each cache access and is aborted upon a cache hit.

The external cache is composed of very high speed SRAMs. The data portion of the cache is arranged as an array of 16k x 32 bits and is used to store 64 kbytes of data. The tag portion of memory is a 4k x 16-bit array. Each entry contains 12 bits of addressing information, 1 VALID bit, and 3 spare bits. The tag is integrated with high speed compare logic to determine cache hit and miss.

Local Memory

Level three is the local dual-port parity-checking memory consisting of 4 Mbytes, expandable to 16 Mbytes, of DRAM. Accessing the third level through an independent local bus reduces traffic along the common system bus. The local dual-port memory allows access through the system bus, as well as the local bus. The path through the system bus serves to simplify the incorporation of peripheral devices by transferring I/O directly to local memory.

Global Memory

The fourth level of the memory hierarchy is the global memory accessible to each processor through the system bus. Each processor's local memory can serve as global memory to other processors in the system. In addition, memory modules not local to any processor, can be used as global memory by all microprocessors in the system. The cacheable address space is 256 Mbytes, of which 4 or 16 Mbytes is local on-board memory.

THE GATEWAY

In a typical CPU, more operations involve read cycles than write cycles to local memory. The efficiency of the internal cache of the NS32532 CPU together with the performance of the external cache creates an effective hit rate in excess of 90%, causing more write cycles than read cycles to memory to occur. Since RAM access may cause a bottleneck in CPU performance, due to frequent write cycles, the VME532 incorporates two custom gate array chips that make up the Gateway circuitry. The Gateway is a 72-bit by 8 location deep write FIFO and read buffer allowing the CPU to write to main memory without wait-states. Analysis indicates an 8-entry deep FIFO is sufficient to buffer, without filling up, 99% of all memory write operations, improving the performance of the VME532.

MULTIPROCESSING

Designed with multiprocessor applications in mind, the VME532 will couple to a total of 16 processors in a separate-memory, shared-bus architecture. The VME532 provides the following multiprocessing features:

- CPU number switch. This thumbwheel switch on the VME532 enables users to assign unique CPU identification numbers, ranging from 0 to 15 for each CPU in the system.
- Local memory can be accessed by other VME masters, including other CPUs. The memory of each CPU is mapped into a unique space of the VME address.
- VME memory is shared among all bus masters, allowing "mailbox" communication.
- Bus Watcher. The bus watcher circuitry is responsible for coherency between VME and cache-memory entries. The bus watcher traces the activity on the VME bus. Whenever cacheable memory is written by one of the other VME masters, the bus watcher latches the address of the memory, and a bus watch request signal is sent to the cache memory controller. When an address match occurs, the cache invalidates the entry. The bus watcher's FIFO of 8 entries prevents the loss of invalidation requests during heavy VME bus traffic.
- Inter-processor interrupts. In addition to the normal VME interrupt system, the VME532 allows other processors to communicate with the VME532 using the inter-processor interrupts. Sixteen address ranges are allocated for this special purpose on the VME532.

INTERRUPTS

Included with the VME532 is National Semiconductor's NS32202 Interrupt Control Unit (ICU). The 16 channel ICU handles all on-board interrupts, all seven levels of VME interrupts, and inter-processor interrupts. The interrupts are individually maskable, and the priority assignment may be customized to suit the needs of the user.

SERIAL I/O

A 2681 Dual-UART provides the user with two serial communication ports to enable communication with a terminal and host processor, with RS-232C compatibility. The internal timer/counter of the DUART can be used as a watchdog timer or real-time clock. The serial ports are provided with Telco connectors, and DB-25 adapters for use as DTE or DCE.

SOFTWARE OPTIONS

MON532 (monitor) with diagnostics is included with the VME532. The VME532 supports National's GENIX® V.3*, and optimizing compilers for Ada, C, Pascal, Modula-2, and FORTRAN. The board also supports VRTX32 for real time applications.

VME SPECIFICATIONS

Master: A32:D32, UAT, RMW, IH7, ROR, RWD

Slave: A32:D32, UAT, BLT, RMW, ADO, BERR

Syscon: BR(0–3), (PRI, RRS, dyn.), BTO 1.6–12.8 dyn.), IACK, SYSRST, SYSCLK

ORDERING INFORMATION

NSV-V532A-KF20 VME532 Development Kit, 20 mHz, 32381 FPU

NSV-V532A-KF25 VME532 Development Kit, 25 mHz, 32381 FPU

NSV-V532A-KF30 VME532 Development Kit, 30 mHz, 32381 FPU

NSV-V532A-KW20 VME532 Development Kit, 20 mHz, 32580/WTL3164 FPU

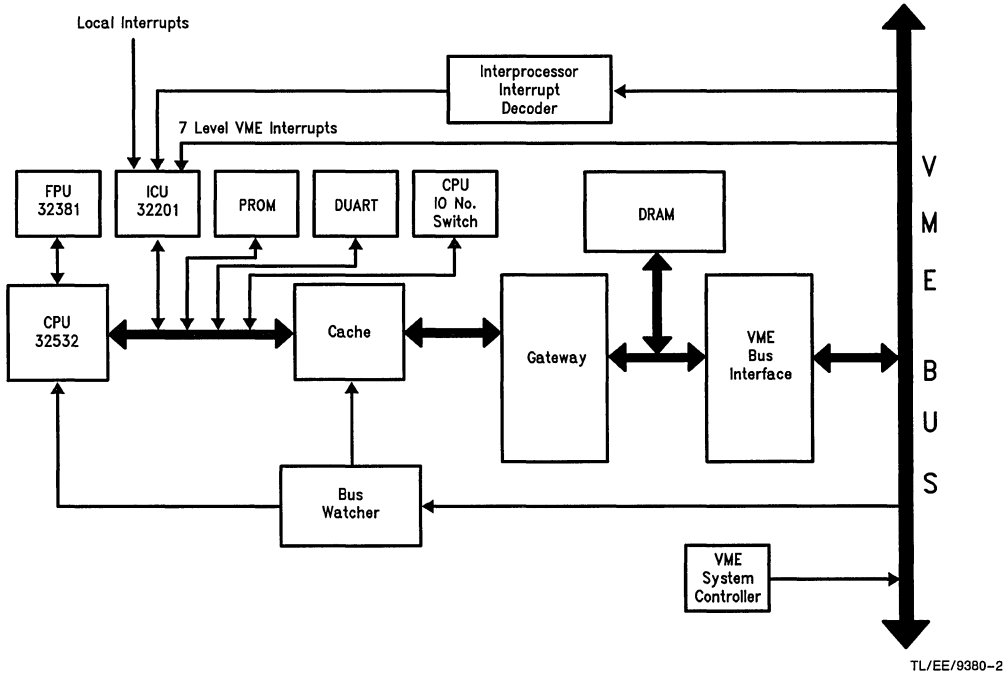
NSV-V532A-KW25 VME532 Development Kit, 25 mHz, 32580/WTL3164 FPU

NSV-V532A-KW30 VME532 Development Kit, 30 mHz, 32580/WTL3164 FPU

NSV-VXM532A-12M 12 Mbyte Local Memory Expansion (20, 25, or 30 mHz)

*Derived from UNIX System V.3

VME532 Block Diagram



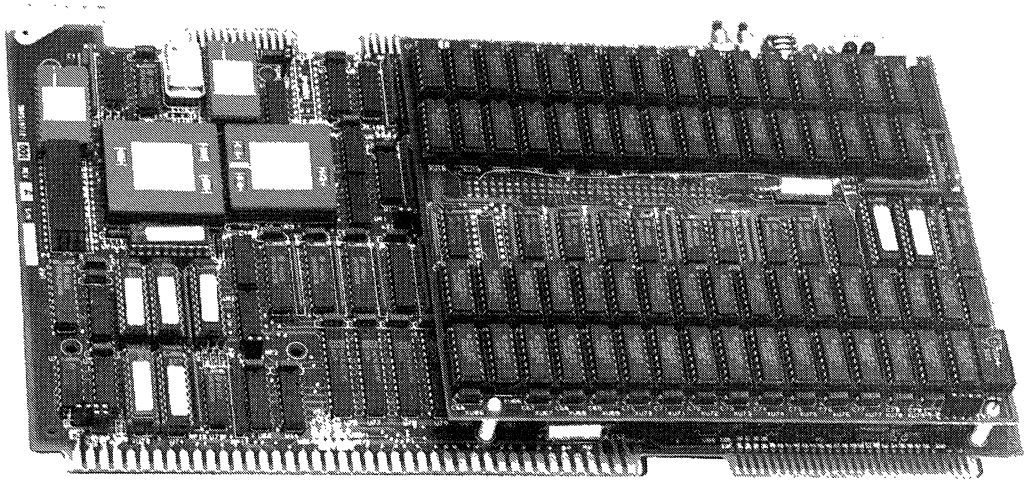
TL/EE/9380–2

FIGURE 2

National Semiconductor

ADVANCED INFORMATION

DB332-PLUS Development Board



TL/C/9249–1

- **Includes the Series 32000® Microprocessor Family**
  - — NS32332 CPU
  - — NS32382 MMU
  - — NS32C201 TCU
  - — NS32081 FPU
  - — NS32202 ICU
- **MULTIBUS® I compatible**
- **1M or 2M bytes of dual ported DRAM**
- **Up to 256K bytes for JEDEC type ROM/PROM/EPROM**
- **Two RS232 Serial Communication Ports**
- **Programmable Serial Port Baud Rates**
- **16 interrupt sources that can be arranged via Wire-Wrap Matrix**
- **Centronics parallel printer interface**
- **MON332B monitor firmware with power-on diagnostic**

Product Overview

The DB332-Plus Development Board is a high performance, 15 MHz, NS32332 based board that enables evaluation of National Semiconductor's NS32332 computer cluster and Series 32000 family. It has a Multibus I interface, with either 1 or 2 MBytes of high-speed, dual-port dynamic RAM, serial and parallel I/O, interrupt controller, ROM socket, and NS32332 computer cluster. The cluster consists of the NS32332 Central Processing Unit, NS32382 Memory Management Unit, NS32081 Floating Point Unit, NS32C201 Timing Control Unit, and NS32202 Interrupt Control Unit.

The instruction sets, cycle timing, bus interfacing, and internal architecture of the Series 32000 family can be examined using the DB332-Plus board. In addition, the DB332-Plus can provide a native debug and execution environment for programs developed on a host computer. The DB332-Plus is compatible with National's GNX software package.

The DB332-Plus board is shipped with the MON332B monitor and diagnostic firmware, serial and parallel printer cables, and user documentation. The board can be used in a Multibus I system, or as stand-alone board. In the stand-alone mode, the board needs a power supply, and terminal.

CENTRAL PROCESSING UNIT

The DB332-Plus incorporates a 15 MHz NS32332, which is a 32-bit, virtual memory microprocessor with

a 4 GByte addressing capability. The NS32332 is fully object code compatible with other Series 32000 microprocessors, and has the added features of 32-bit addressing, higher instruction execution throughput, and expanded bus handling capabilities. The bus features include bus error and retry support, dynamic bus sizing, burst mode memory accessing, and enhanced slave processor communication protocol.

The NS32332, being a member of the Series 32000 family, has powerful addressing modes, symmetric instruction set, modular software support, and linear addressing. The NS32332 is designed to work with both 16- and 32-bit slave processors of the Series 32000 family. They allow the processor to implement demand-paged virtual memory system through the use of the memory management unit (MMU), and support for high-speed floating point processing through the floating point unit (FPU).

SLAVE PROCESSORS

The DB332-Plus contains both the NS32382 MMU, and the NS32081 FPU. In addition, the board incorporates a connector that allows the next generation FPU, the NS32381, to be added. The NS32381 FPU will need to be mounted on a module that will be plugged into the DB332-Plus's expansion connector.

NS32382:

The NS32382 MMU provides hardware support for demand paged virtual memory management for the NS32332 CPU. The MMU has a 32-bit data path and translates 32-bit virtual addresses from the CPU into 32-bit physical addresses. High-speed address translation is performed on-chip through a Translation Buffer which holds the address mappings for 32 pages. If the virtual address generated by the CPU has no corresponding entry in the translation buffer, the MMU will perform address translation using a two level page table algorithm. The memory page size of the NS32332 is 4 Kbytes.

NS32081:

The NS32081 FPU provides high-speed floating-point processing support, and is compatible with the IEEE 754 standard for binary floating-point arithmetic. The NS32081 operates on two floating-point data types—single precision (32-bits) and double precision (64-bits). In addition, the FPU performs conversion between integer and floating-point data types. The NS32081 has eight, 32-bit floating point registers, a floating-point status register, and operates as a slave processor for transparent expansion of the NS32332 CPU's basic instruction set.

Interrupts

The DB332-PLUS development board incorporates the NS32202 Interrupt Control Unit (ICU). The ICU manages up to 16 maskable interrupt sources, resolves interrupt priorities, and supplies a single-byte vector to the CPU. In addition, two 16-bit counters are provided by the NS32202.

Memory

The DB332-PLUS comes with either 1M or 2M bytes of 85 ns static column, dual ported DRAM. At 15 MHz it can be accessed with 1 wait state. Memory supports Burst access via either the CPU or external MULTIBUS masters. Due to the MULTIBUS I form factor, the memory module and its controller is mounted on a separate P.C. board which is plugged into the DB332-PLUS.

Up to 256K bytes are available for JEDEC type ROM/EPROMs via a 28 pin socket. This socket is normally occupied by the MON332B firmware PROM.

Multibus Interface

The DB332-PLUS incorporates a MULTIBUS I interface, allowing the user to configure larger systems. Most often, the DB332-PLUS would be used in conjunction with MULTIBUS compatible expansion RAM, disk controller, or serial controller boards. However there is no restriction, beyond MULTIBUS compliance.

The DB332-PLUS's MULTIBUS compliance levels are:

Master D16 M24 V0 E1; indicating 16-bit data path, 24-bit memory address path, 16-bit I/O address path, and level or edge triggered non-bus vectored interrupts.

Slave D16 M24; indicating 16-bit data path and 24-bit memory address path.

Parallel I/O

A 40-pin connector (J3) and the necessary cable are provided to interface with a Centronix compatible printer.

Serial I/O

The two serial interfaces (J1 and J2) are designed to provide a wide variety of asynchronous, RS232C-compatible communications. Jumper options are provided for altering the configuration of each interface. Appropriate cables are included with the package.

Switches

The DB332-PLUS board has a non-maskable interrupt push-button (NMI) designated S1, a RESET push-switch designated S2 and a four- position DIP switch.

These three switches are located on the front edge of the CPU board. The status of the DIP switch can be read by the DB332-PLUS software.

Indicators

The DB332-PLUS board has four LEDs designated DS1 through DS4. Led DS1 is controlled by the physical address valid signal (NPAV) from the CPU cluster and indicates that the CPU cluster is active. DS2 through DS4 are software controlled and may be used as status or diagnostic indicators.

User Modes

The DB332-PLUS can operate stand-alone, with no assistance from the host computer system. Optionally, the board can be operated in conjunction with a host, taking advantage of more powerful software development tools and I/O capabilities. *Figure 1-2* represents the most common variations in user modes.

Stand-Alone Mode

From *Figure 1-2,* it is clear that the stand-alone user mode is the most simplistic and requires the least additional equipment. In this case, only an RS232 compatible terminal and power supplies for the DB332-PLUS are required to achieve effective operation. Using the monitor commands given in the Development Board Reference Manual, limited amounts of debugging can be accomplished.

Host Assisted Mode

The DB332-PLUS can be connected to another computer system or host. In this case, the user first develops Series 32000 software on the host system, then uses the RS232 communication link to download the software to the DB332-PLUS, which executes and debugs the software in a native environment. Several development software packages are available for use in generating Series 32000 user programs. Among them is National's GENIX Native and Cross Support Tools (GNX) which includes assemblers, linkers, and debuggers.

The DB332-PLUS is supplied with MON332B for interfacing between the host and terminal in this mode. The monitor software will provide:

- Terminal Handler (for use in transparent mode)
- Run-Time Environment (to permit execution of downloaded programs)
- Debugger Execute Module (to permit operation with host's debugger)

Consult the Development Board Monitor Reference Manual for a complete description of capabilities.

Two different configurations are available in host assisted mode, transparent and stand-aside. Both are illustrated in *Figure 1,* and explained below.

In transparent configuration, the user's communication with the host is conducted through the DB332-PLUS, which is transparent to the user. One advantage is that a single RS232 port on the host computer will support both the user's terminal and the DB332-PLUS.

In stand-aside configuration, the user communicates directly with the host while the DB332-PLUS "stands aside". This mode is useful when the DB332-PLUS is connected to single-user hosts, notably those where the terminal and keyboard are integral to the host. Optionally, stand-aside operation is possible with multi-user hosts where two RS232 ports are available.

Specifications

Environment

The DB332-PLUS is designed for operation in an office or laboratory environment. Sufficient air flow should be present to ensure all components are within their specified temperature ranges.

Environment	Description
Temperature	Operative 5°C to 50°C Inoperative −40°C to 60°C
Humidity	10% to 90% relative, non-condensing
Altitude	Operative 15,000 feet Inoperative 25,000 feet

Power Requirements

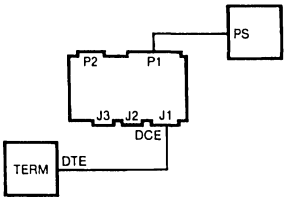
The DB332-PLUS requires three regulated DC voltages for operation.

1. +5V DC, ±5%, 10 Amps (when utilizing 2 Mbytes of memory)
2. +12V DC, ±10%, 100 mA
3. −12V DC, ±10%, 100 mA

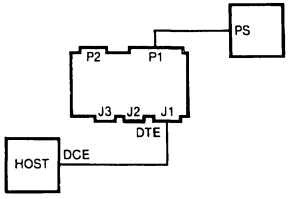
Ordering Information

Part Number	Description
NSV-32332B1M-15	15 MHz, 1MB memory version.
NSV-32332B2M-15	15 MHz, 2MB memory version.

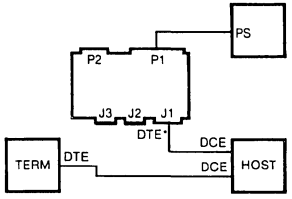
1. STAND-ALONE MODE



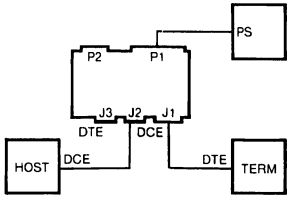
2. HOST-ASSISTED MODES
   a) STAND-ASIDE, SINGLE-USER HOST
      (eg. SPX II)



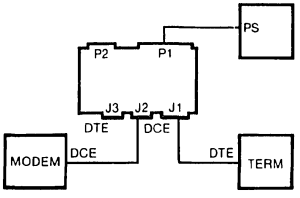
   b) STAND-ASIDE MULTIUSER HOST



   c) TRANSPARENT, LOCAL HOST



   d) TRANSPARENT, REMOTE HOST



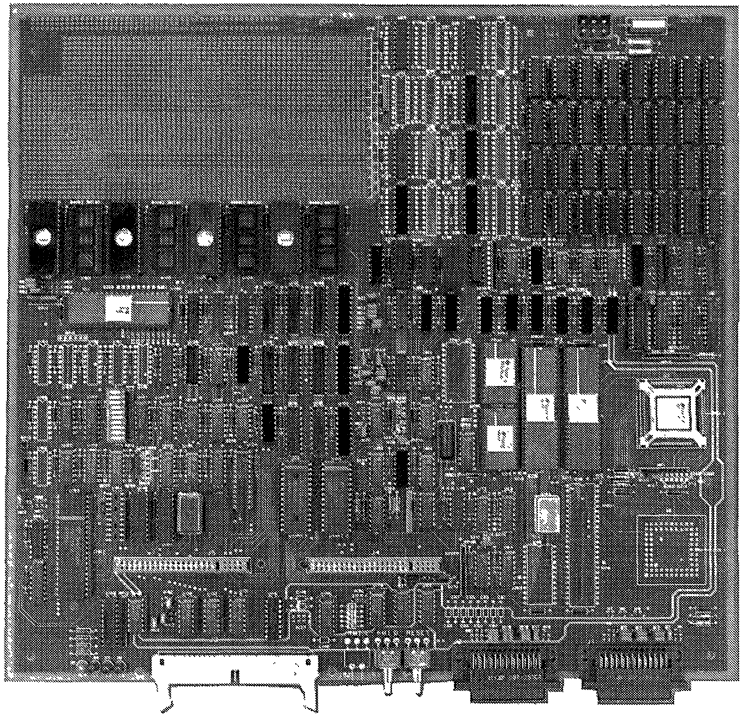
*REQUIRES RECONFIGURATION

TL/C/9249–2

5

National Semiconductor

DB32000 Development Board



TL/EE/8523–1

- **Series 32000® Microprocessor Family**
  - **— NS32032 Central Processing Unit (CPU) (can be replaced by NS32016 CPU, or NS32008 CPU, for evaluation)**
  - **— NS32082 Memory Management Unit (MMU)**
  - **— NS32081 Floating Point Unit (FPU)**
  - **— NS32202 Interrupt Controller Unit (ICU)**
  - **— NS32201 Timing Control Unit (TCU)**
- **256K bytes DRAM expandable to 1 Mbyte**
- **Up to 256K bytes of EPROM in two banks**
- **Two RS-232 Serial Communication Ports**
- **24 Programmable Parallel I/O Lines**
- **Two BLX™ Connectors**
- **Wire-wrap area for user expansion**
  - **— Bus interface**
  - **— Dual port RAM**
  - **— ROM expansion**
  - **— I/O expansion**
  - **— RAM expansion**
- **TDS™ firmware provides edit, assembly, and debug capabilities**

Product Overview

National Semiconductor's DB32000 Development Board is a complete microcomputer system. It is specifically designed to assist the user in evaluating and developing hardware and software for the NS32032 CPU, related slave processors (NS32081 FPU and NS32082 MMU) and support devices. With the DB32000, the user may evaluate other CPUs such as the NS32016 and NS32008. The DB32000 enables

Product Overview (Continued)

the user to examine the architecture, instruction set, cycle timing, and the bus interfaces for the Series 32000® family of microprocessors. Small programs can be written, debugged, assembled, and executed with EPROM-based TDS (Tiny Development System) software.

Optionally, the DB32000 can provide a native debug and execution environment for programs developed on a larger host computer system. In this case, the board complements capabilities provided by National's Pascal, Fortran and C cross-software packages.

The DB32000 includes the NS32032 CPU, NS32082 MMU, NS32081 FPU, NS32202 ICU, support circuitry, dynamic RAM, extensive ROM/EPROM capacity, and serial and parallel I/O. I/O capability can also be expanded via BLX interfaces.

Central and Slave Processors

The DB32000 is equipped with an NS32032 CPU, featuring 32-bit internal structure and 32-bit data bus. Optionally, an NS32016 or NS32008 CPU can be installed, with 32-bit internal structure and 16-bit or 8-bit data path. Each CPU provides a very powerful instruction set designed for high level language support.

The DB32000 also includes the NS32082 MMU and the NS32081 FPU. The NS32082 Memory Management Unit provides hardware support for demand-paged virtual memory management. The NS32081 provides high-speed floating-point instruction execution.

Interrupts

As part of factory configuration, the DB32000 comes with the NS32202 ICU installed. The NS32202 Interrupt Control Unit manages up to 16 maskable interrupt sources, resolves interrupt priorities, and supplies a single-byte vector to the CPU. In addition, the ICU provides two, 16-bit counters.

Memory

Expandable to 1 Mbyte, 256K bytes of on-board dynamic RAM are provided. The wire-wrap area may be used in conjunction with the DB32000 circuitry to develop dual port capability.

Up to 256K bytes of ROM/EPROM space is provided in eight 28-pin sockets. The sockets are divided into two banks, each bank permitting installation of 24- or 28-pin devices. All factory configurations include TDS firmware installed in the lower bank, with the upper bank vacant.

Parallel I/O

Twenty-four parallel I/O lines are provided via an 8255A Programmable Peripheral Interface. These may be divided into two 8-bit ports and two 4-bit ports.

Serial I/O

Two serial I/O ports are provided via 2651 Universal Synchronous/Asynchronous Receiver/Transmitters. These ports permit the DB32000 to communicate with RS232C compatible terminals or other computers. The baud rate for each port is software programmable.

BLX I/O Expansion

Two connectors are provided for attachment of 8- or 16-bit BLX expansion modules. BLX modules may be used to expand the DB32000's I/O capability; *e.g.,* additional serial on parallel ports.

Switches

Two button switches (S3 and S4), and one 10-position DIP switch (S1) are provided. S3, labeled NMI 0, will introduce a non-maskable interrupt to the DB32000's CPU when pressed. S4, labeled RESET, will reset the board when pressed. Switch S1 is a software readable dip switch that may be used to indicate defined options, *e.g.,* baud rate, MMU present, etc. Each switch position function is defined by the on-board PROM-based software.

Indicators

Four LED indicators (D2–D5) are mounted near the lower left corner of the DB32000. D2–D4 are controlled by the contents of a program-addressed register. They are used by the TDS power-on confidence test program to indicate test status. They may also be used to indicate any other information the user desires. D5 is driven directly by a 15-millisecond 1-shot timer. D5 will be extinguished whenever there is no CPU memory or I/O access within this time. D5 is illuminated when the CPU is executing instructions. This LED indicates whether or not the CPU is active.

Wire-Wrap Expansion Area

The wire-wrap expansion area provides the user with space that is drilled to accept integrated circuits. Signal pad terminators (stubs) are located at different locations on the board enabling the user to construct the following functions in the wire-wrap area:

— External Bus Interface
— Dual Port Memory Interface
— ROM Expansion
— I/O Expansion
— DRAM Capacity Expansion Using the On-board DRAM Controller

Tiny Development Systems (TDS) Functional Description

The TDS firmware allows the user to create programs by entering source via the editor. This source is then assembled to produce executable code suitable for debugging. These functions have the following features:

Assembler:

— Subset of existing Series 32000 assembler
— Supports FPU by providing long and short format real number data initialization
— Generates listings to either a printer at the parallel port, or any RS232 device connected via serial port
— Symbolic definition of static base or PC segment

Debugger:

— Numerical arguments to commands can be in four bases: decimal, hex, long real and short real
— Program flow visually traced by displaying source line at all breakpoints or step stops
— Memory/register print or change commands
— Step-through program commands: step "n" instructions, step while variable in range, step until variable reached

Editor:

— Commands to insert, replace, delete, type lines
— Automatic line number maintenance
— Save and retrieve source from audio cassette recorder
— Upload/download to/from any RS232–equipped PC
— Debug data displayed by type command after assembly

User Program Run Time Support:

— Accessed via a supervisor call instruction
— Routines to do terminal I/O
— Printer driver access to parallel port
— Routine to convert binary value to ASCII string
— Routine to convert ASCII string to binary value
— Conversion in four bases: decimal, hex, long real and short real

As shipped with the DB32000, TDS provides on-board hardware confidence test routines. These are invoked by power-on or manual reset.

User Modes

The DB32000 can operate stand-alone, with no assistance from a host computer system. Optionally, the board can be operated in conjunction with a host, taking advantage of more powerful software development tools and I/O capabilities.

Stand-Alone Mode (Factory Configuration)

The stand-alone user mode (see *Figure 1*) requires only an RS232C-compatible terminal and power supplies for the DB32000.

TDS (Tiny Development System) software is supplied in on-board PROMs to support this user mode. TDS is used to edit, assemble, and execute small Assembly language programs. In addition, TDS can control the DB32000's on-board I/O to provide cassette and printer interfaces, making the DB32000 a light duty development vehicle.

Host-Assisted Modes

The DB32000 can be connected to another computer system or host (refer to *Figure 1*). In this case, the user first develops Series 32000 software on the host system, then uses the RS232 communication link to download the software to the DB32000, which executes and debugs the software in a native environment.

Several development software packages are available for use in generating Series 32000 user programs. Among them are:

— Pascal, Fortran and C, operating under VAX/VMS
— Pascal, Fortran and C, operating under VAX/UNIX®

In each case, the DB32000's factory-supplied, on-board TDS software must be replaced. A suitable PROM-based monitor software package is supplied with the host development software.

The basic modes of host-assisted DB32000 operation are "stand-aside" and "transparent". The terms "stand-aside" and "transparent" may be visualized by observing the communication configuration for each mode. Refer to *Figure 1*.

The monitor software will provide:

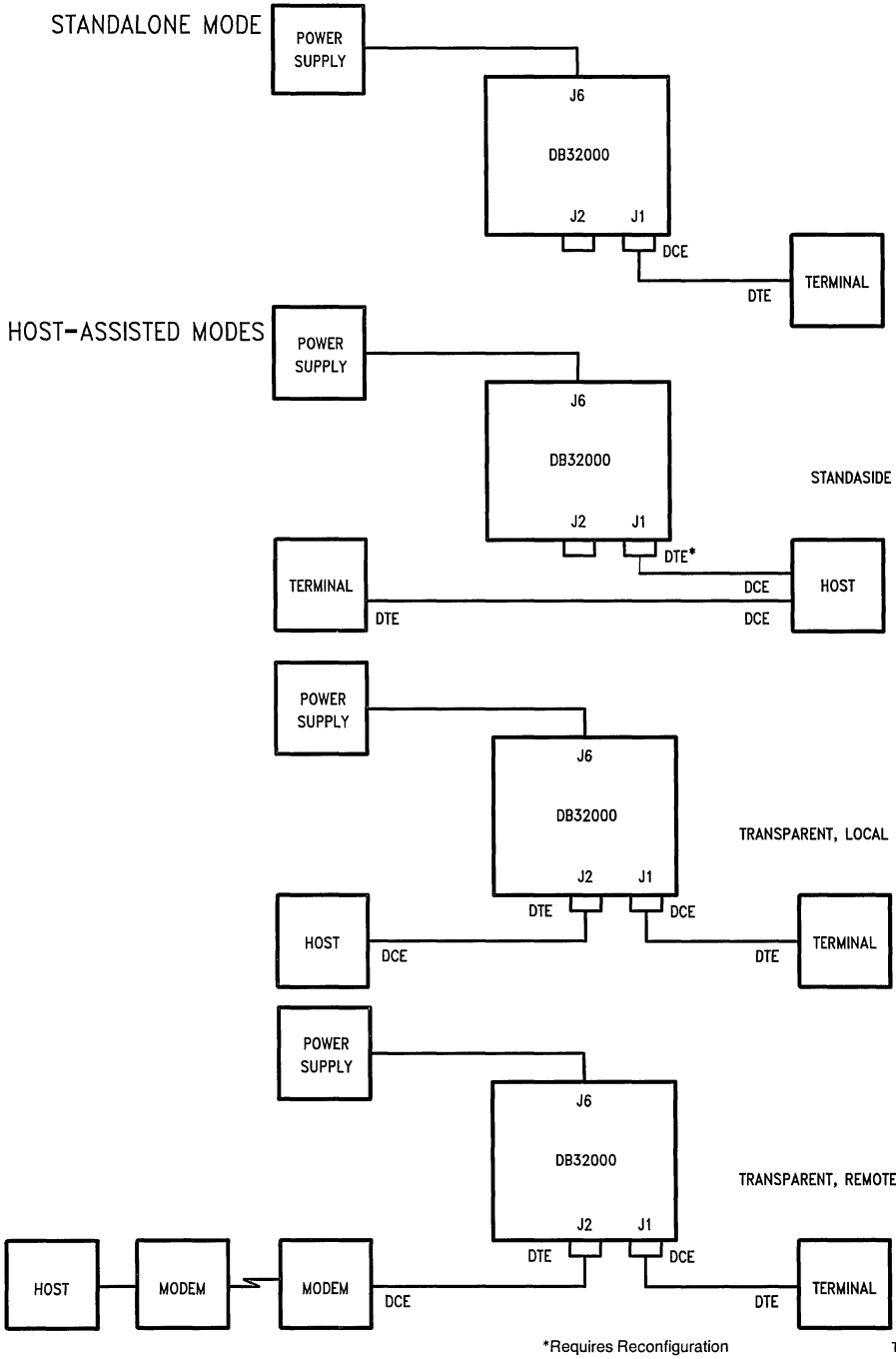
— Terminal Handler (for use in transparent mode)
— Run-Time Environment (to permit execution of downloaded programs)
— Debugger Execute Module (to permit operation with the host's debugger)

Consult the Development Board Monitor Reference Manual for a complete description of capabilities.

In transparent mode, the user's communication with the host is conducted through the DB32000, which is transparent to the user. One advantage is that a single RS232 port on the host computer will support both the user's terminal and the DB32000.

In stand-aside mode, the user communicates directly with the host while the DB32000 "stands aside". This mode is useful when the DB32000 is connected to single-user hosts, notably those where the terminal and keyboard are integral to the host. Optionally, stand-aside operation is possible with multi-user hosts where two RS232 ports are available.

User Modes (Continued)



*Requires Reconfiguration

TL/EE/8523-2

FIGURE 1. DB32000 Configurations

Specifications

Environment

The DB32000 is designed for operation in an office or laboratory environment. Avoid confining the DB32000 in a closed space, unless sufficient air flow is provided to ensure all components are operated within their specified temperature range.

Temperature:	Operating	0°C to +55°C
	Nonoperating	−40°C to +75°C
Humidity:	5% to 95% relative, noncondensing	
Altitude:	Operating	up to 15,000 ft.
	Nonoperating	up to 25,000 ft.

Power Requirements

The DB32000 requires three regulated DC voltages for operation:

— +12 volts DC, ±10%, 40 mA typical (50 mA max)
— −12 volts DC, ±10%, 40 mA typical (50 mA max)
— +5 volts DC, ±5%, 5A typical (10A max)

Ordering Information:

NSV-32032S6T-10 DB32000 Development Board

All models are shipped with:

Two RS232 cable sets

Model DB32000-110 Includes NS32032-10 CPU
NS32201-10 TCU
NS32202-10 ICU
NS32081-10 FPU
NS32082-10 MMU

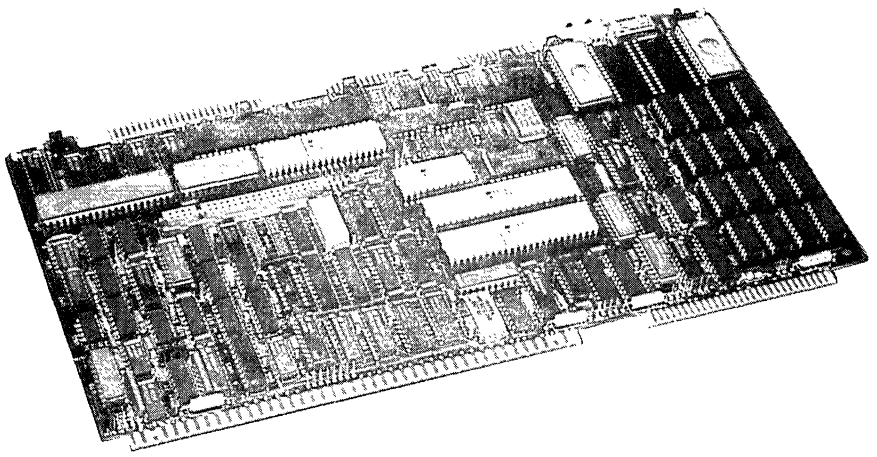
NSP-TDS-M Series 32000 TDS: Tiny Development System User's Manual

NSP-DB32000-M Series 32000 DB32000 Development Board User's Manual

NSP-INST-REF-M Series 32000 Instruction Set Reference Manual

National Semiconductor

DB32016 Development Board



TL/R/7083–1

- **Series 32000® Microprocessor Family**
  - **NS32016 CPU (can be replaced by NS32008 CPU, for evaluation)**
  - **NS32082 MMU**
  - **NS32081 FPU**
  - **NS32202 ICU**
  - **NS32201 TCU**
- **MULTIBUS® multi-master bus interface**
- **128 Kbytes dual ported RAM**
- **Up to 96 Kbytes PROM capacity**
- **Two RS232 serial communication ports**
- **24-programmable parallel I/O lines**
- **Three 16-bit programmable timer/ counters**
- **One BLX™ expansion module connector for additional I/O capability**
- **TDS™ firmware provides edit, assembly, and debug capabilities**

Product Overview

The DB32016 Development Board is a complete microcomputer using the National Semiconductor Series 32000 family of advanced microprocessors. It is specifically designed to assist evaluation and development of Series 32000 applications in a variety of environments.

By itself, the DB32016 can be used to examine the Series 32000 architecture and instruction set. Small programs can be written, debugged, and executed with EPROM-based TDS (Tiny Development System) software.

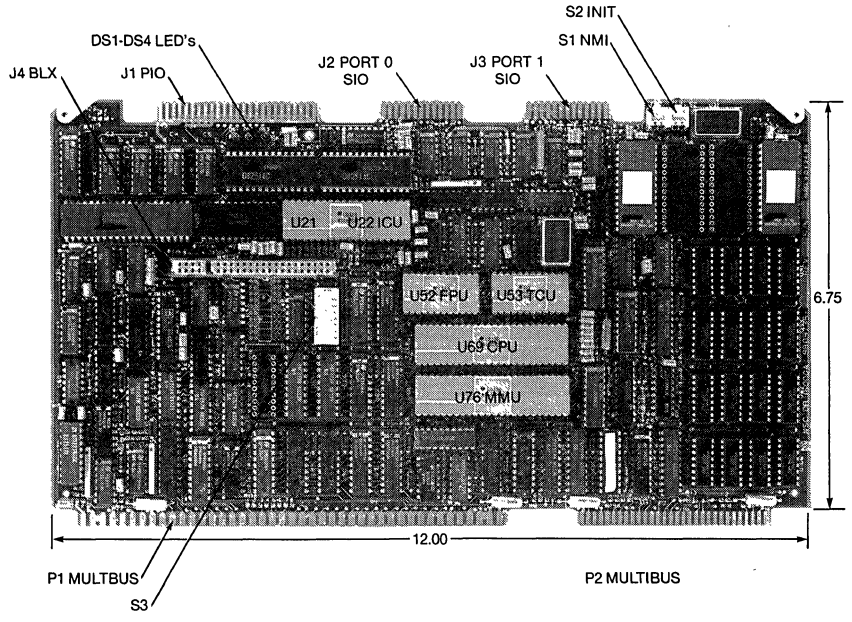
Optionally, the DB32016 can provide a native debug and execution environment for programs developed on a larger host computer. In this case, the board complements capabilities provided by National's C and Pascal cross software packages.

Flexibility is further enhanced by the board's MULTIBUS interface. This permits expansion of the DB32016 microcomputer system to include functions provided by other MULTIBUS compatible boards; e.g. disk/tape controllers, bulk RAM, etc.

All models of the DB32016 include, as a minimum, the NS32016 CPU, support circuitry, serial and parallel I/O, dynamic RAM, and extensive ROM/EPROM capacity. Optionally, the board can be populated with NS32082 Memory Management Unit, NS32081 Floating-Point Unit, and NS32202 Interrupt Control Unit. In all cases, I/O capability can be expanded via BLX and MULTIBUS interfaces.

Hardware Function Description

(Refer to *Figure 1-1*)



TL/R/7083–2

FIGURE 1-1. DB32016 Topography

Central and Slave Processors

The DB32016 is equipped with a NS32016 CPU, featuring 32-bit internal structure and 16-bit data bus. Optionally, a NS32008 CPU can be installed, with 32-bit internal structure and 8-bit data path. Each CPU provides a very powerful instruction set designed for high level-language support.

Included with each DB32016 is the NS32082 MMU and the NS32081 FPU slave processors. The NS32082 Memory Management Unit provides hardware support for demand-paged virtual memory management. The NS32081 provides high-speed floating-point instruction execution.

If the DB32016 is purchased without slave processors, they may be installed by the customer, as required.

Interrupts

Also included with the DB32016 is the NS32202 ICU. The NS32202 Interrupt Control Unit manages up to 16 maskable interrupt sources, resolves interrupt priorities, and supplies a single-byte vector to the CPU. In addition, the ICU provides two, 16-bit counters, one of which can provide programmable baud rate capability for the DB32016's serial I/O ports.

If the DB32016 is purchased without the ICU, it may be installed by the customer, as required.

Memory

128 Kbytes of on-board, dual-ported dynamic RAM are provided. The MULTIBUS starting address of RAM is mappable in 32K byte increments, across the entire 16M byte address space.

Up to 96 Kbytes of ROM/EPROM space is provided in four 28-pin sockets. The sockets are divided into two banks, each bank permitting installation of 24 or 28-pin devices. All factory configurations include TDS firmware installed in the lower bank, with the upper bank vacant.

MULTIBUS Interface

The DB32016 incorporates a MULTIBUS interface, allowing the user to configure larger systems. Most often, the DB32016 would be used in conjunction with MULTIBUS compatible expansion RAM, disk controller, or serial controller boards. However there is no restriction, beyond MULTIBUS compliance.

The DB32016's MULTIBUS compliance levels are:

Master	D16 M24 I16 VOEL; indicating 8/16-bit data path, 24-bit memory address path, 8- or 16-bit I/O address path, and level or edge triggered non-bus vectored interrupts (if NS32202 is installed).
Slave	D16 M24; indicating 8/16-bit data path, and 24-bit memory address path.

Parallel I/O

24 parallel I/O lines are provided via an 8255A Programmable Peripheral Interface. These may be divided into two 8-bit ports and two 4-bit ports.

Serial I/O

Two serial I/O ports are provided via 8251A Universal Synchronous/Asynchronous Receiver/Transmitters. These ports permit the DB32016 to communicate with RS232 compatible terminals or other computers.

Port baud rates may be derived from a variety of sources:

- a fixed, 9600 baud operation of both ports, if the NS32202 ICU is not installed.
- single programmable baud rate for both ports, if the NS32202 ICU is installed.
- Individually programmable baud rates for each port, via the DB32016's 8253-5 PIT.

Timer/Counters

As mentioned above, the NS32202 ICU provides two 16-bit timer/counters, when installed. In addition, three 16-bit counters are provided by the DB32016's 8253-5 Programmable Interval Timer. Each counter output is available for connection as an interrupt source for the ICU, or baud rate generation for the serial ports.

BLX I/O Expansion

A connector is provided for attachment of 8- or 16-bit BLX expansion modules. BLX modules may be used to expand the DB32016's I/O capability; e.g. additional serial or parallel ports.

Switches

Two push button switches (S1 and S2), and one eight-position DIP switch (S3) are provided.

S1, labeled NMI, will introduce a non-maskable interrupt to the DB32016's CPU when pressed. S2, labeled INIT, will reset the board when pressed. Both switches are located on the front edge of the board assembly. DIP switch S3 is used to set the Baud rate of the serial ports and other board configurations.

Indicators

Four LED indicators (DS1-DS4) are mounted near the front edge of the board assembly.

DS1-3 are controlled by the contents of a program addressed register. They are used by the TDS power-on confidence test program to indicate test status. They may also be used to indicate any other information the user desires.

DS4 is driven directly by a one-shot timer, whose period is approximately 15 milliseconds. DS4 will be illuminated whenever there is no memory or I/O access completed by the CPU within this period. This is useful to indicate a MULTIBUS timeout.

Tiny Development Systems (TDS) Functional Description

The TDS firmware allows the user to create programs by entering source via the editor. This source is then assembled to produce executable code suitable for debugging. These functions have the following features:

Assembler:

— Subset of Series 32000 assembler
— Supports FPU by providing long and short format real number data initialization
— Generates listings to either a printer at the parallel port, or any RS232 device connected via serial port
— Symbolic definition of static base or PC segment

Debugger:

— Numerical arguments to commands can be in four bases: decimal, hex, long real and short real
— Program flow visually traced by displaying source line at all breakpoints or step stops
— Memory/register print or change commands
— Step-thru program commands: step "n" instructions, step while variable in range, step until variable reached

Editor:

— Command to insert, replace, delete, type lines
— Automatic line number maintenance
— Save and retrieve source from audio cassette recorder
— Upload/download to/from any RS232 equipped PC
— Debug data displayed by type command after assembly

User Program Run Time Support:

— Accessed via a supervisor call instruction
— Routines to do terminal I/O
— Printer driver access to parallel port
— Routine to convert binary value to ASCII string
— Routine to convert ASCII string to binary value
— Conversion in four bases: decimal, hex, long real and short real

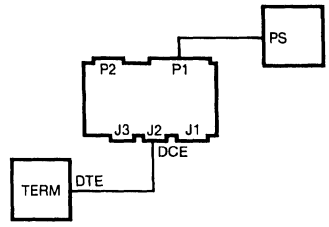
As shipped with the DB32016, TDS provides on-board hardware confidence test routines. These are invoked following power on.

User Modes

The DB32016 can operate stand-alone, with no assistance from a host computer system. Optionally, the board can be operated in conjunction with a host, taking advantage of more powerful software development tools and I/O capabilities.

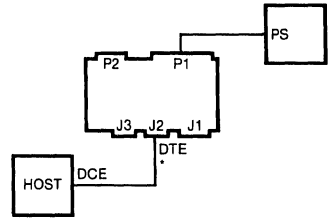
Figure 1-2 represents the most common variations in user modes.

1. Standalone Mode

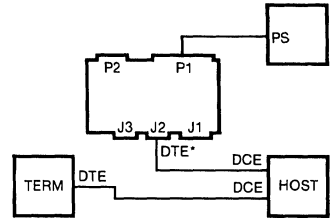


2. Host-assisted Modes

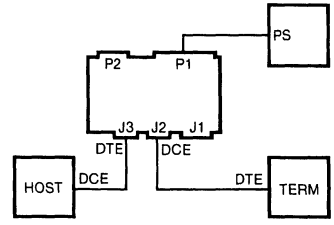
a) Standaside, single-user host



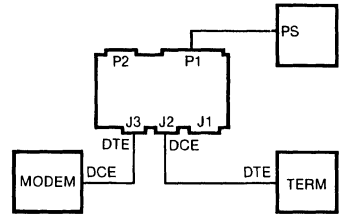
b) Standaside, multiuser host



c) Transparent, Local host



d) Transparent, Remote host



TL/R/7083–3

*requires reconfiguration

FIGURE 1-2. DB32016 User Modes

Stand-Along Mode (Factory Configuration)

From *Figure 1-2* it is clear that the stand-alone user mode is the most simplistic; requiring the least additional equipment. In this case, only an RS232C compatible terminal and power supplies for the DB32016 are required to achieve effective operation.

TDS (Tiny Development System) software is supplied in on-board PROM to support this user mode. TDS is used to edit, assemble, and execute small assembly language programs. In addition, TDS can control the DB32016's on-board I/O to provide cassette and printer interfaces; making the DB32016 a light duty development vehicle.

Host Assisted Modes

Referring to *Figure 1-2,* the DB32016 can be connected to another computer system, or host. In this case, the user will first develop Series 32000 software on the host system, then utilize RS232 communication to download the software to the DB32016. The DB32016 functions as a means of executing and debugging the software in a native environment.

Several development software packages are available for use in generating Series 32000 user programs.

Among them are:

- Pascal and C for VAX/VMS environments
- Pascal and C for VAX/UNIX environments

Host assisted modes require the TDS PROMs to be replaced by a PROM-based monitor program, compatible to the host development software. Monitor software is bundled with National's Series 32000 software packages. The monitor provides:

- a terminal handler, to control RS232 communications
- run-time environment, to permit execution of downloaded programs
- debugger execute module, to facilitate operation with the host's debugger software

The basic host assisted modes are:

- transparent
- standaside

The terms, transparent and standaside, may be visualized by observing the communication configuration in each mode. (Refer to *Figure 1-2*)

In transparent mode, the user's communication with the host is conducted through the DB32016; the DB32016 is transparent to the user. An advantage is that a single RS232 port on the host computer will support both the user's terminal, and the DB32016.

In standaside mode, the user communicates directly with the host; the DB32016 "stands aside". This mode is useful when the DB32016 is connected to single-user hosts. Optionally, standaside operation is possible with multi-user hosts, where two RS232 ports are available.

Specifications

Environment

The DB32016 is designed for operation in an office or laboratory environment. Avoid confining the DB32016 in a closed space, unless sufficient air flow is provided to ensure all components are operated within their specified temperature range.

- Temperature
  Operating 0°C to 55°C
  Non Operating −40°C to 75°C
- Humidity
  5% to 95% relative, non-condensing
- Altitude
  Operating 15,000 ft.
  Non Operating 25,000 ft.

Power Requirements

The DB32016 requires three, regulated DC voltages for operation:

+ 12 VDC, ±10%, 50 ma max
−12 VDC, ±10%, 50 ma max
+5 VDC, ±5%, 7.5A max

All power connections are made via P1. These connections are normally provided by a MULTIBUS compatible backplane. Optionally the user may elect to provide power, using one of the recommended connectors listed for P1.

Connectors

Local bus expansion (P2)-	CDC VPB01B30A00A2 AMP PES-14559 TI H311130
Parallel I/O (J1)-	3M 3415-001 AMP 2-86792-3
Serial I/O (J2)-	3M 3462-0001 flat AMP 1-583715-1 round
Bus interface (P1)- and Power	SAE FUPH7212-86MTNE Viking 2KH43/9AMK12

Ordering Information

Model DB32016-110 (Order #NSV-32016P8T-10)

Includes NS32016-10 CPU, NS32082-10 MMU, NS32081-10 FPU, NS32202-10 ICU, and NS32201-10 TCU for 10 MHz operation.

All Models are shipped with:

- Two RS232 cable sets
- TDS: Tiny Development System User's Manual (Publication No. 420306440-001)
- DB32016 Development Board User's Manual (Publication No. 420310111-001)

Related Reference Material

Series 32000 Instruction Set Reference Manual (Customer Order No. NSP-INST-REF-M)

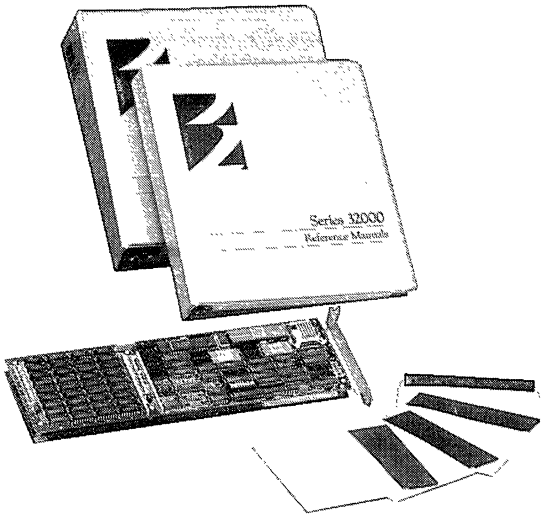
Section 6

Development Tools

Section 6 Contents

National Semiconductor

SYS32/30 PC-Add-In Development Package



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- **15 MHz NS32332/NS32382 Add-In board for an IBM® PC/AT® or compatible system**
- **2–3 MIP system performance**
- **No wait-state, on-board memory in 4-, 8- or 16-Mbyte configurations**
- **Operating system derived from AT&T's UNIX® System V Release 3**
- **Multi-user support**
- **GENIX™ Native and Cross-Support (GNX™) language tools. Includes— assembler, linker, libraries, debuggers**
- **Support for other Series 32000® development products:**
  - **— SPLICE**
  - **— National's Series 32000 Development Board family**
  - **— Compilers: C, FORTRAN77, Pascal, Ada®**
- **Easy to use DOS/UNIX interface**

Product Overview

The SYS32™/30 is a complete, high-performance development package that converts an IBM PC/AT or compatible computer into a powerful multi-user system for developing applications that use National Semiconductor Series 32000 microprocessor family components. The SYS32/30 add-in processor board containing the Series 32000 chip cluster with the NS32332 microprocessor allows programs to run on a personal computer at speeds greater than those of a VAX™ 780. The chip cluster on the processor board includes the NS32332 Central Processing Unit, NS32382 Memory Management Unit, NS32C201 Timing Control Unit and the NS32081 Floating-Point Unit.

Along with the processor board, the SYS32/30 package contains the Opus5™ operating system. This operating system is a port of AT&T's UNIX System V Release 3, and is derived from GENIX V.3, National

Product Overview (Continued)

Semiconductor's port of UNIX System V Release 3. Specially developed software is included to efficiently integrate the NS32332 processor board and the host PC/AT processor, allowing them to function as a complete UNIX computer system. National's Series 32000 GENIX Native and Cross-Support (GNX) language tools are included in the SYS32/30 package to provide stable and effective tools for software development. Optional compilers are available for FORTRAN77, C, Pascal, and Ada.

Functional Description

15 MHz ADD-IN PROCESSOR BOARD FOR AN IBM PC/AT OR COMPATIBLE SYSTEM

The SYS32/30 development package contains a processor board designed around the Series 32000 chip set. This chip set includes the NS32332 Central Processing Unit, NS32382 Memory Management Unit, NS32C201 Timing Control Unit, and the NS32081 Floating-Point Unit.

This processor board forms the high-performance center of the computer system with the host PC/AT processor. Peripherals are under the control of the PC/AT's microprocessor and are located either on the PC/AT motherboard or on other boards in the AT chassis. The PC/AT handles all direct access to devices and serves as an integral dedicated I/O processor.

The SYS32/30 processor board plugs into the PC/AT bus, uses the standard control and data signals, and appears to the PC/AT as 16 bytes in the PC/AT Input/Output (I/O) space. Communication between the PC/AT and the board is accomplished via this address space. This architecture allows the board to interface to the PC/AT in the same manner as any other AT peripheral. The PC/AT processes I/O commands while the SYS32/30 processor board continues with regular operation. I/O is requested via interrupt to the PC/AT, which then performs the data transfer using Direct Memory Access (DMA). (See *Figure 1*).

The processor board requires two slots in the PC/AT motherboard and plugs into a single long 16-bit bus slot. The space of the second slot is needed to accommodate the piggybacked memory board attached to the processor board. No additional connections are required.

2–3 MIPS SYSTEM PERFORMANCE

The NS32332 CPU and associated devices operating at 15 MHz provide computing power greater than that of a VAX 780. Sustained performance for the NS32332 device cluster is 2–3 VAX MIPS (Million Instructions Per Second). An example of relative performance using the widely recognized Dhrystone benchmark is shown in *Figure 2*.

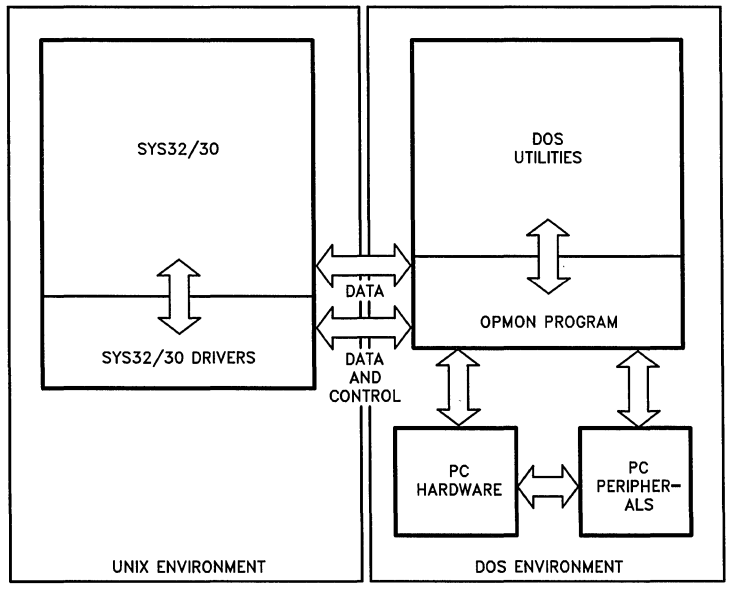

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FIGURE 1

Functional Description (Continued)

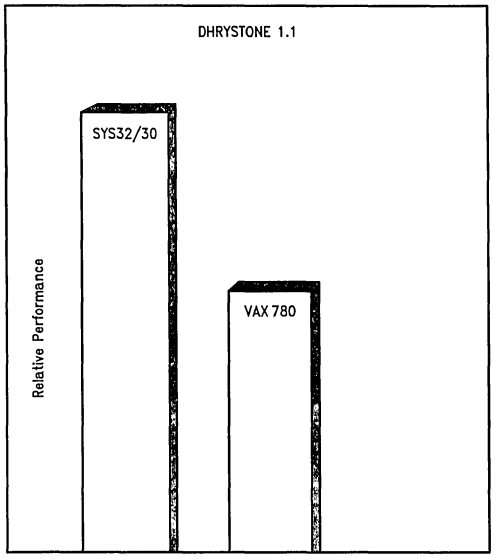

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FIGURE 2. SYS32/30 Dhrystone Program Compiled with GNXr2 C Compiler VAX 780 Dhrystone Data Obtained from USENET

ON-BOARD MEMORY CONFIGURATIONS OF 4, 8 OR 16 MBYTES

The processor board is configured with either 4, 8, or 16 Mbytes of zero wait-state physical memory. It is possible to upgrade the 4- or 8-Mbyte configuration to 16 Mbytes through the purchase of an optional 16-Mbyte memory card.

OPERATING SYSTEM

The SYS32/30 operating system is a port of AT&T's UNIX System V Release 3, and is derived from GENIX V.3, National Semiconductor's port of UNIX System V Release 3.

The UNIX operating system is a powerful, multi-user, multitasking operating system that includes the following key features:

Demand Paged Virtual Memory
Hierarchical file system
Source Code Control System (SCCS)
UNIX to UNIX copy (uucp)
"make" utility
Menu-driven system administration

The UNIX operating system has a proven reputation as an effective and productive environment for efficient software development. UNIX allows multiple users to work simultaneously on the same computer and project. The Source Code Control System (SCCS) automatically tracks program revisions as development work progresses. The "make" software saves valuable time in regenerating complex software systems after changes are made. The *uucp* software allows users on different UNIX systems to communicate using electronic mail and to transfer files over dial-up or serial communications links. Menu-driven system administration is available for system setup, adding users, controlling communication lines, installing software packages, changing passwords, and other administrative functions.

ADDITIONAL SUPPORT UTILITIES

Many of the popular utilities from the Berkeley 4.2 UNIX operating system, not contained in AT&T's UNIX System V Release 3, are supplied as part of the package. These utilities are listed in Table I.

TABLE I. Bsd 4.2 Utilities

C Shell	apply	banner
bsu	chsh	clear
ctags	expand	factor
from	head	last
leave	more	primes
scrpt	strings	test
unexpand	whereis	which

The Tools for Documenters package, derived from the AT&T Documenter's Workbench™ Utility, provides the Series 32000 programmer with the tools to prepare documentation. The major components of this package are shown in Table II.

TABLE II. Tools for Documenters Utilities

Name	Description
nroff	A text formatter for line printers
troff	A text formatter for typesetters
otroff	A text formatter for typesetters
mm	A macro package
mmt	A macro package
eqn	A troff preprocessor for typesetting mathematics on a phototypesetter
neqn	A troff preprocessor for typesetting mathematics on a terminal
tbl	A preprocessor for formatting tables
pic	A preprocessor for graphic illustrations
col	A filter to nroff for processing multicolumn text output, as from tbl

NETWORKING CAPABILITY

The SYS32/30 based development system configured to support networking using the TCP/IP protocol allows project development using multiple systems, including SYS32/30 based systems, VAX/VMS™ (using TCP/IP), and VAX/4.2bsd. The compatibility de-

Functional Description (Continued)

sign of the GNX language tools allows software modules developed on these networked systems to be linked together on a single system for execution as one program. Networking requires that additional hardware and software be installed in the system. Third party products that enable networking are listed in the SYS32/30 configuration guide.

MANUALS

A complete manual set for the operating system and related software is included in the SYS32/30 package. This includes:

Installation instructions for the PC Add-in board
Installation instructions for software
UNIX System V.3 reference manuals and user guides
GNX Language Tools Manuals
Tools for Documenters Reference Manual
Berkeley Utilities Manual

MULTI-USER SUPPORT

The SYS32/30 operating system is an interactive, multi-user, multitasking operating system. Many activities or jobs can be performed simultaneously when serial ports are added to the host system. These additional serial ports are used for terminals, printers, modems, I/O-to-development boards, I/O-to-target hardware, or for communication with National's SPLICE debugging tool. Information about third party products that provide additional serial ports is contained in the SYS32/30 configuration guide.

GNX LANGUAGE TOOLS

The GENIX Native and Cross-Support (GNX) language tools allow the user to compile, assemble, and link user programs to create executable files. These files can then be executed and debugged on a Series 32000 development board, target system application hardware, or a 32000/UNIX-based system such as the SYS32/30.

The GNX language tools include the assembler, linker, debuggers, libraries, and the monitor software for all Series 32000 development boards in both PROM and source code form.

The Series 32000 GNX language tools are based on AT&T's Common Object File Format (COFF). Under COFF, object modules created by any of the GNX compilers or the GNX assembler may be linked to object modules of any other translator in the GNX tools. Compilers available are FORTRAN77, C, and Pascal.

The COFF file format also allows object modules that have been created by the GNX tools on other development hosts (VAX/VMS or VAX/4.2bsd, for example) to be linked with modules created on the SYS32/30 system. This flexibility is most valuable where non-centralized software development is desired and the systems are able to transfer or share files via a common network. Information for configuring the SYS32/30 for integration into a network is contained in the configuration guide.

Compilers are available as separate optional software to allow individual selection of the application language. The C and FORTRAN compilers are the result of National's optimizing compiler project and reflect state-of-the-art compiler technology for optimizing execution speed. Pascal and Ada compilers are also available. For additional details about the GNX tools consult the GNX tools data sheet, Literature Number 114299.

Real-time kernels such as National's EXEC or VRTX®/Series 32000 are supported by the GNX tools. With the appropriate command-line arguments, and when linked with appropriate libraries, the GNX tools are used to develop code for execution with these real-time kernels. More information on EXEC is contained in its data sheet in the Series 32000 Databook. The VRTX data sheet (Literature Number 114269) provides more information about VRTX.

ADA COMPILER

The Series 32000 Ada cross-development system completely supports Ada language program development on National's SYS32/30 host and is part of National's Validated Ada Development Environment (NVADE). NVADE provides a high performance Ada compiler that supports all required features of the Ada language and is fully compliant with ANSI/MIL-STD-1815A. Consult the data sheet (Literature Number 114262) on the Ada cross-development system for additional details.

SUPPORT FOR AN INTEGRATED DEVELOPMENT ENVIRONMENT

The SYS32/30 contains the functionality and compatibility needed to utilize other tools available from National Semiconductor for developing and debugging Series 32000-based applications. These tools include the SPLICE software debugger and National's Series 32000 Development Board set.

The SPLICE development tool provides a communication link between a Series 32000 target and a development system host. This connection allows users to download and map their software onto target memory and then debug this software using National Semiconductor's GNX debugger. Consult the SPLICE data sheet for more information.

The Series 32000 development boards used with the SYS32/30 are complete microcomputer systems specifically designed to assist the user in evaluating and developing hardware and software for the Series 32000 family of CPUs. More information on the Series 32000 development boards is contained in the Series 32000 Databook, Literature Number 400094.

Functional Description (Continued)

DOS/UNIX INTEGRATION

The SYS32/30 PC add-in development package allows easy transfer of data between DOS and the UNIX operating system. A system console user can switch between either operating system using only a few keystrokes. A shell interface allows DOS commands to be executed from the UNIX shell, UNIX commands to be executed from DOS, and files to be transferred between the UNIX and DOS partitions on the system disk. In addition, the user can suspend the SYS32/30 operation, enter DOS, run an application, and then return to the SYS32/30 environment.

Series 32000 Application Development

The SYS32/30 with the PC/AT operates as a local host computer system for integrating application software into target prototype boards containing Series 32000 components. Programs can be written in assembly language or in a higher level language. Optional compilers are available for C, FORTRAN, Pascal, and Ada.

During compilation, the C, FORTRAN, and Pascal compilers generate assembly code which is assembled by the GNX assembler. (See *Figure 3*.) The output of the assembler is an object file which can be linked to other object files and/or libraries, resulting in an executable file. The Ada compiler generates executable code without creating assembly language as an intermediate step.

Since the SYS32/30 provides a Series 32000 native environment, the executable file may be run on the host SYS32/30 system or loaded into RAM on either a target system, SPLICE, or one of the Series 32000 development boards. The source-level software debuggers in the GNX tools provide powerful facilities for debugging software on the target system.

The GNX debugger, working in conjunction with SPLICE or with the monitor program on the target board, is capable of downloading and controlling the execution of software on the target system. Executable monitor software is provided in PROMs in the SYS32/30 package for the Series 32000 development boards. Monitor software is also provided in source form in the GNX language tools so application designers can modify and port the monitor to suit the needs of their target system.

After debugging, the executable file created by linking can also be converted to PROM format using the GNX *nburn* utility.

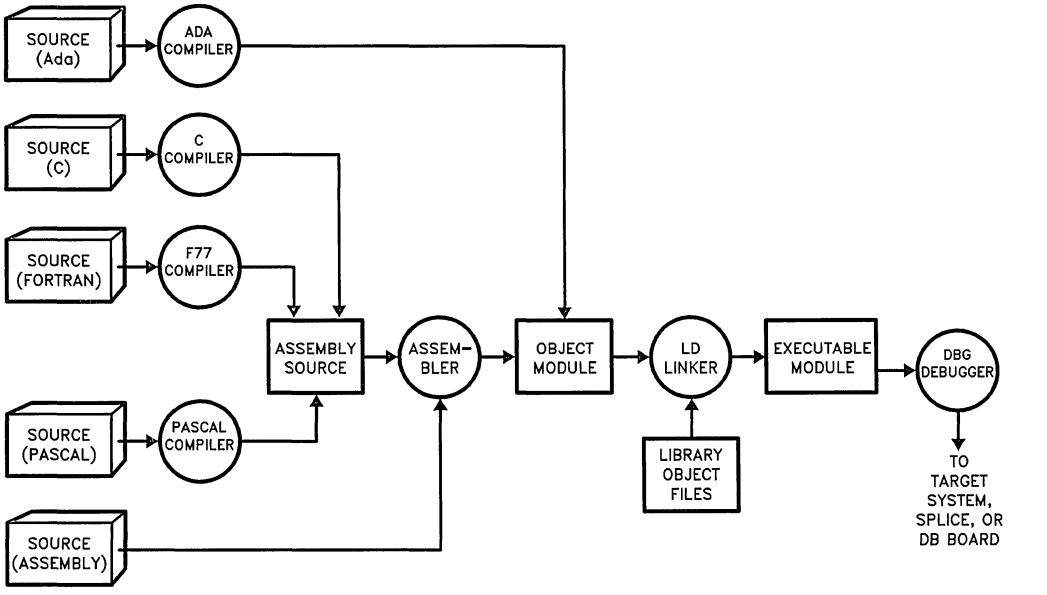

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FIGURE 3

Configuring a System

The SYS32/30 PC Add-In package supports a variety of configurations. Based on developer needs, the final configuration may need extra serial I/O ports, and/or networking capability. A hard disk of sufficient size is also an important part of the configuration. A configuration guide that outlines available options and recommended products for configuring the SYS32/30 development system is available.

Host system elements required for SYS32/30 operation are:

— IBM PC/AT or compatible system
— Two full length slots in the motherboard
— 512 Kbytes of RAM
— PC-DOS 3.1 or later
— 1.2-Mbyte floppy disk drive
— Adequate hard disk storage (see the next section on disk size)

Note: The SYS32/30 processor board actually plugs into a single slot. The second slot is required to accommodate the space taken by the piggybacked memory board attached to the NS32332 processor board.

The SYS32/30 PC/AT Add-In Development Package runs on an IBM PC/AT or compatible computer. If an IBM PC/AT is not used for the host system, it is important to remember that compatibility can vary between IBM PC/AT compatible systems. The SYS32/30 processor board may not be adequately supported by systems that lack full IBM PC/AT compatibility. The configuration guide available contains a list of IBM PC/AT compatible systems that have the required compatibility.

HARD DISK CAPACITY

Several factors influence the size selected for a hard disk. Consideration should include the number of users for the system, space for user files, the size of the application to be developed, and extra software packages and compilers that must reside on the system.

For example, a 40-Mbyte hard disk is the minimum size recommended for a SYS32/30-based development environment. This provides sufficient space for a single-user account, the UNIX operating system and utilities, the GNX tools, compiler software, basic DOS software, and a moderate size application. If the system is used for developing an Ada-based application, a minimum of 60 Mbytes of disk storage is recommended. Disk drives with even greater capacity than the minimum sizes indicated here should be considered for additional users or software and to provide for growth of the system.

When selecting hard disk drives or other peripheral devices, it is important that the device conform to the industry-standard for peripheral devices designed for use on the PC/AT bus.

Basic Kits

The SYS32/30 Add-In Development package is available in three basic kits:

NSS-SYS30-KIT1	For IBM-AT and compatible systems PC Add-In coprocessor board with 4 Mbytes on-board memory UNIX System V.3 based operating system GNX Language Tools Tools for Documenters Berkeley Utilities Installation instructions for the PC Add-In board Installation instructions for software UNIX System V.3 reference manuals and user guides GNX Language Tools Manuals Tools For Documenters Reference Manuals Berkeley Utilities Manual
NSS-SYS30-KIT2	Same as KIT1 except with 8 Mbytes of on-board memory
NSS-SYS30-KIT3	Same as KIT1 except with 16 Mbytes of on-board memory

MEMORY UPGRADE

To upgrade the memory size to 16 Mbytes after the purchase of KIT1 or KIT2, the following 16-Mbyte memory board must be purchased to replace the existing memory board:

NSS-SYS30-MEM16 16-Mbyte memory board.

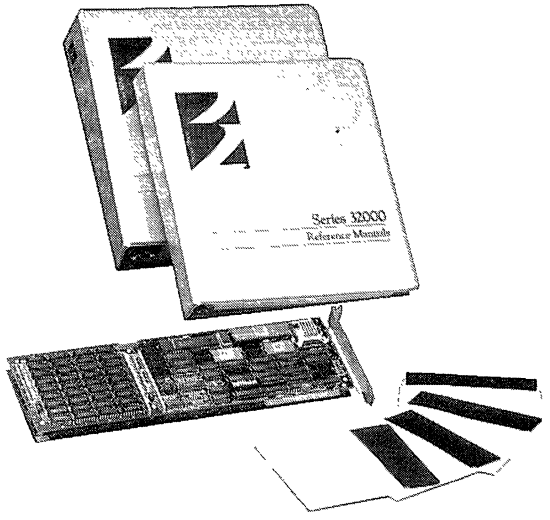
Optional Software Packages

(A prerequisite for use is the purchase of one of the above basic kits).

NSW-C-BHBF3	Optimizing C Compiler
NSW-F77-BHBF3	Optimizing FORTRAN77 compiler
NSW-PAS-BHBF3	Pascal compiler
NSW-ADA-BHBF	Ada compiler
NSW-NET-BHBF3	Networking software
NSP-SYS32/V3-MS	Additional operating system manual set

National Semiconductor

SYS32/20 PC Add-In Development Package



TL/C/9250–1

- **High Performance, 10 MHz, no-wait state, 32-bit expansion board for an IBM-PC/AT or compatible system**
- **An Operating System derived from AT&T's UNIX® System V.3**
- **The Series 32000 GNX (GENIX Native and Cross-Support) Language tools including the Series 32000 assembler, linker, monitors and debuggers**
- **Hardware that supports the NS32032 CPU, NS32082 MMU, NS32201 TCU and the NS32081 FPU**
- **Two available on-board memory configurations:**
  - 2-Mbyte RAM
  - 4-MByte RAM
- **Software available on 1.2-MByte floppies**
- **Complete support for the following application tools:**
  - SPLICE
  - National's Series 32000 Development Board Family
  - Compilers for C, FORTRAN77, Pascal and Ada
  - Complete System V Documentation
  - 4.2 "bsd" Utilities
  - Tools for Documentors (TFD), a derivative of AT&T's DWB™ utilities
  - Multiuser environment

Description

National Semiconductor's SYS32/20 is a complete, high performance development package that converts an IBM-PC/AT or compatible system into an ideal environment for the support of Series 32000®-based applications. The SYS32/20 PC Add-In Development Package allows mainframe-size programs to run on a personal computer at speeds similar to those of a VAX 780. The SYS32/20 consists of a 32-bit PC Add-In board based on the Series 32000 chip set, a complete port of AT&T's UNIX® System V.3 specially developed software that integrates the UNIX and DOS operating systems, and National's Series 32000 development tools (GNX).

6

Hardware

The SYS32/20 hardware consists of a Series 32000 chip set on a single-slot co-processor board. The chip set includes an NS32032 CPU with either 2 or 4 MBytes of on-board memory.* The hardware is an IBM PC Add-In board that plugs into the no-wait-state motherboard. No additional connections are required. Up to 8 serial ports can be used on all supported PCs. Parallel ports are also supported. The SYS32/20 Add-In board supports a variety of Series 32000 family components including the high-performance, 10 MHz NS32032 Central Processing Unit, the NS32082 Memory Management Unit, the NS32201 Timing Control Unit and the NS32081 Floating-Point Unit.

Software

The SYS32/20 contains the Opus5™ operating system. Opus5 is a complete port of AT&T's UNIX System V Release 3 (V.3), and is derived from GENIX/V.3, National Semiconductor's port of UNIX System V.3.

System V is an advanced, proven programming environment that fully supports the Series 32000 microprocessor family, including Demand-Paged Virtual Memory (DPVM). System V's general-purpose, multitasking, interactive system makes the programmer's computing environment simple, efficient and productive.

The SYS32/20 Add-In board can also be used to execute object code under a native environment. Object files conform to a superset of the AT&T Common Object File Format (COFF), and take full advantage of the advanced features of the Series 32000 architecture. The GNX (GENIX Native and Cross-Support) software consists of an assembler, a linker, debuggers, monitors, basic I/O routines and other tools that support a group of optional compilers such as C, Pascal and FORTRAN77. Other software features supported by the SYS32/20 include Tools for Documenters.

Installation

Installation of the SYS32/20 PC Add-In Package is straight-forward and well-documented.

The SYS32/20 software occupies a PC fixed disk in one of two ways: it either uses a separate partition for the logical disk or it uses a large DOS file. The first method is necessary for file systems larger than 28 Mbytes; the second method is recommended for fixed disks that don't use the ROM BIOS interface.

Installation is divided into three general stages: partitioning the fixed disk, installing the core system, and adding the desired software subsets. User-friendly software guides you easily through each stage of installation.

*__Note:__ The hardware configuration does not allow the 2-Mbyte version to be upgraded to the 4-Mbyte version.

Integrated Environment

The SYS32/20 PC Add-In Development Package allows data to be easily shared between DOS and the UNIX System V Operating system. A user can switch between either operating system using only a few keystrokes. A shell interface allows DOS commands to be executed from the System V shell, System V commands to be executed from DOS, and files to be transferred between the System V and DOS partitions on the system disk. In addition, the user can suspend the SYS32/20 operation, enter DOS, run an application and then return to the SYS32/20 environment.

Support for Hardware/Software Integration

Two solutions are available for integrating application software, created under the PC-SYS32/20 development environment with target prototype. The PC with SYS32/20 operates as a local host computer system for the environments of both solutions. Under the environment of both solutions, the high language software debuggers provide powerful emulation facilities to test and shakeout the integrated hardware/software target system until a proven product is achieved. Such facilities include setting of breakpoints and registers and memory data display and modifications.

The first solution requires the use of an In-System Emulator (ISE). The SYS32/20 Add-In Development Package supports National's ISE32 (In-System Emulator for the NS32032). The ISE software consists of the ISE monitor firmware, which resides in PROMs in the emulator pod, and the ISE Debugger (IDBG), which is included with, and runs on the SYS32/20. The monitor firmware controls the ISE hardware. The IDBG is a high-level, user-friendly debugger program. It translates commands entered by the user, into low-level instructions the ISE monitor uses to drive the hardware. IDBG also translates and sends ISE responses to the user.

The second solution requires the use of monitor firmware programs running in the user's target hardware and Debugger (DBG). DBG is a superset of the IDBG described in the first solution above, and, like IDBG, is included with, and runs on, the SYS32/20. DBG performs the same functions as IDBG. The monitor downloads and controls the execution of the user's software. Monitor firmware programs include MON16 (monitor firmware program for NS32016-based target hardware) and MON32 (monitor firmware program for

NS32032-based target hardware). These monitor firmware programs are provided in PROMs and included with SYS32/20. The monitors are also provided in source form so Series 32000 designers can modify the monitor to suit their target system requirements.

Configuring a System

The SYS32/20 PC Add-In package supports a variety of configurations. Based on developer needs, the final configuration may need extra serial I/O ports, and/or networking capability. A hard disk of sufficient size is also an important part of the configuration. A configuration guide that outlines available options and recommended products for configuring the SYS32/20 development system is available.

Minimum System Configuration

The following list specifies the minimum configuration required to install a SYS32/20 PC Add-In Board:

- 30-Mbyte hard disk. (40-Mbyte or larger is strongly recommended.)
- 512 Kbytes of RAM.
- PC/AT or compatible personal computer system.
- PC-DOS 3.1 or later operating system.
- Slots:
  —The 2-Mbyte board consists of 1 full board + 1/2 piggyback board and may require 2 slots depending on the arrangement of other expansion boards in the PC.
  —The 4-Mbyte board consists of 1 full board + 1 full piggyback board and may require 2 slots depending on the arrangement of other expansion boards in the PC.

Basic Kits (Note: No Compiler Included.)

NSS-SYS203-KIT1 For IBM-AT and compatible systems; 2MB on-board memory; UNIX System V.3 Operating System; GNX Assembler tools; "bsd" and Tools For Documenters utilities; software on 1.2 MB high density floppy diskettes; a complete set of manuals, including AT&T UNIX System V.3 manuals.

NSS-SYS203-KIT2 For IBM-AT and compatible systems; same as KIT1 except with 4MB on-board memory.

Optional Software Packages

(Prerequisite for use is purchase of the above basic kits.)

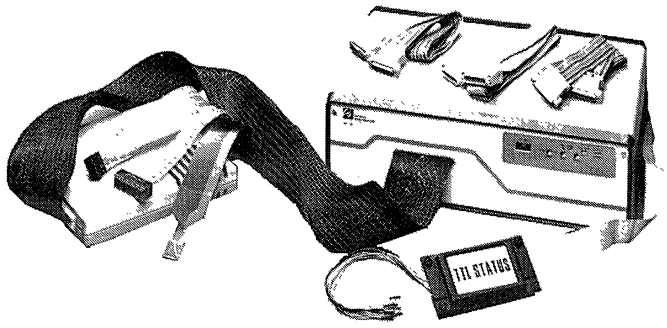
The following software should be ordered for execution on the System V.3-derived operating system. Available on high density diskettes only.

NSW-C-BHAF3	Optimizing C compiler.
NSW-F77-BHAF3	Optimizing FORTRAN77 compiler.
NSW-PAS-BHAF3	Pascal compiler.
NSW-ADA-BHBF	Ada compiler.
NSW-NET-BHAF3	Networking software.
NSP-SYS32/V3-MS	Additional V.3 operating system manual sets.

Note: For purchase of any and all software packages (NSW- . . .) user must show or demonstrate proof of prior purchase of one of the NSS-SYS203-KITx packages above.

National Semiconductor

ISE32™ NS32032 In-System Emulator



TL/R/8522–1

- **Operation up to 10 MHz***
- **Emulation of NS32032 Central Processing Unit, NS32082 Memory Management Unit, NS32201 Timing Control Unit**
- **Host resident debuggers**
- **Generalized event driven system**
- **Memory mapping, up to 128 kbytes**
- **Read/write protection of 4 kbyte memory blocks**
- **Program flow tracing, up to 1023 non-sequential fetches**
- **Complete bus activity trace**
- **Qualified tracing**
- **Pre-, post-, or center-triggering on trace**
- **Two 32-bit execution counters**
- **Supports Memory Management Unit functions**
- **Supported under various host systems and operating systems**
- **Hierarchical on-line help facility**
- **Self-diagnostic**

*Refer to ISE speed consideration section.

Description

The NS32032 In-System Emulator (ISE32) is a powerful tool for both hardware and software development of NS32032 microprocessor-based products.

The ISE32 emulates the NS32032 Central Processing Unit (CPU), the NS32201 Timing Control Unit (TCU) and NS32082 Memory Management Unit (MMU). NS32082 MMU emulation can be disabled by a switch setting. The ISE32 allows users to test and debug both hardware and software in their own hardware environment.

The ISE32 is a complete unit, including an internal clock oscillator that generates a choice of three clock signals: 10 MHz, 5 MHz, and 2.5 MHz; and 128 kbytes of dedicated user's ISE™ memory. With the ISE32, users can easily stop emulation and examine the contents of CPU registers, slave processor registers, and memory.

The ISE32 consists of the ISE hardware, the ISE firmware monitor, and RS232 cables. A host-dependent debugger software program is available as part of the appropriate Series 32000® software support package.

Each of the Series 32000 software support packages include software tools to produce code compatible with the debugger software. Refer to the section "Required User-Supplied Equipment".

Hardware Description

The ISE32 hardware is housed in three enclosures: the ISE Support Box; the Emulator Pod; and the TTL Status Pod. *Figure 1* is a block diagram of ISE32 hardware.

The ISE Support Box is the largest enclosure. It contains the emulation support circuits for trace, breakpoints, and mapped memory; as well as the hardware for the RS232 serial ports, which are used to communicate with the host and the user's terminal. It also houses the power supplies and the ISE32 control switches and indicators. *Figure 2* shows the location of the ISE32 control switches and indicators. Table I lists the functions of each switch and LED.

The Emulator Pod contains the NS32032 CPU, NS32082 MMU, and NS32201 TCU required for target system emulation. It also contains the ISE Monitor firmware.

The Emulator Pod connects to the ISE Support Box via a four-foot flat cable assembly. Connections to the target system are made via three one-foot target cables. One target cable is provided for each member of the Series 32000 chip set (CPU, MMU, and TCU).

The Status Pod is the smallest enclosure. It provides TTL-compatible input and output signals for use during ISE operation. The Status Pod has ten leads and three binder posts that can be connected to either the target system or test equipment such as logic analyzers or oscilloscopes. Table II lists the function of each lead and post of the Status Pod. The Status Pod connects to the ISE Support Box via a six-foot cable.

ISE32 Software Overview

The ISE32 software consists of the ISE firmware monitor, which resides in PROMs in the Emulator Pod, and the ISE Debugger, which runs on the host system.

When the ISE32 unit is not running an emulation program, it is running a program called the ISE monitor.

The monitor communicates with the ISE Debugger and provides a command protocol that allows the host complete control of the ISE32 hardware.

The ISE Debugger translates commands entered on the host system from a terminal, into low-level instructions that the ISE monitor uses to drive the hardware. The ISE Debugger also translates and sends ISE responses to the user via the terminal. All ISE monitor operation is transparent to the user.

The ISE32 Debugger

The ISE32 Debugger is user compatible with the standard non-ISE Series 32000 Debugger. Compatibility

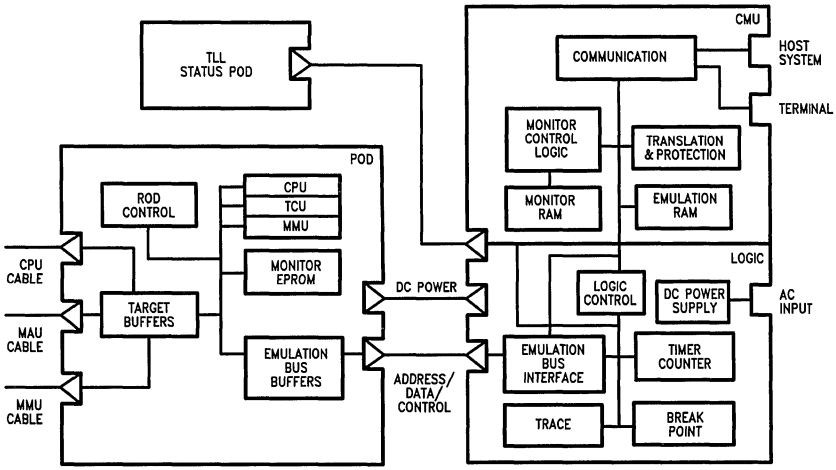


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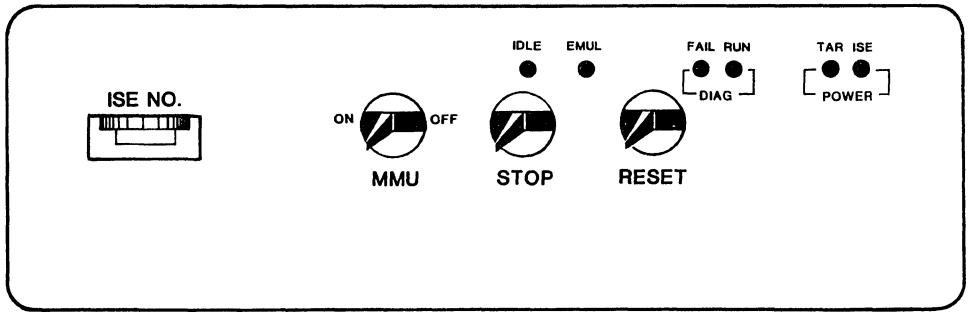
FIGURE 1. ISE32 Block Diagram



FRONT PANEL

TL/R/8522–3

FIGURE 2. ISE32 Controls and Indicators

minimizes the user's learning time of the various development tools. The ISE32 Debugger fully supports all the powerful debugging and emulation facilities provided by the ISE32 hardware, and supplements these features with a very powerful software-based program debugging environment.

The basic debugging features of the ISE32 are as follows:

(1) Supports both high-level and assembly languages*.

(2) Breakpoints can be set at the source code level, even when using high-level languages.*

(3) Supports symbolic debugging; variables can be referenced by their source code names.*

(4) Certain procedure parameters and variables are easily displayed.

(5) Structured data types and pointers are easily displayed.

(6) Supports both command and history files.

(7) Memory can be displayed in many different ways, including a disassembly mode displaying memory as NS32032 instructions.

(8) Supports all the emulation and debug facilities provided by the ISE32 hardware.

*Depends on host environment and language.

Modes of Operation

ISE32 can be set-up to operate in either stand-aside mode or transparent mode.

In stand-aside mode, one serial RS232 link from the host system is connected to the ISE32 while another serial RS232 from the host system is connected to the user's terminal. In this configuration, any of the host's users can access the ISE32.

In transparent mode, one serial RS232 link from the host system is connected to one serial port on the ISE32 while the user terminal is connected to a second serial port on the ISE32. In this configuration, only one serial port is required from the host system. In non-emulation mode, the ISE32 is transparent to the user, allowing normal communication between the user and the host system.

ISE32 Operation

Human Interface

ISE32 is easy to learn and easy to use. The software includes a complete on-line help facility. Invoking the

TABLE I. ISE32 Control and Indicator Functions

Control/Indicator	Function
ISE NO. Switch	Set to 0; other positions reserved.
MMU Switch	When ON, ISE32 enables MMU operation.
STOP Switch	Interrupts emulations, restores control to the ISE32 monitor.
RESET Switch	Resets the ISE32 hardware.
IDLE	Warning that POD CPU is in a wait state. (Time out)
EMUL	Indicates that ISE32 is executing the user's program.
FAIL	Warning that diagnostics have failed.
RUN	Indicates that ISE32 diagnostics are running.
TAR	Indicates that target power is on.
ISE	Indicates that ISE32 is on.

TABLE II. Status Pod Signal Description

Status Pod Label	ISE Function
Leads	
1-WHT-USRCLK-U	Not Used
2-BLK-GND	Common Ground
3-BRN-EXT0-U	EXT0 (external input 0)
4-RED-EXT1	EXT1 (external input 1)
5-ORN-EXT2	EXT2 (external input 2)
6-YEL-EXT3	EXT3 (external input 3)
7-GRN-EXT4	EXT4 (external input 4)
8-BLU-EXT5	EXT5 (external input 5)
9-VIO-EXT6	EXT6 (external input 6)
10-GRY-EXT7	EXT7 (external input 7)
11-WHT-USEBRK/U	IS (input sync)
Posts	
TBRUN	Not Used
BK SYNCH/-U	Output Sync
TR SYNCH/-U	Not Used
GND	Common Ground
TSYNC31/	Not Used
TSYNC21	Not Used
GND	Common Ground

"HELP" command gives a summary of all ISE32 commands, an individual command, or an individual commands parameters. This feature helps the user get his work done quickly with less frustration.

Emulation

The ISE32 unit has its own CPU, MMU, and TCU components. These components are connected to the target system via cables. These components perform the same functions, with close to the same timing characteristics as they would if mounted in the target system.* The ISE32 does not require wait states for operation.

Emulation memory, resident in the ISE32, can be used instead of target system memory. This feature is implemented by the mapping capabilities. With this feature, the ISE32 can run and debug programs without a working target system. User target memory from the entire address space of the CPU or MMU (whether it exists or not) can be mapped onto the ISE32 emulation memory in 4 kbyte blocks. The total amount of mapped memory cannot exceed 32 4 kbyte blocks (128 kbytes).

Associated with the emulation memory mapping scheme is a capability for read/write protection. Any 4 kbyte block within the address space of the CPU or MMU can be protected.

Generalized Events

To provide a versatile way of observing and controlling the significant state changes on the microprocessor, ISE32 allows the use and definition of "events". In general, a simple event is a breakpoint, a bus change, or a significant observation. An event can also be a logical combination of simple events (an Event-Expression).

Simple Event Definition

The simple events are:

— Breakpoints
— Latched Events
— Counter Done
— Status Pod Inputs
— Trace Done

Breakpoint Events

ISE32 provides four common breakpoint events, named A, B, C, and D. The breakpoint event can be used in two ways:

(1) Execution Breakpoint—occurs just prior to execution of an instruction at a specified address.
(2) Reference Breakpoint—occurs on a match when sampling:

— Address Bits
— Data Bits
— External Status Bits
— User/Supervisor Pin
— Byte Enable Pins
— Data Direction Pin
— Status Bits
— Interlock Bit
— Masked combinations of any of the above options.

Either virtual or physical addresses can be sampled. ISE32 also provides a range breakpoint event, R. The range breakpoint can be qualified by any of the above options within a specified address range.

Any breakpoint can cause emulation to stop immediately. Also, if used with the No Stop option, breakpoints can be combined with other events to cause a variety of action.

Event-Expressions

An event-expression is a Boolean expression made up of simple events, i.e., a logical combination of simple events. This allows the user to generate many different event combinations, tailored to system activity of particular interest to the user. These generalized events are used by many ISE32 commands such as stop, trace, event counting, etc. Event-expressions provide creative and flexible debugging procedures.

Event-expressions can be evaluated as either logically true or logically false. Valid logic operations for event expressions are: Negation (NOT), AND, and OR.

Stopping Execution on Events

A common debugging activity is to stop emulation on the occurrence of an event of interest. Stopping emulation puts ISE32 in the monitor mode so the user can examine and alter the state of the CPU, memory, and ISE32 functions. Emulation can be stopped on either simple events or event-expressions.

Flexible Tracing

ISE32 maintains a 1023-entry trace memory. Trace memory captures bus activity in one of two trace modes:

— Program Flow Trace
— Memory Bus Trace

Any combination of events can be used to qualify tracing. When enabled, tracing in either mode continues until a specified terminating event occurs. The actual end of tracing can be delayed after the terminating event by a count of 1 to 1023. This allows trace data to be captured before, after, or around the terminating event.

Program Flow Trace

The Program Flow Trace mode captures the CPU Program Counter address of 1023 non-sequential instructions. This mode also maintains a count of sequential instructions executed between each non-sequential instruction stored in the trace memory.

Memory Bus Trace

The Memory Bus Trace mode captures a summary of the following system parameters:

— Address bus contents

*Refer to ISE speed consideration section.

— Data bus contents
— CPU status (data transfer, non-sequential fetch, interrupt acknowledge, etc.)
— Time base counter contents
— PFS counter contents
— Status Pod external inputs
— States of the following CPU pins:
UNS—User/Not Supervisor
BE0–BE3—Byte Enable
DDIN—Data Direction In
NMI—Non-Maskable Interrupt
ILO—Interlock

Counters

The ISE32 contains two 32-bit counters with an overflow flag that may be used to count events, instruction cycles, memory cycles, or clock cycles. The counters may be programmed to start and stop counting on specific events. This permits counters to be used as timers to determine relative timing differences between various events. One use of this feature is to measure software or hardware performance. The counters may also be used to generate other ISE32 events upon completion of a count.

Event Trigger for External Test Equipment

ISE32 events can trigger external test equipment, such as oscilloscopes and logic analyzers. This test equipment can be used in conjunction with the ISE32's debugging features to solve system timing problems. The external trigger signal is available at the status pod output:

— BKSYNCH/-U (Output Sync)

Self-Test Diagnostics

At power-up, ISE32 runs a diagnostic program to verify ISE firmware integrity and proper hardware function.

ISE32 Timing Options

ISE32 includes the following timing options:

— Sampling time can be set to sample either virtual or physical addresses
— Status Pod external lines can be sampled at either data valid or address valid times
— The emulation clock frequency can be set to one of the following frequencies:
2.5 MHz
5.0 MHz
10.0 MHz
Target Board Frequency

ISE Speed Considerations

ISE32 utilizes standard, 10 MHz NS32032, NS32082 and NS32201 devices to perform control and emulation functions. When emulating, each device is connected to customer hardware via a target cable and associated cable transceivers. This arrangement delays the signal propagation between the Series 32000 components in the ISE32 POD and Series 32000 sockets in the customer hardware. These delays reduce timing margins in that hardware; i.e., combined propagation paths are lengthened by the ISE32 target cable and transceiver delays.

If sufficient timing margins are not restored, emulation may not be successful. In many cases, margin can be restored by reducing the emulation speed, lengthening the available time for signals to propagate. However, the exact speed reduction necessary to regain margins will depend on how Series 32000 components are used in the customer hardware. Tables III, IV and V list the combined cable and transceiver maximum propagation delay for each signal. It is the customer's responsibility to factor these delays with those of his own circuitry. In doing so, it can be determined whether ISE32 can reliably emulate with that circuitry.

Supported Configurations

This product is designed to work in most target systems configurations. However, certain design restrictions may apply. Refer to the ISE32 User's Manual for further information. (See "Documentation section")

Required User-Supplied Equipment

For use with SYS32™/GENIX™ Systems:

— Included with the GENIX Operating System Software Package.

For use with VR32/System V/Series 32000

— Included with the System V/32000 Operating System Software Package.

For use with VAX™/UNIX™ Systems:

— Valid DEC VAX-11™ configuration with available RS232 port.
— Berkeley UNIX 4.2 bsd Operating System.
— NSW-C-4VXR Series 32000 Cross Software Package.

For use with VAX/VMS™ Systems:

- Valid DEC VAX/11 configuration with available RS232 port.
- VMS™ Operating System, Version 4.2 or later.
- NSW-ASSEMB-9VMR or NSW-PASCAL-9VMR Series 32000 Cross Software Package.

Specifications

Environmental	Operating Temperature +10°C to +40°C Storage Temperature −20°C to +65°C	
Power	2.5A @ 115 VAC, 50/60 Hz, single phase 1.5A @ 220 VAC, 50/60 Hz, single phase. Approximately 1170 BTU.	
Physical		
ISE Support Box	Height:	5.8 in. (14.7 cm)
	Width:	18.5 in. (47.1 cm)
	Depth:	12.3 in. (31.2 cm)
Emulation Pod	Height:	2.1 in. (5.3 cm)
	Width:	9.3 in. (23.6 cm)
	Depth:	10.0 in. (25.4 cm)

Specifications (Continued)

TTL Status Pod
Height: 1.0 in. (2.5 cm)
Width: 3.125 in. (7.9 cm)
Depth: 6.125 in. (15.6 cm)

Cable Lengths
ISE Support Box to Emulation Pod: 4.0 ft. (1.22M)
ISE Support Box to TTL Status Pod: 6.0 ft. (1.83M)
Emulation Pod to Target Board: 1.0 ft. (0.30M)

Target Interface Electrical Characteristics— See Tables III through V.

Order Information

Complete ISE32 Units

NSS-ISE32	ISE32 (NS32032), 115 VAC
NSS-ISE32E	ISE32 (NS32032), 220 VAC

TABLE III. Electrical Characteristics for TCU Interface

Signal Name	Interface Device	Input And/Or Output Current		Propagation Delay Time T_{pd}*
Outgoing Signals		I_{OH}	I_{OL}	
NTSO	74ALS244	15 mA	†48 mA	12.4 ns
CTTL	74ALS244	15 mA	†48 mA	12.4 ns
FCLK	74ALS244	15 mA	†48 mA	12.4 ns
NDBE	74ALS244	15 mA	†48 mA	12.4 ns
NRD	74ALS244	15 mA	†48 mA	12.4 ns
NWR	74ALS244	15 mA	†48 mA	12.4 ns
NRSTO	74ALS244	15 mA	†48 mA	12.4 ns
RDY	74ALS244	15 mA	†48 mA	12.4 ns
Incoming Signals		I_{IH}	I_{IL}	
NPER	74F244	20 μA	1.6 mA	7.9 ns
NCWAIT	74F244	20 μA	1.6 mA	7.9 ns
NWAIT1	74ALS244	20 μA	0.1 mA	12.4 ns
NWAIT2	74ALS244	20 μA	0.1 mA	12.4 ns
NWAIT4	74F244	20 μA	1.6 mA	14.5 ns
NWAIT8	74ALS244	20 μA	0.1 mA	12.4 ns
XCTL1	74F244	20 μA	1.6 mA	7.9 ns
NRWEN	74F244	20 μA	1.6 mA	7.9 ns
NRST1	74ALS244	20 μA	0.1 mA	12.4 ns

*Interface device, plus cable.
†For V_{CC} maintained between 4.75V and 5.25V.

TABLE IV. Electrical Characteristics for MMU Interface

Signal Name	Interface Device	Input And/Or Output Current				Propagation Delay Time T_{pd}*
		I_{OH}	I_{OL}	I_{IH}	I_{IL}	
BIDIRECTIONAL SIGNAL						
NPAV	74ALS245	15 mA	†48 mA	20 μA	0.1 mA	11.4 ns
OUTGOING SIGNALS						
A24	74ALS244	15 mA	†48 mA	—	—	12.4 ns
MMUINT	74ALS244	15 mA	†48 mA	—	—	12.4 ns
NABT	74ALS244	15 mA	†48 mA	—	—	12.4 ns
NFLT	74ALS244	15 mA	†48 mA	—	—	12.4 ns
NHLDAO	74ALS244	15 mA	†48 mA	—	—	12.4 ns
INCOMING SIGNALS						
NHOLD	74LS126	—	—	20 μA	0.4 mA	19.4 ns

*Interface device, plus cable.
†For V_{CC} maintained between 4.75V and 5.25V.

TABLE V. Electrical Characteristics for CPU Interface

Signal Name	Interface Device	Input And/Or Output Current				Propagation Delay Time
		I_{OH}	I_{OL}	I_{IH}	I_{IL}	T_{pd}*
BIDIRECTIONAL SIGNAL						
NSPC	74ALS245	15 mA	†48 mA	20 μA	0.1 mA	12 ns
AD00	74ALS245	15 mA	†48 mA	20 μA	0.1 mA	12 ns
AD01	74ALS245	15 mA	†48 mA	20 μA	0.1 mA	12 ns
AD02	74ALS245	15 mA	†48 mA	20 μA	0.1 mA	12 ns
AD03	74ALS245	15 mA	†48 mA	20 μA	0.1 mA	12 ns
AD04	74ALS245	15 mA	†48 mA	20 μA	0.1 mA	12 ns
AD05	74ALS245	15 mA	†48 mA	20 μA	0.1 mA	12 ns
AD06	74ALS245	15 mA	†48 mA	20 μA	0.1 mA	12 ns
AD07	74ALS245	15 mA	†48 mA	20 μA	0.1 mA	12 ns
AD08	74ALS245	15 mA	†48 mA	20 μA	0.1 mA	12 ns
AD09	74ALS245	15 mA	†48 mA	20 μA	0.1 mA	12 ns
AD10	74ALS245	15 mA	†48 mA	20 μA	0.1 mA	12 ns
AD11	74ALS245	15 mA	†48 mA	20 μA	0.1 mA	12 ns
AD12	74ALS245	15 mA	†48 mA	20 μA	0.1 mA	12 ns
AD13	74ALS245	15 mA	†48 mA	20 μA	0.1 mA	12 ns
AD14	74ALS245	15 mA	†48 mA	20 μA	0.1 mA	12 ns
AD15	74ALS245	15 mA	†48 mA	20 μA	0.1 mA	12 ns
AD16	74ALS245	15 mA	†48 mA	20 μA	0.1 mA	12 ns
AD17	74ALS245	15 mA	†48 mA	20 μA	0.1 mA	12 ns
AD18	74ALS245	15 mA	†48 mA	20 μA	0.1 mA	12 ns
AD19	74ALS245	15 mA	†48 mA	20 μA	0.1 mA	12 ns
AD20	74ALS245	15 mA	†48 mA	20 μA	0.1 mA	12 ns
AD21	74ALS245	15 mA	†48 mA	20 μA	0.1 mA	12 ns
AD22	74ALS245	15 mA	†48 mA	20 μA	0.1 mA	12 ns
AD23	74ALS245	15 mA	†48 mA	20 μA	0.1 mA	12 ns
D24	74ALS245	15 mA	†48 mA	20 μA	0.1 mA	12 ns
D25	74ALS245	15 mA	†48 mA	20 μA	0.1 mA	12 ns
D26	74ALS245	15 mA	†48 mA	20 μA	0.1 mA	12 ns
D27	74ALS245	15 mA	†48 mA	20 μA	0.1 mA	12 ns
D28	74ALS245	15 mA	†48 mA	20 μA	0.1 mA	12 ns
D29	74ALS245	15 mA	†48 mA	20 μA	0.1 mA	12 ns
D30	74ALS245	15 mA	†48 mA	20 μA	0.1 mA	12 ns
D31	74ALS245	15 mA	†48 mA	20 μA	0.1 mA	12 ns
NNDIN	74ALS245	15 mA	†48 mA	20 μA	0.1 mA	12 ns
NADS	74ALS245	15 mA	†48 mA	20 μA	0.1 mA	12 ns
NBE0	74ALS245	15 mA	†48 mA	20 μA	0.1 mA	12 ns
NBE1	74ALS245	15 mA	†48 mA	20 μA	0.1 mA	12 ns
NBE2	74ALS245	15 mA	†48 mA	20 μA	0.1 mA	12 ns
NBE3	74ALS245	15 mA	†48 mA	20 μA	0.1 mA	12 ns

*Interface device, plus cable.
†For V_{CC} maintained between 4.75V and 5.25V.

Signal Name	Interface Device	Input And/Or Output Current		Propagation Delay Time
Outgoing signals		I_{OH}	I_{OL}	T_{pd}*
NILO	74ALS244	15 mA	†48 mA	13.0 ns
ST0	74ALS244	15 mA	†48 mA	13.0 ns
ST1	74ALS244	15 mA	†48 mA	13.0 ns
ST2	74ALS244	15 mA	†48 mA	13.0 ns
ST3	74ALS244	15 mA	†48 mA	13.0 ns
NPFS	74ALS244	15 mA	†48 mA	13.0 ns
UNS	74ALS244	15 mA	†48 mA	13.0 ns
BB	74ALS244	15 mA	†48 mA	13.0 ns
NDS	74ALS244	15 mA	†48 mA	13.0 ns
NBRO	74F244	15 mA	†48 mA	8.5 ns
NHLDA	74ALS244	15 mA	†48 mA	13.0 ns
Incoming signals		I_{IH}	I_{IL}	
TGTPC	—	—	—	—
NINTC	74ALS244	20 mA	0.1 mA	13.0 ns
NMI	74ALS244	20 mA	0.1 mA	19.6 ns
NBRI	74F244	20 mA	1.6 mA	8.5 ns
NHOLDC	74ALS244	20 mA	0.1 mA	19.6 ns

*Including internal logic, interface device, and cable.
†For V_{CC} maintained between 4.75V and 5.25V.

Documentation

NSP-ISE32GNX-M ISE32 User's Manual for SYS32/GENIX and VAX/UNIX operation. (Included with the appropriate Series 32000 support/cross-support software package.)

NSP-ISE32COF-M ISE32 User's Manual for VR32/System V/Series 32000 operation. (Included with the appropriate Series 32000 support software package.)

NSP-ISE32VMS-M ISE32 User's Manual for VAX/VMS operation. (Included with the appropriate Series 32000 cross-support software package.)

ISE32 Debugger Command Summary

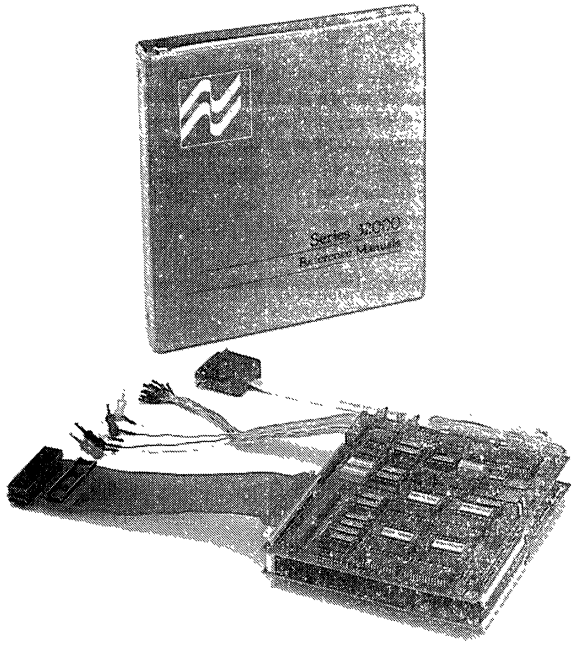
The following comprehensive list of ISE32 Debugger commands is in alphabetical order. Refer to the ISE32 User's Manual for a detailed description of each command.

Command	Function
Begin	Load the program into memory and initializes registers.
Breakpoint Create	Creates breakpoint A, B, C, D at specified address or, creates RANGE breakpoint at specified address range.
Breakpoint Delete	Deletes specified breakpoint.
Breakpoint Print	Print address and conditions of specified breakpoints.
Breakpoint Revive	Revives specified breakpoint.
Indirect File	Executes command file or debugger string.
Debugger String	Sets debugger string.
Define Counter	Defines set up for ISE counter 1 or 2.
Define Latch	Defines the latch 0 or latch 1 event.
Define Output Sync	Defines output sync event.
Define Stop	Defines stop event.
Define Trace	Defines the end, delay, and trace mode parameter for trace.
Disassemble	Disassembles instructions.
Go	Starts execution of the program.
Help	Displays general help.
In	Checks that the contents of address or register are within a specified range.
List Calls	List entries in a call.
List Definition	Lists current definitions.
List Files	Lists nine entries of a selected file.
List Information	Lists current ISE status.
List Modules	Lists modules in current program.
List Strings	Lists current debugger string values.
List Trace	Lists nine trace entries.
Map Create	Maps and/or protects 4 kbyte blocks in a specified address range.
Map Print	Prints current mapping.
Memory Fill	Fills specified address range with value.

Command	Function
Memory Move	Moves memory content from address range to address range.
Memory Search	Searches for value.
On	Sets idbg32 response on condition.
Print	Prints content of address range or registers.
Print Address	Prints absolute address and module area associated with address.
Protection Create	Creates protection/ translation for pages specified by address range.
Protection Print	Prints protection level status.
Quit	Terminates session.
Repeat	Repeats previous command.
Replace	Replaces content of address or register.
Select Echo	Selects echo mode.
Select Full	Selects full symbolic PC.
Select History	Selects history file.
Select Link	Selects communication channel.
Select Module	Selects module.
Select Options	Select current ISE operation option.
Select Radix	Select global radix.
Step	Execute specified number of machine instructions.
Step Call	Executes until a call or return.
Step Down	Executes one instruction inside a procedure, skips over call instructions.
Step Instruction	Executes specified number of instructions inside a module.
Step Until	Executes instructions until contents of address or register are within specified value.
Step While	Executes instructions while contents of address or register are within specified value.

National Semiconductor

SPLICE Development Tool



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- **Download capabilities via serial connections**
- **256 Kbytes of mappable memory**
- **Optional 1-Mbyte memory board, expands memory up to 8 Mbytes**
- **On-board monitor with power-on diagnostics**
- **Supports Series 32000 CPUs, including: NS32332 NS32CG16 NS32032 NS32C032 NS32016 NS32C016 NS32008**
- **Parallel I/O port reserved for future highspeed download capabilities**
- **Programmable serial port baud rates**
- **CPU bus status test points for logic analyzer connections**
- **4 LED indicators for diagnostic results and general user applications**
- **RESET and NMI push buttons**
- **15 MHz maximum operation**

1.0 Product Overview

The SPLICE Development Tool provides a communication link between a Series 32000 target and a development system host. This connection allows users to download and map their software onto target memory and then debug this software using National Semiconductor's debuggers.

SPLICE includes two RS232 serial ports for the system host/terminal. These ports are particularly useful for target systems that have no serial ports, such as embedded controller designs.

SPLICE is also useful for designs with ROM-based software, or designs whose memory portion has not yet been built. SPLICE provides 256 Kbytes of SRAM which users can map into target memory. Using mapped memory considerably reduces software development time.

SPLICE also uses the target system's chipset. This cost-effective feature is achieved through the use of CPU and MMU target cables.

2.0 Description of Features

2.1 PHYSICAL DESCRIPTION

The SPLICE logic board is a 7″ by 9″ printed circuit board that is the base unit for all operating configurations. Accessory parts include an expansion memory board and target cables (see Sections 2.4 and 2.6).

Figure 2 shows the physical layout of the SPLICE logic board. Each of these features are discussed in the following sections.

2.2 SERIAL CONNECTORS

SPLICE provides two serial ports (P5 and P6) for connection to a terminal/host. SPLICE also supplies RS232 cables for connecting SPLICE to the host/terminal (see Section 3 for connection diagrams). These ports are jumper configurable for DTE (Data Terminal Equipment) or DCE (Data Communication Equipment). DSR/DTR or CTS/RTS handshaking may also be selected.

2.3 MEMORY

The SPLICE logic board contains 256 Kbytes of Static RAM. Each of the 32k x 8-bit memory devices has 150 ns access times. The memory capacity of SPLICE may be increased by adding 1 MByte memory expansion boards (see Section 2.4). When using memory expansion boards, the SPLICE on-board RAM is disabled.

Regardless of the amount of memory used, SPLICE divides the memory into 4 equal, separate banks. Each bank may be mapped at non-overlapping starting addresses using the SPLICE, PROM-based monitor or DBG commands. See the GNX Symbolic Debuggers's Reference Manual (Publication No. 424510899-001A) or SPLICE Hardware Reference Manual for details.

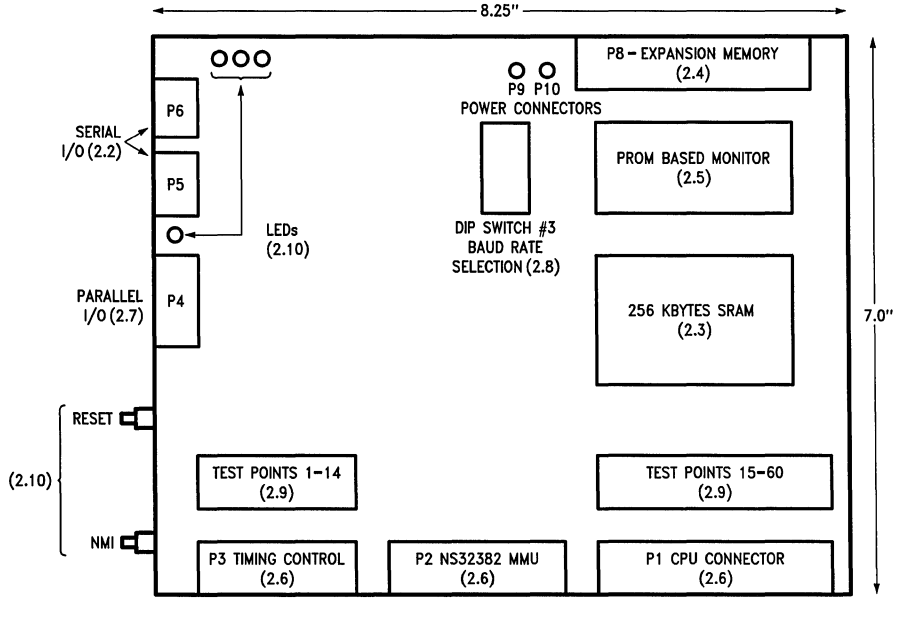
The SPLICE monitor and I/O addressing occupy 256 Kbytes of memory. This block of memory will boot up at address zero. The user may relocate these 256 Kbytes to any address; if this block of memory is relocated, SPLICE requires 2 Kbytes of the first 64 Kbytes of RAM for a scratch pad area.

2.4 MEMORY EXPANSION

1-Mbyte memory expansion boards are available as an option to the user. SPLICE supports expansion up to 8 Mbytes, in the following configurations only:

SPLICE with 1 memory board,
with 2 memory boards,
with 4 memory boards,
or with 8 memory boards.

The memory boards connect beneath the SPLICE logic board to a 94-pin connector, P8. When using memory expansion boards, the SPLICE on-board memory is disabled.



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Numbers in parenthesis indicate text sections

FIGURE 2. SPLICE Logic Board

2.0 Description of Features (Continued)

2.5 MONITOR

Four EPROMs contain the monitor firmware. When power is initially applied (cold boot) to SPLICE, the monitor performs four diagnostic tests. The diagnostics test the ROM, RAM, mapping RAM and UART.

If a failure is detected, a message code will appear on the LEDs and on the terminal. Refer to the SPLICE Hardware Reference Manual for explanation of error codes.

The main function of the monitor is to interpret and handle commands from the terminal or debugger. The SPLICE monitor communicates with National's Symbolic Debugger, DBG32. DBG32 resides on a development system host, as part of the GENIX™ Native and Cross (GNX) Language Tools, Release 2, revision C, or a subsequent revision of GNX functions with SPLICE.

Some of the features of DBG32 include:

— Assembly and mixed-language program debugging,
— Symbolics
— Source-level debugging
— Single stepping, breakpoints
— Multimodule program debugging
— Variety of Radixes
— Indirect files and History files
— On-line help facility

Refer to the GNX Symbolic Debugger's Reference Manual or the GNX datasheet for details.

2.6 CABLE DESCRIPTION

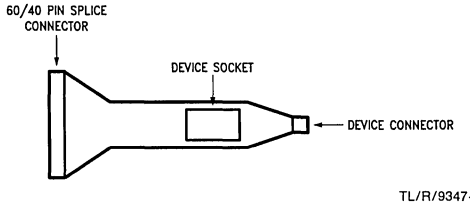
Two different cables are supplied to connect SPLICE with the target hardware: flexible printed circuit cable for CPU/MMU signals and a twisted pair, flying lead cable for timing control signals. Both types of cables are detailed in the following text.

CPU/MMU CABLES

Depending on the target design, SPLICE requires one or more of the following cables:

NS32332 CPU cable
NS32032/C032 CPU cable
NS32016/C016/008 CPU cable
NS32CG16 CPU cable
NS32382 MMU cable

Figure 3 shows the basic layout of the flex cable.



Top View

FIGURE 3. Flexible Printed Circuit Cable

The "device connector" is inserted into the user's target socket, replacing the user's device. The user's device plugs into the "device socket." At the opposite end of the flex cable is a 60 pin connector for CPUs, or a 40 pin connector for the NS32382 MMU. These are installed on P1 and P2, respectively, on SPLICE. Targets using the NS32082 MMU do not require a cable.

Refer to the Hardware Reference Manual for more details on the wiring, installation, and handling of cables.

TIMING CONTROL CABLE

The timing control cable is a twisted pair cable consisting of 26 flying leads. The following table lists the signals, pin numbers, and functional decription of each signal. This cable connects to P3 on SPLICE. Section 3.2 describes how to connect this cable to the target.

2.0 Description of Features (Continued)

Signal	Pin	I/O	Functional Description
$\overline{\text{PAV}}$	1	I	Used to latch the address information from the CPU's AD bus when the NS32082 MMU is installed. **NOTE:** When the NS32382 MMU is used, the MMU's $\overline{\text{PAV}}$ pin is connected to SPLICE via the 382 MMU cable, and it is not necessary to connect this signal.
CTTL	3	I	A TTL compatible version of the PHI1 clock signal.
082RDYIN	5	I	When installing SPLICE, the signal that normally is connected to the ready input of the 082 MMU should be disconnected and connected to the SPLICE via P3–5.
082RDOUT	7	O	The output generated from SPLICE, after receiving the 082 ready input and ANDing it with SPLICE's ready signal, is connected to the ready input of the 082 MMU.
$\overline{\text{RSTIN}}$	9	I	A Schmitt triggered input connected to the reset circuitry of the target system.
$\overline{\text{RSTOUT}}$	11	O	An active low, CMOS level synchronous reset output generated by ANDing the $\overline{\text{RSTIN}}$ signal with the SPLICE's reset circuitry output. The $\overline{\text{RSTOUT}}$ signal should be used to reset the target's circuitry.
BDEN	13	O	Active high Board Enable output. When asserted, the SPLICE ROM/IO or RAM is accessed. This signal is connected to the user's target to disable the buffers and drivers of the CPU's address/data bus.
$\overline{\text{BDEN}}$	15	O	Complementary output of BDEN.
BBDEN	17	O	CMOS level version of BDEN.
$\overline{\text{BBDEN}}$	19	O	Complementary output of BBDEN.
$\overline{\text{INT}}$	21	O	A CMOS level output generated by the DUART asserted whenever the DUART is ready to transmit or receive.
$\overline{\text{DACK}}$	23	O	An open-collector signal driven low when BDEN is asserted and SPLICE's data buffers are enabled.
$\overline{\text{TRIG1}}$	25	O	A TTL level output signal driven by the DUART's output port bit 2 on SPLICE. The user may program the state of this output using a special supervisory call.
$\overline{\text{TRIG2}}$	26	O	Like $\overline{\text{TRIG1}}$, this is a TTL output signal driven by the DUART's output port 3 on SPLICE. The SPLICE monitor will drive this bit low during the monitor mode and set when running the user program.

2.7 PARALLEL I/O INTERFACE

P4 has been reserved for a future high speed download connection.

2.8 PROGRAMMABLE BAUD RATES

Various baud rates can be selected by setting positions 1, 2 and 3 of DIP switch 3 as follows:

Baud Rate	SW3-1	SW3-2	SW3-3
19200	on	on	on
9600	off	on	on
4800	on	off	on
2400	off	off	on
1800	on	on	off
1200	off	on	off
600	on	off	off
300	off	off	off

2.9 TEST POINTS

SPLICE has 60 test points which allow the user to trace, using a logic analyzer, the CPU's bus activity.

Test Points	Signals
1–14	P3-Timing Control Signals
15–46	AD Bus Signals
47–60	Control Signals from CPU

2.10 INDICATORS AND PUSH BUTTONS

SPLICE uses 4 LEDs to indicate failures during power-on diagnostics. The programmer may also use these as general purpose indicators.

Two push buttons are on the SPLICE logic board: NMI and RESET. The reset circuit is jumper configurable to originate from SPLICE reset or the target reset.

2.11 OPERATING SPEEDS

SPLICE operates at up to 15 MHz. When operating from target memory, full speed operation may be achieved. However, when accesses are made to SPLICE memory or the UART, wait states are required. The following is a table of required wait states:

ROM/UART	RAM	FREQ. (MHz)
1	0	6
2	1	10
3	1	15

3.0 Required Operating Environment

In addition to the logic board and CPU/MMU cables, SPLICE requires the following equipment:

— A regulated +5 VDC power supply capable of supplying a 4A minimum

— A host computer system with NSC's GENIX Native and Cross (GNX) Development Tools, Release 2, revision C or later

— An RS232 compatible terminal

The following sections describe how to connect SPLICE to the user's target and host.

3.1 SPLICE/HOST INTERFACE

SPLICE connects to the development host through RS232 cable(s). The monitor on SPLICE will interface with any host that has a DBG32. DBG32 is a symbolic debugger available in the GENIX Native and Cross Support (GNX) Development Tools software package. The SPLICE monitor functions with GNX Tools R2 rev. C or later.

SPLICE can be connected to the host in one of two ways: Stand-aside mode or Transparent mode. Stand-aside mode is used when only one serial port is available from the host for SPLICE operation *(Figure 4)*. Stand-aside mode is also convenient when SPLICE needs to be shared by different users.

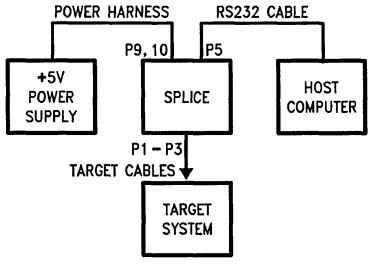


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FIGURE 4. Stand-Aside Mode

Transparent mode is useful for remote hosts. Transparent mode uses both serial ports (P5 and P6), as shown in *Figure 5*.

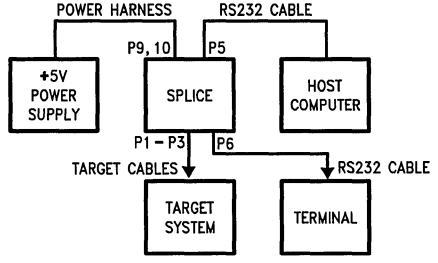

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FIGURE 5. Transparent Mode

3.2 SPLICE/TARGET INTERFACE

SPLICE connects to the user target through P1, P3, and if the NS32382 MMU is used, P2. P1 connects to the CPU cable which is, in turn, connected to the target CPU socket. P2 connects to the NS32382 MMU cable. P3 connects to the timing control cable. A minimum of five timing control signals must be connected to operate with SPLICE: CTTL, $\overline{\text{RSTIN}}$, $\overline{\text{RSTOUT}}$, BDEN, and $\overline{\text{PAV}}$. SPLICE taps onto CTTL and $\overline{\text{PAV}}$ directly. $\overline{\text{RSTIN}}$ and $\overline{\text{RSTOUT}}$ will require the designer to disconnect the target reset circuitry and route it through SPLICE. BDEN is the most important signal. An extra OR gate (see *Figure 6B, G1*) is required to OR the target board enable with the SPLICE board enable. ORing these signals together prevents bus collisions. The target board enable is taken from the CPU data buffers; the SPLICE board enable is P3–13, –14, –15, or –16 of the timing control cable.

IMPORTANT: The target's CPU data buffers must be disabled to operate with SPLICE.

Other signals may be required, depending on the target design. (Refer to Section 2.6 for details on other timing control cable signals.) When designing a board for use with SPLICE, the designer should allow easy access to these signals.

Figure 6 illustrates how to connect the timing control cable to a typical NS32016 target. *Figure 6A* shows a typical circuit, and *Figure 6B* shows the target connected to SPLICE.

4.0 Specifications/Characteristics

Environment

SPLICE is designed to operate in a laboratory environment. Sufficient air flow must be allowed to ensure all components stay within their specified temperature range.

Temperature:	Operative 0°C to 55°C
	Non-operative −40°C to +60°C
Humidity	10% to 90% relative, non-condensing
Altitude	Operative 15,000 feet

Power Requirements

SPLICE requires a regulated +5 VDC power source capable of supplying a 4A minimum. SPLICE has a DC–DC converter which generates the +12 VDC and −12 VDC required by the RS232 interface drivers.

DC Characteristics

Table 1 lists the DC characteristics for the logic circuits on SPLICE.

AC Characteristics

Table 2 lists the AC characteristics for the signals of the SPLICE circuits. *Figure 7* illustrates SPLICE access timing, RDY circuit timing, READ timing, NMI timing, and $\overline{\text{BACKOUT}}$ timing.

4.0 Specifications/Characteristics (Continued)

TABLE 1. DC Characteristics of I/O Signals

Signal	Max Input Current (μA)		Min Output Current (mA)		Max Input Cap. (pF)
	I_{IH}	I_{IL}	I_{OH}	I_{OL}	
AD0–AD16	25	105	6.0	6.0	30
AD16–AD31	50	755	6.0	6.0	35
PA0–PA15	20	100	—	—	5
PA16–PA31	45	750	—	—	10
PD0–PD7	50	500	15.0	64.0	5
$\overline{\text{ADS}}$ $\overline{\text{PAV}}$	20	500	—	—	5
CTTL (1) (2)	80 20	2000 500	— —	— —	20 5
$\overline{\text{RSTIN}}$	20	600	—	—	5
BW0 BW1	20	600	—	—	5
$\overline{\text{BE1}}$ $\overline{\text{BE2}}$ $\overline{\text{BE3}}$ $\overline{\text{HBE}}$	50	700	—	—	5
$\overline{\text{FLT}}$	25	250	—	—	5
$\overline{\text{DDIN}}$	1	1	—	—	10
$\overline{\text{BACKIN}}$	20	500	—	—	5
$\overline{\text{NMIN}}$	25	250	—	—	5
$\overline{\text{MATN}}$ $\overline{\text{SATN}}$	50	400	15.0	64.0	5
$\overline{\text{MACK}}$ $\overline{\text{SACK}}$	50	400	15.0	64.0	5
RDYOUT	—	—	2.0	20.0	—
082RDYOUT	—	—	2.0	20.0	—
$\overline{\text{RSTOUT}}$	—	—	6.0	6.0	—
$\overline{\text{BACKOUT}}$	—	—	2.0	20.0	—
$\overline{\text{NMIOUT}}$	—	—	1.0	20.0	—
$\overline{\text{INT}}$	—	—	6.0	6.0	—
$\overline{\text{TRIG1}}$	—	—	0.4	2.4	—
$\overline{\text{TRIG2}}$	—	—	0.4	2.4	—
$\overline{\text{BDEN}}$	—	—	2.0	20.0	—
BDEN	—	—	2.0	20.0	—
$\overline{\text{BBDEN}}$	—	—	6.0	6.0	—
BBDEN	—	—	6.0	6.0	—
PDIR	—	—	30.0	64.0	5
$\overline{\text{PRESET}}$	—	—	30.0	64.0	5

NOTE: (1) When W8 A-B is connected.
(2) When W8 B-C is connected.

4.0 Specifications/Characteristics (Continued)

TABLE 2. AC Characteristics of SPLICE

Name	Figure	Description	Ref/Conditions	Min	Typ	Max	Units
t_{CP}	7A	Clock Period	Rising Edge CTTL to Next Rising Edge CTTL	50.0			ns
t_{BDENAV_a}	7A	BDEN Active (High)	After Address Valid		27.0	33.5	ns
t_{BDEN_a}	7A	BDEN Active (High)	After $\overline{ADS}$ or $\overline{PAV}$ Active (Low)		34.0	44.0	ns
$t_{\overline{BDEN}_a}$	7A	$\overline{BDEN}$ Active (Low)	After BDEN Active (High)		6.0	8.0	ns
t_{BBDEN_a}	7A	BBDEN Active (High)	After BDEN Active (High)		15.0	25.0	ns
$t_{\overline{BBDEN}_a}$	7A	$\overline{BBDEN}$ Active (Low)	After BDEN Active (High)		21.0	33.0	ns
$t_{RDY_{ia}}$	7A	RDYOUT Inactive (Low)	After BDEN Active (High)		8.0	10.5	ns
t_{332RDY_a}	7B	RDYOUT Active (High) for 32332	After Rising Edge CTTL		9.0 12.5	11.8* 16.8**	ns
t_{RDY_a}	7B	RDYOUT Active (High) for 32008/016/032	After Rising Edge CTTL		7.5 11.0	10.5** 15.5**	ns
t_{AADS_n}	7A	Address Bits 0–31 Hold From	After $\overline{ADS}$ Inactive (High)	4.5			ns
t_{RAM_r}	7D	RAM Data Valid	After Address Valid			246	ns
t_{PROM_r}	7D	PROM Data Valid	After Address Valid			348	ns
$t_{\overline{DACK}_a}$	7B	$\overline{DACK}$ Active (Low)	After Rising Edge CTTL		19.0	27.0	ns
$t_{\overline{NMI}}$	7C	$\overline{NMIOUT}$ Active/Inactive	After Rising Edge CTTL		15.0	25.0	ns
$t_{\overline{BACKOUT}_a}$	7E	$\overline{BACKOUT}$ Active (Low)	After $\overline{BACKIN}$ Active (Low)	2.0		5.8	ns
$t_{\overline{BACKOUT}_{ia}}$	7E	$\overline{BACKOUT}$ Inactive (High)	After $\overline{BACKIN}$ Inactive (High)	1.0		5.8	ns

*W8 A-B connected

**W8 B-C connected

6

4.0 Specifications/Characteristics (Continued)

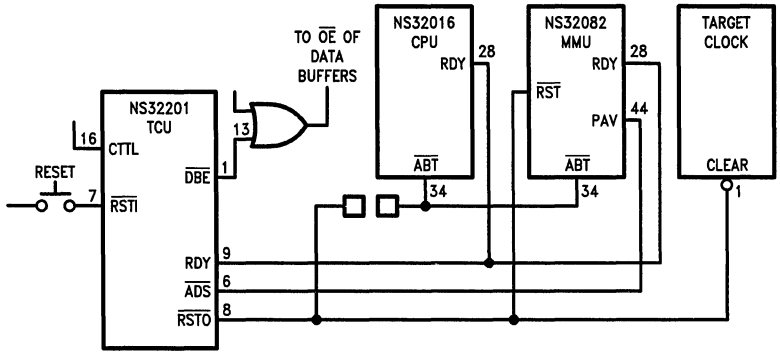

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FIGURE 6A. Typical Circuitry for a NS32016 Target

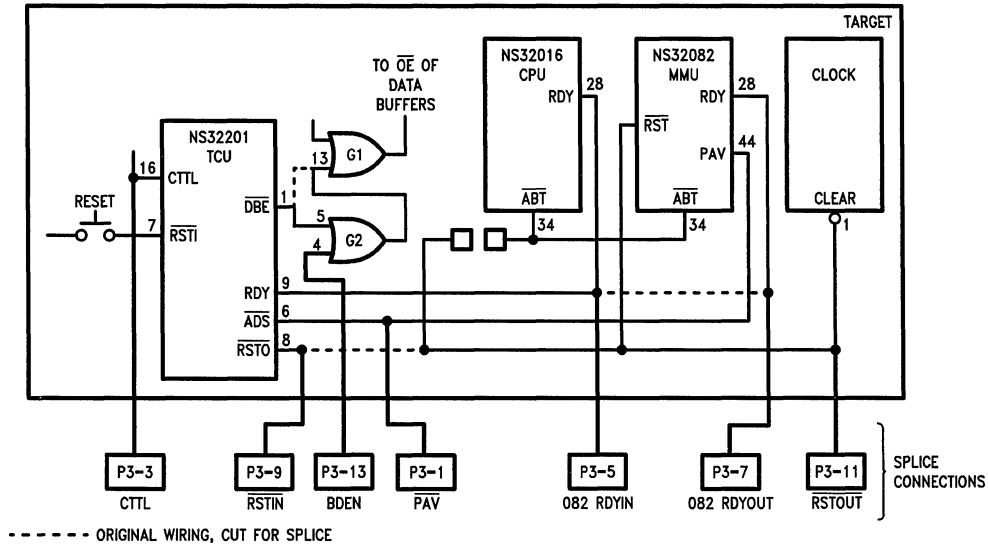

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FIGURE 6B. Modified NS32016 Target, with SPLICE Connections

4.0 Specifications/Characteristics (Continued)

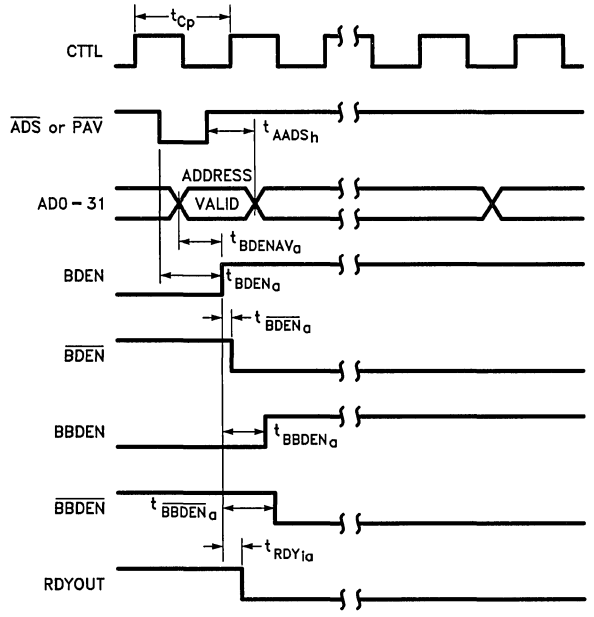

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FIGURE 7A. SPLICE Access Timing

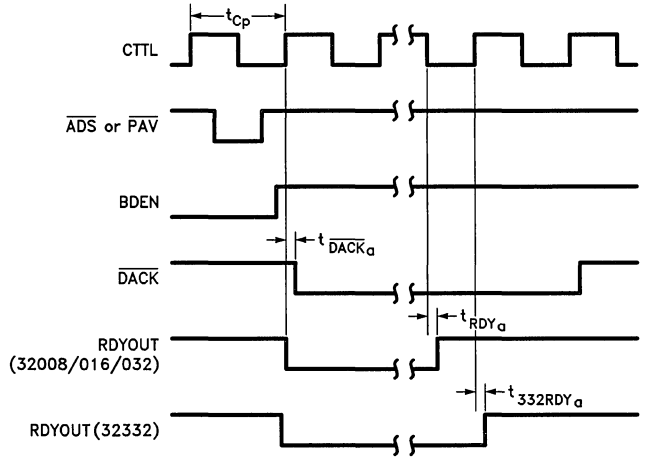

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FIGURE 7B. RDY Circuit Timing

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4.0 Specifications/Characteristics (Continued)

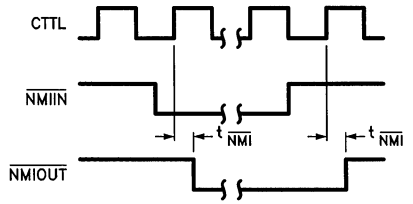

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FIGURE 7C. NMI Timing

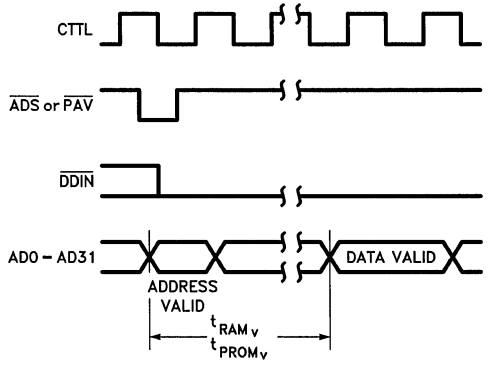

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FIGURE 7D. READ Timing

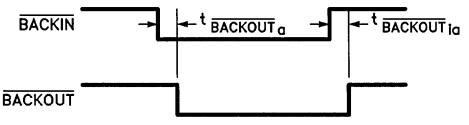

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FIGURE 7E. Timing of $\overline{\text{BACKOUT}}$ when SPLICE is not Accessed

5.0 Ordering Information

SPLICE Logic Boards:

NSV-SPLICE-256	SPLICE logic board and 256 Kbytes of on-board memory.
NSV-SPLICE-1MB	SPLICE logic board with 1-Mbyte memory expansion board instead of 256 Kbytes of on-board memory.

SPLICE logic boards ship with the following:

- SPLICE logic board
- 2 RS232 connectors
- 2 female-to-female connectors
- Power supply cable
- Timing control cable and clips
- Stand offs
- SPLICE User's Manual
- SPLICE schematics

Note: Memory expansion boards disable 256 Kbytes of memory on the logic board. Users whose applications require more than 256 Kbytes of memory should order part number NSV-SPLICE-1MB. This configuration ships without the 256 Kbytes of SRAM on the logic board and with a 1-Mbyte expansion board.

ACCESSORIES

NSV-SPLC-MEM-BD	1-Mbyte expansion memory board
NSV-SPLCBL-016	SPLICE cable for the NS32016/C016/008 CPU
NSV-SPLCBL-032	SPLICE cable for the NS32032/C032 CPU
NSV-SPLCBL-CG16	SPLICE cable for the NS32CG16 CPU
NSV-SPLCBL-332	SPLICE cable for the NS32332 CPU
NSV-SPLCBL-382	SPLICE cable for the NS32382 MMU

Note: The part numbers are the same for NS32016 and NS32008 CPU cables since both parts have the same pinouts.

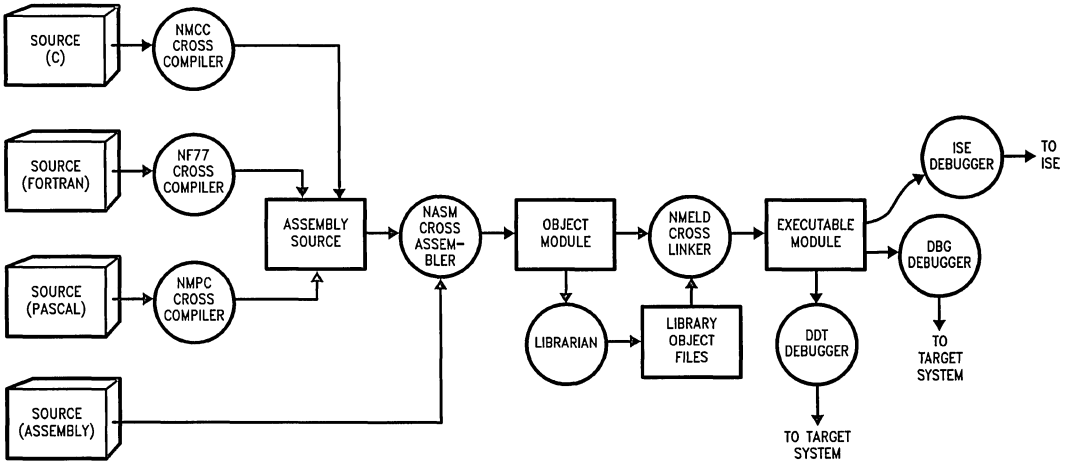
Section 7

Software Support

Section 7 Contents

National Semiconductor

Series 32000® GENIX™ Native and Cross-Support (GNX™) Language Tools (Release 2)



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- **Implements AT&T's standard Common Object File Format (COFF)**
- **Optimizing C Compiler (optional)**
- **Optimizing FORTRAN 77 Compiler (optional)**
- **Pascal Compiler (optional)**
- **Series 32000 assembler and linker**
- **In-System Emulator Support**
- **Interactive remote debugger with helpful command interface**
- **Available in binary for the VAX™ UNIX® 4.3 bsd operating system under derivatives of the Berkeley operating system**
- **Available in binary for the VAX/VMS™ operating system**
- **Available in binary on National Semiconductor Series 32000 Systems**
- **Available in source for porting to other operating system environments**

Product Overview

The Series 32000 GNX Language Tools are a set of software development tools for the Series 32000 microprocessor family. Optional high-level language compilers work in conjunction with the standard components to provide tools that can be combined to meet a variety of development needs.

GENIX Native and Cross-Support (GNX) Language Tools

The Series 32000 GNX Language Tools are based on AT&T's Common Object File Format (COFF). With appropriate command-line arguments and when linked with appropriate libraries, code generated by the GNX language tools can be executed in any Series 32000 target environment. In addition, these tools can be used to develop operating-system-independent code or code designed to run in conjunction with real-time kernels, such as National's EXEC and VRTX®/Series 32000. All of National's new language tools conform to the COFF file format, thereby ensuring that modules produced by any one set of tools can be linked with objects produced by any other set of GNX tools.

7

Standard Components

nasm	an assembler for GNX assembly language source code (produced either by a high-level language compiler or by an assembly language programmer) and produces an object file; supports NS32332 configuration register and 32-bit addressing; also supports NS32381, NS32382 chips;
nmeld	a linker that resolves references between object files and library routines and assigns relocated addresses to produce Series 32000 executable code;
nar	an archiver used to store frequently referenced objects in a library for convenient retrieval by the linker;
nlorder	finds ordering relation for an object library;
libm.a	a library that includes math routines that can be called from code written in assembly or high level languages. This library includes Bessel functions, exp, log, log10, pow, sqrt, floor, ceil, fmod, fabs, gamma, hypot, sinh, cosh, tanh, sin, cos, tan, asin, acos, atan, and atan2;
idbg16, idbg32	debuggers for use with National's ISE16™ and ISE32™, respectively;
dbg16	debuggers for downloading and debugging code on boards that use the NS32008, NS32016, NS32032, or NS32332 CPU and associated monitors.
mon16, mon32, mon332, mon332B	monitors for use with DB32016, DB32000, DB32332, and DB32332 plus Development Boards. Provided in PROMs and in assembly language source so the user can modify and install the monitor on user-designed Series 32000 hardware.
nburn	a PROM—programming utility that converts a COFF object file into ASCII hex, Intel hex, or Motorola S-record format output file. Suitable for driving a DATA I/O Model 19 PROM-programming.
db library	development board support routines, such as string, scanf, printf, atof, abs, regex, getc, putc, and puts; to be used with the development board monitor;

A library of terminal I/O functions is also provided. These functions can be called by user-developed code to allow a program running on a development board to print data to and accept data from the console terminal. Source to these routines is provided, should the user elect to expand or modify the functionality of these routines. In addition, functions from the C library, "libc.a", that do not rely on the kernel for execution, are included.

cvtasm	utility to assist in converting previous assembler syntaxes to GNX assembler syntax;
nsize	a utility for displaying the size of the text, uninitialized data, and initialized data segments of an object file;
nstrip	a utility to remove symbol table information from an object file;
nnm	a utility to display the symbol table of an object file.

The following two programs are available for configurations designed for operation on a VAX under derivatives of the Berkeley UNIX 4.3 bsd operating system.

ddt	a debugger specifically designed for kernel debugging;
dbmon	a monitor for use with ddt provided on PROM and in assembly language source so the user can modify and install the monitor on user-built Series 32000 hardware.

Optional Components

Optimizing C Compiler

The Optimizing C Compiler is derived from the UNIX C Compiler and supports the C language as defined by Kernighan and Ritchie. Enhancements include passing structures as arguments to functions, long variable names, single-precision floating constants, signed and unsigned bitfields. The compiler generates Series 32000 assembly code which is passed to the GNX assembler.

The optimizer and code generator use state-of-the-art optimization techniques to process C code into assembly statements that approach hand-optimized assembly code in execution speed. Optimization techniques include register allocation by coloring, constant folding, subexpression and assignment elimination, copy propagation, peephole optimizations, and others.

Optimizer processing can be controlled with switches to request optimization for space instead of speed, perform partial optimizations, specify addressing

Optional Components (Continued)

modes and influence allocation of variables to registers.

Code can be compiled with optimization disabled in order to generate debuggable code.

C object modules can be linked with assembly, Pascal and FORTRAN 77 object modules for mixed-language development.

Pascal Compiler

The Pascal compiler is an ISO-standard Pascal compiler derived from the 4.2 bsd "pc" compiler.

The Pascal compiler supports several extensions to the standard Pascal language that are designed to simplify program development, such as separate compilation of individual modules. In addition, I/O of enumerated types, output of octal and hexadecimal numbers, and comparison of strings of unequal length are supported. The Pascal library, "libpc.a", includes several useful procedures and functions, for example, a random number generator, file manipulation procedures, and clock functions.

Pascal object modules can be linked with assembly, C, and FORTRAN 77 object modules for mixed-language development. Pascal programs can call the terminal I/O functions described for the C Compiler.

Optimizing FORTRAN 77 Compiler

The Optimizing FORTRAN 77 Compiler is derived from the UNIX System V Release 2 "f77" Compiler. Enhancements include double-complex data types, recursion, hex constants, one-trip do loop option, short integers and bitwise Boolean operations.

The compiler generates Series 32000 assembly code which is passed to the GNX assembler.

The optimizer and code generator use state-of-the-art optimization techniques to process FORTRAN code into assembly statements that approach hand-optimized assembly code in execution speed. Optimization techniques include register allocation by coloring, constant folding, subexpression and assignment elimination, copy propagation, peephole optimizations and others.

Optimizer processing can be controlled with switches to request optimization for space instead of speed, perform partial optimizations, specify addressing modes and influence allocation of variables to registers.

Code can be compiled with optimization disabled in order to generate debuggable code.

FORTRAN object modules can be linked with assembly, Pascal, and C object modules for mixed-language development.

Source Products

The assembler, associated tools, and the optional C, Pascal, and FORTRAN 77 Compilers are provided in binary form for use on a VAX under the 4.2 bsd operating system. The source to all programs that make up the Series 32000 GNX Language Tools is available for porting to other UNIX operating system environments.

Customer Support

National Semiconductor offers a full 90 day warranty period. Extended warranty provisions can be arranged by calling MCS Logistics at the toll-free numbers listed below.

The MCS Service Technical Support Engineering Center has highly trained technical specialists available to assist customers over the telephone with any product related technical problems.

for more information, please call:

(800) 538-1866,

(800) 672-1811 for California,

(800) 223-3248 for Canada.

Licensing

All binary versions of the Series 32000 GNX Language Tools require the execution of National's Binary User Agreement. Because the language tools include AT&T proprietary code, a System V source license is a prerequisite for obtaining source versions of these language tools.

Part Numbers

Binaries for Cross-Support Mode hosted on VAX under 4.2 bsd:

NSW-ASM-BRVX	The assembler ("nasm"), linker ("nmeld"), math library ("libm.a"), archiver ("nar"), ISE debugger ("idbg16/32") development-board -support library, development board debuggers ("ddt" and "dbg16"), monitors in source ("dbmon" and "mon16/32"), monitors in PROM, the PROM-burning utility ("nburn"), dblibrary, cvtasm, nsize, nstrip, and nnm.
NSW-C-BRVX	Optional C compiler to be used in conjunction with NSW-ASM-BRVX described above.
NSW-F77-BRVX	Optional FORTRAN 77 Compiler to be used in conjunction with NSW-ASM-BRVX described above.
NSW-PAS-BRVX	Optional Pascal Compiler to be used in conjunction with NSW-ASM-BRVX described above.

All binaries for VAX/4.2 bsd are delivered on 9-track reel tape in "tar" format.

Part Numbers (Continued)

Binaries for Cross-Support Mode hosted on VAX under VMS:

NSW-ASM-BRVM	The assembler ("nasm"), linker ("nmeld"), math library ("libm.a"), archiver ("nar"), ISE debugger ("idbg16/32") development-board-support library, development board debugger ("dbg16"), monitor in source ("mon16/32"), monitor in PROM, the PROM-burning utility ("nburn"), dblibrary, cvtasm, nsize, nstrip, and nnm.
NSW-C-BRVM	Optional C Compiler to be used in conjunction with NSW-ASM-BRVM described above.
NSW-F77-BRVM	Optional FORTRAN 77 Compiler to be used in conjunction with NSW-ASM-BRVM described above.
NSW-PAS-BRVM	Optional Pascal Compiler to be used in conjunction with NSW-ASM-BRVM described above.

All binaries for VAX/VMS are delivered on 9-track reel tape in VMS BACKUP format.

Binaries hosted on SYS32/20 under System V:

NSW-C-BLAF	Optional C Compiler to be used in conjunction with NSW-ASM-BLAF described above.
NSW-F77-BLAF	Optional FORTRAN 77 Compiler to be used in conjunction with NSW-ASM-BLAF described above.
NSW-PAS-BLAF	Optional Pascal Compiler to be used in conjunction with NSW-ASM-BLAF described above.

Above binaries for SYS32/20 are delivered on low-density (360 kbyte) 5¼ inch PC-DOS floppy disks in MS-DOS format.

Source

NSW-ASM-SRNN	The source to NSW-ASM-BRVX, as described above.
NSW-C-SRNN	The source to NSW-C-BRVX, as described above.
NSW-PAS-SRNN	The source to NSW-PAS-BRVX, as described above.
NSW-F77-SRNN	The source to NSW-F77-BRVX, as described above.

All source tapes are delivered on 9-track reel tape written in "tar" format.

For future product releases contact your National Semiconductor sales representative or call Series 32000 Software Marketing at (408) 721-5551.

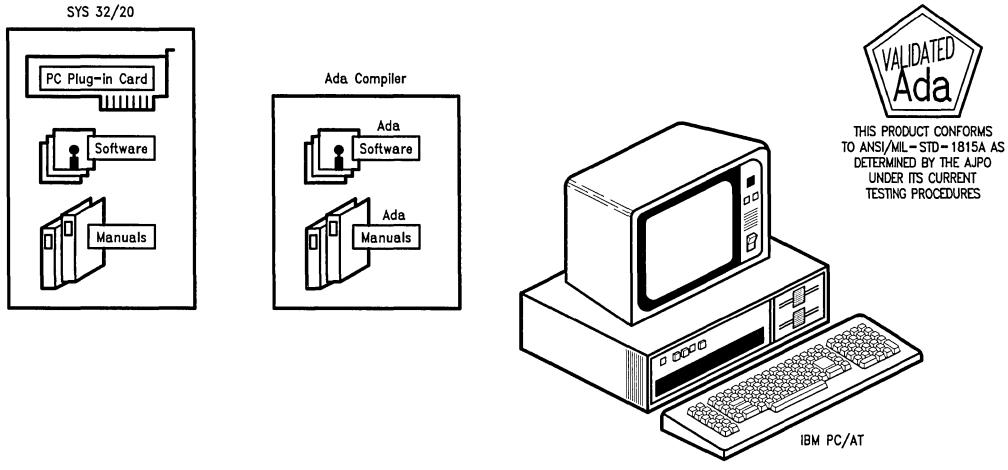
Manuals

Each software package is delivered with one copy of each appropriate manual.

NSP-ASM-M-MS:	Manual Set included with NSW-ASM-BRVM
NSP-ASM-X-MS:	Manual Set included with NSW-ASM-BRVX
NSP-C-M:	Manual included with NSW-C-BRVM and NSW-C-BRVX
NSP-PASCAL-M:	Manual included with NSW-PASCAL-BRVM and NSW-C-BRVX
NSP-F77-M:	Manual included with NSW-F77-BRVM and NSW-F77-BRVX

National Semiconductor

Series 32000®
Ada Cross-Development System for SYS32™/20 Host



TL/GG/9307–2

- **Series 32000 cross-support development environment for SYS32/20**
- **Validated under 1.8 ACVC**
- **Derived from the VERDIX™ Ada Development System (VADS™)**
- **Compiler support for Ada Pragmas and Representation Attributes**
- **Comprehensive Support Services available from National**
- **Generates GNX™ Common Object File Format (COFF)**
- **Debugging Tools**
- **Program Generation Utilities**
- **SPLICE support**
- **Extensive Ada Library Management Utilities**
- **Run-time system to support bare-board environment**
- **Ada VRTX® Interface Package (Optional)**
- **Source to Ada Run-Time System (Optional)**

Product Overview

The Series 32000 Ada cross-compiler supports full Ada language program development on National's SYS32/20 host and is part of National's Validated Ada Development Environment (NVADE). NVADE provides a high performance Ada compiler that supports all required features of the Ada language and is fully compliant with ANSI/MIL-STD-1815A. NVADE also provides a comprehensive set of tools specifically tailored to provide the optimum Ada Programming Support Environment (APSE) for a host of application development.

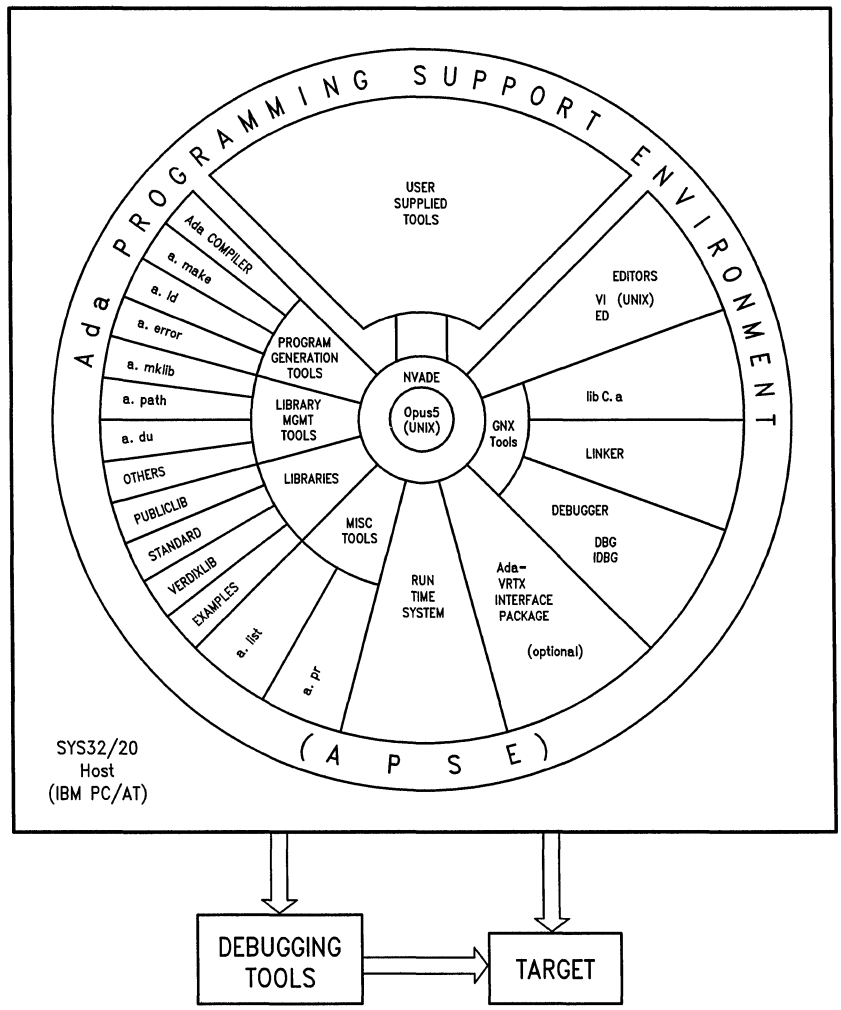
Product Overview (Continued)

The SYS32/20 Development system includes a high-performance add-in card that converts an IBM-PC/AT or compatible system into a Series 32000-based development environment.

Once compiled, the Ada program will execute on either a Series 32000 development board or a customer target board. This "production quality" Ada compiler focuses on high performance, and is intended for large-scale development of real-time, embedded control, or training simulator software applications. The Series 32000 Ada Cross-Development System includes the Ada compiler, program library utilities, program generation utilities, library management and a complete run-time system. This product directly interfaces with GNX language tools provided with the SYS32/20 system, including GNX linker, DBG and IDBG debuggers, library management tools and other utility programs.

The Series 32000 Ada Cross-Development System has been engineered and designed to run under OPUS5, the SYS32/20 Operating System derived from AT&T's UNIX™ System V. Therefore, rather than learning a new operating system, the programmer can immediately concentrate on Ada program development. To aid the user, complete on-line manual entries are provided. These can be configured to use either the UNIX man utility or a separate interactive help command, supplied with the product.

Series 32000 Ada Cross-Development System for SYS32/20 Host



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NVADE Components

Ada Compiler

The Ada Compiler accepts as input Ada source and generates Series 32000 code that can be downloaded to, and executed on, a Series 32000-based target development board.

The Series 32000 Ada Compiler supports the full Ada language. Features include shared or unshared generics, separates, in-lines, bit representation, machine-code insertion, monitor tasks and terminal I/O. The compiler generates GNX COFF (Common Object File Format) object files that can be linked with object files generated by other GNX compilers. The Ada compiler performs several optimizations, including value-tracking global register allocation, register assignment for commons and locals, common sub-expression removal, branch and dead code analysis, some constraint check removal, and local peephole optimizations. The Ada compiler operates as a re-entrant shareable process in the SYS32/20 host system, allowing the compiler to make full use of most operating system facilities.

In addition, the Ada compiler provides features to aid in the development of real-time, embedded control and training simulator software applications. Some of these include Ada Pragmas as specified in Chapter 13 of the Ada Language Reference Manual (LRM), such as: Inline, Interface, Interface_Object, Pack, Page, Priority, Share_Body, and Suppress. Also included is a Machine Code Package which provides an interface for handling machine code insertion and generics (Unchecked_Deallocation and Unchecked_Conversion) for controlling storage and type conversions.

Program Generation Utilities

An Ada make utility, similar in operation to that found in the UNIX operating system, is provided to simplify program compilation by maintaining program unit dependancy information. This utility determines which files must be recompiled to produce a current executable file. This utility can also be used to ensure that the named unit is up-to-date, recompiling dependencies as necessary. Also provided is a source code formatter, easily configurable for individual Ada coding standards.

Program Library Utilities

The Ada language imposes stringent requirements on an Ada Program Library. While the language provides for separate compilation of program units, each unit is compiled in the "context" of previously compiled units. The compiler must have access to this context, and the context must be carefully organized in the form of a Program Library. This library has been designed to enhance the compiler performance. A set of utilities is provided to manage, manipulate, and display Program Library information.

In addition, the Series 32000 Ada Cross-Development System permits Ada Program Libraries to be hierarchically organized, so that units not local to one library can be found in other libraries. Thus, programmers can work without interference on local versions of individual program units, while retrieving the remainder of the program from higher-level libraries.

NVADE also uses DIANA (Descriptive Intermediate Attributed Notation for Ada), which generates an intermediated representation for each unit. DIANA provides a tree-structured representation of an Ada program encoding the complete syntactic and semantic information of each individual Ada unit. The presence of DIANA as an integrated mechanism makes possible powerful editing, debugging and program query facilities, thus providing the means for simple and efficient incremental compilation.

Debuggers

The standard GNX debugger, DBG32, is used with the Series 32000 Ada Cross-Development System. DBG32 can be used to debug code on the SYS32/20 host and/or to download and remotely debug or execute code on a Series 32000 development board. DBG32 supports the use of National's SPLICE software debugging tool. Machine-level debug support is provided by the debugger.

Linker

Ada object files are linked by the standard GNX linker, which is called by the Ada compiler pre-linker. The GNX linker resolves references between object files and library routines and assigns relocated addresses to produce Series 32000 executable code.

Ada Run-Time System

The Series 32000 Ada Run-time System provides comprehensive support for tasking, debugging, exception handling and input/output.

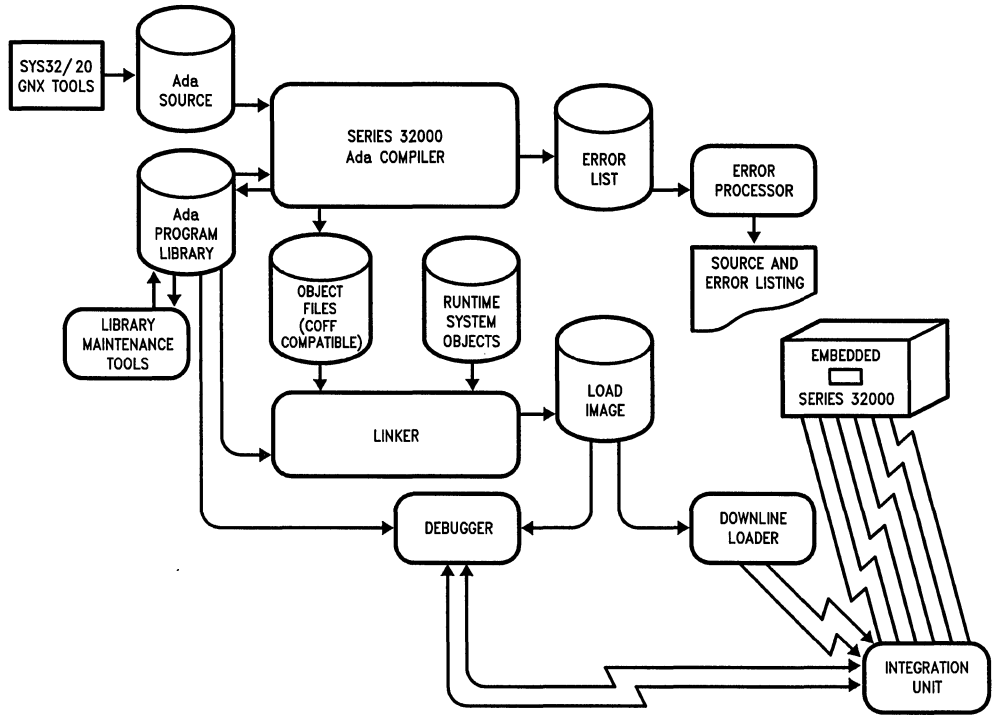
The Run-time System is linked with the user's generated Ada program. To facilitate resource utilization efficiency, major portions of the Run-time System have been optimized. Run-time source for customization is also available.

Ada-VRTX Interface Package (Optional)

The Ada Run-time System includes a large, rich, and elegant tasking system. VRTX (the Versatile Real-Time Executive) provides a small, simple, compact and fast tasking system and may be a preferred alternative to using the Ada Run-time System, particularly for embedded microprocessor applications where space and timing are critical. The Ada-VRTX interface package (AVIP) offers Ada language users a convenient means of interfacing with VRTX. AVIP allows Ada programmers the ability to call any VRTX service from their Ada program. (The exceptions are

Program Library Utilities (Continued)

Series 32000 Ada Cross-Development System for SYS32/20 Host
NVADE Modules and Run-Time Environment



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calls provided for the user-defined interrupt handlers and partition create and extend.) The actual operations performed by VRTX are identical in both assembly language and Ada. Thus, this package gives users both the elegant features of the Ada language and VRTX's unique tasking system.

Pre-Requisites

— SYS32/20 KIT (KIT 2 is recommended) installed on an IBM PC/AT
— DB32000, DB332-PLUS target development system board with power supply
— 60 mbyte hard disk capacity (minimum)
— IBM PC/AT with 1.2 mbyte floppy drive or IBM PC/AT with Tape Cartridge Unit
— A minimum of one available serial port

Supported Hardware/Software

— SYS32/20 HOST
— SYS32/20 Operating System (OPUS5)
— DB32000, DB332-PLUS target development system board with power supply
— In-System Emulator
— SPLICE II

Shipping Package

— Series 32000 Installation Instructions and Release Letter
— SYS32/20 Cartridge tape or high density floppy diskettes
— Ada Language Reference Manual (ANSI/MIL-STD 1815A)
— Ada Compiler and support tools documentation

Ordering Information

— NSW-Ada-BHAF Ada Cross-Development System, binary high density diskettes, SYS32/20
— NSW-Ada-BCAF Ada Cross-Development System, binary cartridge tape, SYS32/20
— NSW-ARTS-SHAF Ada Run-time System, source, high density diskettes, SYS32/20
— NSW-ARTS-SCAF Ada Run-time System, source, cartridge, SYS32/20
— NSW-AVIP-BHAF Ada-VRTX-Interface Package, Binary high density diskettes, SYS32/20
— NSW-AVIP-BCAF Ada-VRTX-Interface Package, Binary Cartridge tape, SYS32/20
— NSP-Ada-MS Manual set for the Ada Development System

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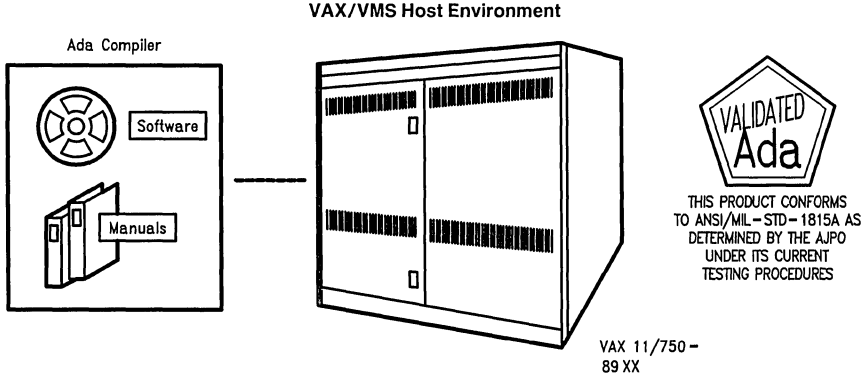
Series 32000®
Ada Cross-Development System for VAX™/VMS™ Host



TL/GG/9364-1

- **Series 32000 cross-support development environment for VAX/VMS host**
- **Validated under 1.8 ACVC**
- **Runs under VAX/VMS 4.4 Operating Systems and future revisions of VMS**
- **Derived from the VERDIX™ Ada Development System (VADS™)**
- **Compiler Support for Ada Pragmas and Representation Attributes**
- **Comprehensive Support Services available from National**
- **Generates GNX™ Common Object File Format (COFF)**
- **Program Generation Utilities**
- **SPLICE support**
- **Extensive Ada Library Management Utilities**
- **Run-time system to support bare-board environment**
- **Debugging Tools**
- **Ada VRTX® Interface Package (Optional)**
- **Source to Ada Run-Time System (Optional)**

Product Overview

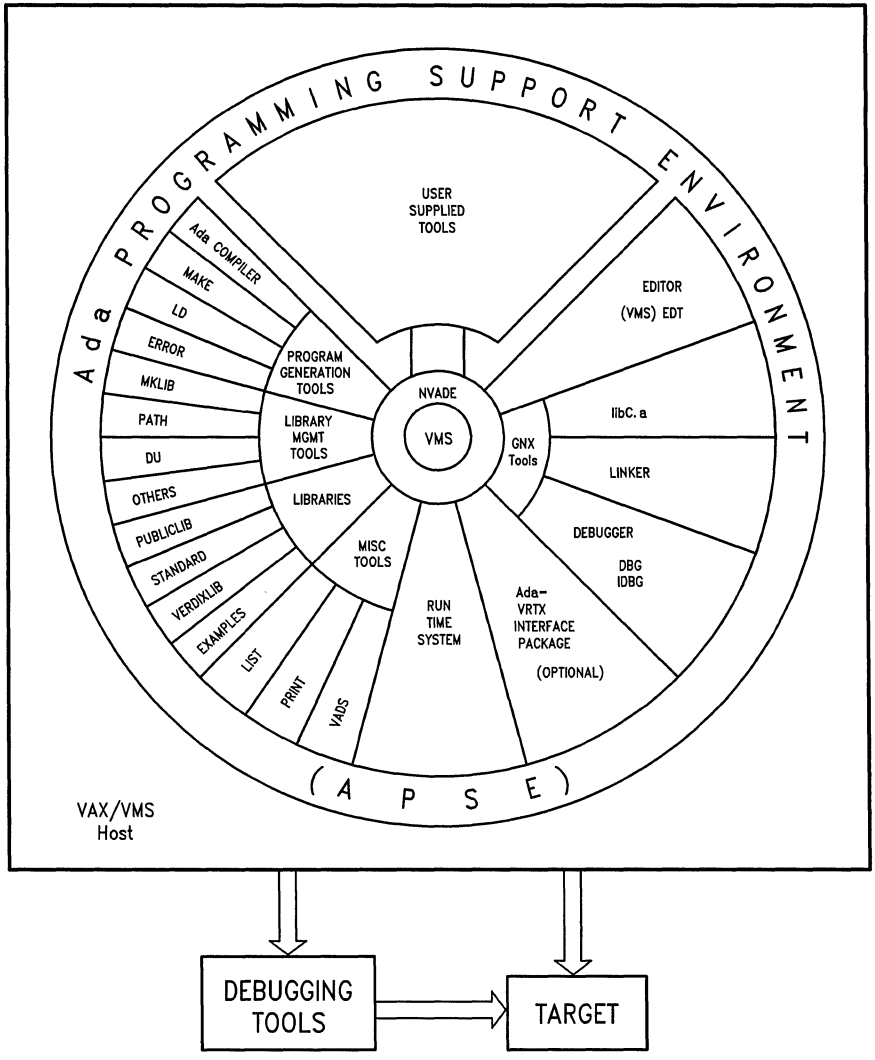
The Series 32000 Ada cross-compiler supports full Ada language program development on Digital Equipment Corporation's VAX/VMS hosts and is part of National's Validated Ada Development Environment (NVADE). NVADE provides a high performance Ada compiler that supports all required features of the Ada language and is fully compliant with ANSI/MIL-STD-1815A. NVADE also provides a comprehensive set of tools specifically tailored to provide the optimum Ada Programming Support Environment (APSE) for host application development.

Product Overview (Continued)

Once compiled, the Ada program will execute on either a Series 32000 development board or a customer target board. This "production quality" Ada compiler focuses on high performance, and is intended for large-scale development of Series 32000 real-time, embedded control, or training simulator software applications. The VAX/VMS Ada Cross-Development System includes the Ada compiler, program library utilities, program generation utilities, library management utilities and a complete run-time system. This product directly interfaces with VAX/VMS GNX language tools provided, including GNX linker, DBG and IDBG debuggers, library management tools and other utility programs.

The VAX/VMS Ada Cross-Development System has been engineered and designed to run under VAX/VMS 4.4 or later Operating Systems. Therefore, rather than learning a new operating system, the programmer can immediately concentrate on Ada program development.

Series 32000 Ada Cross-Development System for VAX/VMS Host



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NVADE Components

Ada Compiler

The Ada Compiler accepts as input Ada source and generates Series 32000 code that can be downloaded to, and executed on, a Series 32000-based target development board.

The Series 32000 Ada Compiler supports the full Ada language. Features include shared or unshared generics, separates, in-lines, bit representation, machine-code insertion, interrupt tasks, monitor tasks and terminal I/O. The compiler generates GNX COFF (Common Object File Format) object files that can be linked with object files generated by other GNX compilers. The Ada compiler performs several optimizations, including value-tracking global register allocation, register assignment for commons and locals, common sub-expression removal, branch and dead code analysis, some constraint check removal, and local peephole optimizations. The Ada compiler operates as a re-entrant shareable process in the VAX/VMS host system, allowing the compiler to make full use of most operating system facilities.

In addition, the Ada compiler provides features to aid in the development of real-time, embedded control, and training simulator software applications. Some of these include Ada Pragmas as specified in Chapter 13 of the Ada Language Reference Manual (LRM), such as: Inline, Interface, Interface_Object, Pack, Page, Priority, Share_Body and Suppress. Also included is a Machine Code Package which provides an interface for handling machine code insertion and generics (Unchecked_Deallocation and Unchecked_Conversion) for controlling storage and type conversions.

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An Ada make utility, similar in operation to that found in the UNIX® operating system, is provided to simplify program compilation by maintaining program unit dependency information. This utility determines which files must be recompiled to produce a current executable file. This utility can also be used to ensure that the named unit is up-to-date, recompiling dependencies as necessary. Also provided is a source code formatter, easily configurable for individual Ada coding standards.

Program Library Utilities

The Ada Language imposes stringent requirements on an Ada Program Library. While the language provides for separate compilation of program units, each unit is compiled in the "context" of previously compiled units. The compiler must have access to this context, and the context must be carefully organized in the form of a Program Library. This library has been designed to enhance the compiler performance. A set of utilities is provided to manage, manipulate, and display Program Library information.

In addition, the Series 32000 Ada Cross-Development System permits Ada Program Libraries to be hierarchically organized, so that units not local to one library can be found in other libraries. Thus, programmers can work without interference on local versions of individual program units, while retrieving the remainder of the program from higher-level libraries.

NVADE also uses DIANA (Descriptive Intermediate Attributed Notation for Ada), which generates an intermediated representation for each unit. DIANA provides a tree-structured representation of an Ada program encoding the complete syntactic and semantic information of each individual Ada unit. The presence of DIANA as an integrated mechanism makes possible powerful editing, debugging and program query facilities, thus providing the means for simple and efficient incremental compilation.

Debuggers

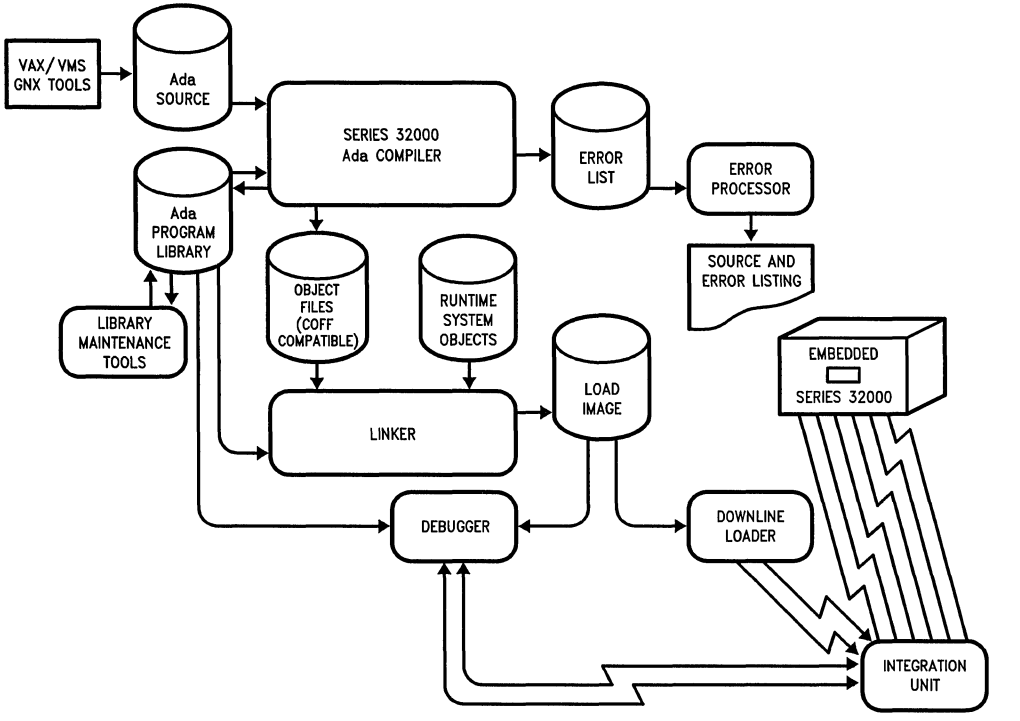
The standard GNX debugger, DBG32, is used with the Series 32000 Ada Cross-Development System. DBG32 can be used to debug code on the VAX host and/or to download and remotely debug or execute code on Series 32000 development board. DBG32 supports the use of National's SPLICE software debugging tool. Full machine-level debug support is provided by the debugger.

Linker

Ada object files are linked with the standard GNX linker, which is called by the Ada compiler pre-linker. The GNX linker resolves references between object files and library routines and assigns relocated addresses to produce Series 32000 executable code.

NVADE Components (Continued)

Series 32000 Ada Cross-Development System for VAX/VMS Host
NVADE Modules and Run-Time Environment



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Ada Run-Time System

The Series 32000 Ada Run-Time System provides comprehensive support for tasking, debugging, exception handling and input/output.

The Run-Time System is linked with the user's generated Ada program. To facilitate resource utilization efficiency, major portions of the Run-Time System have been optimized. Run-Time source code for customization is also available.

Ada-VRTX Interface Package (Optional)

The Ada Run-Time System consists of a large, rich and elegant tasking system. VRTX (the Versatile Real-Time Executive) provides a small, simple, compact and fast tasking system and may be a preferred alternative to using the Ada Run-Time System, particulary for embedded microprocessor applications where space and timing are critical. This Ada-VRTX interface package (AVIP) offers Ada language users a convenient means of interface with VRTX. AVIP allows Ada programmers the ability to call any VRTX service from their Ada program. (The only exceptions are the calls provided for user-defined interrupt handlers and for partition create and extend.) The actual operations performed by VRTX are identical in both assembly language and Ada. Thus, this package gives users both the elegant features of the Ada language and VRTX's unique tasking system.

PRE-REQUISITES

— VAX/VMS Host Computer 750-89XX
— VMS Operating System
— VAX/VMS GNX Assembler Package

Supported Hardware/Software

— All VAX/VMS computers
— DB32000, DB332-PLUS, VME532 target development system board with power supply

NVADE Components (Continued)

Shipping Package

— Series 32000 Installation Instructions and Applications Notes

— 1600 bpi magnetic tape (9-track VMS copy format)

— Ada Language Reference Manual (ANSI/MIL-STD 1815A)

— Ada Compiler and support tools documentation

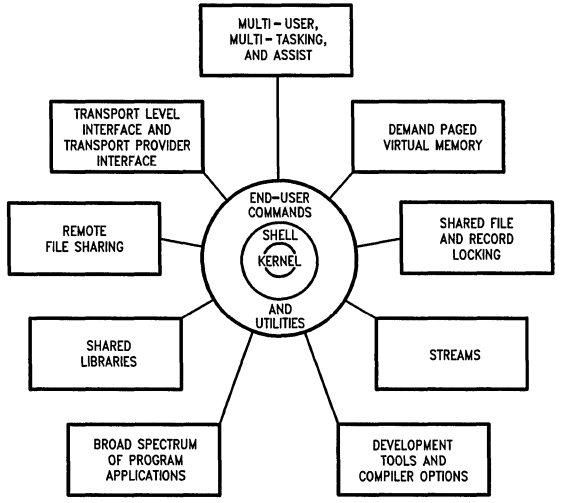
Ordering Information

Part Number

NSW-Ada-BRVM-1	Binary Ada Cross Dev. System Tape, Vax-11/750, 11/780, 82XX
NSW-Ada-BRVM-2	Binary Ada Cross Dev. System Tape, Vax-11/785, 83XX
NSW-Ada-BRVM-3	Binary Ada Cross Dev. System Tape, Vax-8500, 8530, 8600
NSW-Ada-BRVM-4	Binary Ada Cross Dev. System Tape, Vax-8550, 8650, 8700
NSW-Ada-BRVM-5	Binary Ada Cross Dev. System Tape, Vax-88XX, 89XX
NSW-AVIP-BRVM-1	Binary Ada VRTX Int. Pckg. Tape, Vax-11/750, 11/780, 82XX
NSW-AVIP-BRVM-2	Binary Ada VRTX Int. Pckg. Tape, Vax-11/785, 83XX
NSW-AVIP-BRVM-3	Binary Ada VRTX Int. Pckg. Tape, Vax-8500, 8530, 8600
NSW-AVIP-BRVM-4	Binary Ada VRTX Int. Pckg. Tape, Vax-8550, 8650, 8700
NSW-AVIP-BRVM-5	Binary Ada VRTX Int. Pckg. Tape, Vax-88XX, 89XX
NSW-ARTS-SRVM-1	Source Ada RUNTIME SYSTEM Tape, Vax-11/750, 11/780, 82XX
NSW-ARTS-SRVM-2	Source Ada RUNTIME SYSTEM Tape, Vax-11/785, 83XX
NSW-ARTS-SRVM-3	Source Ada RUNTIME SYSTEM Tape, Vax-8500, 8530, 8600
NSW-ARTS-SRVM-4	Source Ada RUNTIME SYSTEM Tape, Vax-8550, 8650, 8700
NSW-ARTS-SRVM-5	Source Ada RUNTIME SYSTEM Tape, Vax-88XX, 89XX
NSP-Ada-VMS	Additional Manual Sets for VAX/VMS Ada Development System

National Semiconductor

GENIX™/V.3 Operating System



TL/R/9263-1

- **Derived from AT&T's System V, Release 3.0, UNIX® Operating System**
- **Demand-paged Virtual Memory**
- **Mandatory and Advisory File and Record Locking**
- **Streams**
- **Transport Level Interface and Transport Provider Interface**
- **Remote File Sharing**
- **Shared Libraries**
- **Assist**
- **C Compiler and Associated Language Tools**

General Description

GENIX/V.3 is a port of AT&T's System V, Release 3.0, UNIX operating system for the Series 32000® microprocessor family. GENIX/V.3 is available in source form and can be adapted to serve as the operating system on customer-designed Series 32000-based systems.

GENIX/V.3 is a multitasking, multiuser operating system that provides an abundance of programs and utilities for text processing, program development, and system administration. GENIX/V.3 supports a wide variety of applications ranging from databases to graphics packages available from independent software vendors.

GENIX/V.3 carries forward all of the enhancements from Systems V/Series 32000, such as demand-paged virtual memory and file and record locking, while introducing significant new features that support local area networking.

GENIX/V.3 Features

Streams

Streams is a general, flexible facility for the development of communications services within the UNIX operating system. Streams provides a consistent framework for the operation of network services (ranging from local area networks to individual device drivers) under the UNIX kernel.

Streams defines a standard interface for character input and output within the kernel and between the kernel and user programs. This standard interface enables modular, portable program development and clean integration of network services.

As a result of Streams, network architectures and high-level protocols are independent of underlying low-level protocols, device drivers, and media.

Transport Level Interface (TLI) and Transport Provider Interface (TPI)

GENIX/V.3 includes two significant libraries that help the protocol-developer produce protocols that conform to industry standards. The TLI library is composed of user-level functions that provide access to standard protocol services as defined by the ISO Transport Service Interface. The TPI library specifies capabilities that must be supplied by a transport provider and the required interface to those capabilities to maintain consistency with the TLI library.

Together, the TLI and the TPI libraries create the means by which network-independent applications can be written. An application written using the TLI library will work without modification over any network implemented according to the TPI specification. GENIX/V.3 includes a new version of 'uucp' (based on the Honey-Danber 'uucp') that is implemented using the TLI library. Remote File Sharing, described below, is also implemented using the TLI library.

Remote File Sharing (RFS)

RFS is an example of the kind of network services that can be developed using Streams. RFS allows a group of computers to be linked together over a network so that resources belonging to one system (e.g., disk files, printers, and tape drives), can be made available to users on other systems. This availability is transparent to the user; the user does not have to know or issue any special commands to access a remote resource.

RFS has built in security features as well. The local machine administrator decides which file systems will be available to the network and which remote resources the local users can access.

Demand-Paged Virtual Memory

The GENIX/V.3 operating system supports programs that access up to 15 Mbytes (if using the NS32082 MMU) or ½ gigabyte (if using the NS32382 MMU) of virtual address space. In addition, the GENIX/V.3 operating system takes advantage of the memory protection scheme afforded by the MMU's separate user and supervisor address space.

C Compiler

The GENIX/V.3 operating system includes a C compiler based on the Berkeley 4.2 bsd 'pcc' (portable C compiler). The C compiler and associated language tools (assembler and linker) produce executable code whose addresses are resolved by relocation during the linkage process. The GENIX/V.3 language tools conform to a superset of AT&T's Common Object File Format (COFF).

Shared Libraries

A shared library is a library of subroutines that is accessed at run-time rather than being included in the program when the program is linked. As a result, programs that use shared libraries occupy less space on disk and in memory. In addition, when a library is modified, programs that use that library do not have to be recompiled to benefit from changes to that library.

GENIX/V.3 binary is provided with a shared version of a subset of 'libc.a' and the Networking Services Library. Tools are provided for the user to generate additional shared libraries.

Assist

'Assist' is a set of programs that provide on-line assistance to users of the GENIX/V.3 operating system. 'Assist' should not be confused with on-line manual pages; rather, 'Assist' is a menu-driven program that helps the user form correct command line syntax on a step-by-step basis. 'Assist' includes tools for building custom menus in addition to the menus provided as a part of the GENIX/V.3 operating system.

File System Switch (FSS)

FSS allows the operating system to support several different types of file systems simultaneously. For example a file system type could be implemented to permit users to access data stored on floppy diskettes created by other operating systems.

Mandatory File and Record Locking

Previous versions of the System V UNIX operating system supported voluntary file and record locking. Under voluntary file and record locking, a group of programs must voluntarily agree to honor locks that may have been placed on a file or a record. It was possible for a programmer to write a 'maverick' program that refused to honor voluntary locks.

With mandatory file and record locking, a database designer is guaranteed that any locks the program places on a file or record will be honored by every program in the system. Mandatory locks guarantee the security of database applications.

Optional Software

Korn Shell

The Korn shell is an optional command interpreter compatible with the Bourne shell and offers many features found in the C shell, such as 'aliases'. The Korn shell introduces new features such as 'vi editing mode', which allows the user to modify and enter previously entered commands with fewer keystrokes.

Tools for Documenters

Tools for Documenters, derived from AT&T's Documenters Workbench 2.0, is an optional set of software that contains programs that help users prepare documentation. The programs include text processors ('nroff', 'troff', and 'ditroff'), macro packages ('mm' and 'man'), preprocessors that prepare special kinds of text ('tbl' and 'eqn'), and postprocessors that prepare documents for handling by a particular output device, such as a printer or phototypesetter.

Machine Readable Documentation

The optional Machine Readable Documentation includes source to all GENIX/V.3 manuals for those OEM's who plan to modify and print their own manual sets.

Benefits

AVAILABLE IN SOURCE FORM TO QUALIFIED CONTRACTORS OF NSC

All source files required to produce a binary version of the GENIX/V.3 operating system are provided. These files include source code to the kernel (including demand-paged virtual memory code), all utilities, device drivers, libraries, the C compiler, assembler and linker.

Kernel source code is adaptable to the NS32016, NS32032, and NS32332 CPU and the NS32082 and the NS32382 MMU by compilation switches. The GENIX/V.3 operating system is designed to run on hardware configurations that include the NS32201 Timing Control Unit, the NS32081 Floating Point Unit, and the NS32202 Interrupt Control Unit, a minimum of one RS232 serial port, 2 Mbytes of RAM, and a minimum 40 Mbytes of disk storage for the binary operating system.

In addition, the GENIX/V.3 operating system source product includes a binary image of the root and /usr file systems which was generated from the provided source files.

Customer Support

The GENIX/V.3 operating system, whether provided in binary or source form, includes a 90-day warranty. During the warranty period, customers are entitled to toll-free telephone access to National's MCS Technical Support Engineering Center to receive assistance, report bugs and obtain workarounds. In addition, the customer will receive any update releases that become available from National Semiconductor at no additional charge.

After the 90-day warranty has expired, extended support can be contracted by calling MCS Logistics at the toll-free numbers below:

(800) 538-1866 in the USA, except California

(800) 672-1811 in California

(800) 223-3248 in Canada

Outside the USA and Canada:

(408) 749-7306

Licensing

The GENIX/V.3 operating system is provided under license from National Semiconductor Corporation. The Source License under Contractor Provisions provides non-exclusive rights to use the GENIX/V.3 operating system source for internal purposes. A separate Binary Distribution License provides right to distribute binary copies and includes per copy royalty rates. To obtain licensing information, contact your National Semiconductor sales engineer.

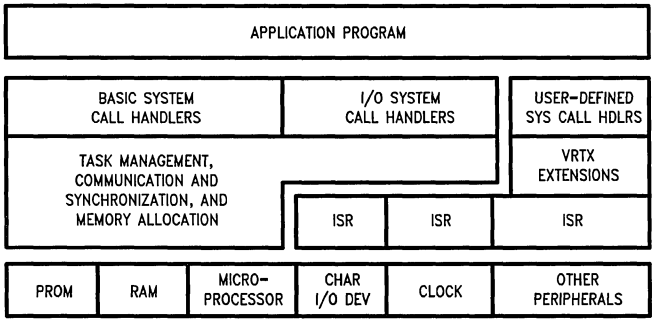
Ordering Information

NSW-GV3-SRNX	GENIX/V.3 source on reel-to-reel 9-track tape
NSW-GV3-SCNX	GENIX/V.3 source on 9-track cartridge tape

National Semiconductor

Series 32000® Real-Time Software Components VRTX, IOX, FMX and TRACER

VRTX/Series 32000 R&D Package



TL/GG/8781-1

- **Real-time executive for Series 32000 embedded systems**
- **Can be installed in any Series 32000 hardware environment**
- **Manages multitasking with priority-based scheduler**
- **Manages memory pool, mailboxes, timing and terminal I/O**
- **Can reside in PROM and be located anywhere in memory**
- **No requirements for particular timers, interrupts or busses**
- **Has hooks at key processing points for easy customization**
- **Comprehensive manuals with many examples**
- **Hot-line technical support**
- **Integrated with interactive multitasking debugger (optional)**
- **Integrated with PC-DOS compatible file system (optional)**

The VRTX®/Series 32000 executive is the central member of a set of silicon software building blocks used in Series 32000-based real-time embedded systems. The executive manages the multitasking environment and responds to operating system service requests from application tasks.

The executive can be used alone or in combination with the other silicon software components to build a more complete operating system. The IOX®/Series 32000 and FMX®/Series 32000 components support a file system that is media-compatible with PC-DOS. The TRACER™/Series 32000 is an interactive multitasking debugger that can be used in VRTX-based systems for debug, download and test.

All the components can reside in PROM's installed in the target system. They can be placed anywhere in the address space and make minimal assumptions about the hardware environment. Small user-written routines supply information about the local implementation of interrupts, timers, I/O devices, etc. Application tasks interface to the components with Series 32000 SVC (Supervisor Call) interrupts, thus code for the components does not require linking with user-written code.

7

VRTX Features

Task Management

The basic logical unit controlled by VRTX is the task. The task is a logically complete path through user code that requires system resources. Each task has a priority level used by VRTX to determine how access to the CPU is allocated. Up to 256 priority levels are available. VRTX allocates the CPU sequentially to the highest priority task that is ready to execute. Tasks can create, delete, suspend, and modify the priority of themselves and other tasks. Task delays and time-slicing are also available.

Intertask Communication and Synchronization

Tasks can communicate and synchronize with other tasks via exchange of pointer-length messages through mailboxes. These permit mutual exclusion and resource-locking. VRTX also has directives for dynamically building and managing message queues.

Interrupt Services

VRTX has directives for user-written interrupt handlers that provide the interface between tasks and devices. They permit the interrupt handler to influence the scheduling of critically important tasks. Additionally, almost all of the VRTX facilities are available to interrupt routines, so system services can be performed immediately upon receipt of an interrupt.

Memory Management

VRTX provides directives for managing the free memory pool. To minimize fragmentation and overhead, storage is allocated and released as fixed size blocks from within memory partitions. Partitions can be built dynamically. There are no constraints on block size.

Special Device Support

Since many applications require a real-time clock and a character I/O device, support for them is integrated into VRTX. Designers need only supply a small hardware-dependent interrupt service routine for each. VRTX will then manage all the logical operations to supply the clock management and character I/O services to application tasks and interrupt handlers.

Extensions

VRTX accommodates applications with special requirements by supplying three hooks at key points in its execution. They permit the designer to modify VRTX processing without having to modify VRTX itself. Whenever VRTX reaches a hook it checks for the presence of an application routine. VRTX hooks are called at task create, delete, and context switch. There are no constraints on hook use.They can be used for saving/restoring the floating-point environment or for maintaining a counter in the task control block to monitor task execution.

The VRTX/Series 32000 R&D Package contains the product, manuals and other documentation required to develop a real-time application using only the VRTX kernel. You can also purchase TRACER/Series 32000, IOX/Series 32000 and FMX/Series 32000 as separate R&D Packages or as bundled combinations.

When the development phase is complete, contact the National Semiconductor Series 32000 Software Products Marketing Group to purchase a license to incorporate VRTX into products in production volumes.

National also offers Host-Based Special Volume Agreements which include R&D Packages and the rights to make unlimited copies of VRTX on a designated workstation or CPU. Contact the Series 32000 Product Marketing Group for details.

Package Contents

The VRTX/Series 32000 R&D Package contains:

One master copy of VRTX in two 2732 PROM's

A boxtop license to make five copies of VRTX (USA only)

Five sets of Hunter & Ready Silicon Software copyright labels

Five VRTX/Series 32000 User's Guides

A binder containing R&D documentation:

- Getting Started with Silicon Software Components
- How to Write a Board Support Package for VRTX
- Interfacing a Language to Silicon Software Components
- Application Notes

Customer Support information

VRTX Release Notes

VRTX Timing Summary

System Call	32332 Time (Cycles)	System Call	32332 Time (Cycles)
SC_ACCEPT	438	SC_QCREATE	614
SC_GBLOCK	611	SC_QINQUIRY	470
SC_GETC	508	SC_QPEND	551
SC_GTIME	417	SC_QPOST	622
SC_LOCK	431	SC_RBLOCK	702
SC_PCREATE	951	SC_STIME	415
SC_PEND	446	SC_TCREATE	984
SC_PEXTEND	955	SC_TDELAY	1257
SC_POST	616	SC_TDELETE	917
SC_PUTC	506	SC_TINQUIRY	593
SC_QACCEPT	472	Rechedule	671

VRTX System Calls		
Type	**Call**	**Description**
Initialization	VRTX_INIT	Initialize VRTX
	VRTX_GO	Start multitasking
Task Management	SC_TCREATE	Create a task
	SC_TDELETE	Delete a task
	SC_TSUSPEND	Suspend a task
	SC_TRESUME	Resume execution of suspended task
	SC_TPRIORITY	Change task priority
	SC_TINQUIRY	Get task status
	SC_LOCK	Disable task rescheduling
	SC_UNLOCK	Enable task rescheduling
Communications Services	SC_POST	Post message to mailbox
	SC_PEND	Pend for message at mailbox
	SC_ACCEPT	Accept message at mailbox
	SC_QCREATE	Create message queue
	SC_QPOST	Post message to queue
	SC_QPEND	Pend for message from queue
	SC_QACCEPT	Accept message from queue
	SC_QINQUIRY	Get queue status
Memory Management	SC_GBLOCK	Get memory block
	SC_RBLOCK	Release memory block
	SC_PCREATE	Create memory partition
	SC_PEXTEND	Extend memory partition
Timer Services	SC_GTIME	Get system time
	SC_STIME	Set system time
	SC_TDELAY	Suspend task temporarily
	SC_TSLICE	Enable round-robin scheduling
	UI_TIMER	Post time increment from interrupt
Character I/O	SC_GETC	Get a character
	SC_PUTC	Put a character
	UI_RXCHR	Post received character from interrupt
	UI_TXRDY	Post transmit ready from interrupt
	SC_WAITC	Wait for special character
Interrupt Services	UI_ENTER	Enter interrupt handler
	UI_EXIT	Exit from interrupt handler

Customer Support

National Semiconductor offers a one year complete technical support period. Extended support provisions can be arranged by calling MCS Logistics at the toll-free numbers which follow.

The MCS Service Technical Support Engineering Center has highly trained technical specialists to assist customers over the telephone with product related technical problems.

For more information, please call:

(800) 538-1866 in the USA except for California
(800) 672-1811 within California
(800) 223-3248 in Canada
(408) 749-7306 for rest of world

Licensing

All R&D packages are licensed through a National Semiconductor Binary Software Licensing Agreement. In the United States, breaking the seal on the product package indicates acceptance of the terms of the license; no signature is required. For international sales a signed Binary Software License Agreement is required. If changes are required to the license agreement, contact the National Semiconductor Series 32000 Software Marketing Group before breaking the seal on the package.

Ordering Information

NSW-VRTX-BRVM VRTX/Series 32000 in two 2732 EPROMs, and as files of S-records and define-byte records on a 1600 bpi 9-track VAX/VMS BACK-UP tape, manuals and R&D documentation.

NSW-VRTX-BRVX VRTX/Series 32000 in two 2732 EPROMs, and as files of S-records and define-byte records on a 1600 bpi 9-track VAX/4.2 bsd "tar" tape, manuals and R&D documentation.

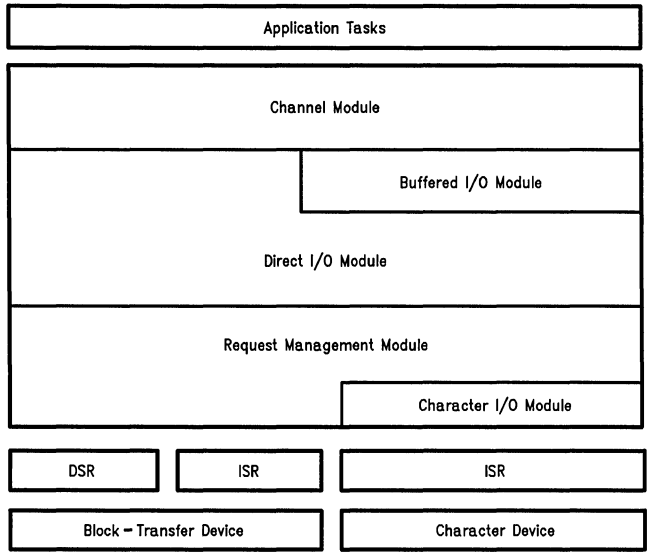
NSW-VRTX-BLAF VRTX/Series 32000 in two 2732 EPROMs, and as files of S-records and define-byte records stored in MS-DOS format on a 5¼ inch PC-DOS floppy diskette, manuals and R&D documentation.

NSW-VRTX-SPNN VRTX/Series 32000 source code listing.

Documentation

NSP-VRTX-M VRTX/Series 32000 User's Guide

IOX/Series 32000 R & D Package



TL/GG/8781–3

- **Input/Output Executive**
- **Provides device-level input/output facilities for VRTX-based software system**
- **Handles the translation of read and write commands from tasks into specific operations on particular devices**
- **Handles the allocation of devices to tasks**
- **Handles the conversion of data from device-specific formats into user-defined formats**
- **Can work with most types of I/O devices**
- **Has hooks and extension services for easy customization**
- **Comprehensive manuals with many examples**
- **Hot-line technical support**

IOX/Series 32000 is the Input/Output Executive, a companion software component for VRTX/Series 32000. IOX provides embedded microprocessor applications with a powerful set of input/output (I/O) facilities for use in a multitasking, real-time environment. Like VRTX, IOX is a silicon software component; it makes no assumptions about its target environment, and can thus be used unchanged in many different custom applications. IOX manages any number and kind of I/O devices in a real-time, multitasking application. IOX services allow several tasks to share a single device, with requests on that device processed according to an application-specified priority. Tasks can transfer data to or from devices in buffered or direct mode, using either sequential or random access. In buffered mode, IOX maintains one or more intermediate buffers for a task using a device, minimizing the time of task suspension by overlapping physical I/O with task processing. Buffering isolates application tasks from the physical characteristics of devices, so that serial devices such as terminals can coexist with random access devices such as disks, both accessed by the same buffered IOX calls.

IOX not only controls device resources, it integrates those devices into a unified framework, providing a consistent I/O interface with a large degree of device independence. Application code written using IOX's buffered I/O services can be transported with only minor modifications to other systems, even if those systems utilize completely different I/O devices. In fact, code written in a high-level language may require no change at all.

For applications that require close control over device operations, IOX's direct mode provides a set of services that can transfer data or perform device-specific control operations and synchronization, yet still free the application programmer from some hardware-dependent considerations such as device addresses, command codes and interrupt handling.

IOX Features

Buffered I/O

IOX's buffering services improve performance and free the application from device-specific data block sizes and formats by transferring data between the application and IOX-maintained buffers, overlapping physical I/O with application processing whenever possible. IOX manages the intermediate buffers to serve several purposes:

Device Independence

Application tasks can ignore the idiosyncrasies of device operation or block sizes and formats, and can transfer fixed or variable length records according to application needs, rather than device requirements.

Overlapping I/O

Buffered I/O overlaps application processing with file I/O operations, freeing the application from synchronizing such operations.

Caching

For random-access devices such as disks, IOX's buffering services improve performance by checking IOX buffers for the sector requested by the application, accessing the device only if the target sector is not buffer-resident.

Variable record length support

With IOX's buffering services, record size can be determined by the presence of a delimiter character in the input or output stream, rather than being tied to a fixed block size.

Direct I/O

Direct I/O allows the programmer to bypass IOX's buffering services whenever an application requires deterministic control over when and how an I/O operation occurs.

Synchronous I/O

The calling task is suspended until the requested operation is completed and either data or status or both have been returned. In this way a lock-step synchronization is enforced on an I/O operation.

Asynchronous I/O

An application using direct I/O can initiate one or more I/O operations and then continue with other processing, retrieving the results of the I/O later via a VRTX mailbox or message queue. This allows I/O to be overlapped with continued operation of the calling task.

Device Support

IOX supports three device types—block, disk and character devices. For each device type IOX provides a number of salient features:

Device sharing

IOX supports shared devices through constructs called channels. A channel is a data structure that represents a logical conduit, or path to a device. IOX provides separate position and error indicators for each channel open to a device, thus facilitating device sharing, critical in a multitasking environment.

Disk position support

IOX maintains position indicators for disks (or any random access devices), thus relieving the application from the responsibility for calculating or maintaining position.

Terminal support

IOX's terminal handling calls support echoing, type ahead and holding or disabling terminal output.

Extensibility

While IOX never has to be modified, it can nonetheless be extended to meet unique needs.

A user-written I/O handler that directly manipulates hardware can be placed into the IOX higher-level functions. This facility can not only service unusual devices, but also emulate a physical device, such as a UNIX like "pipe" between separate processes.

For less fundamental extensions IOX includes four software "hooks" that give the system programmer the capability to fine-tune IOX functionality so that it matches it's computer environment.

IOX can also be extended by adding auxiliary file management software components (FMX).

The IOX/Series 32000 R&D Package contains the product, manuals and other documentation required in conjunction with VRTX/Series 32000 to develop a real-time embedded application which requires advanced, multitasking, device-level I/O facilities for peripherals. You can also purchase TRACER/Series 32000 and FMX/Series 32000 as separate R&D Packages or as bundled combinations.

Package Contents

The IOX/Series 32000 R&D Package contains:

One master copy of IOX in two 27128 PROMs

A boxtop license to make five copies of IOX (USA only)

Five Hunter & Ready Silicon Software copyright labels

Five IOX/Series 32000 User's Guides and Installation Guides

Customer Support Information

Release Notes

Customer Support

National Semiconductor offers a one year complete technical support period. Extended support provisions can be arranged by calling MCS Logistics at the toll-free numbers which follow.

The MCS Service Technical Support Engineering Center has highly trained technical specialists to assist customers over the telephone with product related technical problems.

For more information, please call:

(800) 538-1866 in the USA except for California
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(800) 223-3248 in Canada
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Licensing

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National also offers a Host-Based Package which includes the R&D packages ordered and the rights to make unlimited copies of VRTX, IOX, FMX and TRACER on a designated workstation or CPU or a Target-Based Package which includes the rights to make unlimited copies of the purchased R&D Packages (VRTX, IOX, FMX or TRACER) for a specific target product.

Ordering Information

NSW-IOX-BRVM IOX/Series 32000 in two 27128 EPROMs, and as files of S-records and define-byte records on a 1600 bpi 9-track VAX/VMS BACK-UP tape, manuals and R&D documentation.

NSW-IOX-BRVX IOX/Series 32000 in two 27128 EPROMs, and as files of S-records and define-byte records on a 1600 bpi 9-track VAX/4.2 bsd "tar" tape, manuals and R&D documentation.

NSW-IOX-BLAF IOX/Series 32000 in two 27128 EPROMs, and as files of S-records and define-byte records stored in MS-DOS format on 5¼ inch PC-DOS floppy diskette, manuals and R&D documentation.

NSW-IOX-SPNN IOX/Series 32000 source code listing.

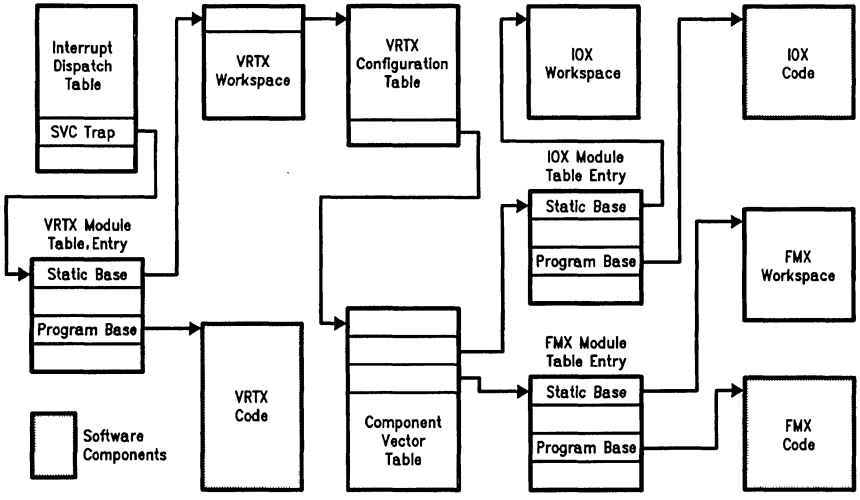
Documentation

NSW-IOX-MS IOX/Series 32000 Installation Guide and User's Guide.

IOX System Calls

Type	Call	Description
Initialization	IOINIT	Initialize IOX
Channel Control Services	IOOPEN	Open channel
	IOCLOSE	Close channel
	IOPOSN	Set file position
Buffered I/O Services	IOGET	Read bytes
	IOPUT	Write bytes
Direct I/O Services	IOREAD	Read block
	IOWRITE	Write block
	IOWAIT	Wait for I/O completion
	IORESET	Reset channel
	IOCNTRL	Perform device control
Device Definition Services	IODFBLK	Define general-block device
	IODFCHR	Define character device
	IODFDSK	Define disk device
	IORMDEV	Remove device definition
Device Interface Services	IOPOST	Post I/O request completion
	IOSTMR	Start device timer
	IOCTMR	Cancel device timer
	IOTIMER	Announce device timer interrupt
	IORXCHR	Put character into input buffer
	IORXCHM	Put multiple characters into input buffer
	IOECHO	Put character into echo buffer
	IOECHOM	Put multiple characters into echo buffer
	IOTXRDY	Get character from output buffer
	IOTXRDM	Get multiple characters from output buffer
	IOEXCPT	Call exception routine
Extension Services	IOATCHC	Attach I/O routine to IOX

FMX/Series 32000 R & D Package



TL/GG/8781-4

- **Multitasking, real-time file manager**
- **Works in conjunction with VRTX and IOX**
- **Can be installed in any Series 32000 hardware environment**
- **Can reside in PROM and be located anywhere in memory**
- **Allows multiple tasks to access files concurrently**
- **Supports buffered and direct I/O operations**
- **Supports sequential and random access for reads and writes**
- **Comprehensive manuals with many examples**
- **Hot-line technical support**
- **Supports hierarchical file structure compatible with Version 2.0 of PC-DOS**

FMX/Series 32000 is the File Management Executive for real-time, multitasking microprocessor applications based on the VRTX real-time executive. FMX is designed to provide disk file management services for VRTX- and IOX-based software systems. Like VRTX and IOX, FMX is a silicon software component; it makes no assumptions about the target environment.

FMX permits the organization of related information into resources called files and allocates these resources to tasks. The information managed by FMX has to be physically resident on a storage device (a magnetic disk). Its operations permit tasks to create and delete files, to assign attributes to these files, and to open IOX channels to them for subsequent use by IOX read and write operations. The IOX operations for reading and writing data to devices can then be used to read and write data to files instead.

FMX supports concurrent file accesses, along with other multitasking requirements and also supports both buffered and unbuffered direct read and write operations. Both sequential and random access methods are provided. FMX provides operations for creating and deleting directories, for referencing files relative to a specifed directory, and operations for mounting and dismounting volumes.

FMX has a facility for formatting disks, and this facility may be used to produce PC-DOS-compatible formats. FMX may be initialized so that it builds files on disks that are compatible with the file organization of PC-DOS.

FMX Features

File Management

FMX provides system calls for creating and deleting files, renaming files, and for getting and setting certain file characteristics. The file management calls and the directory management calls are implementations of the "generic file management operations" defined by IOX. IOX provides a thin layer of code that identifies these calls, then routes them to FMX for interpretation and execution.

Directory Management Services

FMX supports a hierarchical directory tree structure. It provides calls for creating directories in given directories and for deleting directories.

Volume Management Services

A logical collection of directories on a disk is called a volume. FMX provides a set of system calls to determine the characteristics of a new disk and to introduce the new disk to the system. These functions include evaluating volume parameters; mounting, dismounting, and synchronizing volumes; and obtaining volume attributes.

Formatting

Formatting is the process of writing the data addressing scheme on the disk or sub-disk. This addressing scheme makes it possible for the system to access precise locations on the disk so that data can be reliably written to and read from the disk. The FMX format system call, FDFMAT, provides the necessary tools to format disks in a variety of ways suitable for most.

Configuration

FMX is initialized via a special call, FDINIT. Initialization is the process by which FMX sets the starting values of all its internal data structures and variables. FMX must be initialized before it can perform any operations.

The FMX/Series 32000 R&D Package contains the product, manuals, and other documentation required in conjunction with VRTX/Series 32000 and IOX/Series 32000 to develop a real-time embedded application which requires advanced, multitasking, file management services. You can also purchase TRACER/Series 32000 as a separate R&D Package.

Package Contents

The FMX/Series 32000 R&D Package contains:

One master copy of FMX in two 27128 EPROMs

A boxtop license to make five copies of FMX (USA only)

Five Hunter & Ready Silicon Software copyright labels

Five FMX/Series 32000 User's Guides

Customer Support Information

Release Notes

Customer Support

National Semiconductor offers a one year complete technical support period. Extended support provisions can be arranged by calling MCS Logistics at the toll-free numbers which follow.

The MCS Service Technical Support Engineering Center has highly trained technical specialists to assist customers over the telephone with product related technical problems.

For more information, please call:

(800) 538-1866 in the USA except for California
(800) 672-1811 within California
(800) 223-3248 in Canada
(408) 749-7306 for rest of world

Licensing

All R&D packages are licensed through a National Semiconductor Binary software Licensing Agreement. In the United States, breaking the seal on the product package indicates acceptance of the terms of the licenses; no signature is required. For international sales a signed Binary Software License Agreement is required. If changes are required to the license agreement, contact the National Semiconductor Series 32000 Marketing Group prior to breaking the seal on the package.

National also offers a Host-Based Package which includes the R&D packages ordered and the rights to make unlimited copies of VRTX, IOX, FMX and TRACER on a designated workstation or CPU or a Target-Based Package which includes the rights to make unlimited copies of the purchased R&D Packages (VRTX, IOX, FMX or TRACER) for a specific target product.

Ordering Information

NSW-FMX-BRVM FMX/Series 32000 in two 27128 EPROMs, and as files of S-records and define-byte records on a 1600 bpi 9-track VAX/VMS BACKUP tape, manuals and R&D documentation.

NSW-FMX-BRVX FMX/Series 32000 in two 27128 EPROMs, and as files of S-records and define-byte records on a 1600 bpi 9-track VAX/4.2 bsd "tar" tape, manuals and R&D documentation.

NSW-FMX-BLAF FMX/Series 32000 in two 27128 EPROMs, and as files of S-records and define-byte records stored in MS-DOS format on a 5¼ inch PC-DOS floppy diskette, manuals and R&D documentation.

NSW-FMX-SPNN FMX/Series 32000 source code listing.

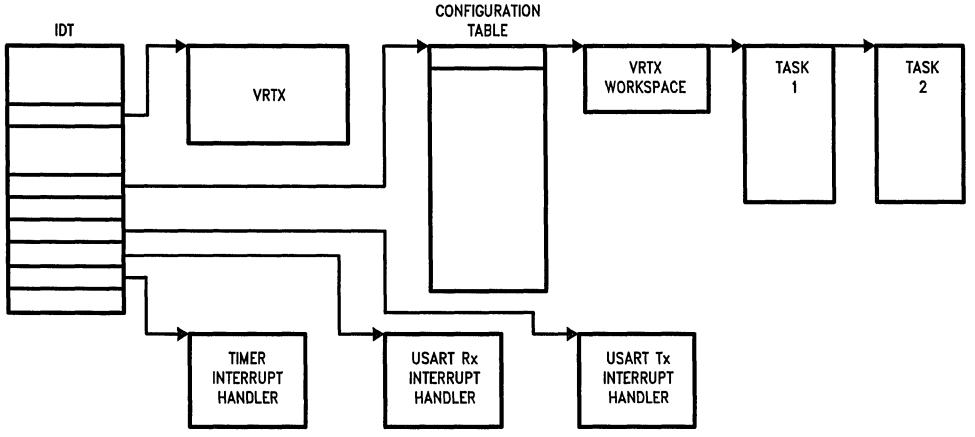
Documentation

NSW-FMX-M FMX/Series 32000 User's Guide.

FMX Service Calls

Type	Call	Description
Initialization	FDINIT	Initialize FMX
File Management Services	FMCREAT	Create file
	FMDELET	Delete file
	FMRENAM	Rename file
	FMGATTR	Get file attributes
	FMSATTR	Set file attributes
Directory Management Services	FMMKDIR	Make subdirectory
	FMRMDIR	Remove subdirectory
File I/O Services	FMOPEN	Open file
Volume Management Services	FDMOUNT	Mount volume
	FDDISMT	Dismount volume
	FDSYNC	Synchronize volume
	FDEVOL	Evaluate volume parameters
	FDQVOL	Get volume attributes
Formatting	FDFMAT	Format disk

VRTX/Series 32000 Board Support Package for National's Series 32000-Based Boards



TL/GG/8781–2

- **Board support routines for popular National Series 32000 boards**
- **Brings up a tested VRTX, IOX, FMX and TRACER application immediately**
- **Includes all code to initialize and run VRTX, IOX, FMX and TRACER**
- **Includes code for sample VRTX, IOX, and FMX application**
- **Routines can be used as templates for other boards**

The routines in this package provide all the code needed to build and run a simple VRTX application (with or without TRACER) on several of National's Series 32000 boards. The application, which is documented in the manual "How to Write a Board Support Package for VRTX", consists of two tasks, one of which receives characters from an interrupting character I/O device and posts them to a VRTX mailbox. The second task pends at the mailbox for the characters and outputs them to the I/O device using VRTX.

The VRTX support routines for each board include:

— Configuration table specific to the board,
— Device initialization code for National's ICU chip (NS32202),
— Initialization code for the timer and serial I/O channel,
— Code to initialize the 32000 data structures including the Interrupt Dispatch Table, Module Table and stack,
— Receive and transmit interrupt handler code,
— Timer interrupt handler code,
— The application configuration table.

For designers wishing to have the TRACER debugger in the system, there are also board support routines with the code needed to run the application with TRACER. In addition to the code described above, these routines include:

— TRACER configuration table,
— TRACER initialization code,
— TRACER character I/O handler code
— VRTX/TRACER interface code.

For IOX, an example device driver for a serial I/O device and a disk controller are provided, along with all of the necessary configuration support software. A FMX example is also provided which runs using either a ramdisk driver or a disk driver. Example disk drivers are provided for several disk controllers.

VRTX, IOX, FMX and TRACER support routines are supplied for National's DB32016, DB32000 and DB332 development boards.

Product Contents

VRTX, IOX, FMX and TRACER board support routines (written in Series 32000 Assembly Language) for National's Series 32000 development boards: DB32016, DB32000 and DB332

Source code for sample tasks described in the manual

Customer Support Information

Installation Guide

Release Documentation

Prerequisites

The syntax in the source code files in this product conform to the standards and conventions used in National's GNX Language Tools Packages. Designers wishing to assemble the files will need the GNX Language Tools or their equivalent. Users of other software development tools may have to modify the source code in order to conform to the requirements of their tools.

See the National Semiconductor datasheet titled "Series 32000 GENIX Native and Cross-Support (GNX) Language Tools" for information about National's tools.

Customer Support

National Semiconductor offers a one year complete technical support period. Extended support provisions can be arranged by calling MCS Logistics at the toll-free numbers below.

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Ordering Information

NSW-VBSP-SRVM	VRTX, IOX and FMX/Series 32000 Board Support Packages on 1600 bpi 9-track reel tape in VAX/VMS BACKUP format; manual and other documentation.
NSW-VBSP-SRVX	VRTX, IOX and FMX/Series 32000 Board Support Packages on 1600 bpi 9-track reel tape in VAX/4.2 bsd "tar" format; manual and other documentation.
NSW-VBSP-SLAF	VRTX, IOX and FMX/Series 32000 Board Support Packages stored in MS-DOS format on a SYS32/20 5¼ inch PC-DOS floppy diskette; manual and other documentation.

VRTX, IOX and FMX/Series 32000 Support Libraries

- **Routines encourage writing VRTX, IOX and FMX applications in C or Pascal**
- **Interface routines matched to National's GNX Language Tools**
- **Package available on same media as National's GNX tools**
- **C Run-Time Library extends C for concurrent programming**
- **C Run-Time support for standard input-output (stdio) functions**
- **Integrates standard I/O run-time library (stdio) with real-time services of VRTX/OS**
- **Hook routines included to add floating-point support to VRTX**

This package provides libraries that simplify the writing of VRTX-based applications in C or Pascal rather than just Series 32000 Assembly Language. The VRTX, IOX and FMX Interface Library enables the designer to make system calls to VRTX, IOX and FMX from C or Pascal programs. The C Run-Time Library supports the standard function calls made from C programs and, where appropriate, invokes services from VRTX, IOX or FMX. Some of the run-time library routines require IOX and FMX as well as VRTX.

Interface Libraries

Since requests for VRTX, IOX and FMX services are made with supervisor calls (SVCs) that can only be performed from assembly language programs, a high level language program must call interface routines to use VRTX, IOX and FMX services. The interface libraries are collections of Series 32000 assembly language routines that logically sit between a C or Pascal program and VRTX, IOX and FMX. When a function is called from the program, the appropriate library routine accepts the parameters from the caller and performs a Series 32000 supervisor call (SVC) to VRTX, IOX and FMX. When VRTX, IOX and FMX return from processing the call, the routine transforms the results into the form expected by the caller and returns control.

The VRTX, IOX and FMX Interface Libraries contain routines to handle calls for task management, intertask communications, memory management, timing services, simple character I/O, allocating device resources, providing a consistent I/O interface, and disk file management. There are no routines for VRTX interrupt handler calls because interrupt handlers are typically written in assembly language and can issue SVCs directly.

The interface routines are written in Series 32000 assembly language and delivered in source code form as well as in libraries of object modules (GNX "ar" format). The assembly language syntax and calling sequences conform to the conventions in National's GNX Language Tools packages.

The VRTX/Series 32000 C Run-Time Library

The C Run-Time Library provides external run-time functions not provided by the C language. It contains character and file I/O, string manipulation, floating-point routines, storage allocation and file management functions. The library functions make calls to the VRTX kernel and, for certain I/O operations, to IOX and FMX. Library functions return an error code if a call is made to a VRTX/OS component absent from the system.

If VRTX is operating in a Series 32000 hardware environment with National's Floating-Point Unit (NS32081), the designer can use hook routines supplied in the library to expand VRTX task management to handle the floating-point environment.

All C Run-Time Library functions are re-entrant, that is, they can be used asynchronously by several tasks. Tasks can share a common copy of function code to save memory space. When a task using a function is interrupted by another task before it finishes with the function, the interrupting task can use the same copy of the function code without corrupting the original task's data.

The C Run-Time Library is delivered as a library of object modules (GNX "ar" format). As a convenience for the VRTX system designer, the library also contains the object modules for the C Interface Library and VRTX hook routines. Like the interface routines the hook routines are included in the package in source code form.

Package Contents

VRTX, IOX, and FMX C Interface Library source code (in GNX assembly language)
VRTX, IOX, and FMX C Interface Library as object module library (GNX "ar" format)
VRTX Pascal Interface Library source code (in GNX assembly language)
VRTX Pascal Interface Library as object module library (GNX "ar" format)
C Run-Time Library as object module library (GNX "ar" format)

VRTX C Language User's Guide
VRTX Pascal Language User's Guide
IOX C User's Guide
FMX C User's Guide
C Run-Time Library User's Guide
Customer Support Information
Release Documentation & Installation Guide

VRTX C Interface Routines and Calling Sequences

Task Management	
sc_tcreate (task, tid, pri, &err)	Create Task
sc_tdelete (tid/pri, code, &err)	Delete Task
sc_tsuspend (tid/pri, code, &err)	Suspend Task
sc_tresume (tid/pri, code, &err)	Resume Task
sc_tpriority (tid, pri, &err)	Change Task Priority
tcb = sc_tinquiry (info, tid, &err)	Task Inquiry
sc_lock( )	Disable Rescheduling
sc_unlock( )	Enable Rescheduling
Communication and Synchronization	
sc_post (&mbox, msg, &err)	Post Messge to Mailbox
msg = sc_pend (&mbox, timeout, &err)	Pend for Message from Mailbox
msg = sc_accept (&mbox, &err)	Accept Message from Mailbox
sc_qcreate (qid, qsize, &err)	Create Queue
sc_qpost (qid, msg, &err)	Post Message to Queue
msg = sc_qpend (qid, timeout, &err)	Pend for Message from Queue
msg = sc_qaccept (qid, &err)	Accept Message from Queue
Memory Management	
block = sc_gblock (pid, &err)	Get Memory Block
sc_rblock (pid, block, &err)	Release Memory Block
sc_pcreate (pid, paddr, psize, bsize &err)	Create Memory Partition
sc_pextend (pid, paddr, psize, &err)	Extend Memory Partition
Real-Time Clock	
time = sc_gtime ( )	Get Time
sc_stime (time)	Set Time
sc_delay (ticks)	Delay Task
sc_tslice (ticks)	Enable Timeslicing
Character I/O	
char = sc_getc ( )	Get Character
sc_putc (char)	Put Character
sc_waitc (char, &err)	Wait for Special Character

IOX C Interface Routines and Calling Sequences

Direct I/O Functions	
iocntrl (chnl, code, &info, opts, &err)	Perform Device Control
bytes = ioread (chnl, buf, count, opts, &err)	Read a Block
ioreset (chnl, opts, &err)	Reset I/O Channel
iowrite (chnl, buf, count, opts, &err)	Write a Block
iowait (chnl, opts, &err)	Wait for Outstanding I/O
Buffered I/O Functions	
bytes = ioget (chnl, buf, count, opts, &err)	Read Bytes
ioput (chnl, buf, count, opts, &err)	Write Bytes
Channel Control Functions	
chnl = ioopen (devid, devtype, opts, &err)	Open a Channel
ioclose (chnl, opts, &err)	Close a Channel
posn = ioposn (chnl, offset, opts, &err)	Set Position
IOX System Services—Block Devices	
iopost (&dsrb, opts, &err)	Post I/O Request Completion
iostmr (&dsrb, ticks, opts, &err)	Start a Request Timer
ioctmr (&dsrb, opts, &err)	Cancel a Request Timer
iotimer (opts, &err)	Announce I/O Timer Interrupt
IOX System Services—Character Devices	
rcnt = iorxchr (ddtep, chr, opts, &err)	Put a Character into Receiver or Typehead Buffer
rcnt = iorxchm (ddtep, buf, len, opts, &err)	Put Characters into Receiver or Typehead Buffer
rcnt = ioecho (ddtep, chr, opts, &err)	Put a Character into Echo Buffer
rcnt = ioechom (ddtep, buf, len, opts, &err)	Put Characters into Echo Buffer
chr = iotxrdy (ddtep, opts, &err)	Get a Character from Transmitter or Echo Buffer
rcnt = iotxrdm (ddtep, buf, len, opts, &err)	Get Characters from Transmitter or Echo Buffer
IOX System Services—Device Definition	
ddtep = iodfchr (devid, &desc, &info, opts, &err)	Define a Character Device
iodfblk (devid, &desc, &info, opts, &err)	Define a Block Device
iodfdsk (devid, &desc, &info, opts, &err)	Define a Disk Device
iormdev (devid, opts, &err)	Remove a Device Definition
IOX System Services—Initialization, Extension, and Exception	
ioinit (&inipk, &err)	Initialize IOX
ioatchc (&atcpk, &err)	Attach an I/O Handler
ioexcpt (ecode, opts, &err)	Raise an I/O Exception
System Call Function	
sc_call (fcode, &packet, &err)	Call a Component

FMX C Interface Routines and Calling Sequences

File Management Functions	
fmcreat (ref_chan, pathname, init_alloc, options, &err)	Create a File
fmdelet (ref_chan, pathname, options, &err)	Delete a File
fmgattr (ref_chan, pathname, &attr, &timpk, &file_len, options, &err)	Get File Attributes
fmrenam (ref_chan, old, new, options, &err)	Rename a File
fmsattr (ref_chan, pathname, attr, &timpk, file_len, options, &err)	Set File Attributes
Directory Management Functions	
fmmkdir (ref_chan, pathname, options, &err)	Create a Directory
fmrmdir (ref_chan, pathname, options, &err)	Remove a Directory
File I/O Functions	
channel = fmopen (ref_chan, pathname, devtype, options, &err)	Open a Channel to a File
ioclose (channel, options, &err)	Close a Channel
bytes = ioget (channel, buffer, count, options, &err)	Read Bytes
position = ioposn (channel, offset, options, &err)	Set Position
ioput (channel, buffer, count, options, &err)	Write Bytes
bytes = ioread (channel, buffer, count, options, &err)	Read a Block
ioreset (channel, options, &err)	Reset I/O Channel
iowait (channel, options, &err)	Wait for Outstanding I/O
iowrite (channel, buffer, count, options, &err)	Write a Block
Volume Management Functions	
fddismt (device, options, &err)	Dismount a Volume
fdevol (&volpk, &err)	Evaluate Volume Parameters
fdfmat (&volpk, &err)	Format a Volume
root_chan = fdmount (&volpk, &err)	Mount a Volume
fdqvol (&volpk, &err)	Query Volume Attributes
fdsync (device, options, &err)	Synchronize a Volume
Initialization Function	
fdinit (&inipk, &err)	Initialize FMX
Extension Functions	
hook_addr = fdhook (func, hbuf)	Build Hook Routines
sc_call (fcode, &packet, &err)	Call a Component

VRTX Pascal Interface Routines and Calling Sequences

Task Management	
sctcreate (task, tid, pri, err)	Create Task
sctdelete (tid/pri, code, err)	Delete Task
sctsuspend (tid/pri, code, err)	Suspend Task
sctresume (tid/pri, code, err)	Resume Task
sctpriority (tid, pri, err)	Change Task Priority
tcb: = sctinquiry (info, tid, err)	Task Inquiry
sclock ( )	Disable Rescheduling
scunlock ( )	Enable Rescheduling
Communication and Synchronization	
scpost (mbox, msg, err)	Post Message to Mailbox
msg: = scpend (mbox, timeout, err)	Pend for Message from Mailbox
msg: = scaccept (mbox, err)	Accept Message from Mailbox
scqcreate (qid, qsize, err)	Create Queue
scqpost (qid, msg, err)	Post Message to Queue
msg: = scqpend (qid, timeout, err)	Pend for Message from Queue
msg: = scqccept (qid, err)	Accept Message from Queue
Memory Management	
block: = scgblock (pid, err)	Get Memory Block
scrblock (pid, block, err)	Release Memory Block
scpcreate (pid, paddr, psize, bsize, err)	Create Memory Partition
scpextend (pid, paddr, psize, err)	Extend Memory Partition
Real-Time Clock	
time: = scgtime ( )	Get Time
scstime (time)	Set Time
scdelay (ticks)	Delay Task
sctslice (ticks)	Enable Timeslicing
Character I/O	
char: = scgetc ( )	Get Character
scputc (char)	Put Character
scwaitc (char, err)	Wait for Special Character

C Run-Time Library Routines

Character and String Routines

bcmp	isalnum	isdigit	isxdigit	strcpy	strrchr
bcopy	isalpha	islower	rindex	strcrspn	toascii
bfill	isascii	isodigit	sprintf	strlen	toint
brev	isblank	isprint	sscanf	strncat	tolower
bzero	iscntrl	ispunct	strcat	strncmp	toupper
ffs	iscsym	isspace	strchr	strncpy	swab
index	iscsymf	isupper	strcmp	strpbrk	upper
iswhite	lower	reverse	strsave	strspn	

Integer Mathematical Routines

abs	atol	atoi	min	max	sign
labs	rand	srand			

Floating-Point Mathematical Routines

acos	atof	exp	hypot	modf	tan
asin	cabs	fabs	ldexp	pow	sinh
atan	ceil	floor	log	sin	cosh
atan2	cos	frexp	log10	sqrt	tanh
square	idexplo	frexplo			

Exception Handling

long jmp	set jmp

Miscellaneous Routines

abort	swab	exit

VRTX Memory Management

calloc	free	malloc	realloc	rcopy

VRTX I/O

gets	getchar	puts	printf	putchar	scanf

IOX & FMX Buffered I/O

clearerr	fflush	fputc	fseek	putc	setlinebuf
fclose	fgetc	fputs	ftell	putw	ungetc
fdopen	fgets	fread	fwrite	rewind	sscanf
feof	fopen	freopen	getc	setbuf	xprintf
ferror	fprintf	fscanf	getw	setbuffer	xscanf
fdreopen	sprintf	fileno	frewind	setnbf	

Prerequisites

Compiling source code files and linking members of object module libraries requires National's GNX language tools (in native or cross support versions) on the host system. See the National Semiconductor datasheet titled "Series 32000 GENIX Native and Cross-Support (GNX) Language Tools" for information.

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Ordering Information

NSW-VIL-SRVM	VRTX/Series 32000 Support Libraries on 1600 bpi 9-track reel tape in VAX/VMS BACKUP format; manuals and other documentation.
NSW-VIL-SRVX	VRTX/Series 32000 Support Libraries on 1600 bpi 9-track reel tape in VAX/4.2 bsd "tar" format; manuals and other documentation.
NSW-VIL-SLAF	VRTX/Series 32000 Support Libraries stored in MS-DOS format on a SYS32/20 5¼ inch PC-DOS floppy diskette; manuals and other documentation.
NSW-IIL-SRVM	IOX/Series 32000 Support Libraries on 1600 bpi 9-track reel tape in VAX/VMS BACKUP format; manuals and other documentation.
NSW-IIL-SRVX	IOX/Series 32000 Support Libraries on 1600 bpi 9-track reel tape in VAX/4.2 bsd "tar" format; manuals and other documentation.
NSW-IIL-SLAF	IOX/Series 32000 Support Libraries stored in MS-DOS format on a SYS32/20 5¼ PC-DOS floppy diskette; manuals and other documentation.
NSW-FIL-SRVM	FMX/Series 32000 Support Libraries on 1600 bpi 9-track reel tape in VAX/VMS BACKUP format; manuals and other documentation.
NSW-FIL-SRVX	FMX/Series 32000 Support Libraries on 1600 bpi 9-track reel tape in VAX/4.2 bsd "tar" format; manuals and other documentation.
NSW-FIL-SLAF	FMX/Series 32000 Support Libraries stored in MS-DOS format on a SYS32/20 5¼ PC-DOS floppy diskette; manuals and other documentation.

Documentation

NSP-VC-M	VRTX C User's Guide
NSP-RTC-M	C Run-Time Library User's Guide
NSP-VPAS-M	VRTX Pascal User's Guide
NSP-IC-M	IOX C User's Guide
NSP-FC-M	FMX C User's Guide

TRACER/Series 32000 R&D Package

- **Operates without modification in any VRTX/Series 32000 hardware environment**
- **Companion product to VRTX: displays VRTX TCB's, mailboxes, queues and buffers**
- **Operates independently of VRTX; does not run as a task**
- **Resides in PROM and can be located anywhere in memory**
- **Allows breakpoints by task or in user-written system code**
- **Displays and modifies memory or registers by task**
- **Provides single-stepping, downloading and disassembly**
- **Can be extended to support user-defined features**
- **Independent of software development environment**
- **Comprehensive manual with many examples**

TRACER/Series 32000 is an interactive multitasking debugger designed for use with VRTX/Series 32000-based systems. TRACER runs in parallel with the multitasking environment rather than as a task. This permits it to monitor and control program execution without competing with tasks for system resources like task control blocks and queues. It does not distort system behavior by affecting the competition of tasks for access to the CPU. Since TRACER has its own data structures, it does not depend on the correct execution of the VRTX-based system for its own execution. If bugs in an application task cause a system crash, TRACER survives and provides a means to diagnose the problem.

There are no dependencies on the host system development environment. TRACER is not linked with user task code. Installation in a system requires only plugging the TRACER PROMs into the target board, building a configuration table to tell TRACER about the hardware environment, and supplying a small device-specific interrupt handler for the TRACER communications I/O channel. TRACER can be hooked into a VRTX-based system during development, and removed completely for production.

TRACER commands are entered interactively via a character-oriented device, usually a terminal. When a spare I/O channel is available, TRACER can use it; otherwise, it can share the terminal associated with VRTX's character I/O facility. TRACER command processing can be extended by adding user-written routines (filters) at hooks called before command processing, and before displays are sent to the output terminal. This permits changes to command syntax, macro-like command expansion and customized displays.

TRACER supports up to 16 breakpoints, each with a unique iteration count. Breakpoints can be set by task, which is useful for debugging code shared between tasks. Since TRACER operates outside the multitasking environment, it can set breakpoints in I/O routines, interrupt service routines, and in user-written system code.

TRACER can display VRTX system structures such as task control blocks, mailboxes, queues and I/O buffers in tabular form with their contents interpreted in easy-to-read format rather than as memory locations.

TRACER can examine a range of memory locations and display them in hex, ASCII or as disassembled code. The contents of a location can be changed, or all locations in a range can be set to a value. Registers can be displayed and modified for any task. For non-executing tasks, TRACER can display and modify the register values directly in the TCB. A disassembler within TRACER can translate binary code into assembly mnemonics. The TRACER on-line help facility also provides the programmer with a brief summary of TRACER command syntax and options.

TRACER Command Summary

Breakpoint Commands

sb	Set Breakpoint
db	Display Current Breakpoints
rb	Remove Breakpoint

Memory and Register Commands

sm	Set Memory
dm	Display Memory in Hex and ASCII
sr	Set Registers for a Task
dr	Display Registers for a Task or System Routine

Execution Control Commands

rx	Resume Execution
xs	Execute Single Step
tc	Switch to Command Mode
tt	Switch to Tasking Mode

System Status Commands

ds	Display System Status
dt	Display Task Status
dq	Display Queue Status
dx	Display Mailbox Pends
di	Display Input Buffer Contents & Status
do	Display Output Buffer Contents & Status

Other Commands

dl	Download Code from Host System
li	List Disassembled Code
he	Display TRACER Commands & Arguments

Package Contents

The TRACER/Series 32000 R&D package contains:

One master copy of TRACER in two 27128 PROMs
A boxtop license to make five copies of TRACER (USA only)
Five sets of Hunter & Ready Silicon Software copyright labels
Five TRACER/Series 32000 User's Guides
Customer Support information
TRACER 32000 release notes

Customer Support

National Semiconductor offers a one year complete technical support period. Extended support provisions can be arranged by calling MCS Logistics at the toll-free numbers below.

The MCS Service Technical Support Engineering Center has highly trained technical specialists to assist customers over the telephone with product related technical problems.

For more information, please call:

(800) 538-1866 in the USA except for California
(800) 672-1811 within California
(800) 223-3248 in Canada
(408) 749-7306 for rest of world

Licensing

All R&D packages are licensed through a National Semiconductor Binary Software Licensing Agreement. In the United States, breaking the seal on the product package indicates acceptance of the terms of the license; no signature is required. For international sales a signed Binary Software License Agreement is required. If changes are required to the license agreement, contact the National Semiconductor Series 32000 Software Marketing Group before breaking the seal on the package.

Ordering Information

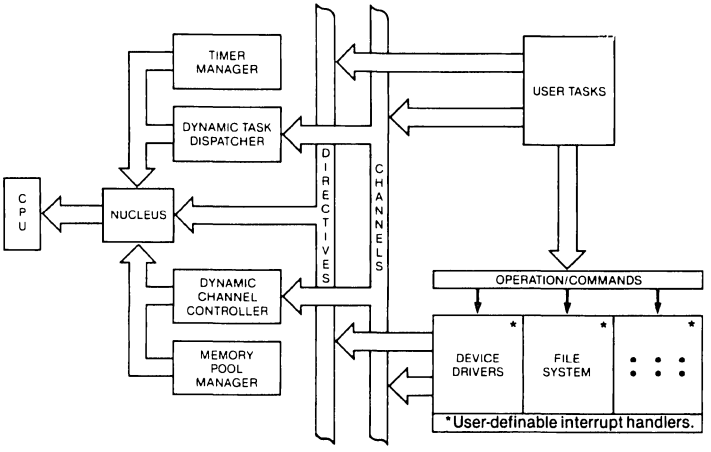
NSW-TRAC-BRVM	TRACER/Series 32000 in two 27128 EPROMs, and as files of S-records and define-byte records on a 1600 bpi 9-track VAX/VMS BACKUP tape, manuals and R&D documentation.
NSW-TRAC-BRVX	TRACER/Series 32000 in two 27128 EPROMs, and as files of S-records and define-byte records on a 1600 bpi 9-track VAX/4.2 bsd "tar" tape, manuals and R&D documentation.
NSW-TRAC-BLAF	TRACER/Series 32000 in two 27128 EPROMs, and as files of S-records and define-byte records stored in MS-DOS format on a SYS32/20 5¼ inch PC-DOS floppy diskette, manuals and R&D documentation.
NSW-TRAC-SPNN	TRACER/Series 32000 source code listing.

Documentation

NSP-TRAC-M	TRACER/Series 32000 User's Guide

National Semiconductor

Series 32000® EXEC ROMable Real-Time Multitasking EXECUTIVE



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- **Provides a multitasking executive for real-time applications**
- **Supports all Series 32000 CPUs**
- **Complete Source Code Package**
  - — Fully user configurable
  - — Hardware independent
- **Extensive user implementation support**
  - — Unique demo, program introduction
  - — C and Pascal interface libraries
  - — Sample terminal drivers
  - — Integrated with Series 32000 development boards and monitor
- **ROMable**
- **Reconfigurable**
- **Real-time clock support for time-of-day and event scheduling**
- **Allows up to 256 levels of task priority which can be dynamically assigned**
- **Up to 256 logical channels for task communication**
- **Free-memory pool control**
- **Available for VAX™/VMS™, VAX/UNIX® and SYS32™ development environments**

Product Overview

EXEC is National Semiconductor's real-time, multitasking executive for Series 32000 based applications. Its primary purpose is to simplify the task of designing application software and provides a base upon which users can build a wide range of application systems. EXEC requires only 2K bytes of RAM and only 4K bytes of ROM and is fully compatible with National Semiconductor's Series 32000 family and the Series 32000 development board family.

EXEC allows the user to monitor and control multiple external events that occur asynchronously in real-time, such as intertask communications, system resource access based upon task priority, real-time clock control, and interrupt handling. These functions greatly simplify application development in such areas as instrumentation and control, test and measurement, and data communications. In these applications, EXEC provides an environment in which systems programmers can immediately implement software for their particular application without regard to the details of the system interaction.

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EXEC executive is fully modular and can be readily configured to suit application needs. It is both hardware and location independent, thus providing a fundamental base on which to build a wide range of applications systems. In addition, it provides a buslike structure that helps to integrate software with the underlying hardware through predefined data structures and interconnect procedures. This architecture ensures maximum standardization for both compatibility and future expansion.

Features

Structured Environment—The EXEC executive and its associated modules support and encourage modular, structured programming, thus providing a consistent structure from application to application, which allows experience gained and software written on one system to be easily transferred to another. Frequently, entire programs may be used in multiple applications, *even if different CPU boards are involved.*

Hardware-Oriented Interface—The EXEC executive provides an intertask and task/executive communications architecture that is similar to hardware communications. Instead of an array of "mailboxes" (or "message centers"), EXEC uses channels. This interface is consistent throughout the range of facilities offered, thus reducing the number of concepts to be learned, providing greater control at the task level, and increasing the efficiency of the system and the programming effort.

Wide Choice of CPUs—EXEC is compatible with the full line of 32-bit Series 32000 CPUs offered. These include the NS32008, NS32032, and the NS32C016. Users will be able to move a NS32016 system:

- to an NS32008 for cost-effectiveness,
- to an NS32032 for increased computing power, or
- to an NS32C016 for low-power applications.

Time-Of-Day Clock—The EXEC executive has an integral system/time-of-day clock. Included is a real-time clock configurable to a resolution of 1ms. This eliminates the need to allocate the extra memory otherwise required for this feature.

Small Nucleus—The EXEC nucleus was hand-coded in assembly language rather than being compiled from intermediate or high-level languages. The resulting product is therefore smaller and allows the incorporation of more features within an optimum size.

Priority-Oriented Scheduler—The EXEC scheduler ensures that the highest priority task that is ready to execute is given control, so the system is responsive to its external world. Dynamic reprioritization of tasks is supported for the most sophisticated of multitasking systems.

Real-Time Speed—Because EXEC was hand-coded in assembly language, several advantages with regard to speed are gained. Task swapping, channel and message management, and I/O interfacing are executed more quickly than could be expected of a system written in a higher level language.

Direct Interrupt Processing—The EXEC architecture employs interrupt channels which allow device-specific interrupt handling routines to interface directly with the interrupt source. This accomplishes servicing of interrupts without the overhead of task swapping, yet allows the operating system to maintain the integrity of the system. Combining this interrupt service architecture with a device-efficient nucleus results in an operating system that better supports demanding, real-time applications.

User Configurability—EXEC executive-based applications may be configured from a wide range of facilities, selecting only those that meet the specific requirements of the application system. The resultant system contains only the modules necessary for its use, allowing the EXEC executive to fit a wide range of applications from small, special-purpose, dedicated applications to large, general-purpose systems.

Event Driven—In the EXEC executive, each user task exists in its own "closed environment"—a virtual processor. Each virtual processor can synchronize with external/internal occurrences through events. EXEC supports a wide variety of events, including synchronization with task activities, external device operations, and the real-time clock.

Memory Pool Manager—The EXEC executive has an integral memory pool manager. This feature not only reduces the amount of RAM required in an application system (potentially reduces board count), but also allows active modules more buffer area within any given space constraint.

Internal Structure

EXEC may be viewed as composed of a set of functions. These functions are:

1. Nucleus— performs task and channel management and controls executing memory.
2. Timer Manager—performs time-dependent control.
3. Dynamic Task Dispatcher—performs dynamic creation and installation of tasks at run-time.
4. Dynamic Channel Controller—performs dynamic creation and installation of software and interrupt channels at run-time.
5. Memory Pool Manager—performs memory allocation and deallocation.

The Timer Manager, Dynamic Task Dispatcher, Dynamic Channel Controller, and the Memory Pool Manager all operate under direction of the Nucleus, which assigns tasks to run on the hardware CPU.

System Functions

EXEC controls CPU allocation by resolving conflicting needs of individual tasks, and monitors external events. The Event Manager, Task Manager, Channel Manager, Memory Manager, and Timer Manager provide system facilities that are directly accessible from the user task level. A representative sampling of system functions are summarized below:

- **Task and Event Management**

1. TSKBD —Build a task and schedule it to run.
2. SUSPD —Suspend a task.
3. GTPRI —Get task priority.
4. STPRI —Change run-time task priority.
5. WAITE —Wait for an event or combination of event to occur before resuming task processing.
6. TSTEV —Test the current state of an event.

- **Intertask Communication**

1. RECV(W) —Receive data from a channel and, optionally, wait for an event to occur.
2. SEND(W) —Send a message to a channel and, optionally, wait for an event to occur.
3. SIGNL —Synchronize with another task through event flags; signal completion.
4. BLDSC —Build software channel.

- **Interrupt Handling**

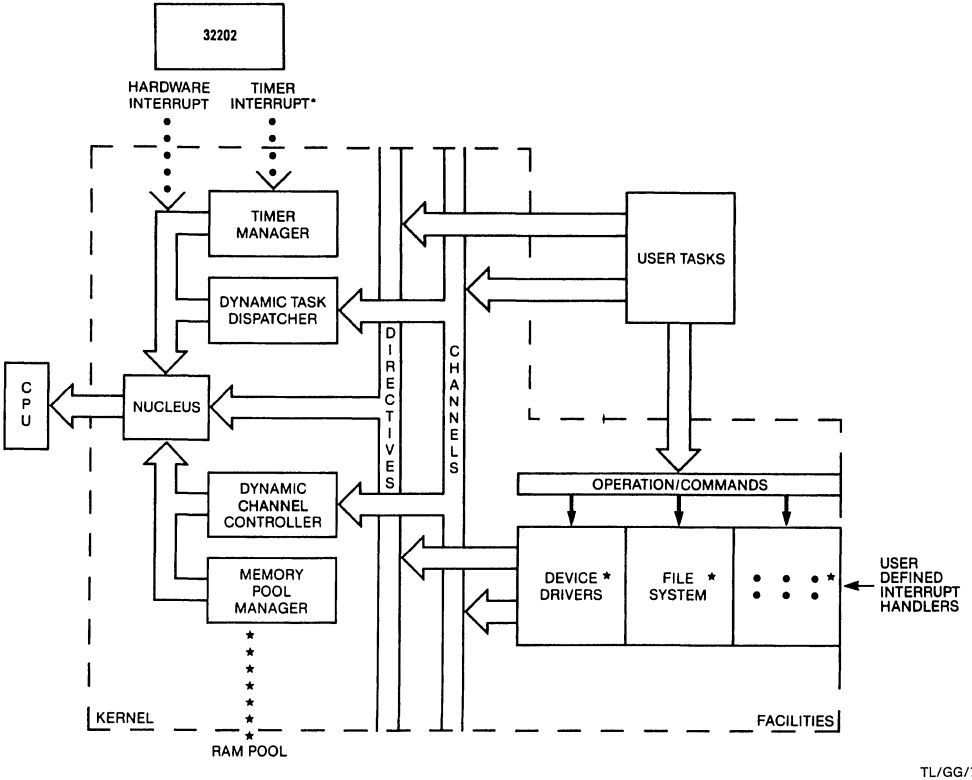
1. INTEX —Interrupt exit from executive.
2. BLDIC —Build an interrupt channel.

- **Memory Pool Management**

1. ALLOC —Allocate a block of pooled memory.
2. DALOC —Deallocate memory back to pool.

- **Timer Management**

1. MRKT(W) —Mark a time delay and, optionally, wait for an event to occur.
2. CMRKT —Cancel previously posted mark-time event.
3. GTIMD —Get current time of day.
4. STIMD —Set current time of day.



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* May or may not be from 32202 ICU.

FIGURE 1. EXEC Structure

Ordering Information

VAX/VMS Environment

Order Number: NSW-EXEC-SRVM*

Shipping Configuration: Software on 1600 bpi magnetic tape (9-track VMS copy format). EXEC reference manual.

Prerequisite: NSW-ASM-BRVM cross software package, at current revision level.

VAX/UNIX Environment

Order Number: NSW-EXEC-SRVX*

Shipping Configuration: Software on 1600 bpi magnetic tape (UNIX tar tape format). EXEC reference manual.

Prerequisite: NSW-ASM-BRVX* cross software package, at current revision level.

SYS32/20, SYS32/30 Environments

Order Number: NSW-EXEC-SLAF

Shipping Configuration: Software on SYS32 format streamer tape cartridge. EXEC reference manual.

Prerequisite: SYS32/20 or SYS32/30 Development System with current revision level software.

Documentation

EXEC ROMable Real-Time Multitasking EXECUTIVE Reference Manual. Included with software package. May also be ordered separately.

Order Number: NSP-EXEC-M

*Software license agreement must be signed prior to order entry.

Section 8

Application Notes

Section 8 Contents

Instruction Execution Times of FPU NS32081 Considered for Stand-Alone Configurations

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The table below gives execution timing information for the FPU NS32081.

The number of clock cycles nCLK is counted from the last SPC pulse, strobing the last operation word or operand into the FPU, and the Done-SPC pulse, which signals the CPU that the result is available (see *Figure 1*). The values are therefore independent of the operand's addressing modes and do not include the CPU/FPU protocol time. This makes it easy to determine the FPU execution times in stand-alone configurations.

The values are derived from measurements, the worst case is always assumed. The results are given in clock cycles (CLK).

Operation	Number of Clock-Cycles nCLK
Add, Subtract	63
Multiply Float	37
Multiply Long	51
Divide Float	78
Divide Long	108
Compare	38

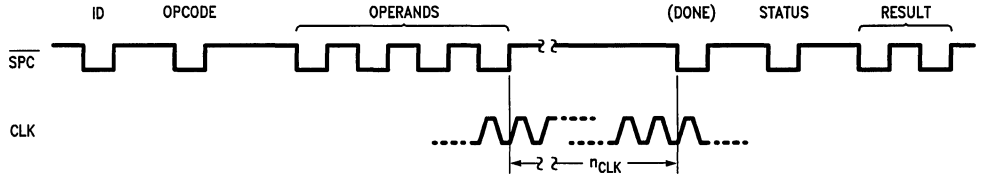

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FIGURE 1

Use of the NS32332 with the NS32082 and the NS32201

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Systems Applications Group

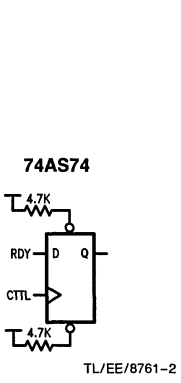
Care should be taken when the NS32332 is designed in a system with the NS32201 and the NS32082. Two configurations need to be considered, one with MMU and one without.

In a configuration without an MMU, TCU and CPU both run a four clock cycle bus (*Figure 1*). The RDY signal is the only incompatible signal between the CPU and TCU and therefore the RDY output of the TCU should not be directly connected to the RDY input of the NS32332. The NS32332 samples its RDY input in the middle of T3 while the NS32201 asserts its RDY output shortly after the middle of T2 and removes it shortly after the middle of T3, thus the NS32332 RDY input hold time (tRDYh) is not met. To meet tRDYh, the RDY output of the NS32201 should be clocked by the rising edge of the CTTL using a D-type flip-flop (74AS74) and then taken to the NS32332. It should be noted that the NS32332 outputs the data in a write cycle in T3 unless DT/SDONE pin is sampled low on the rising edge of the reset in which case the data is output during T2. The DT/SDONE pin is implemented as of revision B of the NS32332.

In a configuration with MMU the NS32332 runs a four clock cycle bus while the NS32082 runs a five cycle bus. Two options can be exercised.

The first option is extending the NS32332 bus cycle to five clocks by adding a blind wait state that bypasses the NS32201 (*Figure 2*). This configuration generally requires the minimum hardware modification for a 320xx based design to run the NS32332. Here the NS32201 output signals can be used to interface the NS32332 and the NS32082 to the memory or I/O. Additional wait states can be inserted by clocking the RDY output of the TCU.

The second option is to have the NS32332 run a four clock cycle bus (*Figure 3*). In this configuration the NS32201 output signals cannot be used to interface the NS32332 to memory or I/O; they can only be used to interface the NS32082 to the memory. In this configuration a revision N of the NS32082 should be used.



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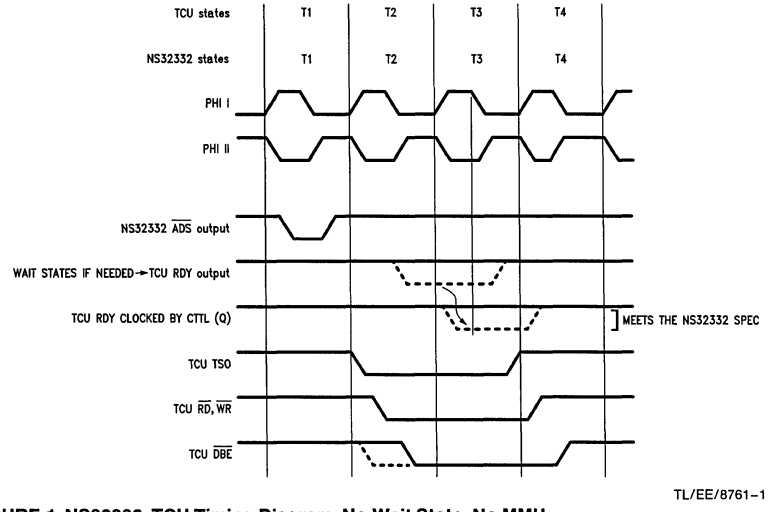

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FIGURE 1. NS32332, TCU Timing Diagram, No Wait State, No MMU

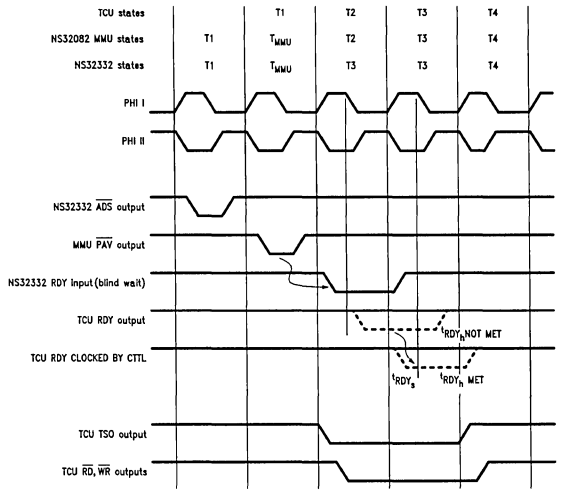

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FIGURE 2. NS32332, MMU, TCU Timing Diagram when NS32332 is Run with 1 Wait State Similar to Timing Diagram of NS32332 Adapter to DB32000

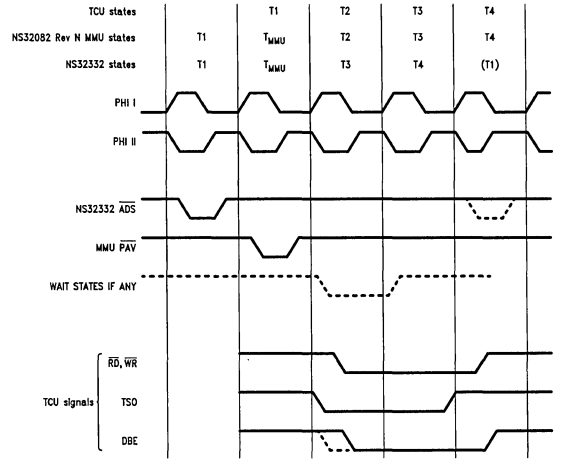

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FIGURE 3. NS32332, MMU, TCU Timing Diagram with No Wait State

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Interfacing the NS32081 as a Floating-Point Peripheral

National Semiconductor
Application Note 383
Microprocessor Applications
Engineering

This note is a guide for users who wish to interface the NS32081 Floating-Point Unit (FPU) as a peripheral unit to CPUs other than those of the Series 32000 family. This is not a particularly expensive procedure, but it requires some in-depth information not all of which is available in the NS32081 data sheet. Four basic topics will be covered here:

An overview of the architecture of the NS32081 as seen in a stand-alone environment.

The protocol used to sequence it through the execution of an instruction.

Special guidelines for connecting and programming the NS32081 as a peripheral component.

A sample application of these guidelines in the form of a circuit interfacing the NS32081 to the Motorola 68000 microprocessor.

References are made here to the NS32081 data sheet and the Series 32000 Instruction Set Reference Manual (Publication #420010099-001). The reader should have both these documents on hand.

1.0 Architecture Overview

1.1 REGISTER SET

The register set internal to the NS32081 FPU is shown in *Figure 1*. It consists of nine registers, each 32 bits in length:

FSR The Floating-Point Status Register. As given in the data sheet, this register holds status and mode information for the FPU. It is loaded by executing the LFSR instruction and examined using the SFSR instruction.

F0–F7 The Floating-Point Registers. Each can hold a single 32-bit single-precision floating-point value. To hold double-precision values, a register pair is referenced using the even-numbered register of the pair.

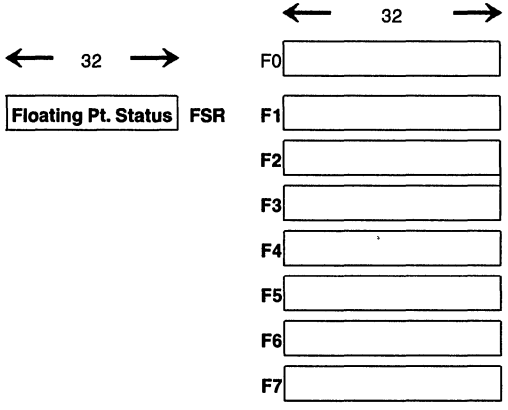


FIGURE 1. FPU Registers

Floating-point operands need not be held in registers; they may be supplied externally as part of the instruction sequence. Integer operands (appearing in conversion instructions) and values being transferred to or from the FSR must be supplied externally; they cannot be held in Floating-Point registers F0–F7.

1.2 INSTRUCTION SET AND ENCODING

The encodings used for NS32081 instructions are shown in *Figure 2*. They fall within two formats, labeled from Series 32000 tradition "Format 9" and "Format 11". These formats are distinguished by their least-significant byte (the "ID Byte"). Execution of an FPU instruction starts by passing first the ID Byte and then the rest of the instruction (the "Operation Word") to the FPU.

Fields within an instruction are interpreted by the FPU in the same manner as documented in Chapter 4 of the Series 32000 Instruction Set Reference Manual, with the exception of the 5-bit General Addressing Mode fields (*gen1, gen2*). Since the FPU does not itself perform memory accesses, it does not need to use these fields for addressing calculations. The only use it makes of these fields is to determine for each operand whether the value is to be found internal to the FPU (that is, within a register F0–F7, or whether it is to be transferred to and/or from the FPU. See *Figure 3*. A value of 0–7 in a *gen* field specifies one of the Floating-Point registers F0–F7, respectively, as the location of the corresponding operand. Any greater value specifies that the operand's location is external to the FPU and that its value will be transferred as part of the protocol. Any non-floating operand is always handled by the FPU as external, regardless of the addressing mode specified in its *gen* field. It is illegal to reference an odd-numbered register for a double-precision operand. If an odd register is referenced, the results are unpredictable.

1.3 PINOUT

The FPU is packaged in a 24-pin DIP (see *Figure 4*). The pin functions can be split into two groups: those that participate in the communication protocol between the FPU and the host system, and those that reflect the familiar requirements of LSI components.

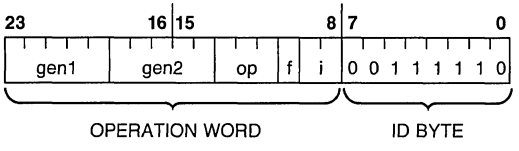
The protocol uses the following pins of the FPU:

D0–D15 The 16-bit data bus. The D0 pin holds the least-significant bit of data transferred on the bus.

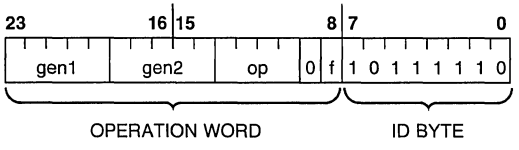
$\overline{SPC}$ A dual-purpose pin, low active. $\overline{SPC}$ is pulsed low from the host system as the data strobe for bus transfers. $\overline{SPC}$ is pulsed low by the FPU to signal that it has completed the internal execution phase of an instruction.

1.0 Architecture Overview (Continued)

ST0, ST1 The status code. This 2-bit value is sampled by the FPU on the falling edge of $\overline{SPC}$, and informs it of the current protocol phase. ST0 is the least-significant bit of the value. The need filled by the status code is most relevant to Series 32000-based systems, where it serves to allow retry of aborted instructions and to disambiguate the protocol when the $\overline{SPC}$ signal is bussed among multiple slave processors. In microprocessor-based peripheral applications, the status code can generally be provided from the CPU's address lines.



Format 9: LFSR/SFSR/Conversions



Format 11: Movement/Calculation

FIGURE 2. FPU Instruction Formats

The pins providing for standard requirements are:

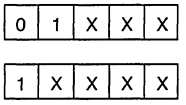
CLK The clock input. This is a TTL-level square wave which the FPU uses to sequence its internal calculations.

$\overline{RST}$ The reset input. This signal is used to reset the FPU's internal logic.

VCC The 5-volt positive supply.

GNDB, GNDL The grounding pins. GNDB serves as ground for the FPU's output buffers, and GNDL is used for the rest of the on-chip logic.

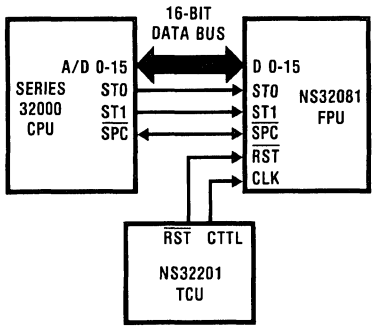
FPU Internal Register: Fn, n = 0 . . . 7
Long Floating = Even Register Only



External to FPU

Note: All non-floating operands are always external.

FIGURE 3. FPU Addressing Modes



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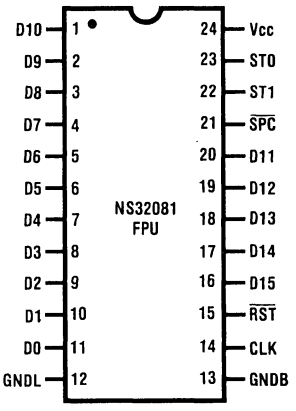

Top View

TL/EE/8388–2

FIGURE 4. NS32081 FPU Connections

2.0 Protocol

The FPU requires a fixed sequence of transfers ("protocol") in its communication with the outside world. Each step of the protocol is identified by a status code (asserted to the FPU on pins ST0 and ST1) and by its position in the sequence, as shown in *Figure 5*.

Status Combinations:
- 11: Write ID Byte
- 01: Transfer Operation/Operand
- 10: Read Status Word

Step	Status	Action
1	11	CPU sends ID Byte on least-significant byte of bus.
2	01	CPU sends Operation Word, bytes swapped on bus.
3	01	CPU sends required operands, *gen1* first, least-significant word first.
4	xx	FPU starts internal execution.
5	xx	FPU pulses $\overline{SPC}$ low.
6	10	CPU reads Status Word (Error/Comparison Result).
7	01	CPU reads result (if any), least-significant word first.

FIGURE 5. FPU Instruction Protocol

Steps 1 and 2 transfer the instruction to the FPU. Step 1 transfers the first byte of the instruction (the ID Byte) and Step 2 transfers the rest of the instruction (the Operation Word). In Step 2, the two bytes of the Operation Word must be swapped on the bus; i.e. the most-significant byte of the Operation Word must be presented on the least-significant byte of the bus.

Step 3 is optional and repeatable depending on the instruction. It is used to transfer to the FPU any external operands that are required by the instruction. The operand specified by *gen1* is sent first, least-significant word first, followed by the operand specified by *gen2*. If an operand is only one byte in length, it is transferred on the least-significant half of the bus.

The FPU initiates Step 4 of the protocol, internal computation, upon receiving the last external operand word or, if there are no external operands, upon receiving the Operation Word of the instruction. During this time, the data bus may be used for any purpose by the rest of the system, as long as the $\overline{SPC}$ pin is kept pulled up by a resistor and is not actively driven.

Step 5 occurs when the FPU completes the instruction. The FPU pulses the $\overline{SPC}$ pin low to acknowledge that it is ready to continue the protocol. This pulse is called the "Done pulse". The bus is not used during this step, and remains floating.

In Step 6, the FPU is polled by reading a Status Word. This word indicates whether an exception has been detected by the FPU. In the Compare instruction (CMPf), it also displays the relationship between the operands and serves as the result. This transfer is mandatory, regardless of whether the information presented by the FPU is intended to be used. See *Figure 3-6* of the data sheet.

Step 7 is, like Step 3, optional and repeatable depending on the instruction. Any external result of an instruction is read from the FPU in this step, least-significant word first. If the result is a 1-byte value, it is presented by the FPU on the least-significant half of the bus (D0–D7).

Note: If in Step 6 the FPU indicates that an error has occurred, it is permissible, though not necessary, to continue the protocol through Step 7. No guarantee is made regarding the validity of the value read, but continuing through Step 7 will not cause any protocol problems.

If at any time within the protocol another ID byte is sent (ST = 11), the FPU will prepare itself internally to execute another instruction, throwing away the instruction that was in progress. This is done to support the Abort with Retry feature of the Series 32000 family.

Because of this feature, however, there is an important consideration when using the FPU in systems that support multitasking: the operating system must not allow a task using the FPU to be interrupted in the middle of an instruction protocol and then transfer control to another task that is also using the FPU. The partially-executed instruction would be thrown away, leaving the first task with a garbage result when it continues. This situation can be avoided easily in software but, depending on the system, some cooperation may be required from the user program. Other solutions involving some additional hardware are also possible.

3.0 Interfacing Guidelines

There are some special interfacing considerations that are required (see *Figure 6*):

1. The edges of the $\overline{SPC}$ pulse must have a fixed relationship to the clock signal (CLK) presented to the FPU. When writing information to the FPU, the pulse must start shortly after a rising edge of CLK and end shortly after the next rising edge of CLK. Failing to do so can cause the FPU to fail, often by causing it to freeze and not generate the Done pulse. This synchronous generation of $\overline{SPC}$ is also important when reading information from the FPU, but the $\overline{SPC}$ pulse is allowed to be two clocks in width. These requirements will be expressed in future NS32081 data sheets as a minimum setup time requirement between each edge of the $\overline{SPC}$ pulse and the next rising edge of CLK, currently set at 40 nanoseconds on the basis of preliminary characterization. The propagation delay in generating $\overline{SPC}$ through a Schottky flip-flop (e.g. 74S74) and a low-power Schottky buffer (e.g. 74LS125A) is therefore acceptable at 10 MHz. LS technology is recommended for the buffer to minimize undershoot when driving $\overline{SPC}$.
2. After the FPU generates the Done pulse, it is necessary to leave the $\overline{SPC}$ pin high for an additional two cycles of CLK before performing the Read Status Word transfer.
3. After performing the Read Status Word transfer, it is necessary to wait for an additional three cycles of CLK before reading a result from the FPU.

4.0 An Interface to the MC68000 Microprocessor

4.1 HARDWARE

A block diagram of the circuitry required to interface the MC68000 MPU to the NS32081 is shown in *Figure 7*.

First the easy part. Direct connections are possible on the data bus, which is numbered compatibly (D0–D15 on both parts), the status pins ST0–ST1 (connected to address lines A4–A5 from the 68000), and the clock (CLK on both). The system reset signal ($\overline{\text{RESET}}$ to and/or from the MC68000) should be synchronized with the clock before presenting it as $\overline{\text{RST}}$ to the FPU.

All that remains to be done is to generate $\overline{\text{SPC}}$ pulses that are within specifications whenever the 68000 accesses the FPU, and to detect the Done pulse from the FPU in a manner that will allow the 68000 to poll for it.

The approach selected for generating $\overline{\text{SPC}}$ pulses uses an address decoder that recognizes two separate address spaces; one to transfer information to or from the FPU ($\overline{\text{XFER}}$), and one to poll for the Done pulse ($\overline{\text{POLL}}$).

The 68000 signals $\overline{\text{AS}}$ (Address Strobe) and R/$\overline{\text{W}}$ (Read / not Write) are used to generate $\overline{\text{SPC}}$ timing.

Figure 8 shows the timing generated when the 68000 is writing to the FPU. The $\overline{\text{SPC}}$ pin is kept floating (held high by a pullup resistor) until bus state S4, at which point it is pulled low. On the next rising edge of CLK, $\overline{\text{SPC}}$ is actively pulled high, and is set floating afterward. It is not simply allowed to float high, as the resulting rise time can be unacceptable at speeds above about 4 MHz. A timing chain, required due to the 10-MHz 68000's treatment of its $\overline{\text{AS}}$ strobe, generates the signals TA, TB and TC, from which the $\overline{\text{SPC}}$ signal's state and enable are controlled.

Figure 9 shows the $\overline{\text{SPC}}$ timing for reading from the FPU. The basic difference is that $\overline{\text{SPC}}$ remains active for two clocks, so that the FPU holds data on the bus until it is sampled by the 68000. Again, $\overline{\text{SPC}}$ is actively driven high before being released.

Note: Although $\overline{\text{SPC}}$ must be driven high before being released, it must not be actively driven for more than two clocks after the trailing edge of $\overline{\text{SPC}}$. This is because the FPU can respond as quickly as three clocks after that edge with a Done pulse.

A simpler scheme in which the $\overline{\text{SPC}}$ pulse is identical for both reading and writing (1-clock wide always, but starting ½ clock later with CLK into the FPU inverted) was considered, but was rejected because the data hold time presented by the 68000 on a Write cycle would be inadequate at 10 MHz.

Any $\overline{\text{SPC}}$ pulse appearing while the $\overline{\text{XFER}}$ Select signal is inactive is interpreted as a Done pulse, which is latched in a flip-flop within the Done Detector block. When the 68000 performs a Read cycle from the address that generates the $\overline{\text{POLL}}$ select signal, the contents of the flip-flop are placed on data bus bit D15. Since this is the sign bit of a 16-bit value, the 68000 can perform a fast test of the bit using a MOVE.W instruction and a conditional branch (BPL) to wait for the FPU.

The schematic for the $\overline{\text{SPC}}$ generator and the Done pulse detector is given in *Figures 10a* and *10b*. The flip-flop labeled SPC generates the edges of the $\overline{\text{SPC}}$ pulse (on the signal $\overline{\text{SPCT}}$). The timing chain (TA, TB) provides the enable control to the buffer driving $\overline{\text{SPC}}$ to the FPU, as well as the signal to terminate the $\overline{\text{SPC}}$ pulse (either TB or TC, depending on the direction of the data transfer). Note that the timing chain assumes a full-speed memory cycle of four clocks in accessing the FPU, and will fail otherwise. The circuit generating the Data Acknowledge signal to the 68000 (DTACK, not shown) must guarantee this. In any system that must use a longer access, some modification to the timing chain will be necessary.

The flip-flop labeled DONE (*Figure 10b*) is the Done pulse detector. It is cleared by performing a data transfer into the FPU and is set by a Done pulse on $\overline{\text{SPC}}$. A buffer, enabled by the $\overline{\text{POLL}}$ select signal, connects its output to data bus bit 15.

4.2 SOFTWARE

Some notes on programming the FPU in a 68000 environment:

1. The byte addressing convention in the 68000 differs from that of the Series 32000 family. In particular, a byte with an even address is transferred on the most-significant half of the bus by the 68000, but the FPU expects to see it on the least-significant byte. When transferring a single byte to or from the FPU, either do so with an odd address specified, or transfer the byte as the least-significant half of a 16-bit value at an even address.
2. The 68000 transfers 32-bit operands by sending the most-significant 16 bits first. The FPU expects values to be transferred in the opposite order. Make certain that operands are transferred in the correct order (the 68000 SWAP instruction can be helpful for this).

A sample program that sequences the FPU through the execution of an ADDF instruction is listed in *Figure 11*. As this example is intended for clarity rather than efficiency, improvements are possible. The $\overline{\text{XFER}}$ select is assumed to be generated by addresses of the form 06xxxx (hex) and the $\overline{\text{POLL}}$ select is assumed to be generated by addresses of the form 07xxxx.

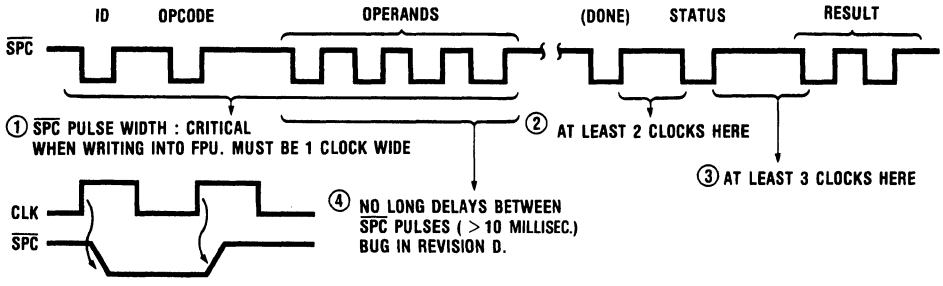

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FIGURE 6. Interfacing to FPU: Cautions

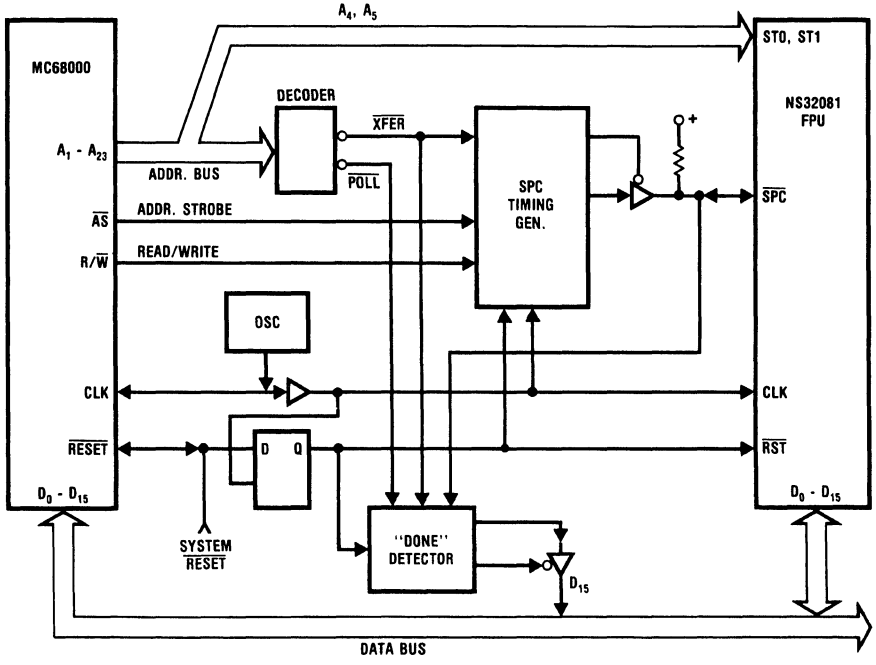

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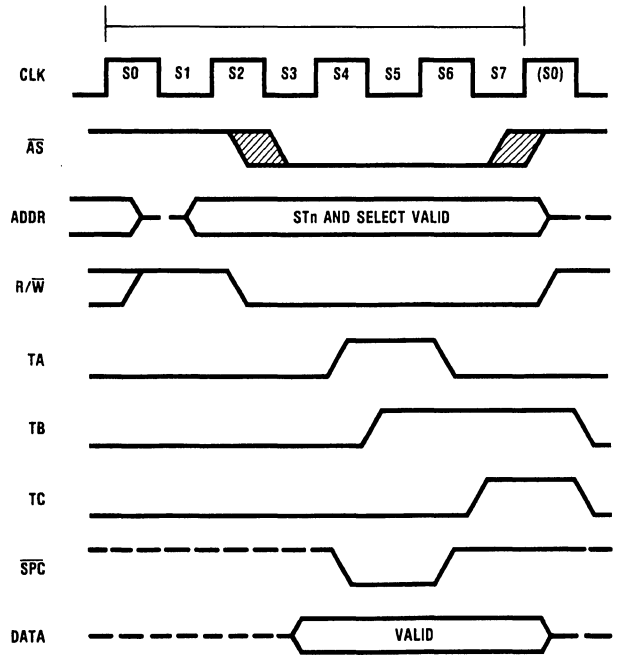
FIGURE 7. 68000-32081 Interface Block Diagram



TL/EE/8388-5

FIGURE 8. 68000 Write to FPU

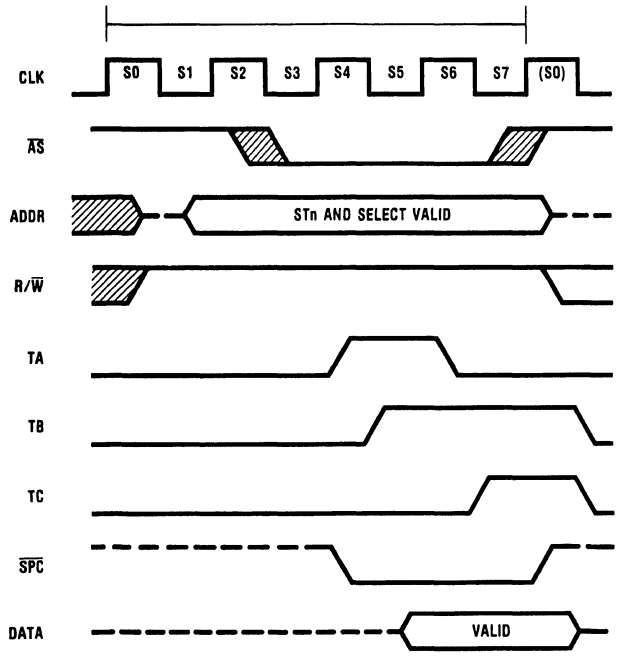


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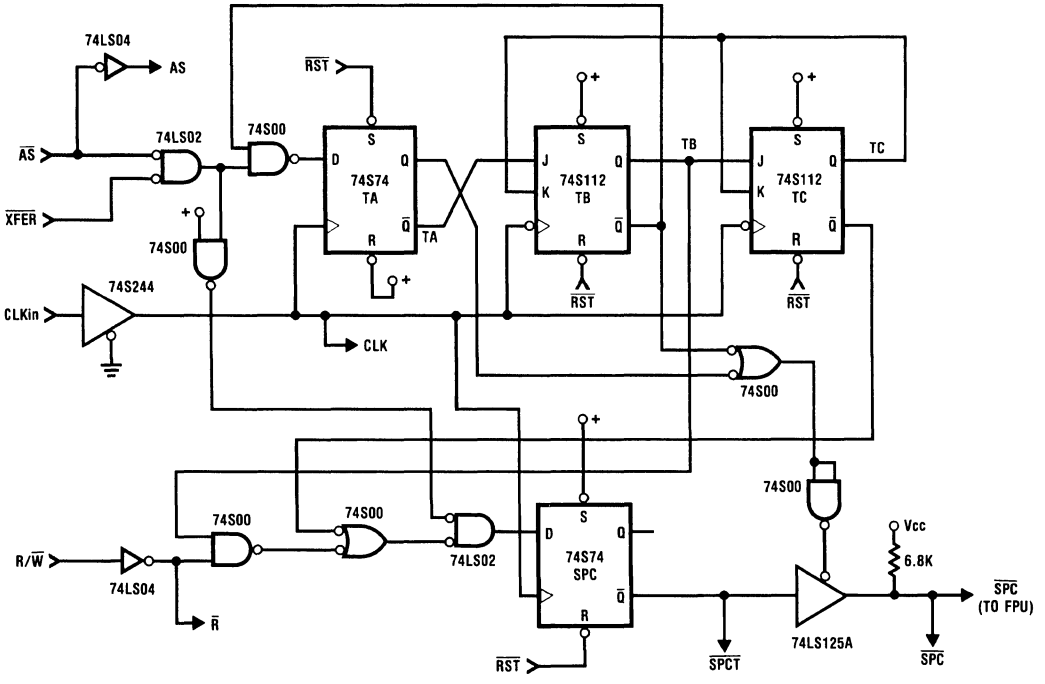
FIGURE 9. 68000 Read from FPU



TL/EE/8388-7

FIGURE 10a. Schematic: $\overline{SPC}$ Timing Generator

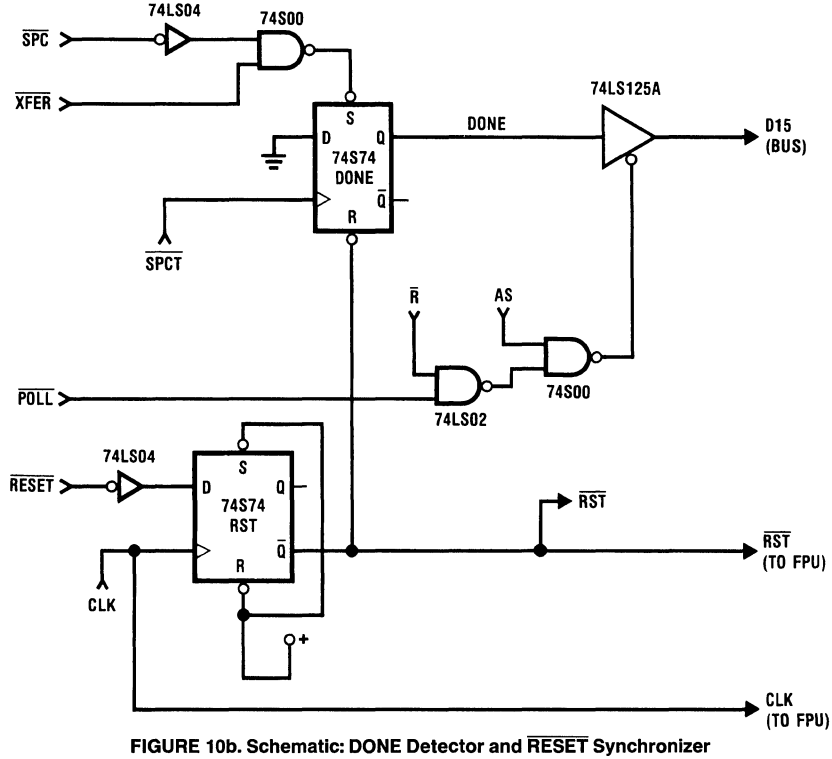


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FIGURE 10b. Schematic: DONE Detector and $\overline{RESET}$ Synchronizer

```
*     Register Contents:
*
*     A0 = 00070000     Address of DONE flip-flop.
*     A1 = 00060010     Address for ST=1 transfer (Transfer Operand).
*     A2 = 00060020     Address for ST=2 transfer (Read Status Word).
*     A3 = 00060030     Address for ST=3 transfer (Broadcast ID).
*
*     D0 = 000000BE     ID byte for ADDF instruction.
*     D1 = 00000184     Operation Word for ADDF. (Note bytes swapped.)
*     D2 = 3F800000     First operand = 1.0.
*     D3 = 3F800000     Second operand = 1.0.
*     D4                Receives Status Word from FPU.
*     D5                Receives result from FPU.
*     D7                Scratch register (for DONE bit test).
*
START MOVE.W  D0,(A3)         Send ID byte.
      MOVE.W  D1,(A1)         Send Operation Word.
      SWAP    D2              Send operands. The swapping
      MOVE.L  D2,(A1)          is included because the
      SWAP    D2               FPU expects the least-
      SWAP    D3               significant word first.
      MOVE.L  D3,(A1)          (Can be avoided, with care.)
      SWAP    D3
*
POLL  MOVE.W  (A0),D7         Check the DONE flip-flop,
      BPL     POLL             loop until FPU is finished.
*                              (DONE bit is sign bit, tested
*                              by the MOVE instruction.)
*
      MOVE.W  (A2),D4         Read Status Word.
      MOVE.L  (A1),D5         Read result.
      SWAP    D5              Swap halves of result.
```

FIGURE 11. Single-Precision Addition (Demo Routine)

10 MHz, No Wait States NS32016 System

National Semiconductor
Application Note 404
Microprocessor Applications
Engineering

INTRODUCTION

Recent microprocessor applications such as high resolution graphics, multiuser workstations, data communication, industrial automation, etc. have placed growing demands on microprocessor throughputs. Higher throughputs, together with increasing complexity of microprocessor systems, require slave support in addition to high speed, powerful microprocessors.

The Series 32000® Microprocessor family serves the needs of high end microprocessor applications. The NS32016 Central Processing Unit (CPU) has a powerful register and instruction set. The NS32082 Memory Management Unit (MMU) and the NS32081 Floating-Point Unit (FPU) function as slave processors for the CPU. All the chips in the family run at 10 MHz. Together, the chips provide the throughput required by high end microprocessor applications. This application note discusses the design considerations for building a 10 MHz NS32016 system with no wait states.

Series 32000 Chip Set:

The NS32016 system described here, uses the Series 32000 chip set consisting of:

1. The NS32016 Central Processing Unit (CPU)
2. The NS32082 Memory Management Unit (MMU)
3. The NS32081 Floating-Point Unit (FPU)
4. The NS32201 Timing Control Unit (TCU)
5. The NS32202 Interrupt Control Unit (ICU)

Details of the five chips are provided in the Series 32000 Data Book. *Figure 1* illustrates the interconnections of a simple NS32016 based system capable of running at 10 MHz without wait states. As shown in *Figure 1*, the CPU, MMU and FPU are interconnected on a multiplexed Address/Data Bus. The TCU provides the clocks and the control signals required by the system. The multiplexed bus is separated into Data and Address buses by using bidirectional Data bus drivers and fall-through Address latches. The ICU, being a peripheral, is interfaced to the demultiplexed Address and Data buses. The ICU Status input (ST1) is driven by a logical combination of ST1 from the CPU and address line A5. This allows the CPU to read both the INTA and RETI vectors from the SVCT register of the ICU.

DESIGN CONSIDERATIONS

The design of a 10 MHz Microprocessor system with no wait states requires system memory to run at comparable speeds. Typically, system memory consists of Read Only Memory (ROM) and Read/Write or Random Access Memory (RAM). A 10 MHz, NS32016-based system functioning without wait states requires careful memory timing consideration.

A read cycle without wait states requires data from memory to be valid prior to the falling edge of the PHI2 clock during the T3 state of the CPU. This allows about 155 nanoseconds following the leading edge of the read strobe for data to be stable. In a memory write cycle, the data is available to the memory for about 215 nanoseconds following the leading edge of the write strobe. It is assumed that the Address lines are valid at the memory pins at the time the read or write strobe goes active.

SRAM INTERFACE:

With high speed, 8K × 8-bit Static RAMs (SRAMs) such as the NMC6264s, which have a 120-nanosecond maximum access time, an interface without wait states is feasible. Besides requiring no wait states, SRAMs do not require the refresh circuitry that Dynamic RAMs (DRAMs) need. Neither do they require the error checking and correcting circuitry that DRAMs need for correcting soft errors. The timing diagrams for SRAM Read and Write cycles with the MMU are illustrated in *Figures 4* and *5* respectively. The SRAMs are organized into even and odd banks. The Write Enable ($\overline{WE}$) signals for the SRAMs are generated by logically combining address line A0 and $\overline{HBE}$ with the $\overline{WR}$ signal from the TCU. Both even and odd SRAM banks are always enabled during Read cycles.

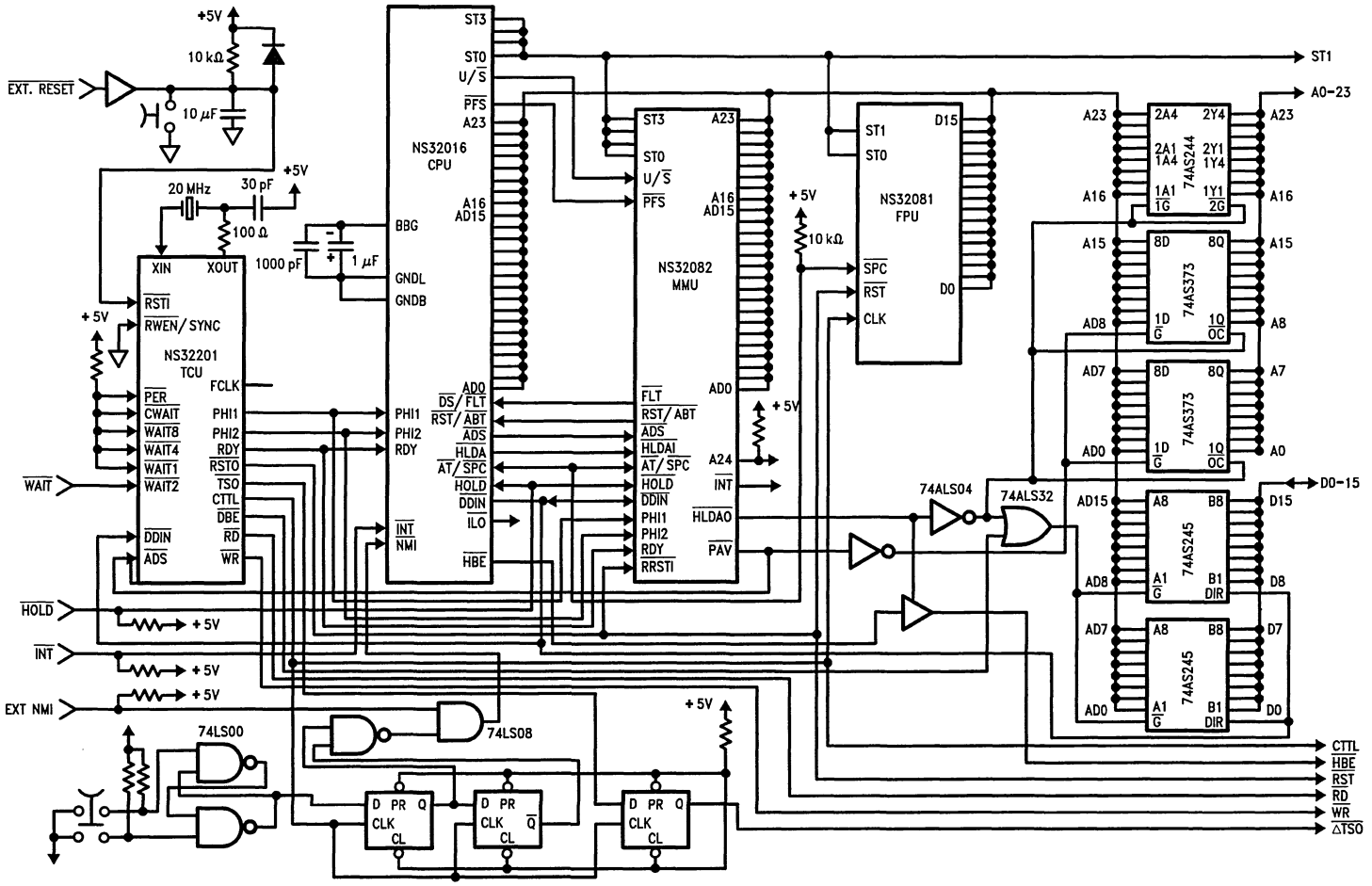
EPROM INTERFACE:

With current technology, EPROMs up to 64-Kbyte densities are available. In particular, the 27128 type EPROMs are available with 150-nanosecond maximum access times. These EPROMs can be used in the NS32016-based system without wait states. The timing diagram for the EPROM Read cycle, with the MMU is illustrated in *Figure 3*. The Output Enable ($\overline{OE}$) inputs to the EPROMs are connected to the $\overline{RD}$ signal. This will cause both even and odd bytes of the set of EPROMs to be enabled for a byte or word read from the CPU. This does not affect the data as the CPU will read the appropriate byte(s). A single DMPAL16L8A device is used to generate all the required chip select signals.

I/O INTERFACE:

CPU accesses to the serial communications devices require the insertion of at least two wait states. This is accomplished by activating the TCU $\overline{WAIT2}$ input during such accesses.

Furthermore, the leading edges of the Read and Write strobes are delayed by one clock cycle. This is necessary since the time delays of the Read and Write strobes from Address Valid, required by the communications devices, are larger than the delays provided by the 32000 chip set during normal bus accesses. The system uses two NS16450s. This facilitates its use in stand-alone, stand-aside or transparent configuration. The two NS16450s have their oscillator pins (XTAL1 and XTAL2) connected to the crystal circuit as illustrated in *Figure 1*. The two NS16450s are interfaced to standard RS232C communication ports with jumpers. The jumpers allow the configuration of either port as a data-terminal or as a data-set.



TL/EE/8506–7

FIGURE 1. Circuit Diagram for the 10 MHz No Wait States NS32016 Based System

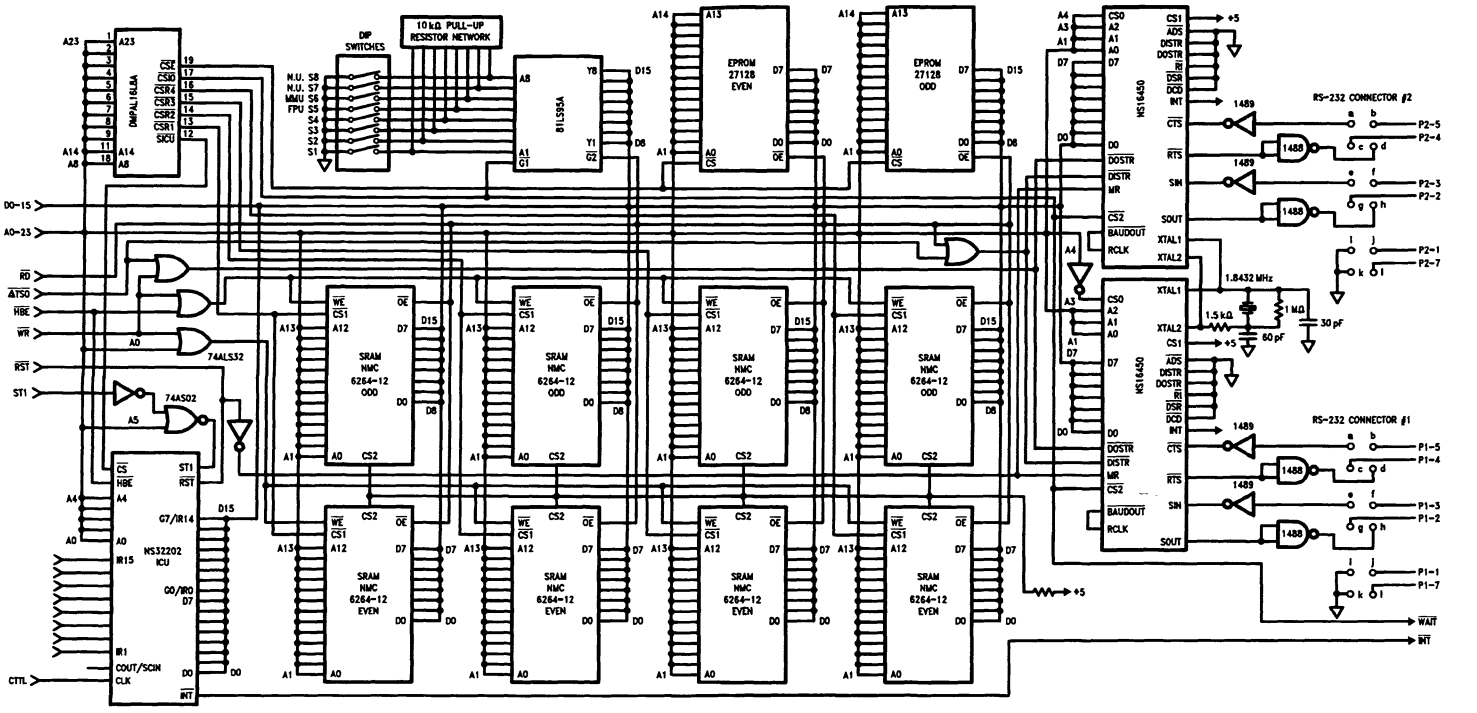


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FIGURE 1. Circuit Diagram for the 10 MHz No Wait States NS32016 Based System (Continued)

One port can be used to communicate with a host computer. The other can be used to interface the system to a terminal. If MON16 software is used, it is possible to communicate from the terminal to a host computer such as a National Semiconductor SYS/32™ or a VAX™. Files stored in the host can be down-loaded into the NS32016-based system memory and executed at 10 MHz without wait states.

The Non-Maskable Interrupt signal ($\overline{NMI}$) is used to return from "runaway" programs to the monitor without destroying the contents of the Program Counter and Processor Status Register. The circuit shown in *Figure 1* provides an $\overline{NMI}$ pulse signal to the CPU.

```
PAL16L8A
Part #
Chip Select Generation
National Semiconductor
A23 A22 A21 A20 A19 A18 A17 A16 A15 GND
A14 SICU CSR1 CSR2 CSR3 CSR4 CSIO A8 CSE VCC
/CSE = /A23 * /A22 * /A21 * /A20 * /A19 * /A18 * /A17 * /A16 * /A15
/CSR1 = /A23 * /A22 * /A21 * /A20 * /A19 * /A18 * /A17 * /A16 * A15 * /A14
/CSR2 = /A23 * /A22 * /A21 * /A20 * /A19 * /A18 * /A17 * /A16 * A15 * A14
/CSR3 = /A23 * /A22 * /A21 * /A20 * /A19 * /A18 * /A17 * A16 * /A15 * /A14
/CSR4 = /A23 * /A22 * /A21 * /A20 * /A19 * /A18 * /A17 * A16 * /A15 * A14
/CSIO = A23 * A22 * A21 * A20 * A19 * A18 * A17 * A16 * A15 * /A14
/SICU = A23 * A22 * A21 * A20 * A19 * A18 * A17 * A16 * A15 * A14 * /A8
```

FIGURE 2. PAL Equations in PALASM™ Format

CONFIGURATION SWITCHES:

Dip switches have been used in the circuit for system configuration as illustrated in *Figure 1*. The CPU reads them at power-on or system reset to set the baud rate of the I/O ports and the CPU configuration register. Switches S1, S2, S3 and S4 set the baud rate. Table I lists the various baud rates possible with MON16 software. Switch S5 indicates the presence of an FPU in the system and S6 indicates the presence of an MMU in the system (Table II).

TABLE I

S4	S3	S2	S1	Baud Rate
ON	ON	ON	ON	19200
ON	ON	ON	OFF	9600
ON	ON	OFF	ON	7200
ON	ON	OFF	OFF	4800
ON	OFF	ON	ON	3600
ON	OFF	ON	OFF	2400
ON	OFF	OFF	ON	2000
ON	OFF	OFF	OFF	1800
OFF	ON	ON	ON	1200
OFF	ON	ON	OFF	600
OFF	ON	OFF	ON	300
OFF	ON	OFF	OFF	150
OFF	OFF	ON	ON	134
OFF	OFF	ON	OFF	110
OFF	OFF	OFF	ON	75
OFF	OFF	OFF	OFF	50

TABLE II

S6	S5	Slave Processors
ON	ON	MMU and FPU
ON	OFF	MMU
OFF	ON	FPU
OFF	OFF	neither

RS232C JUMPER CONNECTIONS:

If a particular port in the system is to be connected to a terminal, the associated jumpers need to be configured for a Data Set. With reference to *Figure 1*, the jumper connections for a Data Set configuration are as follows:

a–c, b–d, e–g, f–h, i–j, k–l.

If the port is to be connected to a host computer, the associated jumpers need to be configured for a Data Terminal. The jumper connections for a Data Terminal configuration are as follows:

a–b, c–d, e–f, g–h, i–j, k–l.

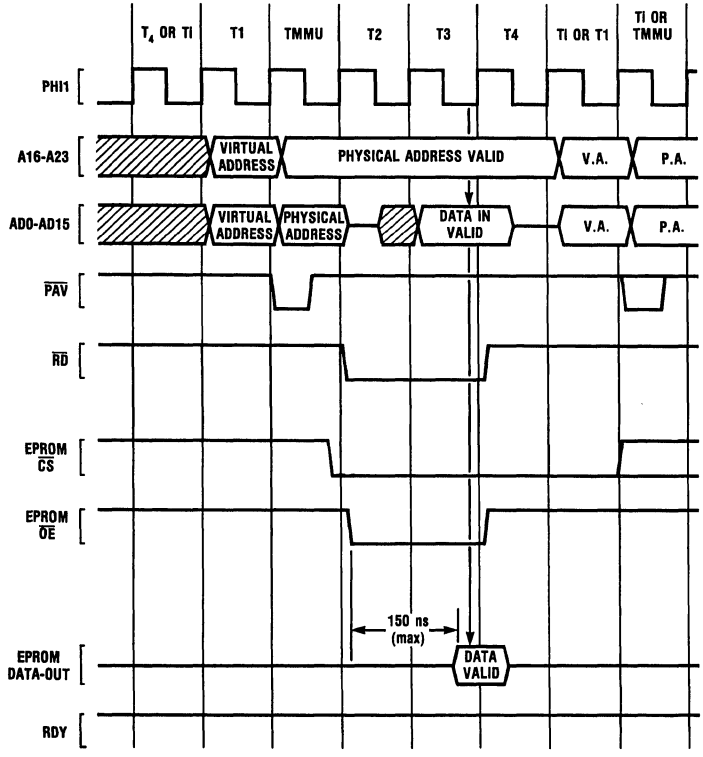
Note: a–b => connect node 'a' to node 'b'.

MEMORY MAP

The memory map of the system described in this note is slightly different from the memory map of the DB32016 CPU board. This has been done to simplify the chip-select generation logic. This requires minor changes to some 'equate' statements in the MON16 modules in addition to the I/O drivers changes to support the NS16450s instead of the 8251s. *Figure 2* shows the PAL equations. The memory map is shown in Table III.

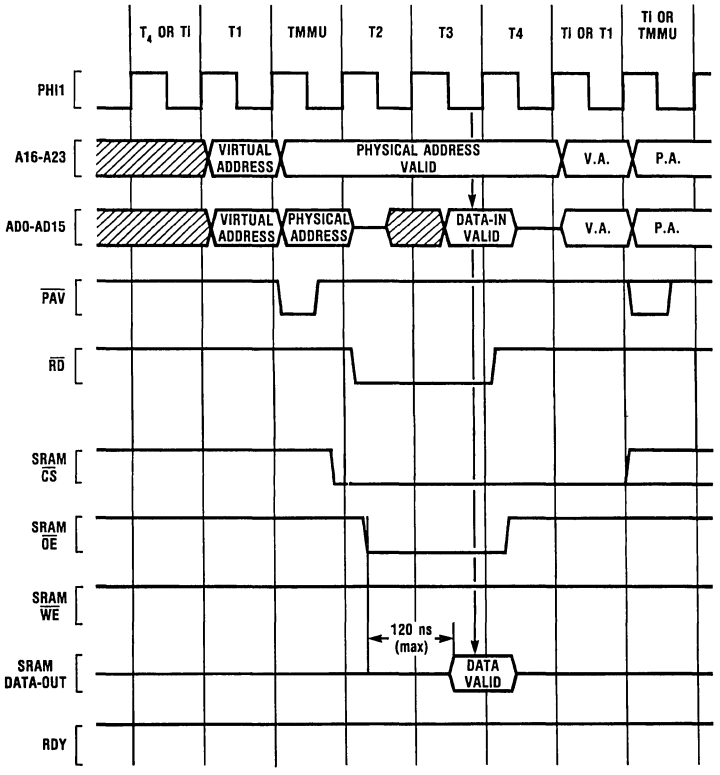
TABLE III

Devices	Memory Locations
EPROMs	$000000-$007FFF
SRAMs	$008000-$017FFF
Serial Port 1	$FF8000-$FF800F
Serial Port 2	$FF8010-$FF801F
ICU-Registers	$FFFE00-$FFFE3F
CNFG Switches	$FF8003



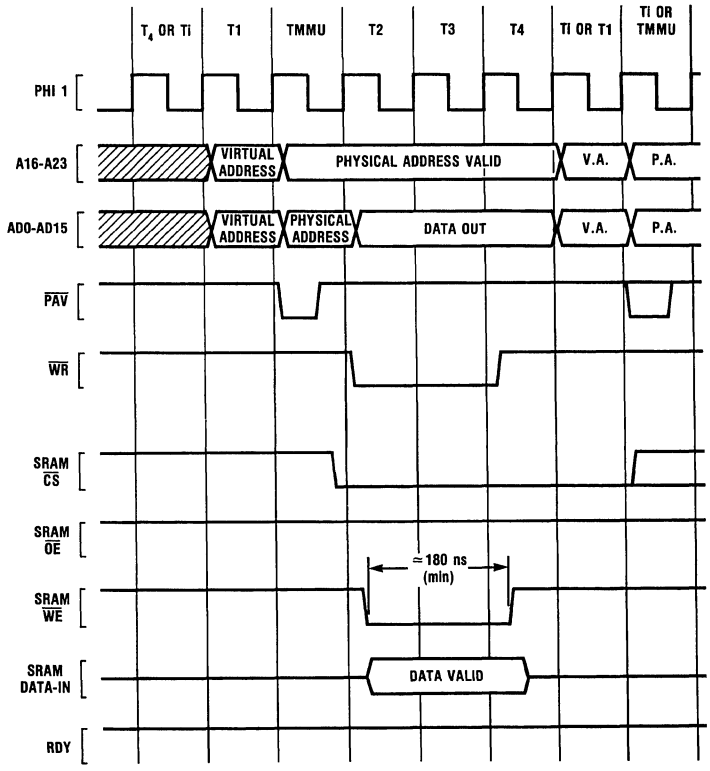
TL/EE/8506–3

FIGURE 3. Memory-Managed EPROM Read Cycle



TL/EE/8506–4

FIGURE 4. Memory-Managed SRAM Read Cycle



TL/EE/8506–5

FIGURE 5. Memory-Managed SRAM Write Cycle

Notes:

1. In all memory and I/O cycles, if the MMU is not used, then the T_{mmu} cycle is absent. See *Figures 3, 4* and *5*. This will not change the memory or I/O cycle requirements. The $\overline{PAV}$ signal will be replaced by the $\overline{ADS}$ signal which is strobed by the CPU in the T1 cycle.

2. The chip selects for the ICU internal registers and the Configuration latch have been partially decoded in order to reduce the chip count for the system.

DECOUPLING CAPACITOR REQUIREMENTS:

Line to ground noise on the system can be eliminated by using decoupling capacitors. For the Series 32000 chip set, the decoupling capacitor details are given in the Series 32000 Data Book. For the random logic used in the system, a 0.1 μF ceramic capacitor for each bipolar TTL device is recommended. For MOS devices, a 0.1 μF ceramic capacitor for every row of four to five devices may be used. At the power input to the system, a 100 μF tantalum capacitor in parallel with a 0.1 μF ceramic capacitor may be used.

PORTING MON16:

The changes made to MON16 to run on this system are in modules MONINT.ASM and MONSUB.ASM. All changes appear in lower-case letters in the listing. The code pertaining to the ICU counters in MON16 has been removed as it is not used.

```
;          MONINT**************************
;   USART CONSTANTS
;
iobeg:    .equ    @h'ff8000               ;IO start address
usrtl:    .equ    @h'ff8000               ;UART0
usrtcsl: .equ    @h'ff800a               ;UART0 line status register
usrt2:    .equ    @h'ff8010               ;UART1
usrtcs2: .equ    @h'ff801a               ;UART1 line status register
datap:    .equ    0                       ;UARTs rev/trans buffer registers
out_rdy:.equ    5                       ;UARTs tx_rdy bit of the LSR reg.
in_rdy: .equ    0                       ;UARTs rx_rdy bit of the LSR reg.
switchp: .equ    @h'ff8003               ;Dip switches port address




;
;   RESET ROUTINE




;
;     init UARTs
;
          save    [r2, r3, r4, r5]
          addr    usrtl, r4
          addr    usrt2, r5
          movb    h'80, 6 (r4)
          movb    h'80, 6 (r5)
;set UARTs baud rate
;         movzbd switchp, r2              ;load switch for baud rate
;         andb    h'0f, r2
;         movb    acetb:w[r2:w],0(r4)     ;set UART0 baud rate
;         movb    acetb+1:w[r2:w],2 (r4)
;         movb    acetb:w[r2:w],0(r5)     ;set UART1 baud rate
;         movb    acetb+1:w[r2:w],2 (r5)
;***for debugging only***
          movb    h'0c,0 (r4)             ;set UART0 to 9600 baud
          movb    h'0,2 (r4)
          movb    h'18,0 (r5)             ;set UART1 to 4800 baud
          movb    h'0,2 (r5)
;************************
          movb    h'3,6 (r4)              ;set LCR of the UARTs
          movb    h'3,6 (r5)
          movb    h'0f,8 (r4)
          movb    h'0f,8 (r5)
          movb    0 (r4), r3
          movb    0 (r5), r3
          restore[r2,r3,r4,r5]
```

Note: Version 2.00 of MON16 has been used for the NS32016 system.

```
;
;the divisor values for UARTs with crystal frequency of 1.8432 MHz
;
acetb:  .word 6,12,16,24                ;19200, 9600, 7200, 4800
        .word 32,48,58,64               ;3600, 2400, 2000, 1800
        .word 96,192,384,768            ;1200, 600, 300, 150
        .word 857,1047,1536,2304        ;134.5, 110, 75, 50
;
        MOVD   H'1B10000,SVMSR          ;INIT SVMSR SET TU BEN UB FT UT
        MOVD   H'90000,MNMSR            ;MONITOR MSR: = TU,A0
        movb   switchp,r1               ;GET MMU & FPU BITS FROM SWITCHES
        COMB   R1,R1                    ;CONVERT TO CFG BYTE
        ANDB   SW__MMU+SW__FPU, R1
        ASHB   -3,R1
        MOVZBD CFGN,R2                  ;PREPARE CALL TP GET__PUT
        MOVB   PUTI,TOS
        MOVQD  0,TOS                    ;GET__PUT (GET,0,CFG);
        CXP    GETPUT
        TBITB  CNFMMU,CONFIG            ;IF MMU THEN
        BFC    RST14:B
        LMR    MSR,MNMSR                ; LOAD MSR;
RST14:  CXP    MAINLP                   ;TYPE RESET MESSAGE




;
        .MODULE MONSUB**********
;
;       USART  CONSTANTS
;
iobeg:  .equ   @h'ff8000        ;IO start address
usrt1:  .equ   @h'ff8000        ;UART0
usrtcs1:.equ   @h'ff800a        ;UART0 line status register
usrt2:  .equ   @h'ff8010        ;UART1
usrtcs2:.equ   @h'ff801a        ;UART1 line status register
datap:  .equ   0
out__rdy:.equ  5
in__rdy: .equ  0
usrtoff: .equ  h'a              ;line status reg offset from buffer reg
;
```

```
;
;    R D C H R      ( DUMMY READ CHAR PROCEDURE )
;
;
RDCHR:   .PROC                    ; PROCEDURE RDCHR (WAIT,TRM)
RD_CHR: .BLKB                     ; PROCEDURE VALUE
RD_WAIT:.BLKB                     ; WAIT/NOWAIT FLAG
RD_TRM: .BLKB                     ; TERMINAL NUMBER
         .RETURNS
         .BLKW                    ; RETURN CHR,CHR_RDY FLAG
         .VAR   [R1,R2]
         .BEGIN
         addr   usrt1,r1          ; R1: ADDRESS OF TRMINAL A
         CMPQB  TRMA,RD_TRM       ; IF TRMINAL_NUM < > 0 THEN
         BEQ    RDCHRLP:B
         addr   usrt2,r1          ; R1: ADDRESS OF TRMINAL B
RDCHRLP:                          ; DO WHILE IN_RDY=0 AND RD_WAIT=TRUE
         tbitb  in_rdy,usrtoff(r1)       ;   INPUT IN_RDY
         BFS    RDCHR3:B
;        BR     RDCHR3:B          ; *** FOR DEBUG ONLY ***
         CMPQB  TRUE,RD_WAIT
         BEQ    RDCHRLP           ; END;
         BR     RDCHREX:B
RDCHR3:  MOVB   0(R1),RD_CHR ; RDCHR;=USART DATA
         MOVQB  TRUE,RD_WAIT      ; RD_WAIT:=TRUE
RDCHREX:
         .ENDPROC




;
;        P R C H R      ( PRINT CHARACTER )
;
;        FUNCTION — SEND ONE CHARACTER TO TERMINAL
;
;        CALLING SEQUENCE PRCHR(ENDF,WAIT,CHR,TRM)
;
;         ENDF/WAIT
;                BOOLEANO  IN/OUT ON INPUT FLAGE WAIT TO END OF OPERATION
;                                 OR REURN
;                                 ON OUTPUT INDICATES END OF OPERATION
;        CHR  — CHARACTER INPUT CHARACTER TO BE PRINTED
;        TRM  — INTEGER   INPUT TERMINAL NUMBER
;
PRCHR:   .PROC
WAIT_PR:.BLKB                     ; WAIT : BOOLEAN
CHR PR: .BLKB                     ; ASCII CHR
```

```
TRM_CHR:.BLKB                   ; TERMINAL NUMBER
        .RETURNS
        .BLKB                   ; OUTPUT WAIT WAIT:BOOLEAN
        .VAR    [R1,R2]
        .BEGIN
        addr    usrt1,r1        ;R1: ADDRESS OF TERMINAL A
        CMPQB   TRMA,TRM_CHR    ;IF TERMINAL_NUM<>0 THEN
        BEQ     PRCHRLP:B
        addr    usrt2,r1        R1: ADDRESS OF TERMINAL B
PRCHRLP:
        tbitb   out_rdy,usrtoff(r1) ;IF TX-RDY = 0
        BFS     PRCHR3:B        ;THEN
;       BR      PRCHR3:B            ;***DEBUG ONLY***
        CMPQB   FALSE,WAIT_PR   ; IF WAIT THEN REPEAT
        BNE     PRCHRLP
        BR      PRCHREX:B           ; ELSE WAIT:=FALSE
PRCHR3: MOVB    CHR_PR,0 (R1)
        MOVQB   TRUE,WAIT_PR    ;ELSE WRITE (DATA-PORT, CHR)
```

CONCLUSION

This application note describes a method of designing a 10-MHz, no-wait-state NS32016-based system with off-the-shelf memory and I/O chips. The system has a powerful instruction set, suitable for high level language compilers. With available cross-support software (NSX16™) and firmware (MON16), the NS32016 system can be used to communicate with a host computer such as a SYS/32. Programs can be written in high level languages such as C on the SYS/32. These programs can then be compiled and assembled to be down-loaded into the NS32016-based system memory to be executed.

Using Dynamic RAM With Series 32000® CPUs

National Semiconductor
Application Note 405
Microprocessor Applications
Engineering

Recent advances in semiconductor technology have led to high-density, high-speed, low-cost dynamic random access memories (DRAMs), making large high-performance memory systems practical. DRAMs have complex timing and refresh requirements that can be met in different ways, depending on the size, speed, and processor interface requirements of the memory being designed. For low or intermediate performance, off-the-shelf components like the DP8419 can be used with a small amount of random logic. For higher performance, specialized high-speed circuitry must be designed

This application note presents the results of a timing analysis, and describes a DRAM interface for the NS32016 optimized for speed, simplicity and cost.

A future application note will discuss such features as error detection and correction, scrubbing, page mode and/or nibble mode support, in conjunction with future CPUs, such as the NS32332.

TIMING ANALYSIS RESULTS

Figures 1 and *2* show the number of CPU wait states required during a DRAM access cycle, for different CPU clock frequencies and DRAM access times.

Figure 1 is related to a DRAM interface using the DP8419 DRAM controller. Descriptions of the circuitry for use with the DP8419 and related timing diagrams are omitted. See the "DP8400 Memory Interface Family Applications" book for details.

Figure 2 shows the same data for a DRAM interface using standard TTL components, specially designed for the NS32016.

The special-purpose interface requires fewer wait states than the DP8419-based interface, especially at high frequencies.

These results assume a minimum amount of buffering between DRAM and CPU.

The results do not apply when CPU and DRAM reside on different circuit boards communicating through the system bus, since extra wait states may be required to provide for synchronization operations and extra levels of buffering.

INTERFACE DESCRIPTION

The DRAM interface presented here has been optimized for overall access time, while requiring moderate speed DRAMs, given the CPU clock frequency.

This may be significant when a relatively large DRAM array must be designed since a substantial saving can be achieved.

The result of these considerations has been the design of a high-speed DRAM interface capable of working with a CPU clock frequency of up to 15-MHz and 100-nsec DRAM chips, without wait states.

The only assumption has been that the DRAM array is directly accessible through the CPU local bus.

RAM Access Time in nsec	CPU Wait States Required							
250	0	1	1	1	1	2		
200	0	0	1	1	1	1	2	2
150	0	0	0	0	1	1	1	1
120	0	0	0	0	0	1	1	1
100	0	0	0	0	0	0	1	1
	6	7	8	9	10	11	12	13

CPU Clock Frequency in MHz

FIGURE 1. Memory Speed vs. CPU Wait States When Using the DP8419 DRAM Controller

RAM Access Time in nsec	CPU Wait States Required									
250	0	0	1	1	1	1				
200	0	0	0	0	1	1	1	1		
150	0	0	0	0	0	0	1	1	1	1
120	0	0	0	0	0	0	0	0	1	1
100	0	0	0	0	0	0	0	0	0	0
	6	7	8	9	10	11	12	13	14	15

CPU Clock Frequency in MHz

FIGURE 2. Memory Speed vs. CPU Wait States When Using Random Logic

This configuration presents some speed advantages; for example, the amount of buffering interposed between CPU and DRAM array is minimal. This translates into shorter propagation delays for address, data and other relevant signals.

Another advantage is that the interface can work in complete synchronization with the CPU. This significantly improves performance since no time is spent for synchronization. Reliability also improves since the possibility of metastable states in synchronizing flip-flops is eliminated.

A block diagram of the DRAM interface is shown in *Figure 3*. *Figures 4* through *7* show circuit diagrams and timing diagrams.

Interface operation details follow.

$\overline{\text{RAS}}$ AND $\overline{\text{CAS}}$ GENERATION

This is the most critical part of the entire interface circuit. To avoid wait states during a CPU read cycle, the DRAM must provide the data before the falling edge of clock phase PH12 during state T3. This requires that the $\overline{\text{RAS}}$ signal be generated early in the CPU bus cycle to meet the DRAM access time. On the other hand, the $\overline{\text{RAS}}$ signal can be asserted only after the row address is valid and the $\overline{\text{RAS}}$ precharge time from a previous CPU access or refresh cycle has elapsed.

The interface circuit shown in *Figures 4* and *5* relies on two advanced clock signals obtained from CTTL through a delay line and some standard TTL gates.

The advanced clock signals, CTTLA and $\overline{\text{CTTLB}}$, are used to clock the circuit that arbitrates between CPU access requests and refresh requests. The $\overline{\text{CTTLB}}$ signal is also used to enable an advanced $\overline{\text{RAS}}$ generation circuit, which causes the $\overline{\text{RAS}}$ signal to be asserted earlier than the CPU access-grant signal from the arbitration circuit. This speeds up the $\overline{\text{RAS}}$ signal by about 10 ns by avoiding the time required by the arbitration circuit to change state.

A different delay line is used to generate the $\overline{\text{CAS}}$ signal and to switch the multiplexers for the column addresses. Note that the $\overline{\text{CAS}}$ signal during write cycles is delayed until the beginning of CPU state T3, to guarantee that the data being written to the DRAM is valid at the time $\overline{\text{CAS}}$ is asserted. The $\overline{\text{CAS}}$ signal is deasserted after the trailing edge of $\overline{\text{RAS}}$ to guarantee the minimum pulse width requirement.

The timing diagrams in *Figures 6* and *7* show the signal sequences for both read and write cycles.

ADDRESS MULTIPLEXING

The multiplexing of the various addresses for the DRAM chips is accomplished via four 74AS153 multiplexer chips in addition to some standard TTL gates used to multiplex the top two address bits needed for 256k DRAMs. The resulting nine address lines are then buffered and sent to the DRAMs through series damping resistors. The function of these resistors is to minimize ringing.

REFRESH

The refresh circuitry includes an address counter, a timer and a number of flip-flops used to generate the refresh cycle and to latch the refresh request until the end of the refresh cycle.

The address counter is an 8-bit counter implemented by cascading the two 4-bit counters of a 74LS393 chip. This counter provides up to 256 refresh addresses and is incremented at the end of each refresh cycle.

The refresh timer is responsible for generating the refresh request signal whenever a refresh cycle is needed. This timer is implemented by cascading two 4-bit counters. Both counters are clocked by the $\overline{\text{CTTLB}}$ signal; the first is a presettable binary counter that divides the clock signal by a specified value; the second can be either a BCD or a binary counter depending on the CPU clock frequency.

With this arrangement, a refresh request is generated after a fixed time interval from the previous request, regardless of the CPU activity. A more sophisticated circuit that generates requests when the CPU is idle could also be implemented. However, such a circuit has not been considered here because the performance degradation due to the refresh is relatively small (less than 3.3 percent), and the improvement attainable by using a more sophisticated circuit would not justify the extra hardware required.

CONCLUSIONS

The DRAM interface described in this application uses two TTL-buffered delay lines to obtain speed advantages. One delay line is used to time the $\overline{\text{CAS}}$ signal and to enable the column address. The other is used to generate the advanced clock signals from CTTL.

Below 10 MHz, the advanced clocks might not be required, and the related delay line can be eliminated. When this is done, however, higher speed DRAMs must be used. If, on the other hand, advanced clocks must be used for frequencies lower than 10 MHz, a delay line with a larger delay (e.g. DDU-7J-100) might be needed.

Delay lines are extremely versatile for this kind of application due to their accuracy and the fact that different delays are easily available to accommodate different DRAM types.

The savings attainable by using slower DRAM chips, in addition to the reliability improvement and cleaner design, make delay lines a valid alternative, even though their cost is relatively high in comparison to standard TTL gates.

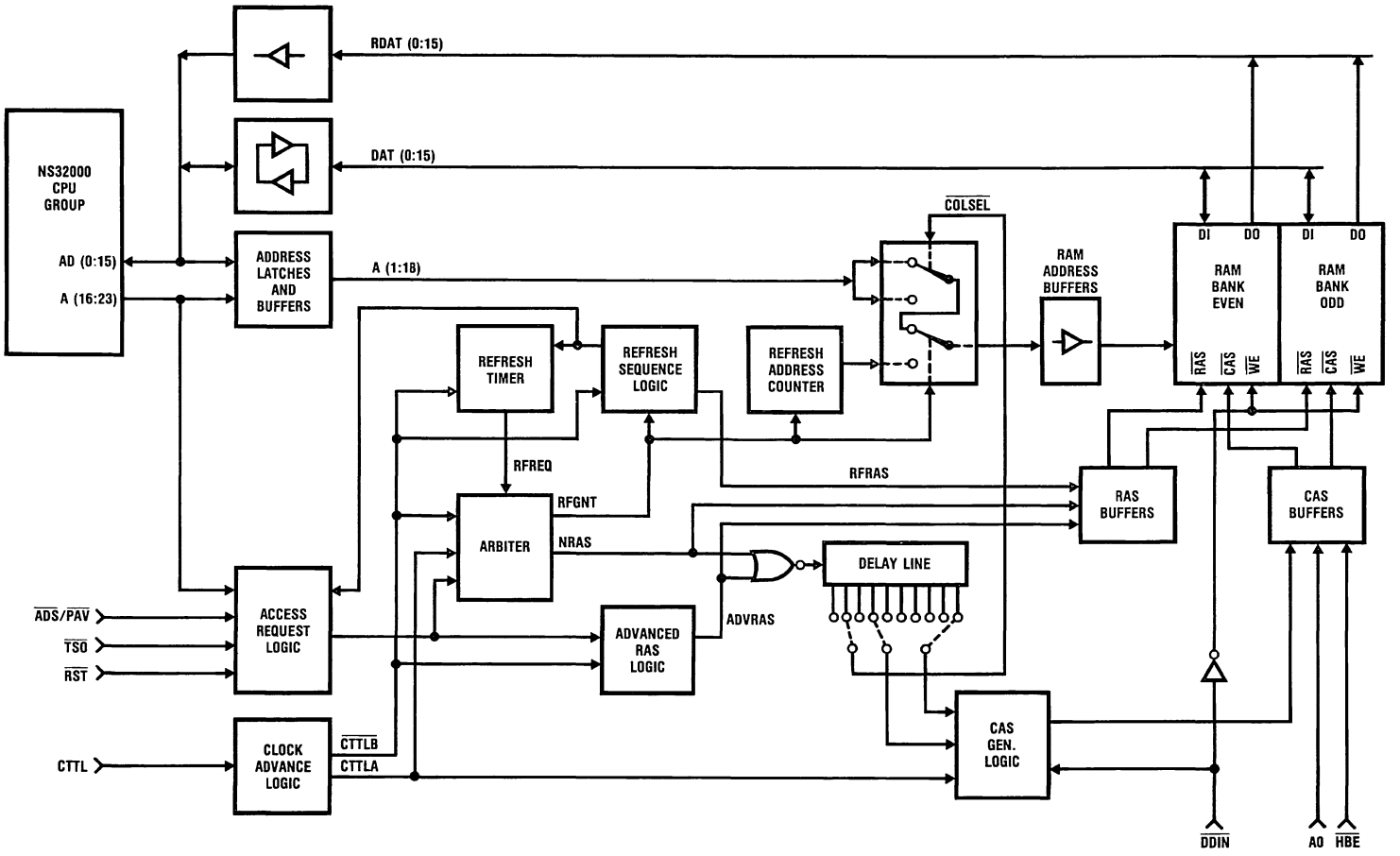
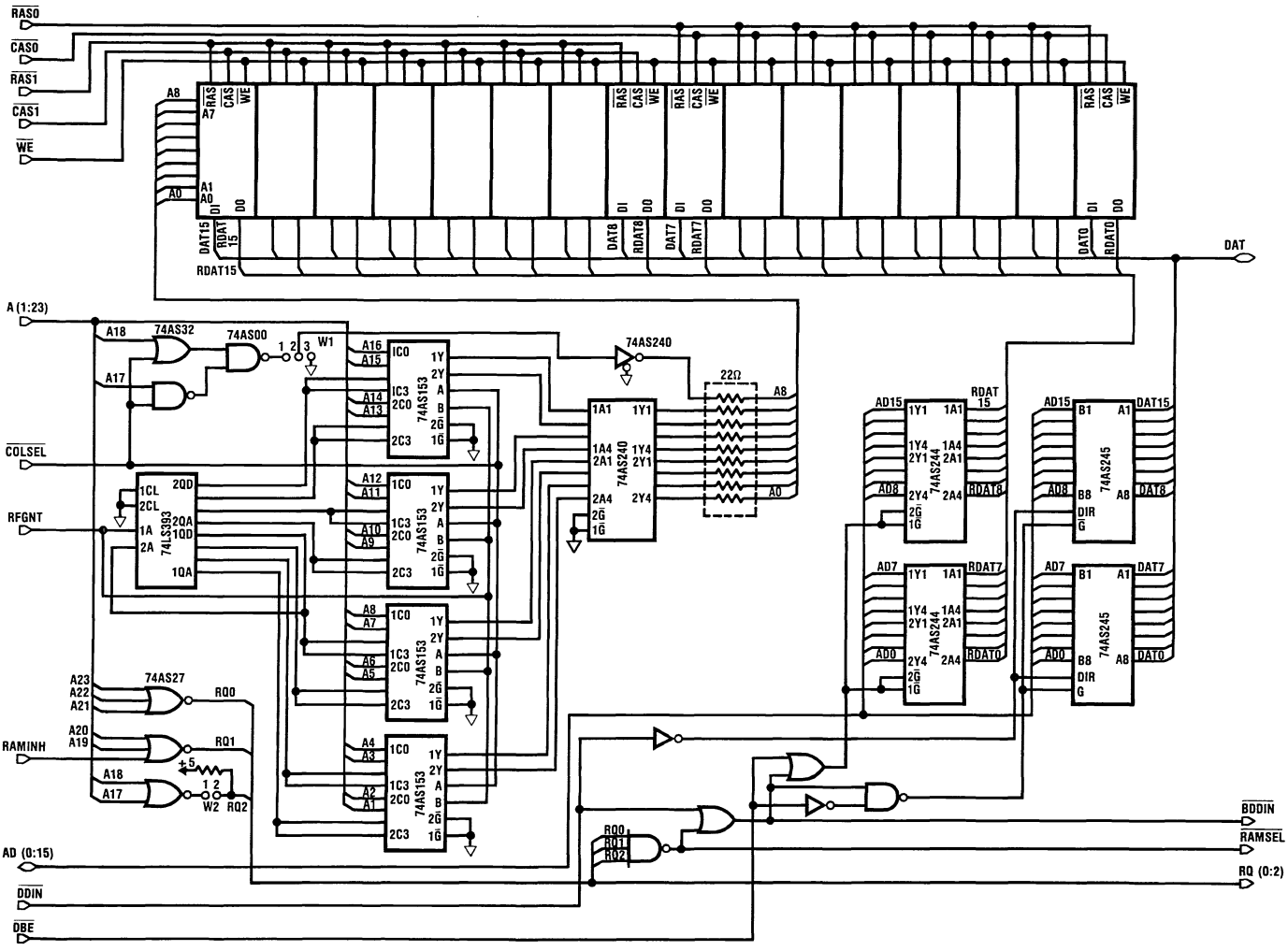


FIGURE 3. DRAM Interface Block Diagram



TL/EE/8517–2

FIGURE 4. DRAM Interface Circuit Diagram (a)

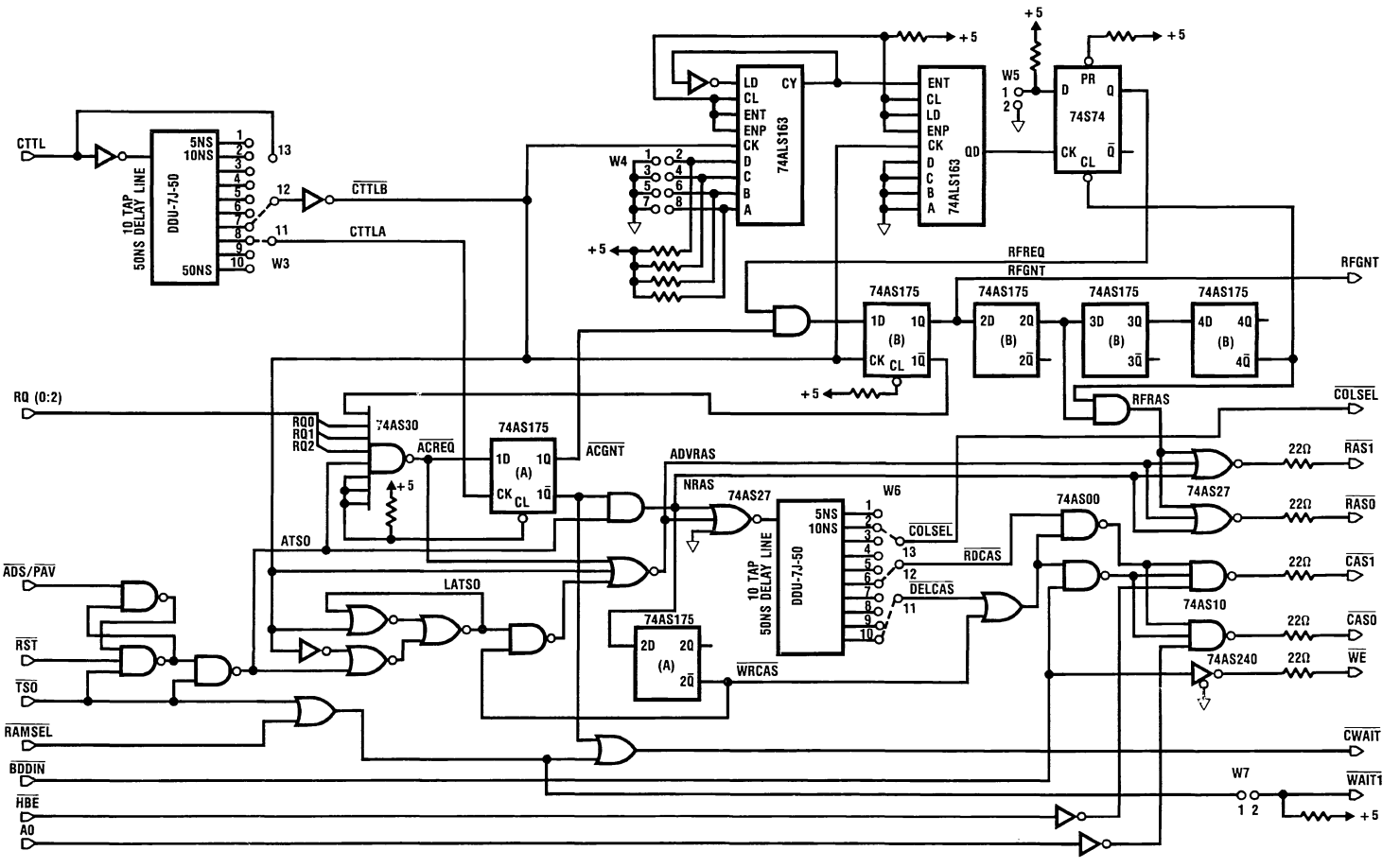
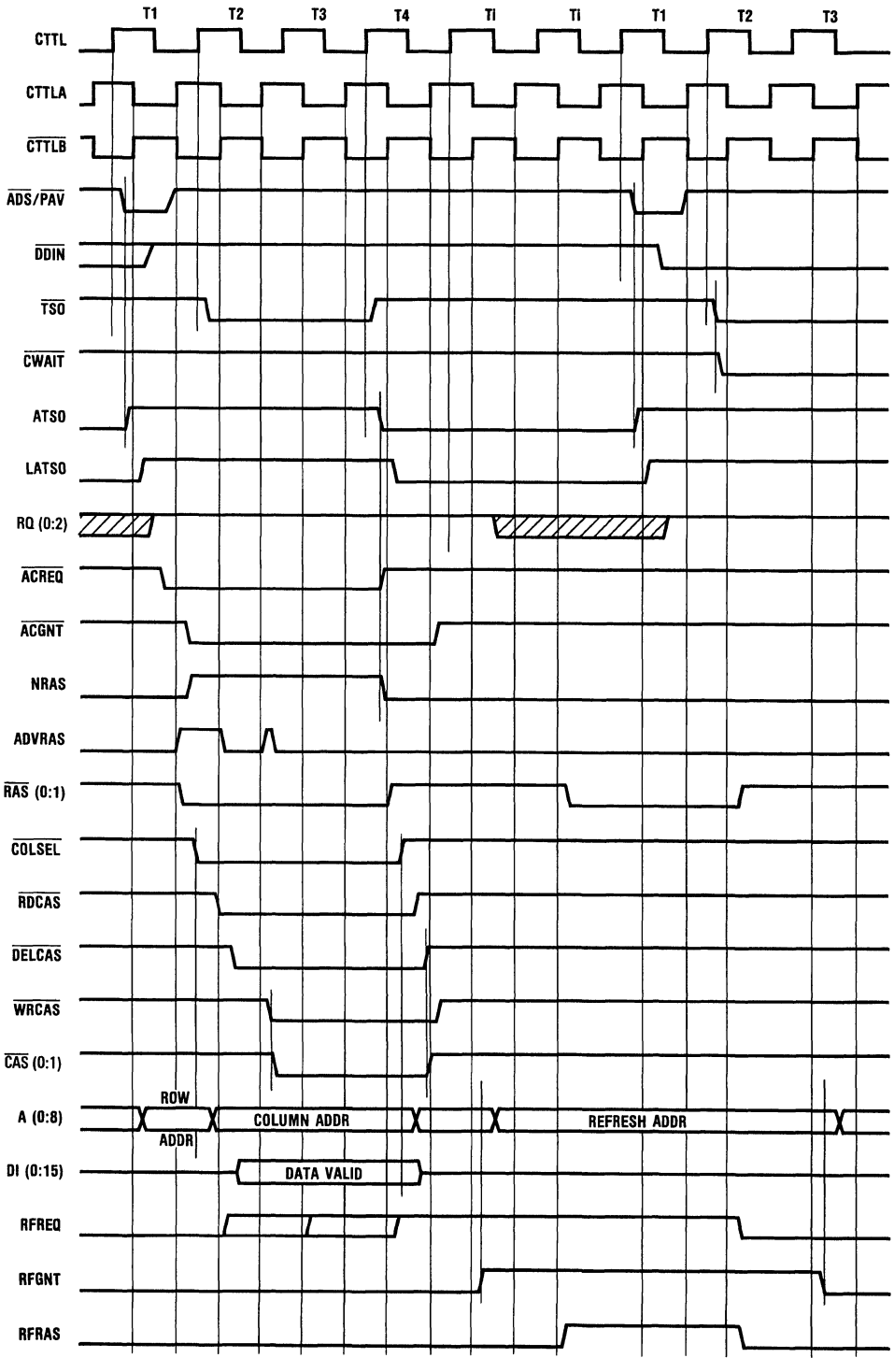
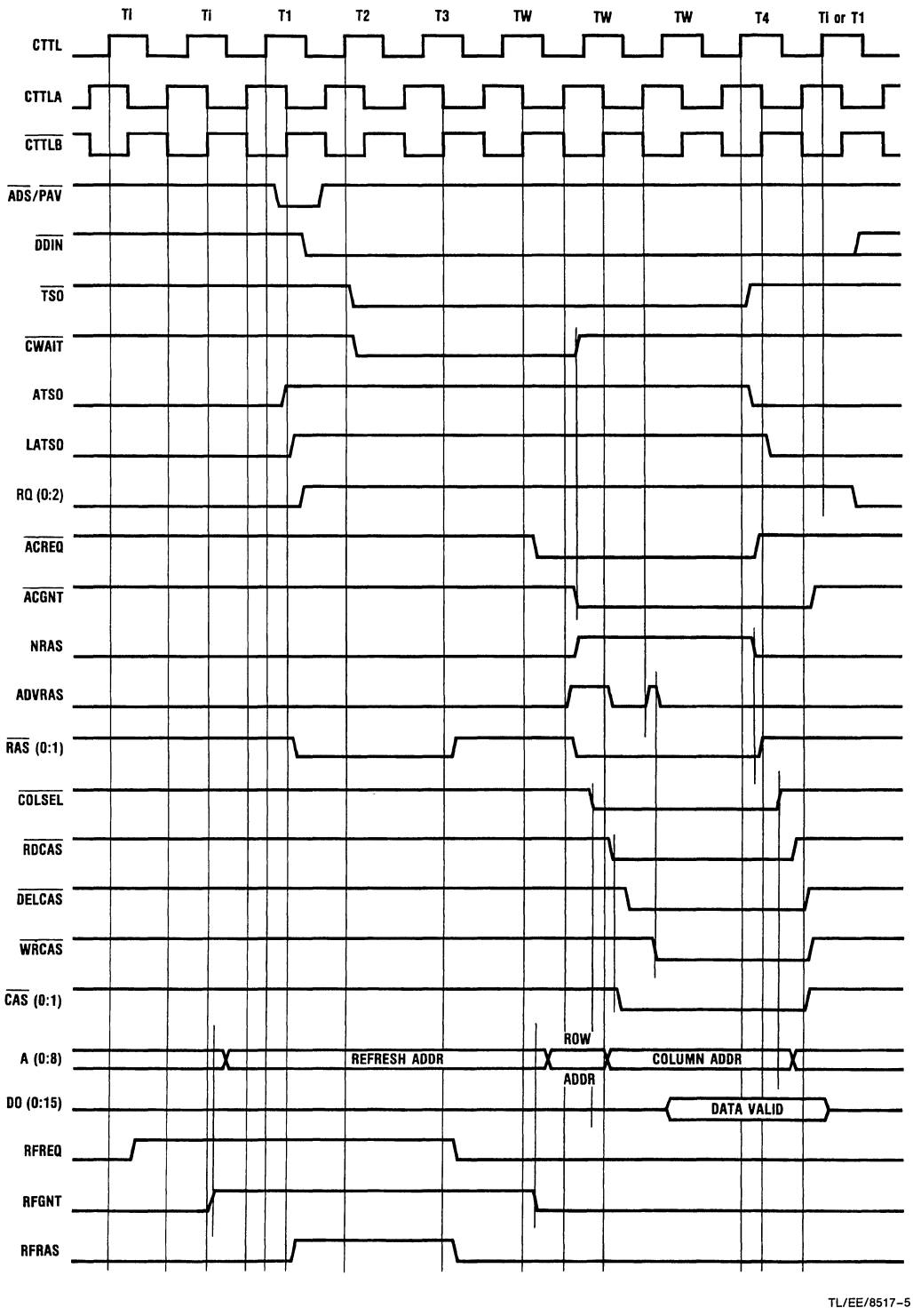


FIGURE 5. DRAM Interface Circuit Diagram (b)



TL/EE/8517–4

FIGURE 6. Write Cycle Followed By a Refresh Cycle



TL/EE/8517–5

FIGURE 7. Refresh Cycle Followed By a Read Cycle

Interfacing the Series 32000® CPUs to the MULTIBUS®

National Semiconductor
Application Note 406
Microprocessor Applications
Engineering

One of the key elements in a computer system is the system bus which holds all the hardware components together. The bus contains the necessary signals to allow the hardware components to interact with each other. Memory and I/O transfers, system interrupts, etc., can all be handled by the system bus.

A variety of alternatives is available to the designer whenever an interface to a particular bus is to be designed. For example, for a low performance CPU, interface performance might not be of prime concern. In this case, the use of a standard LSI device implementing the interface functions might be recommended. If, on the other hand, a high performance CPU is being used and the performance of the interface is critical to overall system performance, a better approach might be to design special circuitry using standard TTL logic in conjunction with high speed PAL®s or gate-arrays. This application note presents an implementation of the arbitration section of a MULTIBUS interface, specially designed for the Series 32000 CPUs.

CIRCUIT DESCRIPTION

The MULTIBUS arbitration circuitry described here uses a high-speed PAL and some standard TTL logic to implement the arbiter state machine and other control functions. This solution, in addition to speed advantages, also provides a higher degree of flexibility as opposed to one which relies on LSI devices.

A detailed circuit diagram of this arbitration circuitry and the arbiter state diagram are shown in *Figures 1* and *2*.

Figure 3 shows a timing diagram of a bus acquisition and release sequence. In this case a higher priority master was in control of the bus and a lower priority master issued a bus request during the current master bus transfer cycle.

As the state diagram shows, the arbiter uses a nonrelease philosophy, called "Parking." In this scheme, once the bus is acquired, it will not be released at the end of the access cycle unless the force-release signal $\overline{\text{FREL}}$ is low or a bus request has been issued by another master. The latter condition is detected by monitoring the bus lines $\overline{\text{BPRN}}$ and $\overline{\text{CBRQ}}$. A bus release sequence is started as soon as $\overline{\text{CBRQ}}$ is asserted low or $\overline{\text{BPRN}}$ goes high. The arbiter enters state S3 and asserts the end-cycle detection enable signal $\overline{\text{ECDEC}}$ to allow appropriate logic to detect the end of the current MULTIBUS transfer cycle from the on-board CPU. When the end-cycle condition is detected, further MULTIBUS accesses from the on-board CPU are inhibited, and the signal ECYC is asserted to notify the arbiter that the bus can be released. Note that if an interlocked operation is in progress, the end-cycle condition occurs at the end of the last cycle of the interlocked operation rather than at the end of the current cycle.

This interlocked mechanism for the bus release is necessary to guarantee proper operation of the arbitration circuitry, regardless of the bus clock and CPU clock frequencies.

The nonrelease philosophy is very effective in that it can save the bus exchange overhead for the current master when no other master is requesting the bus. An increase in reliability also results, since the number of synchronization operations required for bus arbitrations is minimized.

In this application, particular care has been taken for the bus interlock. This is important, especially if a dual-port memory is used, since hardware deadlocks could result if interlocked cycles are not handled properly.

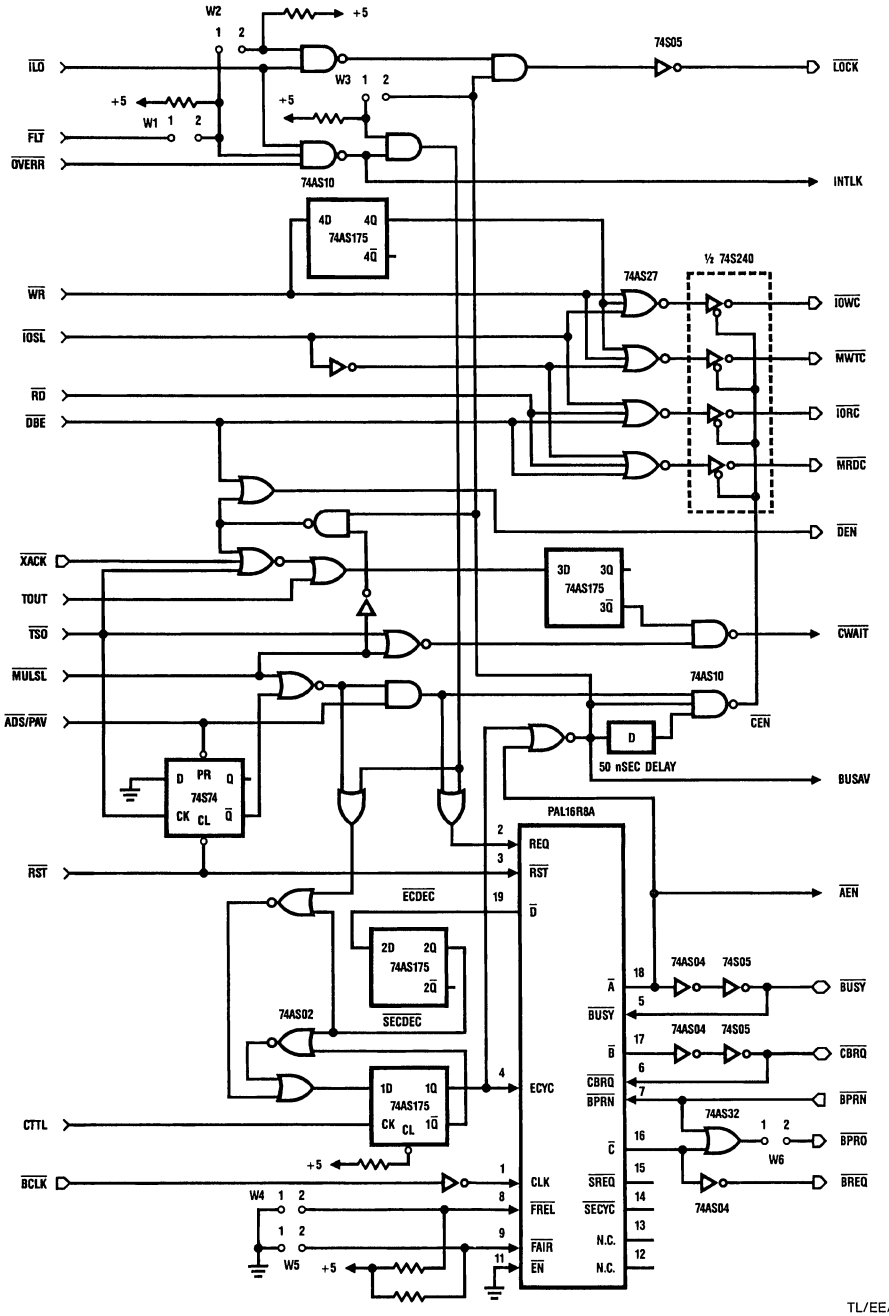
Consider the case of interlocked operations involving multiple access cycles, with the first access directed to the dual-port memory and some or all of the subsequent accesses directed to the system memory. This could happen, for example, when the MMU cycles are interlocked, the first-level page table resides in the dual-port memory, and some shared second-level page tables are kept either in the system memory or in the dual-port memory of another master. In this case, if the dual-port memory control logic grants an interlocked access to the MMU (thus setting a locking mechanism to prevent accesses from external masters until the end of the interlocked operation), and in the meantime the bus is acquired by an external master trying to access the dual-port memory, a hardware deadlock will result. This is because the dual-port memory is not unlocked until the MMU accesses the system memory to complete its operation, while the MULTIBUS is not released by the external master until the dual-port memory access is granted.

This problem can be solved by requesting the bus at the beginning of the interlocked operation, even though the interlocked cycle is not directed to the system memory, and delaying the first interlocked access to the dual-port memory until the bus has been acquired.

Another relevant point is the generation of the MULTIBUS read and write signals. These are derived from the TCU signals $\overline{\text{RD}}$ and $\overline{\text{WR}}$. The leading edges of these signals are delayed to meet the MULTIBUS timing requirements. The MULTIBUS read signals $\overline{\text{MRTC}}$ and $\overline{\text{IORC}}$ are delayed until the $\overline{\text{DBE}}$ signal becomes active, since only the address set-up time requirement must be met. A larger delay is needed instead, for the MULTIBUS write signals $\overline{\text{MWTC}}$ and $\overline{\text{IOWC}}$ to meet the data set-up time requirement. Note that the delay line serves this purpose only during the first bus access immediately following an arbitration sequence.

SIGNALS DESCRIPTION

Details on most signals used in the MULTIBUS arbitration circuitry can be found in the appropriate MULTIBUS specification manuals and Series 32000 data sheets. A description of those signals not found in these documents follows.



TL/EE/8518–1

FIGURE 1. 32000 MULTIBUS Interface Circuit Diagram

Bus Override ($\overline{\text{OVERR}}$): This signal is from an override flip-flop and can be used to hold the bus during burst transfers. The maximum duration for this signal to be asserted must not exceed the shortest time-out setting in the system. Note that the signal $\overline{\text{LOCK}}$ is not activated when the bus is overridden by the signal $\overline{\text{OVERR}}$. This is because the $\overline{\text{LOCK}}$ signal can only be asserted for a maximum of 12 microseconds, while the bus can be overridden for several milliseconds, depending upon the system requirements.

IO Select ($\overline{\text{IOSL}}$): This signal is generated by the address decoder and is asserted when the MULTIBUS I/O space is accessed.

MULTIBUS Select ($\overline{\text{MULSL}}$): $\overline{\text{MULSL}}$ is from the address decoder and is asserted when a MULTIBUS memory or I/O access is requested.

Time-Out (TOUT): This signal is generated by a fail-safe timer and is used to terminate the cycle if a bus grant, a peripheral, or memory acknowledge is not generated within a certain period of time.

Address Buffers Enable ($\overline{\text{AEN}}$): When $\overline{\text{AEN}}$ is active, the MULTIBUS address buffers are enabled.

Data Buffers Enable ($\overline{\text{DEN}}$): When $\overline{\text{DEN}}$ is active, the MULTIBUS data buffers are enabled.

Interlocked Cycle (INTLK): Active high. This signal, when active, indicates that an interlocked cycle either is being started or is in progress. INTLK is used by the dual-port memory control logic to control interlocked accesses.

Bus Available (BUSAV): This signal is used to notify the dual-port memory control logic that the bus has been acquired and an interlocked access can be granted. This is necessary to avoid hardware deadlocks.

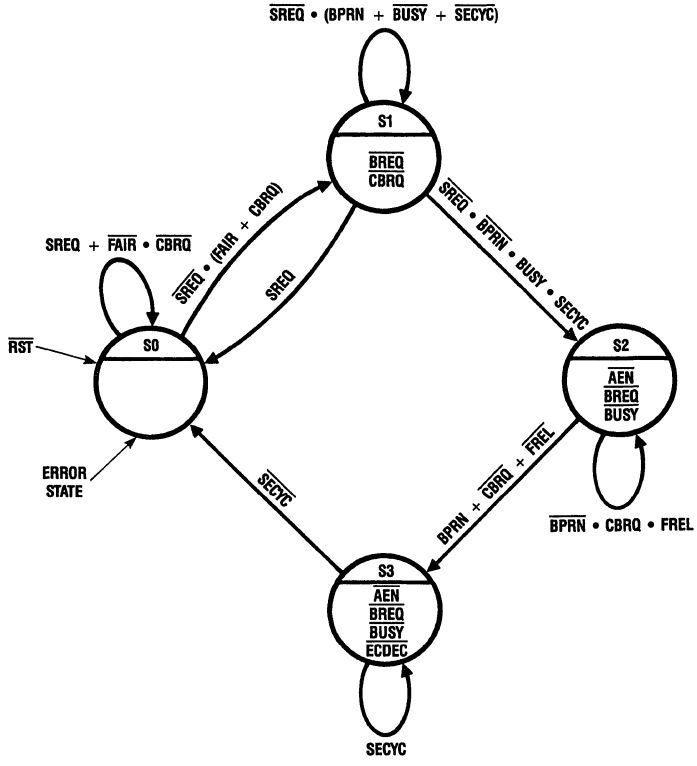


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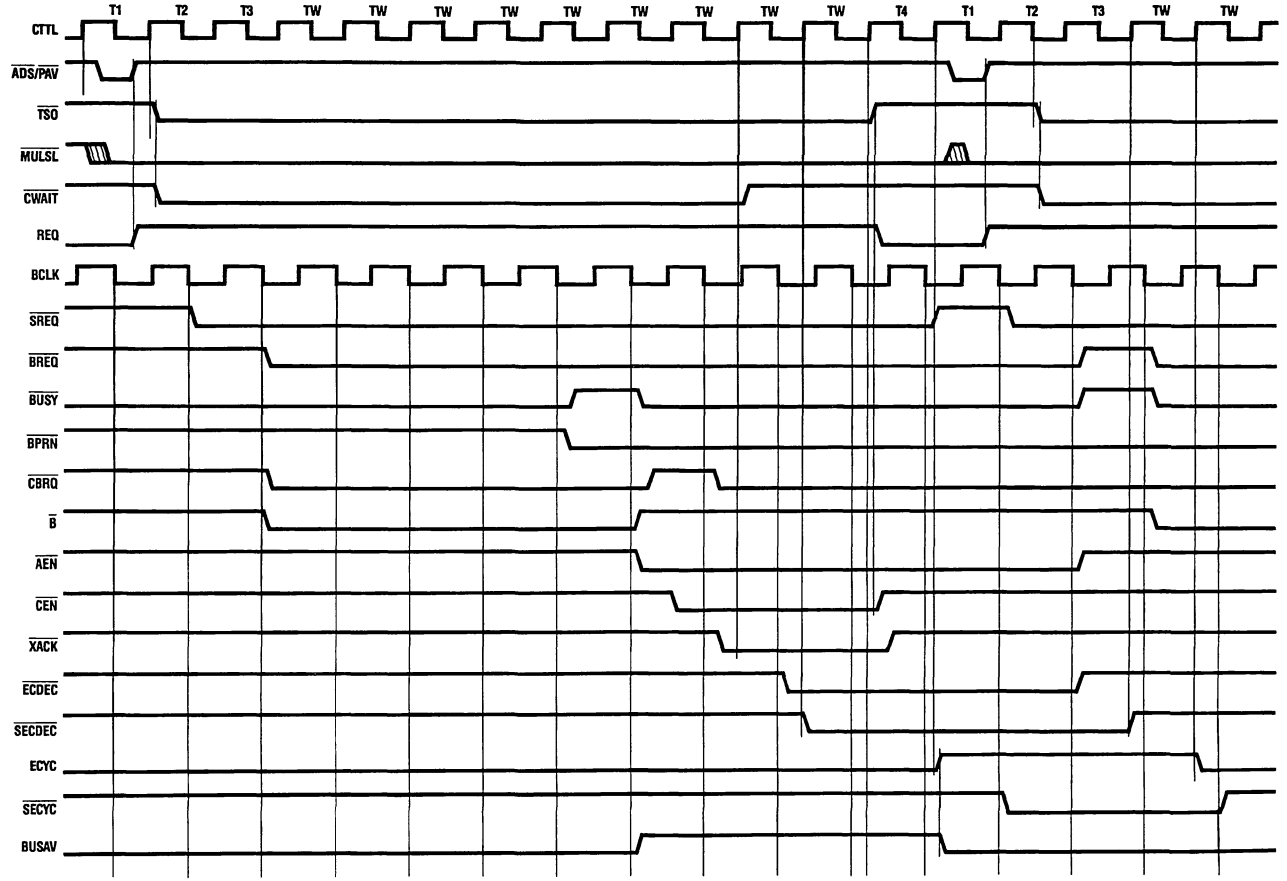
FIGURE 2. MULTIBUS Arbiter State Diagram



TL/EE/8518–3

FIGURE 3. MULTIBUS Acquisition and Release Timing Diagram

JUMPER SETTINGS

The following explains how to use the different jumpers provided in the MULTIBUS arbitration circuitry.

W1: This jumper should be installed if MMU cycles must be interlocked. This may be necessary if some page tables must be shared by different masters.

W2: W2 should be installed if W1 is installed and some shared page tables are kept in the dual-port memory of another master.

W3: If this jumper is not installed, an interlocked access cycle generates a MULTIBUS request, even though the cycle is not directed to the MULTIBUS. This may be necessary to avoid deadlocks. This jumper can be installed if all the cycles of an interlocked operation are always directed to either the MULTIBUS or the dual-port memory. This could improve the system performance by eliminating the need to acquire the bus when an interlocked operation only accesses the dual-port memory. This jumper should not be installed when using the present versions of the Series 32000 CPUs because these CPUs can prefetch between the read and write cycles of an interlocked operation.

W4: When this jumper is installed, the bus is released at the end of each cycle. This should be avoided if all the masters in the system support $\overline{\text{CBRQ}}$, since a significant performance degradation would result. However, if some lower priority master does not support $\overline{\text{CBRQ}}$, W4 must be installed, otherwise the lower priority master (not supporting $\overline{\text{CBRQ}}$) will not be able to acquire the bus.

W5: When W5 is installed, a "fairness" arbitration mechanism is activated. In this case a new bus request is issued only when all other external requests have been serviced. This allows a serial arbitration scheme to be used with three masters (or more, if the bus clock frequency is reduced) heavily using the bus, without the risk of the bus being monopolized by the two top priority masters.

W6: W6 must be installed when a serial (daisy chain) arbitration scheme is used. It must be removed when using a parallel scheme.

Arbiter Logic Equations

$S0 := S0 * (SREQ + \overline{FAIR} * \overline{CBRQ}) + S1 * SREQ + S3 * \overline{SECYC} + \overline{RST} + ERRST$

$S1 := (S0 * \overline{SREQ} * (FAIR + CBRQ) + S1 * \overline{SREQ} * (BPRN + \overline{BUSY} + \overline{SECYC})) * RST$

$S2 := (S1 * \overline{SREQ} * \overline{BPRN} * BUSY * SECYC + S2 * \overline{BPRN} * CBRQ * FREL) * RST$

$S3 := (S2 * (BPRN + \overline{CBRQ} + \overline{FREL}) + S3 * SECYC) * RST$

State Encodings

$S0 = A \bullet B \bullet \overline{C} \bullet D$

$S1 = A \bullet \overline{B} \bullet C \bullet D$

$S2 = \overline{A} \bullet B \bullet C \bullet D$

$S3 = \overline{A} \bullet B \bullet C \bullet \overline{D}$

Error state

$ERRST = A \bullet B \bullet C \bullet D$

FIGURE 4. Arbiter Logic Equations and State Encodings

```
PAL16R8A
PART #
MULTIBUS ARBITER
NATIONAL SEMICONDUCTOR
CLK REQ RST ECYC BUSY CBRQ BPRN FREL FAIR GND
EN NC NC SECYC SREQ C B A D VCC
/A := A * /B * C * D * /SREQ * /BPRN * BUSY * SECYC * RST + /A * B * C * D * RST
   + /A * B * C * /D * SECYC * RST
/B := A * B * /C * D * /SREQ * FAIR * RST + A * B * /C * D * /SREQ * CBRQ * RST
   + A * /B * C * D * /SREQ * BPRN * RST + A * /B * C * D * /SREQ * /BUSY * RST
   + A * /B * C * D * /SREQ * /SECYC * RST
/C := A * B * /C * D * SREQ + A * B * /C * D * /FAIR * /CBRQ + A * /B * C * D * SREQ
   + /A * B * C * /D * /SECYC + /RST + A * B * C * D
/D := /A * B * C * D * BPRN * RST + /A * B * C * D * /CBRQ * RST
   + /A * B * C * D * /FREL * RST + /A * B * C * /D * SECYC * RST
/SREQ := REQ
/SECYC := ECYC
```

FIGURE 5. PAL Equations in "PALASM" Format

Effects of NS32082 Memory Management Unit on Processor Through Put

National Semiconductor
Application Note 464
Chris Siegl

INTRODUCTION

The purpose of this application note is to give a satisfactory answer to the question, "How great is the performance penalty for using the NS32082 memory management unit?" To arrive at a satisfactory answer a number of benchmarks have been run on the DB32000 board using the NS32032 with and without the NS32082 as well as the NS32016 with and without the NS32082. The benchmarks were compiled on two different compilers to show the differing effects of the MMU based on the degree of code optimization. The results are tabulated in a table along with the percent performance penalty.

The results show that the percentages vary over the wide range of 6% to 18.5% with generally a greater MMU impact with higher levels of code optimization in the compiler. The Whetstone benchmark has also been included to show the effects of the MMU on floating-point instructions. As can be seen in the tables the effects are much smaller with longer instructions such as the floating-point instructions. The last section of this ap-note rationalizes the differences in performance under varying conditions and gives some rules of thumb to use in applying this data to a specific case.

THE TEST SET-UP

To run this set of tests the DB32000 board was used. This board is a complete microprocessor system specifically designed to assist the user in evaluating and developing hardware and software for the NS32032 CPU, related slave processors (NS32081 FPU and NS32082 MMU) and support devices. Through the use of on board multiplexers the NS32016 and NS32008 CPU's can also be run on this board. The configuration of this board used for these tests consist of the NS32081 FPU (floating point unit), the NS32202 ICU (interrupt control unit), 256K of dynamic RAM, extensive ROM/EPROM capability, and two serial RS-232 ports as well as a parallel I/O port. See the DB32000 data sheet for more detailed information.

The TDS monitor (shipped installed on the DB32000 board) was then removed and replaced with MON32. This monitor is compatible with National's DBG16 debugger and allows downloading of code from a host computer through the debugger using an RS-232 link therefore allowing the host machine to be remote from the development environment. This can even be done over a modem line to the host.

A timing routine using the counters in the ICU was linked to the compiled benchmark programs before they were downloaded to the DB32000. A command to the debugger then started the timing program executing which in turn called the compiled benchmark after starting the ICU counters. After the benchmark completes, it returns to the timing routine where the counters are stopped and the execution time is read from the registers. This set-up and the timing program used are covered in detail in another application note titled "Using the DB32000 Evaluation Board for Benchmarking".

The SYS-32 Multi-User development system was used as the host. This system is based on the Series 32000 family, runs GENIX™ (National's version of Berkley 4.1 UNIX™) operating system in a demand paged virtual memory environment. The system supports up to eight simultaneous users, C and Pascal high level language compilers, a Series 32000 assembler, symbolic debugger and supports in-system emulation for the 32000 family. The minimum system configuration consists of 1.25 megabytes of RAM (expandable to 3.25 megabytes) 70 megabytes of hard disk (expandable to 490 megabytes) and a streamer tape drive for backup. For more detailed information on the SYS-32, please refer to the SYS-32 data sheet. The details of the DBG16 symbolic debugger's usage for down loading and execution of the benchmaks is covered in the ap-note "Using the DB32000 Evaluation Board for Benchmarks".

RESULTS

TABLES I, II and III show the results of running the benchmarks under the four different part combinations. As can be seen in tables the MMU penalty varies considerably from benchmark to benchmark and especially from one compiler to another. To set an understanding of why the variations are so big, we must look at how the 32000 family of CPU's operate in memory.

TABLE I
Benchmarks Executed on DB32000—All Processors Running at 10 MHz with no Wait States using Genix 4.1 C Compiler

Benchmark	NS32032 W MMU	NS32032 W/O MMU	MMU Penalty	NS32016 W MMU	NS32016 W/O MMU	MMU Penalty
Ackerman. c	4.72	4.32	9.3%	6.03	5.27	14.4%
BenchE. c	8.89	8.12	9.5%	11.97	10.50	14.0%
Puzzle. c	20.59	19.10	7.8%	26.96	23.65	14.0%
Sieve. c	19.42	18.09	7.4%	22.15	19.62	12.9%
Fibonacci. c	22.13	20.28	9.1%	26.31	23.61	11.4%
Longsearch. c	7.36	6.71	9.7%	10.31	8.70	18.5%

TABLE II
Benchmarks Executed on DB32000—All Processors Running at 10 MHz with no Wait States using Greenhill's C-32000 1.6.8 Compiler

Benchmark	NS32032 W MMU	NS32032 W/O MMU	MMU Penalty	NS32016 W MMU	NS32016 W/O MMU	MMU Penalty
Ackerman. c	3.75	3.30	13.6%	5.06	4.37	15.8%
BenchE. c	4.44	4.00	11.0%	4.76	4.48	6.3%
Puzzle. c	7.82	7.09	10.3%	9.61	8.57	12.1%
Sieve. c	17.71	16.41	7.9%	19.65	17.89	9.9%
Fibonacci. c	18.34	16.47	11.4%	24.87	21.17	17.5%
Longsearch. c	6.77	5.97	13.4%	8.75	7.48	17.0%

TABLE III
Benchmarks Executed on DB32000—All Processors Running at 10 MHz with no Wait States using Genix 4.1 Pascal Compiler

Benchmark	NS32032 W MMU	NS32032 W/O MMU	MMU Penalty	NS32016 W MMU	NS32016 W/O MMU	MMU Penalty
Whetstone. P	5.08	4.83	5.2%	6.17	5.63	9.6%

Both the NS32032 and the NS32016 have an eight byte queue for instruction prefetching. As a result of this queue having an MMU in the system has little effect on instruction fetching. An interesting test that helps in understanding this is to add wait states only to the code segment while using no waitstate RAM for the stacks and static data segments. These tests show a performance degradation of only 2 or 3% per waitstate. Another approach to demonstrating the same effect which is not dependent on a special hardware setup (controlling the number of wait states on different areas of memory space is done in hardware) is to generate a software loop which only uses the registers and immediate data for holding operands. A short example of such a program is shown in listing 1. Table IV shows the results obtained from timing this program both with and without the MMU. As can be seen from the times the penalty is very small, much less than 1%. This example clearly demonstrates that the queue is doing a good job of minimizing the effects of the MMU or waitstates on intruction fetching. This is why, even though the MMU lengthens each memory cycle by 25% (memory cycle goes from 4 t-states to 5) the net effect on performance is typically less than 10%. The penalty comes primarily from the lengthening of operand fetches. The NS32032 takes a much smaller penalty if the operands are primarily 32 bits or more in length. In that case the NS32032 is only doing half as many operand fetches as the NS32016, which has to do two accesses to get 32 bit operands. Another thing to note is that the performance times between NS32032 and the NS32016 is less than 1% in our software program loop test (see Table IV). This is because both processors are internally identical except in the queue and bus interface. If the queue keeps up and there are no stack or memory reference operations the execution time would be identical. The difference in time in this test is due to the queue not quite keeping up and the branch which purges the queue which the NS32032 reloads twice as fast.

TABLE IV
Benchmarks Executed on DB32000—All Processors Running at 10 MHz with No Wait States
(times are in microseconds)

Benchmark	NS32032 W MMU	NS32032 W/O MMU	MMU Penalty	NS32016 W MMU	NS32016 W/O MMU	MMU Penalty
Progloop.b.s	12622	12559	0.50%	12750	12668	0.65%
Progloop.w.s	13344	13291	0.40%	13432	13350	0.61%
Progloop.d.s	14988	14939	0.33%	15075	14992	0.55%

Tables I and II are the results of two different compilers using the same source files for input but generating code at different levels of optimization. The compiler in Table II optimizes to a much greater degree resulting in a much smaller ratio of instruction fetches to operand fetches while the table one compiler generates more code to do the same work. The number of operands does not decrease through optimization but extraneous code is eliminated, driving down the code to operand fetch ratio. As a result the penalty rises but is still in the neighborhood of 10%. The greater the complexity of the instruction the smaller the MMU penalty because the queue is more likely to keep up and a larger ratio of execution time to operands fetched especially with the NS32032. Table III gives the results of the Whetstone benchmark which illustrates this. The Whetstone benchmark is primarily floating point, the big NS32032 advantage comes from the operands being 32 or 64 bits in length. The NS32016 is making two times as many operand memory references as the NS32032 and therefore gets two times the MMU penalty.

CONCLUSIONS

After studying the above tests we can see the major factor effecting the performance penalty due to the MMU is the number of operand references and stack operations per unit of time. If operands are typically longer than 16 bits or the stack is heavily used, the NS32032 will show a much lower MMU penalty than the NS32016. However, even for the NS32016 the MMU penalty is seldom greater than 15% and typically half that for the NS32032. This penalty being so small makes a strong case for using the MMU even in systems not using a bulk memory device and benefiting from the page replacement aspects. The MMU can be useful in these non bulk memory applications for protection at the page level as well as for system debugging and program maintenance. If portions of the ROM based code require changes only the ROM holding the effected page table needs to be replaced with the new code being addable in any available ROM socket. The MMU with the on board breakpoint resistors and counter can often greatly simplify isolating bugs in the field where system disassembly on an ISE (In System Emulator) would be out of the question or inconvenient.

In bulk memory based systems there is no question that the performance improvements due to the MMU far outweigh the performance lost due to a longer memory cycle. For more details in this area see the technical note entitled "Series 32000 The Benefits of Demand Paged Virtual Memory".

LISTING 1

```
;#########################################################################
;       INLINE CODE LOOP
;       12-10-85 by Chris Siegl
;       all operands in registers
;#########################################################################
;       progloop.b.s = i's replaced by b at end of instructions - operands
;                      are bytes (8 bits)
;       progloop.w.s = i's replaced by w at end of instructions - operands
;                      are words (16 bits)
;       progloop.d.s = i's replaced by d at end of instructions - operands
;                      are double-words (32 bits)
        .program
-main::
        movi    0,r0        ;set loop counter to 0 for 256 loops
        movi    9,r3        ;put bcd values in r3 & r4
        movi    9,r4
        movi    r3,r1
        movi    r3,r2
        movi    r3,r5
        movi    r3,r6
```

```
loop:
        absi    rl,r2
        addi    rl,r2
        addci   rl,r2
        addpi   r3,r4
        subpi   r3,r4
        addqi   4,rl
        ashi    4,rl
        lshi    5,rl
        roti    6,rl
        andi    r2,r5
        comi    r2,rl
        ori     r2,rl
        xori    r2,rl
        nop
        muli    r5,r6
        absi    rl,r2
        addi    rl,r2
        addci   rl,r2
        addpi   r3,r4
        subpi   r3,r4
        addqi   4,rl
        ashi    4,rl
        lshi    5,rl
        roti    6,rl
        andi    r2,r5
        comi    r2,rl
        ori     r2,rl
        xori    r2,rl
        nop
        muli    r5,r6
        acbb    1,r0,loop
        rxp     0
        .endseg
```

Interfacing Memory to the NS32532

National Semiconductor
Application Note 513
Tony Radi

The overall throughput of microprocessor systems often depends on the performance of the memory subsystem. To achieve optimum throughput with a high-performance microprocessor such as the NS32532, memory should operate with few or no wait states. The processor's clock frequency and the speed of memory components determine the number of wait states. This Application Note discusses design considerations for interfacing DRAM and SRAM to the NS32532. It covers four topics:

- An overview of NS32532 memory interface requirements
- A simple SRAM interface
- An interleaved SRAM interface
- A simple DRAM interface

BACKGROUND

The NS32532 microprocessor communicates with its environment via parallel busses and signals. These include a 32-bit data bus, a 32-bit address bus, a number of control signals, and five bus status pins.

The processor has instruction and data caches as well as an on-chip Memory Management Unit (MMU) to reduce bus utilization, thereby increasing throughput. The MMU uses page tables in external memory to perform logical-to-physical address translation. In order to minimize page table accesses, the NS32532 maintains a Translation Look-aside Buffer (TLB) containing information about frequently-used addresses. When the TLB does not contain needed information, the NS32532 fetches it from the external page tables. The on-chip caches duplicate a subset of external memory. The contents of an on-chip cache are acquired in one clock cycle, while it takes a minimum of two clocks to fetch data from external memory. Therefore, on-chip caches substantially reduce average memory access time when they contain the code and data the processor needs.

On each memory access, the processor initiates a memory access cycle while searching the internal cache. This reduces access time, since the memory cycle is already in process when the cache does not contain the needed information. During a read that fails to find the data in the cache (a cache miss), the memory cycle continues and the processor fetches the data from external memory. Unless declared non-cacheable, the information is placed in the internal instruction or data cache for future reference. Conversely, when the instruction or data cache contains the sought information (a cache hit), the processor cancels the memory access cycle.

A memory write is always treated as a cache miss, so that external memory is updated; this is a "write through" cache policy. When an internal cache contains a copy of the memory location being updated, the processor also updates the cache using a "write allocate" cache policy, thus ensuring that both copies of the data are the same.

MEMORY ORGANIZATION

The 32-bit address bus of the NS32532 provides up to 4 Gbytes of memory in a uniform linear address space starting at zero and ending at $2^{32}-1$. Each memory location contains an eight-bit byte. Two contiguous bytes form a word, and two contiguous words are a double-word. A word or double-word can start at any address, since there are no memory alignment requirements with the Series 32000® processors. Although addressable as bytes, memory is organized as double-words, where the address of a double-word is the address of its least significant byte.

While the NS32532 has no address alignment requirements, alignment affects the time to access a word or double-word. The processor more quickly accesses a double-word whose address is a multiple of four than one whose address is otherwise; it takes two memory cycles to fetch non-double-word aligned data.

The NS32532 supports the memory mapping of peripheral devices and coprocessors. Such devices can be located anywhere in the address space except for the upper 8 MB (addresses $FF800000_{16}$ through $FFFFFFFF_{16}$), which are reserved. The following section describes the bus signals required for memory or I/O interfacing.

BUS INTERFACE

The NS32532 performs six types of bus operations:

1. Instruction fetch
2. Memory or I/O read
3. Memory or I/O write
4. Read or update page table entries
5. Acknowledge interrupt or completion of interrupt service routine
6. Transfer information to/from Slave Processor

Cases 1 through 5 have identical bus timing characteristics and are discussed below. The only external difference among these cases is a six-bit code placed on the bus status pins (ST_0–ST_5) during bus cycles for the purpose of identifying which operation is occurring. Case 6 has separate control signals; Slave Processor operation is not relevant to this Application Note and is not discussed here.

The NS32532 can "burst read" up to four consecutive double-words from memory. This feature reduces the amount of time the processor spends on the memory bus while increasing the hit rate of internal caches. Details of burst operation appear later in this document.

The I/O signals of the NS32532 support interfacing to memory, memory-mapped devices, slave processors, and external caches. The following control signals implement RAM interfacing on any system without the external cache:

- D_0–D_{31}: Bidirectional data bus. Either 8, 16, or 32 bits of data are transferred at a time. D_0 is the least significant bit.
- A_0–A_{31}: Address bus. A_0 is the least significant bit.
- $\overline{ADS}$: Address strobe. Indicates that a bus cycle has begun and a valid address is on the bus. This signal is the earliest indication of a bus cycle in progress. The bus cycle may potentially be cancelled in event of an internal cache hit.
- $\overline{BE_0}$–$\overline{BE_3}$: Byte enable. These signals indicate which bytes should be selected for transfer. During write cycles, $\overline{BE_0}$–$\overline{BE_3}$ enable the memory banks for writing. During reads, they select the appropriate banks of an I/O device

that may exhibit undesired effects of reading intended only for some banks. During cacheable read cycles, the processor reads all bytes regardless of how the byte enable signals are encoded. Thus all memory banks should be selected for a cacheable read cycle, disregarding $\overline{BE}_0$–$\overline{BE}_3$.

- $\overline{BMT}$: Begin memory transaction. This signal indicates that a bus cycle has begun. The processor may cancel the bus cycle and negate $\overline{BMT}$ if there is an internal cache hit. This signal cannot be used as a strobe in read cycles. However, in a write cycle due to "write through" implementation of the internal caches, this signal can be used as a strobe to start a bus cycle.
- $\overline{CONF}$: Confirmation. Indicates that a bus cycle initiated by $\overline{ADS}$ is valid and has not been cancelled. This signal should be used to start a memory transfer or proceed with a memory transfer that has already been initiated.
- ST_0–ST_5: Bus status. These six bits indicate the type of bus cycle currently in progress. If the processor is idle on the bus, these outputs indicate why.
- U/$\overline{S}$: User or supervisor. Specifies the address space (user or supervisor) of the current bus cycle.
- $\overline{DDIN}$: Data direction in. Indicating the direction of data transfer, this signal is used to generate read and write strobes.
- $\overline{BOUT}$: Burst out. The processor asserts this signal to request a burst cycle. Due to the timing of $\overline{BOUT}$ activation, it should not be used as a burst request or to generate the $\overline{BIN}$ signal (described next). Instead, it should be monitored to continue or terminate a burst that has already been initiated.
- $\overline{BIN}$: Burst in. Notifies the processor if the memory supports burst cycles. The memory controller should not wait for $\overline{BOUT}$ before asserting this signal. The address decoder should determine whether or not to assert $\overline{BIN}$.
- $\overline{RDY}$: Ready. Notifies the processor when memory or a peripheral device is ready to transfer data. If this signal is not active, the processor inserts wait states to extend the current bus cycle, thus supporting slow memory and peripheral devices.
- $\overline{BER}$: Bus error. Indicates that an error has occurred during the bus cycle. The processor treats $\overline{BER}$ as the highest priority exception after reset, and executes the $\overline{BER}$ exception routine.
- $\overline{BRT}$: Bus retry. Indicates that the current bus cycle should be retried. The processor will reexecute the bus cycle.
- CLK: Input clock signal. The 32000 series requires a single-phase clock signal running at a frequency twice that of the processor's operating speed in MHz. CLK is internally divided to generate two non-overlapping clock signals, BCLK and $\overline{BCLK}$.
- BCLK: Bus clock. One of the clock output signals derived from CLK.
- $\overline{BCLK}$: Complementary bus clock. This signal should be used for timing reference and for synchronization of external devices with the processor.

Figure 1 is the timing diagram for a read cycle, and *Figure 2* for a write. Both figures assume that the selected memory or peripheral device is capable of communicating with the processor at full speed.

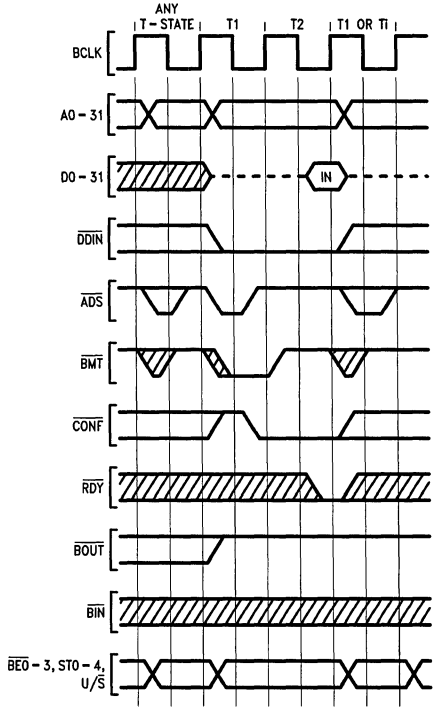


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FIGURE 1. Basic Read Cycle

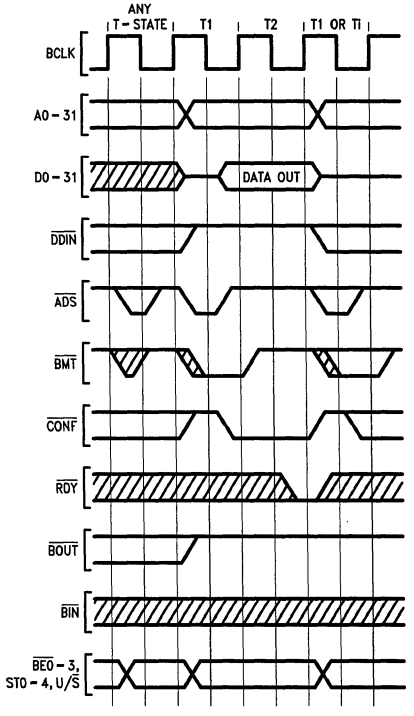

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FIGURE 2. Basic Write Cycle

A full-speed bus access occurs during two cycles of BCLK, T1 and T2. The processor asserts $\overline{ADS}$ during the first half of T1 to indicate the start of a bus cycle for both reads and writes. From the beginning of T1 until completion of the bus cycle, the processor drives the address bus and other relevant control signals as the timing diagrams indicate. The processor asserts $\overline{CONF}$ in the middle of T1 if the bus cycle is not cancelled and T2 will be entered with the next clock cycle. $\overline{BMT}$ may be asserted at the start of the cycle and then deasserted before the time it is guaranteed valid. This is caused by an internal cache hit, which cancels the initiated bus cycle. A confirmed bus cycle completes at the end of T2 unless $\overline{RDY}$ is high, in which case the processor inserts additional T2 (wait) states.

For write bus cycles, valid data is output from the middle of T1 until the end of the cycle (T2). Due to write-through implementation of the internal caches, write cycles are not cancelled. When one write cycle immediately follows another, the processor continues driving the bus with data from the previous operation until the middle of state T1 of the second bus cycle.

Following state T2 is either state T1 of the next bus cycle or an idle T-state if the processor has no bus cycle to perform.

BURST CYCLES

The NS32532 is capable of performing burst transfers, which increase bus efficiency and tend to raise the internal cache hit rate. Burst is only available in instruction fetch and data read cycles from 32-bit memories. *Figure 3* is the burst cycle timing diagram, which assumes no wait states.

A burst cycle consists of two parts. The first is a regular (opening) cycle, in which the processor outputs its status and asserts the relevant control signals. The processor asserts $\overline{BOUT}$ to indicate that it wants to perform burst cycles. If the selected memory supports burst mode, it notifies the processor via $\overline{BIN}$ low. If the memory does not allow burst ($\overline{BIN}$ high) and the cycle extension has not been requested via $\overline{RDY}$, the memory cycle terminates at the end of T2 and the processor deasserts $\overline{BOUT}$. If the memory supports burst and the processor has not deasserted $\overline{BOUT}$, the second part of the burst cycle occurs and $\overline{BOUT}$ remains active until termination of the operation.

The second part of the burst consists of up to three nibbles in state T2B. In each of these nibbles, the processor reads a 32-bit data item. After each data read, address bits A_0–A_1 go to zero and A_2–A_3 increment, and all byte enable out-

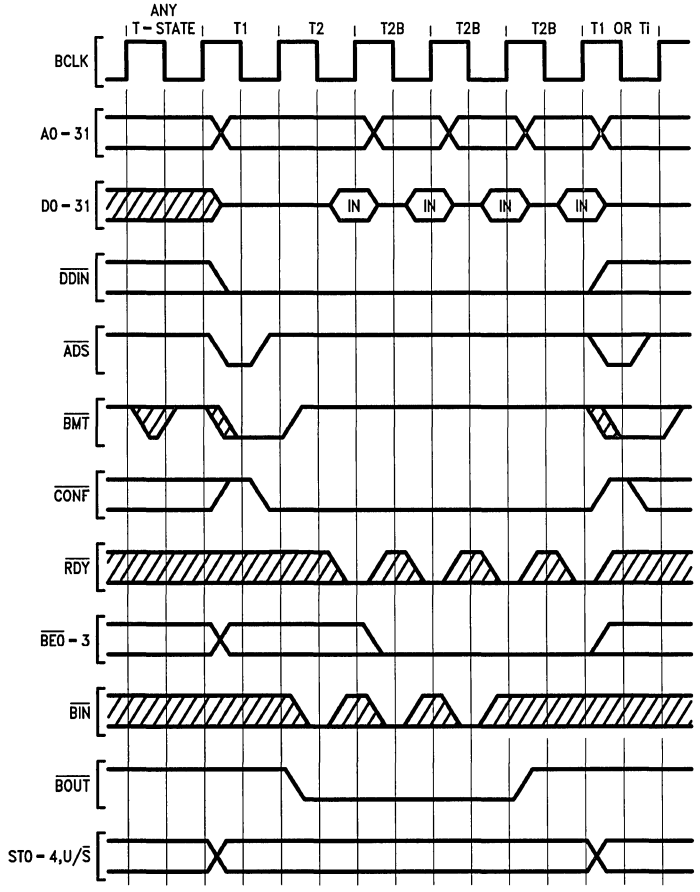

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FIGURE 3. Burst Read Cycle

puts $\overline{BE}_0$–$\overline{BE}_3$ are activated. If the $\overline{RDY}$ pin is high at the end of each T2B, the processor inserts additional T2B states to allow slow memories to work with the burst cycle.

The following sections discuss three simple designs. The first two work at up to 30 MHz, and the third at 30 MHz. The first design is a simple SRAM interface that requires no wait states on regular memory cycles. However, it requires one wait state in each nibble access at speeds higher than 20 MHz. The second design shows an interleaved memory implementation on burst access cycles, eliminating the single wait state of the first design and thus operating with memory at full speed. The third design shows a simple DRAM interface to the NS32532. This design inserts three wait states in a regular memory cycle, but only one wait state in each nibble transfer at 30 MHz.

All three designs use PAL® devices for address decoding. Standard driver, 74AS1034, are used to increase drive where the processor address bus lacks the necessary drive capability. High speed 8-bit transceivers, 74PCT245, provide isolation and additional drive capability for the data bus.

SIMPLE SRAM MEMORY INTERFACE TO THE NS32532

This section presents the results of a timing analysis and describes an SRAM interface for the NS32532 optimized for simplicity and cost. The interface does not utilize the processor's Bus Error and Bus Retry features.

This design allows all memory writes and the opening cycle of memory reads to proceed without wait states at any frequency up to 30 MHz. It also supports the NS32532's burst mode without wait states at up to 20 MHz. For burst transfers at 25 MHz and 30 MHz, one wait state is inserted in each nibble via jumper W1. *Figure 4* shows the timing diagram of the interface.

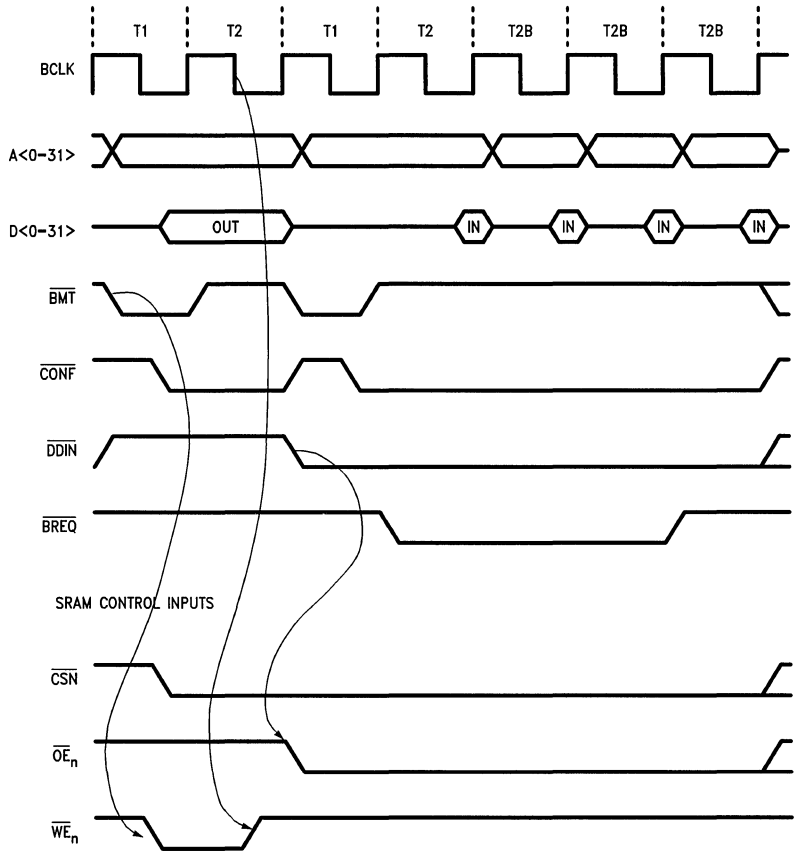

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FIGURE 4. Timing Diagram of the Simple SRAM Interface

The basis of the design is a state machine implemented by PAL16R4D (see Appendix A for state diagram PAL equations and schematics). This PAL keeps track of the processor state and drives the $\overline{RDY}$ signal high if a wait state needs to be inserted in the nibble transfer. The processor increments A_2–A_3 during burst access cycles.

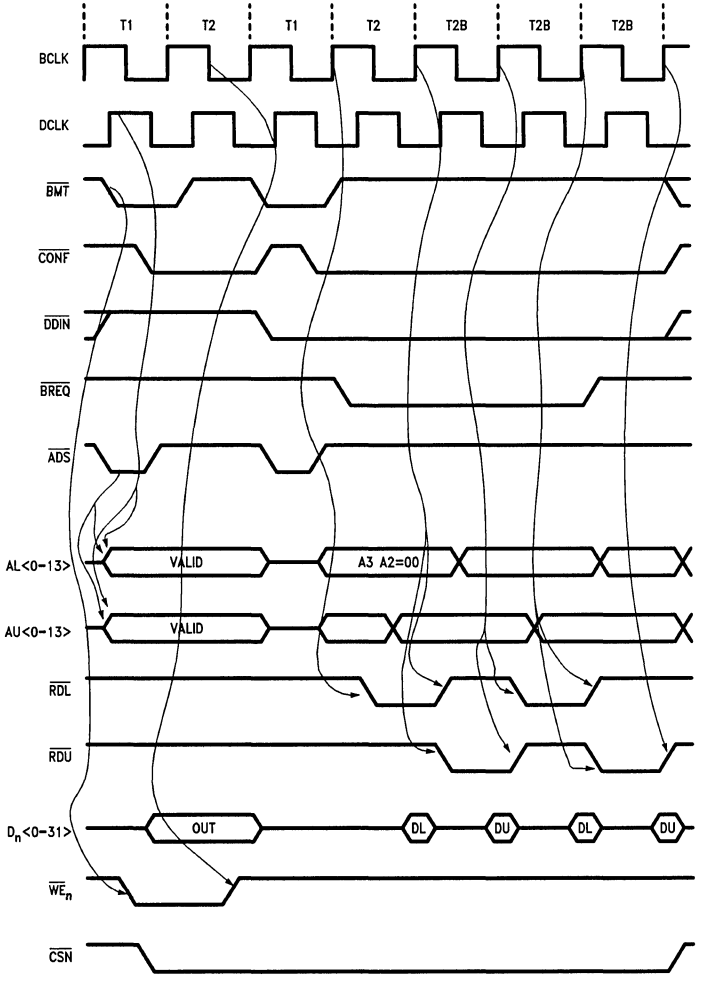
Another PAL (16L8D) generates the write strobe for memory banks. The memory write strobe is generated by $\overline{BMT}$ during write cycles (DDIN high) and terminated by the rising edge of BCLK during T2. The memory write strobe is qualified with $\overline{BE_0}$–$\overline{BE_3}$ before being routed to the memory banks. A second PAL16L8D provides address decoding, generating the $\overline{MEMRD}$ signal when the memory is addressed in a read cycle with burst allowed.

This SRAM interface uses 25 ns static RAMs, Fast or Advanced Schottky TTL gates, and D type PALs to achieve no wait state operation during regular memory cycles. During burst memory transfers at processor speeds over 20 MHz, one wait state is required in each nibble cycle for correct operation. This wait state causes only a 3% performance degradation on average.

INTERLEAVED SRAM MEMORY INTERFACE TO THE NS32532

This section presents the results of a timing analysis and describes an NS32532 SRAM interface optimized for speed and simplicity. The interface does not utilize the processor's Bus Error and Bus Retry features. Memory banks are accessed concurrently and the data is read in an interleaved fashion during burst transfers, thus eliminating the need for wait states during nibble cycles.

This design provides for operation of the NS32532 at up to 30 MHz without wait states during regular and burst memory accesses. The latched A_2 bit of the processor enables memory banks for read or write. Reads from memory banks are interleaved during burst access cycles. This way the address setup for one bank overlaps with the data read from another. *Figure 5* shows the interface's timing diagram.



TL/EE/9452–5

FIGURE 5. Timing Diagram of the Interleaved SRAM Interface

Four PALs implement the design: two for the processor state machine and specific memory control signals, one for generating write strobes, and one for address decoding (see Appendix B for state diagram PAL equations and schematics). PAL16R4D implements the state machine. It uses the latched A_2–A_3 bits to control the selection of memory banks during a burst access, alternating the assertion of $\overline{RDL}$ and $\overline{RDU}$ in successive cycles. The A_3 value is set up in a given cycle, for a bank that will be enabled in the subsequent cycle via $\overline{RDL}$ or $\overline{RDU}$ inputs. A_3 should fall through the D flip-flops in order to meet the address setup time for the SRAM in the opening cycle. To do this, a pulse is generated by qualifying a skewed clock (DCLK) with $\overline{ADS}$. This pulse clocks A_3 in the D flip-flops. For proper operation at different processor frequencies, the jumpers should be installed as follows:

- 1–2 for 30 MHz
- 3–4 for 25 MHz
- 5–6 for 20 MHz

After the opening cycle, the Set and Clear inputs of the D flip-flops change the A_3 value under control of the state machine PAL.

PAL16L8D generates the memory write strobe from $\overline{BMT}$ during write cycles (DDIN high) and terminates it on the rising edge of BCLK during T2. The memory strobe is qualified with $\overline{BE_0}$–$\overline{BE_3}$ before being routed to the memory banks.

The third PAL (16L8D) is the address decoder. It generates $\overline{MEMRD}$ when the memory is addressed in read cycles and burst is allowed. 74AS1034 is used as the buffer driver where the processor output pins lack the necessary drive capability.

This SRAM interface uses 25 ns static RAMs, Fast or Advanced Schottky TTL gates, and type D PALs to achieve no wait state operation during regular memory cycles. During burst transfers, the interleaving of memory banks allows no wait state operation of the processor up to 30 MHz.

SIMPLE DRAM INTERFACE TO THE NS32532

This section presents the results of a timing analysis and describes a DRAM interface to the NS32532 optimized for speed and simplicity. The interface, which operates at 30 MHz and does not utilize the Bus Error and Bus Retry features of the processor, uses 80 ns DRAMs to minimize the number of wait states. All $\overline{RAS}$ signals are activated during a normal DRAM access and refresh cycle. During write cycles, only the $\overline{CAS}$ signals corresponding to the enabled bytes are active, while all $\overline{CAS}$ signals are active during reads. *Figure 6* shows the interface timing diagram.

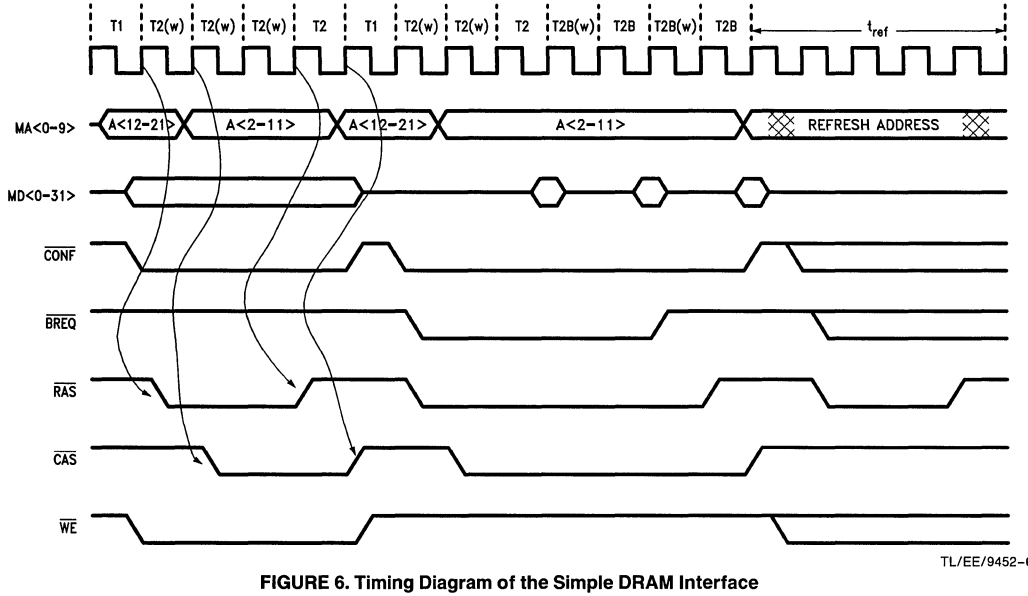


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FIGURE 6. Timing Diagram of the Simple DRAM Interface

The design uses five PALs: two for generating refresh address and refresh request, one for the state machine, one for generating $\overline{CAS}$ strobes, and one for address decoding (see Appendix C for state diagram PAL equations and schematics).

PAL16R8D implements the state machine. It keeps track of the processor state and drives the $\overline{RDY}$ signals high when wait states are inserted into bus cycles. This design uses static column DRAM, although it could use nibble mode DRAM with a simple modification to the state machine. Static column DRAM simplifies the design since the processor drives and increments A_2–A_3 during burst access cycles without the need to toggle $\overline{CAS}$. With nibble mode DRAM, the $\overline{CAS}$ lines must be toggled during nibble cycles.

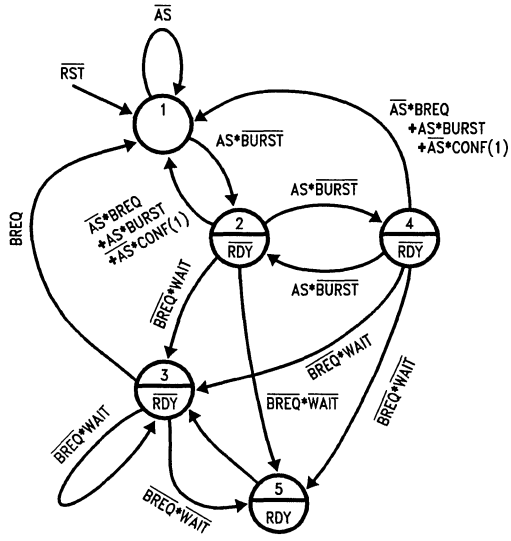
Two PAL20X10s generate the refresh address and refresh request. One PAL is the refresh address counter, which increments at the end of each refresh period. Its outputs drive the address lines of the DRAMs (row address) during the refresh period. The other PAL is the refresh interval counter, generating a refresh request ($\overline{RFRQ}$) approximately every eight μs. Clocked by BCLK, it must be modified if this interface operates at speeds other than 30 MHz. To make the PAL accommodate different speeds, a load term can be used in the PAL equations, with PAL inputs jumpered to ground or V_{CC}.

PAL16L8D generates the $\overline{CAS}$ strobes for the memory banks. In read cycles, all $\overline{CAS}$ strobes are asserted on the assumption that memory is cacheable, whereas in write cycles, the $\overline{CAS}$ strobes are qualified with $\overline{BE_0}$–$\overline{BE_3}$ before being routed to the memory banks. The memory write strobe is derived from DDIN. The data transceivers establish their direction from DDIN and are enabled by $\overline{CONF}$. The data transceivers are recommended, but not necessary to have this interface operating.

This DRAM interface uses 80 ns column DRAMs, Fast or Advanced Schottky TTL gates, and type D PALs. It achieves regular memory transfers in five cycles and burst nibbles in two cycles. It is possible to operate the NS32532 with fewer wait states by employing RAS prediction. A future Application Note will discuss features such as RAS prediction and error detection and correction.

Appendix A

State Diagram of the Simple SRAM Interface



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Note 1: This condition is a subset of /AS*BREQ condition.

PAL16R4D
STATE MACHINE PAL
STATE MACHINE PAL, WAIT STATE GENERATOR
NATIONAL SEMICONDUCTOR CORP, SANTA CLARA, CALIFORNIA
CLK NC NC WAIT RST BURST NC AS BREQ GND
OE NC A B C D NC NC NC VCC

A := A * B * /D * /BREQ * /WAIT * RST + A * C * /D * /BREQ * /WAIT * RST

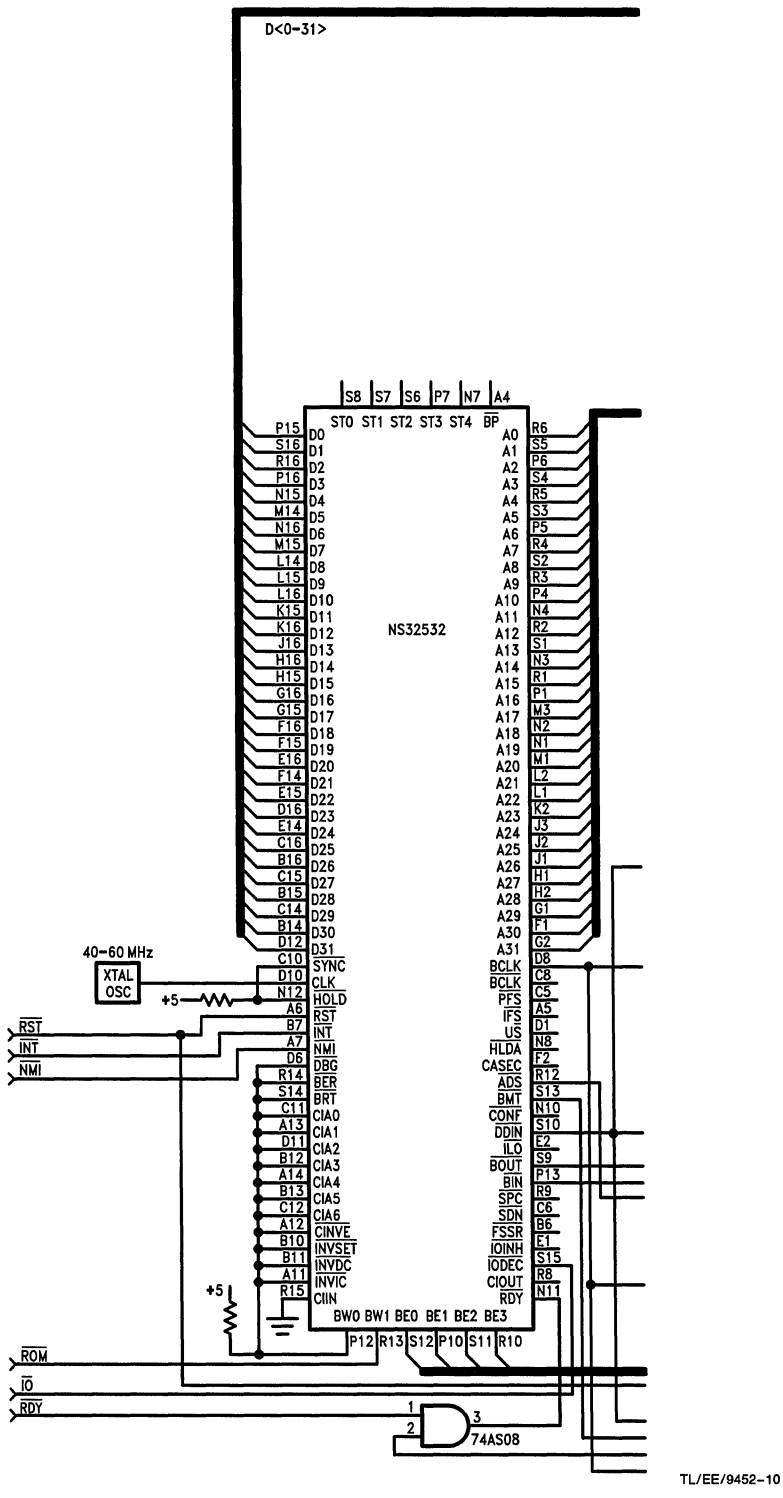
B := A * B * /D * /BREQ * WAIT * RST + A * C * /D * /BREQ * WAIT * RST
+ /A * B * C * D * RST

C := A * B * C * /D * AS * /BURST * RST

D := A * B * C * AS * /BURST * RST + A * B * /D * AS * /BURST * RST
+ A * B * /D * /BREQ * WAIT * RST + A * C * /D * /BREQ * WAIT * RST
+ /A * B * C * D * RST

```
PAL16L8D
WRITE STROBE GENERATOR
WRITE STROBE GENERATOR FOR SRAM BANKS
NATIONAL SEMICONDUCTOR, SANTA CLARA, CALIFORNIA
BE0 BE1 BE2 BE3 BDDIN A16 CONF BMT NC GND
BCLK WL0 WL2 WL3 WU0 WU1 WU2 WU3 WL1 VCC
/WL0  =  /BMT * BDDIN * /BE0 * /A16 + BCLK * /CONF * BDDIN * /BE0 * /A16
/WL1  =  /BMT * BDDIN * /BE1 * /A16 + BCLK * /CONF * BDDIN * /BE1 * /A16
/WL2  =  /BMT * BDDIN * /BE2 * /A16 + BCLK * /CONF * BDDIN * /BE2 * /A16
/WL3  =  /BMT * BDDIN * /BE3 * /A16 + BCLK * /CONF * BDDIN * /BE3 * /A16
/WU0  =  /BMT * BDDIN * /BE0 * A16 + BCLK * /CONF * BDDIN * /BE0 * A16
/WU1  =  /BMT * BDDIN * /BE1 * A16 + BCLK * /CONF * BDDIN * /BE1 * A16
/WU2  =  /BMT * BDDIN * /BE2 * A16 + BCLK * /CONF * BDDIN * /BE2 * A16
/WU3  =  /BMT * BDDIN * /BE3 * A16 + BCLK * /CONF * BDDIN * /BE3 * A16

PAL16L8D
ADDRESS DECODE PAL
ADDRESS DECODER FOR THE SRAM BANKS
NATIONAL SEMICONDUCTOR, SANTA CLARA, CALIFORNIA
F1 F2 F3 A17 A16 NC NC NC NC GND
BDDIN NC CSL CSU NC NC NC BURST NC VCC
/CSL    =  F1 * F2 * F3 * /A16 * /A17
/CSU    =  F1 * F2 * F3 * A16 * /A17
/BURST  =  F1 * F2 * F3 * /A17 * /BDDIN
```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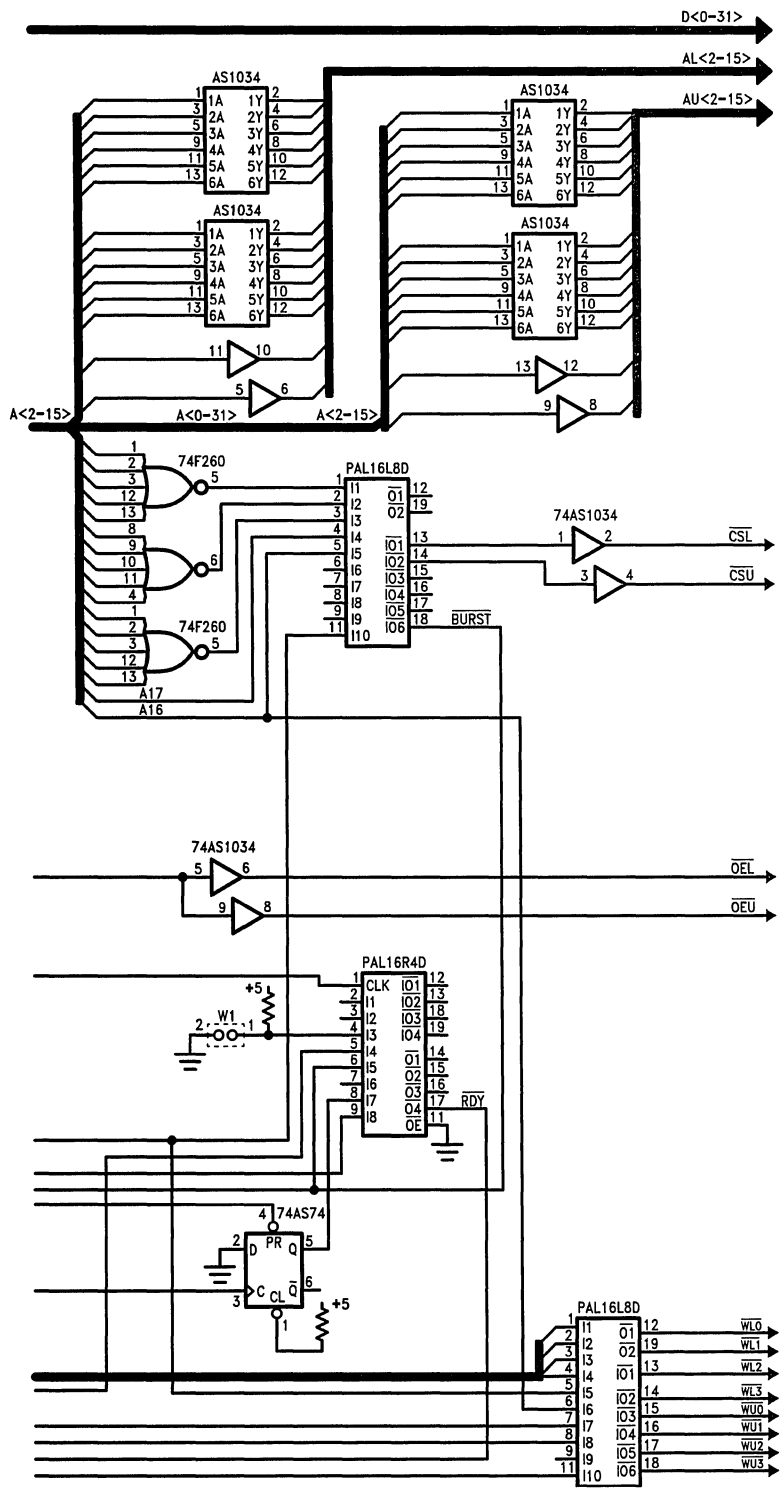
ST0 ST1 ST2 ST3 ST4 BP
NS32532
BW0 BW1 BE0 BE1 BE2 BE3
P12 R13 S12 P10 S11 R10
40-60 MHz
XTAL OSC
+5
RST
INT
NMI
ROM
IO
RDY
74AS08
TL/EE/9452-10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A<2-15>
A<0-31>
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PAL16L8D
74AS1034
CSL
CSU
BURST
A17
A16
OEL
OEU
PAL16R4D
+5
W1
RDY
74AS74
WL0
WL1
WL2
WL3
WU0
WU1
WU2
WU3

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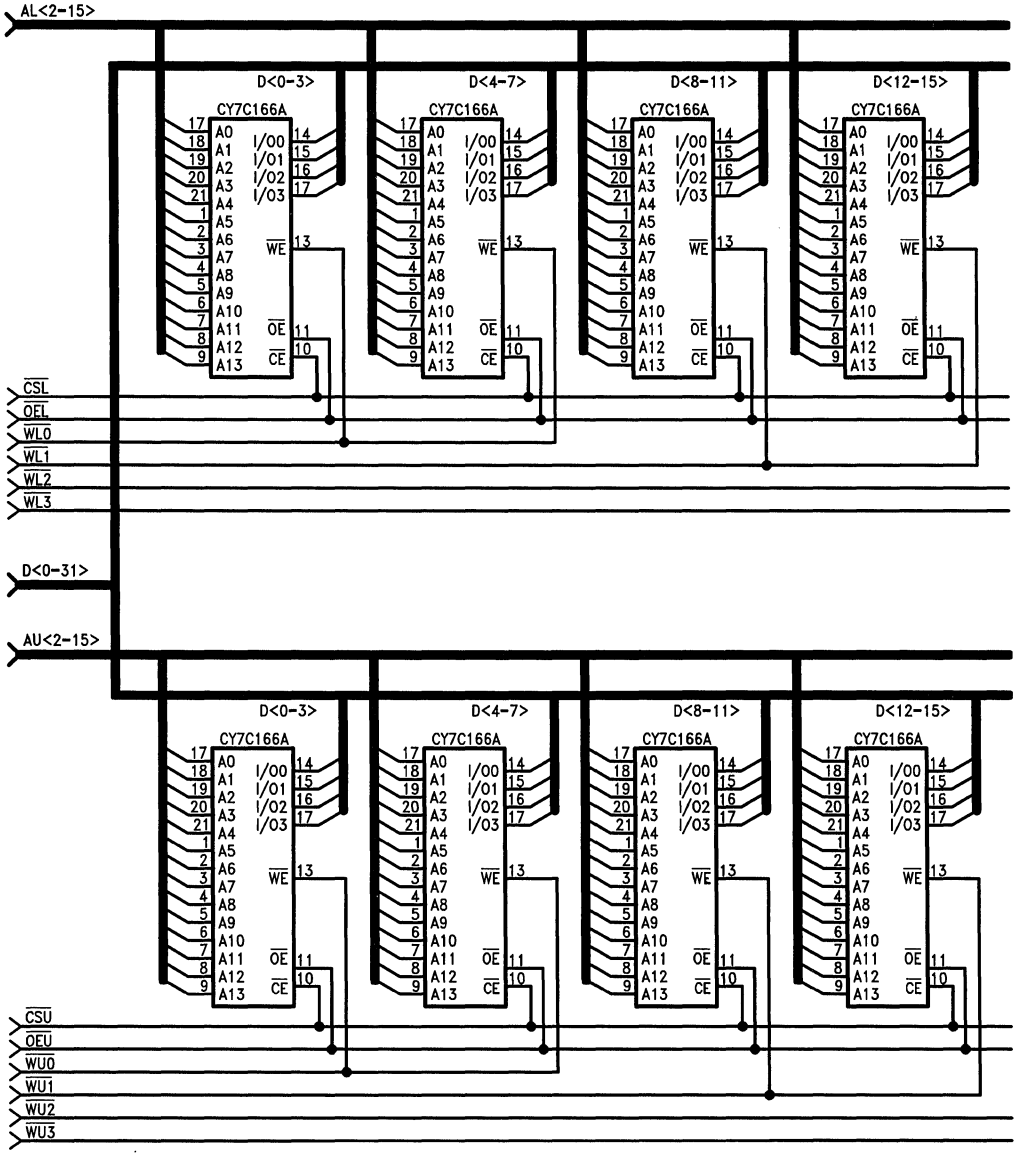
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A9
A10
A11
A12
A13
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I/O1
I/O2
I/O3
WE
OE
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OEL
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WL1
WL2
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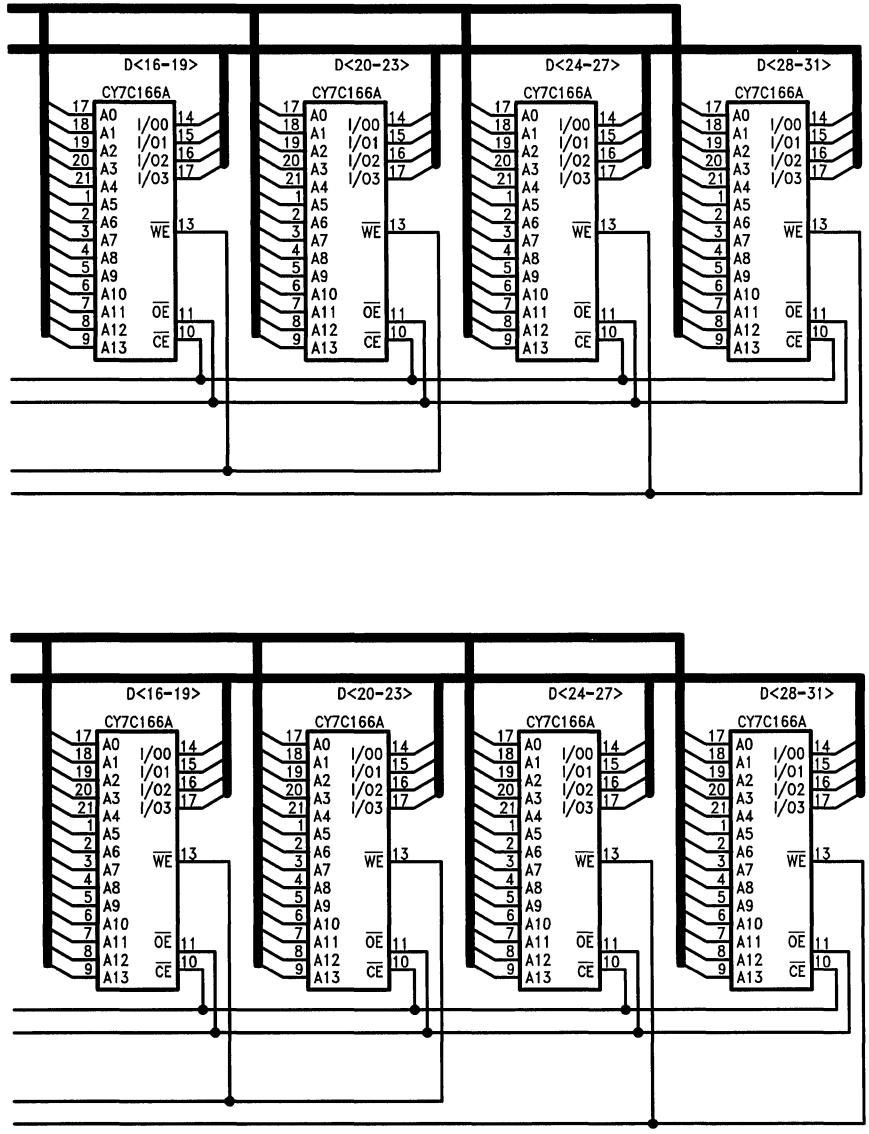
WU1
WU2
WU3

TL/EE/9452-12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A11
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A13
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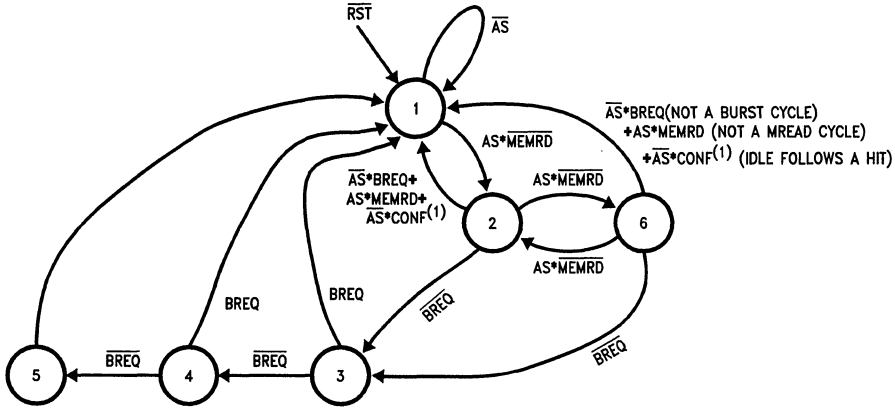
I/O1
I/O2
I/O3
WE
OE
CE

TL/EE/9452-13

Appendix B

State Diagram of the Interleaved SRAM Interface



TL/EE/9452–8

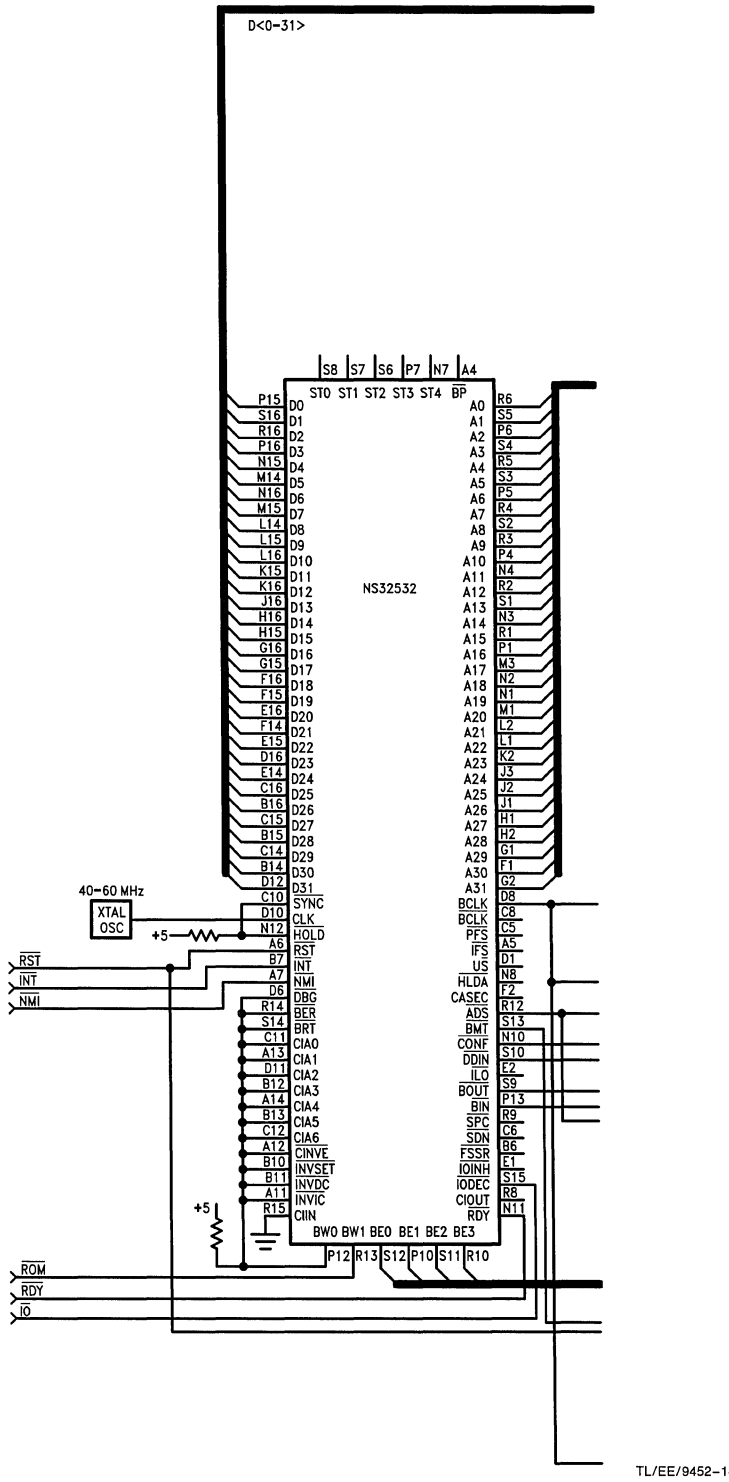
Note 1: This condition is a subset of /AS * BREQ condition.

```
PAL16R4D
STATE MACHINE PAL
STATE MACHINE ENCODING TO CONTROL SRAM BANKS
NATIONAL SEMICONDUCTOR, SANTA CLARA, CALIFORNIA
CLK LA3 LA2 NC RST /MEMRD CONF AS BREQ GND
OE RA30 RA31 A B C D OE1 OE0 VCC
/A    := A * B * C * /D * AS */MEMRD * RST + A * B * /C * D * /BREQ * RST
/B    := B * C * /D * RST
/C    := A * /B * C * D * /BREQ * RST
/D    := A * B * C * AS * /MEMRD * RST + B * C * /D * AS * /MEMRD * RST
/OE0  := B * C * /D * /LA2 * /CONF * RST + A * B * /C * D * /LA2 * RST + A * /B * C * D * LA2 * RST
       + /A * B * C * D * LA2 * RST
/OE1  := A * /B * C * D * /LA2 * RST + /A * B * C * D * /LA2 * RST + B * C * /D * LA2 * /CONF * RST
       + A * B * /C * D * LA2 * RST
/RA30 := /LA3 * LA2 * A * B * /C * D * RST + LA3 * /LA2 * A * /B * C * D * RST
       + LA3 * LA2 * B * C * /D * RST
/RA31 := /LA3 * /LA2 * A * B * /C * D * RST + LA3 * LA2 * A+ /B * C * D * RST

PAL16L8D
ADDENDUM TO STATE MACHINE
NATIONAL SEMICONDUCTOR, SANTA CLARA, CALIFORNIA
LA2 LA3 NC NC NC A B C D GND
RST SA30 NC NC NC NC NC NC SA31 VCC
/SA30 = /LA3 * /LA2 * A * /B * C * D * RST + /LA3 * LA2 * B * C * /D * RST
       + LA3 * LA2 * A * B * /C * D * RST
/SA31 = /LA3 * /LA2 * A * B * /C * D * RST + /LA3 * LA2 * A * /B * C * D * RST

PAL16L8D
WRITE STROBE PAL
WRITE STROBE GENERATOR FOR SRAM BANKS
NATIONAL SEMICONDUCTOR, SANTA CLARA, CALIFORNIA
BE0 BE1 BE2 BE3 BDDIN LA2 CONF BMT EBMT GND
BCLK WL0 WL2 WL3 WU0 WU1 WU2 WU3 WL1 VCC
/WL0 = /BMT * BDDIN * /BE0 * /LA2 * + EMBT * /CONF * BDDIN * /BE0 * /LA2
       + BCLK * /CONF * BDDIN * /BE0 * /LA2
/WL1 = /BMT * BDDIN * /BE1 * /LA2 + EBMT * /CONF * BDDIN * /BE1 * /LA2
       + BCLK * /CONF * BDDIN * /BE1 * /LA2
/WL2 = /BMT * BDDIN * /BE2 * /LA2 + EBMT * /CONF * BDDIN * /BE2 * /LA2
       + BCLK * /CONF * BDDIN * /BE2 * /LA2
/WL3 = /BMT * BDDIN * /BE3 * /LA2 + EBMT * /CONF * BDDIN * /BE3 * /LA2
       + BCLK * /CONF * BDDIN * /BE3 * /LA2
/WU0 = /BMT * BDDIN * /BE0 * LA2 + EBMT * /CONF * BDDIN * /BE0 * LA2
       + BCLK * /CONF * BDDIN * /BE0 * LA2
/WU1 = /BMT * BDDIN * /BE1 * LA2 + EBMT * /CONF * BDDIN * /BE1 * LA2
       + BCLK * /CONF * BDDIN * /BE1 * LA2
/WU2 = /BMT * BDDIN * /BE2 * LA2 + EBMT * /CONF * BDDIN * /BE2 * LA2
       + BCLK * /CONF * BDDIN * /BE2 * LA2
/WU3 = /BMT * BDDIN * /BE3 * LA2 + EBMT * /CONF * BDDIN * /BE3 * LA2
       + BCLK * /CONF * BDDIN * /BE3 * LA2

PAL16L8D
ADDRESS DECODE PAL
ADDRESS DECODE PAL
NATIONAL SEMICONDUCTOR, SANTA CLARA, CALIFORNIA
F1 F2 F3 A17 NC NC NC NC NC GND
BDDIN NC CS NC NC NC NC MEMRD NC VCC
/CS     = F1 * F2 * F3 * /A17
/MEMRD  = F1 * F2 * F3 * /BDDIN
```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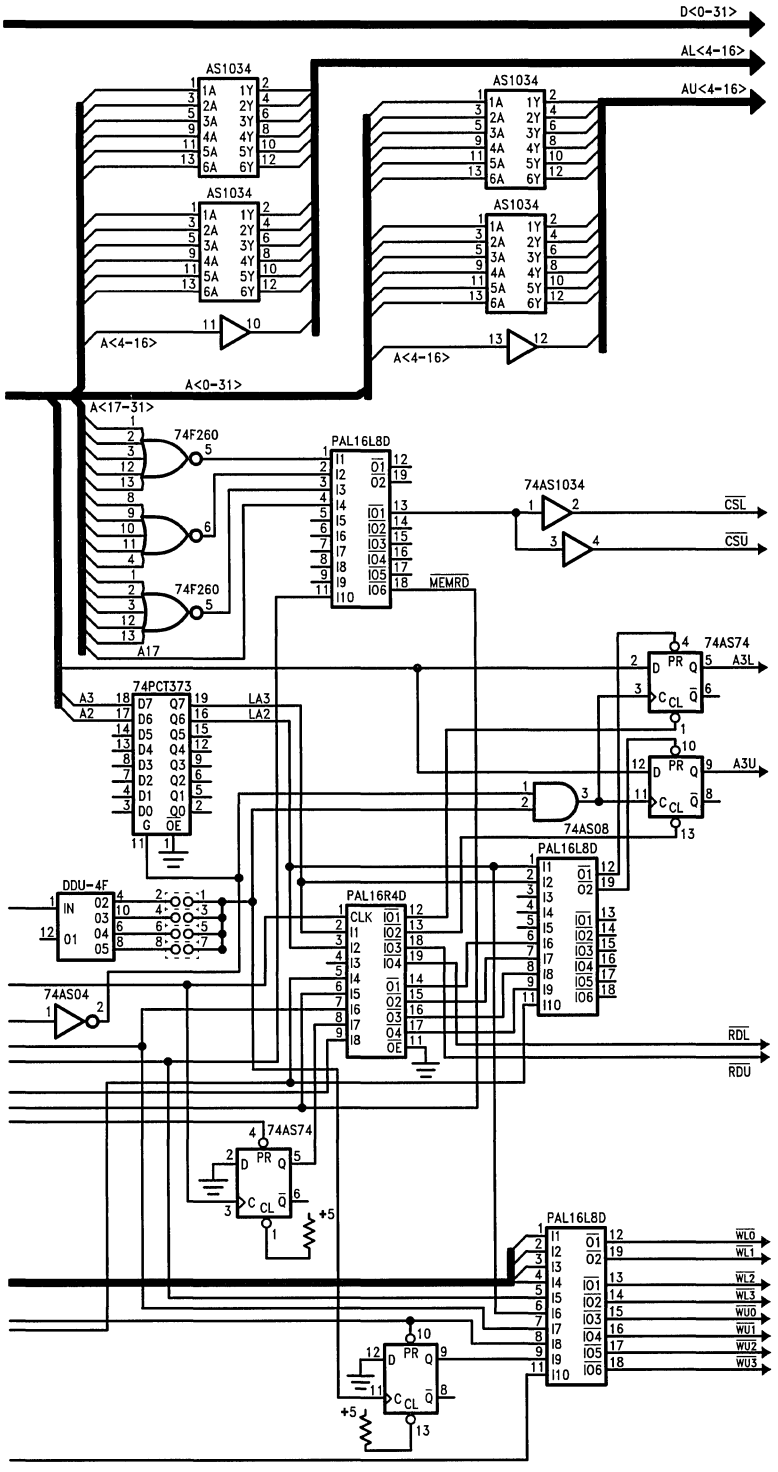
ST0 ST1 ST2 ST3 ST4 BP
NS32532
40-60 MHz
XTAL OSC
+5
BW0 BW1 BE0 BE1 BE2 BE3
P12 R13 S12 P10 S11 R10
TL/EE/9452-14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74F260
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CSU
MEMRD
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A3L
74PCT373
A3
A2
LA3
LA2
A3U
74AS08
PAL16L8D
DDU-4F
PAL16R4D
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RDU
74AS74
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WL3
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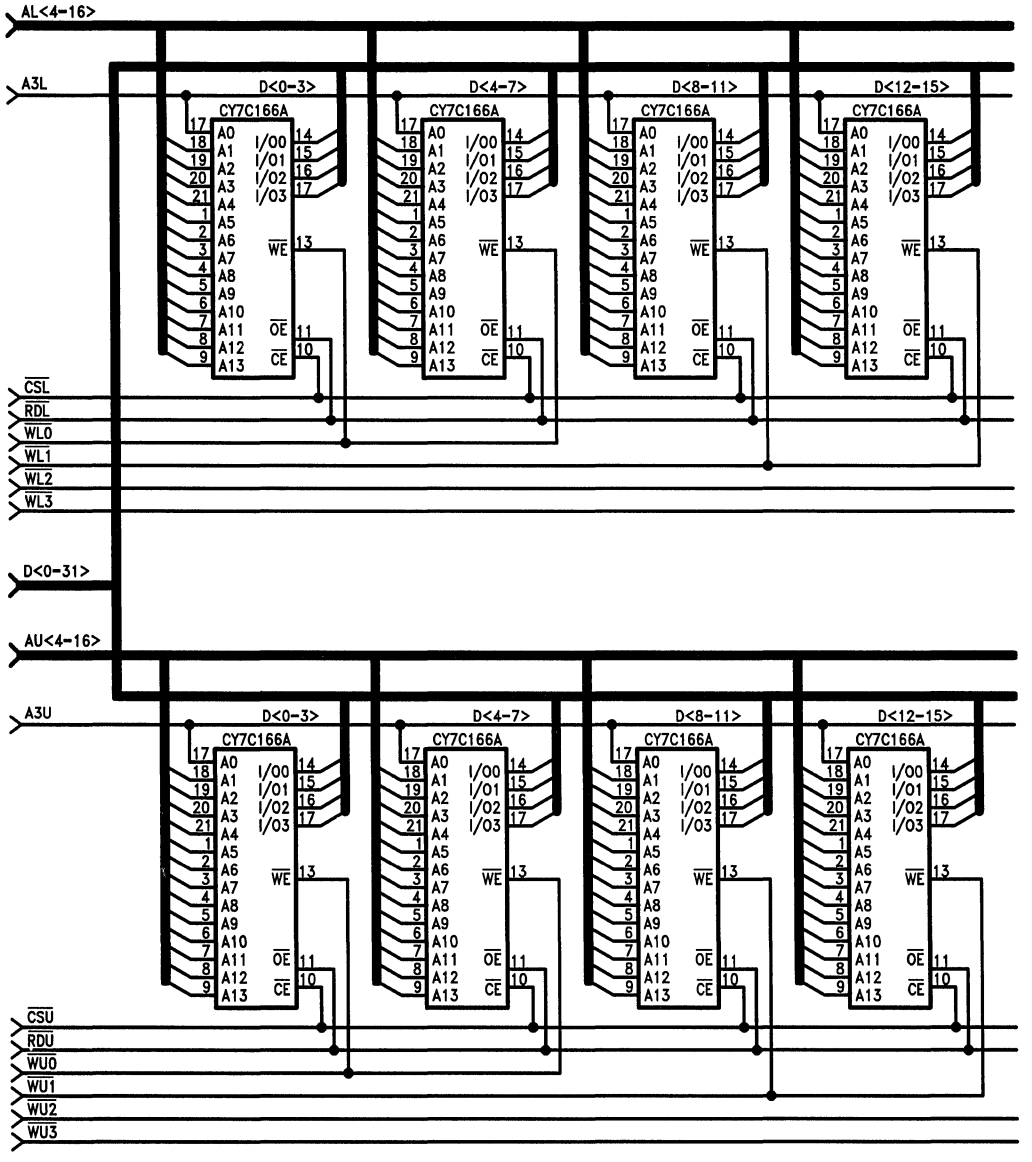
WU1
WU2
WU3
+5

TL/EE/9452–15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I/O2
I/O3
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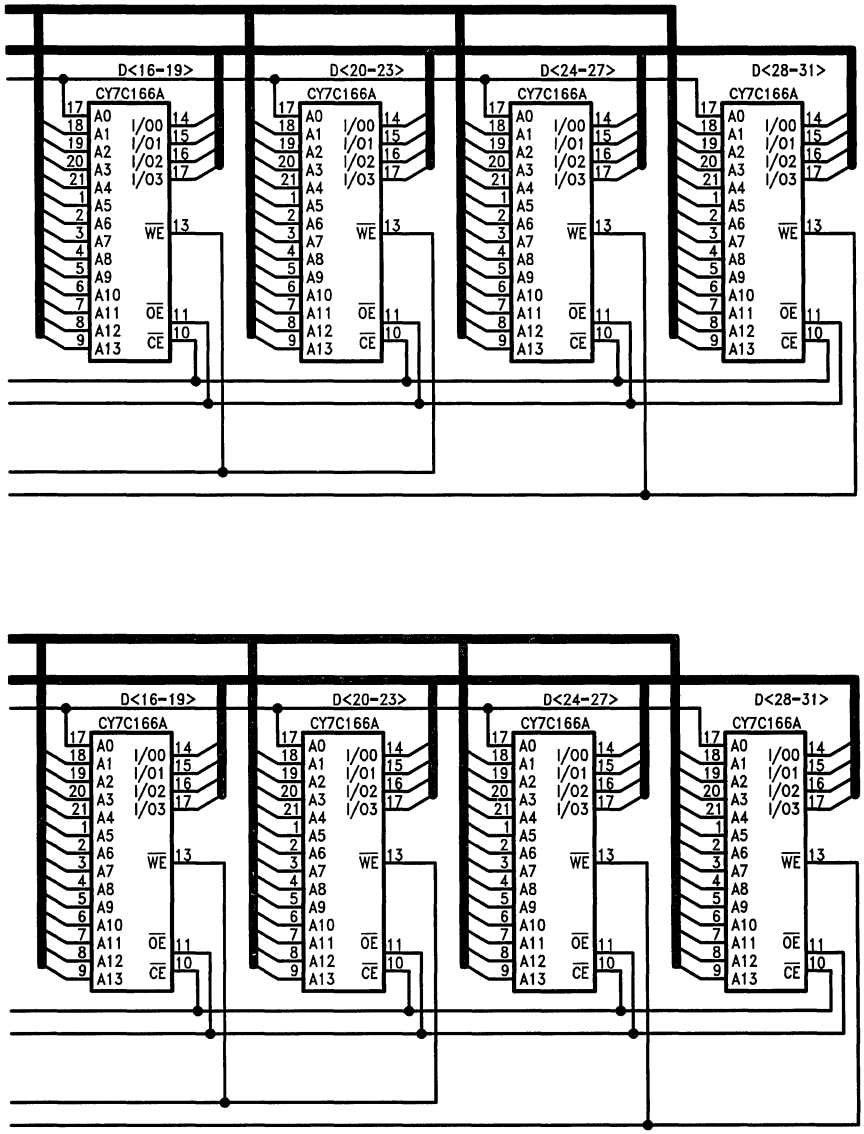
WU3

TL/EE/9452-16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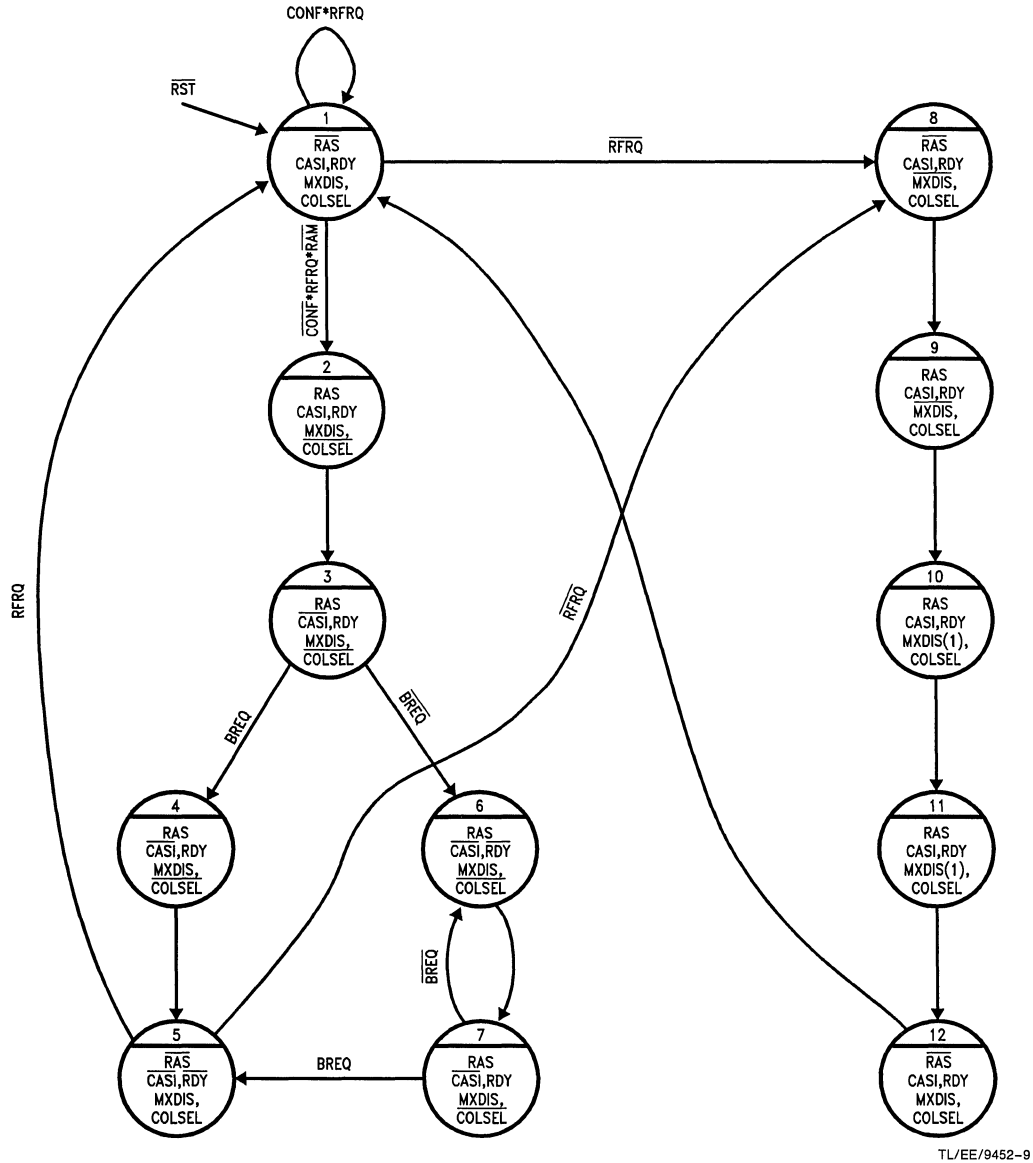
A9
A10
A11
A12
A13
I/O0
I/O1
I/O2
I/O3
WE
OE
CE

TL/EE/9452-17

Appendix C

State Diagram of the Simple DRAM Interface



TL/EE/9452–9

Note 1: MXDIS and COLSEL are Don't Care in these states.

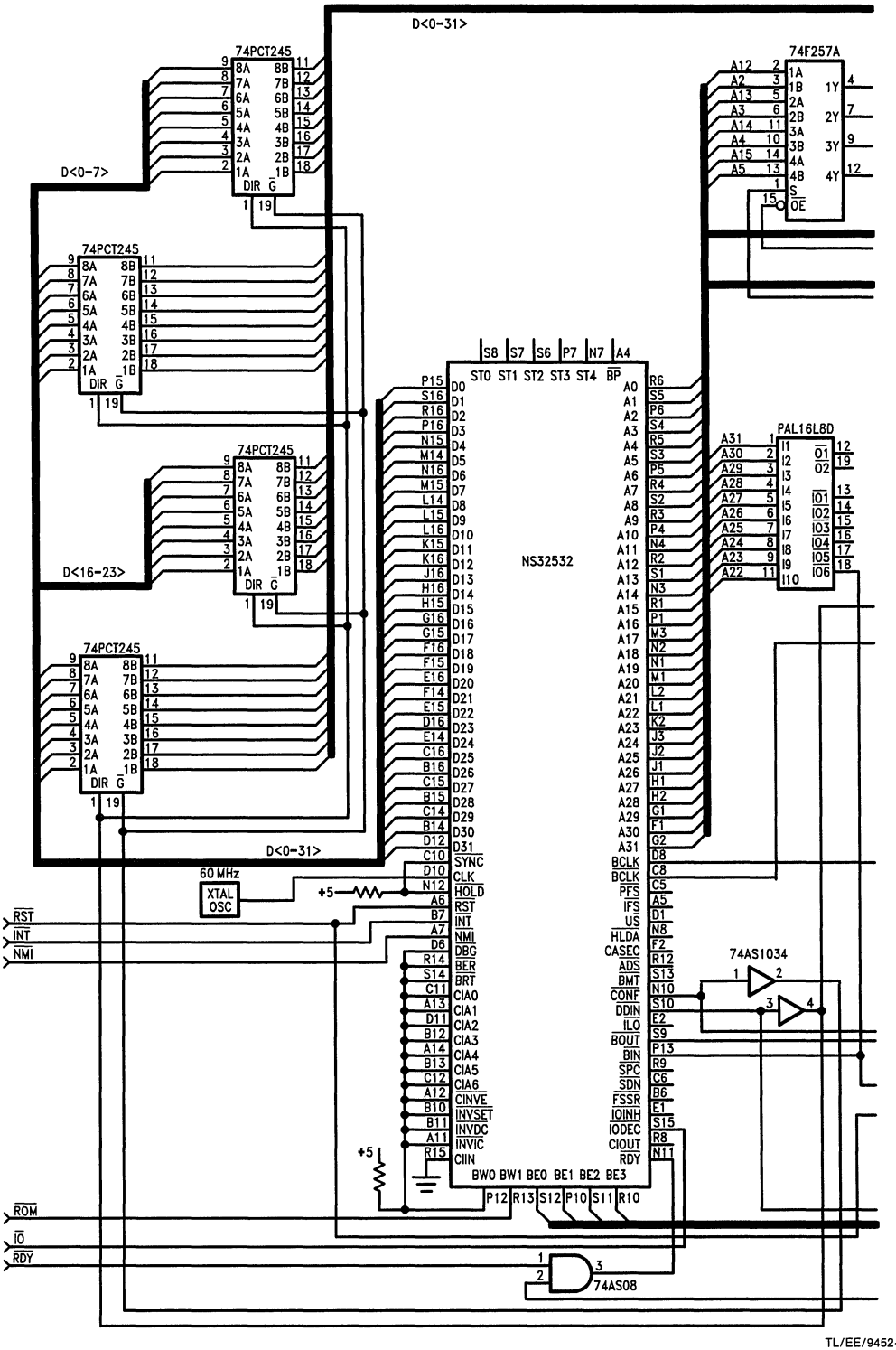
```
PAL16R8D
STATE MACHINE PAL
STATE MACHINE FOR DRAM CONTROLLER
NATIONAL SEMICONDUCTOR, SANTA CLARA, CALIFORNIA
CLK RFRQ CONF BREQ RAM NC IRST NC NC GND
OE A B NC C D E F G VCC
/A := A * B * /C * D * E * F * G * /RFRQ + A * B * /C * D * E * /F * /G * /RFRQ
      + /A * B * /C * D * E * F * G + /A * B * C * /D * E * F * G
/B := A * B * /C * D * E * F * G * /CONF * RFRQ * /RAM + A * /B * C * /D * E * /F * G * BREQ
      + A * /B * C * D * E * F * G + A * /B * C * D * E * /F * /G + A * /B * C * /D * /F * G * /BREQ
/C := A * B * /C * D * E * /F * /G * RFRQ + A * B * /C * D * E * F * G * CONF * RFRQ + /RST
      + A * B * /D * E * F * G + A * /B * C * D * /E * /F * G + A * /B * C * /D * /E * /F * G * BREQ
      + A * B * /C * D * E * F * G * /RFRQ + A * B * /C * D * E * /F * /G * /RFRQ
/D := A * /B * C * D * E * F * G + A * /B * C * D * E * /F * /G + /A * B * /C * D * E * F * G
      + /A * B * C * D * /E * F * G + A * B * C * /D * E * F * G
/E := A * /B * C * /D * E * /F * G * BREQ + A * /B * C * D * E * /F * /G + /A * B * C * /D * E * F * G
/F := A * /B * C * D * E * F * G + A * /B * C * /E * /F * G + A * /B * C * D * E * /F * /G
      + A * /B * C * /D * /F * G
/G := A * /B * C * /E * /F * G + A * /B * C * /D * /F * G * /BREQ

PAL16L8D
/CASn PAL
GENERATES /CASn FOR DRAM BANKS
NATIONAL SEMICONDUCTOR, SANTA CLARA, CALIFORNIA
NC CASI DDIN NC BE0 BE1 BE2 BE3 NC GND
NC NC CAS0 CAS1 CAS2 CAS3 NC NC NC VCC
/CAS0 = /CASI * /DDIN + /CASI * /BE0 * DDIN
/CAS1 = /CASI * /DDIN + /CASI * /BE1 * DDIN
/CAS2 = /CASI * /DDIN + /CASI * /BE2 * DDIN
/CAS3 = /CASI * /DDIN + /CASI * /BE3 * DDIN

PAL16L8D
ADDRESS DECODE PAL
ADDRESS DECODER FOR DRAM INTERFACE
NATIONAL SEMICONDUCTOR, SANTA CLARA, CALIFORNIA
A31 A30 A29 A28 A27 A26 A25 A24 A23 GND
A22 RAM RAML RAMU NC NC NC NC NC VCC
/RAM  = /A31 * /A30 * /A29 * /A28 * /A27 * /A26 * /A25 * /A24 * /A23
/RAML = /A31 * /A30 * /A29 * /A28 * /A27 * /A26 * /A25 * /A24 * /A23 * /A22
/RAMU = /A31 * /A30 * /A29 * /A28 * /A27 * /A26 * /A25 * /A24 * /A23 * /A22
```

```
PAL20X10A
REFRESH INTERVAL COUNTER
30 MHZ REFRESH INTERVAL COUNTER PAL
NATIONAL SEMICONDUCTOR, SANTA CLARA, CALIFORNIA
BCLK NC NC NC NC NC NC NC NC RFACK GND
OE Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7 NC RFRQ VCC
/Q0     :=  /Q0 + /Q7 * /Q6 * /Q5
            :+: VCC
/Q1     :=  /Q1 + /Q7 * /Q6 * /Q5
            :+: /Q7 * /Q6 * /Q5 + /Q0
/Q2     :=  /Q2 + /Q7 * /Q6 * /Q5
            :+: /Q7 * /Q6 * /Q5 + /Q1 + /Q0
/Q3     :=  /Q3 + /Q7 * /Q6 * /Q5
            :+: /Q7 * /Q6 * /Q5 + /Q2 * /Q1 * /Q0
/Q4     :=  /Q4 + /Q7 * /Q6 * /Q5
            :+: /Q7 * /Q6 * /Q5 + /Q3 * /Q2 * /Q1 * /Q0
/Q5     :=  /Q5 + /Q7 * /Q6 * /Q5
            :+: /Q7 * /Q6 * /Q5 + /Q4 * /Q3 * /Q2 * /Q1 * /Q0
/Q6     :=  /Q6 + /Q7 * /Q6 * /Q5
            :+: /Q7 * /Q6 * /Q5 + /Q5 * /Q4 * /Q3 * /Q2 * /Q1 * /Q0
/Q7     :=  /Q7 + /Q7 * /Q6 * /Q5
            :+: /Q7 * /Q6 * /Q5 + /Q6 * /Q5 * /Q4 * /Q3 * /Q2 * /Q1 * /Q0
/RFRQ   :=  RFRQ * Q7 * Q6 * Q5 * Q4 * Q3 * Q2 * Q1 * Q0 + /RFRQ * /RFACK
            :+: /RFRQ

PAL20X10A
REFRESH ADDRESS COUNTER
REFRESH ADDRESS GENERATOR FOR DRAM BANKS
NATIONAL SEMICONDUCTOR, SANTA CLARA, CALIFORNIA
CLK NC NC NC NC NC NC NC NC NC GND
OE A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 VCC
/A0 :=  /A0 :+: VCC
/A1 :=  /A1 :+: A0
/A2 :=  /A2 :+: A1 * A0
/A3 :=  /A3 :+: A2 * A1 * A0
/A4 :=  /A4 :+: A3 * A2 * A1 * A0
/A5 :=  /A5 :+: A4 * A3 * A2 * A1 * A0
/A6 :=  /A6 :+: A5 * A4 * A3 * A2 * A1 * A0
/A7 :=  /A7 :+: A6 * A5 * A4 * A3 * A2 * A1 * A0
/A8 :=  /A8 :+: A7 * A6 * A5 * A4 * A3 * A2 * A1 * A0
/A9 :=  /A9 :+: A8 * A7 * A6 * A5 * A4 * A3 * A2 * A1 * A0
```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74PCT245
74PCT245
D<16-23>
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D<0-31>
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PAL16L8D
NS32532
ST0 ST1 ST2 ST3 ST4 BP
S8 S7 S6 P7 N7 A4
60 MHz
XTAL OSC
+5
RST
INT
NMI
ROM
IO
RDY
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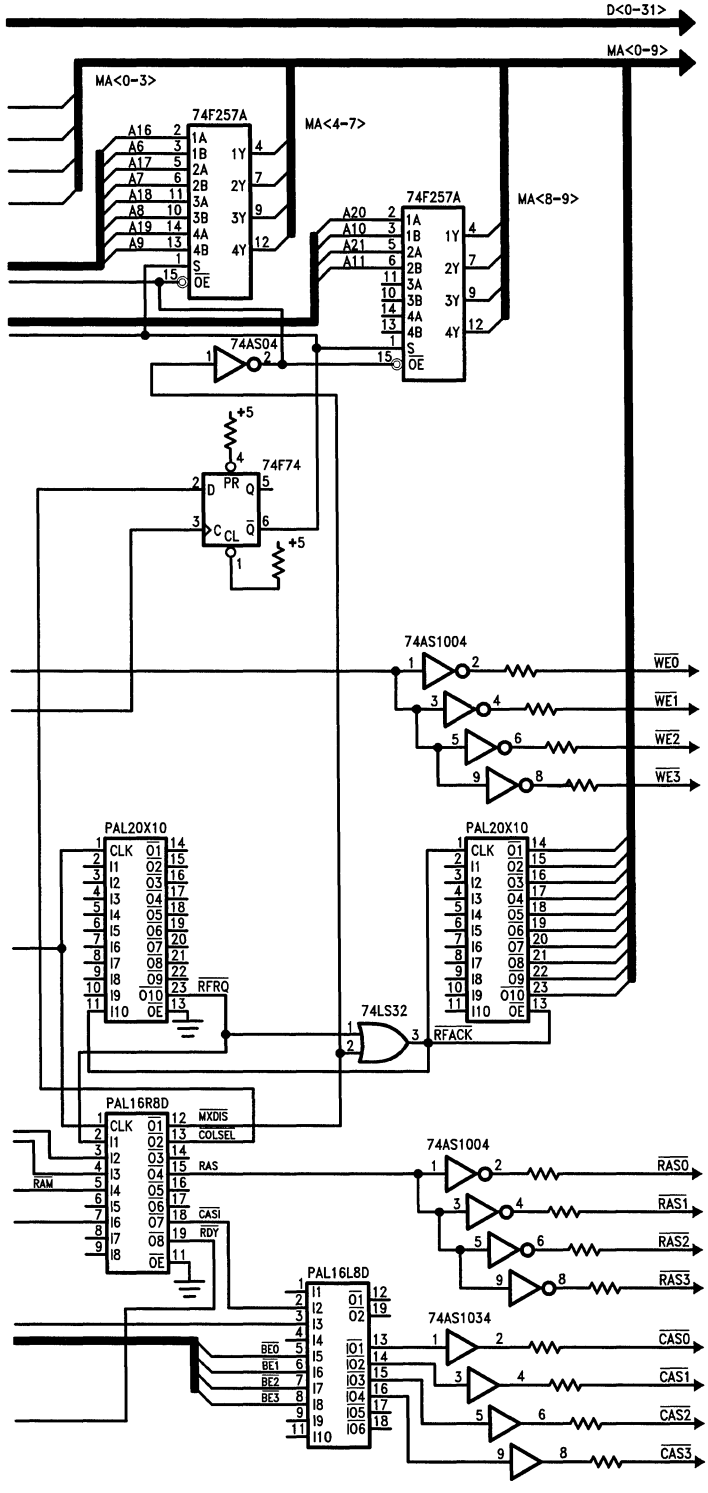
74AS08
BW0 BW1 BE0 BE1 BE2 BE3
P12 R13 S12 P10 S11 R10
TL/EE/9452-18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MA<8-9>
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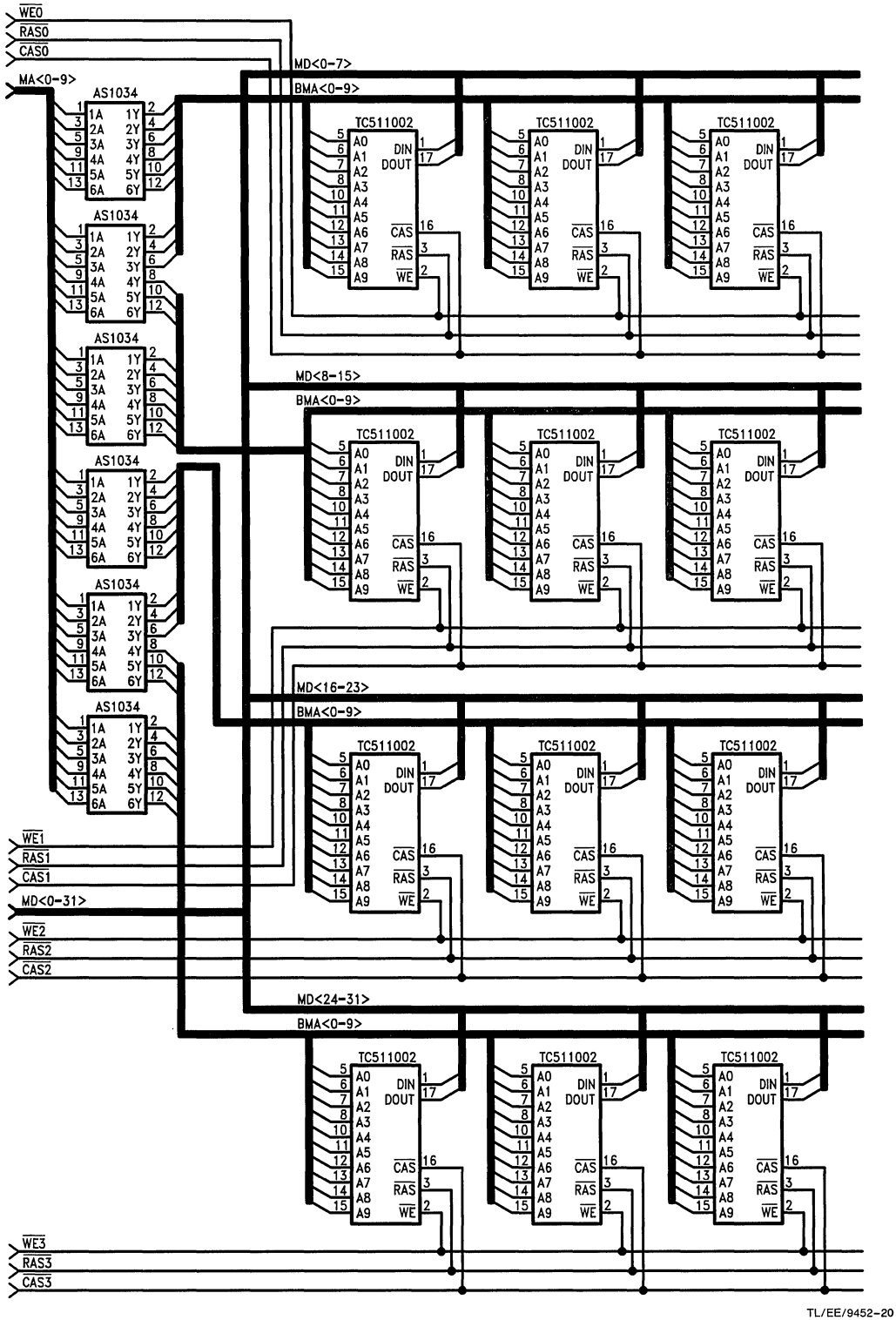
74F257A
74AS04
+5
74F74
74AS1004
WE0
WE1
WE2
WE3
PAL20X10
PAL20X10
RFRQ
74LS32
RFACK
PAL16R8D
MXDIS
COLSEL
RAM
RAS
CASI
RDY
74AS1004
RAS0
RAS1
RAS2
RAS3
PAL16L8D
BE0
BE1
BE2
BE3
74AS1034
CAS0
CAS1
CAS2
CAS3

TL/EE/9452-19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RAS0
CAS0
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AS1034
MD<0-7>
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DOUT
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WE
MD<8-15>
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MD<16-23>
BMA<0-9>
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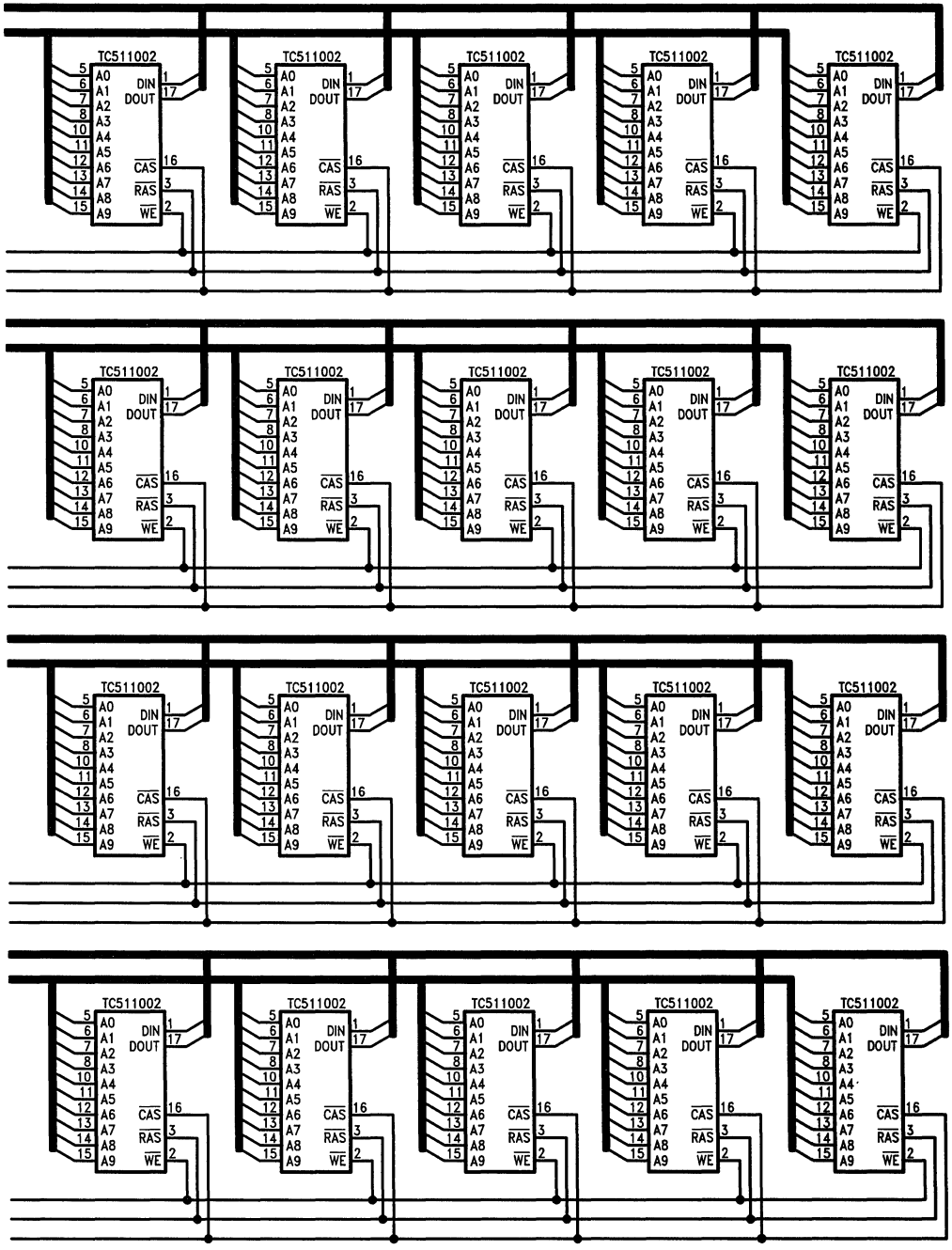
RAS1
CAS1
MD<0-31>
WE2
RAS2
CAS2
MD<24-31>
BMA<0-9>
WE3
RAS3
CAS3

TL/EE/9452-20



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Introduction to Bresenham's Line Algorithm Using the SBIT Instruction; Series 32000® Graphics Note 5

National Semiconductor
Application Note 524
Nancy Cossitt

1.0 INTRODUCTION

Even with today's achievements in graphics technology, the resolution of computer graphics systems will never reach that of the real world. A true real line can never be drawn on a laser printer or CRT screen. There is no method of accurately printing all of the points on the continuous line described by the equation $y = mx + b$. Similarly, circles, ellipses and other geometrical shapes cannot truly be implemented by their theoretical definitions because the graphics system itself is discrete, not real or continuous. For that reason, there has been a tremendous amount of research and development in the area of discrete or raster mathematics. Many algorithms have been developed which "map" real-world images into the discrete space of a raster device. Bresenham's line-drawing algorithm (and its derivatives) is one of the most commonly used algorithms today for describing a line on a raster device. The algorithm was first published in Bresenham's 1965 article entitled "Algorithm for Computer Control of a Digital Plotter". It is now widely used in graphics and electronic printing systems. This application note will describe the fundamental algorithm and show an implementation on National Semiconductor's Series 32000 microprocessor using the SBIT instruction, which is particularly well-suited for such applications. A timing diagram can be found in *Figure 8* at the end of the application note.

2.0 DESCRIPTION

Bresenham's line-drawing algorithm uses an iterative scheme. A pixel is plotted at the starting coordinate of the line, and each iteration of the algorithm increments the pixel one unit along the major, or x-axis. The pixel is incremented along the minor, or y-axis, only when a decision variable (based on the slope of the line) changes sign. A key feature of the algorithm is that it requires only integer data and simple arithmetic. This makes the algorithm very efficient and fast.

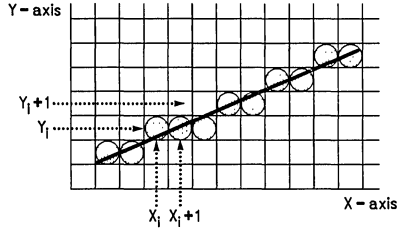

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FIGURE 1

The algorithm assumes the line has positive slope less than one, but a simple change of variables can modify the algorithm for any slope value. This will be detailed in section 2.2.

2.1 Bresenham's Algorithm for 0 < slope < 1

Figure 1 shows a line segment superimposed on a raster grid with horizontal axis X and vertical axis Y. Note that x_i and y_i are the integer abscissa and ordinate respectively of each pixel location on the grid.

Given (x_i, y_i) as the previously plotted pixel location for the line segment, the next pixel to be plotted is either $(x_i + 1, y_i)$ or $(x_i + 1, y_i + 1)$. Bresenham's algorithm determines which of these two pixel locations is nearer to the actual line by calculating the distance from each pixel to the line, and plotting that pixel with the smaller distance. Using the familiar equation of a straight line, $y = mx + b$, the y value corresponding to $x_i + 1$ is

$$y = m(x_i + 1) + b$$

The two distances are then calculated as:

$$d1 = y - y_i$$

$$d1 = m(x_i + 1) + b - y_i$$

$$d2 = (y_i + 1) - y$$

$$d2 = (y_i + 1) - m(x_i + 1) - b$$

and,

$$d1 - d2 = m(x_i + 1) + b - y_i - (y_i + 1) + m(x_i + 1) + b$$

$$d1 - d2 = 2m(x_i + 1) - 2y_i + 2b - 1$$

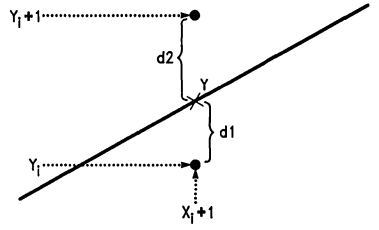
Multiplying this result by the constant dx, defined by the slope of the line $m = dy/dx$, the equation becomes:

$$dx(d1-d2) = 2dy(x_i) - 2dx(y_i) + c$$

where c is the constant $2dy + 2dxb - dx$. Of course, if $d2 > d1$, then $(d1-d2) < 0$, or conversely if $d1 > d2$, then $(d1-d2) > 0$. Therefore, a parameter p_i can be defined such that

$$p_i = dx(d1-d2)$$

$$p_i = 2dy(x_i) - 2dx(y_i) + c$$



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Distances d1 and d2 are compared.
The smaller distance marks next pixel to be plotted.

FIGURE 2

If $p_i > 0$, then d1 > d2 and y_{i+1} is chosen such that the next plotted pixel is $(x_i + 1, y_i)$. Otherwise, if $p_i < 0$, then d2 > d1 and $(x_i + 1, y_i + 1)$ is plotted. (See *Figure 2.*)

Similarly, for the next iteration, p_{i+1} can be calculated and compared with zero to determine the next pixel to plot. If $p_{i+1} < 0$, then the next plotted pixel is at $(x_{i+1} + 1, y_{i+1})$; if $p_{i+1} > 0$, then the next point is $(x_{i+1} + 1, y_{i+1} + 1)$. Note that in the equation for p_{i+1}, $x_{i+1} = x_i + 1$.

$$p_{i+1} = 2dy(x_i + 1) - 2dx(y_{i+1}) + c$$

Subtracting p_i from p_{i+1}, we get the recursive equation:

$$p_{i+1} = p_i + 2dy - 2dx(y_{i+1} - y_i)$$

Note that the constant c has conveniently dropped out of the formula. And, if $p_i < 0$ then $y_{i+1} = y_i$ in the above equation, so that:

$$p_{i+1} = p_i + 2dy$$

or, if $p_i > 0$ then $y_{i+1} = y_i + 1$, and

$$p_{i+1} = p_i + 2(dy-dx)$$

To further simplify the iterative algorithm, constants c1 and c2 can be initialized at the beginning of the program such that c1 = 2dy and c2 = 2(dy−dx). Thus, the actual meat of the algorithm is a loop of length dx, containing only a few integer additions and two compares *(Figure 3).*

2.2 For Slope < 0 and |Slope| > 1

The algorithm fails when the slope is negative or has absolute value greater than one (|dy| > |dx|). The reason for this is that the line will always be plotted with a positive slope if x_i and y_i are always incremented in the positive direction, and the line will always be "shorted" if |dx|<|dy| since the algorithm executes once for every x coordinate (i.e., dx times). However, a closer look at the algorithm must be taken to reveal that a few simple changes of variables will take care of these special cases.

For negative slopes, the change is simple. Instead of incrementing the pixel along the positive direction (+1) for each iteration, the pixel is incremented in the negative direction. The relationship between the starting point and the finishing point of the line determines which axis is followed in the negative direction, and which is in the positive. *Figure 4* shows all the possible combinations for slopes and starting points, and their respective incremental directions along the X and Y axis.

Another change of variables can be performed on the incremental values to accommodate those lines with slopes greater than 1 or less than −1. The coordinate system containing the line is rotated 90 degrees so that the X-axis now becomes the Y-axis and vice versa. The algorithm is then performed on the rotated line according to the sign of its slope, as explained above. Whenever the current position is incremented along the X-axis in the rotated space, it is actually incremented along the Y-axis in the original coordinate space. Similarly, an increment along the Y-axis in the rotated space translates to an increment along the X-axis in the original space. *Figure 4a., g.* and *h.* illustrates this translation process for both positive and negative lines with various starting points.

3.0 IMPLEMENTATION IN C

Bresenham's algorithm is easily implemented in most programming languages. However, C is commonly used for many application programs today, especially in the graphics area. The Appendix gives an implementation of Bresenham's algorithm in C. The C program was written and executed on a SYS32/20 system running UNIX on the NS32032 processor from National. A driver program, also written in C, passed to the function starting and ending points for each line to be drawn. *Figure 6* shows the output on an HP laser jet of 160 unique lines of various slopes on a bit map of 2,000 x 2,000 pixels. Each line starts and ends exactly 25 pixels from the previous line.

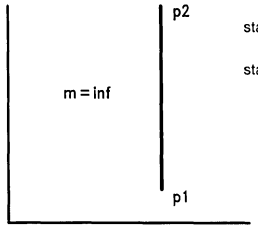
The program uses the variable *bit* to keep track of the current pixel position within the 2,000 x 2,000 bit map *(Figure 5).* When the Bresenham algorithm requires the current position to be incremented along the X-axis, the variable *bit* is incremented by either +1 or −1, depending on the sign of the slope. When the current position is incremented along the Y-axis (i.e., when p > 0) the variable *bit* is incremented by +warp or −warp, where *warp* is the vertical bit displacement of the bit map. The constant *last bit* is compared with *bit* during each iteration to determine if the line is complete. This ensures that the line starts and finishes according to the coordinates passed to the function by the driver program.

```
do while count < > dx
   if (p < 0) then p+ = c1
   else

                    p+ = c2
                    next_y = prev_y + y_inc
   next_x = prev_x + x_inc
   plot(next_x,next_y)
   count + = 1

/* PSEUDO CODE FOR BRESENHAM LOOP */
```

FIGURE 3



start p1: x_inc = y'_inc = 0
y_inc = x'_inc = +1
start p2: x_inc = y'_inc = 0
y_inc = x'_inc = −1

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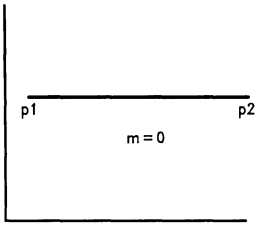
a.



start p1: x_inc = +1
y_inc = 0
start p2: x_inc = −1
y_inc = 0

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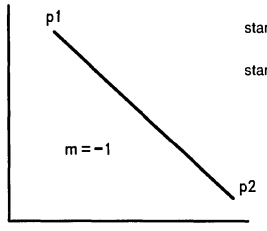
b.



start p1: x_inc = +1
y_inc = −1
start p2: x_inc = −1
y_inc = +1

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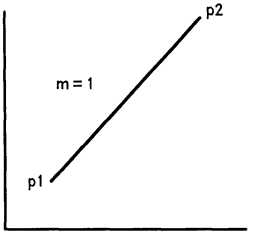
c.



start p1: x_inc = +1
y_inc = +1
start p2: x_inc = −1
y_inc = −1

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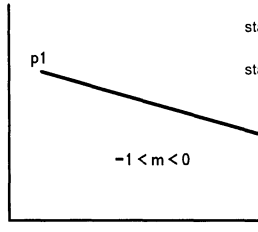
d.



start p1: x_inc = +1
y_inc = −1
start p2: x_inc = −1
y_inc = +1

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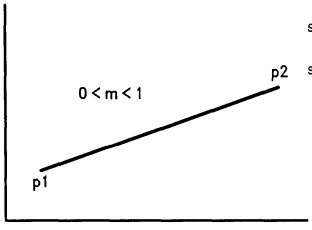
e.



start p1: x_inc = +1
y_inc = +1
start p2: x_inc = −1
y_inc = −1

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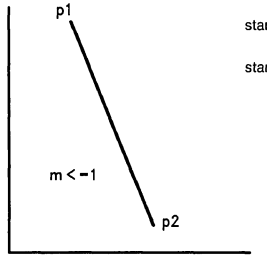
f.



start p1: x_inc = y'_inc = +1
y_inc = x'_inc = −1
start p2: x_inc = y'_inc = −1
y_inc = x'_inc = +1

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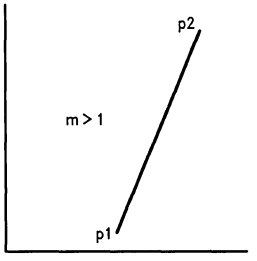
g.



start p1: x_inc = y'_incl = −1
y_inc = x'_inc = +1
start p2: x_inc = y'_inc = +1
y_inc = x'_inc = −1

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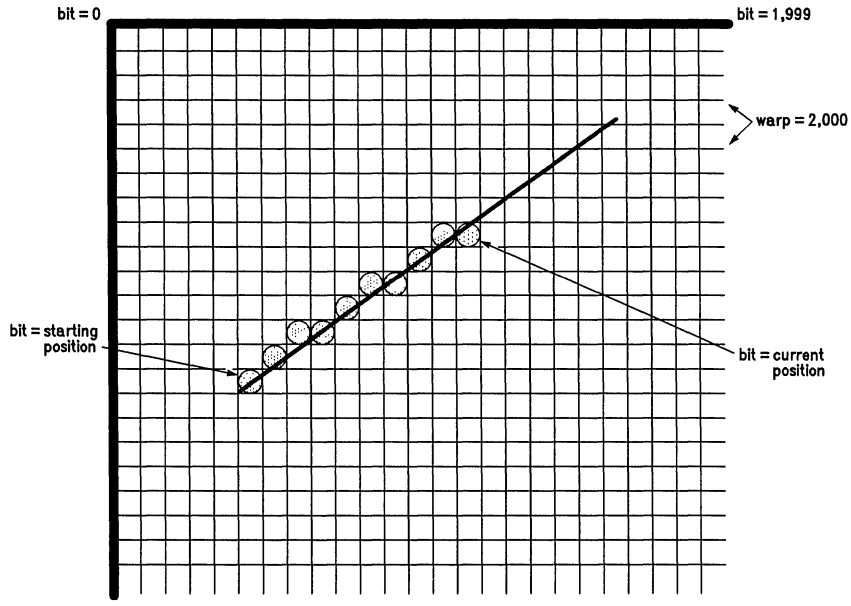
h.

Note: a., g., and h. are rotated 90 degrees left and x', y' refer to the original axis.

FIGURE 4



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Bit Map is 500 kbytes, 2k x 2k Bits
Base Address of Bit Map is 'Bit_Map'

FIGURE 5

Graphics Image (2000 x 2000 Pixels), 300 DPI

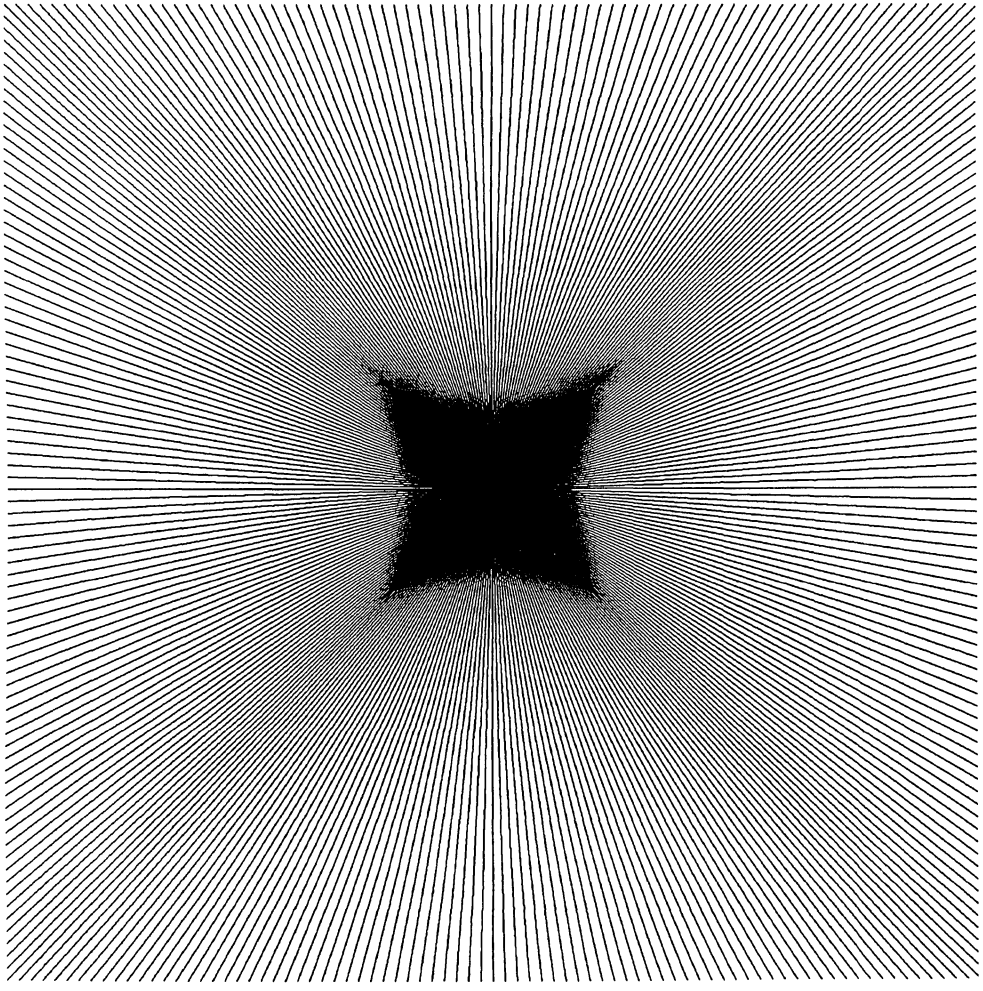

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FIGURE 6. Star-Burst Benchmark—This Star-Burst image was done on a 2k x 2k pixel bit map. Each line is 2k pixels in length and passes through the center of the image, bisecting the square. The lines are 25 pixel units apart, and are drawn using the LINE_DRAW.S routine. There are a total of 160 lines. The total time for drawing this Star-Burst is 2.9 sec on 10 MHz NS32C016.

4.0 IMPLEMENTATION IN SERIES 32000 ASSEMBLY: THE SBIT INSTRUCTION

National's Series 32000 family of processors is well-suited for the Bresenham's algorithm because of the SBIT instruction. *Figure 7* shows a portion of the assembly version of the Bresenham algorithm illustrating the use of the SBIT instruction. The first part of the loop, handles the algorithm for $p < 0$ and .CASE2 handles the algorithm for $p > 0$. The main loop is unrolled in this manner to minimize unnecessary branches (compare loop structure of *Figure 7* to *Figure 3*). The SBIT instruction is used to plot the current pixel in the line.

The SBIT instruction uses *bit_map* as a base address from which it calculates the bit position to be set by adding the offset *bit* contained in register r1. For example, if *bit*, or R1, contains 2,000*, then the instruction:

sbitd r1,@ *bit_map*

will set the bit at position 2,000, given that *bit_map* is the memory location starting at bit 0 of this grid. In actuality, if *base* is a memory address, then the bit position set is:

offset MOD 8

within the memory byte whose address is:

base + (*offset* DIV 8)

So, for the above example,

2,000 MOD 8 = 0

bit_map + 2,000 DIV 8 = *bit_map* + 250

Thus, bit 0 of byte (*bit_map* + 250) is set. This bit corresponds to the first bit of the second row in *Figure 5*.

*All numbers are in decimal.

The SBIT instruction greatly increases the speed of the algorithm. Notice the method of setting the pixel in the C program given in the Appendix:

bit_map[*bit*/8] | = *bit_pos*[(bit & 7)]

This line of code contains a costly division and several other operations that are eliminated with the SBIT instruction. The SBIT instruction helps optimize the performance of the program. Notice also that the algorithm can be implemented using only 7 registers. This improves the speed performance by avoiding time-consuming memory accesses.

5.0 CONCLUSION

An optimized Bresenham line-drawing algorithm has been presented using the SYS32/20 system. Both Series 32000 assembly and C versions have been included. *Figure 8* presents the various timing results of the algorithm. Most of the optimization efforts have been concentrated in the main loop of the program, so the reader may spot other ways to optimize, especially in the set-up section of the algorithm.

Several variations of the Bresenham algorithm have been developed. One particular variation from Bresenham himself relies on "run-length" segments of the line for speed optimization. The algorithm is based on the original Bresenham algorithm, but uses the fact that typically the decision variable p has one sign for several iterations, changing only once in-between these "run-length" segments to make one vertical step. Thus, most lines are composed of a series of horizontal "run-lengths" separated by a single vertical jump. (Consider the special cases where the slope of the line is exactly 1, the slope is 0 or the slope is infinity.) This algorithm will be explored in the NS32CG16 Graphics Note 5, AN-522, "Line Drawing with the NS32CG16", where it will be optimized using special instructions of the NS32CG16.

```
# Main loop of Bresenham algorithm
.LOOP: #p < 0: move in x direction only
                cmpqd           $0,r4
                ble             .CASE2
                addd            r0,r4
                addd            r5,r1
                sbitd           r1,@_bit_map
                cmpd            r3,r1
                bne             .LOOP
                exit            [r3,r4,r5,r6,r7]
                ret             $0
                .align 4
.CASE2: #P > 0: move in x and y direction
                addd            r2,r4
                addd            r7,r1
                addd            r5,r1
                sbitd           r1,@_bit_map
                cmpd            r1,r3
                bne             .LOOP
                exit            [r3,r4,r5,r6,r7]
                ret             $0
```

```
   Register and Memory
        Contents
r0 = c1 constant
r1 = bit current
     position
r2 = c2 constant
r3 = last_bit
r4 = p decision var
r5 = x_inc increment
r6 = unused register
r7 = y_inc increment
_bit_map = address of
first byte in bit map
```

FIGURE 7

Note: Instructions followed by the letter 'd' indicate "double word" operations.

Timing Performance
2k x 2k Bit Map
2k Pix/Vector 160 Lines per Star-Burst

Version	NS32000 Assembly with SBIT	
Parameter	**NS32C016-10**	**NS32C016-15**
Set-up Time Per Vector	45 μs	30 μs
Vectors/Sec	54	82
Pixels/Sec	109,776	164,771
Total Time Star-Burst Benchmark	2.9s	1.9s

FIGURE 8

Set-up time per line is measured from the start of LINE_DRAW.S only. The overhead of calling the LINE_DRAW routine, starting the timer and creating the endpoints of the vector are not included in this time. Set-up time does include all register set-up and branching for the Bresenham algorithm up to the entry point of the main loop.

Vectors/Second is determined by measuring the number of vectors per second the LINE_DRAW routine can draw, not including the overhead of the DRIVER.C and START.C routines, which start the timer and calculate the vector endpoints. All set-up of registers and branching for the Bresenham algorithm are included.

Pixels/Second is measured by dividing the Vectors/Second value by the number of pixels per line.

Total Time for the Star-Burst benchmark is measured from start of benchmark to end. It does include all overhead of START.C and DRIVER.C and all set-up for LINE_DRAW.S. This number can be used to approximate the number of pages per second for printing the whole Star-Burst image.

```
#       National Semiconductor Corporation.
#       CTP version 2.4     -- line_draw.s --

.file   "line_draw.s"
        .comm   _bit_map,49975ø
        .globl  _line_draw
        .set    WARP,2øøø
        .align 4
_line_draw:                             # initialize
        enter   [r3,r4,r5,r6,r7],12
        movd    12(fp),r5               # r5=ys
        movd    8(fp),r6                # r6=xs
        movd    r5,r1                   # initialize starting 'bit'
        muld    $(WARP),r1              # bit=warp*ys+xs
        addd    r6,r1                   # r1=bit
        movd    2ø(fp),r4               # r4=yf
        subd    r5,r4                   # r4=dy
        absd    r4,r3                   # r3=|dy|
        movd    16(fp),r2               # r2=xf
        subd    r6,r2                   # r2=dx
        absd    r2,r6                   # r6=|dx|
        cmpd    r3,r6                   # branch if slope<1
        ble     .LL1                    # must rotate axis for slope>1
        cmpqd   $(ø),r4                 # if dy<ø want x_inc<ø
        bge     .LL2                    # else x_inc is pos
        addr    WARP,r5                 # x_inc=+/-warp because of rotate
        br      .LL3
        .align 4
.LL2:
        addr    -WARP,r5
.LL3:
        cmpqd   $(ø),r2                 # if dx<ø want y_inc<ø
        bge     .LL4                    # else y_inc is pos
        movqd   $(1),r7                 # y_inc=+/-1 becaue of rotate
        br      .LL5
        .align 4
.LL4:
        movqd   $(-1),r7
.LL5:                                   # calculate c1,c2 and p
        movd    r6,rø
        addd    rø,rø                   # rø=c1=2*|dx| because of rotate
        subd    r3,r6                   # r6=|dx-dy|   r2=2*r6=c2
        addr    ø[r6:w],r2              # this muls r6 by 2 and puts in r2
        movd    rø,r4
        subd    r3,r4                   # r4=c2-|dy|=p in rotated space
        movd    2ø(fp),r3               # calculate last_bit
        muld    $(WARP),r3
        addd    16(fp),r3               # r3=last_bit
        br      .LL6
        .align 4
.LL1:                                   # slope<1 use original axis
        cmpqd   $(ø),r4                 # dy determines y_inc
        bge     .LL7
        addr    WARP,r7                 # dy>ø then y_inc=+warp
        br      .LL8
        .align 4
.LL7:
        addr    -WARP,r7                # dy<ø then y_inc=-warp
.LL8:
        cmpqd   $(ø),r2
        bge     .LL9
        movqd   $(1),r5                 # dx>ø then x_inc=+1
        br      .LL1ø
        .align 4
.LL9:
        movqd   $(-1),r5                # dx<ø then x_inc=-1
```

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```
.LL1ø:                                  # calculate c1,c2,p
        addr    ø[r3:w],rø              # rø=2*r3=c1
        movd    r3,r2
        subd    r6,r2
        addd    r2,r2                   # r2=2*|dy-dx|=c2
        movd    rø,r4
        subd    r6,r4                   # p=2*dy-dx=r4
        movd    2ø(fp),r3               # calculate last_bit=r3
        muld    $(WARP),r3
        addd    16(fp),r3
.LL6:                                   # main loop for algorithm
        cmpqd   $(ø),r4                 # check sign of p
        ble     .LL11                   # branch if pos
        addd    rø,r4                   # add c1 to p
        addd    r5,r1                   # inc bit by x_inc only
        sbitd   r1,@_bit_map            # plot bit
        cmpd    r3,r1                   # end only if bit=last_bit
        bne     .LL6
        exit    [r3,r4,r5,r6,r7]
        ret     $(ø)
        .align 4
.LL11:                                  # p>ø then inc in y dir
        addd    r2,r4                   # add c2 to p
        addd    r7,r1                   # add y_inc to bit
        addd    r5,r1                   # add x_inc to bit
        sbitd   r1,@_bit_map            # plot bit
        cmpd    r1,r3                   # end only when bit=last_bit
        bne     .LL6
        exit    [r3,r4,r5,r6,r7]
        ret     $(ø)
```

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```
/* This program calculates points on a line using Bresenham's iterative */
/* method.  */

#include<stdio.h>
#define xbytes   25ø              /* number of bytes along x-axis*/
#define warp     xbytes * 8       /* number of bits along x_axis*/
#define maxy     1999             /* number of lines in y_axis*/
unsigned char   bit_map[xbytes*maxy];   /* array contains bit map*/
static unsigned char    bit_pos[]={1,2,4,8,16,32,64,128};
                                 /* look-up table for setting bit */

line_draw(xs,ys,xf,yf)           /* starting (s) and finishing (f) points */

int     xs,ys,xf,yf;

{
        int     dx,dy,x_inc,y_inc,      /* deltas and increments */
                bit,last_bit,           /* current and last bit positions */
                p,c1,c2;                /* decision variable p and constants */

        dx=xf-xs;
        dy=yf-ys;
        bit=(ys*warp)+xs;               /* initialize bit to first bit pos */
        last_bit=(yf*warp)+xf;          /* calculate last bit on line */

        if (abs(dy) > abs(dx))
        {                               /* abs(slope)>1 must rotate space */
                                        /* see Figure 5 a.,g.,and h. */
                if (dy>ø)
                        x_inc=warp;     /* x_axis is now original y_axis */
                else
                        x_inc= -warp;
                if (dx>ø)
                        y_inc=1;        /* y_axis is now original x_axis */
                else
                        y_inc= -1;
                c1=2*abs(dx);           /* calculate Bresenham's constants */
                c2=2*(abs(dx)-abs(dy));
                p=2*abs(dx)-abs(dy);    /* p is decision variable now rotated */
        }
        else {                          /* abs(slope)<1 use original axis */
                if (dy>ø)
                        y_inc=warp;     /* y_inc is +/-warp number of bits */
                else
                        y_inc= -warp;
                if (dx>ø)
                        x_inc=1;        /* move forward one bit */
                else
                        x_inc= -1;      /* or backward one bit */
                c1=2*abs(dy);           /* calculate constants and p */
                c2=2*(abs(dy)-abs(dx));
                p=2*abs(dy)-abs(dx);
        }

/* Bresenham's Algorithm */
                do      /* do once for each x increment, i.e. dx times */
                {
                        if (p<ø)                /* no y movement if p<ø */
                                p+=c1;
                        else {                  /* move in y dir if p>ø */
                                p+=c2;
                                bit+=y_inc;
                        }
                        bit+=x_inc;             /* always increment x */

                        /* bit is set by calculating bit MOD 8, which is */
```

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```
                        /* same as bit & 7, then looking up appropriate  */
                        /* bit in table bit_pos.  This bit pos is then set */
                        /* in byte bit/8 */

                        bit_map[bit/8] |= bit_pos[(bit&7)];
                } while (bit!=last_bit);
```

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```
 /* Program driver.c feeds line vectors to LINE_DRAW.S forming Star-Burst.   */

#include <stdio.h>
#define xbytes  25ø
#define maxx    1999
#define maxy    1999

unsigned char   bit_map[xbytes*maxy];

main()

{
    int i,count;

/* generate Star-Burst image */

        for (count=1;count<=1øøø;test++){

                for (i=ø;i<=maxy;i+=25)
                        line_draw(ø,i,maxx,maxy-i);
                for (i=ø;i<=maxx;i+=25)
                        line_draw(i,maxy,maxx-i,ø);
        }

}
```

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```
/* Start timer and call main procedure of DRIVER.C to draw lines */

start() {
    long *timer = (long *) øx6øø;
    *timer = ø;             /* write a zero to timer location */
                main(ø,ø);      /* Show argc as zero, argv ->ø */
    return(*timer);     /* return, in rø, the current time */
}
```

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Block Move Optimization Techniques Series 32000® Graphics Note 2

National Semiconductor
Application Note 526
Dave Rand

1.0 INTRODUCTION

This application note discusses fast methods of moving data in printer applications using the National Semiconductor Series 32000. Typically this data is moved to or from the band of RAM representing a small portion (or slice) of the total image. The length of data is fixed. The controller design may require moving data every few milliseconds to image the page, until a total of 1 page has been moved. This may be (at 300 DPI, for example) (8.5 × 300) × (11 × 300), or 1,051,875 bytes. In current controller designs the width is often rounded to a word boundary (usually 320 bytes at 300 DPI). This technique uses 1,056,000 bytes, or 528,000 words.

2.0 DESCRIPTION

The move string instructions (MOVSi) in the 32000 are very powerful, however, when all that is needed is a string copy, they may be overkill. The string instructions include string translation, conditionals and byte/word/double sizes. If the application needs only to move a block of data from one location to another, and that data is a known size (or at least a multiple of a known size), using unrolled MOVD instructions is a faster way of moving the data from A to B on the NS32032 and NS32332.

3.0 IMPLEMENTATION

A code sample follows which makes use of a block size of 128 bytes. To move 256 bytes, for example, R0 should contain 2 on entry.

```
; Version 1.0  Sun Mar 29 12:57:20 1987
;
;A subroutine to move blocks of memory. Uses a granularity of
;128 bytes.
;
;       Inputs:
;               r0 = number of 128 byte blocks to move
;               r1 = source block address
;               r2 = destination block address
;
;Listing continues on following page
;
```

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```
;       Outputs:
;               r0 = 0
;               r1 = source block address + (128 * blocks)
;               r2 = destination block address + (128 * blocks)
;
;Notes:
;       This algorithm corresponds closely to the MOVSD instruction,
;       except that r0 contains the number of 128 byte blocks, not
;       4 byte double words. The output values are the same as if a
;       MOVSD instruction were used.
;
movmem: cmpqd   0,r0            ;if no blocks to move
        beq     mvexit          ;exit now.
        .align  4
mvlp1:  movd    0(r1),0(r2)     ;move one block of data
        movd    4(r1),4(r2)
        movd    8(r1),8(r2)
        movd    12(r1),12(r2)
        movd    16(r1),16(r2)
        movd    20(r1),20(r2)
        movd    24(r1),24(r2)
        movd    28(r1),28(r2)
        movd    32(r1),32(r2)
        movd    36(r1),36(r2)
        movd    40(r1),40(r2)
        movd    44(r1),44(r2)
        movd    48(r1),48(r2)
        movd    52(r1),52(r2)
        movd    56(r1),56(r2)
        movd    60(r1),60(r2)
        movd    64(r1),64(r2)
        movd    68(r1),68(r2)
        movd    72(r1),72(r2)
        movd    76(r1),76(r2)
        movd    80(r1),80(r2)
        movd    84(r1),84(r2)
        movd    88(r1),88(r2)
        movd    92(r1),92(r2)
        movd    96(r1),96(r2)
        movd    100(r1),100(r2)
        movd    104(r1),104(r2)
        movd    108(r1),108(r2)
        movd    112(r1),112(r2)
        movd    116(r1),116(r2)
        movd    120(r1),120(r2)
        movd    124(r1),124(r2)
        addr    128(r1),r1      ;quick way of adding 128
        addr    128(r2),r2
        acbd    -1,r0,mvlp1     ;loop for rest of blocks
mvexit: ret     $0
```

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4.0 TIMING

All timing assumes word aligned data (double word aligned for 32-bit bus). Unaligned data is permitted, but will reduce the speed.

On the 32532 (no wait states, @ 30 MHz, 32-bit bus), this code executes in 204 clocks, assuming burst mode access is available. To move 256 bytes, this routine would take 13.6 μs. The MOVSD instruction takes about 156 clocks to move a 128-byte block. The MOVSD instruction is the best choice, therefore, on the 32532.

On the 32332 (no wait states, @ 15 MHz, 32-bit bus), this code executes in 458 clocks per 128-byte block. Thus, to move 256 bytes, this algorithm takes 61.1 μs. The loop overhead (the ADDR and ACBD instructions) is about 10%. Doubling the block size (to 256 bytes) would reduce the loop overhead to 5%, and reducing the block size (to 64 bytes) would increase the loop overhead to 20%. In comparison, the 32332 MOVSD instruction takes about 721 clocks to move a 128-byte block.

On the 32032 (no wait states. @ 10 MHz, 32-bit bus), this code executes in 634 clocks per 128-byte block. Thus, to move 256 bytes, this algorithm takes 126.8 μs. The loop overhead (the ADDR and ACBD instructions) is about 5%. Doubling the block size (to 256 bytes) would reduce the loop overhead to 2.5%, and reducing the block size (to 64 bytes) would increase the loop overhead to 10%. In comparison, the 32032 MOVSD instruction takes about 690 clocks to move a 128-byte block.

On the 32016 (1 wait state. @ 10 MHz, 16-bit bus), this code executes in 1150 clocks per 128-byte block. Thus, to move 256 bytes, this algorithm takes 230.0 μs. The loop overhead on the 32016 is about 2.5%. In comparison, the 32016 MOVSD instruction would take about 1,074 clocks. Thus, the MOVSD instruction is faster, and makes better use of the available bus bandwidth of the NS32016.

5.0 CONCLUSIONS

The MOVSi instructions on the NS32016 provide a very fast memory block move capability, with variable size. On the NS32332 and NS32032, however, unrolled MOVD instructions are faster due to the larger bus bandwidth of the NS32332 and NS32032.

Clearing Memory with the 32000; Series 32000® Graphics Note 3

National Semiconductor
Application Note 527
Dave Rand

1.0 INTRODUCTION

In printer applications, large amounts of RAM may need to be initialized to a zero value. This application note describes a fast method.

2.0 DESCRIPTION

While several different methods of initializing memory to all zeros are available, here is one that works very well on the Series 32000. While the current version clears memory only in blocks of 128 bytes, other block sizes are possible by extending the algorithm.

3.0 IMPLEMENTATION

This routine is written to clear blocks of 128 bytes. This provides an optimal tradeoff between loop size (granularity) and loop overhead. This can be modified to use a different size. For example, to use a block size of 64 bytes, simply delete 16 of the MOVQD 0,TOS instructions from the listing. As well, since the value of r1 is now the number of 64 byte groups, one of the ADDD R2,R2 instructions (prior to the loading of the stack pointer) must be removed. Since the 32000 has two stacks, interrupts will be handled properly using this code. If only a fixed buffer size needs to be cleared, the code can be further unrolled to clear that area (i.e., increase the number of MOVQD 0,TOS instructions.)

```
; Version 1.1  Sun Mar 29 10:22:19 1987
;
;Subroutine to clear a block of memory. The granularity of this
;algorithm is 128 bytes, to reduce the looping overhead.
;
;       Inputs:
;               r0 = start of block
;               r1 = number of 128-byte groups to clear
;
;       Outputs:
;               All registers preserved.
;
;
;Listing continues on following page
;
```

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```
clram:  cmpqd   0,r1            ;any blocks to clear?
        beq     clexit:w        ;no, exit now.
        save    [r0,r1,r2]      ;save our working registers
        movd    r1,r2           ;here we set r0 = r0 + (r1 * 128) + 4
        addd    r2,r2           ;length *= 2
        addd    r2,r2           ;*4
        addd    r2,r2           ;*8
        addd    r2,r2           ;*16
        addr    4(r0)[r2:q],r0  ;get starting point + 4
        sprd    sp,r2           ;save current stack
        lprd    sp,r0           ;move to last double
        .align  4
cl2:    movqd   0,tos           ;clear a double
        movqd   0,tos
        movqd   0,tos
        movqd   0,tos
        movqd   0,tos
        movqd   0,tos
        movqd   0,tos
        movqd   0,tos
        movqd   0,tos
        movqd   0,tos
        movqd   0,tos
        movqd   0,tos
        movqd   0,tos
        movqd   0,tos
        movqd   0,tos
        movqd   0,tos
        movqd   0,tos
        movqd   0,tos
        movqd   0,tos
        movqd   0,tos
        movqd   0,tos
        movqd   0,tos
        movqd   0,tos
        movqd   0,tos
        movqd   0,tos
        movqd   0,tos
        movqd   0,tos
        movqd   0,tos
        movqd   0,tos
        movqd   0,tos
        movqd   0,tos
        movqd   0,tos
        acbd    -1,r1,cl2
        lprd    sp,r2          ;restore stack pointer
        restore [r0,r1,r2]     ;restore our saved registers
clexit: ret     0
```

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FIGURE 1

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```
clram:  cmpqd   0,r1            ;any blocks to clear?
        beq     clexit:w        ;no, exit now.
        .align  4
cl2:    movqd   0,00(r0)                ;clear a double
        movqd   0,04(r0)
        movqd   0,08(r0)
        movqd   0,12(r0)
        movqd   0,16(r0)
        movqd   0,20(r0)
        movqd   0,24(r0)
        movqd   0,28(r0)
        movqd   0,32(r0)
        movqd   0,36(r0)
        movqd   0,40(r0)
        movqd   0,44(r0)
        movqd   0,48(r0)
        movqd   0,52(r0)
        movqd   0,56(r0)
        movqd   0,60(r0)
        movqd   0,64(r0)
        movqd   0,68(r0)
        movqd   0,72(r0)
        movqd   0,76(r0)
        movqd   0,80(r0)
        movqd   0,84(r0)
        movqd   0,88(r0)
        movqd   0,92(r0)
        movqd   0,96(r0)
        movqd   0,100(r0)
        movqd   0,104(r0)
        movqd   0,108(r0)
        movqd   0,112(r0)
        movqd   0,116(r0)
        movqd   0,120(r0)
        movqd   0,124(r0)
        addd    $128,r0
        acbd    -1,r1,cl2
clexit: ret     0
```

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FIGURE 2

4.0 TIMING RESULTS

On the NS32016, NS32032 and NS32332, 4 clock cycles per write are required. To clear one page of 300 DPI 8½ x 11 (1,056,000 bytes), for example, requires 264,000 double words to be written. The optimal time for this, using 100% of the bus bandwidth on a 16 bit bus, would be 528,000 * 400 ns, or 211.2 ms, @ 10 MHz. All timing data assumes word aligned data (double word aligned for 32 bit bus). Unaligned data is permitted, but will reduce the speed somewhat.

On the NS32332 (no wait states. @15 MHz, 32 bit bus), this code clears the full page image in 178 ms.

On the NS32032 (no wait states. @10 MHz, 32 bit bus), this code clears the full page image in 324 ms.

On the NS32016 (1 wait state. @10 MHz, 16 bit bus), this code clears the full page image in 509 ms.

Doubling the block size (to 256 bytes) would increase the speed by 1%–2%, on the code sample.

On the NS32532, a better approach is to use the register indirect method of referencing memory, as is shown in *Figure 2*. With this approach, the page memory can be cleared in 19 ms, assuming a no wait state 30 MHz system, with a 32 bit bus. The optimal time, using 100% of the bus bandwidth of the NS32532 (2 clock bus cycle) would be 264,000 * 66.6 ns, or 17.6 ms.

Image Rotation Algorithm Series 32000® Graphics Note 4

National Semiconductor
Application Note 528
Dave Rand

1.0 INTRODUCTION

Fast image rotation of 90 and 270 degrees is important in printer applications, since both Portrait and Landscape orientation printing may be desired. With a fast image rotation algorithm, only the Portrait orientation fonts need to be stored. This minimizes ROM storage requirements.

This application note shows a fast image rotation algorithm that may be used to rotate an 8 pixel by 8 line image. Larger image sizes may be rotated by successive application of the rotation primitive.

2.0 DESCRIPTION

This Rotate Image algorithm (developed by the Electronic Imaging Group at National Semiconductor) does a very fast 8 by 8 (64 bit) rotation of font data. Note also that this algorithm does not exclusively deal with fonts, but any 64 bit image. Larger images can be rotated by breaking the image down into 8 x 8 segments, and using a 'source warp' constant to index into the source data.

The source data is pointed to by R0 on entry. A 'source warp' is contained in R1, and is added to R0 after each read of the source font. This allows the rotation of 16 by 16, 32 by 32 and larger fonts.

ROTIMG deals with the 8 by 8 destination character as 8 sequential bytes in two registers (R2 and R3), as follows:

Destination Font Matrix

Low Address

1				
2				
3				
4	= R2	4	3	2	1
5	= R3	8	7	6	5
6				
7				
8				

High Address

ROTIMG uses an external table (a pointer to the start of the table is located in register R4) to speed the rotation and to minimize the code. This table consists of 256 64 bit entries, or a total of 2,048 bytes. The table may be located code (PC) or data (SB) relative. The complete table is at the end of this document (see *Figure 1*). A few entries of the table are reproduced above.

Entry	Definition
0	0x00000000 00000000
1	0x00000000 00000001
2	0x00000000 00000100
3	0x00000000 00000101
. . .	
253	0x01010101 01010001
254	0x01010101 01010100
255	0x01010101 01010101

The bytes in the table are standard LSB to MSB format. Since there is no quad-byte assembler pseudo-op (other than LONG, which is floating point), we must reverse the 'double' declaration to get the correct byte ordering, as is shown below:

Entry	Definition
0	double 0,0
1	double 1,0
2	double 256,0
3	double 257,0
. . .	
253	double 16842753,16843009
254	double 0x01010100,0x01010101
255	double 0x01010101,0x01010101

Each byte within each eight byte table entry represents one bit of output data. By indexing into the table, and ORing the table's contents with R2 and R3, we set the destination byte if the corresponding source bit is set. In this manner, the character is rotated.

3.0 IMPLEMENTATION

What we are doing is setting the LS Bit of the destination byte if the source bit corresponding to that byte is set. We then shift the entire 64 bit destination left one bit, and repeat this process until we have set all eight bits, and processed all eight bytes of source information.

The source data for an 8 by 8 character ">" appears below:

Character Table for '>'

	Bit Number	Hex Value
	0 1 2 3 4 5 6 7	
Byte	0 0 1 0 0 0 0 0 0	02
	1 0 0 1 0 0 0 0 0	04
	2 0 0 0 1 0 0 0 0	08
	3 0 0 0 0 1 0 0 0	10
	4 0 0 0 0 1 0 0 0	10
	5 0 0 0 1 0 0 0 0	08
	6 0 0 1 0 0 0 0 0	04
	7 0 1 0 0 0 0 0 0	02

The ROTIMG algorithm, expressed in 32000 code, appears below:

```
#
#
#Rotate image emulation code
#
#    Inputs:
#         R0 = Source font address
#         R1 = Source font warp
#         R4 = Rotate table address
#
#    Outputs:
#         R2 = Destination font low 4 bytes (lsb->msb, 0 - 3)
#         R3 = Destination font high 4 bytes (lsb->msb, 4 - 7)
#
ROTIMG:   save [r0,r5,r6,r7]      #save registers we will use
          movqd    0,r2           #clear destination font
          movd     r2,r3          #clear high bits of dest.
          movd     r2,r5          #clear high bits of temp.
          addr     8,r6           #deal with 8 bytes of src.
rotlp:    movb     0(r0),r5       #get a byte of source
          addd     r1,r0          #add source warp
          addd     r2,r2          #shift destination left one bit
          addd     r3,r3          #top 32 bits too
          addrd    r4[r5:q],r7    #get pointer to table
          ord      0(r7),r2       #or in low bits
          ord      4(r7),r3       #or in high bits
          acbd     -1,r6,rotlp    #and back for more
          restore  [r0,r5,r6,r7]  #restore registers
          ret      $0             #and return
```

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Now, let's look at what happens to the data, given the example font of '>'.

Loop #	Source Font	R3	R2	
0	—	00000000	00000000	;0 destination
1	02 hex	00000000	00000100	;first bits in
2	04	00000000	00010200	;next bits in
3	08	00000000	01020400	;and so on
4	10	00000001	02040800	
5	10	00000003	04081000	
6	08	00000006	09102000	
7	04	0000000C	12214000	
8	02	00000018	24428100	;last iteration

Now, arranging this in the appropriate order gives us:

Destination Character Table for '>', 90 degree

	Bit Number	Hex Value
	0 1 2 3 4 5 6 7	
Byte	0 0 0 0 0 0 0 0 0	00
	1 1 0 0 0 0 0 0 1	81
	2 0 1 0 0 0 0 0 1 0	42
	3 0 0 1 0 0 1 0 0	24
	4 0 0 0 1 1 0 0 0	18
	5 0 0 0 0 0 0 0 0	00
	6 0 0 0 0 0 0 0 0	00
	7 0 0 0 0 0 0 0 0	00

Destination Character Table for '>', 270 degree

	Bit Number	Hex Value
	0 1 2 3 4 5 6 7	
Byte	0 0 0 0 0 0 0 0 0	00
	1 0 0 0 0 0 0 0 0	00
	2 0 0 0 0 0 0 0 0	00
	3 0 0 0 1 1 0 0 0	18
	4 0 0 1 0 0 1 0 0	24
	5 0 1 0 0 0 0 1 0	42
	6 1 0 0 0 0 0 0 1	81
	7 0 0 0 0 0 0 0 0	00

Note that by re-ordering the output data, we may rotate 90 or 270 degrees. This may also be accomplished by using a different table (see *Figure 2*).

4.0 TIMING

With unrolled 32000 code, the time for this algorithm is about 588 clocks on the 32016. Subtracting the font read time from this (about 113 clocks), the actual time for rotation is 475 clocks. On the 32332, the time is about 388 clocks. On the 32532, the unrolled loop time is 120–180 clocks, depending on burst mode availability. Repetition of the character data also affects the 32532, due to the data cache. See *Figure 3* for an unrolled code listing.

This table is used for the ROTIMG code. It is 256 entries of 64 bits each (8 bytes * 256 = 2048 bytes). There are two entries per line. This table is used for 90° rotation.

```
rottab1: .double  0x00000000,0x00000000,0x00000001,0x00000000 ;0,1
         .double  0x00000100,0x00000000,0x00000101,0x00000000 ;2,3
         .double  0x00010000,0x00000000,0x00010001,0x00000000 ;4,5
         .double  0x00010100,0x00000000,0x00010101,0x00000000 ;6,7
         .double  0x01000000,0x00000000,0x01000001,0x00000000 ;...
         .double  0x01000100,0x00000000,0x01000101,0x00000000
         .double  0x01010000,0x00000000,0x01010001,0x00000000
         .double  0x01010100,0x00000000,0x01010101,0x00000000
         .double  0x00000000,0x00000001,0x00000001,0x00000001
         .double  0x00000100,0x00000001,0x00000101,0x00000001
         .double  0x00010000,0x00000001,0x00010001,0x00000001
         .double  0x00010100,0x00000001,0x00010101,0x00000001
         .double  0x01000000,0x00000001,0x01000001,0x00000001
         .double  0x01000100,0x00000001,0x01000101,0x00000001
         .double  0x01010000,0x00000001,0x01010001,0x00000001
         .double  0x01010100,0x00000001,0x01010101,0x00000001
         .double  0x00000000,0x00000100,0x00000001,0x00000100
         .double  0x00000100,0x00000100,0x00000101,0x00000100
         .double  0x00010000,0x00000100,0x00010001,0x00000100
         .double  0x00010100,0x00000100,0x00010101,0x00000100
         .double  0x01000000,0x00000100,0x01000001,0x00000100
         .double  0x01000100,0x00000100,0x01000101,0x00000100
         .double  0x01010000,0x00000100,0x01010001,0x00000100
         .double  0x01010100,0x00000100,0x01010101,0x00000100
         .double  0x00000000,0x00000101,0x00000001,0x00000101
         .double  0x00000100,0x00000101,0x00000101,0x00000101
         .double  0x00010000,0x00000101,0x00010001,0x00000101
         .double  0x00010100,0x00000101,0x00010101,0x00000101
         .double  0x01000000,0x00000101,0x01000001,0x00000101
         .double  0x01000100,0x00000101,0x01000101,0x00000101
         .double  0x01010000,0x00000101,0x01010001,0x00000101
         .double  0x01010100,0x00000101,0x01010101,0x00000101
         .double  0x00000000,0x00010000,0x00000001,0x00010000
         .double  0x00000100,0x00010000,0x00000101,0x00010000
         .double  0x00010000,0x00010000,0x00010001,0x00010000
         .double  0x00010100,0x00010000,0x00010101,0x00010000
         .double  0x01000000,0x00010000,0x01000001,0x00010000
         .double  0x01000100,0x00010000,0x01000101,0x00010000
         .double  0x01010000,0x00010000,0x01010001,0x00010000
         .double  0x01010100,0x00010000,0x01010101,0x00010000
         .double  0x00000000,0x00010001,0x00000001,0x00010001
         .double  0x00000100,0x00010001,0x00000101,0x00010001
         .double  0x00010000,0x00010001,0x00010001,0x00010001
         .double  0x00010100,0x00010001,0x00010101,0x00010001
         .double  0x01000000,0x00010001,0x01000001,0x00010001
         .double  0x01000100,0x00010001,0x01000101,0x00010001
         .double  0x01010000,0x00010001,0x01010001,0x00010001
         .double  0x01010100,0x00010001,0x01010101,0x00010001
         .double  0x00000000,0x00010100,0x00000001,0x00010100
```

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FIGURE 1

```
.double  0x00000100,0x00010100,0x00000101,0x00010100
.double  0x00010000,0x00010100,0x00010001,0x00010100
.double  0x00010100,0x00010100,0x00010101,0x00010100
.double  0x01000000,0x00010100,0x01000001,0x00010100
.double  0x01000100,0x00010100,0x01000101,0x00010100
.double  0x01010000,0x00010100,0x01010001,0x00010100
.double  0x01010100,0x00010100,0x01010101,0x00010100
.double  0x00000000,0x00010101,0x00000001,0x00010101
.double  0x00000100,0x00010101,0x00000101,0x00010101
.double  0x00010000,0x00010101,0x00010001,0x00010101
.double  0x00010100,0x00010101,0x00010101,0x00010101
.double  0x01000000,0x00010101,0x01000001,0x00010101
.double  0x01000100,0x00010101,0x01000101,0x00010101
.double  0x01010000,0x00010101,0x01010001,0x00010101
.double  0x01010100,0x00010101,0x01010101,0x00010101
.double  0x00000000,0x01000000,0x00000001,0x01000000
.double  0x00000100,0x01000000,0x00000101,0x01000000
.double  0x00010000,0x01000000,0x00010001,0x01000000
.double  0x00010100,0x01000000,0x00010101,0x01000000
.double  0x01000000,0x01000000,0x01000001,0x01000000
.double  0x01000100,0x01000000,0x01000101,0x01000000
.double  0x01010000,0x01000000,0x01010001,0x01000000
.double  0x01010100,0x01000000,0x01010101,0x01000000
.double  0x00000000,0x01000001,0x00000001,0x01000001
.double  0x00000100,0x01000001,0x00000101,0x01000001
.double  0x00010000,0x01000001,0x00010001,0x01000001
.double  0x00010100,0x01000001,0x00010101,0x01000001
.double  0x01000000,0x01000001,0x01000001,0x01000001
.double  0x01000100,0x01000001,0x01000101,0x01000001
.double  0x01010000,0x01000001,0x01010001,0x01000001
.double  0x01010100,0x01000001,0x01010101,0x01000001
.double  0x00000000,0x01000100,0x00000001,0x01000100
.double  0x00000100,0x01000100,0x00000101,0x01000100
.double  0x00010000,0x01000100,0x00010001,0x01000100
.double  0x00010100,0x01000100,0x00010101,0x01000100
.double  0x01000000,0x01000100,0x01000001,0x01000100
.double  0x01000100,0x01000100,0x01000101,0x01000100
.double  0x01010000,0x01000100,0x01010001,0x01000100
.double  0x01010100,0x01000100,0x01010101,0x01000100
.double  0x00000000,0x01000101,0x00000001,0x01000101
.double  0x00000100,0x01000101,0x00000101,0x01000101
.double  0x00010000,0x01000101,0x00010001,0x01000101
.double  0x00010100,0x01000101,0x00010101,0x01000101
.double  0x01000000,0x01000101,0x01000001,0x01000101
.double  0x01000100,0x01000101,0x01000101,0x01000101
.double  0x01010000,0x01000101,0x01010001,0x01000101
.double  0x01010100,0x01000101,0x01010101,0x01000101
.double  0x00000000,0x01010000,0x00000001,0x01010000
.double  0x00000100,0x01010000,0x00000101,0x01010000
.double  0x00010000,0x01010000,0x00010001,0x01010000
.double  0x00010100,0x01010000,0x00010101,0x01010000
.double  0x01000000,0x01010000,0x01000001,0x01010000
.double  0x01000100,0x01010000,0x01000101,0x01010000
.double  0x01010000,0x01010000,0x01010001,0x01010000
.double  0x01010100,0x01010000,0x01010101,0x01010000
```

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FIGURE 1 (Continued)

```
.double  0x00000000,0x01010001,0x00000001,0x01010001
.double  0x00000100,0x01010001,0x00000101,0x01010001
.double  0x00010000,0x01010001,0x00010001,0x01010001
.double  0x00010100,0x01010001,0x00010101,0x01010001
.double  0x01000000,0x01010001,0x01000001,0x01010001
.double  0x01000100,0x01010001,0x01000101,0x01010001
.double  0x01010000,0x01010001,0x01010001,0x01010001
.double  0x01010100,0x01010001,0x01010101,0x01010001
.double  0x00000000,0x01010100,0x00000001,0x01010100
.double  0x00000100,0x01010100,0x00000101,0x01010100
.double  0x00010000,0x01010100,0x00010001,0x01010100
.double  0x00010100,0x01010100,0x00010101,0x01010100
.double  0x01000000,0x01010100,0x01000001,0x01010100
.double  0x01000100,0x01010100,0x01000101,0x01010100
.double  0x01010000,0x01010100,0x01010001,0x01010100
.double  0x01010100,0x01010100,0x01010101,0x01010100
.double  0x00000000,0x01010101,0x00000001,0x01010101
.double  0x00000100,0x01010101,0x00000101,0x01010101
.double  0x00010000,0x01010101,0x00010001,0x01010101
.double  0x00010100,0x01010101,0x00010101,0x01010101
.double  0x01000000,0x01010101,0x01000001,0x01010101
.double  0x01000100,0x01010101,0x01000101,0x01010101 ;250,251
.double  0x01010000,0x01010101,0x01010001,0x01010101 ;252,253
.double  0x01010100,0x01010101,0x01010101,0x01010101 ;254,255
```

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FIGURE 1 (Continued)

This table is used for the ROTIMG code. It is 256 entries of 64 bits each (8 bytes * 256 = 2048 bytes). There are two entries per line. This gives a 270° rotation.

```
rottab2:  .double  0x00000000,0x00000000,0x00000000,0x01000000
          .double  0x00000000,0x00010000,0x00000000,0x01010000
          .double  0x00000000,0x00000100,0x00000000,0x01000100
          .double  0x00000000,0x00010100,0x00000000,0x01010100
          .double  0x00000000,0x00000001,0x00000000,0x01000001
          .double  0x00000000,0x00010001,0x00000000,0x01010001
          .double  0x00000000,0x00000101,0x00000000,0x01000101
          .double  0x00000000,0x00010101,0x00000000,0x01010101
          .double  0x01000000,0x00000000,0x01000000,0x01000000
          .double  0x01000000,0x00010000,0x01000000,0x01010000
          .double  0x01000000,0x00000100,0x01000000,0x01000100
          .double  0x01000000,0x00010100,0x01000000,0x01010100
          .double  0x01000000,0x00000001,0x01000000,0x01000001
          .double  0x01000000,0x00010001,0x01000000,0x01010001
          .double  0x01000000,0x00000101,0x01000000,0x01000101
          .double  0x01000000,0x00010101,0x01000000,0x01010101
          .double  0x00010000,0x00000000,0x00010000,0x01000000
          .double  0x00010000,0x00010000,0x00010000,0x01010000
          .double  0x00010000,0x00000100,0x00010000,0x01000100
          .double  0x00010000,0x00010100,0x00010000,0x01010100
          .double  0x00010000,0x00000001,0x00010000,0x01000001
          .double  0x00010000,0x00010001,0x00010000,0x01010001
          .double  0x00010000,0x00000101,0x00010000,0x01000101
          .double  0x00010000,0x00010101,0x00010000,0x01010101
```

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FIGURE 2

```
.double  0x01010000,0x00000000,0x01010000,0x01000000
.double  0x01010000,0x00010000,0x01010000,0x01010000
.double  0x01010000,0x00000100,0x01010000,0x01000100
.double  0x01010000,0x00010100,0x01010000,0x01010100
.double  0x01010000,0x00000001,0x01010000,0x01000001
.double  0x01010000,0x00010001,0x01010000,0x01010001
.double  0x01010000,0x00000101,0x01010000,0x01000101
.double  0x01010000,0x00010101,0x01010000,0x01010101
.double  0x00000100,0x00000000,0x00000100,0x01000000
.double  0x00000100,0x00010000,0x00000100,0x01010000
.double  0x00000100,0x00000100,0x00000100,0x01000100
.double  0x00000100,0x00010100,0x00000100,0x01010100
.double  0x00000100,0x00000001,0x00000100,0x01000001
.double  0x00000100,0x00010001,0x00000100,0x01010001
.double  0x00000100,0x00000101,0x00000100,0x01000101
.double  0x00000100,0x00010101,0x00000100,0x01010101
.double  0x01000100,0x00000000,0x01000100,0x01000000
.double  0x01000100,0x00010000,0x01000100,0x01010000
.double  0x01000100,0x00000100,0x01000100,0x01000100
.double  0x01000100,0x00010100,0x01000100,0x01010100
.double  0x01000100,0x00000001,0x01000100,0x01000001
.double  0x01000100,0x00010001,0x01000100,0x01010001
.double  0x01000100,0x00000101,0x01000100,0x01000101
.double  0x01000100,0x00010101,0x01000100,0x01010101
.double  0x00010100,0x00000000,0x00010100,0x01000000
.double  0x00010100,0x00010000,0x00010100,0x01010000
.double  0x00010100,0x00000100,0x00010100,0x01000100
.double  0x00010100,0x00010100,0x00010100,0x01010100
.double  0x00010100,0x00000001,0x00010100,0x01000001
.double  0x00010100,0x00010001,0x00010100,0x01010001
.double  0x00010100,0x00000101,0x00010100,0x01000101
.double  0x00010100,0x00010101,0x00010100,0x01010101
.double  0x01010100,0x00000000,0x01010100,0x01000000
.double  0x01010100,0x00010000,0x01010100,0x01010000
.double  0x01010100,0x00000100,0x01010100,0x01000100
.double  0x01010100,0x00010100,0x01010100,0x01010100
.double  0x01010100,0x00000001,0x01010100,0x01000001
.double  0x01010100,0x00010001,0x01010100,0x01010001
.double  0x01010100,0x00000101,0x01010100,0x01000101
.double  0x01010100,0x00010101,0x01010100,0x01010101
.double  0x00000001,0x00000000,0x00000001,0x01000000
.double  0x00000001,0x00010000,0x00000001,0x01010000
.double  0x00000001,0x00000100,0x00000001,0x01000100
.double  0x00000001,0x00010100,0x00000001,0x01010100
.double  0x00000001,0x00000001,0x00000001,0x01000001
.double  0x00000001,0x00010001,0x00000001,0x01010001
.double  0x00000001,0x00000101,0x00000001,0x01000101
.double  0x00000001,0x00010101,0x00000001,0x01010101
.double  0x01000001,0x00000000,0x01000001,0x01000000
.double  0x01000001,0x00010000,0x01000001,0x01010000
.double  0x01000001,0x00000100,0x01000001,0x01000100
.double  0x01000001,0x00010100,0x01000001,0x01010100
.double  0x01000001,0x00000001,0x01000001,0x01000001
.double  0x01000001,0x00010001,0x01000001,0x01010001
.double  0x01000001,0x00000101,0x01000001,0x01000101
```

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FIGURE 2 (Continued)

```
.double  0x01000001,0x00010101,0x01000001,0x01010101
.double  0x00010001,0x00000000,0x00010001,0x01000000
.double  0x00010001,0x00010000,0x00010001,0x01010000
.double  0x00010001,0x00000100,0x00010001,0x01000100
.double  0x00010001,0x00010100,0x00010001,0x01010100
.double  0x00010001,0x00000001,0x00010001,0x01000001
.double  0x00010001,0x00010001,0x00010001,0x01010001
.double  0x00010001,0x00000101,0x00010001,0x01000101
.double  0x00010001,0x00010101,0x00010001,0x01010101
.double  0x01010001,0x00000000,0x01010001,0x01000000
.double  0x01010001,0x00010000,0x01010001,0x01010000
.double  0x01010001,0x00000100,0x01010001,0x01000100
.double  0x01010001,0x00010100,0x01010001,0x01010100
.double  0x01010001,0x00000001,0x01010001,0x01000001
.double  0x01010001,0x00010001,0x01010001,0x01010001
.double  0x01010001,0x00000101,0x01010001,0x01000101
.double  0x01010001,0x00010101,0x01010001,0x01010101
.double  0x00000101,0x00000000,0x00000101,0x01000000
.double  0x00000101,0x00010000,0x00000101,0x01010000
.double  0x00000101,0x00000100,0x00000101,0x01000100
.double  0x00000101,0x00010100,0x00000101,0x01010100
.double  0x00000101,0x00000001,0x00000101,0x01000001
.double  0x00000101,0x00010001,0x00000101,0x01010001
.double  0x00000101,0x00000101,0x00000101,0x01000101
.double  0x00000101,0x00010101,0x00000101,0x01010101
.double  0x01000101,0x00000000,0x01000101,0x01000000
.double  0x01000101,0x00010000,0x01000101,0x01010000
.double  0x01000101,0x00000100,0x01000101,0x01000100
.double  0x01000101,0x00010100,0x01000101,0x01010100
.double  0x01000101,0x00000001,0x01000101,0x01000001
.double  0x01000101,0x00010001,0x01000101,0x01010001
.double  0x01000101,0x00000101,0x01000101,0x01000101
.double  0x01000101,0x00010101,0x01000101,0x01010101
.double  0x00010101,0x00000000,0x00010101,0x01000000
.double  0x00010101,0x00010000,0x00010101,0x01010000
.double  0x00010101,0x00000100,0x00010101,0x01000100
.double  0x00010101,0x00010100,0x00010101,0x01010100
.double  0x00010101,0x00000001,0x00010101,0x01000001
.double  0x00010101,0x00010001,0x00010101,0x01010001
.double  0x00010101,0x00000101,0x00010101,0x01000101
.double  0x00010101,0x00010101,0x00010101,0x01010101
.double  0x01010101,0x00000000,0x01010101,0x01000000
.double  0x01010101,0x00010000,0x01010101,0x01010000
.double  0x01010101,0x00000100,0x01010101,0x01000100
.double  0x01010101,0x00010100,0x01010101,0x01010100
.double  0x01010101,0x00000001,0x01010101,0x01000001
.double  0x01010101,0x00010001,0x01010101,0x01010001
.double  0x01010101,0x00000101,0x01010101,0x01000101
.double  0x01010101,0x00010101,0x01010101,0x01010101
```

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FIGURE 2 (Continued)

The following is an unrolled version of the rotate image algorithm. For the NS32532, the address computation, currently done with a separate addr instruction, may be done with the ORD instruction. This makes the execution time slightly faster.

```
#
#
#Rotate image emulation code
#
#     Inputs:
#          R0 = Source font address
#          R1 = Source font warp
#          R4 = Rotate table address
#
#     Outputs:
#          R2 = Destination font low 4 bytes (lsb->msb, 0 - 3)
#          R3 = Destination font high 4 bytes (lsb->msb, 4 - 7)
#
ROTIMG:
          movqd     0,r2           #clear destination font
          movd      r2,r3          #clear high bits of dest.
          movd      r2,r5          #clear high bits of temp.
          movb      0(r0),r5       #get a byte of source
          addd      r1,r0          #add source warp
          addd      r2,r2          #shift destination left one bit
          addd      r3,r3          #top 32 bits too
          addr      r4[r5:q],r6    #get pointer to table
          ord       0(r6),r2       #or in low bits
          ord       4(r6),r3       #or in high bits
          movb      0(r0),r5       #get a byte of source
          addd      r1,r0          #add source warp
          addd      r2,r2          #shift destination left one bit
          addd      r3,r3          #top 32 bits too
          addr      r4[r5:q],r6    #get pointer to table
          ord       0(r6),r2       #or in low bits
          ord       4(r6),r3       #or in high bits
          movb      0(r0),r5       #get a byte of source
          addd      r1,r0          #add source warp
          addd      r2,r2          #shift destination left one bit
          addd      r3,r3          #top 32 bits too
          addr      r4[r5:q],r6    #get pointer to table
          ord       0(r6),r2       #or in low bits
          ord       4(r6),r3       #or in high bits
          movb      0(r0),r5       #get a byte of source
          addd      r1,r0          #add source warp
          addd      r2,r2          #shift destination left one bit
          addd      r3,r3          #top 32 bits too
          addr      r4[r5:q],r6    #get pointer to table
          ord       0(r6),r2       #or in low bits
          ord       4(r6),r3       #or in high bits
          movb      0(r0),r5       #get a byte of source
          addd      r1,r0          #add source warp
```

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FIGURE 3

```
addd    r2,r2         #shift destination left one bit
addd    r3,r3         #top 32 bits too
addr    r4[r5:q],r6   #get pointer to table
ord     0(r6),r2      #or in low bits
ord     4(r6),r3      #or in high bits
movb    0(r0),r5      #get a byte of source
addd    r1,r0         #add source warp
addd    r2,r2         #shift destination left one bit
addd    r3,r3         #top 32 bits too
addr    r4[r5:q],r6   #get pointer to table
ord     0(r6),r2      #or in low bits
ord     4(r6),r3      #or in high bits
movb    0(r0),r5      #get a byte of source
addd    r1,r0         #add source warp
addd    r2,r2         #shift destination left one bit
addd    r3,r3         #top 32 bits too
addr    r4[r5:q],r6   #get pointer to table
ord     0(r6),r2      #or in low bits
ord     4(r6),r3      #or in high bits
movb    0(r0),r5      #get a byte of source
addd    r1,r0         #add source warp
addd    r2,r2         #shift destination left one bit
addd    r3,r3         #top 32 bits too
addr    r4[r5:q],r6   #get pointer to table
ord     0(r6),r2      #or in low bits
ord     4(r6),r3      #or in high bits
ret     $0            #and return
```

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FIGURE 3 (Continued)

80x86 to Series 32000® Translation; Series 32000 Graphics Note 6

National Semiconductor
Application Note 529
Dave Rand

1.0 INTRODUCTION

This application note discusses the conversion of Intel 8088, 8086, 80188 and 80186 (referred to here as 80x86) source assembly language to Series 32000 source code. As this is not intended to be a tutorial on Series 32000 assembly language, please see the Series 32000 Programmers Reference Manual for more information on instructions and addressing modes.

2.0 DESCRIPTION

The 80x86 model has 6 general purpose registers (AX, BX, CX, DX, SI, DI), each 16 bits wide. 4 of these registers can be further addressed as 8-bit registers (AL, AH, BL, BH, CL, CH, DL, DH). Series 32000 has 8 general purpose registers (R0–R7), each 32 bits wide. Each Series 32000 register may be accessed as an 8-, 16- or 32-bit register. Two special purpose registers on the 80x86, SP and BP, are 16-bit stack and base pointers. These are represented in Series 32000 with the SP and FP registers, each 32-bit.

The 80x86 model is capable of addressing up to 1 Megabyte of memory. Since the 16-bit register pointers are only capable of addressing 64 kbytes, 4 segment registers (CS, DS, ES, SS) are used in combination with the basic registers to point to memory. Series 32000 registers and addressing modes are all full 32-bit, and may point anywhere in the 16 Megabyte (or 4 Gigabyte, depending on processor model) addressing range.

Device ports are given their own 16-bit address on the 80x86, and there is a complement of instructions to handle input and output to these ports. Device ports on Series 32000 are memory mapped, and all instructions are available for port manipulation.

There are 6 addressing modes for data memory on the 80x86: Immediate, Direct, Direct indexed, Implied, Base relative and Stack. There are 9 addressing modes on Series 32000: Register, Immediate, Absolute, Register-relative, Memory space, External, Top-of-stack and Scaled index. Scaled index may be applied to any of the addressing modes (except scaled index) to create more addressing modes. The following figure shows the 80x86 addressing modes, and their Series 32000 counterparts.

Series 32000 assembly code reads left-to-right, meaning source is on the left, destination on the right. As you can see, most of the 80x86 addressing modes fall into the register-relative class of Series 32000. Also note that the ADDW could have been ADDD, performing a 32-bit add instead of only a 16-bit.

Series 32000 also permits memory-to-memory (two address) operation. A common operation like adding two variables is easier in Series 32000. Series 32000 has the same form for all math operations (multiply, divide, subtract), as well as all logical operators.

80x86		Series 32000
ADD AX,1234	Immediate	ADDW $1234,R0
ADD AX,LAB1	Direct	ADDW LAB1,R0
ADD AX,16[SI]	Direct Indexed	ADDW 16(R6),R0
ADD AX,[SI]	Implied	ADDW 0(R6),R0
ADD AX,[BX]	Base Relative	ADDW 0(R1),R0
ADD AX,[BX+SI]	Base Relative Implied	ADDW R1[R6:B],R0
ADD AX,12[BX+SI]	Base Relative Implied Indexed	ADDW 12(R1)[R6:B],R0
ADD AX,4[BP]	Stack (Relative)	ADDW 4(FP),R0
PUSH AX	Stack	MOVW R0,TOS

80x86	Series 32000	
MOV AL,LAB1 ADD LAB2,AL	ADDB LAB1,LAB2	8-Bit Add Operation
MOV AX,LAB3 ADD LAB4,AX	ADDW LAB3,LAB4	16-Bit Add Operation

MOV AX,LAB5L
ADD LAB6L,AX
MOV AX,LAB5H
ADDC LAB6H,AX
	ADDD LAB5,LAB6	32-Bit Add Operation

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Most 80x86 instructions have direct Series 32000 equivalents—with a major difference. Most 80x86 instructions affect the flags. Most Series 32000 instructions do not affect the flags in the same manner. For example, the 80x86 ADD instruction affects the Overflow, Carry, Arithmetic, Zero, Sign and Parity flags. The Series 32000 ADD instruction affects the Overflow and Carry flags. Programs that rely on side-effects of instructions which set flags must be changed in order to work correctly on Series 32000.

Table I gives a general guideline of instruction correlation between 80x86 and Series 32000. Many of the common subroutines in 80x86 may be replaced by a single instruction in Series 32000 (for example, 32-bit multiply and divide routines). Many special purpose instructions exist in Series 32000, and these instructions may help to optimize various algorithms.

3.0 IMPLEMENTATION

As an example, we will show some small 80x86 programs which we wish to convert to Series 32000. The first program reads a number of bytes from a port, waiting for status information. Below is the program in 80x86 assembly language:

```
;This program reads count bytes from port ioport, waiting for bit 7 of
;statport to be active (1) before reading each byte.
        xor     bx,bx           ;zero checksum
        mov     cx,count        ;get count of bytes
        mov     es,bufseg       ;get buffer segment
        lea     di,buffer       ;point to buffer offset
l1:     mov     dx,statport     ;get status port address
l2:     in      al,dx           ;read status port
        rcl     al,1            ;move bit 7 to carry
        jnc     l2              ;loop until status available
        mov     dx,ioport       ;point to data port
        in      al,dx           ;read port
        stosb                   ;store byte
        xor     ah,ah           ;zero high part of ax
        add     bx,ax           ;add to checksum
        loop    l1              ;loop for all bytes
        ret
```

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A direct translation of this program to Series 32000 using Table I, appears below. Note that this program will not work directly, due to the side effect of the rcl instruction being used.

```
#This program reads count bytes from port ioport, waiting for bit 7 of
#statport to be active (1) before reading each byte.
#
# Before optimization

        xord    r1,r1           # zero checksum
        movw    $count,r2       # get count of bytes
        addr    buffer,r5       # point to buffer
l11:    addr    statport,r3     # get status port address
l12:    movb    0(r3),r0        # read status port
        rotb    $1,r0           # move bit 7 to carry <<- does not work
        bcc     l12             # branch if carry clear
        addr    ioport,r3       # point to data port
        movb    0(r3),r0        # read port
        movb    r0,0(r5)        # store byte
        addqd   1,r5
        movzbw  r0,r0           # zero high part of ax
        addw    r0,r1           # add to checksum
        acbw    -1,r2,l11       # loop for all bytes
        ret     $0
```

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By using some of the special Series 32000 instructions, we can make this program much faster. The ROTB wil not work to test status, so we will replace that with a TBITB instruction. Since TBITB can directly address the port, there is no need to read the status port value at all. We will remove the read status port line, and the register load of r3. Reading the IO port as well can be done directly now, and we use a zero extension to ensure the high bits are cleared in preparation for the checksum addition. Note that it is easy to do a 32-bit checksum instead of only a 16-bit. Below is the 'optimized' code:

```
#This program reads count bytes from port ioport, waiting for bit 7 of
#statport to be active (1) before reading each byte.
#
# After optimization

        xord    r1,r1           # zero checksum
        movw    $count,r2       # get count of bytes
        addr    buffer,r5       # point to buffer
111:
112:    tbitb   $7,statport     # is bit 7 of status port valid?
        bfc     112             # no, loop until it is
        movzbd  ioport,r0       # read io port
        movb    r0,0(r5)        # store in buffer
        addqd   1,r5
        addw    r0,r1           # add to checksum
        acbw    -1,r2,111       # loop for all bytes
        ret     $0
```

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A second program shows, in 80x86 assembler, a method to copy and convert a string from mixed case ASCII to all upper case ASCII. This program is shown below:

```
;This program translates a null terminated ASCII string to uppercase
;
        mov     ds,buf1seg      ;point to input segment
        lea     si,buf1         ;point to input string
        mov     es,buf2seg      ;point to output segment
        lea     di,buf2         ;point to output string
        cld                     ;clear direction flag (increasing add)
11:     lodsb                   ;get a byte
        cmp     al,'a'          ;is the char less than 'a'?
        jb      12              ;yes, branch out
        cmp     al,'z'          ;is the char greater than 'z'?
        ja      12              ;yes, branch out
        and     al,5fh          ;and with 5f to make uppercase
12:     stosb                   ;store the character
        or      al,al           ;is this the last char?
        jnz     11              ;no, loop for more
        ret                     ;yes, exit
```

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A direct translation to Series 32000 works fine, as is shown below:

```
#This program translates a null terminate ASCII string to uppercase
#
# Before optimization

        addr    buf1,r4         # point to input string
        addr    buf2,r5         # point to output string
111:    movb    0(r4),r0        # get a byte
        addqd   1,r0
        cmpb    $'a',r0         # is the char less than 'a'?
        blo     112             # yes, branch out
        cmpb    $'z',r0         # is the char greater than 'z'?
        bhi     112             # yes, branch out
```

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```
        andb    $0x5f,r0        # and with 5f to make uppercase
112:    movb    r0,0(r5)        # store the character
        addqd   1,r5
        cmpqb   0,r0            # is this the last char?
        bne     111             # no, loop for more
        ret     $0
```

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This program allows us to exploit another Series 32000 instruction, the MOVST (Move and String Translate). With a 256 byte external table, we can translate any byte to any other byte. In this example, we simply use the full range of ASCII values in the translation table, with the lower case entries containing uppercase values.

Watch for other optimization opportunities, especially with multiply and add sequences (the INDEXi instruction could be used), and possible memory to memory sequence changes. When optimizing Series 32000 code, it is important to fully utilize the Complex Instruction Set. Allow the fewest number of instructions possible to do the work. Use the advanced addressing modes where possible. Try to employ larger data types in programs (Series 32000 takes the same number of clocks to add Bytes, Words or Double words).

4.0 CONCLUSION

Series 32000 assembly language offers a much richer complement of instructions when compared to the 80x86 assembly language. Translation from 80x86 to Series 32000 is made much easier by this full instruction set.

```
#This program translates a null terminate ASCII string to uppercase
#
# After optimization

        movqd   -1,r0           # number of bytes in string max.
        addr    buf1,r1         # point to input string
        addr    buf2,r2         # point to output string
        addr    ctable,r3       # address of conversion table
        movqd   0,r4            # match on a zero
        movst   u               # move string, translate, until 0
        movqb   0,0(r2)         # move a zero to output string
        ret     $0
```

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TABLE I

The following is a conversion table from 80x86 mnemonics to Series 32000. Note that many of the conversions are not exact, as the 80x86 instructions may affect flags that Series 32000 instructions do not. A * marks those instructions that may be affected most by this change in flags. The i in the Series 32000 instructions refers to the size of the data to be operated on. It may be B for Byte, W for Word or D for Double. Most arithmetic instructions also support F for single-precision Floating Point, and L for double-precision Floating-Point.

80x86	Series 32000	Comments
AAA	—	Suggest changing algorithm to use ADDPi
AAD	—	Suggest changing algorithm to use ADDPi/SUBPi
AAM	—	"
AAS	—	Suggest changing algorithm to use SUBPi
ADC	ADDCi	
ADD	ADDi	
AND	ANDi	
BOUND	CHECKi	
CALL	BSR/JSR	
CBW	MOVXBW	You may directly sign-extend data while moving
CLC	BICPSRB $1	Usually not required
CLD	—	Direction encoded within string instructions
CLI	BICPSRW $0x800	Supervisor mode instruction
CMC	—	Usually not required
CMP	CMPi	
CMPS	CMPSi	Many options available
CWD	MOVXWD	You may directly sign-extend data while moving
DAA	—	Suggest changing algorithm to use ADDPi
DAS	—	Suggest changing algorithm to use SUBPi
DEC	ADDQi-1*	Watch for flag usage
DIV	DIVi	Note: Series 32000 uses signed division
ENTER	ENTER[reglist],d	Builds stack frame, saves regs, allocates stack space
ESC	—	Usually used for Floating Point-see Series 32000 FP instructions
HLT	WAIT	
IDIV	DIVi/QUOi	DIVi rounds towards -infinity, QUOi to zero
IMUL	MULi	
IN	—	Series 32000 uses memory-mapped I/O
INC	ADDQi 1*	Watch for flag usage
INS	—	Series 32000 uses memory mapped I/O
INT	SVC	Not exact conversion, but usually used to call O/S
INTO	FLAG	Trap on overflow
IRET	RETI $0	Causes Interrupt Acknowledge cycle
JA/JNBE	BHI	Unsigned comparison
JAE/JNB	BHS	Unsigned comparison
JB/JNAE	BLT	Unsigned comparison
JBE/JNA	BLS	Unsigned comparison
JCXZ	—	Use CMPQi 0, followed by BEQ
JE/JZ	BEQ	Equal comparison
JG/JNLE	BGT	Signed comparison
JGE/JNL	BGE	Signed comparison
JL/JNGE	BLT	Signed comparison
JLE/JNG	BLE	Signed comparison
JMP	BR/JUMP	
JNE/JNZ	BNE	Not Equal comparison
JNO	—	Subroutines should be used for these instructions
JNP	—	as most Series 32000 code will not need these
JNS	—	operations.
JO	—	"
JP	—	"
JPE	—	"
JPO	—	"
JS	—	"
LAHF	—	SPRB UPSR,xxx may be useful
LDS	—	Segment registers not required on Series 32000
LEA	ADDR	
LEAVE	EXIT[reglist]	Restores regs, unallocates frame and stack
LES	—	Segment registers not required
LOCK	—	SBITIi, CBITIi interlocked instructions
LODS	MOVi/ADDQD	MOV instruction followed by address increment
LOOP	ACBi-1	ACBi may use memory or register

TABLE I (Continued)

80x86	Series 32000	Comments
LOOPE	—	BEQ followed by ACBi may be used
LOOPNE	—	BNE followed by ACBi may be used
LOOPNZ	—	BNE followed by ACBi may be used
LOOPZ	—	BEQ followed by ACBi may be used
MOV	MOVi	
MOVS	MOVSi	Many options available
MUL	MULi	Series 32000 uses signed multiplication
NEG	NEGi	Two's complement
NOP	NOP	
NOT	COMi	One's complement
OR	ORi	
OUT	—	Series 32000 uses memory mapped I/O
OUTS	—	Series 32000 uses memory mapped I/O
POP	MOVi TOS,	TOS addressing mode auto increments/decrements SP
POPA	RESTORE [r0,r1 . . r7]	Restores list of registers
POPF	LPRB UPSR,TOS	User mode loads 8 bits, supervisor 16 bits of PSR
PUSH	MOVi xx,TOS	Any data may be moved to TOS
PUSHA	SAVE [r0,r1 . . r7]	Saves list of registers
PUSHF	SPRB UPSR,TOS	User mode stores 8 bits, supervisor 16 bits of PSR
RCL	ROTi*	Does not rotate through carry
RCR	ROTi*	Does not rotate through carry
REP	—	Series 32000 string instructions use 32-bit counts
RET	RET	
ROL	ROTi	
ROR	ROTi	Rotates work in both directions
SAHF	—	LPRB UPSR,xx may be useful
SAL	ASHi	Arithmetic shift
SAR	ASHi	Arithmetic shift works both directions
SBB	SUBCi	
SCAS	SKPSi	Many options available
SHL	LSHi	Logical shift
SHR	LSHi	Logical shift works both directions
STC	BISPSRB $1	
STD	—	Direction is encoded in string instructions
STI	BISPSRW $0x800	Supervisor mode instruction
STOS	MOVi/ADDQD	MOV instruction followed by address increment
SUB	SUBi	
TEST	—	TBITi may be used as a substitute
WAIT	—	
XCHG	—	MOVi x,temp; MOVi y,x; MOVi temp,y
XLAT	MOVi x[R0:b],	Scaled index addressing mode
XOR	XORi	

Bit Mirror Routine; Series 32000® Graphics Note 7

National Semiconductor
Application Note 530
Dave Rand

1.0 INTRODUCTION

The bit mirror routine is designed to reorder the bits in an image. The bits are swapped around a fixed point, that being one half of the size of the data, as is shown for the byte mirror below. These routines can be used for conversion of 68000 based data.

2.0 DESCRIPTION

	Bit Number								Hex Value
	7	6	5	4	3	2	1	0	
Source	1	0	1	1	0	0	1	0	B2
Result of Mirror	0	1	0	0	1	1	0	1	4D

The "mirror", in this case, is between bits 3 and 4.

Several different algorithms are available for the mirror operation. The best algorithm to mirror a byte takes 20 clocks on a NS32016 (about 2.5 clocks per bit), and uses a 256 byte table to do the mirror operation. The table is reproduced at the end of this document. To perform a byte mirror, the following code may be used. The byte to be mirrored is in R0, and the destination is to be R1.

```
MOVB mirtab[r0:b],r1     #Mirror a byte
```

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An extension of this algorithm is used to mirror larger amounts of data. To mirror a 32-bit block of data from one location to another, the following code may be used. Register R0 points to the source block, register R1 points to the destination. R2 is used as a temporary value.

```
MOVZBD    0(r0),r2              #get first byte
MOVB      mirtab[r2:b],3(r1)    #store in last place
MOVB      1(r0),r2              #get next byte
MOVB      mirtab[r2:b],2(r1)    #store in next place
MOVB      2(r0),r2              #get the third byte
MOVB      mirtab[r2:b],1(r1)    #store in next place
MOVB      3(r0),r2              #get the last byte
MOVB      mirtab[r2:b],0(r1)    #first place
```

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This code uses 33 bytes of memory, and just 169 clocks to execute. Larger blocks of data can be mirrored with this method as well, with each additional byte taking about 40 clocks.

Registers can also be mirrored with this method, with just a few more instructions. To mirror R0 to R1, for example, the following code could be used. R2 is used as a temporary variable.

```
MOVZBD    r0,r2          #get lsbyte
MOVB      mirtab[r2:b],r1 #mirror the byte
LSHD      $8,r1          #move into higher byte of destination
LSHD      $-8,r0         #and of source
MOVB      r0,r2          #get lsbyte
MOVB      mirtab[r2:b],r1 #mirror the byte
LSHD      $8,r1          #move into higher byte of destination
LSHD      $-8,r0         #and of source
MOVB      r0,r2          #get lsbyte
MOVB      mirtab[r2:b],r1 #mirror the byte
LSHD      $8,r1          #move into higher byte of destination
LSHD      $-8,r0         #and of source
MOVB      r0,r2          #get lsbyte
MOVB      mirtab[r2:b],r1 #mirror the byte
```

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This code occupies 49 bytes, and executes in 286 clocks on an NS32016.

If space is at a premium, a shorter table may be used, at the expense of time. Each nibble (4 bits) instead of each byte is processed. This means that the table only requires 16 entries. To mirror a byte in R0 to R1, the following code can be used. R2 is used as a temporary variable.

```
MOVB    r0,r2               #get lsbyte
ANDD    $15,r2              #mask to get ls nibble
MOVB    mirtb16[r2:b],r1    #mirror the nibble
LSHD    $4,r1               #high nibble of destination
LSHD    $-4,r0              #and of source
MOVB    r0,r2               #get lsbyte
ANDD    $15,r2              #mask to get ls nibble
ORB     mirtb16[r2:b],r1    #mirror the nibble
```

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This code requires 32 bytes of memory, and executes in 125 clock cycles on an NS32016. A slightly faster time (100 clocks) may be obtained by adding a second table for the high nibble, and eliminating the LSHD 4,r1 instruction.

TABLES

MIRTAB is a table of all possible mirror values of 8 bits, or 256 bytes. MIRTB16 is a table of all possible mirror values of 4 bits, or 16 bytes. These tables should be aligned for best performance. They may reside in code (PC relative), or data (SB relative) space.

```
mirtab:
        .byte   0x00,0x80,0x40,0xc0,0x20,0xa0,0x60,0xe0,0x10,0x90,0x50
        .byte   0xd0,0x30,0xb0,0x70,0xf0
        .byte   0x08,0x88,0x48,0xc8,0x28,0xa8,0x68,0xe8,0x18,0x98,0x58
        .byte   0xd8,0x38,0xb8,0x78,0xf8
        .byte   0x04,0x84,0x44,0xc4,0x24,0xa4,0x64,0xe4,0x14,0x94,0x54
        .byte   0xd4,0x34,0xb4,0x74,0xf4
        .byte   0x0c,0x8c,0x4c,0xcc,0x2c,0xac,0x6c,0xec,0x1c,0x9c,0x5c
        .byte   0xdc,0x3c,0xbc,0x7c,0xfc
        .byte   0x02,0x82,0x42,0xc2,0x22,0xa2,0x62,0xe2,0x12,0x92,0x52
        .byte   0xd2,0x32,0xb2,0x72,0xf2
        .byte   0x0a,0x8a,0x4a,0xca,0x2a,0xaa,0x6a,0xea,0x1a,0x9a,0x5a
        .byte   0xda,0x3a,0xba,0x7a,0xfa
        .byte   0x06,0x86,0x46,0xc6,0x26,0xa6,0x66,0xe6,0x16,0x96,0x56
        .byte   0xd6,0x36,0xb6,0x76,0xf6
        .byte   0x0e,0x8e,0x4e,0xce,0x2e,0xae,0x6e,0xee,0x1e,0x9e,0x5e
        .byte   0xde,0x3e,0xbe,0x7e,0xfe
        .byte   0x01,0x81,0x41,0xc1,0x21,0xa1,0x61,0xe1,0x11,0x91,0x51
        .byte   0xd1,0x31,0xb1,0x71,0xf1
        .byte   0x09,0x89,0x49,0xc9,0x29,0xa9,0x69,0xe9,0x19,0x99,0x59
        .byte   0xd9,0x39,0xb9,0x79,0xf9
        .byte   0x05,0x85,0x45,0xc5,0x25,0xa5,0x65,0xe5,0x15,0x95,0x55
        .byte   0xd5,0x35,0xb5,0x75,0xf5
        .byte   0x0d,0x8d,0x4d,0xcd,0x2d,0xad,0x6d,0xed,0x1d,0x9d,0x5d
        .byte   0xdd,0x3d,0xbd,0x7d,0xfd
        .byte   0x03,0x83,0x43,0xc3,0x23,0xa3,0x63,0xe3,0x13,0x93,0x53
        .byte   0xd3,0x33,0xb3,0x73,0xf3
        .byte   0x0b,0x8b,0x4b,0xcb,0x2b,0xab,0x6b,0xeb,0x1b,0x9b,0x5b
        .byte   0xdb,0x3b,0xbb,0x7b,0xfb
        .byte   0x07,0x87,0x47,0xc7,0x27,0xa7,0x67,0xe7,0x17,0x97,0x57
        .byte   0xd7,0x37,0xb7,0x77,0xf7
        .byte   0x0f,0x8f,0x4f,0xcf,0x2f,0xaf,0x6f,0xef,0x1f,0x9f,0x5f
        .byte   0xdf,0x3f,0xbf,0x7f,0xff

mirtb16:
        .byte   0x0,0x8,0x4,0xc,0x2,0xa,0x6,0xe,0x1,0x9,0x5
        .byte   0xd,0x3,0xb,0x7,0xf
```

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Section 9

NSC800 Family

Section 9 Contents

National Semiconductor

microCMOS

NSC800™ High-Performance Low-Power CMOS Microprocessor

General Description

The NSC800 is an 8-bit CMOS microprocessor that functions as the central processing unit (CPU) in National Semiconductor's NSC800 microcomputer family. National's microCMOS technology used to fabricate this device provides system designers with performance equivalent to comparable NMOS products, but with the low power advantage of CMOS. Some of the many system functions incorporated on the device, are vectored priority interrupts, refresh control, power-save feature and interrupt acknowledge. The NSC800 is available in dual-in-line and surface mounted chip carrier packages.

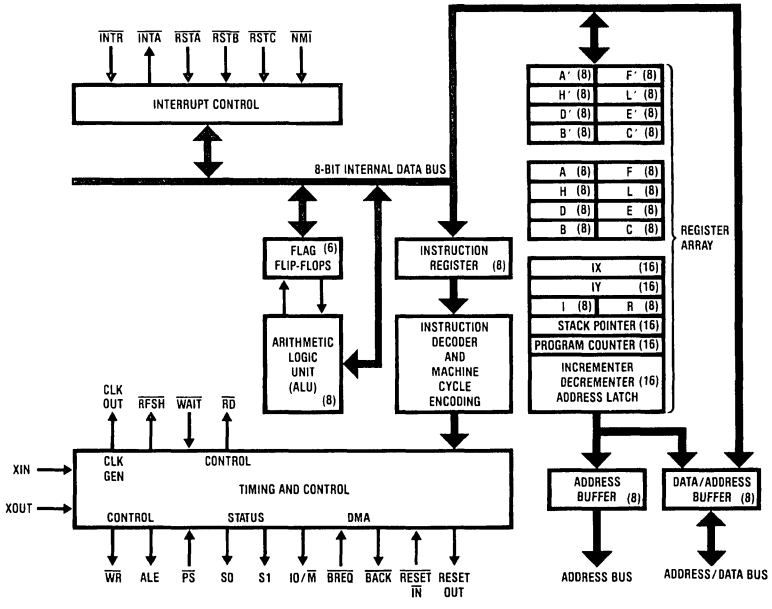
The system designer can choose not only from the dedicated CMOS peripherals that allow direct interfacing to the NSC800 but from the full line of National's CMOS products to allow a low-power system solution. The dedicated peripherals include NSC810A RAM I/O Timer, NSC858 UART, and NSC831 I/O.

All devices are available in commercial, industrial and military temperature ranges along with two added reliability flows. The first is an extended burn in test and the second is the military class C screening in accordance with Method 5004 of MIL-STD-883.

Features

- Fully compatible with Z80® instruction set:
  Powerful set of 158 instructions
  10 addressing modes
  22 internal registers
- Low power: 50 mW at 5V V_{CC}
- Unique power-save feature
- Multiplexed bus structure
- Schmitt trigger input on reset
- On-chip bus controller and clock generator
- Variable power supply 2.4V−6.0V
- On-chip 8-bit dynamic RAM refresh circuitry
- Speed: 1.0 μs instruction cycle at 4.0 MHz
  NSC800-4 4.0 MHz
  NSC800-3 2.5 MHz
  NSC800-1 1.0 MHz
- Capable of addressing 64k bytes of memory and 256 I/O devices
- Five interrupt request lines on-chip

Block Diagram



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1.0 Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Voltage on Any Pin with Respect to Ground	−0.3V to V_{CC} +0.3V
Maximum V_{CC}	7V
Power Dissipation	1W
Lead Temp. (Soldering, 10 seconds)	300°C

2.0 Operating Conditions

NSC800-1 → T_A = 0°C to +70°C
T_A = −40°C to +85°C
NSC800-3 → T_A = 0°C to +70°C
T_A = −40°C to +85°C
T_A = −55°C to +125°C
NSC800-4 → T_A = 0°C to +70°C
T_A = −40°C to +85°C
T_A = −55°C to +125°C

3.0 DC Electrical Characteristics V_{CC} = 5V ±10%, GND = 0V, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	Logical 1 Input Voltage		0.8 V_{CC}		V_{CC}	V
V_{IL}	Logical 0 Input Voltage		0		0.2 V_{CC}	V
V_{HY}	Hysteresis at RESET IN input	V_{CC} = 5V	0.25	0.5		V
V_{OH1}	Logical 1 Output Voltage	I_{OUT} = −1.0 mA	2.4			V
V_{OH2}	Logical 1 Output Voltage	I_{OUT} = −10 μA	V_{CC} −0.5			V
V_{OL1}	Logical 0 Output Voltage	I_{OUT} = 2 mA	0		0.4	V
V_{OL2}	Logical 0 Output Voltage	I_{OUT} = 10 μA	0		0.1	V
I_{IL}	Input Leakage Current	0 ≤ V_{IN} ≤ V_{CC}	−10.0		10.0	μA
I_{OL}	Output Leakage Current	0 ≤ V_{IN} ≤ V_{CC}	−10.0		10.0	μA
I_{CC}	Active Supply Current	I_{OUT} = 0, $f_{(XIN)}$ = 2 MHz, T_A = 25°C		8	11	mA
I_{CC}	Active Supply Current	I_{OUT} = 0, $f_{(XIN)}$ = 5 MHz, T_A = 25°C		10	15	mA
I_{CC}	Active Supply Current	I_{OUT} = 0, $f_{(XIN)}$ = 8 MHz, T_A = 25°C		15	21	mA
I_Q	Quiescent Current	I_{OUT} = 0, $\overline{PS}$ = 0, V_{IN} = 0 or V_{IN} = V_{CC} $f_{(XIN)}$ = 0 MHz, T_A = 25°C, X_{IN} = 0, CLK = 1		2	5	mA
I_{PS}	Power-Save Current	I_{OUT} = 0, $\overline{PS}$ = 0, V_{IN} = 0 or V_{IN} = V_{CC} $f_{(XIN)}$ = 5.0 MHz , T_A = 25°		5	7	mA
C_{IN}	Input Capacitance			6	10	pF
C_{OUT}	Output Capacitance			8	12	pF
V_{CC}	Power Supply Voltage	(Note 2)	2.4	5	6	V

Note 1: Absolute Maximum Ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under DC Electrical Characteristics.

Note 2: CPU operation at lower voltages will reduce the maximum operating speed. Operation at voltages other than 5V ±10% is guaranteed by design, not tested.

4.0 AC Electrical Characteristics V_{CC} = 5V ±10%, GND = 0V, unless otherwise specified

Symbol	Parameter	NSC800-1		NSC800		NSC800-4		Units	Notes
		Min	Max	Min	Max	Min	Max		
t_X	Period at XIN and XOUT Pins	500	3333	200	3333	125	3333	ns	
T	Period at Clock Output (=2 t_X)	1000	6667	400	6667	250	6667	ns	
t_R	Clock Rise Time		110		110		80	ns	Measured from 10%–90% of signal
t_F	Clock Fall Time		70		60		50	ns	Measured from 10%–90% of signal
t_L	Clock Low Time	435		150		85		ns	50% duty cycle, square wave input on XIN
t_H	Clock High Time	450		145		75		ns	50% duty cycle, square wave input on XIN
$t_{ACC(OP)}$	ALE to Valid Data		1340		490		300	ns	Add t for each $\overline{WAIT}$ STATE
$t_{ACC(MR)}$	ALE to Valid Data		1875		620		375	ns	Add t for each $\overline{WAIT}$ STATE
t_{AFR}	AD(0–7) Float after $\overline{RD}$ Falling		0		0		0	ns	
t_{BABE}	$\overline{BACK}$ Rising to Bus Enable		1000		400		250	ns	
t_{BABF}	$\overline{BACK}$ Falling to Bus Float		50		50		50	ns	
t_{BACL}	$\overline{BACK}$ Fall to CLK Falling	425		125		55		ns	
t_{BRH}	$\overline{BREQ}$ Hold Time	0		0		0		ns	
t_{BRS}	$\overline{BREQ}$ Set-Up Time	100		50		45		ns	
t_{CAF}	Clock Falling ALE Falling	0	70	0	65	0	55	ns	
t_{CAR}	Clock Rising to ALE Rising	0	100	0	100	0	80	ns	
t_{CRD}	Clock Rising to Read Rising		100		90		80	ns	
t_{CRF}	Clock Rising to Refresh Falling		80		70		60	ns	
t_{DAI}	ALE Falling to $\overline{INTA}$ Falling	445		160		85		ns	
t_{DAR}	ALE Falling to $\overline{RD}$ Falling	400	575	160	250	90	160	ns	
t_{DAW}	ALE Falling to $\overline{WR}$ Falling	900	1010	350	420	200	255	ns	
$t_{D(BACK)1}$	ALE Falling to $\overline{BACK}$ Falling	2460		975		600		ns	Add t for each $\overline{WAIT}$ state Add t for opcode fetch cycles
$t_{D(BACK)2}$	$\overline{BREQ}$ Rising to $\overline{BACK}$ Rising	500	1610	200	700	125	475	ns	
$t_{D(I)}$	ALE Falling to $\overline{INTR}$, $\overline{NMI}$, $\overline{RSTA\text{-}C}$, $\overline{PS}$, $\overline{BREQ}$, Inputs Valid		1360		475		250	ns	Add t for each $\overline{WAIT}$ state Add t for opcode fetch cycles
t_{DPA}	Rising $\overline{PS}$ to Falling ALE	500	1685	200	760	125	500	ns	See *Figure 14* also
$t_{D(WAIT)}$	ALE Falling to $\overline{WAIT}$ Input Valid		550		250		125	ns	

4.0 AC Electrical Characteristics V_{CC} = 5V ±10%, GND = 0V, unless otherwise specified (Continued)

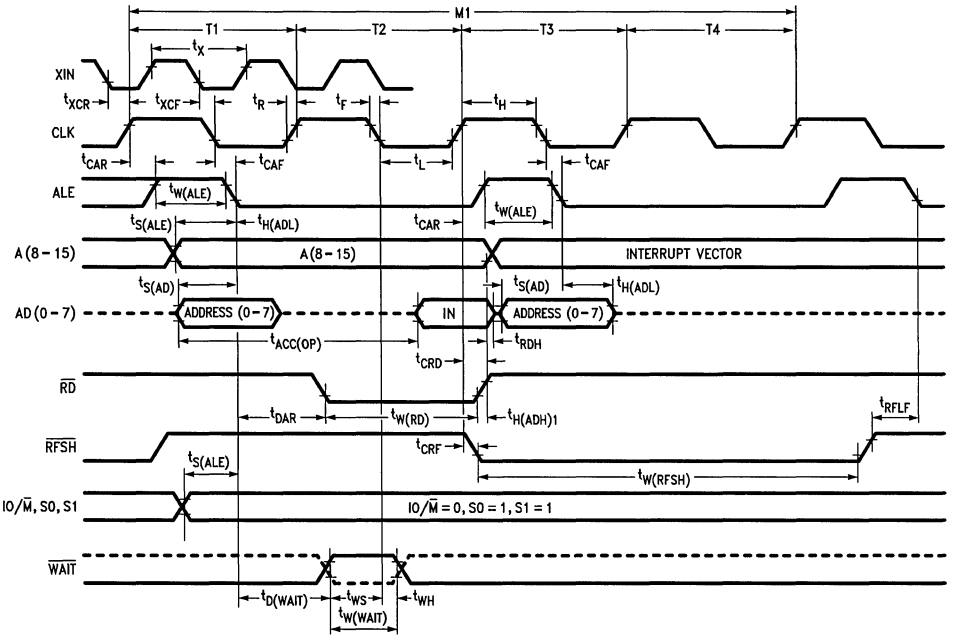
Symbol	Parameter	NSC800-1		NSC800		NSC800-4		Units	Notes
		Min	Max	Min	Max	Min	Max		
$T_{H(ADH)1}$	A(8–15) Hold Time During Opcode Fetch	0		0		0		ns	
$T_{H(ADH)2}$	A(8–15) Hold Time During Memory or IO, $\overline{RD}$ and $\overline{WR}$	400		100		60		ns	
$T_{H(ADL)}$	AD(0–7) Hold Time	100		60		30		ns	
$T_{H(WD)}$	Write Data Hold Time	400		100		75		ns	
t_{INH}	Interrupt Hold Time	0		0		0		ns	
t_{INS}	Interrupt Set-Up Time	100		50		45		ns	
t_{NMI}	Width of NMI Input	50		30		20		ns	
t_{RDH}	Data Hold after Read	0		0		0		ns	
t_{RFLF}	$\overline{RFSH}$ Rising to ALE Falling	60		50		40		ns	
$t_{RL(MR)}$	$\overline{RD}$ Rising to ALE Rising (Memory Read)	390		100		45		ns	
$t_{S(AD)}$	AD(0–7) Set-Up Time	300		45		40		ns	
$t_{S(ALE)}$	A(8–15), SO, SI, IO/$\overline{M}$ Set-Up Time	350		70		50		ns	
$t_{S(WD)}$	Write Data Set-Up Time	385		75		30		ns	
$t_{W(ALE)}$	ALE Width	430		130		100		ns	
t_{WH}	$\overline{WAIT}$ Hold Time	0		0		0		ns	
$t_{W(I)}$	Width of $\overline{INTR}$, $\overline{RSTA-C}$, $\overline{PS}$, $\overline{BREQ}$	500		200		125		ns	
$t_{W(INTA)}$	$\overline{INTA}$ Strobe Width	1000		400		200		ns	Add two t states for first $\overline{INTA}$ of each interrupt response string Add t for each $\overline{WAIT}$ state
t_{WL}	$\overline{WR}$ Rising to ALE Rising	450		130		70		ns	
$t_{W(RD)}$	Read Strobe Width During Opcode Fetch	960		360		185		ns	Add t for each $\overline{WAIT}$ State Add t/2 for Memory Read Cycles
$t_{W(RFSH)}$	Refresh Strobe Width	1925		725		395		ns	
t_{WS}	$\overline{WAIT}$ Set-Up Time	100		70		55		ns	
$t_{W(WAIT)}$	$\overline{WAIT}$ Input Width	550		250		175		ns	
$t_{W(WR)}$	Write Strobe Width	985		390		220		ns	Add t for each $\overline{WAIT}$ state
t_{XCF}	XIN to Clock Falling	25	100	20	95	5	80	ns	
t_{XCR}	XIN to Clock Rising	25	85	20	85	5	80	ns	

Note 1: Test conditions: t = 1000 ns for NSC800-1, 400 ns for NSC800, 250 ns for NSC800-4.

Note 2: Output timings are measured with a purely capacitive load of 100 pF.

5.0 Timing Waveforms

Opcode Fetch Cycle



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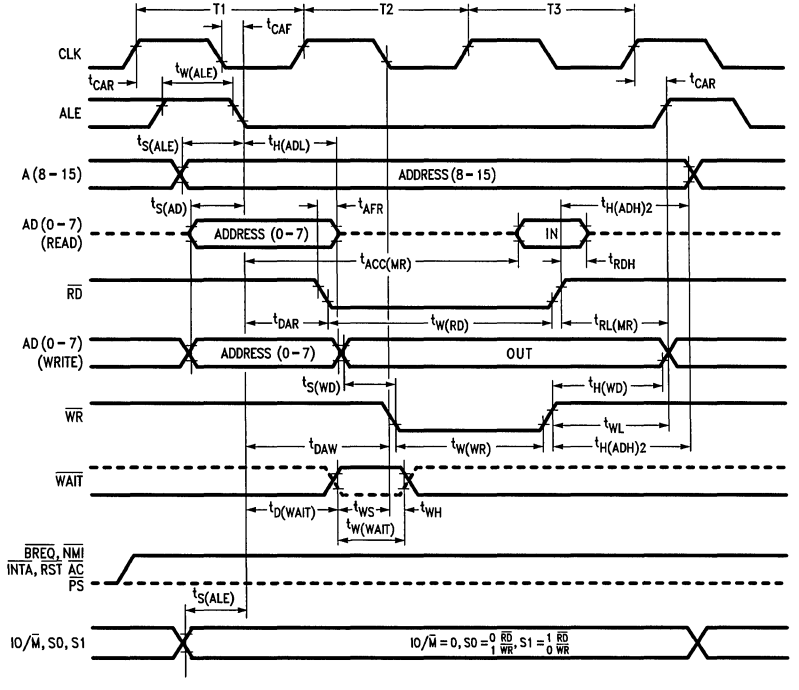
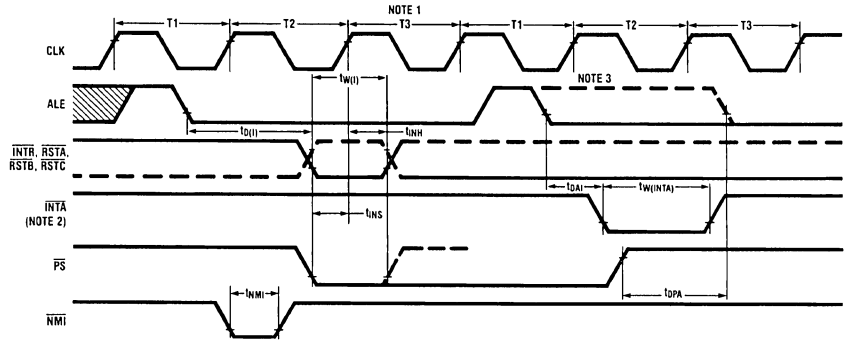
Memory Read and Write Cycle



TL/C/5171–4

5.0 Timing Waveforms (Continued)

Interrupt—Power-Save Cycle



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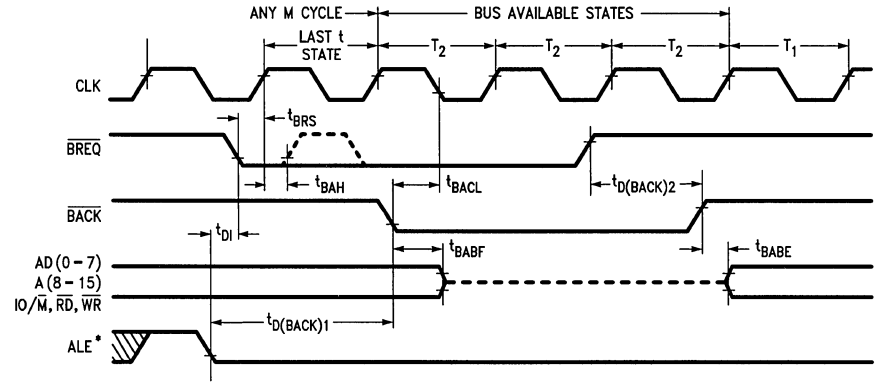
Note 1: This t state is the last t state of the last M cycle of any instruction.

Note 2: Response to INTR input.

Note 3: Response to PS input.

Bus Acknowledge Cycle



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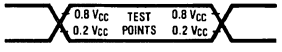
*Waveform not drawn to proportion. Use only for specifying test points.

AC Testing Input/Output Waveform



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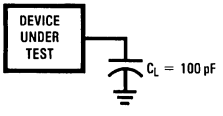
AC Testing Load Circuit



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NSC800 HARDWARE

6.0 Pin Descriptions

6.1 INPUT SIGNALS

Reset Input ($\overline{\text{RESET IN}}$): Active low. Sets A (8–15) and AD (0–7) to TRI-STATE® (high impedance). Clears the contents of PC, I and R registers, disables interrupts, and activates reset out.

Bus Request ($\overline{\text{BREQ}}$): Active low. Used when another device requests the system bus. The NSC800 recognizes $\overline{\text{BREQ}}$ at the end of the current machine cycle, and sets A(8–15), AD(0–7), IO/$\overline{\text{M}}$, $\overline{\text{RD}}$, and $\overline{\text{WR}}$ to the high impedance state. $\overline{\text{RFSH}}$ is high during a bus request cycle. The CPU acknowledges the bus request via the $\overline{\text{BACK}}$ output signal.

Non-Maskable Interrupt ($\overline{\text{NMI}}$): Active low. The non-maskable interrupt, generated by the peripheral device(s), is the highest priority interrupt. The edge sensitive interrupt requires only a pulse to set an internal flip-flop which generates the internal interrupt request. The $\overline{\text{NMI}}$ flip-flop is monitored on the same clock edge as the other interrupts. It must also meet the minimum set-up time spec for the interrupt to be accepted in the current machine instruction. When the processor accepts the interrupt the flip-flop resets automatically. Interrupt execution is independent of the interrupt enable flip-flop. $\overline{\text{NMI}}$ execution results in saving the PC on the stack and automatic branching to restart address X'0066 in memory.

Restart Interrupts, A, B, C ($\overline{\text{RSTA}}$, $\overline{\text{RSTB}}$, $\overline{\text{RSTC}}$): Active low level sensitive. The CPU recognizes restarts generated by the peripherals at the end of the current instruction, if their respective interrupt enable and master enable bits are set. Execution is identical to $\overline{\text{NMI}}$ except the interrupts vector to the following restart addresses:

Name	Restart Address (X')
$\overline{\text{NMI}}$	0066
$\overline{\text{RSTA}}$	003C
$\overline{\text{RSTB}}$	0034
$\overline{\text{RSTC}}$	002C
$\overline{\text{INTR}}$ (Mode 1)	0038

The order of priority is fixed. The list above starts with the highest priority.

Interrupt Request ($\overline{\text{INTR}}$): Active low, level sensitive. The CPU recognizes an interrupt request at the end of the current instruction provided that the interrupt enable and master interrupt enable bits are set. $\overline{\text{INTR}}$ is the lowest priority interrupt. Program control selects one of three response modes which determines the method of servicing $\overline{\text{INTR}}$ in conjunction with $\overline{\text{INTA}}$. See Interrupt Control.

Wait (WAIT): Active low. When set low during $\overline{\text{RD}}$, $\overline{\text{WR}}$ or $\overline{\text{INTA}}$ machine cycles (during the $\overline{\text{WR}}$ machine cycle, wait must be valid prior to write going active) the CPU extends its machine cycle in increments of t (wait) states. The wait machine cycle continues until the $\overline{\text{WAIT}}$ input returns high.

The wait strobe input will be accepted only during machine cycles that have $\overline{\text{RD}}$, $\overline{\text{WR}}$ or $\overline{\text{INTA}}$ strobes and during the machine cycle immediately after an interrupt has been accepted by the CPU. The later cycle has its RD strobe suppressed but it will still accept the wait.

Power-Save ($\overline{\text{PS}}$): Active low. $\overline{\text{PS}}$ is sampled during the last t state of the current instruction cycle. When $\overline{\text{PS}}$ is low, the CPU stops executing at the end of current instruction and keeps itself in the low-power mode. Normal operation resumes when $\overline{\text{PS}}$ returns high (see Power Save Feature description).

CRYSTAL (X_{IN}, X_{OUT}): X_{IN} can be used as an external clock input. A crystal can be connected across X_{IN} and X_{OUT} to provide a source for the system clock.

6.2 OUTPUT SIGNALS

Bus Acknowledge ($\overline{\text{BACK}}$): Active low. $\overline{\text{BACK}}$ indicates to the bus requesting device that the CPU bus and its control signals are in the TRI-STATE mode. The requesting device then commands the bus and its control signals.

Address Bits 8–15 [A(8–15)]: Active high. These are the most significant 8 bits of the memory address during a memory instruction. During an I/O instruction, the port address on the lower 8 address bits gets duplicated onto A(8–15). During a BREQ/BACK cycle, the A(8–15) bus is in the TRI-STATE mode.

Reset Out (RESET OUT): Active high. When RESET OUT is high, it indicates the CPU is being reset. This signal is normally used to reset the peripheral devices.

Input/Output/Memory (IO/$\overline{\text{M}}$): An active high on the IO/$\overline{\text{M}}$ output signifies that the current machine cycle is an input/output cycle. An active low on the IO/$\overline{\text{M}}$ output signifies that the current machine cycle is a memory cycle. It is TRI-STATE during $\overline{\text{BREQ}}$/$\overline{\text{BACK}}$ cycles.

Refresh ($\overline{\text{RFSH}}$): Active low. The refresh output indicates that the dynamic RAM refresh cycle is in progress. $\overline{\text{RFSH}}$ goes low during T3 and T4 states of all M1 cycles. During the refresh cycle, AD(0–7) has the refresh address and A(8–15) indicates the interrupt vector register data. $\overline{\text{RFSH}}$ is high during $\overline{\text{BREQ}}$/$\overline{\text{BACK}}$ cycles.

Address Latch Enable (ALE): Active high. ALE is active only during the T1 state of any M cycle and also T3 state of the M1 cycle. The high to low transition of ALE indicates that a valid memory, I/O or refresh address is available on the AD(0–7) lines.

Read Strobe ($\overline{\text{RD}}$): Active low. The CPU receives data via the AD(0–7) lines on the trailing edge of the $\overline{\text{RD}}$ strobe. The $\overline{\text{RD}}$ line is in the TRI-STATE mode during $\overline{\text{BREQ}}$/$\overline{\text{BACK}}$ cycles.

Write Strobe ($\overline{\text{WR}}$): Active low. The CPU sends data via the AD(0–7) lines while the $\overline{\text{WR}}$ strobe is low. The $\overline{\text{WR}}$ line is in the TRI-STATE mode during $\overline{\text{BREQ}}$/$\overline{\text{BACK}}$ cycles.

Clock (CLK): CLK is the output provided for use as a system clock. The CLK output is a square wave at one half the input frequency.

Interrupt Acknowledge ($\overline{\text{INTA}}$): Active low. This signal strobes the interrupt response vector from the interrupting peripheral devices onto the AD(0–7) lines. $\overline{\text{INTA}}$ is active during the M1 cycle immediately following the t state where the CPU recognized the $\overline{\text{INTR}}$ interrupt request.

Two of the three interrupt request modes use $\overline{\text{INTA}}$. In mode 0 one to four $\overline{\text{INTA}}$ signals strobe a one to four byte instruction onto the AD(0–7) lines. In mode 2 one $\overline{\text{INTA}}$ signal strobes the lower byte of an interrupt response vector onto the bus. In mode 1, $\overline{\text{INTA}}$ is inactive and the CPU response to $\overline{\text{INTR}}$ is the same as for an NMI or restart interrupt.

6.0 Pin Descriptions (Continued)

Status (SO, S1): Bus status outputs provide encoded information regarding the current M cycle as follows:

Machine Cycle	Status			Control	
	S0	S1	IO/$\overline{M}$	$\overline{RD}$	$\overline{WR}$
Opcode Fetch	1	1	0	0	1
Memory Read	0	1	0	0	1
Memory Write	1	0	0	1	0
I/O Read	0	1	1	0	1
I/O Write	1	0	1	1	0
Halt*	0	0	0	0	1
Internal Operation*	0	1	0	1	1
Acknowledge of Int**	1	1	0	1	1

*ALE is not suppressed in this cycle.

**This is the cycle that occurs immediately after the CPU accepts an interrupt ($\overline{RSTA}$, $\overline{RSTB}$, $\overline{RSTC}$, $\overline{INTR}$, $\overline{NMI}$).

Note 1: During halt, CPU continues to do dummy opcode fetch from location following the halt instruction with a halt status. This is so CPU can continue to do its dynamic RAM refresh.

Note 2: No early status is provided for interrupt or hardware restarts.

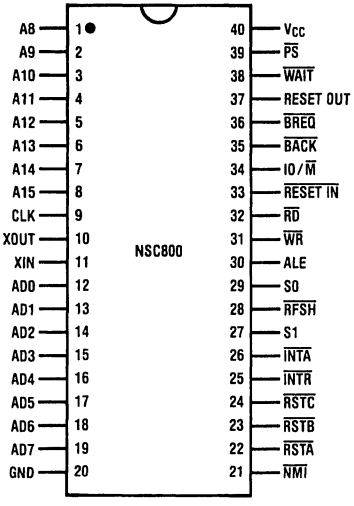
6.3 INPUT/OUTPUT SIGNALS

Multiplexed Address/Data [AD(0–7)]: Active high

At $\overline{RD}$ Time:	Input data to CPU.
At $\overline{WR}$ Time:	Output data from CPU.
At Falling Edge of ALE Time:	Least significant byte of address during memory reference cycle. 8-bit port address during I/O reference cycle.
During $\overline{BREQ}$/ $\overline{BACK}$ Cycle:	High impedance.

7.0 Connection Diagrams

Dual-In-Line Package



Top View

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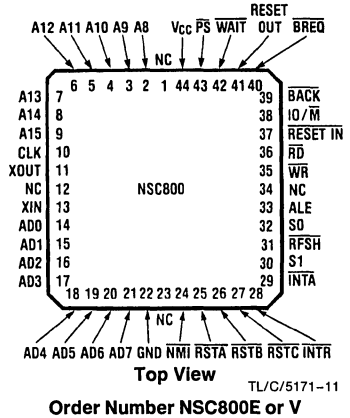
Order Number NSC800D or N
See NS Package D40C or N40A

Chip Carrier Package



Top View

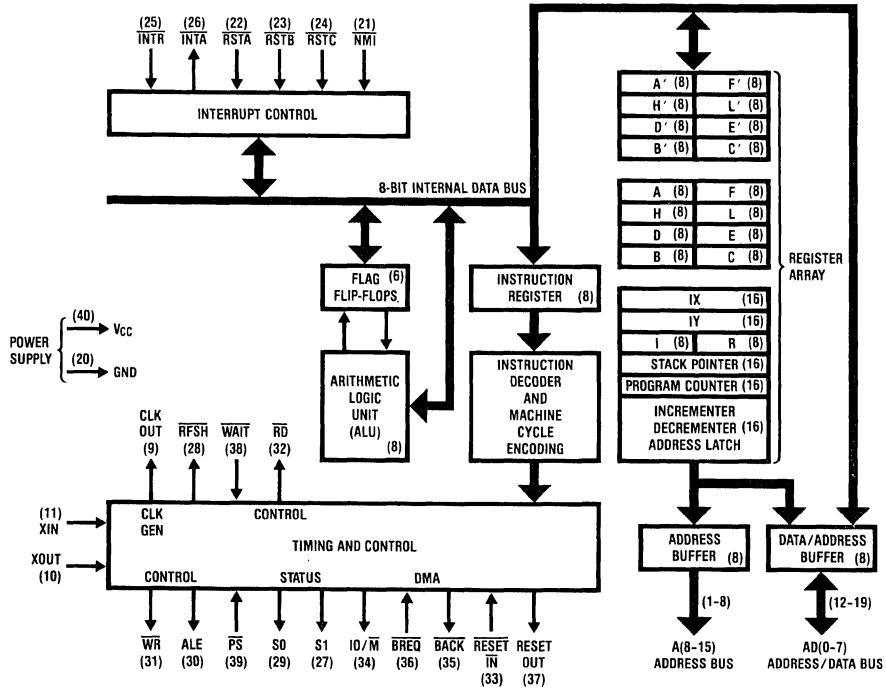
TL/C/5171–11

Order Number NSC800E or V
See NS Package E44B or V44A

8.0 Functional Description

This section reviews the CPU architecture shown below, focusing on the functional aspects from a hardware perspective, including timing details.

As illustrated in *Figure 1*, the NSC800 is an 8-bit parallel device. The major functional blocks are: the ALU, register array, interrupt control, timing and control logic. These areas are connected via the 8-bit internal data bus. Detailed descriptions of these blocks ae provided in the following sections.



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Note: Applicable pinout for 40-pin dual-in-line package within parentheses

FIGURE 1. NSC800 CPU Functional Block Diagram

8.0 Functional Description (Continued)

8.1 REGISTER ARRAY

The NSC800 register array is divided into two parts: the dedicated registers and the working registers, as shown in *Figure 2*.

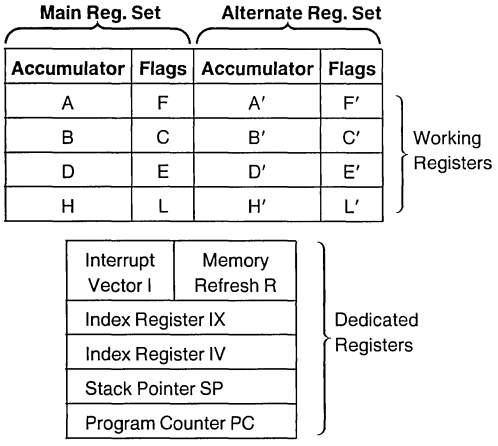

FIGURE 2. NSC800 Register Array

8.2 DEDICATED REGISTERS

There are 6 dedicated registers in the NSC800: two 8-bit and four 16-bit registers (see *Figure 3*).

Although their contents are under program control, the program has no control over their operational functions, unlike the CPU working registers. The function of each dedicated register is described as follows:

CPU Dedicated Registers

Program Counter PC	(16)
Stack Pointer SP	(16)
Index Register IX	(16)
Index Register IY	(16)
Interrupt Vector Register I	(8)
Memory Refresh Register R	(8)

FIGURE 3. Dedicated Registers

8.2.1 Program Counter (PC)

The program counter contains the 16-bit address of the current instruction being fetched from memory. The PC increments after its contents have been transferred to the address lines. When a program jump occurs, the PC receives the new address which overrides the incrementer.

There are many conditional and unconditional jumps, calls, and return instructions in the NSC800's instruction repertoire that allow easy manipulation of this register in controlling the program execution (i.e. JP NZ nn, JR Zd2, CALL NC, nn).

8.2.2 Stack Pointer (SP)

The 16-bit stack pointer contains the address of the current top of stack that is located in external system RAM. The stack is organized in a last-in, first-out (LIFO) structure. The pointer decrements before data is pushed onto the stack, and increments after data is popped from the stack.

Various operations store or retrieve, data on the stack. This, along with the usage of subroutine calls and interrupts, allows simple implementation of subroutine and interrupt nesting as well as alleviating many problems of data manipulation.

8.2.3 Index Register (IX and IY)

The NSC800 contains two index registers to hold independent, 16-bit base addresses used in the indexed addressing mode. In this mode, an index register, either IX or IY, contains a base address of an area in memory making it a pointer for data tables.

In all instructions employing indexed modes of operation, another byte acts as a signed two's complement displacement. This addressing mode enables easy data table manipulations.

8.2.4 Interrupt Register (I)

When the NSC800 provides a Mode 2 response to $\overline{\text{INTR}}$, the action taken is an indirect call to the memory location containing the service routine address. The pointer to the address of the service routine is formed by two bytes, the high-byte is from the I Register and the low-byte is from the interrupting peripheral. The peripheral always provides an even address for the lower byte (LSB = 0). When the processor receives the lower byte from the peripheral it concatenates it in the following manner:

I Register	External byte	
8 bits		0

↑

The LSB of the external byte must be zero.

FIGURE 4a. Interrupt Register

The even memory location contains the low-order byte, the next consecutive location contains the high-order byte of the pointer to the beginning address of the interrupt service routine.

8.2.5 Refresh Register (R)

For systems that use dynamic memories rather than static RAM's, the NSC800 provides an integral 8-bit memory refresh counter. The contents of the register are incremented after each opcode fetch and are sent out on the lower portion of the address bus, along with a refresh control signal. This provides a totally transparent refresh cycle and does not slow down CPU operation.

The program can read and write to the R register, although this is usually done only for test purposes.

8.0 Functional Description (Continued)

8.3 CPU WORKING AND ALTERNATE REGISTER SETS

8.3.1 CPU Working Registers

The portion of the register array shown in *Figure 4b* represents the CPU working registers. These sixteen 8-bit registers are general-purpose registers because they perform a multitude of functions, depending on the instruction being executed. They are grouped together also due to the types of instructions that use them, particularly alternate set operations.

The F (flag) register is a special-purpose register because its contents are more a result of machine status rather than program data. The F register is included because of its interaction with the A register, and its manipulations in the alternate register set operations.

8.3.2 Alternate Registers

The NSC800 registers designated as CPU working registers have one common feature: the existence of a duplicate register in an alternate register set. This architectural concept simplifies programming during operations such as interrupt response, when the machine status represented by the contents of the registers must be saved.

The alternate register concept makes one set of registers available to the programmer at any given time. Two instructions (EX AF, A'F' and EXX), exchange the current working set of registers with their alternate set. One exchange between the A and F registers and their respective duplicates (A' and F') saves the primary status information contained in the accumulator and the flag register. The second exchange instruction performs the exchange between the remaining registers, B, C, D, E, H, and L, and their respective alternates B', C', D', E', H', and L'. This essentially saves the contents of the original complement of registers while providing the programmer with a usable alternate set.

CPU Main Working Register Set

Accumulator A	(8)	Flags F	(8)
Register B	(8)	Register C	(8)
Register D	(8)	Register E	(8)
Register H	(8)	Register L	(8)

CPU Alternate Working Register Set

Accumulator A'	(8)	Flags F'	(8)
Register B'	(8)	Register C'	(8)
Register D'	(8)	Register E'	(8)
Register H'	(8)	Register L'	(8)

FIGURE 4b. CPU Working and Alternate Registers

8.4 REGISTER FUNCTIONS

8.4.1 Accumulator (A Register)

The A register serves as a source or destination register for data manipulation instructions. In addition, it serves as the accumulator for the results of 8-bit arithmetic and logic operations.

The A register also has a special status in some types of operations; that is, certain addressing modes are reserved for the A register only, although the function is available for all the other registers. For example, any register can be loaded by immediate, register indirect, or indexed addressing modes. The A register, however, can also be loaded via an additional register indirect addressing.

Another special feature of the A register is that it produces more efficient memory coding than equivalent instruction functions directed to other registers. Any register can be rotated; however, while it requires a two-byte instruction to normally rotate any register, a single-byte instruction is available for rotating the contents of the accumulator (A register).

8.4.2 F Register - Flags

The NSC800 flag register consists of six status bits that contain information regarding the results of previous CPU operations. The register can be read by pushing the contents onto the stack and then reading it, however, it cannot be written to. It is classified as a register because of its affiliation with the accumulator and the existence of a duplicate register for use in exchange instructions with the accumulator.

Of the six flags shown in *Figure 5*, only four can be directly tested by the programmer via conditional jump, call, and return instructions. They are the Sign (S), Zero (Z), Parity/Overflow (P/V), and Carry (C) flags. The Half Carry (H) and Add/Subtract (N) flags are used for internal operations related to BCD arithmetic.

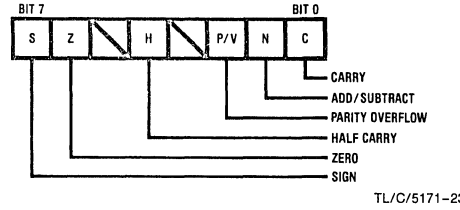

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FIGURE 5. Flag Register

8.0 Functional Description (Continued)

8.4.3 Carry (C)

A carry from the highest order bit of the accumulator during an add instruction, or a borrow generated during a subtraction instruction sets the carry flag. Specific shift and rotate instructions also affect this bit.

Two specific instructions in the NSC800 instruction repertoire set (SCF) or complement (CCF) the carry flag.

Other operations that affect the C flag are as follows:

- Adds
- Subtracts
- Logic Operations (always resets C flag)
- Rotate Accumulator
- Rotate and Shifts
- Decimal Adjust
- Negation of Accumulator

Other operations do not affect the C flag.

8.4.4 Adds/Subtract (N)

This flag is used in conjunction with the H flag to ensure that the proper BCD correction algorithm is used during the decimal adjust instruction (DAA). The correction algorithm depends on whether an add or subtract was previously done with BCD operands.

The operations that set the N flag are:

- Subtractions
- Decrements (8-bit)
- Complementing of the Accumulator
- Block I/O
- Block Searches
- Negation of the Accumulator

The operations that reset the N flag are:

- Adds
- Increments
- Logic Operations
- Rotates
- Set and Complement Carry
- Input Register Indirect
- Block Transfers
- Load of the I or R Registers
- Bit Tests

Other operations do not affect the N flag.

8.4.5 Parity/Overflow (P/V)

The Parity/Overflow flag is a dual-purpose flag that indicates results of logic and arithmetic operations. In logic operations, the P/V flag indicates the parity of the result; the flag is set (high) if the result is even, reset (low) if the result is odd. In arithmetic operations, it represents an overflow condition when the result, interpreted as signed two's complement arithmetic, is out of range for the eight-bit accumulator (i.e. −128 to +127).

The following operations affect the P/V flag according to the parity of the result of the operation:

- Logic Operations
- Rotate and Shift
- Rotate Digits
- Decimal Adjust
- Input Register Indirect

The following operations affect the P/V flag according to the overflow result of the operation.

- Adds (16 bit with carry, 8-bit with/without carry)
- Subtracts (16 bit with carry, 8-bit with/without carry)
- Increments and Decrements
- Negation of Accumulator

The P/V flag has no significance immediately after the following operations.

- Block I/O
- Bit Tests

In block transfers and compares, the P/V flag indicates the status of the BC register, always ending in the reset state after an auto repeat of a block move. Other operations do not affect the P/V flag.

8.4.6 Half Carry (H)

This flag indicates a BCD carry, or borrow, result from the low-order four bits of operation. It can be used to correct the results of a previously packed decimal add, or subtract, operation by use of the Decimal Adjust Instruction (DAA).

The following operations affect the H flag:

- Adds (8-bit)
- Subtracts (8-bit)
- Increments and Decrements
- Decimal Adjust
- Negation of Accumulator
- Always Set by: Logic AND
  Complement Accumulator
  Bit Testing
- Always Reset By: Logic OR's and XOR's
  Rotates and Shifts
  Set Carry
  Input Register Indirect
  Block Transfers
  Loads of I and R Registers

The H flag has no significance immediately after the following operations.

- 16-bit Adds with/without carry
- 16-Bit Subtracts with carry
- Complement of the carry
- Block I/O
- Block Searches

Other operations do not affect the H flag.

8.0 Functional Description (Continued)

8.4.7 Zero Flag (Z)

Loading a zero in the accumulator or when a zero results from an operation sets the zero flag.

The following operations affect the zero flag.

- Adds (16-bit with carry, 8-bit with/without carry)
- Subtracts (16-bit with carry, 8-bit with/without carry)
- Logic Operations
- Increments and Decrements
- Rotate and Shifts
- Rotate Digits
- Decimal Adjust
- Input Register Indirect
- Block I/O (always set after auto repeat block I/O)
- Block Searches
- Load of I and R Registers
- Bit Tests
- Negation of Accumulator

The Z flag has no signficance immediately after the following operations:

- Block Transfers

Other operations do not affect the zero flag.

8.4.8 Sign Flag (S)

The sign flag stores the state of bit 7 (the most-significant bit and sign bit) of the accumulator following an arithmetic operation. This flag is of use when dealing with signed numbers.

The sign flag is affected by the following operation according to the result:

- Adds (16-bit with carry, 8-bit with/without carry)
- Subtracts (16-bit with carry, 8-bit with/without carry)
- Logic Operations
- Increments and Decrements
- Rotate and Shifts
- Rotate Digits
- Decimal Adjust
- Input Register Indirect
- Block Search
- Load of I and R Registers
- Negation of Accumulator

The S flag has no significance immediately after the following operations:

- Block I/O
- Block Transfers
- Bit Tests

Other operations do not affect the sign bit.

8.4.9 Additional General-Purpose Registers

The other general-purpose registers are the B, C, D, E, H and L registers and their alternate register set, B', C', D', E', H' and L'. The general-purpose registers can be used interchangeably.

In addition, the B and C registers perform special functions in the NSC800 expanded I/O capabilities, particularly block I/O operations. In these functions, the C register can address I/O ports; the B register provides a counter function when used in the register indirect address mode.

When used with the special condition jump instruction (DJNZ) the B register again provides the counter function.

8.4.10 Alternate Configurations

The six 8-bit general purpose registers (B,C,D,E,H,L) will combine to form three 16-bit registers. This occurs by concatenating the B and C registers to form the BC register, the D and E registers form the DE register, and the H and L registers form the HL register.

Having these 16-bit registers allows 16-bit data handling, thereby expanding the number of 16-bit registers available for memory addressing modes. The HL register typically provides the pointer address for use in register indirect addressing of the memory.

The DE register provides a second memory pointer register for the NSC800's powerful block transfer operations. The BC register also provides an assist to the block transfer operations by acting as a byte-counter for these operations.

8.5 ARITHMETIC-LOGIC UNIT (ALU)

The arithmetic, logic and rotate instructions are performed by the ALU. The ALU internally communicates with the registers and data buffer on the 8-bit internal data bus.

8.6 INSTRUCTION REGISTER AND DECODER

During an opcode fetch, the first byte of an instruction is transferred from the data buffer (i.e. its on the internal data bus) to the instruction register. The instruction register feeds the instruction decoder, which gated by timing signals, generates the control signals that read or write data from or to the registers, control the ALU and provide all required external control signals.

9.0 Timing and Control

9.1 INTERNAL CLOCK GENERATOR

An inverter oscillator contained on the NSC800 chip provides all necessary timing signals. The chip operation frequency is equal to one half of the frequency of this oscillator.

The oscillator frequency can be controlled by one of the following methods:

1. Leaving the X_{OUT} pin unterminated and driving the X_{IN} pin with an externally generated clock as shown in *Figure 6*. When driving X_{IN} with a square wave, the minimum duty cycle is 30% high.

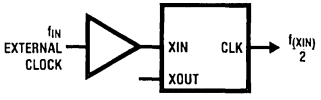

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FIGURE 6. Use of External Clock

2. Connecting a crystal with the proper biasing network between X_{IN} and X_{OUT} as shown in *Figure 7*. Recommended crystal is a parallel resonance AT cut crystal.

Note 1: If the crystal frequency is 2 MHz or less a series resistor, R_S, (470Ω to 1500Ω) should be connected between X_{OUT} and R, XTAL and C_Z. Additionally, the capacitance of C1 and C2 should be increased by 2 to 3 times the recommended value.

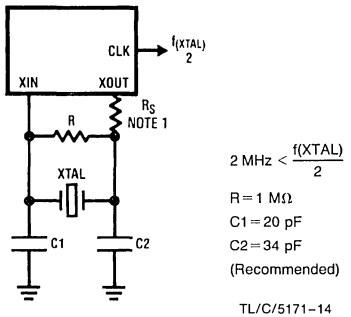

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FIGURE 7. Use Of Crystal

The CPU has a minimum clock frequency input (@ X_{IN}) of 300 kHz, which results in 150 kHz system clock speed. All registers internal to the chip are static, however there is dynamic logic which limits the minimum clock speed. The input clock can be stopped without fear of losing any data or damaging the part. You stop it in the phase of the clock that has X_{IN} low and CLK OUT high. When restarting the CPU, precautions must be taken so that the input clock meets these minimum specification. Once started, the CPU will continue operation from the same location at which it was stopped. During DC operation of the CPU, typical current drain will be 2 mA. This current drain can be reduced by placing the CPU in a wait state during an opcode fetch cycle then stopping the clock. For clock stop circuit, see *Figure 8*.

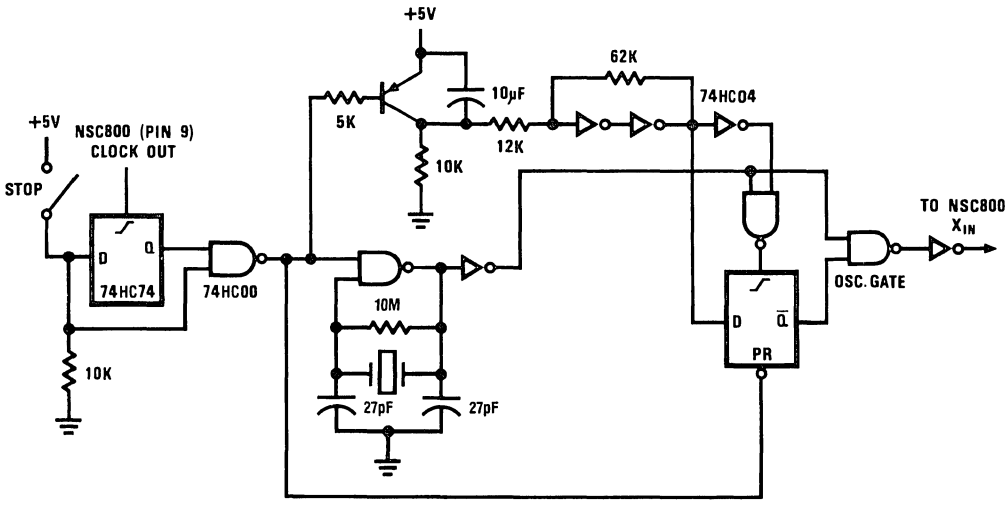

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FIGURE 8. Clock Stop Circuit

9.0 Timing and Control (Continued)

9.2 CPU TIMING

The NSC800 uses a multiplexed bus for data and addresses. The 16-bit address bus is divided into a high-order 8-bit address bus that handles bits 8–15 of the address, and a low-order 8-bit multiplexed address/data bus that handles bits 0–7 of the address and bits 0–7 of the data. Strobe outputs from the NSC800 (ALE, $\overline{RD}$ and $\overline{WR}$) indicate when a valid address or data is present on the bus. IO/$\overline{M}$ indicates whether the ensuing cycle accesses memory or I/O.

During an input or output instruction, the CPU duplicates the lower half of the address [AD(0–7)] onto the upper address bus [A(8–15)]. The eight bits of address will stay on A(8–15) for the entire machine cycle and can be used for chip selection directly.

Figure 9 illustrates the timing relationship for opcode fetch cycles with and without a wait state.

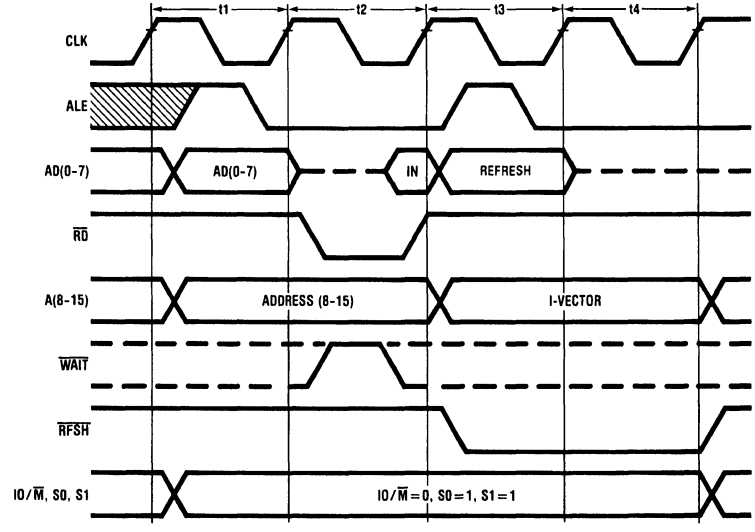

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FIGURE 9a. Opcode Fetch Cycles without $\overline{WAIT}$ States

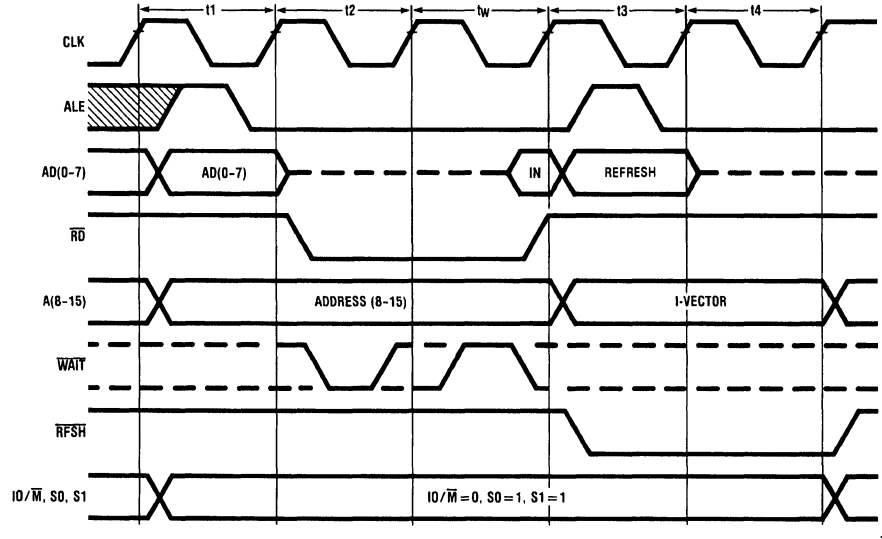

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FIGURE 9b. Opcode Fetch Cycles with $\overline{WAIT}$ States

9.0 Timing and Control (Continued)

During the opcode fetch, the CPU places the contents of the PC on the address bus. The falling edge of ALE indicates a valid address on the AD(0–7) lines. The $\overline{WAIT}$ input is sampled during t_2 and if active causes the NSC800 to insert a wait state (t_w). WAIT is sampled again during t_w so that when it goes inactive, the CPU continues its opcode fetch by latching in the data on the rising edge of $\overline{RD}$ from the AD(0–7) lines. During t_3, $\overline{RFSH}$ goes active and AD(0–7) has the dynamic RAM refresh address from register R and A(8–15) the interrupt vector from register I.

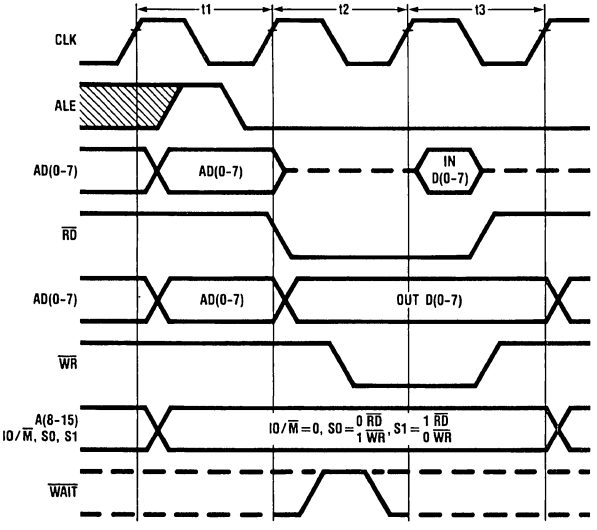

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FIGURE 10a. Memory Read/Write Cycles without $\overline{WAIT}$ States

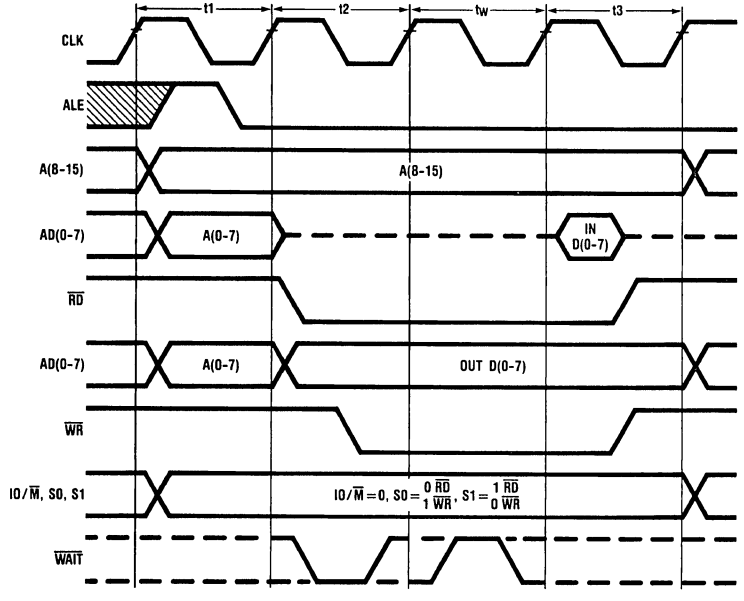

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FIGURE 10b. Memory Read and Write with $\overline{WAIT}$ States

9.0 Timing and Control (Continued)

Figure 10 shows the timing for memory read (other than opcode fetchs) and write cycles with and without a wait state. The $\overline{RD}$ stobe is widened by $\frac{t}{2}$ (half the machine state) for memory reads so that the actual latching of the input data occurs later.

Figure 11 shows the timing for input and output cycles with and without wait states. The CPU automatically inserts one wait state into each I/O instruction to allow sufficient time for an I/O port to decode the address.

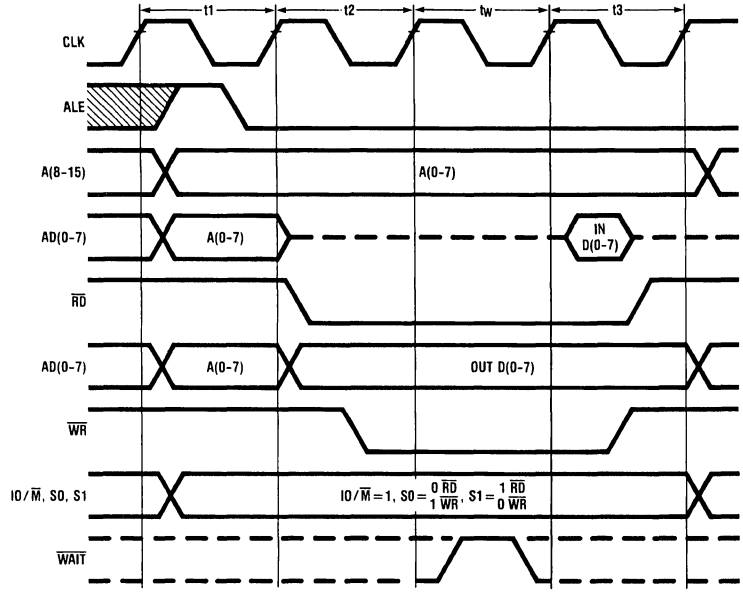

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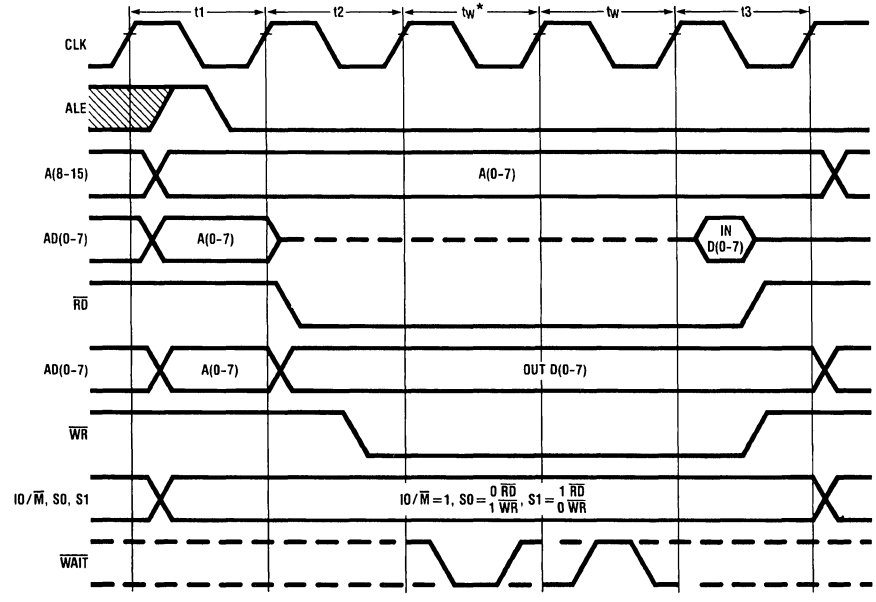
FIGURE 11a. Input and Output Cycles without $\overline{WAIT}$ States



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*$\overline{WAIT}$ state automatically inserted during IO operation.

FIGURE 11b. Input and Output Cycles with $\overline{WAIT}$ States

9.0 Timing and Control (Continued)

9.3 INITIALIZATION

$\overline{\text{RESET IN}}$ initializes the NSC800; RESET OUT initializes the peripheral components. The Schmitt trigger at the $\overline{\text{RESET IN}}$ input facilitates using an R-C network reset scheme during power up (see *Figure 12*).

To ensure proper power-up conditions for the NSC800, the following power-up and initialization procedure is recommended:

1. Apply power (V_{CC} and GND) and set $\overline{\text{RESET IN}}$ active (low). Allow sufficient time (approximately 30 ms if a crystal is used) for the oscillator and internal clocks to stabilize. $\overline{\text{RESET IN}}$ must remain low for at least 3t state (CLK) times. RESET OUT goes high as soon as the active $\overline{\text{RESET IN}}$ signal is clocked into the first flip-flop after the on-chip Schmitt trigger. RESET OUT signal is available to reset the peripherals.
2. Set $\overline{\text{RESET IN}}$ high. RESET OUT then goes low as the inactive $\overline{\text{RESET IN}}$ signal is clocked into the first flip-flop after the on-chip Schmitt trigger. Following this the CPU initiates the first opcode fetch cycle.

Note: The NSC800 initialization includes: Clear PC to X'0000 (the first opcode fetch, therefore, is from memory location X'0000). Clear registers I (Interrupt Vector Base) and R (Refresh Counter) to X'00. Clear interrupt control register bits IEA, IEB and IEC. The interrupt control bit IEI is set to 1 to maintain INS8080A/Z80A compatibility (see INTERRUPTS for more details). The CPU disables maskable interrupts and enters $\overline{\text{INTR}}$ Mode 0. While $\overline{\text{RESET IN}}$ is active (low), the A(8–15) and AD(0–7) lines go to high impedance (TRI-STATE) and all CPU strobes go to the inactive state (see *Figure 13*).

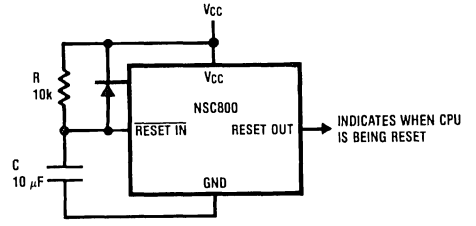

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FIGURE 12. Power-On Reset

9.4 POWER-SAVE FEATURE

The NSC800 provides a unique power-save mode by the means of the $\overline{\text{PS}}$ pin. $\overline{\text{PS}}$ input is sampled at the last t state of the last M cycle of an instruction. After recognizing an active (low) level on $\overline{\text{PS}}$, The NSC800 stops its internal clocks, thereby reducing its power dissipation to one half of operating power, yet maintaining all register values and internal control status. The NSC800 keeps its oscillator running, and makes the CLK signal available to the system. When in power-save the ALE strobe will be stopped high and the address lines [AD(0–7), A(8–15)] will indicate the next machine address. When $\overline{\text{PS}}$ returns high, the opcode fetch (or M1 cycle) of the CPU begins in a normal manner. Note this M1 cycle could also be an interrupt acknowledge cycle if the NSC800 was interrupted simultaneously with $\overline{\text{PS}}$ (i.e. $\overline{\text{PS}}$ has priority over a simultaneously occurring interrupt). However, interrupts are not accepted during power save. *Figure 14* illustrates the power save timing.

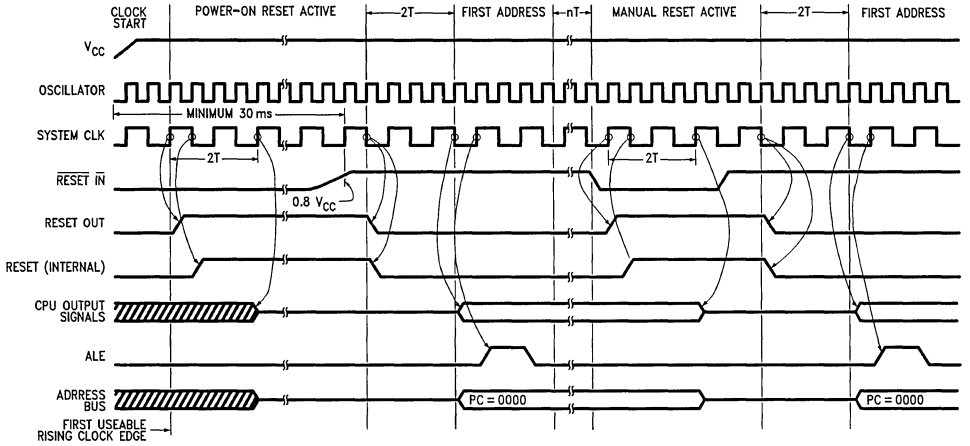

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FIGURE 13. NSC800 Signals During Power-On and Manual Reset

9.0 Timing and Control (Continued)

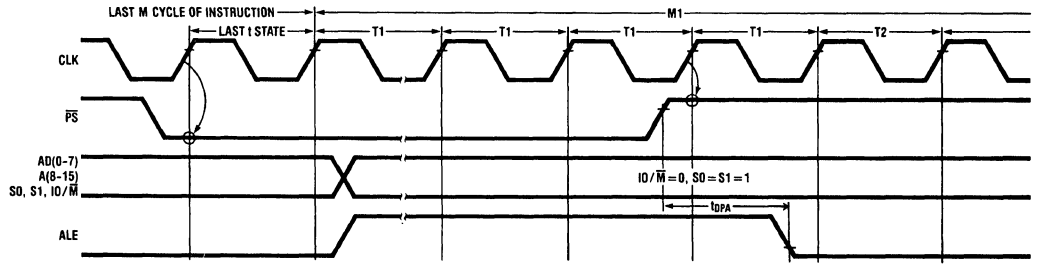

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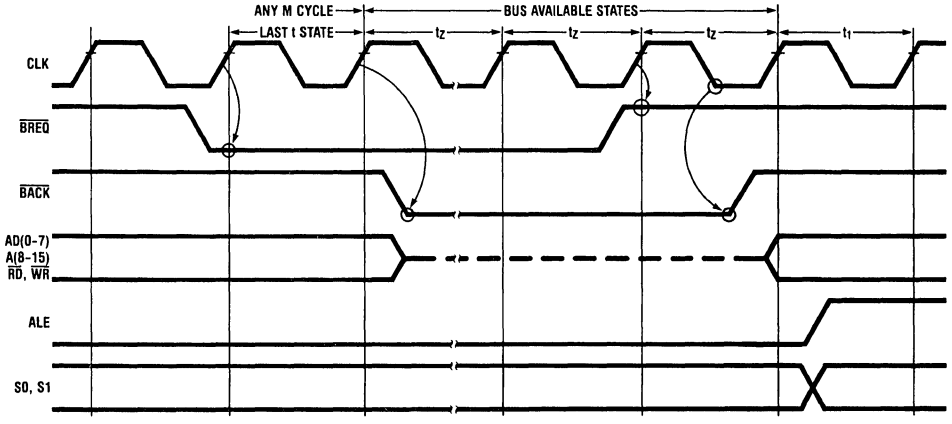
FIGURE 14. NSC800 Power-Save



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*S0, S1 during $\overline{BREQ}$ will indicate same machine cycle as during the cycle when $\overline{BREQ}$ was accepted.

t_Z = time states during which bus and control signals are in high impedance mode.

FIGURE 15. Bus Acknowledge Cycle

In the event $\overline{BREQ}$ is asserted (low) at the end of an instruction cycle and $\overline{PS}$ is active simultaneously, the following occurs:

1. The NSC800 will go into $\overline{BACK}$ cycle.
2. Upon completion of $\overline{BACK}$ cycle if $\overline{PS}$ is still active the CPU will go into power-save mode.

9.5 BUS ACCESS CONTROL

Figure 15 illustrates bus access control in the NSC800. The external device controller produces an active $\overline{BREQ}$ signal that requests the bus. When the CPU responds with $\overline{BACK}$ then the bus and related control strobes go to high impedance (TRI-STATE) and the $\overline{RFSH}$ signal remains high. It should be noted that (1) $\overline{BREQ}$ is sampled at the last t state of any M machine cycle only. (2) The NSC800 will not acknowledge any interrupt/restart requests, and will not peform any dynamic RAM refresh functions until after $\overline{BREQ}$ input signal is inactive high. (3) $\overline{BREQ}$ signal has priority over all interrupt request signals, should $\overline{BREQ}$ and interrupt request become active simultaneously. Therefore, interrupts latched at the end of the instruction cycle will be serviced after a simultaneously occurring $\overline{BREQ}$. $\overline{NMI}$ is latched during an active $\overline{BREQ}$.

9.6 INTERRUPT CONTROL

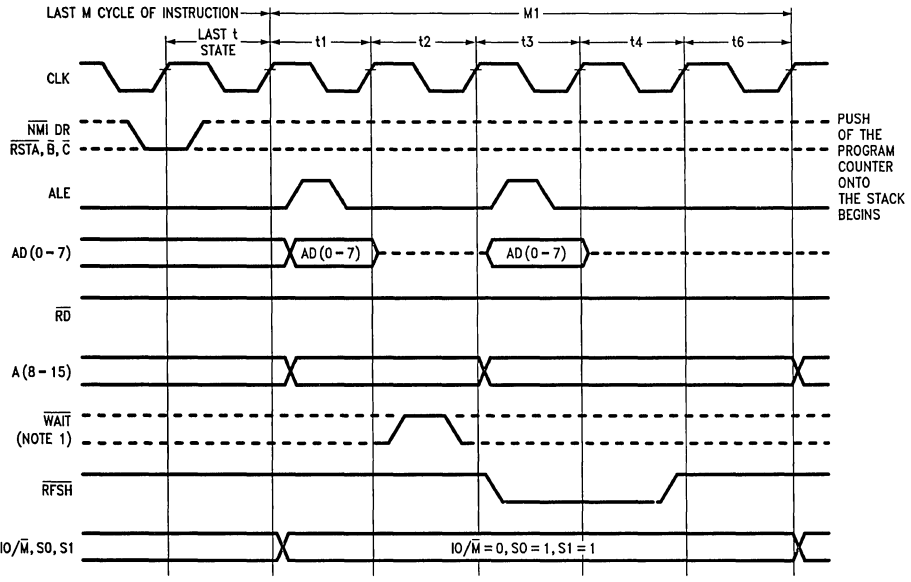
The NSC800 has five interrupt/restart inputs, four are maskable ($\overline{RSTA}$, $\overline{RSTB}$, $\overline{RSTC}$, and $\overline{INTR}$) and one is non-maskable ($\overline{NMI}$). $\overline{NMI}$ has the highest priority of all interrupts; the user cannot disable $\overline{NMI}$. After recognizing an active input on $\overline{NMI}$, the CPU stops before the next instruction, pushes the PC onto the stack, and jumps to address X'0066, where the user's interrupt service routine is located (i.e., restart to memory location X'0066). $\overline{NMI}$ is intended for interrupts requiring immediate attention, such as power-down, control panel, etc.

$\overline{RSTA}$, $\overline{RSTB}$ and $\overline{RSTC}$ are restart inputs, which, if enabled, execute a restart to memory location X'003C, X'0034, and X'002C, respectively. Note that the CPU response to the $\overline{NMI}$ and $\overline{RST}$ ($\overline{A}$, $\overline{B}$, $\overline{C}$) request input is basically identical, except for the restored memory location. Unlike $\overline{NMI}$, however, restart request inputs must be enabled.

Figure 16 illustrates $\overline{NMI}$ and $\overline{RST}$ interrupt machine cycles. M1 cycle will be a dummy opcode fetch cycle followed by M2 and M3 which are stack push operations. The following instruction then starts from the interrupts restart location.

Note: $\overline{RD}$ does *not* go low during this dummy opcode fetch. A unique indication of INTA can be decoded using 2 ALEs and $\overline{RD}$.

9.0 Timing and Control (Continued)



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Note 1: This is the only machine cycle that does not have an $\overline{RD}$, $\overline{WR}$, or $\overline{INTA}$ strobe but will accept a wait strobe.

FIGURE 16. Non-Maskable and Restart Interrupt Machine Cycle

The NSC800 also provides one more general purpose interrupt request input, $\overline{INTR}$. When enabled, the CPU responds to $\overline{INTR}$ in one of the three modes defined by instruction IM0, IM1, and IM2 for modes 0, 1, and 2, respectively. Following reset, the CPU automatically enables mode 0.

Interrupt ($\overline{INTR}$) Mode 0: The CPU responds to an interrupt request by providing an INTA (interrupt acknowledge) strobe, which can be used to gate an instruction from a peripheral onto the data bus. The CPU inserts two wait states during the first $\overline{INTA}$ cycle to allow the interrupting device (or its controller) ample time to gate the instruction and determine external priorities (*Figure 18*). This can be any instruction from one to four bytes. The most popular instruction is one-byte call (restart instruction) or a three-byte call (CALL NN instruction). If it is a three-byte call, the CPU issues a total of three $\overline{INTA}$ strobes. The last two (which do not include wait states) read NN.

Note: If the instruction stored in the ICU doesn't require the PC to be pushed onto the stack (eq. JP nn), then the PC will not be pushed.

Interrupt ($\overline{INTR}$) Mode 1: Similar to restart interrupts except the restart location is X'0038 (*Figure 18*).

Interrupt ($\overline{INTR}$) Mode 2: With this mode, the programmer maintains a table that contains the 16-bit starting address of every interrupt service routine. This table can be located anywhere in memory. When the CPU accepts a Mode 2 interrupt (*Figure 17*), it forms a 16-bit pointer to obtain the desired interrupt service routine starting address from the table. The upper 8 bits of this pointer are from the contents of the I register. The lower 8 bits of the pointer are supplied by the interrupting device with the LSB forced to zero. The programmer must load the interrupt vector prior to the interrupt occurring. The CPU uses the pointer to get the two adjacent bytes from the interrupt service routine starting address table to complete 16-bit service routine starting address. The first byte of each entry in the table is the least significant (low-order) portion of the address. The programmer must obviously fill this table with the desired addresses before any interrupts are to be accepted.

Note that the programmer can change this table at any time to allow peripherals to be serviced by different service routines. Once the interrupting device supplies the lower portion of the pointer, the CPU automatically pushes the program counter onto the stack, obtains the starting address from the table and does a jump to this address.

The interrupts have fixed priorities built into the NSC800 as:

$\overline{NMI}$	0066	(Highest Priority)
$\overline{RSTA}$	003C	
$\overline{RSTB}$	0034	
$\overline{RSTC}$	002C	
$\overline{INTR}$	0038	(Lowest Priority)

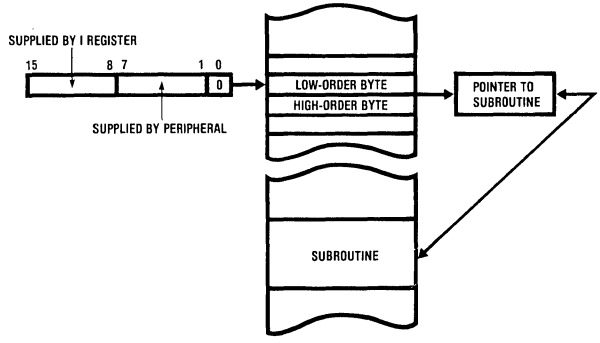
Interrupt Enable, Interrupt Disable. The NSC800 has two types of interrupt inputs, a non-maskable interrupt and four software maskable interrupts. The non-maskable interrupt ($\overline{NMI}$) cannot be disabled by the programmer and will be accepted whenever a peripheral device requests an interrupt. The $\overline{NMI}$ is usually reserved for important functions that must be serviced when they occur, such as imminent power failure. The programmer can selectively enable or disable maskable interrupts ($\overline{INT}$, $\overline{RSTA}$, $\overline{RSTB}$ and $\overline{RSTC}$). This selectivity allows the programmer to disable the maskable interrupts during periods when timing constraints don't allow program interruption.

There are two interrupt enable flip-flops (IFF_1 and IFF_2) on the NSC800. Two instructions control these flip-flops. Enable Interrupt (EI) and Disable Interrupt (DI). The state of IFF_1 determines the enabling or disabling of the maskable interrupts, while IFF_2 is used as a temporary storage location for the state of IFF_1.

9.0 Timing and Control (Continued)

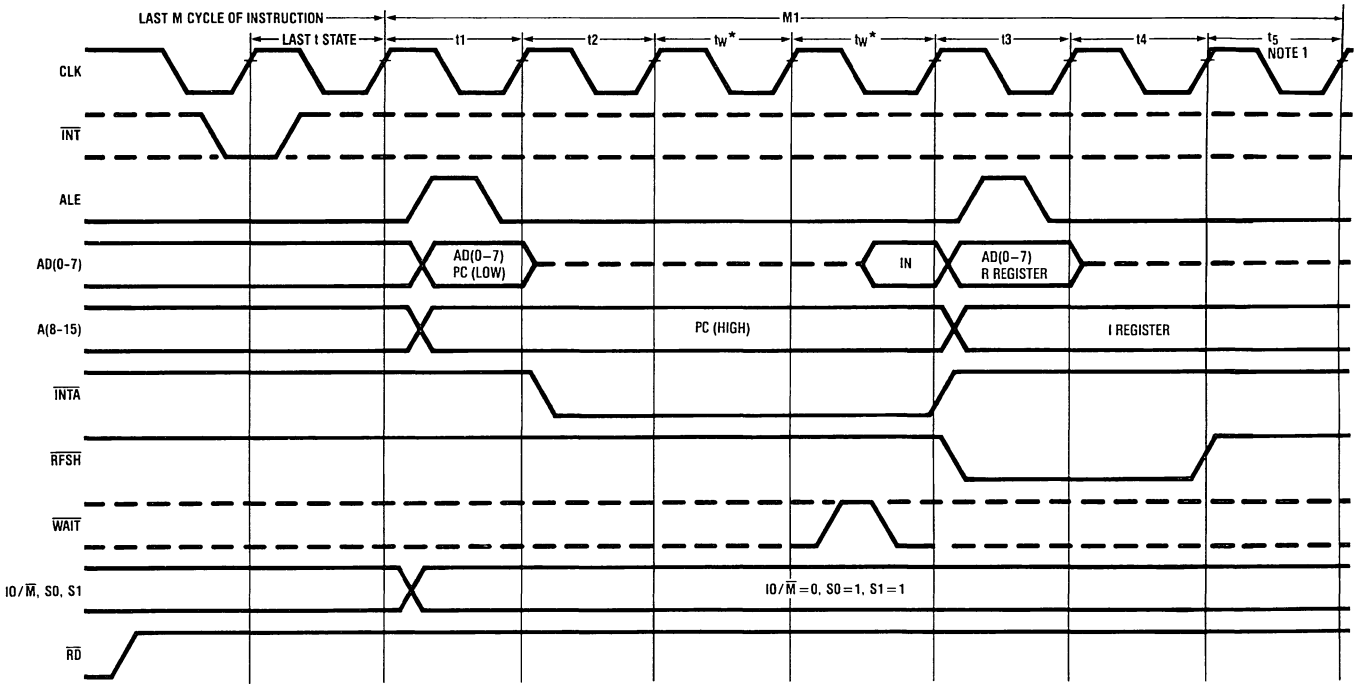
A reset to the CPU will force both IFF_1 and IFF_2 to the reset state disabling maskable interrupts. They can be enabled by an EI instruction at any time by the programmer. When an EI instruction is executed, any pending interrupt requests will not be accepted until after the instruction following EI has been executed. This single instruction delay is necessary in situations where the following instruction is a return instruction and interrupts must not be allowed until the return has been completed. The EI instruction sets both IFF_1 and IFF_2 to the enable state. When the CPU accepts an interrupt, both IFF_1 and IFF_2 are automatically reset, inhibiting further interrupts until the programmer wishes to issue a new EI instruction. Note that for all the previous cases, IFF_1 and IFF_2 are always equal.

The function of IFF_2 is to retain the status of IFF_1 when a non-maskable interrupt occurs. When a non-maskable interrupt is accepted, IFF_1 is reset to prevent further interrupts until reenabled by the programmer. Thus, after a non-maskable interrupt has been accepted, maskable interrupts are disabled but the previous state of IFF_1 is saved by IFF_2



TL/C/5171–27

FIGURE 17. Interrupt Mode 2



TL/C/5171–25

*t_W is the CPU generated WAIT state in response to an interrupt request.

Note 1: t5 will only occur in mode 1 and mode 2. During t5 the stack pointer is decremented.

Note 2: A jump to the appropriate address occurs here in mode 1 and mode 2. The CPU continues gathering data from the interrupting peripheral in mode 0 for a total of 2–4 machine cycles. In mode 0 cycles M2–M4 have only 1 wait state.

FIGURE 18. Interrupt Acknowledge Machine Cycle

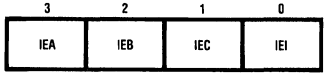
9.0 Timing and Control (Continued)

so that the complete state of the CPU just prior to the non-maskable interrupt may be restored. The method of restoring the status of IFF_1 is through the execution of a Return Non-Maskable Interrupt (RETN) instruction. Since this instruction indicates that the non-maskable interrupt service routine is completed, the contents of IFF_2 are now copied back into IFF_1, so that the status of IFF_1 just prior to the acceptance of the non-maskable interrupt will be automatically restored.

Figure 19 depicts the status of the flip flops during a sample series of interrupt instructions.

Interrupt Control Register. The interrupt control register (ICR) is a 4-bit, write only register that provides the programmer with a second level of maskable control over the four maskable interrupt inputs.

The ICR is internal to the NSC800 CPU, but is addressed through the I/O space at I/O address port X'BB. Each bit in the register controls a mask bit dedicated to each maskable interrupt, $\overline{RSTA}$, $\overline{RSTB}$, $\overline{RSTC}$ and $\overline{INTR}$. For an interrupt request to be accepted on any of these inputs, the corresponding mask bit in the ICR must be set (= 1) and IFF_1 and IFF_2 must be set. This provides the programmer with control over individual interrupt inputs rather than just a system wide enable or disable.



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Bit	Name	Function
0	IEI	Interrupt Enable for $\overline{INTR}$
1	IEC	Interrupt Enable for $\overline{RSTC}$
2	IEB	Interrupt Enable for $\overline{RSTB}$
3	IEA	Interrupt Enable for $\overline{RSTA}$

For example: In order to enable $\overline{RSTB}$, CPU interrupts must be enabled and IEB must be set.

At reset, IEI bit is set and other mask bits IEA, IEB, IEC are cleared. This maintains the software compatibility between NSC800 and Z80A.

Execution of an I/O block move instruction will not affect the state of the interrupt control bits. The only two instructions that will modify this write only register are OUT (C), r and OUT (N), A.

Operation	IFF_1	IFF_2	Comment
Initialize	0	0	Interrupt Disabled
•			
•			
•			
EI	1	1	Interrupt Enabled after
•			next instruction
•			
•			
$\overline{INTR}$	0	0	Interrupt Disable and $\overline{INTR}$
			Being Serviced
•			
•			
•			
EI	1	1	Interrupt Enabled after
			next instruction
RET	1	1	Interrupt Enabled
•			
•			
•			
$\overline{NMI}$	0	1	Interrupt Disabled
•			
•			
•			
RETN	1	1	Interrupt Enabled
•			
$\overline{INTR}$	0	0	Interrupt Disabled
•			
•			
•			
$\overline{NMI}$	0	0	Interrupt Disabled and $\overline{NMI}$
•			Being Serviced
•			
•			
RETN	0	0	Interrupt Disabled and $\overline{INTR}$
•			Being Serviced
•			
•			
EI	1	1	Interrupt Enabled after
			next instruction
RET	1	1	Interrupt Enabled
•			
•			
•			

FIGURE 19. IFF_1 and IFF_2 States Immediately after the Operation has been Completed

NSC800 SOFTWARE

10.0 Introduction

This chapter provides the reader with a detailed description of the NSC800 software. Each NSC800 instruction is described in terms of opcode, function, flags affected, timing, and addressing mode.

11.0 Addressing Modes

The following sections describe the addressing modes supported by the NSC800. Note that particular addressing modes are often restricted to certain types of instructions. Examples of instructions used in the particular addressing modes follow each mode description.

The 10 addressing modes and 158 instructions provide a flexible and powerful instruction set.

11.1 REGISTER

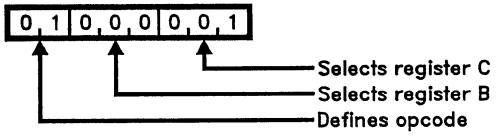
The most basic addressing mode is that which addresses data in the various CPU registers. In these cases, bits in the opcode select specific registers that are to be addressed by the instruction.

Example:

Instruction: Load register B from register C

Mnemonic: LD B,C

Opcode:



TL/C/5171–50

In this instruction, both the B and C registers are addressed by opcode bits.

11.2 IMPLIED

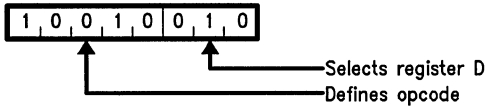
The implied addressing mode is an extension to the register addressing mode. In this mode, a specific register, the accumulator, is used in the execution of the instruction. In particular, arithmetic operations employ implied addressing, since the A register is assumed to be the destination register for the result without being specifically referenced in the opcode.

Example:

Instruction: Subtract the contents of register D from the Accumulator (A register)

Mnemonic: SUB D

Opcode:



TL/C/5171–51

In this instruction, the D register is addressed with register addressing, while the use of the A register is implied by the opcode.

11.3 IMMEDIATE

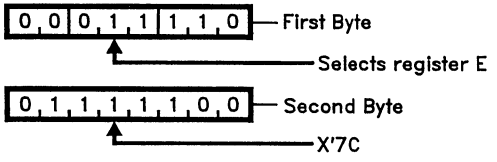
The most straightforward way of introducing data to the CPU registers is via immediate addressing, where the data is contained in an additional byte of multi-byte instructions.

Example:

Instruction: Load the E register with the constant value X'7C.

Mnemonic: LD E,X'7C

Opcode:



TL/C/5171–52

In this instruction, the E register is addressed with register addressing, while the constant X'7C is immediate data in the second byte of the instruction.

11.4 IMMEDIATE EXTENDED

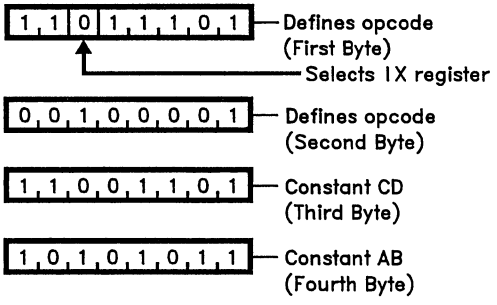
As immediate addressing allows 8 bits of data to be supplied by the operand, immediate extended addressing allows 16 bits of data to be supplied by the operand. These are in two additional bytes of the instruction.

Example:

Instruction: Load the 16-bit IX register with the constant value X'ABCD.

Mnemonic: LD IX,X'ABCD

Opcode:



TL/C/5171–53

In this instruction, register addressing selects the IX register, while the 16-bit quanity X'ABCD is immediate data supplied as immediate extended format.

11.0 Addressing Modes (Continued)

11.5 DIRECT ADDRESSING

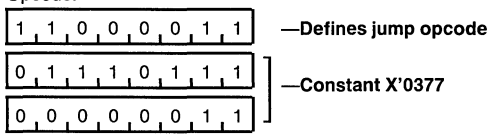
Direct addressing is the most straightforward way of addressing supplies a location in the memory space. Direct addressing, 16-bits of memory address information in two bytes of data as part of the instruction. The memory address could be either data, source of destination, or a location for program execution, as in program control instructions.

Example:

Instruction: Jump to location X'0377

Mnemonic: JP X'0377

Opcode:



This instruction loads the Program Counter (PC) is loaded with the constant in the second and third bytes of the instruction. The program counter contents are transferred via direct addressing.

11.6 REGISTER INDIRECT

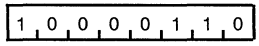
Next to direct addressing, register indirect addressing provides the second most straightforward means of addressing memory. In register indirect addressing, a specified register pair contains the address of the desired memory location. The instruction references the register pair and the register contents define the memory location of the operand.

Example:

Instruction: Add the contents of memory location X'0254 to the A register. The HL register contains X'0254.

Mnemonic: ADD A,(HL)

Opcode



This instruction uses implied addressing of the A and HL registers and register indirect addressing to access the data pointed to by the HL register.

11.7 INDEXED

The most flexible mode of memory addressing is the indexed mode. This is similar to the register indirect mode of addressing because one of the two index registers (IX or IY) contains the base memory address. In addition, a byte of data included in the instruction acts as a displacement to the address in the index register.

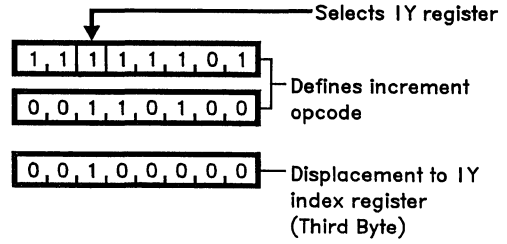
Indexed addressing is particularly useful in dealing with lists of data.

Example:

Instruction: Increment the data in memory location X'1020. The IY register contains X'1000.

Mnemonic: INC (IY+X'20)

Opcode:



TL/C/5171-54

The indexed addressing mode uses the contents of index registers IX or IY along with the displacement to form a pointer to memory.

11.8 RELATIVE

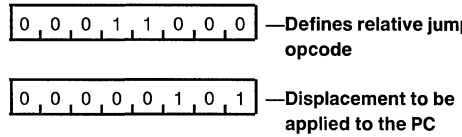
Certain instructions allow memory locations to be addressed as a position relative to the PC register. These instructions allow jumps to memory locations which are offsets around the program counter. The offset, together with the current program location, is determined through a displacement byte included in the instruction. The formation of this displacement byte is explained more fully in the "Instructions Set" section.

Example:

Instruction: Jump to a memory location 7 bytes beyond the current location.

Mnemonic: JR $+7

Opcode:



The program will continue at a location seven locations past the current PC.

11.0 Addressing Modes (Continued)

11.9 MODIFIED PAGE ZERO

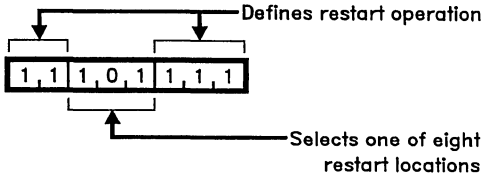
A subset of NSC800 instructions (the Restart instructions) provides a code-efficient single-byte instruction that allows CALLs to be performed to any one of eight dedicated locations in page zero (locations X'0000 to X'00FF). Normally, a CALL is a 3-byte instruction employing direct memory addressing.

Example:

Instruction: Perform a restart call to location X'0028.

Mnemonic: RST X'28

Opcode:



TL/C/5171–55

p	00H	08H	10H	18H	20H	28H	30H	38H
t	000	001	010	011	100	101	110	111

Program execution continues at location X'0028 after execution of a single-byte call employing modified page zero addressing.

11.10 BIT

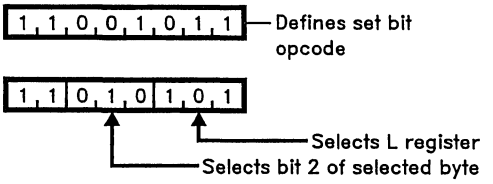
The NSC800 allows setting, resetting, and testing of individual bits in registers and memory data bytes.

Example:

Operation: Set bit 2 in the L register

Mnemonic: SET 2,L

Opcode:



TL/C/5171–56

Bit addressing allows the selection of bit 2 in the L register selected by register addressing.

12.0 Instruction Set

This section details the entire NSC800 instruction set in terms of

- Opcode
- Instruction
- Function
- Timing
- Addressing Mode

The instructions are grouped in order under the following functional headings:

- 8-Bit Loads
- 16-Bit Loads
- 8-Bit Arithmetic
- 16-Bit Arithmetic
- Bit Set, Reset, and Test
- Rotate and Shift
- Exchanges
- Memory Block Moves and Searches
- Input/Output
- CPU Control
- Program Control

12.1 Instruction Set Index

12.1 Instruction Set Index (Continued)

Alphabetical Assembly Mnemonic	Operation	Page
DI	Disable interrupts	9-56
DJNZ,d	Decrement B and jump relative B $\neq$ 0	9-58
EI	Enable interrupts	9-56
EX (SP),ss	Exchange the location (SP) with register ss	9-52
EX AF,A'F'	Exchange the contents of AF and A'F'	9-51
EX DE,HL	Exchange the contents of DE and HL	9-51
EXX	Exchange the contents of BC, DE and HL with the contents of B'C, D'E' and H'L', respectively	9-52
HALT	Halt (wait for interrupt or reset)	9-56
IM 0	Set interrupt mode 0	9-56
IM 1	Set interrupt mode 1	9-57
IM 2	Set interrupt mode 2	9-57
IN A,(n)	Load Accumulator with input from device (n)	9-54
IN r,(C)	Load register r with input from device (C)	9-54
INC m_1	Increment data in memory location m_1	9-44
INC r	Increment register r	9-39
INC rr	Increment contents of register pair rr	9-45
IND	Load location (HL) with input from port (C), decrement HL and B	9-54
INDR	Load location (HL) with input from port (C), decrement HL and B; repeat until B = 0	9-56
INI	Load location (HL) with input from port (C), increment HL, decrement B	9-54
INIR	Load location (HL) with input from port (C), increment HL, decrement B; repeat until B = 0	9-55
JP cc,nn	Jump to location nn, if condition cc is true	9-57
JP nn	Unconditional jump to location nn	9-57
JP (ss)	Unconditional jump to location (ss)	9-57
JR d	Unconditional jump relative to PC + d	9-57
JR kk,d	Jump relative to PC + d, if kk true	9-57
LD A,I	Load Accumulator with register I contents	9-34
LD A,m_2	Load Accumulator from location m_2	9-35
LD A,R	Load Accumulator with register R contents	9-34
LD I,A	Load register I with Accumulator contents	9-34
LD m_1,n	Load memory with immediate data n	9-35
LD m_1,r	Load memory from register r	9-34
LD m_2,A	Load memory from Accumulator	9-35
LD (nn),rr	Load memory location nn with register pair rr	9-36
LD r,m_1	Load register r from memory	9-35
LD r,n	Load register with immediate data n	9-34
LD R,A	Load register R from Accumulator	9-34
LD r_d,r_s	Load destination register r_d from source register r_s	9-34
LD rr,(nn)	Load register pair rr from memory location nn	9-37
LD rr,nn	Load register pair rr with immediate data nn	9-36
LD SP,ss	Load SP from register pair ss	9-36
LDD	Load location (DE) with location (HL), decrement DE, HL and BC	9-52
LDDR	Load location (DE) with location (HL), decrement DE, HL and BC; repeat until BC = 0	9-53
LDI	Load location (DE) with location (HL), increment DE and HL, decrement BC	9-52
LDIR	Load location (DE) with location (HL), increment DE and HL, decrement BC; repeat until BC = 0	9-53
NEG	Negate Accumulator (2's complement)	9-40
NOP	No operation	9-56

12.1 Instruction Set Index (Continued)

12.0 Instruction Set (Continued)

12.2 INSTRUCTION SET MNEMONIC NOTATION

In the following instruction set listing, the notations used are shown below.

b: Designates one bit in a register or memory location. Bit address mode uses this indicator.

cc: Designates condition codes used in conditional Jumps, Calls, and Return instruction; may be:

NZ = Non-Zero (Z flag = 0)
Z = Zero (Z flag = 1)
NC = Non-Carry (C flag = 0)
C = Carry (C flag = 1)
PO = Parity Odd or No Overflow (P/V = 0)
PE = Parity Even or Overflow (P/V = 1)
P = Positive (S = 0)
M = Negative (S = 1)

d: Designates an 8-bit signed complement displacement. Relative or indexed address modes use this indicator.

kk: Subset of cc condition codes used in conjunction with conditional relative jumps; may be NZ, Z, NC or C.

m_1: Designates (HL), (IX + d) or (IY + d). Register indirect or indexed address modes use this indicator.

m_2: Designates (BC), (DE) or (nn). Register indirect or direct address modes use this indicator.

n: Any 8-bit binary number.

nn: Any 16-bit binary number.

p: Designates restart vectors and may be the hex values 0, 8, 10, 18, 20, 28, 30 or 38. Restart instructions employing the modified page zero addressing mode use this indicator.

pp: Designates the BC, DE, SP or any 16-bit register used as a destination operand in 16-bit arithmetic operations employing the register address mode.

qq: Designates BC, DE, HL, A, F, IX, or IY during operations employing register address mode.

r: Designates A, B, C, D, E, H or L. Register addressing modes use this indicator.

rr: Designates BC, DE, HL, SP, IX or IY. Register addressing modes use this indicator.

ss: Designates HL, IX or IY. Register addressing modes use this indicator.

X_L: Subscript L indicates the lower-order byte of a 16-bit register.

X_H: Subscript H indicates the high-order byte of a 16-bit register.

( ): parentheses indicate the contents are considered a pointer address to a memory or I/O location.

12.3 ASSEMBLED OBJECT CODE NOTATION

Register Codes:

r	Register	rp	Register	rs	Register
000	B	00	BC	00	BC
001	C	01	DE	01	DE
010	D	10	HL	10	HL
011	E	11	SP	11	AF
100	H	**pp**	**Register**	**qq**	**Register**
101	L	00	BC	00	BC
111	A	01	DE	01	DE
		10	IX	10	HL
		11	SP	11	AF

Conditions Codes:

cc	Mnemonic	True Flag Condition
000	NZ	Z = 0
001	Z	Z = 1
010	NC	C = 0
011	C	C = 1
100	PO	P/V = 0
101	PE	P/V = 1
110	P	S = 0
111	M	S = 1
kk	**Mnemonic**	**True Flag Condition**
00	NZ	Z = 0
01	Z	Z = 1
10	NC	C = 0
11	C	C = 1

Restart Addresses:

t	T
000	X'00
001	X'08
010	X'10
011	X'18
100	X'20
101	X'28
110	X'30
111	X'38

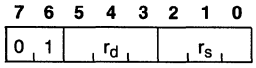
12.4 8-Bit Loads

REGISTER TO REGISTER

LD r_d, r_s

Load register r_d with r_s:

$r_d \leftarrow r_s$ No flags affected



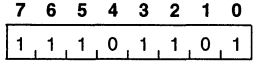
Timing: M cycles — 1
T states — 4

Addressing Mode: Register

LD A, I

Load Accumulator with the contents of the I register.

A ← I
S: Set if negative result
Z: Set if zero result
H: Reset
P/V: Set according to IFF_2 (zero if interrupt occurs during operation)
N: Reset
C: Not affected



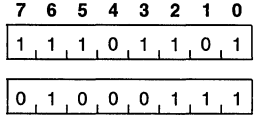
Timing: M cycles — 2
T states — 9 (4, 5)

Addressing Mode: Register

LD I, A

Load Interrupt vector register (I) with the contents of A.

I ← A No flags affected



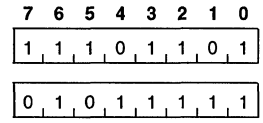
Timing: M cycles — 2
T states — 9 (4, 5)

Addressing Mode: Register

LD A, R

Load Accumulator with contents of R register.

A ← R
S: Set if negative result
Z: Set if zero result
H: Reset
P/V: Set according to IFF_2 (zero if interrupt occurs during operation)
N: Reset
C: Not affected



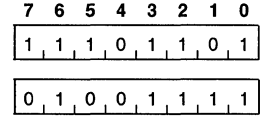
Timing: M cycles — 2
T states — 9 (4, 5)

Addressing Mode: Register

LD R, A

Load Refresh register (R) with contents of the Accumulator.

R ← A No flags affected



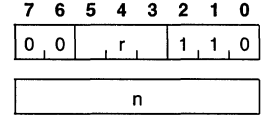
Timing: M cycles — 2
T states — 9 (4, 5)

Addressing Mode: Register

LD r, n

Load register r with immediate data n.

r ← n No flags affected



Timing: M cycles — 2
T states — 7 (4, 3)

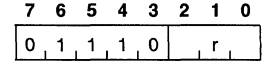
Addressing Mode: Source — Immediate
Destination — Register

REGISTER TO MEMORY

LD m_1, r

Load memory from reigster r.

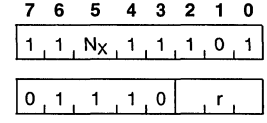
$m_1 \leftarrow r$ No flags affected



LD (HL), r

Timing: M cycles — 2
T states — 7 (4,3)

Addressing Mode: Source — Register
Destination — Register Indirect



LD (IX+d), r(for $N_X=0$)
LD (IY+d), r(for $N_X=1$)

Timing: M cycles — 2
T states — 19 (4, 4, 3, 5, 3)

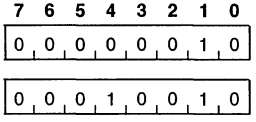
Addressing Mode: Source — Register
Destination — Indexed

12.4 8-Bit Loads (Continued)

LD m_2, A

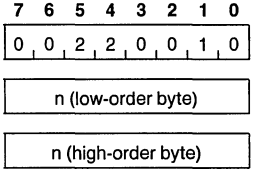
Load memory from the Accumulator.

$m_2 \leftarrow A$ No flags affected



Timing: M cycles — 2
T states — 7 (4, 3)

Addressing Mode: Source — Register (Implied)
Destination — Register Indirect



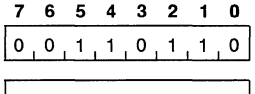
Timing: M cycles — 4
T states — 3 (4, 3, 3, 3)

Addressing Mode: Source — Register (Implied)
Destination — Direct

LD m_1, n

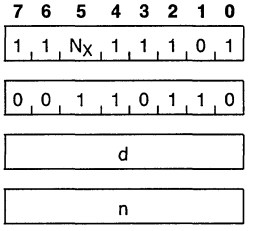
Load memory with immediate data.

$m_1 \leftarrow n$ No flags affected



Timing: M cycles—3
T states—10 (4, 3, 3)

Addressing Mode: Source—Immediate
Destination—Register Indirect



Timing: M cycles—5
T states—19 (4, 4, 3, 5, 3)

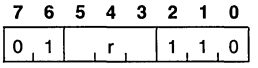
Addressing Mode: Source—Immediate
Destination—Indexed

MEMORY TO REGISTER

LD r, m_1

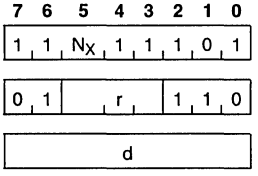
Load register r from memory location m_1.

$r \leftarrow m_1$ No flags affected



Timing: M cycles—2
T states—7 (4, 3)

Addressing Mode: Source—Register Indirect
Destination—Register



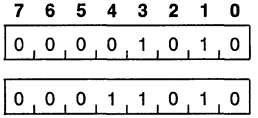
Timing: M cycles—5
T states—19 (4, 4, 3, 5, 3)

Addressing Mode: Source—Indexed
Destination—Register

LD A, m_2

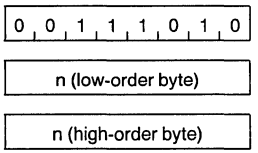
Load the Accumulator from memory location m_2.

$A \leftarrow m_2$ No flags affected



Timing: M cycles—2
T states—7 (4, 3)

Addressing Mode: Source—Register Indirect
Destination—Register (Implied)



Timing: M cycles—4
T states—13 (4, 3, 3, 3)

Addressing Mode: Source—Immediate Extended
Destination—Register (Implied)

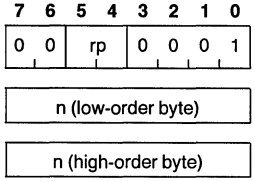
12.5 16-Bit Loads

REGISTER TO REGISTER

LD rr, nn

Load 16-bit register pair with immediate data.

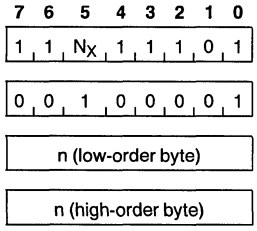
rr, ← nn — No flags affected



LD BC, nn
LD DE, nn
LD HL, nn
LD SP, nn

Timing: M cycles—3
T states—10 (4, 3, 3)

Addressing Mode: Source—Immediate Extended
Destination—Register



LD IX, nn (for $N_X = 0$)
LD IY, nn (for $N_X = 1$)

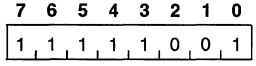
Timing: M cycles—4
T states—14 (4, 4, 3, 3)

Addressing Mode: Source—Immediate Extended
Destination—Register

LD SP, ss

Load the SP from 16-bit register ss.

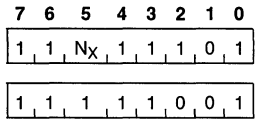
SP ← ss — No flags affected



LD SP, HL

Timing: M cycles—1
T states—6

Addressing Mode: Source—Register
Destination—Register (Implied)



LD SP, IX (for $N_X = 0$)
LD SP, IY (for $N_X = 1$)

Timing: M cycles—2
T states—10 (4, 6)

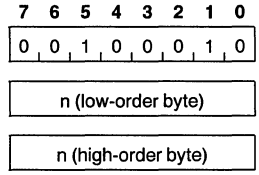
Addressing Mode: Source—Register
Destination—Register (Implied)

REGISTER TO MEMORY

LD (nn), rr

Load memory location nn with contents of 16-bit register, rr.

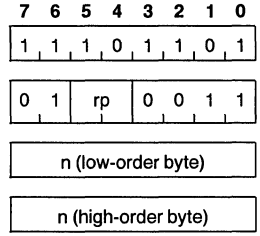
(nn) ← rr_L — No flags affected
(nn + 1) ← rr_H



LD (nn), HL
(note an alternate opcode below)

Timing: M cycles—5
T states—16 (4, 3, 3, 3, 3)

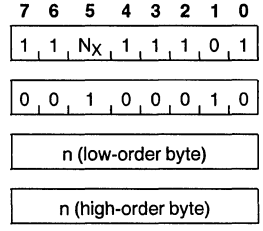
Addressing Mode: Source—Register
Destination—Direct



LD (nn), BC
LD (nn), DE
LD (nn), HL
LD (nn), SP

Timing: M cycles—6
T states—20 (4, 4, 3, 3, 3, 3)

Addressing Mode: Source—Register
Destination—Direct



LD (nn), IX (for $N_X = 0$)
LD (nn) IY (for $N_X = 1$)

Timing: M cycles—6
T states—20 (4, 4, 3, 3, 3, 3)

Addressing Mode: Source—Register
Destination—Direct

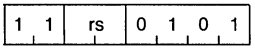
12.5 16-Bit Loads (Continued)

PUSH qq

Push the contents of register pair qq onto the memory stack.

$(SP - 1) \leftarrow qq_H$
$(SP - 2) \leftarrow qq_L$
$SP \leftarrow SP - 2$

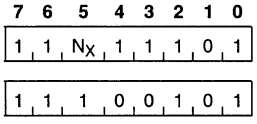
No flags affected



PUSH BC
PUSH DE
PUSH HL
PUSH AF

Timing: M cycles—3
T states—11 (5, 3, 3)

Addressing Mode: Source—Register
Destination—Register Indirect (Stack)



PUSH IX (for $N_X = 0$)
PUSH IY (for $N_X = 1$)

Timing: M cycles—3
T states—15 (4, 5, 3, 3)

Addressing Mode: Source—Register
Destination—Register Indirect (Stack)

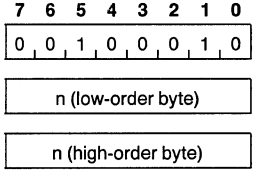
MEMORY TO REGISTER

LD rr, (nn)

Load 16-bit register from memory location nn.

$rr_L \leftarrow (nn)$
$rr_H \leftarrow (nn + 1)$

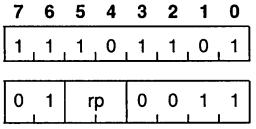
No flags affected



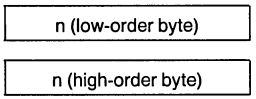
LD HL, (nn)
(note an alternate opcode below)

Timing: M cycles—5
T states—16 (4, 3, 3, 3, 3)

Addressing Mode: Source—Direct
Destination—Register

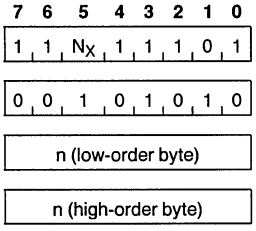


LD BC, (nn)
LD DE, (nn)
LD HL, (nn)
LD SP, (nn)



Timing: M cycles—6
T states—20 (4, 4, 3, 3, 3, 3)

Addressing Mode: Source—Direct
Destination—Register



LD IX, (nn)(for $N_X = 0$)
LD IY, (nn) (for $N_X = 1$)

Timing: M cycles—6
T states—20 (4, 4, 3, 3, 3, 3)

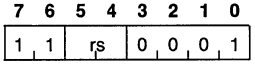
Addressing Mode: Source—Direct
Destination—Register

POP qq

Pop the contents of the memory stack to register qq.

$qq_L \leftarrow (SP)$
$qq_H \leftarrow (SP + 1)$
$SP \leftarrow SP + 2$

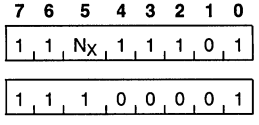
No flags affected



POP BC
POP DE
POP HL
POP AF

Timing: M cycles—3
T states—10 (4, 3, 3)

Addressing Mode: Source—Register Indirect (Stack)
Destination—Register



POP IX (for $N_X = 0$)
POP IY (for $N_X = 1$)

Timing: M cycles—4
T states—14 (4, 4, 3, 3)

Addressing Mode: Source—Register Indirect (Stack)
Destination—Register

12.6 8-Bit Arithmetic

REGISTER ADDRESSING ARITHMETIC

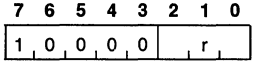
Op	C Before DAA	Hex Value In Upper Digit (Bits 7-4)	H Before DAA	Hex Value In Lower Digit (Bits 3-0)	Number Added To Byte	C After DAA
	0	0-9	0	0-9	00	0
	0	0-8	0	A-F	06	0
	0	0-9	1	0-3	06	0
ADD	0	A-F	0	0-9	60	1
ADC	0	9-F	0	A-F	66	1
INC	0	A-F	1	0-3	66	1
	1	0-2	0	0-9	60	1
	1	0-2	0	A-F	66	1
	1	0-3	1	0-3	66	1
SUB	0	0-9	0	0-9	00	0
SBC	0	0-8	1	6-F	FA	0
DEC	1	7-F	0	0-9	A0	1
NEG	1	6-F	1	6-F	9A	1

ADD A, r

Add contents of register r to the Accumulator.

A ← A+r

S: Set if negative result
Z: Set if zero result
H: Set if carry from bit 3
P/V: Set according to overflow condition
N: Reset
C: Set if carry from bit 7



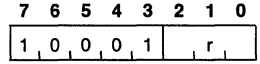
Timing: M cycles—1, T states—4
Addressing Mode: Source—Register, Destination—Implied

ADC A, r

Add contents of register r, plus the carry flag, to the Accumulator.

A ← A + r + CY

S: Set if negative result
Z: Set if zero result
H: Set if carry from bit 3
P/V: Set if result exceeds 2's complement range
N: Reset
C: Set if carry from bit 7



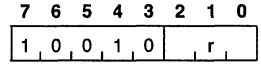
Timing: M cycles—1, T states—4
Addressing Mode: Source—Register, Destination—Implied

SUB r

Subtract the contents of register r from the Accumulator.

A ← A − r

S: Set if result is negative
Z: Set if result is zero
H: Set if borrow from bit 4
P/V: Set if result exceeds 8-bit 2's complement range
N: Set
C: Set according to borrow



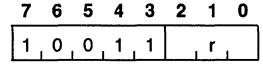
Timing: M cycles—1, T states—4
Addressing Mode: Source—Register, Destination—Implied

SBC A, r

Subtract contents of register r and the carry bit C from the Accumulator.

A ← A − r − CY

S: Set if result is negative
Z: Set if result is zero
H: Set if borrow from bit 4
P/V: Set if result exceeds 8-bit 2's complement range
N: Set
C: Set according to borrow



Timing: M cycles—1, T states—4
Addressing Mode: Source—Register, Destination—Implied

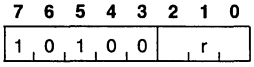
AND r

Logically AND the contents of the r register and the Accumulator.

A ← A ∧ r

S: Set if result is negative
Z: Set if result is zero
H: Set
P/V: Set if result parity is even
N: Reset
C: Reset

12.6 8-Bit Arithmetic (Continued)



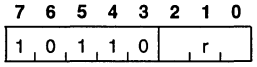
Timing: M cycles—1
T states—4
Addressing Mode: Source—Register
Destination—Implied

OR r

Logically OR the contents of the r register and the Accumulator.

A ← A ∨ r

S: Set if result is negative
Z: Set if result is zero
H: Reset
P/V: Set if result parity is even
N: Reset
C: Reset



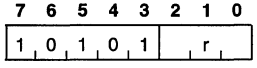
Timing: M cycles—1
T states—4
Addressing Mode: Source—Register
Destination—Implied

XOR r

Logically exclusively OR the contents of the r register with the Accumulator.

A ← A ⊕ r

S: Set if result is negative
Z: Set if result is zero
H: Reset
P/V: Set if result parity is even
N: Reset
C: Reset



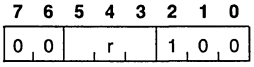
Timing: M cycles—1
T states—4
Addressing Mode: Source—Register
Destination—Implied

INC r

Increment register r.

r ← r + 1

S: Set if result is negative
Z: Set if result is zero
H: Set if carry from bit 3
P/V: Set only if r was X'7F before operation
N: Reset
C: N/A



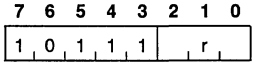
Timing: M cycles—1
T states—4
Addressing Mode: Source—Register
Destination—Register

CP r

Compare the contents of register r with the Accumulator and set the flags accordingly.

A − r

S: Set if result is negative
Z: Set if result is zero
H: Set if borrow from bit 4
P/V: Set if result exceeds 8-bit 2's complement range
N: Set
C: Set according to borrow



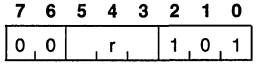
Timing: M cycles—1
T states—4
Addressing Mode: Source—Register
Destination—Implied

DEC r

Decrement the contents of register r.

r ← r − 1

S: Set if result is negative
Z: Set if result is zero
H: Set according to a borrow from bit 4
P/V: Set only if r was X'80 prior to operation
N: Set
C: N/A



Timing: M cycles—1
T states—4
Addressing Mode: Source—Register
Destination—Register

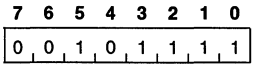
CPL

Complement the Accumulator (1's complement).

A ← $\overline{A}$

S: N/A
Z: N/A
H: Set
P/V: N/A
N: Set
C: N/A

12.6 8-Bit Arithmetic (Continued)



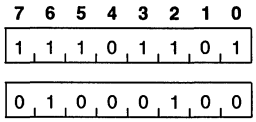
Timing: M cycles—1
T states—4
Addressing Mode: Implied

NEG

Negate the Accumulator (2's complement).

A ← 0 − A

S: Set if result is negative
Z: Set if result is zero
H: Set according to borrow from bit 4
P/V: Set only if Accumulator was X'80 prior to operation
N: Set
C: Set only if Accumulator was not X'00 prior to operation



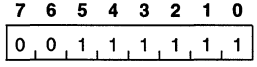
Timing: M cycles—2
T states—8 (4, 4)
Addressing Mode: Implied

CCF

Complement the carry flag.

CY ← $\overline{CY}$

S: N/A
Z: N/A
H: Previous carry
P/V: N/A
N: Reset
C: Complement of previous carry



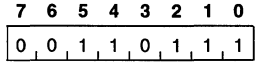
Timing: M cycles—1
T states—4
Addressing Mode: Implied

SCF

Set the carry flag.

CY ← 1

S: N/A
Z: N/A
H: Reset
P/V: N/A
N: Reset
C: Set

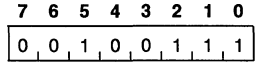


Timing: M cycles—1
T states—4
Addressing Mode: Implied

DAA

Adjust the Accumulator for BCD addition and subtraction operations. To be executed after BCD data has been operated upon the standard binary ADD, ADC, INC, SUB, SBC, DEC or NEG instructions (see "Register Addressing Arithmetic" table).

———
S: Set according to bit 7 of result
Z: Set if result is zero
H: Set according to instructions
P/V: Set according to parity of result
N: N/A
C: Set according to instructions



Timing: M cycles—1
T states—4
Addressing Mode: Implied

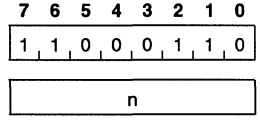
IMMEDIATELY ADDRESSED ARITHMETIC

ADD A, n

Add the immediate data n to the Accumulator.

A ← A + n

S: Set if result is negative
Z: Set if result is zero
H: Set if carry from bit 3
P/V: Set if result exceeds 8-bit 2's complement range
N: Reset
C: Set if carry from bit 7



Timing: M cycles—2
T states—7 (4, 3)
Addressing Mode: Source—Immediate
Destination—Implied

ADC A, n

Add, with carry, the immediate data n and the Accumulator.

A ← A + n + CY

S: Set if result is negative
Z: Set if result is zero
H: Set if carry from bit 3
P/V: Set if result exceeds 8-bit 2's complement range
N: Reset
C: Set according to carry from bit 7

12.6 8-Bit Arithmetic (Continued)

7	6	5	4	3	2	1	0
1	1	0	0	1	1	1	0
n							

Timing: M cycles—2
T states—7 (4, 3)
Addressing Mode: Source—Immediate
Destination—Implied

SUB n

Subtract the immediate data n from the Accumulator.

A ← A − n

S: Set if result is negative
Z: Set if result is zero
H: Set if borrow from bit 4
P/V: Set if result exceeds 8-bit 2's complement range
N: Set
C: Set according to borrow condition

7	6	5	4	3	2	1	0
1	1	0	1	0	1	1	0
n							

Timing: M cycles—2
T states—7 (4, 3)
Addressing Mode: Source—Immediate
Destination—Implied

SBC A, n

Subtract, with carry, the immediate data n from the Accumulator.

A ← A − n − CY

S: Set if result is negative
Z: Set if result is zero
H: Set if borrow from bit 4
P/V: Set if result exceeds 8-bit 2's complement range
N: Set
C: Set according to borrow condition

7	6	5	4	3	2	1	0
1	1	0	1	1	1	1	0
n							

Timing: M cycles—2
T states—7 (4, 3)
Addressing Mode: Source—Immediate
Destination—Implied

AND n

The immediate data n is logically AND'ed to the Accumulator.

A ← A ∧ n

S: Set if result is negative
Z: Set if result is zero
H: Set
P/V: Set if result parity is even
N: Reset
C: Reset

7	6	5	4	3	2	1	0
1	1	1	0	0	1	1	0
n							

Timing: M cycles—2
T states—7 (4, 3)
Addressing Mode: Source—Immediate
Destination—Implied

OR n

The immediate data n is logically OR'ed to the contents of the Accumulator.

A ← A ∨ s

S: Set if result is negative
Z: Set if result is zero
H: Reset
P/V: Set if result parity is even
N: Reset
C: Reset

7	6	5	4	3	2	1	0
1	1	1	1	0	1	1	0
n							

Timing: M cycles—2
T states—7 (4, 3)
Addressing Mode: Source—Immediate
Destination—Implied

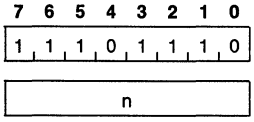
XOR n

The immediate data n is exclusively OR'ed with the Accumulator.

A ← A ⊕ n

S: Set if result is negative
Z: Set if result is zero
H: Reset
P/V: Set if result parity is even
N: Reset
C: Reset

12.6 8-Bit Arithmetic (Continued)



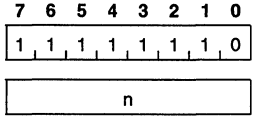
Timing: M cycles—2
T states—7 (4, 3)
Addressing Mode: Source—Immediate
Destination—Implied

CP n

Compare the immediate data n with the contents of the Accumulator via subtraction and return the appropriate flags. The contents of the Accumulator are not affected.

A − n

S: Set if result is negative
Z: Set if result is zero
H: Set if borrow from bit 4
P/V: Set if result exceeds 8-bit 2's complement range
N: Set
C: Set according to borrow condition



Timing: M cycles—2
T states—7 (4, 3)
Addressing Mode: Immediate

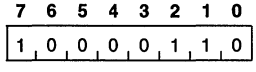
MEMORY ADDRESSED ARITHMETIC

ADD A, m1

Add the contents of the memory location m_1 to the Accumulator.

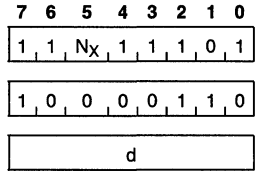
A ← A + m_1

S: Set if result is negative
Z: Set if result is zero
H: Set if carry from bit 3
P/V: Set if result exceeds 8-bit 2's complement range
N: Reset
C: Set according to carry from bit 7



ADD A, (HL)

Timing: M cycles—2
T states—7 (4, 3)
Addressing Mode: Source—Register Indirect
Destination—Implied



ADD A, (IX + d) (for N_X=0)
ADD A, (IY + d) (for N_X=1)

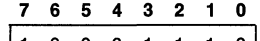
Timing: M cycles—5
T states—19 (4, 4, 3, 5, 3)
Addressing Mode: Source—Indexed
Destination—Implied

ADC A, m_1

Add the contents of the memory location m_1 plus the carry to the Accumulator.

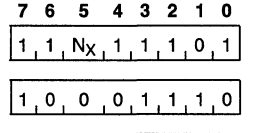
A ← A + m_1 + CY

S: Set if result is negative
Z: Set if result is zero
H: Set if carry from bit 3
P/V: Set if result exceeds 8-bit 2's complement range
N: Reset
C: Set according to carry from bit 7



ADC A, (HL)

Timing: M cycles—2
T states—7 (4, 3)
Addressing Mode: Source—Register Indirect
Destination—Implied



ADC A, (IX + d) (for N_X=0)
ADC A, (IY + d) (for N_X=1)

Timing: M cycles—5
T states—19 (4, 4, 3, 5, 3)
Addressing Mode: Source—Indexed
Destination—Implied

SUB m_1

Subtract the contents of memory location m_1 from the Accumulator.

A ← A − m_1

S: Set if result is negative
Z: Set if result is zero
H: Set if borrow from bit 4
P/V: Set if result exceeds 8-bit 2's complement range
N: Set
C: Set according to borrow condition

12.6 8-Bit Arithmetic (Continued)

7	6	5	4	3	2	1	0	
1	0	0	1	0	1	1	0	SUB (HL)

Timing: M cycles—2
T states—7 (4, 3)
Addressing Mode: Source—Register Indirect
Destination—Implied

7	6	5	4	3	2	1	0	
1	1	N_X	1	1	1	0	1	SUB (IX + d) (for $N_X=0$) SUB (IY + d) (for $N_X=1$)
1	0	0	1	0	1	1	0	
d								

Timing: M cycles—5
T states—19 (4, 4, 3, 5, 3)
Addressing Mode: Source—Indexed
Destination—Implied

SBC A, m_1

Subtract, with carry, the contents of memory location m_1 from the Accumulator.

$A \leftarrow A - m_1 - CY$

S: Set if result is negative
Z: Set if result is zero
H: Set if carry from bit 3
P/V: Set if result exceeds 8-bit 2's complement range
N: Set
C: Set according to borrow condition

7	6	5	4	3	2	1	0	
1	0	0	1	1	1	1	0	SBC A, (HL)

Timing: M cycles—2
T states—7 (4, 3)
Addressing Mode: Source—Register Indirect
Destination—Implied

7	6	5	4	3	2	1	0	
1	1	N_X	1	1	1	0	1	SBC A, (IX + d) (for $N_X=0$) SBC A, (IY + d) (for $N_X=1$)
1	0	0	1	1	1	1	0	
d								

Timing: M cycles—5
T states—19 (4, 4, 3, 5, 3)
Addressing Mode: Source—Indexed
Destination—Implied

AND m_1

The data in memory location m_1 is logically AND'ed to the Accumulator.

$A \leftarrow A \wedge m_1$

S: Set if result is negative
Z: Set if result is zero
H: Set
P/V: Set if result parity is even
N: Reset
C: Reset

7	6	5	4	3	2	1	0	
1	0	1	0	0	1	1	0	AND (HL)

Timing: M cycles—2
T states—7 (4, 3)
Addressing Mode: Source—Register Indirect
Destination—Implied

7	6	5	4	3	2	1	0	
1	1	N_X	1	1	1	0	1	AND (IX + d) (for $N_X=0$) AND (IY + d) (for $N_X=1$)
1	0	1	0	0	1	1	0	
d								

Timing: M cycles—5
T states—19 (4, 4, 3, 5, 3)
Addressing Mode: Source—Indexed
Destination—Implied

OR m_1

The data in memory location m_1 is logically OR'ed with the Accumulator.

$A \leftarrow A \vee m_1$

S: Set if result is negative
Z: Set if result is zero
H: Reset
P/V: Set if result parity is even
N: Reset
C: Reset

7	6	5	4	3	2	1	0	
1	0	1	1	0	1	1	0	OR (HL)

Timing: M cycles—2
T states—7 (4, 3)
Addressing Mode: Source—Register Indexed
Destination—Implied

7	6	5	4	3	2	1	0	
1	1	N_X	1	1	1	0	1	OR (IX + d) (for $N_X=0$) OR (IY + d) (for $N_X=1$)
1	0	1	1	0	1	1	0	
d								

Timing: M cycles—5
T states—19 (4, 4, 3, 5, 3)
Addressing Mode: Source—Indexed
Destination—Implied

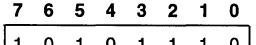
12.6 8-Bit Arithmetic (Continued)

XOR m_1

The data in memory location m_1 is exclusively OR'ed with the data in the Accumulator.

$A \leftarrow A \oplus m_1$

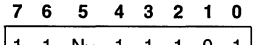
S: Set if result is negative
Z: Set if result is zero
H: Reset
P/V: Set if result parity is even
N: Reset
C: Reset



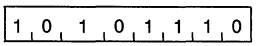
XOR (HL)

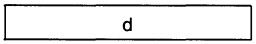
Timing: M cycles—2
T states—7 (4, 3)

Addressing Mode: Source—Register Indexed
Destination—Implied



XOR (IX + d) (for $N_X = 0$)
XOR (IY + d) (for $N_X = 1$)





Timing: M cycles—5
T states—19 (4, 4, 3, 5, 3)

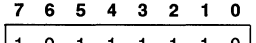
Addressing Mode: Source—Indexed
Destination—Implied

CP m_1

Compare the data in memory location m_1 with the data in the Accumulator via subtraction.

$A - m_1$

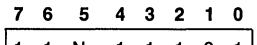
S: Set if result is negative
Z: Set if result is zero
H: Set if borrow from bit 4
P/V: Set if result exceeds 8-bit 2's complement range
N: Set
C: Set according to borrow condition



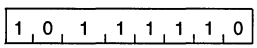
CP (HL)

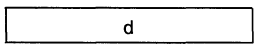
Timing: M cycles—2
T states—7 (4, 3)

Addressing Mode: Source—Register Indirect
Destination—Implied



CP (IX + d) (for $N_X = 0$)
CP (IY + d) (for $N_X = 1$)





Timing: M cycles—5
T states—19 (4, 4, 3, 5, 3)

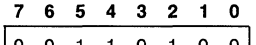
Addressing Mode: Source—Indexed
Destination—Implied

INC m_1

Increment data in memory location m_1.

$m_1 \leftarrow m_1 + 1$

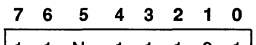
S: Set if result is negative
Z: Set if result is zero
H: Set according to carry from bit 3
P/V: Set if data was X'7F before operation
N: Reset
C: N/A



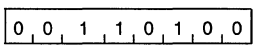
INC (HL)

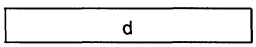
Timing: M cycles—3
T states—11 (4, 4, 3)

Addressing Mode: Source—Register Indexed
Destination—Register Indexed



INC (IX + d) (for $N_X = 0$)
INC (IY + d) (for $N_X = 1$)





Timing: M cycles—6
T states—23 (4, 4, 3, 5, 4, 3)

Addressing Mode: Source—Indexed
Destination—Indexed

DEC m_1

Decrement data in memory location m_1.

$m_1 \leftarrow m_1 - 1$

S: Set if result is negative
Z: Set if result is zero
H: Set according to borrow from bit 4
P/V: Set only if m_1 was X'80 before operation
N: Set
C: N/A

12.6 8-Bit Arithmetic (Continued)

7	6	5	4	3	2	1	0	
0	0	1	1	0	1	0	1	DEC (HL)

Timing: M cycles — 3
T states — 11 (4, 4, 3)
Addressing Mode: Source — Register Indexed
Destination — Register Indexed

7	6	5	4	3	2	1	0	
1	1	N_X	1	1	1	0	1	DEC (IX + d) (for $N_X = 0$) / DEC (IY + d) (for $N_X = 1$)
0	0	1	1	0	1	0	1	
d								

Timing: M cycles — 6
T states — 23 (4, 4, 3, 5, 4, 3)
Addressing Mode: Source — Indexed
Destination — Indexed

12.7 16-Bit Arithmetic

ADD ss, pp

Add the contents of the 16-bit register pp to the contents of the 16-bit register ss.

ss ← ss + pp
S: N/A
Z: N/A
H: Set if carry from bit 11
P/V: N/A
N: Reset
C: Set if carry from bit 15

7	6	5	4	3	2	1	0	
0	0	pp		1	0	0	1	ADD HL, pp

Timing: M cycles — 3
T states — 11 (4, 4, 3)
Addressing Mode: Source — Register
Destination — Register

7	6	5	4	3	2	1	0	
1	1	N_X	1	1	1	0	1	ADD IX, pp (for $N_X = 0$) / ADD IY, pp (for $N_X = 1$)
0	0	pp		1	0	0	1	

Timing: M cycles — 4
T states — 15 (4, 4, 4, 3)
Addressing Mode: Source — Register
Destination — Register

ADC HL, pp

The contents of the 16-bit register pp are added, with the carry bit, to the HL register.

HL ← HL + pp + CY
S: Set if result is negative
Z: Set if result is zero
H: Set according to carry out of bit 11
P/V: Set if result exceeds 16-bit 2's complement range
N: Reset
C: Set if carry out of bit 15

7	6	5	4	3	2	1	0	
1	1	1	0	1	1	0	1	
0	1	pp		1	0	1	0	

Timing: M cycles — 4
T states — 15 (4, 4, 4, 3)
Addressing Mode: Source — Register
Destination — Register

SBC HL, pp

Subtract, with carry, the contents of the 16-bit pp register from the 16-bit HL register.

HL ← HL − pp − CY
S: Set if result is negative
Z: Set if result is zero
H: Set according to borrow from bit 12
P/V: Set if result exceeds 16-bit 2's complement range
N: Set
C: Set according to borrow condition

7	6	5	4	3	2	1	0	
1	1	1	0	1	1	0	1	
0	1	pp		0	0	1	0	

Timing: M cycles — 4
T states — 15 (4, 4, 4, 3)
Addressing Mode: Source — Register
Destination — Register

INC rr

Increment the contents of the 16-bit register rr.

rr ← rr + 1
No flags affected

7	6	5	4	3	2	1	0	
0	0	rp		0	0	1	1	INC BC / INC DE / INC HL / INC SP

Timing: M cycles — 1
T states — 6
Addressing Mode: Register

7	6	5	4	3	2	1	0	
1	1	N_X	1	1	1	0	1	INC IX (for $N_X = 0$) / INC IY (for $N_X = 1$)
0	0	1	0	0	0	1	1	

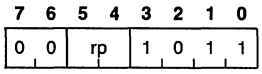
Timing: M cycles — 2
T states — 10 (4, 6)
Addressing Mode: Register

12.7 16-Bit Arithmetic (Continued)

DEC rr

Decrement the contents of the 16-bit register rr.

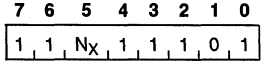
rr ← rr − 1 No flags affected



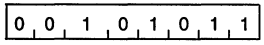
DEC BC
DEC DE
DEC HL
DEC SP

Timing: M cycles — 1
T states — 6

Addressing Mode: Register



DEC IX (for $N_X=0$)
DEC IY (for $N_X=1$)



Timing: M cycles — 2
T states — 10 (4, 6)

Addressing Mode: Register

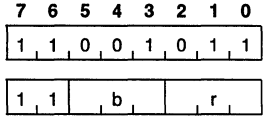
12.8 Bit Set, Reset, and Test

REGISTER

SET b, r

Bit b in register r is set.

R_b ← 1 No flags affected



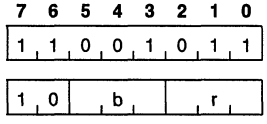
Timing: M cycles — 2
T states — 8 (4, 4)

Addressing Mode: Bit/Register

RES b, r

Bit b in register r is reset.

r_b ← 0 No flags affected



Timing: M cycles — 2
T states — 8 (4, 4)

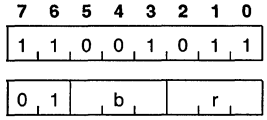
Addressing Mode: Bit/Register

BIT b, r

Bit b in register r is tested with the result put in the Z flag.

Z ← $\overline{r_b}$

S: Undefined
Z: Inverse of tested bit
H: Set
P/V: Undefined
N: Reset
C: N/A



Timing: M cycles — 2
T states — 8 (4, 4)

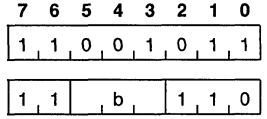
Addressing Mode: Bit/Register

MEMORY

SET b, m_1

Bit b in memory location m_1 is set.

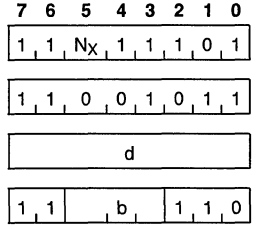
m_{1b} ← 1 No flags affected



SET b, (HL)

Timing: M cycles — 4
T states — 15 (4, 4, 4, 3)

Addressing Mode: Bit/Register Indirect



SET b, (IX+d) (for $N_X=0$)
SET b, (IY+d) (for $N_X=1$)

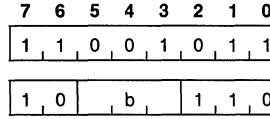
Timing: M cycles — 6
T states — 23 (4, 4, 3, 5, 4, 3)

Addressing Mode: Bit/Indexed

RES b, m_1

Bit b in memory location m_1 is reset.

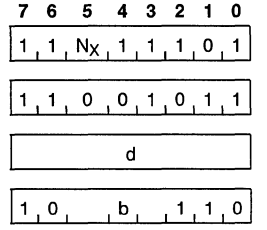
m_{1b} ← 0 No flags affected



RES b, (HL)

Timing: M cycles — 4
T states — 15 (4, 4, 4, 3)

Addressing Mode: Bit/Register Indirect



RES b, (IX+d) (for $N_X=0$)
RES b, (IY+d) (for $N_X=1$)

Timing: M cycles — 6
T states — 23 (4, 4, 3, 5, 4, 3)

Addressing Mode: Bit/Indexed

12.8 Bit Set, Reset, and Test (Continued)

BIT b, m_1

Bit b in memory location m_1 is tested via the Z flag.

$Z \leftarrow \overline{m_{1b}}$

S: Undefined
Z: Inverse of tested bit
H: Set
P/V: Undefined
N: Reset
C: N/A

7	6	5	4	3	2	1	0	
1	1	0	0	1	0	1	1	BIT b, (HL)
0	1	b				1	1	0

Timing: M cycles — 3
T states — 12 (4, 4, 4)

Addressing Mode: Bit/Register Indirect

7	6	5	4	3	2	1	0	
1	1	N_X	1	1	1	0	1	BIT b, (IX+d) (for $N_X=0$) / BIT b, (IY+d) (for $N_X=1$)
1	1	0	0	1	0	1	1	
d								
0	1	b				1	1	0

Timing: M cycles — 5
T states — 20 (4, 4, 3, 5, 4)

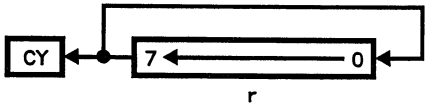
Addressing Mode: Bit/Indexed

12.9 Rotate and Shift

REGISTER

RLC r

Rotate register r left circular.



TL/C/5171-57

S: Set if result is negative
Z: Set if result is zero
H: Reset
P/V: Set if result parity is even
N: Reset
C: Set according to bit 7 of r

7	6	5	4	3	2	1	0	
1	1	0	0	1	0	1	1	RLC r
0	0	0	0	0		r		(Note alternate for A register below)

Timing: M cycles — 2
T states — 8 (4, 4)

Addressing Mode: Register

7	6	5	4	3	2	1	0	
0	0	0	0	0	1	1	1	RLCA

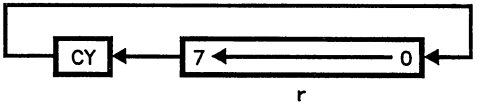
Timing: M cycles — 1
T states — 4

Addressing Mode: Implied

(Note RLCA does not affect S, Z, or P/V flags.)

RL r

Rotate register r left through carry.



TL/C/5171-58

S: Set if result is negative
Z: Set if result is zero
H: Reset
P/V: Set if result parity is even
N: Reset
C: Set according to bit 7 of r

7	6	5	4	3	2	1	0	
1	1	0	0	1	0	1	1	RL r
0	0	0	1	0		r		(Note alternate for A register below)

Timing: M cycles — 2
T states — 8 (4, 4)

Addressing Mode: Register

7	6	5	4	3	2	1	0	
0	0	0	1	0	1	1	1	RLA

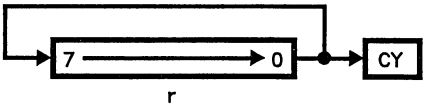
Timing: M cycles — 1
T states — 4

Addressing Mode: Implied

(Note RLA does not affect S, Z, or P/V flags.)

RRC r

Rotate register r right circular.



TL/C/5171-59

S: Set if result is negative
Z: Set if result is zero
H: Reset
P/V: Set if result parity is even
N: Reset
C: Set according to bit 0 of r

12.9 Rotate and Shift (Continued)

7	6	5	4	3	2	1	0	
1	1	0	0	1	0	1	1	RRC r
0	0	0	0	1	r			(Note alternate for A register below)

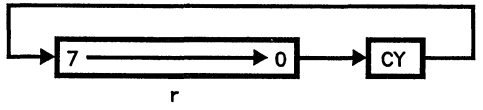
Timing: M cycles — 2
T states — 8 (4, 4)
Addressing Mode: Register

7	6	5	4	3	2	1	0	
0	0	0	0	1	1	1	1	RRCA

Timing: M cycles — 1
T states — 4
Addressing Mode: Implied
(Note RRCA does not affect S, Z, or P/V flags.)

RR r

Rotate register r right through carry.



TL/C/5171–60

S: Set if result is negative
Z: Set if result is zero
H: Reset
P/V: Set if result parity is even
N: Reset
C: Set according to bit 0 of r

7	6	5	4	3	2	1	0	
1	1	0	0	1	0	0	1	RR r
0	0	0	1	1	r			(Note alternate for A register below)

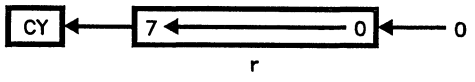
Timing: M cycles — 2
T states — 8 (4, 4)
Addressing Mode: Register

7	6	5	4	3	2	1	0	
0	0	0	1	1	1	1	1	RRA

Timing: M cycles — 1
T states — 4
Addressing Mode: Implied
(Note RRA does not affect S, Z, or P/V flags.)

SLA r

Shift register r left arithmetic.



TL/C/5171–61

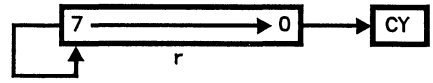
S: Set if result is negative
Z: Set if result is zero
H: Reset
P/V: Set if result parity is even
N: Reset
C: Set according to bit 7 of r

7	6	5	4	3	2	1	0	
1	1	0	0	1	0	1	1	
0	0	1	0	0	r			

Timing: M cycles — 2
T states — 8 (4, 4)
Addressing Mode: Register

SRA r

Shift register r right arithmetic.



TL/C/5171–62

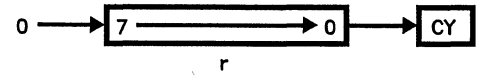
S: Set if result is negative
Z: Set if result is zero
H: Reset
P/V: Set if result parity is even
N: Reset
C: Set according to bit 0 of r

7	6	5	4	3	2	1	0	
1	1	0	0	1	0	1	1	
0	0	1	0	1	r			

Timing: M cycles — 2
T states — 8 (4, 4)
Addressing Mode: Register

SRL r

Shift register r right logical.



TL/C/5171–63

S: Reset
Z: Set if result is zero
H: Reset
P/V: Set if result parity is even
N: Reset
C: Set according to bit 0 of r

7	6	5	4	3	2	1	0	
1	1	0	0	1	0	1	1	
0	0	1	1	1	r			

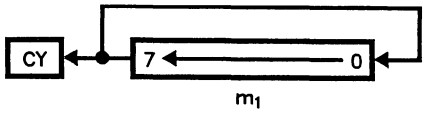
Timing: M cycles — 2
T states — 8 (4, 4)
Addressing Mode: Register

12.9 Rotate and Shift (Continued)

MEMORY

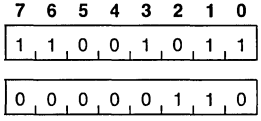
RLC m_1

Rotate date in memory location m_1 left circular.



TL/C/5171–64

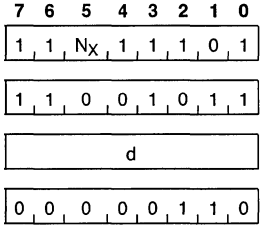
S: Set if result is negative
Z: Set if result is zero
H: Reset
P/V: Set if result parity is even
N: Reset
C: Set according to bit 7 of m_1



RLC (HL)

Timing: M cycles — 4
T states — 15 (4, 4, 4, 3)

Addressing Mode: Register indirect



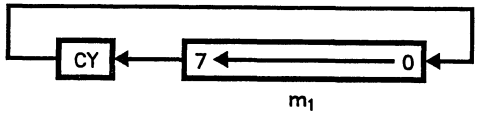
RLC (IX+d) (for $N_X=0$)
RLC (IY+d) (for $N_X=1$)

Timing: M cycles — 6
T states — 23 (4, 4, 3, 5, 4, 3)

Addressing Mode: Indexed

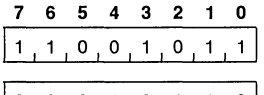
RL m_1

Rotate the data in memory location m_1 left though carry.



TL/C/5171–65

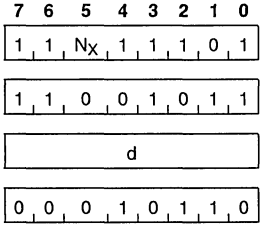
S: Set if result is negative
Z: Set if result is zero
H: Reset
P/V: Set if result parity is even
N: Reset
C: Set according to bit 7 of m_1



RL (HL)

Timing: M cycles — 4
T states — 15 (4, 4, 4, 3)

Addressing Mode: Register Indirect



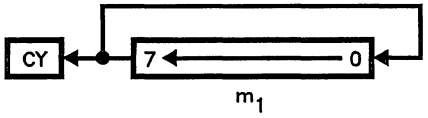
RL (IX+d) (for $N_X=0$)
RL (IY+d) (for NX=1)

Timing: M cycles — 6
T states — 23 (4, 4, 3, 5, 4, 3)

Addressing Mode: Indexed

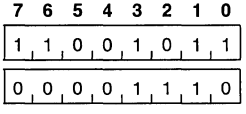
RRC m_1

Rotate the data in memory location m_1 right circular.



TL/C/5171–66

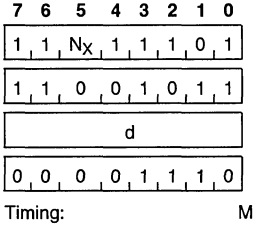
S: Set if result is negative
Z: Set if result is zero
H: Reset
P/V: Set if result parity is even
N: Reset
C: Set according to bit 0 of m_1



RRC (HL)

Timing: M cycles — 4
T states — 15 (4, 4, 4, 3)

Addressing Mode: Register Indirect



RRC (IX + d) (for $N_X = 0$)
RRC (IY + d) (for $N_X = 1$)

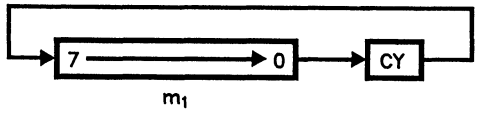
Timing: M cycles — 6
T states — 23 (4, 4, 3, 5, 4, 3)

Addressing Mode: Indexed

12.9 Rotate and Shift (Continued)

RR m_1

Rotate the data in memory location m_1 right through the carry.



TL/C/5171–67

S: Set if result is negative
Z: Set if result is zero
H: Reset
P/V: Set if result parity is even
N: Reset
C: Set according to bit 0 of m_1

7	6	5	4	3	2	1	0	
1	1	0	0	1	0	1	1	RR (HL)
0	0	0	1	1	1	1	0	

Timing: M cycles — 4
T states — 15 (4, 4, 4, 3)

Addressing Mode: Register Indirect

7	6	5	4	3	2	1	0	
1	1	N_X	1	1	1	0	1	RR (IX + d) (for $N_X = 0$)
1	1	0	0	1	0	1	1	RR (IY + d) (for $N_X = 1$)
d								
0	0	0	1	1	1	1	0	

Timing: M cycles — 6
T states — 23 (4, 4, 3, 5, 4, 3)

Addressing Mode: Indexed

SLA m_1

Shift the data in memory location m_1 left arithmetic.

TL/C/5171–68

S: Set if result is negative
Z: Set if result is zero
H: Reset
P/V: Set if result parity is even
N: Reset
C: Set according to bit 7 of m_1

7	6	5	4	3	2	1	0	
1	1	0	0	1	0	1	1	SLA (HL)
0	0	1	0	0	1	1	0	

Timing: M cycles — 4
T states — 15 (4, 4, 4, 3)

Addressing Mode: Register Indirect

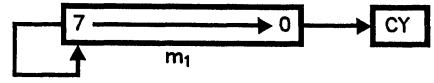
7	6	5	4	3	2	1	0	
1	1	N_X	1	1	1	0	1	SLA (IX + d) (for $N_X = 0$)
1	1	0	0	1	0	1	1	SLA (IY + d) (for $N_X = 1$)
d								
0	0	1	0	0	1	1	0	

Timing: M cycles — 6
T states — 23 (4, 4, 3, 5, 4, 3)

Addressing Mode: Indexed

SRA m_1

Shift the data in memory location m_1 right arithmetic.



TL/C/5171–69

S: Set if result is negative
Z: Set if result is zero
H: Reset
P/V: Set if result parity is even
N: Reset
C: Set according to bit 0 of m_1

7	6	5	4	3	2	1	0	
1	1	0	0	1	0	1	1	SRA (HL)
0	0	1	0	1	1	1	0	

Timing: M cycles — 4
T states — 15 (4, 4, 4, 3)

Addressing Mode: Register Indirect

7	6	5	4	3	2	1	0	
1	1	N_X	1	1	1	0	1	SRA (IX + d) (for $N_X = 0$)
1	1	0	0	1	0	1	1	SRA (IY + d) (for $N_X = 1$)
d								
0	0	1	0	1	1	1	0	

Timing: M cycles — 6
T states — 23 (4, 4, 3, 5, 4, 3)

Addressing Mode: Indexed

SRL m_1

Shift right logical the data in memory location m_1.

TL/C/5171–70

S: Reset
Z: Set if result is zero
H: Reset
P/V: Set if result parity is even
N: Reset
C: Set according to bit 0 of m_1

12.9 Rotate and Shift (Continued)

7	6	5	4	3	2	1	0	
1	1	0	0	1	0	1	1	SRL (HL)
0	0	1	1	1	1	1	0	

Timing: M cycles — 4
T states — 15 (4, 4, 4, 3)
Addressing Mode: Register Indirect

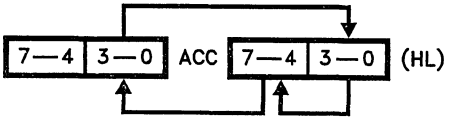
7	6	5	4	3	2	1	0	
1	1	N_X	1	1	1	0	1	SRL (IX + d) (for N_X = 0) / SRL (IY + d) (for N_X = 1)
1	1	0	0	1	0	1	1	
d								
0	0	1	1	1	1	1	0	

Timing: M cycles — 6
T states — 23 (4, 4, 3, 5, 4, 3)
Addressing Mode: Indexed

REGISTER/MEMORY

RLD

Rotate digit left and right between the Accumulator and memory (HL).



TL/C/5171-71

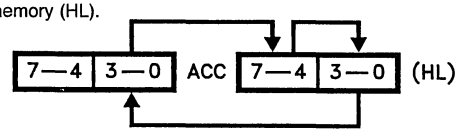
S: Set if result is negative
Z: Set if result is zero
H: Reset
P/V: Set if result parity is even
N: Reset
C: N/A

7	6	5	4	3	2	1	0
1	1	1	0	1	1	0	1
0	1	1	0	1	1	1	1

Timing: M cycles — 5
T states — 18 (4, 4, 3, 4, 3)
Addressing Mode: Implied/Register Indirect

RRD

Rotate digit right and left between the Accumulator and memory (HL).



TL/C/5171-72

S: Set if result is negative
Z: Set if result is zero
H: Reset
P/V: Set if result parity is even
N: Reset
C: N/A

7	6	5	4	3	2	1	0
1	1	1	0	1	1	0	1
0	1	1	0	0	1	1	1

Timing: M cycles — 5
T states — 18 (4, 4, 3, 4, 3)
Addressing Mode: Implied/Register Indirect

12.10 Exchanges

REGISTER/REGISTER

EX DE, HL

Exchange the contents of the 16-bit register pairs DE and HL.

DE ⟷ HL — No flags affected

7	6	5	4	3	2	1	0
1	1	1	0	1	0	1	1

Timing: M cycles — 1
T states — 4
Addressing Mode: Register

EX AF, A'F'

The contents of the Accumulator and flag register are exchanged with their corresponding alternate registers, that is A and F are exchanged with A' and F'.

A ⟷ A' — No flags affected
F ⟷ F'

7	6	5	4	3	2	1	0
0	0	0	0	1	0	0	0

Timing: M cycles — 1
T states — 4
Addressing Mode: Register

12.10 Exchanges (Continued)

EXX

Exchange the contents of the BC, DE, and HL registers with their corresponding alternate register.

BC ⟷ B'C'
DE ⟷ D'E'
HL ⟷ H'L'

No flags affected

7	6	5	4	3	2	1	0
1	1	0	1	1	0	0	1

Timing: M cycles — 1
T states — 4

Addressing Mode: Implied

REGISTER/MEMORY

EX (SP), ss

Exchange the two bytes at the top of the external memory stack with the 16-bit register ss.

(SP) ⟷ SS_L
(SP + 1) ⟷ SS_H

No flags affected

7	6	5	4	3	2	1	0	
1	1	1	0	0	0	1	1	EX (SP), HL

Timing: M cycles — 5
T states — 19 (4, 3, 4, 3, 5)

Addressing Mode: Register/Register Indirect

7	6	5	4	3	2	1	0	
1	1	N_X	1	1	1	0	1	EX (SP), IX (for N_X = 0)
1	1	1	0	0	0	1	1	EX (SP),IY (for N_X = 1)

Timing: M cycles — 6
T states — 23 (4, 4, 3, 4, 3, 5)

Addressing Mode: Register/Register Indirect

12.11 Memory Block Moves and Searches

SINGLE OPERATIONS

LDI

Move data from memory location (HL) to memory location (DE), increment memory pointers, and decrement byte counter BC.

(DE) ← (HL)
DE ← DE + 1
HL ← HL + 1
BC ← BC − 1

S: N/A
Z: N/A
H: Reset
P/V: Set if BC −1 ≠0, otherwise reset
N: Reset
C: N/A

7	6	5	4	3	2	1	0
1	1	1	0	1	1	0	1
1	0	1	0	0	0	0	0

Timing: M cycles — 4
T states — 16 (4, 4, 3, 5)

Addressing Mode: Register Indirect

LDD

Move data from memory location (HL) to memory location (DE), and decrement memory pointer and byte counter BC.

(DE) ← (HL)
DE ← DE − 1
HL ← HL − 1
BC ← BC − 1

S: N/A
Z: N/A
H: Reset
P/V: Set if BC −1 ≠0, otherwise reset
N: Reset
C: N/A

7	6	5	4	3	2	1	0
1	1	1	0	1	1	0	1
1	0	1	0	1	0	0	0

Timing: M cycles — 4
T states — 16 (4, 4, 3, 5)

Addressing Mode: Register Indirect

CPI

Compare data in memory location (HL) to the Accumulator, increment the memory pointer, and decrement the byte counter. The Z flag is set if the comparison is equal.

A − (HL)
HL ← HL + 1
BC ← BC − 1
Z ← 1
if A = (HL)

S: Set if result of comparison subtract is negative
Z: Set if result of comparison is zero
H: Set according to borrow from bit 4
P/V: Set if BC − 1≠ 0, otherwise reset
N: Set
C: N/A

7	6	5	4	3	2	1	0
1	1	1	0	1	1	0	1
1	0	1	0	0	0	0	1

Timing: M cycles — 4
T states — 16 (4, 4, 3, 5)

Addressing Mode: Register Indirect

CPD

Compare data in memory location (HL) to the Accumulator, and decrement the memory pointer and byte counter. The Z flag is set if the comparison is equal.

A − (HL)
HL ← HL − 1
BC ← BC − 1
Z ← 1
if A = (HL)

S: Set if result is negative
Z: Set if result of comparison is zero
H: Set according to borrow from bit 4
P/V: Set if BC − 1≠ 0, otherwise reset
N: Set
C: N/A

12.11 Memory Block Moves and Searches (Continued)

7	6	5	4	3	2	1	0
1	1	1	0	1	1	0	1
1	0	1	0	1	0	0	1

Timing: M cycles — 4
T states — 16 (4, 4, 3, 5)

Addressing Mode: Register Indirect

REPEAT OPERATIONS

LDIR

Move data from memory location (HL) to memory location (DE), increment memory pointers, decrement byte counter BC, and repeat until BC = 0.

(DE) ← (HL)
DE ← DE + 1
HL ← HL + 1
BC ← BC − 1
Repeat until
BC = 0

S: N/A
Z: N/A
H: Reset
P/V: Reset
N: Reset
C: N/A

7	6	5	4	3	2	1	0
1	1	1	0	1	1	0	1
1	0	1	1	0	0	0	0

Timing: For BC≠0 M cycles — 5
T states — 21 (4, 4, 3, 5, 5)
For BC=0 M cycles — 4
T states — 16 (4, 4, 3, 5)

Addressing Mode: Register Indirect

(Note that each repeat is accomplished by a decrement of the BC, so that refresh, etc. continues for each cycle.)

LDDR

Move data from memory location (HL) to memory location (DE), decrement memory pointers and byte counter BC, and repeat until BC = 0.

(DE) ← (HL)
DE ← DE − 1
HL ← HL − 1
BC ← BC − 1
Repeat until
BC = 0

S: N/A
Z: N/A
H: Reset
P/V: Reset
N: Reset
C: N/A

7	6	5	4	3	2	1	0
1	1	1	0	1	1	0	1
1	0	1	1	1	0	0	0

Timing: For BC≠0 M cycles — 5
T states — 21 (4, 4, 3, 5, 5)
For BC=0 M cycles — 4
T states — 16 (4, 4, 3, 5)

Addressing Mode: Register Indirect

(Note that each repeat is accomplished by a decrement of the BC, so that refresh, etc. continues for each cycle.)

CPIR

Compare data in memory location (HL) to the Accumulator, increment the memory, decrement the byte counter BC, and repeat until BC = 0 or (HL) equals A.

A − (HL)
HL ← HL + 1
BC ← BC + 1
Repeat until BC = 0
or A = (HL)

S: Set if sign of subtraction performed for comparison is negative
Z: Set if A = (HL), otherwise reset
H: Set according to borrow from bit 4
P/V: Set if BC − 1 ≠ 0, otherwise reset
N: Set
C: N/A

7	6	5	4	3	2	1	0
1	1	1	0	1	1	0	1
1	0	1	1	0	0	0	1

Timing: For BC ≠ 0 M cycles — 5
T states — 21 (4, 4, 3, 5, 5)
For BC = 0 M cycles — 4
T states — 16 (4, 4, 3, 5)

Addressing Mode: Register Indirect

(Note that each repeat is accomplished by a decrement of the PC, so that refresh, etc. continues for each cycle.)

CPDR

Compare data in memory location (HL) to the contents of the Accumulator, decrement the memory pointer and byte counter BC, and repeat until BC = 0, or until (HL) equals the Accumulator.

A − (HL)
HL ← HL − 1
BC ← BC − 1
Repeat until BC = 0
or A = (HL)

S: Set if sign of subtraction performed for comparison is negative
Z: Set according to equality of A and (HL), set if true
H: Set according to borrow from bit 4
P/V: Set if BC − 1 ≠ 0, otherwise reset
N: Set
C: N/A

7	6	5	4	3	2	1	0
1	1	1	0	1	1	0	1
1	0	1	1	1	0	0	1

Timing: For BC ≠ 0 M cycles — 5
T states — 21 (4, 4, 3, 5, 5)
For BC = 0 M cycles — 4
T states — 16 (4, 4, 3, 5)

Addressing Mode: Register Indirect

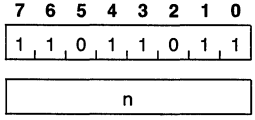
(Note that each repeat is accomplished by a decrement of the BC, so that refresh, etc. continues for each cycle.)

12.12 Input/Output

IN A, (n)

Input data to the Accumulator from the I/O device at address N.

A ← (n) — No flags affected



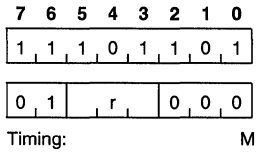
Timing: M cycles — 3
T states — 11 (4, 3, 4)

Addressing Mode: Source — Direct
Destination — Register

IN r, (C)

Input data to register r from the I/O device addressed by the contents of register C. If r = 110 only flags are affected.

r ← (C)
S: Set if result is negative
Z: Set if result is zero
H: Reset
P/V: Set if result parity is even
N: Reset
C: N/A



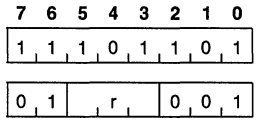
Timing: M cycles — 3
T states — 12 (4, 4, 4)

Addressing Mode: Source — Register Indirect
Destination — Register

OUT (C), r

Output register r to the I/O device addressed by the contents of register C.

(C) ← r — No flags affected



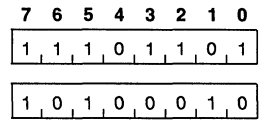
Timing: M cycles — 3
T states — 12 (4, 4, 4)

Addressing Mode: Source — Register
Destination — Register Indirect

INI

Input data from the I/O device addressed by the contents of register C to the memory location pointed to by the contents of the HL register. The HL pointer is incremented and the byte counter B is decremented.

(HL) ← (C)
B ← B − 1
HL ← HL + 1
S: Undefined
Z: Set if B − 1 = 0, otherwise reset
H: Undefined
P/V: Undefined
N: Set
C: N/A



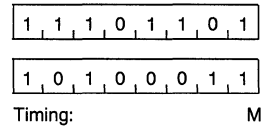
Timing: M cycles — 4
T states — 16 (4, 5, 3, 4)

Addressing Mode: Implied/Source — Register Indirect
Destination — Register Indirect

OUTI

Output data from memory location (HL) to the I/O device at port address (C), increment the memory pointer, and decrement the byte counter B.

(C) ← (HL)
B ← B − 1
HL ← HL + 1
S: Undefined
Z: Set if B − 1 = 0, otherwise reset
H: Undefined
P/V: Undefined
N: Set
C: N/A



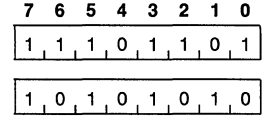
Timing: M cycles — 4
T states — 16 (4, 5, 3, 4)

Addressing Mode: Implied/Source — Register Indirect
Destination — Register Indirect

IND

Input data from I/O device at port address (C) to memory location (HL), and decrement HL memory pointer and byte counter B.

(HL) ← (C)
HL ← HL − 1
B ← B − 1
S: Undefined
Z: Set if B − 1 = 0, otherwise reset
H: Undefined
P/V: Undefined
N: Set
C: N/A



Timing: M cycles — 4
T states — 16 (4, 5, 3, 4)

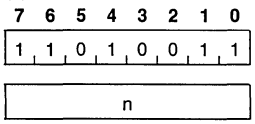
Addressing Mode: Implied/Source — Register Indirect
Destination — Register Indirect

12.12 Input/Output (Continued)

OUT (n), A

Output the Accumulator to the I/O device at address n.

(n) ← A — No flags affected



Timing: M cycles — 3
T states — 11 (4, 3, 4)

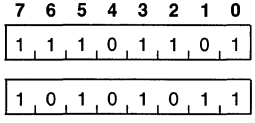
Addressing Mode: Source — Register
Destination — Direct

OUTD

Data is output from memory location (HL) to the I/O device at port address (C), and the HL memory pointer and byte counter B are decremented.

(C) ← (HL)
B ← B − 1
HL ← HL − 1

S: Undefined
Z: Set if B−1=0, otherwise reset
H: Undefined
P/V: Undefined
N: Set
C: N/A



Timing: M cycles — 4
T states — 16 (4, 5, 3, 4)

Addressing Mode: Implied/Source — Register Indirect
Destination — Register Indirect

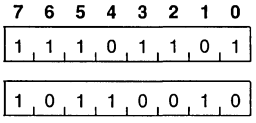
INIR

Data is input from the I/O device at port address (C) to memory location (HL), the HL memory pointer is incremented, and the byte counter B is decremented. The cycle is repeated until B = 0.

(Note that B is tested for zero after it is decremented. By loading B initially with zero, 256 data transfers will take place.)

(HL) ← (C)
HL ← HL + 1
B ← B − 1
Repeat until B = 0

S: Undefined
Z: Set
H: Undefined
P/V: Undefined
N: Set
C: N/A



Timing: For B ≠ 0 — M cycles — 5
T states — 21 (4, 5, 3, 4, 5)
For B = 0 — M cycles — 4
T states — 16 (4, 5, 3, 4)

Addressing Mode: Implied/Source — Register Indirect
Destination — Register Indirect

(Note that at the end of each data transfer cycle, interrupts may be recognized and two refresh cycles will be performed.)

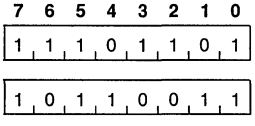
OTIR

Data is output to the I/O device at port address (C) from memory location (HL), the HL memory pointer is incremented, and the byte counter B is decremented. The cycles are repeated until B = 0.

(Note that B is tested for zero after it is decremented. By loading B initially with zero, 256 data transfers will take place.)

(C) ← (HL)
HL ← HL + 1
B ← B − 1
Repeat until B = 0

S: Undefined
H: Undefined
Z: Set
P/V: Undefined
N: Set
C: N/A



Timing: For B ≠ 0 — M cycles — 5
T states — 21 (4, 5, 3, 4, 5)
For B = 0 — M cycles — 4
T states — 16 (4, 5, 3, 4)

Addressing Mode: Implied/Source — Register Indirect
Destination — Register Indirect

(Note that at the end of each data transfer cycle, interrupts may be recognized and two refresh cycles will be performed.)

12.12 Input/Output (Continued)

INDR

Data is input from the I/O device at address (C) to memory location (HL), then the HL memory pointer is byte counter B are decremented. The cycle is repeated until B = 0.

(Note that B is tested for zero after it is decremented. By loading B initially with zero, 256 data transfers will take place.)

(HL) ← (C)
HL ← HL − 1
B ← B − 1
Repeat until B = 0

S: Undefined
Z: Set
H: Undefined
P/V: Undefined
N: Set
C: N/A

7	6	5	4	3	2	1	0
1	1	1	0	1	1	0	1

1	0	1	1	0	0	1	0

Timing: For B ≠ 0 — M cycles — 5; T states — 21 (4, 5, 3, 4, 5)
For B = 0 — M cycles — 4; T states — 16 (4, 5, 3, 4)

Addressing Mode: Implied/Source — Register Indirect; Destination — Register Indirect

(Note that after each data transfer cycle, interrupts may be recognized and two refresh cycles are performed.)

OTDR

Data is output from memory location (HL) to the I/O device at port address (C), then the HL memory pointer and byte counter B are decremented. The cycle is repeated until B = 0.

(Note that B is tested for zero after it is decremented. By loading B initially with zero, 256 data transfers will take place.)

(C) ← (HL)
HL ← HL − 1
B ← B − 1
Repeat until B = 0

S: Undefined
Z: Set
H: Undefined
P/V: Undefined
N: Set
C: N/A

7	6	5	4	3	2	1	0
1	1	1	0	1	1	0	1

1	0	1	1	1	0	1	1

Timing: For B ≠ 0 — M cycles — 5; T states — 21 (4, 5, 3, 4, 5)
For B = 0 — M cycles — 4; T states — 16 (4, 5, 3, 4)

Addressing Mode: Implied/Source — Register Indirect; Destination — Register Indirect

(Note that after each data transfer cycle the NSC800 will accept interrupts and perform two refresh cycles.)

12.13 CPU Control

NOP

The CPU performs no operation.

— — — No flags affected

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0

Timing: M cycles — 1; T states — 4

Addressing Mode: N/A

HALT

The CPU halts execution of the program. Dummy op-code fetches are performed from the next memory location to keep the refresh circuits active until the CPU is interrupted or reset from the halted state.

— — — No flags affected

7	6	5	4	3	2	1	0
0	1	1	1	0	1	1	0

Timing: M cycles — 1; T states — 4

Addressing Mode: N/A

DI

Disable system level interrupts.

IFF_1 ← 0
IFF_2 ← 0

No flags affected

7	6	5	4	3	2	1	0
1	1	1	1	0	0	1	1

Timing: M cycles — 1; T states — 4

Addressing Mode: N/A

EI

The system level interrupts are enabled. During execution of this instruction, and the next one, the maskable interrupts will be disabled.

IFF_1 ← 1
IFF_2 ← 1

No flags affected

7	6	5	4	3	2	1	0
1	1	1	1	1	0	1	1

Timing: M cycles — 1; T states — 4

Addressing Mode: N/A

IM 0

The CPU is placed in interrupt mode 0.

— — — No flags affected

7	6	5	4	3	2	1	0
1	1	1	0	1	1	0	1

0	1	0	0	0	1	1	0

Timing: M cycles — 2; T states — 8 (4, 4)

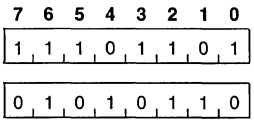
Addressing Mode: N/A

12.13 CPU Control (Continued)

IM 1

The CPU is placed in interrupt mode 1.

— — — No flags affected



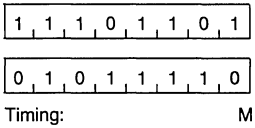
Timing: M cycles — 2
T states — 8 (4, 4)

Addressing Mode: N/A

IM 2

The CPU is placed in interrupt mode 2.

— — — No flags affected



Timing: M cycles — 2
T states — 8 (4, 4)

Addressing Mode: N/A

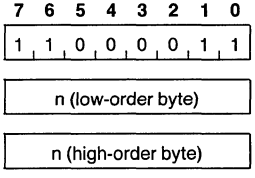
12.14 Program Control

JUMPS

JP nn

Unconditional jump to program location nn.

PC ← nn No flags affected



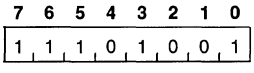
Timing: M cycles — 3
T states — 10 (4, 3, 3)

Addressing Mode: Direct

JP (ss)

Unconditional jump to program location pointed to by register ss.

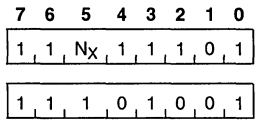
PC ← ss No flags affected



JP (HL)

Timing: M cycles — 1
T states — 4

Addressing Mode: Register Indirect



JP (IX) (for $N_X = 0$)
JP (IY) (for $N_X = 1$)

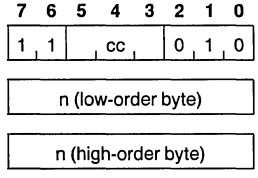
Timing: M cycles — 2
T states — 8 (4, 4)

Addressing Mode: Register Indirect

JP cc, nn

Conditionally jump to program location nn based on testable flag states.

If cc true, No flags affected
PC ← nn,
otherwise continue



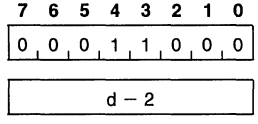
Timing: M cycles — 3
T states — 10 (4, 3, 3)

Addressing Mode: Direct

JR d

Unconditional jump to program location calculated with respect to the program counter and the displacement d.

PC ← PC + d No flags affected



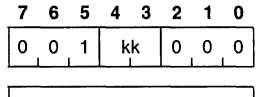
Timing: M cycles — 3
T states — 12 (4, 3, 5)

Addressing Mode: PC Relative

JR kk, d

Conditionally jump to program location calculated with respect to the program counter and the displacement d, based on limited testable flag states.

If kk true, No flags affected
PC ← PC + d,
otherwise continue



Timing: if kk met (true) M cycles — 3
T states — 12 (4, 3, 5)
if kk not met (not true) M cycles — 2
T states — 7 (4, 3)

Addressing Mode: PC Relative

12.14 Program Control (Continued)

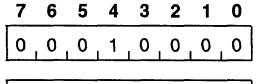
DJNZ d

Decrement the B register and conditionally jump to program location calculated with respect to the program counter and the displacement d, based on the contents of the B register.

B ← B − 1 — No flags affected

If B = 0 continue,

else PC ← PC + d



Timing: If B ≠ 0 — M cycles — 3; T states — 13 (5, 3, 5)

If B = 0 — M cycles — 2; T states — 8 (5, 3)

Addressing Mode: PC Relative

CALLS

CALL nn

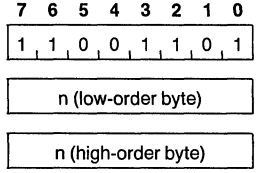
Unconditional call to subroutine at location nn.

(SP − 1) ← PC_H — No flags affected

(SP − 2) ← PC_L

SP ← SP − 2

PC ← nn



Timing: M Cycles — 5; T states — 17 (4, 3, 4, 3, 3)

Addressing Mode: Direct

CALL cc, nn

Conditional call to subroutine at location nn based on testable flag stages.

If cc true, — No flags affected

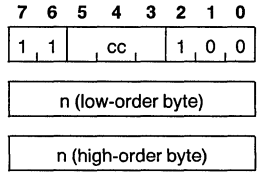
(SP − 1) ← PC_H

(SP − 2) ← PC_L

SP ← SP − 2

PC ← nn,

else continue



Timing: If cc true — M cycles — 5; T states 17 (4, 3, 4, 3, 3)

If cc not true — M cycles — 3; T states — 10 (4, 3, 3)

Addressing Mode: Direct

RETURNS

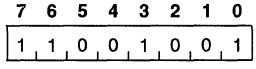
RET

Unconditional return from subroutine or other return to program location pointed to by the top of the stack.

PC_L ← (SP) — No flags affected

PC_H ← (SP + 1)

SP ← SP + 2



Timing: M cycles — 3; T states — 10 (4, 3, 3)

Addressing Mode: Register Indirect

RET cc

Conditional return from subroutine or other return to program location pointed to by the top of the stack.

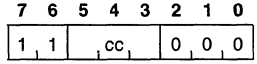
If cc true, — No flags affected

PC_L ← (SP)

PC_H ← (SP + 1)

SP ← SP + 2,

else continue



Timing: If cc true — M cycles — 3; T states — 11 (5, 3, 3)

If cc not true — M cycles — 1; T states — 5

Addressing Mode: Register Indirect

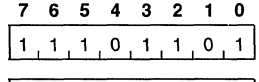
RETI

Unconditional return from interrupt handling subroutine. Functionally identical to RET instruction. Unique opcode allows monitoring by external hardware.

PC_L ← (SP) — No flags affected

PC_H ← (SP + 1)

SP ← SP + 2



Timing: M cycles — 4; T states — 14 (4, 4, 3, 3)

Addressing Mode: Register Indirect

12.14 Program Control (Continued)

RETN

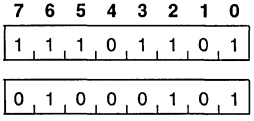
Unconditional return from non-maskable interrupt handling subroutine. Functionally similar to RET instruction, except interrupt enable state is restored to that prior to non-maskable interrupt.

$PC_L \leftarrow (SP)$ No flags affected

$PC_H \leftarrow (SP + 1)$

$SP \leftarrow SP + 2$

$IFF_1 \leftarrow IFF_2$



Timing: M cycles — 4

T states — 14 (4, 4, 3, 3)

Addressing Mode: Register Indirect

RESTARTS

RST P

The present contents of the PC are pushed onto the memory stack and the PC is loaded with dedicated program locations as determined by the specific restart executed.

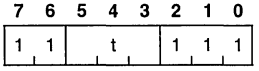
$(SP - 1) \leftarrow PC_H$ No flags affected

$(SP - 2) \leftarrow PC_L$

$SP \leftarrow SP - 2$

$PC_H \leftarrow 0$

$PC_L \leftarrow P$



Timing: M cycles — 3

T states — 11 (5, 3, 3)

Addressing Mode: Modified Page Zero

p	00H	08H	10H	18H	20H	28H	30H	38H
t	000	001	010	011	100	101	110	111

12.15 Instruction Set: Alphabetical Order

ADC	A, (HL)	8E
ADC	A, (IX+d)	DD 8Ed
ADC	A, (IY+d)	FD 8Ed
ADC	A, A	8F
ADC	A, B	88
ADC	A, C	89
ADC	A, D	8A
ADC	A, E	8B
ADC	A, H	8C
ADC	A, L	8D
ADC	A, n	CE n
ADC	HL, BC	ED 4A
ADC	HL, DE	ED 5A
ADC	HL, HL	ED 6A
ADC	HL, SP	ED 7A
ADD	A, (HL)	86
ADD	A, (IX+d)	DD 86d
ADD	A, (IY+d)	FD 86d
ADD	A, A	87
ADD	A, B	80
ADD	A, C	81
ADD	A, D	82
ADD	A, E	83
ADD	A, H	84
ADD	A, L	85
ADD	A, n	C6 n
ADD	HL, BC	09
ADD	HL, DE	19
ADD	HL, HL	29
ADD	HL, SP	39
ADD	IX, BC	DD 09
ADD	IX, DE	DD 19
ADD	IX, IX	DD 29
ADD	IX, SP	DD 39
ADD	IY, BC	FD 09
ADD	IY, DE	FD 19
ADD	IY, IY	FD 29
ADD	IY, SP	FD 39
AND	(HL)	A6
AND	(IX+d)	DD A6d
AND	(IY+d)	FD A6d
AND	A	A7
AND	B	A0
AND	C	A1
AND	D	A2
AND	E	A3
AND	H	A4
AND	L	A5
AND	n	E6 n
BIT	0, (HL)	CB 46
BIT	0, (IX+d)	DD CBd46
BIT	0, (IY+d)	FD CBd46
BIT	0, A	CB 47
BIT	0, B	CB 40
BIT	0, C	CB 41
BIT	0, D	CB 42
BIT	0, E	CB 43
BIT	0, H	CB 44
BIT	0, L	CB 45
BIT	1, (HL)	CB 4E
BIT	1, (IX+d)	DD CBd4E
BIT	1, (IY+d)	FD CBd4E
BIT	1, A	CB 4F
BIT	1, B	CB 48
BIT	1, C	CB 49
BIT	1, D	CB 4A
BIT	1, E	CB 4B
BIT	1, H	CB 4C
BIT	1, L	CB 4D
BIT	2, (HL)	CB 56
BIT	2, (IX+d)	DD CBd56
BIT	2, (IY+d)	FD CBd56
BIT	2, A	CB 57
BIT	2, B	CB 50
BIT	2, C	CB 51
BIT	2, D	CB 52
BIT	2, E	CB 53
BIT	2, H	CB 54
BIT	2, L	CB 55
BIT	3, (HL)	CB 5E
BIT	3, (IX+d)	DD CBd5E
BIT	3, (IY+d)	FD CBd5E
BIT	3, A	CB 5F
BIT	3, B	CB 58
BIT	3, C	CB 59
BIT	3, D	CB 5A
BIT	3, E	CB 5B
BIT	3, H	CB 5C
BIT	3, L	CB 5D
BIT	4, (HL)	CB 66
BIT	4, (IX+d)	DD CBd66
BIT	4, (IY+d)	FD CBd66
BIT	4, A	CB 67
BIT	4, B	CB 60
BIT	4, C	CB 61
BIT	4, D	CB 62
BIT	4, E	CB 63
BIT	4, H	CB 64
BIT	4, L	CB 65
BIT	5, (HL)	CB 6E
BIT	5, (IX+d)	DD CBd6E
BIT	5, (IY+d)	FD CBd6E
BIT	5, A	CB 6F
BIT	5, B	CB 68
BIT	5, C	CB 69
BIT	5, D	CB 6A

(nn) = address of memory location
d = signed displacement
nn = Data (16 bit)
d2 = d−2
n = Data (8 bit)

12.15 Instruction Set: Alphabetical Order (Continued)

BIT	5, E	CB 6B
BIT	5, H	CB 6C
BIT	5, L	CB 6D
BIT	6, (HL)	CB 76
BIT	6, (IX+d)	DD CBd76
BIT	6, (IY+d)	FD CBd76
BIT	6, A	CB 77
BIT	6, B	CB 70
BIT	6, C	CB 71
BIT	6, D	CB 72
BIT	6, E	CB 73
BIT	6, H	CB 74
BIT	6, L	CB 75
BIT	7, (HL)	CB 7E
BIT	7, (IX+d)	DD CBd7E
BIT	7, (IY+d)	FD CBd7E
BIT	7, A	CB 7F
BIT	7, B	CB 78
BIT	7, C	CB 79
BIT	7, D	CB 7A
BIT	7, E	CB 7B
BIT	7, H	CB 7C
BIT	7, L	CB 7D
CALL	C, nn	DCnn
CALL	M, nn	FCnn
CALL	NC, nn	D4nn
CALL	nn	CDnn
CALL	NZ, nn	C4nn
CALL	P, nn	F4nn
CALL	PE, nn	ECnn
CALL	PO, nn	E4nn
CALL	Z, nn	CCnn
CCF		3F
CP	(HL)	BE
CP	(IX+d)	DD BEd
CP	(IY+d)	FD BEd
CP	A	BF
CP	B	B8
CP	C	B9
CP	D	BA
CP	E	BB
CP	H	BC
CP	L	BD
CP	n	FE n
CPD		ED A9
CPDR		ED B9
CPI		ED A1
CPIR		ED B1
CPL		2F
DAA		27
DEC	(HL)	35
DEC	(IX+d)	DD 35d
DEC	(IY+d)	FD 35d
DEC	A	3D
DEC	B	05
DEC	BC	0B
DEC	C	0D
DEC	D	15
DEC	DE	1B
DEC	E	1D
DEC	H	25
DEC	HL	2B
DEC	IX	DD 2B
DEC	IY	FD 2B
DEC	L	2D
DEC	SP	3B
DI		F3
DJNZ	d2	10 d2
EI		FB
EX	(SP), HL	E3
EX	(SP), IX	DD E3
EX	(SP), IY	FD E3
EX	AF, A'F'	08
EX	DE, HL	EB
EXX		D9
HALT		76
IM	0	ED 46
IM	1	ED 56
IM	2	ED 5E
IN	A, (C)	ED78
IN	A, (n)	DB n
IN	B, (C)	ED 40
IN	C, (C)	ED 48
IN	D, (C)	ED 50
IN	E, (C)	ED 58
IN	H, (C)	ED 60
IN	L, (C)	ED 68
INC	(HL)	34
INC	(IX+d)	DD 34d
INC	(IY+d)	FD 34d
INC	A	3C
INC	B	04
INC	BC	03
INC	C	0C
INC	D	14
INC	DE	13
INC	E	1C
INC	H	24
INC	HL	23
INC	IX	DD 23
INC	IY	FD 23
INC	L	2C
INC	SP	33
IND		ED AA
INDR		ED BA
INI		ED A2

(nn) = Address of memory location
nn = Data (16 bit)
n = Data (8 bit)
d = signed displacement
d2 = d − 2

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12.15 Instruction Set: Alphabetical Order (Continued)

INIR		ED B2
JP	(HL)	E9
JP	(IX)	DD E9
JP	(IY)	FD E9
JP	C, nn	DAnn
JP	M, nn	FAnn
JP	NC, nn	D2nn
JP	nn	C3nn
JP	NZ, nn	C2nn
JP	P, nn	F2nn
JP	PE, nn	EAnn
JP	PO, nn	E2nn
JP	Z, nn	CAnn
JR	C, d2	38 d2
JR	d2	18 d2
JR	NC, d2	30 d2
JR	NZ, d2	20 d2
JR	Z, d2	28 d2
LD	(BC), A	02
LD	(DE), A	12
LD	(HL), A	77
LD	(HL), B	70
LD	(HL), C	71
LD	(HL), D	72
LD	(HL), E	73
LD	(HL), H	74
LD	(HL), L	75
LD	(HL), n	36 n
LD	(IX+d), A	DD 77d
LD	(IX+d), B	DD 70d
LD	(IX+d), C	DD 71d
LD	(IX+d), D	DD 72d
LD	(IX+d), E	DD 73d
LD	(IX+d), H	DD 74d
LD	(IX+d), L	DD 75d
LD	(IX+d), n	DD 36dn
LD	(IY+d), A	FD 77d
LD	(IY+d), B	FD 70d
LD	(IY+d), C	FD 71d
LD	(IY+d), D	FD 72d
LD	(IY+d), E	FD 73d
LD	(IY+d), H	FD 74d
LD	(IY+d), L	FD 75d
LD	(IY+d), n	FD 36dn
LD	(nn), A	32nn
LD	(nn), BC	ED 43nn
LD	(nn), DE	ED 53nn
LD	(nn), HL	22nn
LD	(nn), IX	DD 22nn
LD	(nn), IY	FD 22nn
LD	(nn), SP	ED 73nn
LD	A, (BC)	0A
LD	A, (DE)	1A
LD	A, (HL)	7E
LD	A, (IX+d)	DD 7Ed
LD	A, (IY+d)	FD 7Ed
LD	A, (nn)	3Ann
LD	A, A	7F
LD	A, B	78
LD	A, C	79
LD	A, D	7A
LD	A, E	7B
LD	A, H	7C
LD	A, I	ED 57
LD	A, L	7D
LD	A, n	3E n
LD	B, (HL)	46
LD	B, (IX+d)	DD 46d
LD	B, (IY+d)	FD 46d
LD	B, A	47
LD	B, B	40
LD	B, C	41
LD	B, D	42
LD	B, E	43
LD	B, H	44
LD	B, L	45
LD	B, n	06 n
LD	BC, (nn)	ED 4B
LD	BC, nn	01nn
LD	C, (HL)	4E
LD	C, (IX+d)	DD 4Ed
LD	C, (IY+d)	FD 4Ed
LD	C, A	4F
LD	C, B	48
LD	C, C	49
LD	C, D	4A
LD	C, E	4B
LD	C, H	4C
LD	C, L	4D
LD	C, n	0E n
LD	D, (HL)	56
LD	D, (IX+d)	DD 56d
LD	D, (IY+d)	FD 56d
LD	D, A	57
LD	D, B	50
LD	D, C	51
LD	D, D	52
LD	D, E	53
LD	D, H	54
LD	D, L	55
LD	D, n	16 n
LD	DE, (nn)	ED 5Bnn
LD	DE, nn	11nn
LD	E, (HL)	5E
LD	E, (IX+d)	DD 5Ed
LD	E, (IY+d)	FD 5Ed

(nn) = Address of memory location
nn = Data (16 bit)
n = Data (8 bit)
d = signed displacement
d2 = d−2

12.15 Instruction Set: Alphabetical Order (Continued)

LD	E, A	5F
LD	E, B	58
LD	E, C	59
LD	E, D	5A
LD	E, E	5B
LD	E, H	5C
LD	E, L	5D
LD	E, n	1E n
LD	H, (HL)	66
LD	H, (IX+d)	DD 66d
LD	H, (IY+d)	FD 66d
LD	H, A	67
LD	H, B	60
LD	H, C	61
LD	H, D	62
LD	H, E	63
LD	H, H	64
LD	H, L	65
LD	H, n	26 n
LD	HL, (nn)	2Ann
LD	HL, nn	21nn
LD	I, A	ED 47
LD	IX, (nn)	DD 2Ann
LD	IX, nn	DD 21nn
LD	IY, (nn)	FD 2Ann
LD	IY, nn	FD 21nn
LD	L, (HL)	6E
LD	L, (IX+d)	DD 6Ed
LD	L, (IY+d)	FD 6Ed
LD	L, A	6F
LD	L, B	68
LD	L, C	69
LD	L, D	6A
LD	L, E	6B
LD	L, H	6C
LD	L, L	6D
LD	L, n	2E n
LD	SP, (nn)	ED 7Bnn
LD	SP, HL	F9
LD	SP, IX	DD F9
LD	SP, IY	FD F9
LD	SP, nn	31nn
LDD		ED A8
LDDR		ED B8
LDI		ED A0
LDIR		ED B0
NEG		ED n
NOP		00
OR	(HL)	B6
OR	(IX+d)	DD B6d
OR	(IY+d)	FD B6d
OR	A	B7
OR	B	B0
OR	C	B1
OR	D	B2
OR	E	B3
OR	H	B4
OR	L	B5
OR	n	F6 n
OTDR		ED BB
OTIR		ED B3
OUT	(C), A	ED 79
OUT	(C), B	ED 41
OUT	(C), C	ED 49
OUT	(C), D	ED 51
OUT	(C), E	ED 59
OUT	(C), H	ED 61
OUT	(C), L	ED 69
OUT	n, A	D3 n
OUTD		ED AB
OUTI		ED A3
POP	AF	F1
POP	BC	C1
POP	DE	D1
POP	HL	E1
POP	IX	DD E1
POP	IY	FD E1
PUSH	AF	F5
PUSH	BC	C5
PUSH	DE	D5
PUSH	HL	E5
PUSH	IX	DD E5
PUSH	IY	FD E5
RES	0, (HL)	CB 86
RES	0, (IX+d)	DD CBd86
RES	0, (IY+d)	FD CBd86
RES	0, A	CB 87
RES	0, B	CB 80
RES	0, C	CB 81
RES	0, D	CB 82
RES	0, E	CB 83
RES	0, H	CB 84
RES	0, L	CB 85
RES	1, (HL)	CB 8E
RES	1, (IX+d)	DD CBd8E
RES	1, (IY+d)	FD CBd8E
RES	1, A	CB 8F
RES	1, B	CB 88
RES	1, C	CB 89
RES	1, D	CB 8A
RES	1, E	CB 8B
RES	1, H	CB 8C
RES	1, L	CB 8D
RES	2, (HL)	CB 96
RES	2, (IX+d)	DD CBd96
RES	2, (IY+d)	FD CBd96

(nn) = Address of memory location
nn = Data (16 bit)
n = Data (8 bit)
d = signed displacement
d2 = d − 2

12.15 Instruction Set: Alphabetical Order (Continued)

RES	2, A	CB 97
RES	2, B	CB 90
RES	2, C	CB 91
RES	2, D	CB 92
RES	2, E	CB 93
RES	2, H	CB 94
RES	2, L	CB 95
RES	3, (HL)	CB 9E
RES	3, (IX+d)	DD CBd9E
RES	3, (IY+d)	FD CBd9E
RES	3, A	CB 9F
RES	3, B	CB 98
RES	3, C	CB 99
RES	3, D	CB 9A
RES	3, E	CB 9B
RES	3, H	CB 9C
RES	3, L	CB 9D
RES	4, (HL)	CB A6
RES	4, (IX+d)	DD CBdA6
RES	4, (IY+d)	FD CBdA6
RES	4, A	CB A7
RES	4, B	CB A0
RES	4, C	CB A1
RES	4, D	CB A2
RES	4, E	CB A3
RES	4, H	CB A4
RES	4, L	CB A5
RES	5, (HL)	CB AE
RES	5, (IX+d)	DD CBdAE
RES	5, (IY+d)	FD CBdAE
RES	5, A	CB AF
RES	5, B	CB A8
RES	5, C	CB A9
RES	5, D	CB AA
RES	5, E	CB AB
RES	5, H	CB AC
RES	5, L	CB AD
RES	6, (HL)	CB B6
RES	6, (IX+d)	DD CBdB6
RES	6, (IY+d)	FD CBdB6
RES	6, A	CB B7
RES	6, B	CB B0
RES	6, C	CB B1
RES	6, D	CB B2
RES	6, E	CB B3
RES	6, H	CB B4
RES	6, L	CB B5
RES	7, (HL)	CB BE
RES	7, (IX+d)	DD CBdBE
RES	7, (IY+d)	FD CBdBE
RES	7, A	CB BF
RES	7, B	CB B8
RES	7, C	CB B9
RES	7, D	CB BA
RES	7, E	CB BB
RES	7, H	CB BC
RES	7, L	CB BD
RET		C9
RET	C	D8
RET	M	F8
RET	NC	D0
RET	NZ	C0
RET	P	F0
RET	PE	E8
RET	PO	E0
RET	Z	C8
RETI		ED 4D
RETN		ED 45
RL	(HL)	CB 16
RL	(IX+d)	DD CBd16
RL	(IY+d)	FD CBd16
RL	A	CB 17
RL	B	CB 10
RL	C	CB 11
RL	D	CB 12
RL	E	CB 13
RL	H	CB 14
RL	L	CB 15
RLA		17
RLC	(HL)	CB 06
RLC	(IX+d)	DD CBd06
RLC	(IY+d)	FD CBd06
RLC	A	CB 07
RLC	B	CB 00
RLC	C	CB 01
RLC	D	CB 02
RLC	E	CB 03
RLC	H	CB 04
RLC	L	CB 05
RLCA		07
RLD		ED 6F
RR	(HL)	CB 1E
RR	(IX+d)	DD CBd1E
RR	(IY+d)	FD CBd1E
RR	A	CB 1F
RR	B	CB 18
RR	C	CB 19
RR	D	CB 1A
RR	E	CB 1B
RR	H	CB 1C
RR	L	CB 1D
RRA		1F
RRC	(HL)	CB OE
RRC	(IX+d)	DD CBd0E
RRC	(IY+d)	FD CBd0E
RRC	A	CB 0F

(nn) = Address of memory location
nn = Data (16 bit)
n = Data (8 bit)
d = signed displacement
d2 = d−2

12.15 Instruction Set: Alphabetical Order (Continued)

RRC	B	CB 08
RRC	C	CB 09
RRC	D	CB 0A
RRC	E	CB 0B
RRC	H	CB 0C
RRC	L	CB 0D
RRCA		0F
RRD		ED 67
RST	0	C7
RST	08H	CF
RST	10H	D7
RST	18H	DF
RST	20H	E7
RST	28H	EF
RST	30H	F7
RST	38H	FF
SBC	A, (HL)	9E
SBC	A, (IX+d)	DD 9Ed
SBC	A, (IY+d)	FD 9Ed
SBC	A, A	9F
SBC	A, B	98
SBC	A, C	99
SBC	A, D	9A
SBC	A, E	9B
SBC	A, H	9C
SBC	A, L	9D
SBC	A, n	DE n
SBC	HL, BC	ED 42
SBC	HL, DE	ED 52
SBC	HL, HL	ED 62
SBC	HL, SP	ED 72
SCF		37
SET	0, (HL)	CB C6
SET	0, (IX+d)	DD CBdC6
SET	0, (IY+d)	FD CBdC6
SET	0, A	CB C7
SET	0, B	CB C0
SET	0, C	CB C1
SET	0, D	CB C2
SET	0, E	CB C3
SET	0, H	CB C4
SET	0, L	CB C5
SET	1, (HL)	CB CE
SET	1, (IX+d)	DD CBdCE
SET	1, (IY+d)	FD CBdCE
SET	1, A	CB CF
SET	1, B	CB C8
SET	1, C	CB C9
SET	1, D	CB CA
SET	1, E	CB CB
SET	1, H	CB CC
SET	1, L	CB CD
SET	2, (HL)	CB D6
SET	2, (IX+d)	DD CBdD6
SET	2, (IY+d)	FD CBdD6
SET	2, A	CB D7
SET	2, B	CB D0
SET	2, C	CB D1
SET	2, D	CB D2
SET	2, E	CB D3
SET	2, H	CB D4
SET	2, L	CB D5
SET	3, (HL)	CB DE
SET	3, (IX+d)	DD CBdDE
SET	3, (IY+d)	FD CBdDE
SET	3, A	CB DF
SET	3, B	CB D8
SET	3, C	CB D9
SET	3, D	CB DA
SET	3, E	CB DB
SET	3, H	CB DC
SET	3, L	CB DD
SET	4, (HL)	CB E6
SET	4, (IX+d)	DD CBdE6
SET	4, (IY+d)	FD CBdE6
SET	4, A	CB E7
SET	4, B	CB E0
SET	4, C	CB E1
SET	4, D	CB E2
SET	4, E	CB E3
SET	4, H	CB E4
SET	4, L	CB E5
SET	5, (HL)	CB EE
SET	5, (IX+d)	DD CBdEE
SET	5, (IY+d)	FD CBdEE
SET	5, A	CB EF
SET	5, B	CB E8
SET	5, C	CB E9
SET	5, D	CB EA
SET	5, E	CB EB
SET	5, H	CB EC
SET	5, L	CB ED
SET	6, (HL)	CB F6
SET	6, (IX+d)	DD CBdF6
SET	6, (IY+d)	FD CBdF6
SET	6, A	CB F7
SET	6, B	CB F0
SET	6, C	CB F1
SET	6, D	CB F2
SET	6, E	CB F3
SET	6, H	CB F4
SET	6, L	CB F5
SET	7, (HL)	CB FE
SET	7, (IX+d)	DD CBdFE
SET	7, (IY+d)	FD CBdFE
SET	7, A	CB FF

(nn) = Address of memory location
nn = Data (16 bit)
n = Data (8 bit)
d = displacement
d2 = d − 2

12.15 Instruction Set: Alphabetical Order (Continued)

SET	7, B	CB F8	SRL	A	CB 3F
SET	7, C	CB F9	SRL	B	CB 38
SET	7, D	CB FA	SRL	C	CB 39
SET	7, E	CB FB	SRL	D	CB 3A
SET	7, H	CB FC	SRL	E	CB 3B
SET	7, L	CB FD	SRL	H	CB 3C
SLA	(HL)	CB 26	SRL	L	CB 3D
SLA	(IX+d)	DD CBd26	SUB	(HL)	96
SLA	(IY+d)	FD CBd26	SUB	(IX+d)	DD 96d
SLA	A	CB 27	SUB	(IY+d)	FD 96d
SLA	B	CB 20	SUB	A	97
SLA	C	CB 21	SUB	B	90
SLA	D	CB 22	SUB	C	91
SLA	E	CB 23	SUB	D	92
SLA	H	CB 24	SUB	E	93
SLA	L	CB 25	SUB	H	94
SRA	(HL)	CB 2E	SUB	L	95
SRA	(IX+d)	DD CBd2E	SUB	n	D6 n
SRA	(IY+d)	FD CBd2E	XOR	(HL)	AE
SRA	A	CB 2F	XOR	(IX+d)	DD AEd
SRA	B	CB 28	XOR	(IY+d)	FD AEd
SRA	C	CB 29	XOR	A	AF
SRA	D	CB 2A	XOR	B	A8
SRA	E	CB 2B	XOR	C	A9
SRA	H	CB 2C	XOR	D	AA
SRA	L	CB 2D	XOR	E	AB
SRL	(HL)	CB 3E	XOR	H	AC
SRL	(IX+d)	DD CBd3E	XOR	L	AD
SRL	(IY+d)	FD CBd3E	XOR	n	EE n

12.16 Instruction Set: Numerical Order

Op Code	Mnemonic	Op Code	Mnemonic	Op Code	Mnemonic
00	NOP	15	DEC D	2Ann	LD HL,(nn)
01nn	LD BC,nn	16n	LD D,n	2B	DEC HL
02	LD (BC),A	17	RLA	2C	INC L
03	INC BC	18d2	JR d2	2D	DEC L
04	INC B	19	ADD HL,DE	2En	LD L,n
05	DEC B	1A	LD A,(DE)	2F	CPL
06n	LD B,n	1B	DEC DE	30d2	JR NC,d2
07	RLCA	1C	INC E	31nn	LD SP,nn
08	EX AF,A'F'	1D	DEC E	32nn	LD (nn),A
09	ADD HL,BC	1En	LD E,n	33	INC SP
0A	LD A,(BC)	1F	RRA	34	INC (HL)
0B	DEC BC	20d2	JR NZ,d2	35	DEC (HL)
0C	INC C	21nn	LD HL,nn	36n	LD (HL),n
0D	DEC C	22nn	LD (nn),HL	37	SCF
0En	LD C,n	23	INC HL	38	JR C,d2
0F	RRCA	24	INC H	39	ADD HL,SP
10d2	DJNZ d2	25	DEC H	3Ann	LD A,(nn)
11nn	LD DE,nn	26n	LD H, n	3B	DEC SP
12	LD (DE),A	27	DAA	3C	INC A
13	INC DE	28d2	JR Z,d2	3D	DEC A
14	INC D	29	ADD HL,HL	3En	LD A,n

(nn) = Address of memory location
nn = Data (16 bit)
n = Data (8 bit)
d = displacement
d2 = d − 2

12.16 Instruction Set: Numerical Order (Continued)

Op Code	Mnemonic	Op Code	Mnemonic	Op Code	Mnemonic
3F	CCF	74	LD (HL),H	A9	XOR C
40	LD B,B	75	LD (HL),L	AA	XOR D
41	LD B,C	76	HALT	AB	XOR E
42	LD B,D	77	LD (HL),A	AC	XOR H
43	LD B,E	78	LD A,B	AD	XOR L
44	LD B,H	79	LD A,C	AE	XOR (HL)
45	LD B,L	7A	LD A,D	AF	XOR A
46	LD B,(HL)	7B	LD A,E	B0	OR B
47	LD B,A	7C	LD A,H	B1	OR C
48	LD C,B	7D	LD A,L	B2	OR D
49	LD C,C	7E	LD A,(HL)	B3	OR E
4A	LD C,D	7F	LD A,A	B4	OR H
4B	LD C,E	80	ADD A,B	B5	OR L
4C	LD C,H	81	ADD A,C	B6	OR (HL)
4D	LD C,L	82	ADD A,D	B7	OR A
4E	LD C,(HL)	83	ADD A,E	B8	CP B
4F	LD C,A	84	ADD A,H	B9	CP C
50	LD D,B	85	ADD A,L	BA	CP D
51	LD D,C	86	ADD A,(HL)	BB	CP E
52	LD D,D	87	ADD A,A	BC	CP H
53	LD D,E	88	ADC A,B	BD	CP L
54	LD D,H	89	ADC A,C	BE	CP (HL)
55	LD D,L	8A	ADC A,D	BF	CP A
56	LD D,(HL)	8B	ADC A,E	C0	RET NZ
57	LD D,A	8C	ADC A,H	C1	POP BC
58	LD E,B	8D	ADC A,L	C2nn	JP NZ,nn
59	LD E,C	8E	ADC A,(HL)	C3nn	JP nn
5A	LD E,D	8F	ADC A,A	C4nn	CALL NZ,nn
5B	LD E,E	90	SUB B	C5	PUSH BC
5C	LD E,H	91	SUB C	C6n	ADD A,n
5D	LD E,L	92	SUB D	C7	RST 0
5E	LD E,(HL)	93	SUB E	C8	RET Z
5F	LD E,A	94	SUB H	C9	RET
60	LD H,B	95	SUB L	CAnn	JP Z,nn
61	LD H,C	96	SUB (HL)	CB00	RLC B
62	LD H,D	97	SUB A	CB01	RLC C
63	LD H,E	98	SBC A,B	CB02	RLC D
64	LD H,H	99	SBC A,C	CB03	RLC E
65	LD H,L	9A	SBC A,D	CB04	RLC H
66	LD H,(HL)	9B	SBC A,E	CB05	RLC L
67	LD H,A	9C	SBC A,H	CB06	RLC (HL)
68	LD L,B	9D	SBC A,L	CB07	RLC A
69	LD L,C	9E	SBC A,(HL)	CB08	RRC B
6A	LD L,D	9F	SBC A,A	CB09	RRC C
6B	LD L,E	A0	AND B	CB0A	RRC D
6C	LD L,H	A1	AND C	CB0B	RRC E
6D	LD L,L	A2	AND D	CB0C	RRC H
6E	LD L,(HL)	A3	AND E	CB0D	RRC L
6F	LD L,A	A4	AND H	CB0E	RRC (HL)
70	LD (HL),B	A5	AND L	CB0F	RRC A
71	LD (HL),C	A6	AND (HL)	CB10	RL B
72	LD (HL),D	A7	AND A	CB11	RL C
73	LD (HL),E	A8	XOR B	CB12	RL D

(nn) = Address of memory location d = displacement
nn = Data (16 bit) d2 = d − 2
n = Data (8-bit)

12.16 Instruction Set: Numerical Order (Continued)

Op Code	Mnemonic	Op Code	Mnemonic	Op Code	Mnemonic
CB13	RL E	CB4F	BIT 1,A	CB83	RES 0,E
CB14	RL H	CB50	BIT 2,B	CB84	RES 0,H
CB15	RL L	CB51	BIT 2,C	CB85	RES 0,L
CB16	RL (HL)	CB52	BIT 2,D	CB86	RES 0,(HL)
CB17	RL A	CB53	BIT 2,E	CB87	RES 0,A
CB18	RR B	CB54	BIT 2,H	CB88	RES 1,B
CB19	RR C	CB55	BIT 2,L	CB89	RES 1,C
CB1A	RR D	CB56	BIT 2,(HL)	CB8A	RES 1,D
CB1B	RR E	CB57	BIT 2,A	CB8B	RES 1,E
CB1C	RR H	CB58	BIT 3,B	CB8C	RES 1,H
CB1D	RR L	CB59	BIT 3,C	CB8D	RES 1,L
CB1E	RR (HL)	CB5A	BIT 3,D	CB8E	RES 1,(HL)
CB1F	RR A	CB5B	BIT 3,E	CB8F	RES 1,A
CB20	SLA B	CB5C	BIT 3,H	CB90	RES 2,B
CB21	SLA C	CB5D	BIT 3,L	CB91	RES 2,C
CB22	SLA D	CB5E	BIT 3,(HL)	CB92	RES 2,D
CB23	SLA E	CB5F	BIT 3,A	CB93	RES 2,E
CB24	SLA H	CB60	BIT 4,B	CB94	RES 2,H
CB25	SLA L	CB61	BIT 4,C	CB95	RES 2,L
CB26	SLA (HL)	CB62	BIT 4,D	CB96	RES 2,(HL)
CB27	SLA A	CB63	BIT 4,E	CB97	RES 2,A
CB28	SRA B	CB64	BIT 4,H	CB98	RES 3,B
CB29	SRA C	CB65	BIT 4,L	CB99	RES 3,C
CB2A	SRA D	CB66	BIT 4,(HL)	CB9A	RES 3,D
CB2B	SRA E	CB67	BIT 4,A	CB9B	RES 3,E
CB2C	SRA H	CB68	BIT 5,B	CB9C	RES 3,H
CB2D	SRA L	CB69	BIT 5,C	CB9D	RES 3,L
CB2E	SRA (HL)	CB6A	BIT 5,D	CB9E	RES 3,(HL)
CB2F	SRA A	CB6B	BIT 5,E	CB9F	RES 3,A
CB38	SRL B	CB6C	BIT 5,H	CBA0	RES 4,B
CB39	SRL C	CB6D	BIT 5,L	CBA1	RES 4,C
CB3A	SRL D	CB6E	BIT 5,(HL)	CBA2	RES 4,D
CB3B	SRL E	CB6F	BIT 5,A	CBA3	RES 4,E
CB3C	SRL H	CB70	BIT 6,B	CBA4	RES 4,H
CB3D	SRL L	CB71	BIT 6,C	CBA5	RES 4,L
CB3E	SRL (HL)	CB72	BIT 6,D	CBA6	RES 4,(HL)
CB3F	SRL A	CB73	BIT 6,E	CBA7	RES 4,A
CB40	BIT 0,B	CB74	BIT 6,H	CBA8	RES 5,B
CB41	BIT 0,C	CB75	BIT 6,L	CBA9	RES 5,C
CB42	BIT 0,D	CB76	BIT 6,(HL)	CBAA	RES 5,D
CB43	BIT 0,E	CB77	BIT 6,A	CBAB	RES 5,E
CB44	BIT 0,H	CB78	BIT 7,B	CBAC	RES 5,H
CB45	BIT 0,L	CB79	BIT 7,C	CBAD	RES 5,L
CB46	BIT 0,(HL)	CB7A	BIT 7,D	CBAE	RES 5,(HL)
CB47	BIT 0,A	CB7B	BIT 7,E	CBAF	RES 5,A
CB48	BIT 1,B	CB7C	BIT 7,H	CBB0	RES 6,B
CB49	BIT 1,C	CB7D	BIT 7,L	CBB1	RES 6,C
CB4A	BIT 1,D	CB7E	BIT 7,(HL)	CBB2	RES 6,D
CB4B	BIT 1,E	CB7F	BIT 7,A	CBB3	RES 6,E
CB4C	BIT 1,H	CB80	RES 0,B	CBB4	RES 6,H
CB4D	BIT 1,L	CB81	RES 0,C	CBB5	RES 6,L
CB4E	BIT 1,(HL)	CB82	RES 0,D	CBB6	RES 6,(HL)

(nn) = Address of memory location d = displacement
nn = Data (16 bit) d2 = d − 2
n = Data (8-bit)

12.16 Instruction Set: Numerical Order (Continued)

Op Code	Mnemonic	Op Code	Mnemonic	Op Code	Mnemonic
CBB7	RES 6,A	CBEC	SET 5,H	DD66d	LD H,(IX+d)
CBB8	RES 7,B	CBED	SET 5,L	DD6Ed	LD L,(IX+d)
CBB9	RES 7,C	CBEE	SET 5,(HL)	DD70d	LD (IX+d),B
CBBA	RES 7,D	CBEF	SET 5,A	DD71d	LD (IX+d),C
CBBB	RES 7,E	CBF0	SET 6,B	DD72d	LD (IX+d),D
CBBC	RES 7,H	CBF1	SET 6,C	DD73d	LD (IX+d),E
CBBD	RES 7,L	CBF2	SET 6,D	DD74d	LD (IX+d),H
CBBE	RES 7,(HL)	CBF3	SET 6,E	DD75d	LD (IX+d),L
CBBF	RES 7,A	CBF4	SET 6,H	DD77d	LD (IX+d),A
CBC0	SET 0,B	CBF5	SET 6,L	DD7Ed	LD A,(IX+d)
CBC1	SET 0,C	CBF6	SET 6,(HL)	DD86d	ADD A,(IX+d)
CBC2	SET 0,D	CBF7	SET 6,A	DD8Ed	ADC A,(IX+d)
CBC3	SET 0,E	CBF8	SET 7,B	DD96d	SUB (IX+d)
CBC4	SET 0,H	CBF9	SET 7,C	DD9Ed	SBC A,(IX+d)
CBC5	SET 0,L	CBFA	SET 7,D	DDA6d	AND (IX+d)
CBC6	SET 0,(HL)	CBFB	SET 7,E	DDAEd	XOR (IX+d)
CBC7	SET 0,A	CBFC	SET 7,H	DDB6d	OR (IX+d)
CBC8	SET 1,B	CBFD	SET 7,L	DDBEd	CP (IX+d)
CBC9	SET 1,C	CBFE	SET 7,(HL)	DDCBd06	RLC (IX+d)
CBCA	SET 1,D	CBFF	SET 7,A	DDCBd0E	RRC (IX+d)
CBCB	SET 1,E	CCnn	CALL Z,nn	DDCBd16	RL (IX+d)
CBCC	SET 1,H	CDnn	CALL nn	DDCBd1E	RR (IX+d)
CBCD	SET 1,L	CEn	ADC A,n	DDCBd26	SLA (IX+d)
CBCE	SET 1,(HL)	CF	RST 8	DDCBd2E	SRA (IX+d)
CBCF	SET 1,A	D0	RET NC	DDCBd3E	SRL (IX+d)
CBD0	SET 2,B	D1	POP DE	DDCBd46	BIT 0,(IX+d)
CBD1	SET 2,C	D2nn	JP NC,nn	DDCBd4E	BIT 1,(IX+d)
CBD2	SET 2,D	D3n	OUT (n),A	DDCBd56	BIT 2,(IX+d)
CBD3	SET 2,E	D4nn	CALL NC,nn	DDCBd5E	BIT 3,(IX+d)
CBD4	SET 2,H	D5	PUSH DE	DDCBd66	BIT 4,(IX+d)
CBD5	SET 2,L	D6n	SUB n	DDCBd6E	BIT 5,(IX+d)
CBD6	SET 2,(HL)	D7	RST 10H	DDCBd76	BIT 6,(IX+d)
CBD7	SET 2,A	D8	RET C	DDCBd7E	BIT 7,(IX+d)
CBD8	SET 3,B	D9	EXX	DDCBd86	RES 0,(IX+d)
CBD9	SET 3,C	DAnn	JP,C,nn	DDCBd8E	RES 1,(IX+d)
CBDA	SET 3,D	DBn	IN A,(n)	DDCBd96	RES 2,(IX+d)
CBDB	SET 3,E	DCnn	CALL C,nn	DDCBd9E	RES 3,(IX+d)
CBDC	SET 3,H	DD09	ADD IX,BC	DDCBdA6	RES 4,(IX+d)
CBDD	SET 3,L	DD19	ADD IX,DE	DDCBdAE	RES 5,(IX+d)
CBDE	SET 3,(HL)	DD21nn	LD IX,nn	DDCBdB6	RES 6,(IX+d)
CBDF	SET 3,A	DD22	LD (nn),IX	DDCBdBE	RES 7,(IX+d)
CBE0	SET 4,B	DD23	INC IX	DDCBdC6	SET 0,(IX+d)
CBE1	SET 4,C	DD29	ADD IX,IX	DDCBdCE	SET 1,(IX+d)
CBE2	SET 4,D	DD2Ann	LD IX,(nn)	DDCBdD6	SET 2,(IX+d)
CBE3	SET 4,E	DD2B	DEC IX	DDCBdDE	SET 3,(IX+d)
CBE4	SET 4,H	DD34d	INC (IX+d)	DDCBdE6	SET 4,(IX+d)
CBE5	SET 4,L	DD35d	DEC (IX+d)	DDCBdEE	SET 5,(IX+d)
CBE6	SET 4,(HL)	DD36dn	LD (IX+d),n	DDCBdF6	SET 6,(IX+d)
CBE7	SET 4,A	DD39	ADD IX,SP	DDCBdFE	SET 7,(IX+d)
CBE8	SET 5,B	DD46d	LD B,(IX+d)	DDE1	POP IX
CBE9	SET 5,C	DD4Ed	LD C,(IX+d)	DDE3	EX (SP),IX
CBEA	SET 5,D	DD56d	LD D,(IX+d)	DDE5	PUSH IX
CBEB	SET 5,E	DD5Ed	LD E,(IX+d)	DDE9	JP (IX)

(nn) = Address of memory location d = displacement
nn = Data (16 bit) d2 = d−2
n = Data (8-bit)

12.16 Instruction Set: Numerical Order (Continued)

Op Code	Mnemonic
DDF9	LD SP,IX
DEn	SCB A,n
DF	RST 18H
E0	RET PO
E1	POP HL
E2nn	JP PO,nn
E3	EX (SP),HL
E4nn	CALL PO,nn
E5	PUSH HL
E6n	AND n
E7	RST 20H
E8	RET PE
E9	JP (HL)
EAnn	JP PE,nn
EB	EX DE,HL
ECnn	CALL PE,nn
ED40	IN B,(C)
ED41	OUT (C),B
ED42	SBC HL,BC
ED43nn	LD (nn),BC
ED44	NEG
ED45	RETN
ED46	IM 0
ED47	LD I,A
ED48	IN C,(C)
ED49	OUT (C),C
ED4A	ADC HL,BC
ED4Bnn	LD BC,(nn)
ED4D	RETI
ED50	IN D,(C)
ED51	OUT (C),D
ED52	SBC HL,DE
ED53nn	LD (nn),DE
ED56	IM 1
ED57	LD A,I
ED58	IN E,(C)
ED59	OUT (C), E
ED5A	ADC HL,DE
ED5Bnn	LD DE,(nn)
ED5E	IM 2
ED60	IN H,(C)
ED61	OUT (C),H
ED62	SBC HL,HL
ED67	RRD
ED68	IN L,(C)
ED69	OUT (C),L
ED6A	ADC HL,HL
ED6F	RLD
ED72	SBC HL,SP
ED73nn	LD (nn),SP
ED78	IN A,(C)
ED79	OUT (C),A
ED7A	ADC HL,SP
ED7Bnn	LD SP,(nn)
EDA0	LDI
EDA1	CPI
EDA2	INI
EDA3	OUTI
EDA8	LDD
EDA9	CPD
EDAA	IND
EDAB	OUTD
EDB0	LDIR
EDB1	CPIR
EDB2	INIR
EDB3	OTIR
EDB8	LDDR
EDB9	CPDR
EDBA	INDR
EDBB	OTDR
EEn	XOR n
EF	RST 28H
F0	RET P
F1	POP AF
F2nn	JP P,nn
F3	DI
F4nn	CALL P,nn
F5	PUSH AF
F6n	OR n
F7	RST 30H
F8	RET M
F9	LD SP,HL
FAnn	JP M,nn
FB	EI
FCnn	CALL M,nn
FD09	ADD IY,BC
FD19	ADD IY,DE
FD21nn	LD IY,nn
FD22nn	LD (nn),IY
FD23	INC IY
FD29	ADD IY,IY
FD2Ann	LD IY,(nn)
FD2B	DEC IY
FD34d	INC (IY+d)
FD35d	DEC (IY+d)
FD36dn	LD (IY+d),n
FD39	ADD IY,SP
FD46d	LD B,(IY+d)
FD4Ed	LD C,(IY+d)
FD56d	LD D,(IY+d)
FD5Ed	LD E,(IY+d)
FD66d	LD H,(IY+d)
FD6Ed	LD L,(IY+d)
FD70d	LD (IY+d),B
FD71d	LD (IY+d),C
FD72d	LD (IY+d),D
FD73d	LD (IY+d),E
FD74d	LD (IY+d),H
FD75d	LD (IY+d),L
FD77d	LD (IY+d),A
FD7Ed	LD A,(IY+d)
FD86d	ADD A,(IY+d)
FD8Ed	ADC A,(IY+d)
FD96d	SUB (IY+d)
FD9Ed	SBC A,(IY+d)
FDA6d	AND (IY+d)
FDAEd	XOR (IY+d)
FDB6d	OR (IY+d)
FDBEd	CP (IY+d)
FDE1	POP IY
FDE3	EX (SP), IY
FDE5	PUSH IY
FDE9	JP (IY)
FDF9	LD SP,IY
FDCBd06	RLC (IY+d)
FDCBd0E	RRC (IY+d)
FDCBd16	RL (IY+d)
FDCBd1E	RR (IY+d)
FDCBd26	SLA (IY+d)
FDCBd2E	SRA (IY+d)
FDCBd3E	SRL (IY+d)
FDCBd46	BIT 0,(IY+d)
FDCBd4E	BIT 1,(IY+d)
FDCBd56	BIT 2,(IY+d)
FDCBd5E	BIT 3,(IY+d)
FDCBd66	BIT 4,(IY+d)
FDCBd6E	BIT 5,(IY+d)
FDCBd76	BIT 6,(IY+d)
FDCBd7E	BIT 7,(IY+d)
FDCBd86	RES 0,(IY+d)
FDCBd8E	RES 1,(IY+d)
FDCBd96	RES 2,(IY+d)
FDCBd9E	RES 3,(IY+d)
FDCBdA6	RES 4,(IY+d)
FDCBdAE	RES 5,(IY+d)
FDCBdB6	RES 6,(IY+d)
FDCBdBE	RES 7,(IY+d)
FDCBdC6	SET 0,(IY+d)
FDCBdCE	SET 1,(IY+d)
FDCBdD6	SET 2,(IY+d)
FDCBdDE	SET 3,(IY+d)
FDCBdE6	SET 4,(IY+d)
FDCBdEE	SET 5,(IY+d)
FDCBdF6	SET 6,(IY+d)
FDCBdFE	SET 7,(IY+d)
FEn	CP n
FF	RST 38H

(nn) = Address of memory location d = displacement

nn = Data (16 bit) d2 = d − 2

n = Data (8-bit)

13.0 Data Acquisition System

A natural application for the NSC800 is one that requires remote operation. Since power consumption is low if the system consists of only CMOS components, the entire package can conceivably operate from only a battery power source. In the application described herein, the only source of power will be from a battery pack composed of a stacked array of NiCad batteries (see *Figure 20*).

The application is that of a remote data acquisition system. Extensive use is made of some of the other LSI CMOS components manufactured by National: notably the ADC0816 and MM58167. The ADC0816 is a 16-channel analog-to-digital converter which operates from a 5V source. The MM58167 is a microprocessor-compatible real-time clock (RTC). The schematic for this system is shown in *Figure 20*. All the necessary features of the system are contained in six integrated circuits: NSC800, NSC810A, NSC831, HN6136P, ADC0816, and MM58167. Some other small scale integration CMOS components are used for normal interface requirements. To reduce component count, linear selection techniques are used to generate chip selects for the NSC810A and NSC831. Included also is a current loop communication link to enable the remote system to transfer data collected to a host system.

In order to keep component count low and maximize effectiveness, many of the features of the NSC800 family have been utilized. The RAM section of the NSC810A is used as a data buffer to store intermediate measurements and as scratch pad memory for calculations. Both timers contained in the NSC810A are used to produce the clocks required by the A/D converter and the RTC. The Power-Save feature of the NSC800 makes it possible to reduce system power consumption when it is not necessary to collect any data. One of the analog input channels of the A/D is connected to the battery pack to enable the CPU to monitor its own voltage supply and notify the host that a battery change is needed.

In operation, the NSC800 makes readings on various input conditions through the ADC0816. The type of devices connected to the A/D input depends on the nature of the remote environment. For example, the duties of the remote system might be to monitor temperature variations in a large building. In this case, the analog inputs would be connected to temperature transducers. If the system is situated in a process control environment, it might be monitoring fluid flow, temperatures, fluid levels, etc. In either case, operation would be necessary even if a power failure occurred, thus the need for battery operation or at least battery backup. At some fixed times or at some particular time durations, the system takes readings by selecting one of the analog input channels, commands the A/D to perform a conversion, reads the data, and then formats it for transmission; or, the system checks the readings against set points and transmits a warning if the set points are exceeded. With the addition of the RTC, the host need not command the remote system to take these readings each time it is necessary. The NSC800 could simply set up the RTC to interrupt it at a previously defined time and when the interrupt occurs, make the readings. The resultant values could be stored in the NSC810A for later correlation. In the example of temperature monitoring in a building, it might be desired to know the high and low temperatures for a 12-hour period. After compiling the information, the system could dump the data to the host over the communications link. Note from the schematic that the current for the communication link is supplied by the host to remove the constant current drain from the battery supply.

The required clocks for the two peripheral devices are generated by the two timers in the NSC810A. Through the use of various divisors, the master clock generated by the NSC800 is divided down to produce the clocks. Four examples are shown in the table following *Figure 20*.

All the crystal frequencies are standard frequencies. The various divisors listed are selected to produce, from the master clock frequency of the NSC800, an exact 32,768 Hz clock for the MM58167 and a clock within the operating range of the A/D converter.

The MM58167 is a programmable real-time clock that is microprocessor compatible. Its data format is BCD. It allows the system to program its interrupt register to produce an interrupt output either on a time of day match (which includes the day of the week, the date and month) and/or every month, week, day, hour, minute, second, or tenth of a second. With this capability added to the system, precise time of day measurements are possible without having the CPU do timekeeping. The interrupt output can be connected, through the use of one port bit of the NSC810A, to put the CPU in the power-save mode and reenable it at a preset time. The interrupt output is also connected to one of the hardware restart inputs ($\overline{\text{RSTB}}$) to enable time duration measurements. This power-down mode of operation would not be possible if the NSC800 had the duties of timekeep-

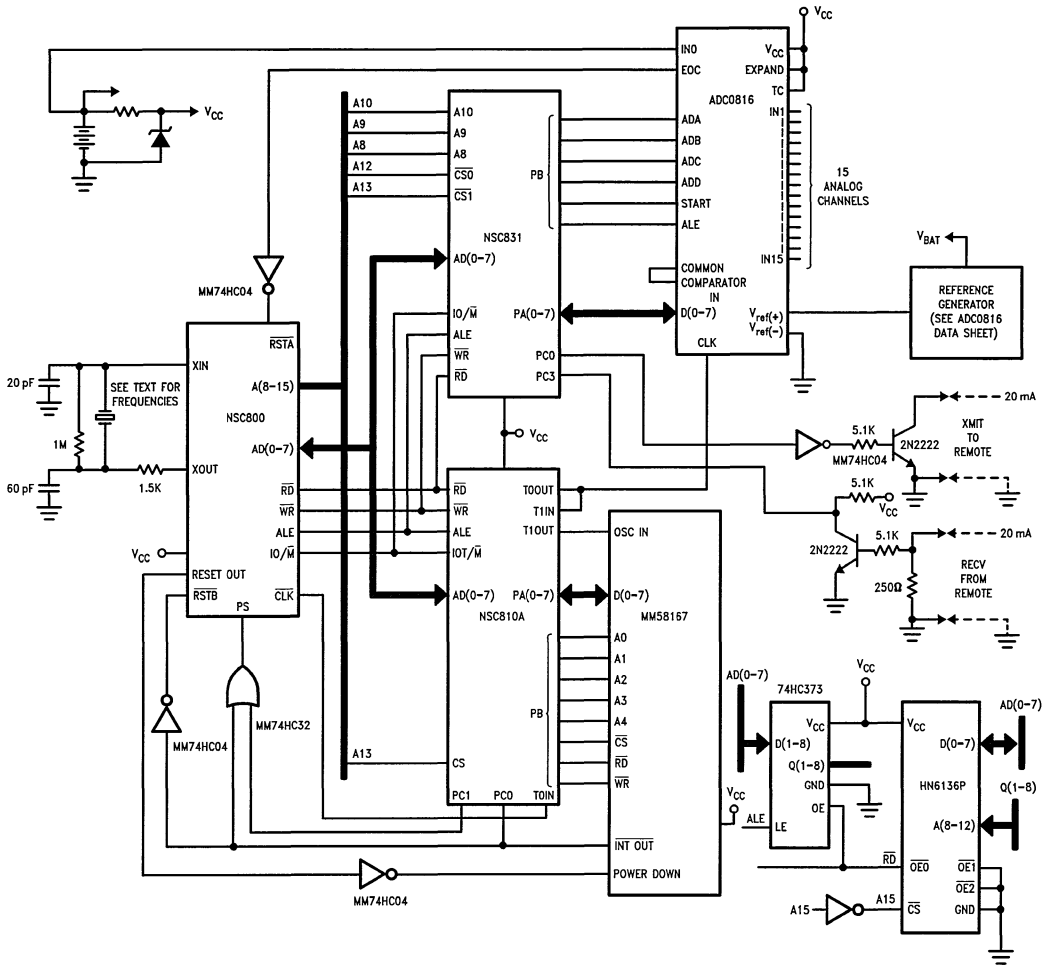

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FIGURE 20. Remote Data Acquisition

13.0 Data Acquisition System (Continued)

ing. When in the power-save mode, the system power requirements are decreased by about 50%, thus extending battery life.

Communication with the peripheral devices (MM58167 and ADC0816) is accomplished through the I/O ports of the NSC810A and NSC831. The peripheral devices are not connected to the bus of the NSC800 as they are not directly compatible with a multiplexed bus structure. Therefore, additional components would be required to place them on the microprocessor bus. Writing data into the MM58167 is performed by first putting the desired data on Port A, followed by selecting the address of the internal register and applying the chip select through the use of Port B. A bit set and clear operation is performed to emulate a pulse on the bit of Port B connected to the $\overline{WR}$ input of the MM58167. For a read operation, the same sequence of operations is performed except that Port A is set for the input mode of operation and the $\overline{RD}$ line is pulsed. Similar techniques are used to read converted data from the A/D converter. When a conversion is desired, the CPU selects a channel and commands the ADC0816 to start a conversion. When the conversion is complete, the converter will produce an End-of-Conversion signal which is connected to the $\overline{RSTA}$ interrupt input of the NSC800.

When operating, the system shown consumes about 125 mw. When in the power-save mode, power consumption is decreased to about 70 mw. If, as is likely, the system is in the power-save mode most of the time, battery life can be quite long depending on the amp-hour rating of the batteries incorporated into the system. For example, if the battery pack is rated at 5 amp-hours, the system should be able to operate for about 400-500 hours before a battery charge or change is required.

As shown in the schematic (refer to *Figure 20*), analog input IN0 is connected to the battery source. In this way, the CPU can monitor its own power source and notify the host that it needs a battery replacement or charge. Since the battery source shown is a stacked array of 7 NiCads producing 8.4V, the converter input is connected in the middle so that it can take a reading on two or three of the cells. Since NiCad batteries have a relatively constant voltage output until very nearly discharged, the CPU can sense that the "knee" of the discharge curve has been reached and notify the host.

Typical Timer Output Frequencies

Crystal Frequency	CPU Clock Output	Timer 0 Output	Timer 1 Output
2.097152 MHz	1.048576 MHz	262.144 kHz divisor = 4	32.768 kHz divisor = 8
3.276800 MHz	1.638400 MHz	327.680 kHz divisor = 5	32.768 kHz divisor = 10
4.194304 MHz	2.097152 MHz	262.144 kHz divisor = 8	32.768 kHz divisor = 8
4.915200 MHz	2.457600 MHz	491.520 kHz divisor = 5	32.768 kHz divisor = 15

14.0 NSC800M/883B MIL-STD-833 Class C Screening

National Semiconductor offers the NSC800D and NSC800E with full class B screening per MIL-STD-883 for Military/ Aerospace programs requiring high reliability. In addition, this screening is available for all of the key NSC800 peripheral devices.

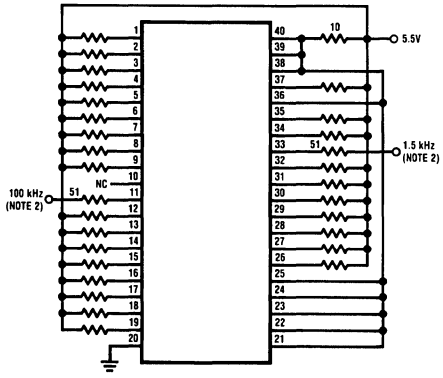
Electrical testing is performed in accordance with RESTS800X, which tests or guarantees all of the electrical performance characteristics of the NSC800 data sheet. A copy of the current revision of RETS800X is available upon request.

100% Screening Flow

Test	MIL-STD-883 Method/Condition	Requirement
Internal Visual	2010B	100%
Stabilization Bake	1008 C 24 Hrs. @ +150°C	100%
Temperature Cycling	1010 C 10 Cycles −65°C/+150°C	100%
Constant Acceleration	2001 E 30,000 G's, Y1 Axis	100%
Fine Leak	1014 A or B	100%
Gross Leak	1014C	100%
Burn-In	1015 160 Hrs. @ +125°C (using burn-in circuits shown below)	100%
Final Electrical	+25°C DC per RETS800X	100%
PDA	10% Max	
	+125°C AC and DC per RETS800X	100%
	−55°C AC and DC per RETS800X	100%
	+25°C AC per RETS800X	100%
QA Acceptance	5005	Sample Per
Quality Conformance		Method 5005
External Visual	2009	100%

15.0 Burn-In Circuits

5240HR
NSC800D/883B (Dual-In-Line)



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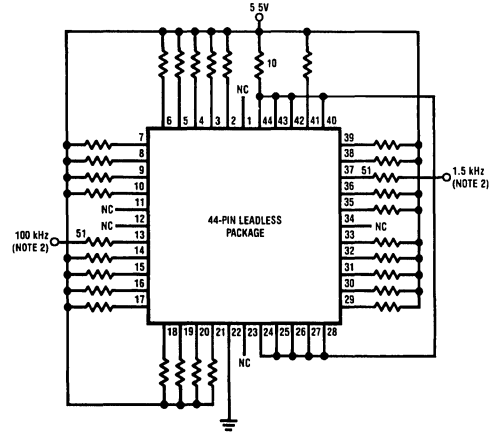
Top View

5241HR
NSC800E/883B (Leadless Chip Carrier)



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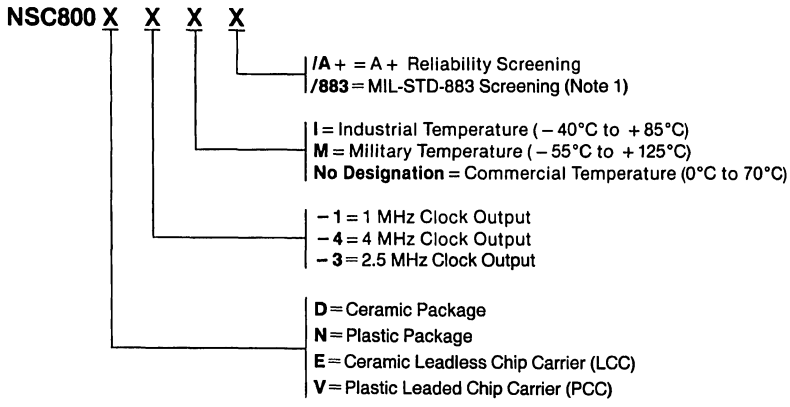
All resistors 2.7 kΩ unless marked otherwise.

Note 1: All resistors are ¼W ± 5% unless otherwise specified.

Note 2: All clocks 0V to 3V, 50% duty cycle, in phase with < 1 μs rise and fall time.

Note 3: Device to be cooled down under power after burn-in.

16.0 Ordering Information



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Note 1: Do not specify a temperature option; all parts are screened to military temperature.

17.0 Reliability Information

Gate Count 2750

Transistor Count 11,000

National Semiconductor

NSC810A RAM-I/O-Timer

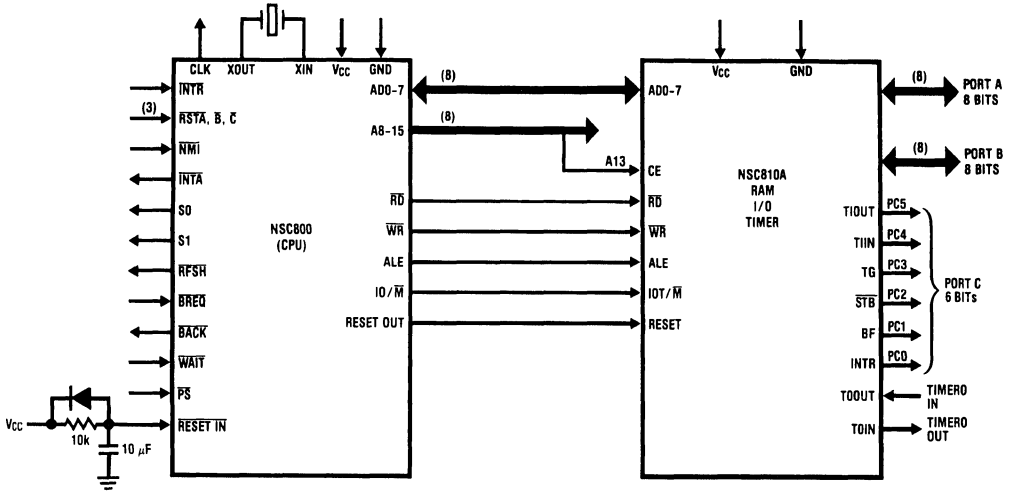
General Description

The NSC810A, the luxury model of our NSC800™ peripheral line, sports triple ported I/O, dual 16-bit timers and a 1024-bit static storage area. The three ports can be combined for a total of 22 general purpose I/O lines. In addition, port A has several strobed mode operations. Note the single instruction I/O bit operations for quick and efficient data handling from the ports. The timers feature 6 modes of operation and prescalers for those complicated timing tasks. The NSC810A comes in two models: the Dual-In-Line (DIP) and the surface mount chip carrier (LCC). It also comes in three exciting temperature ranges (Commercial, Industrial, and Military) and two reliability flows (extended burn-in and military class B in accordance with Method 5004 of MIL-STD-883). This is brought to you through the microCMOS silicon gate technology of National Semiconductor.

Features

- Three programmable I/O ports
- Dual 16-bit programmable counter/timers
- 2.4V–6.0V power supply
- Very low power consumption
- Fully static operation
- Single-instruction I/O bit operations
- Timer operation—DC to 5 MHz
- Bus compatible with NSC800™ family
- Speed: compatible with NSC800
  NSC810A-4 → NSC800-4 @ 4.0 MHz
  NSC810A-3 → NSC800 @ 2.5 MHz
  NSC810A-1 → NSC800-1 @ 1.0 MHz

NSC810A Connection Diagram



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1.0 Absolute Maximum Ratings

(Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Storage Temperature Range	−65°C to +150°C
Voltage at Any Pin with Respect to Ground	−0.3V to V_{CC} + 0.3V
V_{CC}	7V
Power Dissipation	1W
Lead Temperature (Soldering, 10 seconds)	300°C

2.0 Operating Conditions

V_{CC} = 5V ± 10%

NSC810A-1 → 0°C to +70°C
−40°C to +85°C

NSC810A-3 → 0°C to +70°C
−40°C to +85°C
−55°C to +125°C

NSC810A-4 → 0°C to +70°C
−40°C to +85°C
−55°C to +125°C

3.0 DC Electrical Characteristics

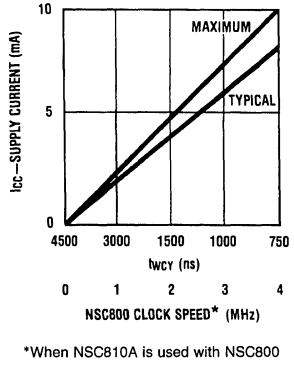
V_{CC}=5V ±10%, GND=0V, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	Logical 1 Input Voltage		0.8 V_{CC}		V_{CC}	V
V_{IL}	Logical 0 Input Voltage		0		0.2 V_{CC}	V
V_{OH}	Logical 1 Output Voltage	I_{OH} = −1.0 mA I_{OUT} = −10 μA	2.4 V_{CC}−0.5			V V
V_{OL}	Logical 0 Output Voltage	I_{OL} = 2 mA I_{OUT} = 10 μA	0 0		0.4 0.1	V V
I_{IL}	Input Leakage Current	$0 \le V_{IN} \le V_{CC}$	−10.0		10.0	μA
I_{OL}	Output Leakage Current	$0 \le V_{IN} \le V_{CC}$	−10.0		10.0	μA
I_{CC}	Active Supply Current	I_{OUT} = 0, Timer = Mode 1, T0IN = T1IN = 2.5 Mhz, t_{WCY} = 750 ns, T_A = 25°C		8	10	mA
I_Q	Quiescent Current	No Input Switching, T_A = 25°C, RESET = 0, IO/$\overline{M}$ = 1, $\overline{RD}$ = 1, $\overline{WR}$ = 1, ALE = 1, V_{IN} = V_{CC}, t_{IN} = 0 Hz, t_{OUT} = 0		10	100	μA
C_{IN}	Input Capacitance			4	7	pF
C_{OUT}	Output Capacitance			6	10	pF
V_{CC}	Power Supply Voltage	(Note 2)	2.4	5	6	V
V_{DRV}	Data Retention Voltage		1.8			V

Note 1: Absolute maximum ratings are those values beyond which the safety of the device cannot be guaranteed. Continuous operation at these limits is not intended; operation should be limited to those conditions specified under DC Electrical Characteristics.

Note 2: Operation at lower power supply voltages will reduce the maximum operating speed. Operation at voltages other than 5V ±10% is guaranteed by design, not tested.

I_{CC} vs Speed



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*When NSC810A is used with NSC800

4.0 AC Electrical Characteristics $V_{CC}=5V \pm 10\%$, GND = 0V

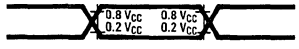
Symbol	Parameter	Conditions	NSC810A-1		NSC810A-3		NSC810-4		Units
			Min	Max	Min	Max	Min	Max	
t_{ACC}	Access Time from ALE	C_L = 150 pF		1000		400		300	ns
t_{AH}	AD0-7, CE, IOT/$\overline{M}$ Hold Time		100		60		30		ns
t_{ALE}	ALE Strobe Width (High)		200		125		100		ns
t_{ARW}	ALE to $\overline{RD}$ or $\overline{WR}$ Strobe		150		120		75		ns
t_{AS}	AD0-7, CE, IOT/$\overline{M}$ Set-Up Time		100		45		25		ns
t_{DH}	Data Hold Time		150		90		40		ns
t_{DO}	Port Data Output Valid			350		310		300	ns
t_{DS}	Data Set-Up Time		100		80		50		ns
t_{PE}	Peripheral Bus Enable			320		200		200	ns
t_{PH}	Peripheral Data Hold Time		150		125		100		ns
t_{PS}	Peripheral Data Set-Up Time		100		75		50		ns
t_{PZ}	Peripheral Bus Disable (TRI-STATE®)			150		150		150	ns
t_{RB}	$\overline{RD}$ to BF Invalid			300		300		300	ns
t_{RD}	Read Strobe Width		400		320		185		ns
t_{RDD}	Data Bus Disable		0	100	0	100	0	75	ns
t_{RI}	$\overline{RD}$ to $\overline{INTR}$ Output			320		320		300	ns
t_{RWA}	$\overline{RD}$ or $\overline{WR}$ to Next ALE		125		100		75		ns
t_{SB}	$\overline{STB}$ to BF Valid			300		300		300	ns
t_{SH}	Peripheral Data Hold with Respect to $\overline{STB}$		150		125		100		ns
t_{SI}	$\overline{STB}$ to $\overline{INTR}$ Output			300		300		300	ns
t_{SS}	Peripheral Data Set-Up with Respect to $\overline{STB}$		100		75		50		ns
t_{SW}	$\overline{STB}$ Width		400		320		220		ns
t_{WB}	$\overline{WR}$ to BF Output			340		340		300	ns
t_{WI}	$\overline{WR}$ to $\overline{INTR}$ Output			320		320		300	ns
t_{WR}	$\overline{WR}$ Strobe Width		400		320		220		ns
t_{WCY}	Width of Machine Cycle		3000		1200		750		ns

Note: Test conditions: t_{WCY} = 3000 ns for NSC810A-1, 1200 ns for NSC810A-3, 750 ns for NSC810A-4

5.0 Timer AC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
F_C	Clock Frequency		DC		2.5	MHz
F_{CP}	Clock Frequency	Prescale Selected	DC		5.0	MHz
t_{CW}	Clock Pulse Width		150			ns
t_{CWP}	Clock Pulse Width	Prescale Selected	75			ns
t_{GS}	Gate Set-Up Time	With Respect to Negative Clock Edge	100			ns
t_{GH}	Gate Hold Time	With Respect to Negative Clock Edge	250			ns
t_{CO}	Clock to Output Delay	C_L = 100 pF			350	ns

AC TESTING INPUT/OUTPUT WAVEFORM



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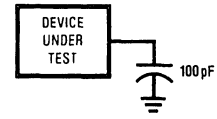
AC TESTING LOAD CIRCUIT



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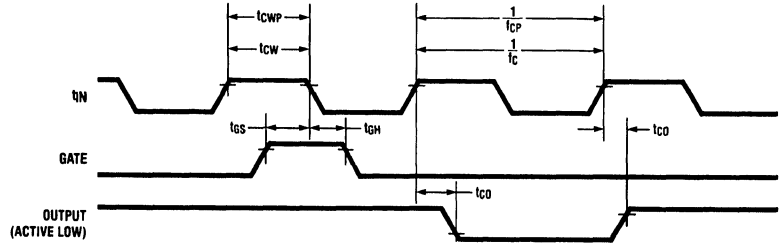
6.0 Timing Waveforms

Timer Waveforms



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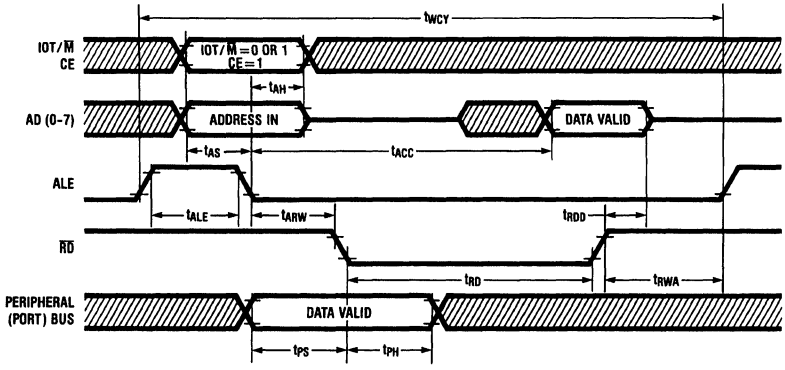
Read Cycle (Read from RAM, Port or Timer)



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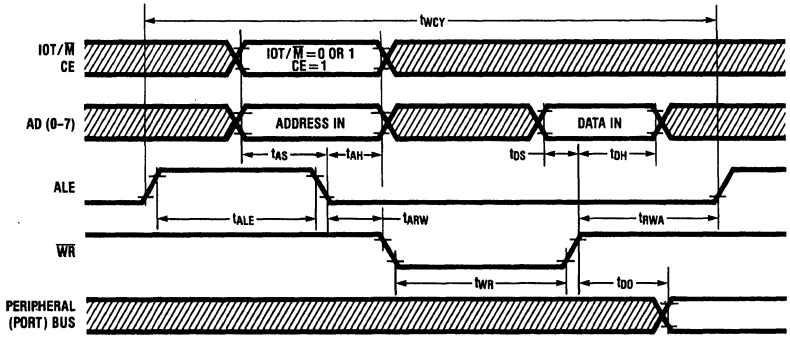
Note: Diagonal lines indicate interval of invalid data.

Write Cycle (Write to RAM, Port or Timer)



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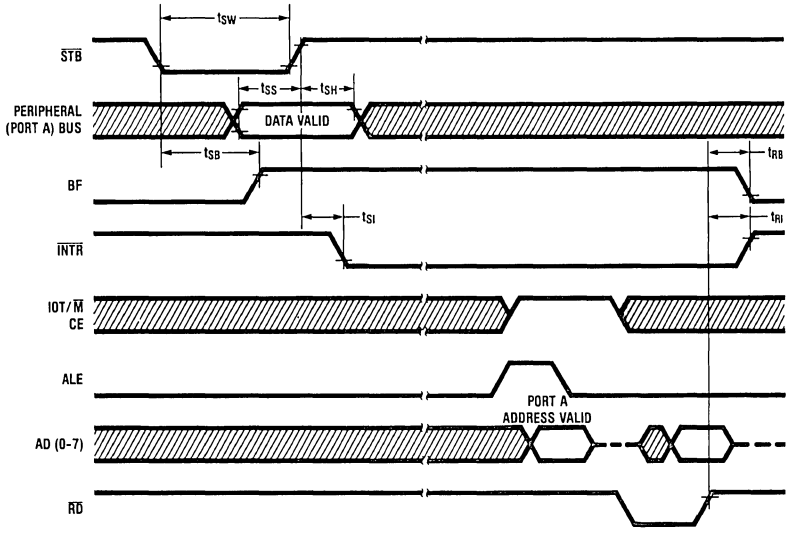
Note: Diagonal lines indicate interval of invalid data.

6.0 Timing Waveforms (Continued)

Strobed Mode Input



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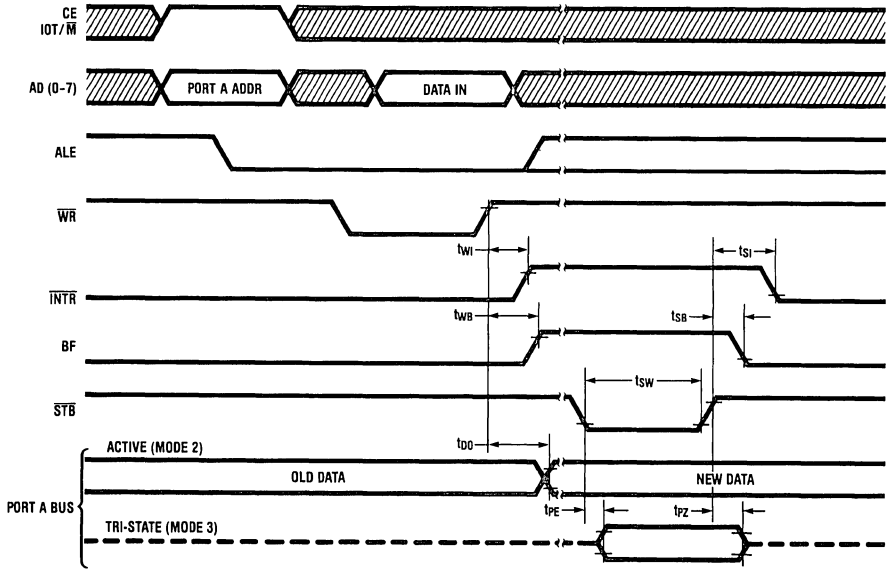
Note: Diagonal lines indicate interval of invalid data.

Strobed Mode Output



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Note: Diagonal lines indicate interval of invalid data.

7.0 Pin Descriptions

The function and mnemonic for the NSC810A signals are described below:

7.1 INPUT SIGNALS

Reset (RESET): RESET is an active-high input that resets all registers to 0 (low). The RAM contents remain unaltered.

Input/Output Timer or RAM Select (IOT/$\overline{M}$): IOT/$\overline{M}$ is an I/O memory select input line. A logic 1 (high) input selects the I/O-timer portion of the chip; a logic 0 (low) input selects the RAM portion of the chip. IOT/$\overline{M}$ is latched at the falling edge of ALE.

Chip Enable (CE): CE is an active-high input that allows access to the NSC810A. CE is latched at the falling edge of ALE.

Read ($\overline{RD}$): The $\overline{RD}$ is an active-low input that enables a read operation of the RAM or I/O-timer location.

Write ($\overline{WR}$): The $\overline{WR}$ is an active-low input that enables a write operation to RAM or I/O-timer locations.

Address Latch Enable (ALE): The falling edge of the ALE input latches AD0–AD7, CE and IOT/$\overline{M}$ inputs to form the address for RAM, I/O or timer.

Timer 0 Input (T0IN): T0IN is the clock input for timer 0.

7.2 OUTPUT SIGNALS

Timer 0 Output (T0OUT): T0OUT is the programmable output of timer 0. After reset, T0OUT is set high.

7.3 POWER SUPPLY SIGNALS

Positive DC Voltage (V_{CC}): V_{CC} is the 5V supply pin.

Ground (GND): Ground reference pin.

7.4 INPUT/OUTPUT SIGNALS

Address/Data Bus (AD0–AD7): The multiplexed bidirectional address/data bus; AD0–AD7 pins, are in the high impedance state when the NSC810A is not selected. AD0–AD7 will latch address inputs at the falling edge of ALE. The address will designate a location in RAM, I/O or timer. $\overline{WR}$ input enables 8-bit data to be written into the addressed location. $\overline{RD}$ input enables 8-bit data to be read from the addressed location. The $\overline{RD}$ or $\overline{WR}$ inputs occur while ALE is low.

Port A, 0–7 (PA0–PA7): Port A is an 8-bit basic mode input/output port, also capable of strobed mode I/O utilizing three control signals from port C. Strobed mode of operation on port A has three different modes; strobed input, strobed output with active peripheral bus, strobed output with TRI-STATE peripheral bus.

Port B, 0–7 (PB0–PB7): Port B is an 8-bit basic mode input/output port.

Port C, 0–5 (PC0–PC5): Port C is a 6-bit basic mode I/O port. Each pin has a programmable second function, as follows:

PC0/$\overline{INTR}$: $\overline{INTR}$ is an active-low, strobed mode interrupt request to the Central Processor Unit (CPU).

PC1/BF: BF is an active-high, strobed mode, buffer full output to peripheral devices.

PC2/$\overline{STB}$: $\overline{STB}$ is an active-low, strobed mode input from peripheral devices.

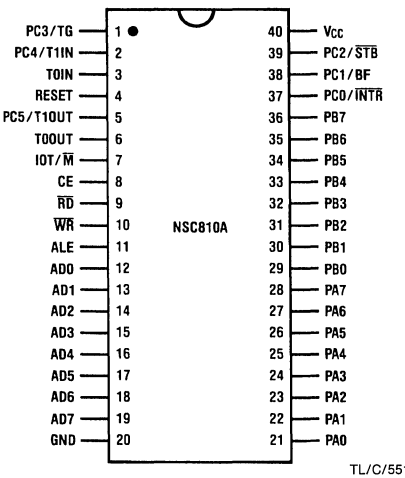
PC3/TG: TG is the timer gating signal.

PC4/T1IN: T1IN is the clock input for timer 1.

PC5/T1OUT: T1OUT is the programmable output of timer 1.

8.0 Connection Diagrams

Dual-In-Line Package



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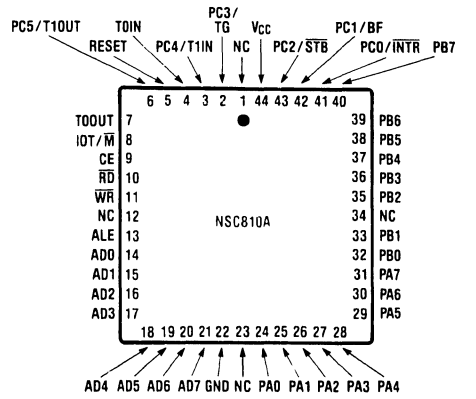
Top View

Order Number NSC810AD or NSC810AN
See NS Package Number D40C or N40A

Chip Carrier



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Top View

NC = no connect

Order Number NSC810AE or NSC810AV
See NS Package Number E44B or V44A

9.0 Functional Description

Figure 1 is a detailed block diagram of the NSC810A. The functional description that follows describes the RAM, I/O and TIMER sections.

9.1 RANDOM ACCESS MEMORY (RAM)

The memory portion of the RAM-I/O-timer is accessed by a 7-bit address input to pins AD0 through AD6. The IOT/$\overline{M}$ input must be low (RAM select) and the CE input must be high at the falling edge of ALE to address the RAM. Address bit AD7 is a "don't care" for RAM addressing. Timing for RAM read and write operations is shown in the timing diagrams. The RAM is 128 x 8.

9.2 DETAILED BLOCK DIAGRAM

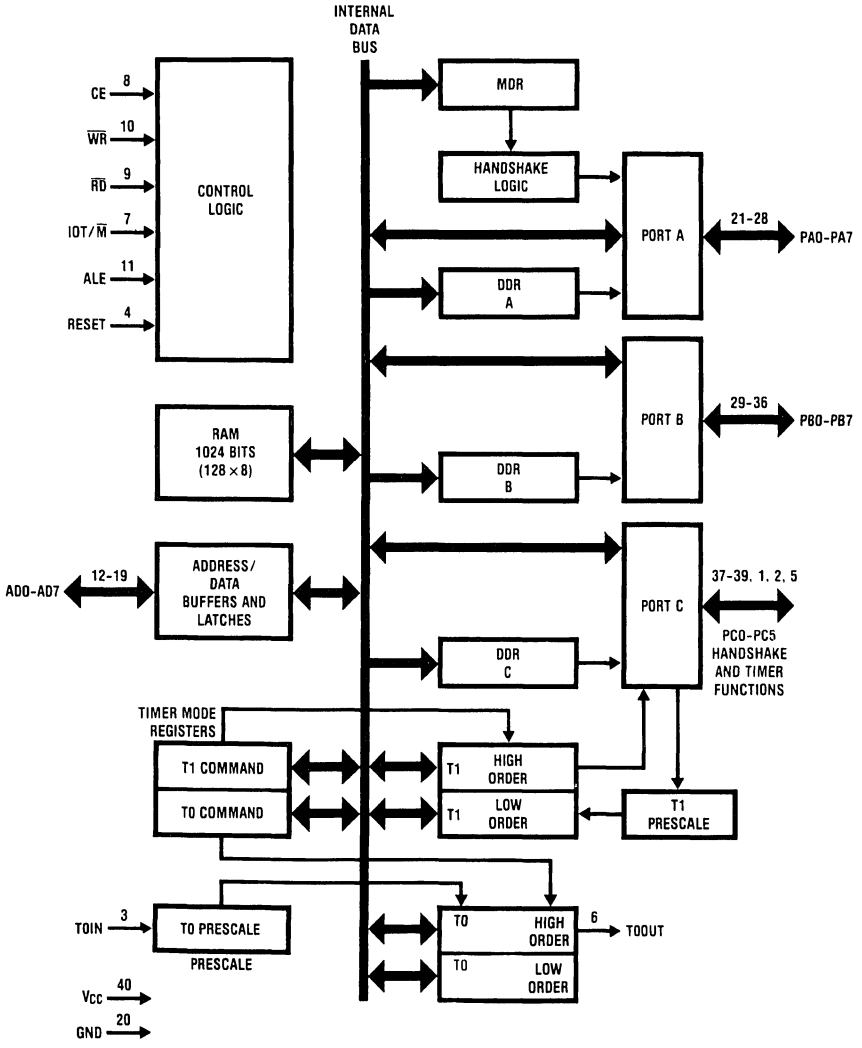

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FIGURE 1

9.0 Functional Description (Continued)

9.3 I/O PORTS

The three I/O ports, labeled A, B, and C, can be programmed to be almost any combination of Input and Output bits. Ports A and B are configured as 8 bits wide, while port C is 6 bits. There are four different modes of operation for the ports. Three of the modes are for timed transfer of data between the peripheral and the NSC810A, this is called strobed I/O. The fourth mode is for direct transfer without handshaking with the peripheral.

The NSC810A can be programmed to operate in four different modes. One of these modes (Basic I/O) allows direct transfer of I/O data without any handshaking between the NSC810A and the peripheral. The other three modes (Strobed I/O) provide for timed transfers of I/O data with handshaking between the NSC810A and the peripheral.

The determination of the mode, data direction and data is done by five registers which are, handily, under program control. The Mode Definition Register (MDR), oddly enough, determines which mode the device will operate in, while the Data Direction Register (DDR) establishes the direction of the data transfer. The Data register contains the data that is being sent or has been received. The other two registers (bit-set, bit-clear) allow the individual bits in the data register to be set or cleared without affecting the other bits. Each port has its own set of these registers, except the MDR which affects ports A and C only.

In the strobed I/O modes, port C bits 0, 1 and 2 function as INTR (for the processor), BF, and STB respectively.

9.3.1 Registers

As can be seen in Table I, all the registers affecting I/O transfer are grouped at the lower address locations, this allows quicker handling and more maneuverability in tight data transfers. Also note in Table I that the NSC810A uses 23 I/O addresses out of a block of 26. The upper three bits of the address are determined by the chip enable address.

- **Mode Definition Register (MDR)**

As noted above this register defines the operating mode for ports A and C (port B is always in the basic I/O mode). The upper 3 bits of port C will also be in the basic I/O mode even when the lower 3 bits are being used for handshaking.

The four modes are as follows:

Mode 0—Basic I/O (Input or Output)

Mode 1—Strobed Mode Input

Mode 2—Strobed Mode Output (Active Peripheral Bus)

Mode 3—Strobed Mode Output (TRI-STATE Peripheral Bus)

The address assignment of the MDR is xxx00111 as shown in Table I. Table II specifies the data that must be loaded into the MDR to select the mode.

- **Data Direction Registers (DDR)**

Each port has a DDR that determines whether an individual port bit will be an input or an output. This can be considered the traffic light for the transfer of data between the CPU and the peripheral. Each port bit has a corresponding bit in this register. If the DDR bit is set (1) the port bit is an output; if it is cleared (0) the port bit is an input. The DDR bits cannot be written to individually. The register as a whole must be set to be consistent with all desired port bit directions.

TABLE I. I/O and Timer Address Designations

8-Bit Address Field Bits								Designation I/O Port, Timer, etc.	R (Read) W (Write)
7	6	5	4	3	2	1	0		
x	x	x	0	0	0	0	0	Port A (Data)	R/W
x	x	x	0	0	0	0	1	Port B (Data)	R/W
x	x	x	0	0	0	1	0	Port C (Data)	R/W
x	x	x	0	0	0	1	1	Not Used	**
x	x	x	0	0	1	0	0	DDR - Port A	W
x	x	x	0	0	1	0	1	DDR - Port B	W
x	x	x	0	0	1	1	0	DDR - Port C	W
x	x	x	0	0	1	1	1	Mode Definition Reg.	W
x	x	x	0	1	0	0	0	Port A - Bit-Clear	W
x	x	x	0	1	0	0	1	Port B - Bit-Clear	W
x	x	x	0	1	0	1	0	Port C - Bit-Clear	W
x	x	x	0	1	0	1	1	Not Used	**
x	x	x	0	1	1	0	0	Port A - Bit-Set	W
x	x	x	0	1	1	0	1	Port B - Bit-Set	W
x	x	x	0	1	1	1	0	Port C - Bit-Set	W
x	x	x	0	1	1	1	1	Not Used	**
x	x	x	1	0	0	0	0	Timer 0 (LB)	*
x	x	x	1	0	0	0	1	Timer 0 (HB)	*
x	x	x	1	0	0	1	0	Timer 1 (LB)	*
x	x	x	1	0	0	1	1	Timer 1 (HB)	*
x	x	x	1	0	1	0	0	STOP Timer 0	W
x	x	x	1	0	1	0	1	START Timer 0	W
x	x	x	1	0	1	1	0	STOP Timer 1	W
x	x	x	1	0	1	1	1	START Timer 1	W
x	x	x	1	1	0	0	0	Timer 0 Mode	R/W
x	x	x	1	1	0	0	1	Timer 1 Mode	R/W
x	x	x	1	1	0	1	0	Not Used	**
x	x	x	1	1	0	1	1	Not Used	**
x	x	x	1	1	1	0	0	Not Used	**
x	x	x	1	1	1	0	1	Not Used	**
x	x	x	1	1	1	1	0	Not Used	**
x	x	x	1	1	1	1	1	Not Used	**

x = don't care

LB = low-order byte

HB = high-order byte

* A write accesses the modulus register, a read the read buffer.

** A read from an unused location reads invalid data, a write does not affect any operation of NSC810A.

TABLE II. Mode Definition Register Bit Assignments

Mode	Bit							
	7	6	5	4	3	2	1	0
0	x	x	x	x	x	x	x	0
1	x	x	x	x	x	x	0	1
2	x	x	x	x	x	0	1	1
3	x	x	x	x	x	1	1	1

9.0 Functional Description (Continued)

Any write or read to the port bits contradicting the direction established by the DDR will not affect the port bits output or input. However, a write to a port bit, defined as an input, will modify the output latch and a read to a port bit, defined as an output, will read this output latch. See *Figure 2*.

• Data Registers

These registers contain the actual data being transferred between the CPU and the peripheral. In Basic I/O, data presented by the peripheral (read cycle) will be latched on the falling edge of $\overline{RD}$. Data presented by the CPU (write cycle) will be valid after the rising edge of $\overline{WR}$ (see AC characteristics for exact timing).

During Strobed I/O, data presented by the peripheral must be valid on the rising edge of $\overline{STB}$. Data received by the peripheral will be valid on the rising edge of $\overline{STB}$. Data latched by the port on the rising edge of $\overline{STB}$ will be preserved until the next CPU read or $\overline{STB}$ signal.

• Bit Set-Clear Registers

The I/O features of the RAM-I/O-timer allow modification of a single bit or several bits of a port with the Bit-Set and Bit-Clear commands. The address selected indicates whether a Bit-Set or Clear will take place. The incoming data on the address/data bus is latched at the trailing edge of the $\overline{WR}$ strobe and is treated as a mask. All bits containing 1s will cause the indicated operation to be performed on the corresponding port bit. All bits of the mask with 0s cause the corresponding port bits to remain unchanged. Three sample operations are shown in Table III using port B as an example.

TABLE III. Bit-Set and Clear Examples

Operation Port B	Set B7	Clear B2 and B0	Set B4, B3 and B1
Address	xxx01101	xxx01001	xxx01101
Data	10000000	00000101	00011010
Port Pins			
Prior State	00001111	10001111	10001010
Next State	10001111	10001010	10011010

9.3.2 Modes

Two data transfer modes are implemented: Basic I/O and Strobed I/O. Strobed I/O can be further subdivided into three categories: Strobed Input, Strobed Output (active peripheral bus) and Strobed Output (TRI-STATE peripheral bus). The following descriptions detail the functions of these categories.

• Basic I/O

Basic I/O mode uses the $\overline{RD}$ and $\overline{WR}$ CPU bus signals to latch data at the peripheral bus. This mode is the permanent mode of operation for ports B and C. Port A is in this mode if the MDR is set to mode 0. Read and write byte operations and bit operations can be done in Basic I/O. Timing for these modes is shown in the AC Characteristics Table and described with the data register definitions.

When the NSC810A is reset, all registers are cleared to zero. This results in the basic mode of operation being selected, all port bits are made inputs and the output latch for each port bit is cleared to zero. The NSC810A, at this point, can read data from any peripheral port without further set-up. If outputs are desired, the CPU merely has to program the appropriate DDR and then send data to the data ports.

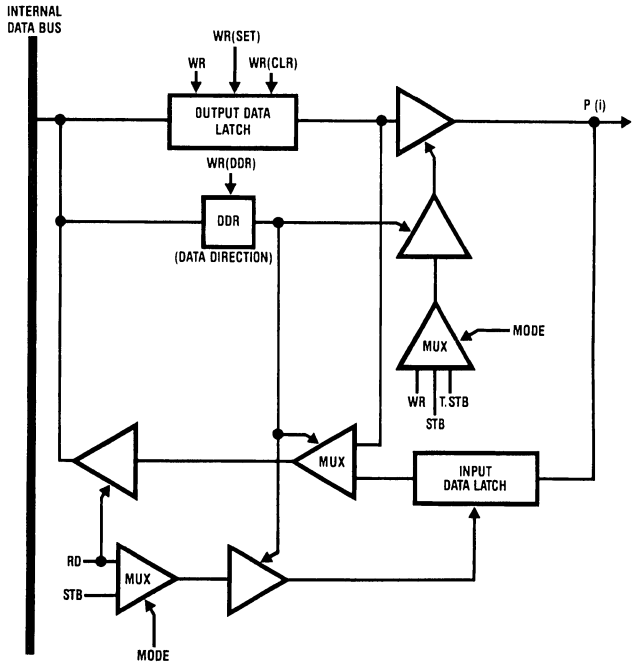

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FIGURE 2

9.0 Functional Description (Continued)

• Strobed I/O

Strobed I/O Mode uses the $\overline{STB}$, BF and $\overline{INTR}$ signals to latch the data and indicate that new data is available for transfer. Port A is used for the transfer of data when in any of the Strobed modes. Port B can still be used for Basic I/O and the lower 3-bits of port C are now the three handshake signals for Strobed I/O. Timing for this mode is shown in the AC Characteristic Tables.

Initializing the NSC810A for Strobed I/O Mode is done by loading the data shown in Table IV Into the specified register. The registers should be loaded in the order (left to right) that they appear in Table IV.

TABLE IV. Mode Definition Register Configurations

Mode	MDR	DDR Port A	DDR Port C	Port C Output Latch
Basic I/O	xxxxxxx0	Port bit directions are determined by the bits of each port's DDR		
Strobed Input	xxxxxx01	00000000	xxx011	xxx1xx
Strobed Output (Active)	xxxxx011	11111111	xxx011	xxx1xx
Strobed Output (TRI-STATE)	xxxxx111	11111111	xxx011	xxx1xx

• Strobed Input (Mode 1)

During strobed input operations, an external device can load data into port A with the $\overline{STB}$ signal. Data is input to the PA0–7 input latches on the leading (negative) edge of $\overline{STB}$, causing BF to go high (true). On the trailing (positive) edge of $\overline{STB}$ the data is latched and the interrupt signal, $\overline{INTR}$, becomes valid indicating to the CPU that new data is available. $\overline{INTR}$ becomes valid only if the interrupt is enabled, that is the output data latch for PC2 is set to 1.

When the CPU reads port A, address x'00, the trailing edge of the $\overline{RD}$ strobe causes BF and $\overline{INTR}$ to become inactive, indicating that the strobed input cycle has been completed.

• Strobed Output—Active (Mode 2)

During strobed output operations, an external device can read data from port A using the $\overline{STB}$ signal. Data is initially loaded into port A by the CPU writing to I/O address x'00. On the trailing edge of $\overline{WR}$, $\overline{INTR}$ is set inactive and BF becomes valid indicating new data is available for the external device. When the external device is ready to accept the data in port A it pulses the $\overline{STB}$ signal. The rising edge of $\overline{STB}$ resets BF and activates the $\overline{INTR}$ signal. $\overline{INTR}$ becomes valid only if the interrupt is enabled, that is the output latch for PC2 is set to 1. $\overline{INTR}$ in this mode indicates a condition that requires CPU intervention (the output of the next byte of data).

• Strobed Output—TRI-STATE (Mode 3)

The Strobed Output TRI-STATE Mode and the Strobed Output active (peripheral) bus mode function in a similar manner with one exception. The exception is that the data signals on PA0–7 assume the high impedance state at all times except when accessed by the $\overline{STB}$ signal. Strobed Mode 3 is identical to Strobed Mode 2, except as indicated above.

Example Mode 1 (Strobed Input):

Action Taken	$\overline{INTR}$	BF	Results of Action
INITIALIZATION			
Reset NSC810A	H	L	Basic input mode all ports.
Load 01'H into MDR	H	L	Strobed input mode entered; no byte loads to port C after this step; bit-set and clear commands to $\overline{INTR}$ and BF no longer work.
Load 00'H into DDR A	H	L	Sets data direction register for port A to input; data from port A peripheral bus is available to the CPU if the $\overline{STB}$ signal is used, other handshake signals aren't initialized, yet.
Load 03'H into DDR C	H	L	Sets data direction register of port C; buffer full signal works after this step and it is unaffected by the bit-set and clear registers.
Load 04'H into Port C Bit-Set Register	H	L	Sets output latch (PC2) to enable $\overline{INTR}$; $\overline{INTR}$ will latch active whenever $\overline{STB}$ goes low; $\overline{INTR}$ can be disabled by a bit-clear to PC2.*
OPERATION			
$\overline{STB}$ pulses low	L	H	Data on peripheral bus is latched into port A; $\overline{INTR}$ is cleared by a CPU read of port A or a bit-clear of $\overline{STB}$.
CPU reads Port A	H	L	CPU gets data from port A; $\overline{INTR}$ is cleared; peripheral is signalled to send next byte via an inactive BF signal. Repeat last two steps until EOT at which time CPU sends bit-clear to the output latch (PC2).

* Port C can be read by the CPU at anytime, allowing polled operation instead of interrupt driven operation.

9.0 Functional Description (Continued)

Example Mode 2 (Strobed Output—active peripheral bus):

Action Taken	$\overline{INTR}$	BF	Results of Action
INITIALIZE			
Reset NSC810A	H	L	basic input mode all ports.
Load 03'H into MDR	H	L	strobed output mode entered; no byte loads to port C after this step; bit-set and clear commands to $\overline{INTR}$ and BF no longer work.
Load FF'H into DDR A	H	L	Sets data direction register for port A to output; data from port A is available to the peripheral if the $\overline{STB}$ signal is used other handshake signals aren't initialized, yet.
Load 03'H into DDR C	H	L	Sets data direction register of port C; buffer full signal works after this step and it is unaffected by the bit-set and clear registers
Load 04'H into Port C Bit-Set Register	L	L	Sets output latch (PC2) to enable $\overline{INTR}$; active $\overline{INTR}$ indicates that CPU should send data; $\overline{INTR}$ becomes inactive whenever the CPU loads port A; $\overline{INTR}$ can be disabled by a bit-clear to $\overline{STB}$.*
OPERATION			
CPU writes to Port A	H	H	Data on CPU bus is latched into port A; $\overline{INTR}$ is set by the CPU write to port A; active
$\overline{STB}$ pulses low	L	L	BF indicates to peripheral that data is valid; Peripheral gets data from port A; $\overline{INTR}$ is reset active; The active $\overline{INTR}$ signals the CPU to send the next byte. Repeat last two steps until EOT at which time CPU sends bit-clear to the output latch (PC2).

*Port C can be read by the CPU at any time, allowing polled operation instead of interrupt driven operation.

In addition to its timing function, $\overline{STB}$ enables port A outputs to active logic levels. This Mode 3 operation allows other data sources, in addition to the NSC810A, to access the peripheral bus.

• Handshaking Signals

In the Strobed mode of operation, the lower 3-bits of port C transmit/receive the handshake signals (PC0 = $\overline{INTR}$, PC1 = BF, PC2 = $\overline{STB}$).

$\overline{INTR}$ (Strobe Mode Interrupt) is an active-low interrupt from the NSC810A to the CPU. In strobed input mode, the CPU reads the valid data at port A to clear the interrupt. In strobed output mode, the CPU clears the interrupt by writing data to port A.

The $\overline{INTR}$ output can be enabled or disabled, thus giving it the ability to control strobed data transfer. It is enabled or disabled, respectively, by setting or clearing bit 2 of the port C output data latch ($\overline{STB}$).

PC2 is always an input during strobed mode of operation, its output data latch is not needed. Therefore, during strobed mode of operation it is internally gated with the interrupt signal to generate the $\overline{INTR}$ output. Reset clears this bit to zero, so it must be set to one to enable the $\overline{INTR}$ pin for strobed operation.

Once the strobed mode of operation is programmed, the only way to change the output data latch of PC2 is by using the Bit-Set and Clear registers. The port C byte write command will not alter the output data latch of PC2 during the strobed mode of operation.

$\overline{STB}$ (Strobe) is an active low input from the peripheral device, signalling a data transfer. The NSC810A latches data on the rising edge of $\overline{STB}$ if the port bit is an input and the peripheral should latch data on the rising edge of $\overline{STB}$ if the port bit is an output.

BF (Buffer Full) is a high active output from the NSC810A. For input port bits, it indicates that new data has been received from the peripheral. For output port bits, it indicates that new data is available for the peripheral.

Note: In either input or output mode the BF may be cleared by rewriting the MDR.

9.4 TIMERS

The NSC810A has two timers. These are independently programmable, 16-bit binary down-counters. Full count is reached at n + 1, where n is the count loaded into the modulus registers. Timer outputs provide six distinct modes of operation and allow the CPU to check the present count at anytime. Each timer has an independent clock input and output. Start and stop words from the CPU can individually start and stop the timers in any of the modes. A common gate signal can start and stop both timers in three of the six modes. Timer 0 has three possible input clock prescalers ÷1, ÷2 and ÷64. Timer 1 has two possible input clock prescalers ÷1 and ÷2.

Primary components of one timer are shown in *Figure 3.* The timer mode register is a read/write register providing

9.0 Functional Description (Continued)

the primary characterization of the timer output. The start/stop logic and prescaler block divides the clock input by the prescale factor, passing the output (INTCLK) to the binary down-counter. This block also gates the clock input signal (TIN) with the timer gate signal (TG). The timer block loads the modulus from the modulus register and uses (INTCLK) to count to zero. It loads the current count into the read buffer block where the CPU can access it at anytime. This timer block also indicates to the output control logic when the modulus is loaded (or reloaded) and when the count reaches 0. The output control logic block drives the output pins according to the timer mode register and the timer block. The output of the timer block (*Figure 3*) (terminal count) is related to the input TIN by:

$$\text{terminal count} = \frac{\text{TIN}}{p[2(m+1)]}$$

where:

TIN = the input frequency

p = the programmed prescale

m = the modulus

This relationship can be seen directly (TOUT) in Mode 5 (square wave) as it is not masked by the subsequent output logic.

9.4.1 Registers

There are five control registers for each timer. These are shown in the second group of Table I. They determine all timer functions and outputs.

• Modulus Registers and Read Buffer

There are two modulus registers per timer (low byte, high byte). These are write only registers, and the two 8-bit values loaded by the CPU are combined into a 16-bit modulus for the timer's down counter.

When the CPU reads from the modulus register addresses, it actually accesses the read buffers. These contain the low and high byte of the decremented modulus. This count is constantly updated by the timer block on the falling edge of INTCLK and can be read without stopping the timers (see single/double precision).

• Timer Mode Register

The timer mode register determines the operating configuration and the active input and output signal levels. Each timer has its own timer mode register, allowing independent operation.

The timer mode register (TMR) may be written or read at any time; however, to assure accurate timing it is important to modify the mode only when the timer is stopped (see Timer Programming). The timer mode is selected from one of six modes by TMR bits 0, 1, and 2 (see Table V). Bits 3 and 4 select the prescale value if the prescaler is to be used. Bits 5, 6 and 7 select the modulus width (8- or 16-bits), gate input polarity, and timer output polarity (active-high or low), respectively. The bit functions of the TMR are illustrated in *Figure 4*.

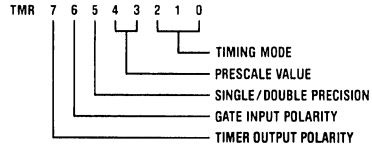

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FIGURE 4. Timer Mode Register

TABLE V. Mode Selection

Bit 2	1	0	–	Timer Function
0	0	0	–	Timer Stopped and Reset
0	0	1	–	Event Counter
0	1	0	–	Event Timer (Stopwatch)
0	1	1	–	Event Timer (Resetting)
1	0	0	–	One Shot
1	0	1	–	Square Wave
1	1	0	–	Pulse Generator
1	1	1	–	Timer Stopped and Reset

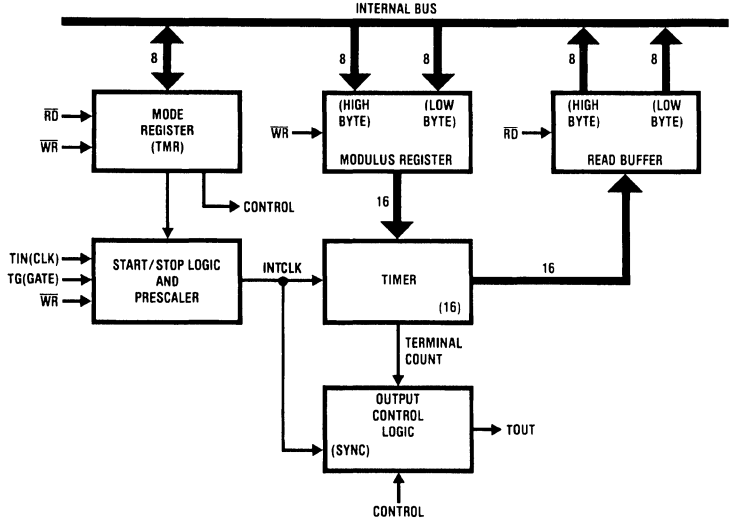

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FIGURE 3. Timer Internal Block Diagram (One of Two Timers)

9.0 Functional Description (Continued)

— Timer Prescaler

There is a prescale function associated with each timer. It serves as an additional divisor to lengthen the counts for each timer circuit. The value of the divisor is fixed and selectable in each TMR, as shown below.

	Bits		
TMR0	4	3	Prescale
	0	0	÷1
	0	1	÷2
	1	1	÷64

The ÷64 is not available on timer 1; TMR1 bit 4 is a "don't care."

	Bits		
TMR1	4	3	Prescale
	x	0	÷1
	x	1	÷2

The timer prescale divides the input clock (TIN) and provides the output (INTCLK) to the drive the timer block (*Figure 3*).

— Single/Double Precision

Bit 5 of the TMR determines whether a single or double byte can be accurately read from the read buffer. This option does not affect the use of the modulus registers by the timer block (i.e., the modulus used is always a double byte regardless of the precision mode selected).

The read buffer keeps track of the count and is constantly being updated by the timer block. In order to allow the CPU to read the read buffer, the NSC810A must discontinue updates to this buffer during the read. The precision bit determines whether one or two bytes in the read buffer will be frozen during the read process. In double precision mode, the NSC810A freezes high and low bytes in the read buffer for two consecutive read cycles. In the single precision mode, the NSC810A freezes the read buffer for only one read cycle. Read accesses should be done as follows.

When the TMR bit 5 is:

0— (double byte) read or write the low byte first, then the high byte to maintain proper read/write communications.

1— (single byte) In this mode either the high or low byte of the count can be read at any given instant but not both bytes consecutively. Always write the low byte first, then the high byte to load the modulus.

The following example illustrates this point. If the read buffer had a value of 0200 when the low byte was read and the down-counter decremented to 01FF before the high byte was read, then in the double precision mode the CPU would have read 00 and 02, respectively. In the single precision mode the CPU would have read 00 and 01.

NOTE: In the double precision mode, the high byte should be read immediately after the low byte. Do not access any other registers or unused address locations between the reads.

— Gate Input Polarity

In modes 2, 3 and 4, the TG input is the common hardware control for starting and stopping the timers.

The polarity of the gate input may be selected by the contents of bit 6 of the TMR. If bit 6 equals 0, the gate signal will be active-high or positive edge for mode 4; if bit 6 equals 1, the gate polarity will be active-low or negative edge for mode 4. Modes 2 and 3 are level sensitive. Mode 4 is edge sensitive.

— Timer Output Polarity

Like the gating function, the polarity of the output signal is programmable via bit 7 of the TMR. A zero will cause an active-low output; a one will generate an active-high output.

The output for T1 is multiplexed with port C, bit 5. (Similarly T1IN is multiplexed with port C, bit 4.) When any timer mode other than 0 or 7 is specified for T1, or when mode 2, mode 3, or mode 4 is specified for T0, the three port C pins, bit 3, bit 4, and bit 5, become TG, T1IN and T1OUT, respectively.

• Start and Stop Registers

This is the software start and stop for the timers. There is one start and one stop register for each timer. Writing any data to the start register of a timer starts that timer or transfers start and stop control to TG (in the gated modes 2, 3 and 4). Writing any data to the stop register stops the timer and removes start and stop control from TG (in the gated modes 2, 3 and 4). Restarting the timers causes the modulus to be reloaded for all gated timer modes (2, 3 and 4).

During software restarts of the timers (write to the STOP register and then to the START register) the modulus will be reloaded only if the internal clock signal (INTCLK) is in the high level or makes at least one transition to the high level between the time that the STOP and START registers are written. If INTCLK doesn't meet one of these criteria then the modulus will not be reloaded and the timer will continue to count down from where it was stopped.*

Since it is difficult, if not impossible, to know the level of INTCLK in non-gated modes the recommended practice for restart operation is to reload the modulus after stopping the timer using the 4 step programming procedure in the Timer Programming section of this datasheet. In gated modes INTCLK always stops high.

***NOTE:** INTCLK is coupled via the prescaler to TIN and reacts to the TIN clock input regardless of whether the timer is started or stopped.

— Start/Stop Timing

Figure 5 shows the relationships between the $\overline{WR}$ signal (start register), TIN and INTCLK for both the non-gated and gated modes. The TG signal is only sampled during the positive half of the TIN cycle. This means that when the gated modes are used the internal clock (INTCLK) is never stopped in the low state. Hence, when TG goes active high INTCLK is restarted on the next high-to-low transition of TIN. When TG goes inactive low INTCLK will stop as soon as TIN is high.

9.4.2 Timer Pins

TIN, TOUT, and TG

Timer 0 has dedicated pins for its clock, T0IN, and its output, T0OUT. Timer 1 must borrow its input and output pins from port C. This is accomplished by writing to the TMR for timer 1. If mode 1, 2, 3, 4, 5 or 6 is specified in TMR1, the pins from port C (PC3, PC4 and PC5) are automatically made available to the timer(s) for gating (TG), T1IN and T1OUT, respectively. These pins are also taken from port C any time timer 0 is in mode 2, 3, 4, so that it has a TG pin. In order to change pins PC3, PC4 and PC5 back to their original configuration as Basic I/O, the timer mode registers must be reset by selecting mode 0 or 7.

TG (PC3), the timer gate, is used for hardware control to start/stop (or trigger) the timers. The timer gate may be used individually by either timer or simultaneously by both timers.

For modes 2 and 3, the timer starts on the gate-active transition assuming the start address was previously written. If

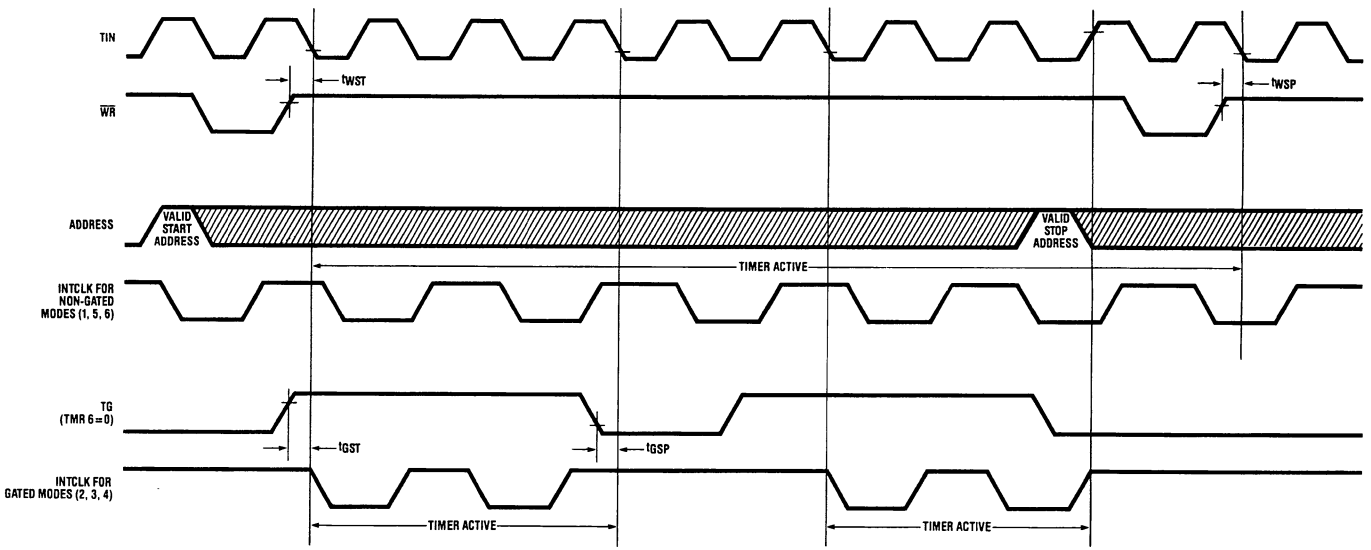

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FIGURE 5. Start/Stop Timing

Note: Diagonal lines indicate interval of invalid data.

For mode 4 (one shot), only start-timing applies.

t_{WST}—$\overline{WR}$ set-up for starting timer 150 ns.

t_{WSP}—$\overline{WR}$ set-up for stopping timer 150 ns.

t_{GST}—TG (gate) set-up for starting timer 100 ns.

t_{GSP}—TG (gate) set-up for stopping timer 100 ns.

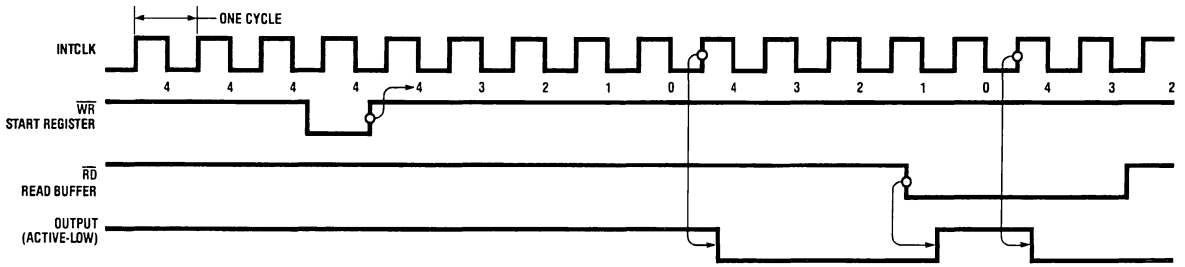

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FIGURE 6a. Event Counter Mode (Mode 1)

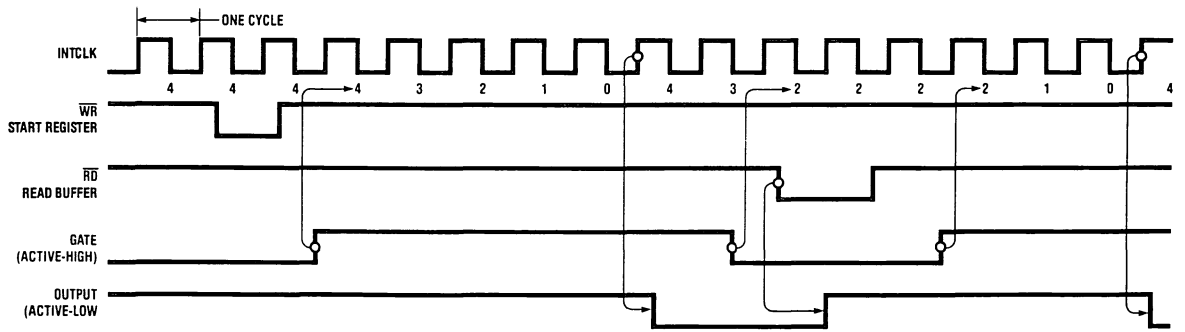

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FIGURE 6b. Accumulative Timer (Mode 2)

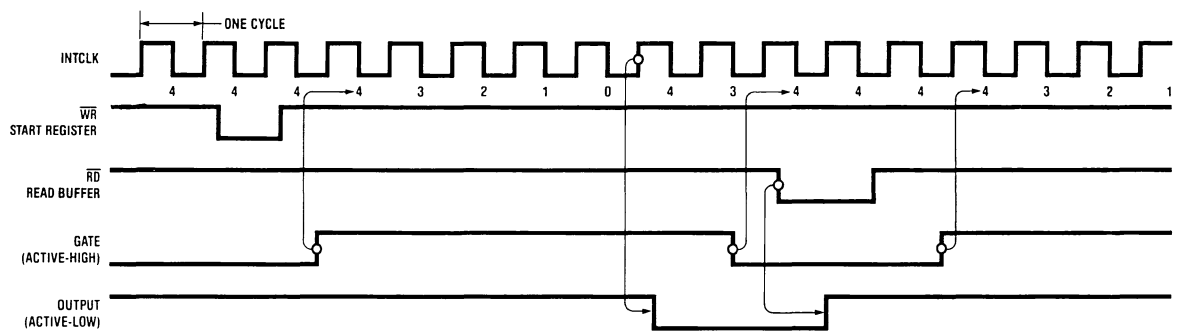

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FIGURE 6c. Restartable Timing

9.0 Functional Description (Continued)

TABLE VI. Timer Programming Selection Example

Mode Register Bit (TMR) 7	6	5	4	3	2	1	0	Timer Output Polarity Active L/H	Timer Gate Polarity Active L/H	Mode Description Single/Double Precision S/D	Prescale Value	Timing Mode	Port C DDR 543210
TIMER 0													
x	x	x	x	x	0	0	0	x	x	x	x	0	x x x x x x
0	x	0	0	0	0	0	1	L	x	D	÷1	1	x x x x x x
1	x	0	1	1	1	1	0	H	x	D	÷64	6	x x x x x x
1	0	0	0	1	1	0	0	H	H	D	÷2	4	1 0 0 x x x
0	1	1	0	0	0	1	0	L	L	S	÷1	2	1 0 0 x x x
TIMER 1													
x	x	x	x	x	1	1	1	x	x	x	x	7	x x x x x x
0	x	0	x	0	0	0	1	L	x	D	÷1	1	1 0 0 x x x
1	0	1	x	1	1	0	1	H	H	S	÷2	5	1 0 0 x x x
0	1	0	x	0	0	1	1	L	L	D	÷1	3	1 0 0 x x x

the timer gate makes an active transition prior to a write to the start register's address, the trailing edge of the $\overline{WR}$ strobe starts the timer. However, for mode 4 the timer always waits for an active gate edge following a write to the start address before it begins counting.

The DDR for port C must be programmed with the correct I/O direction for TG, T1IN and T1OUT of timer 1. See Table VI for programming examples.

9.4.3 Timer Modes

The low-order three bits (bits 0, 1, 2) of the timer mode registers (TMR) define the mode of operation for the timers. Each TMR may be written to, or read from, at any time. However, to ensure accurate timing, it is important to modify the mode of the timer only when the timer is stopped. Inputs of 000 or 111 define a NOP (no operation) mode. In either of these modes (0 or 7) the timer is stopped, INTCLK is high, and the output is inactive. Inputs of 001 through 110 will select one of six distinct timer functions.

In the explanations that follow, assume that the modulus register for the timer was loaded with the appropriate value (0004) by writing to the low and high bytes of each timer modulus register. Assume also, that the prescale is ÷1.

- **Event Counter (mode 1 TMR bits = 001)**

In this non-gated mode the count is decremented for each clock period (INTCLK) input to the timer block (see *Figure 6a*). When the count reaches zero, the output goes valid and remains valid, until the read buffer is read by the CPU or the timer stop register is written.

At the terminal count (0) the modulus is reloaded into the timer block and the count continues even when the output is valid. This mode can be used to cause periodic interrupts to the CPU.

- **Accumulative Timer (mode 2, TMR bits = 010)**

In this gated mode, the counter will decrement only when the gate input is active (see *Figure 6b*). If the gate becomes inactive, the counter will hold at its present value and continue to decrement when the gate again becomes active. When the count decrements to zero, the output becomes valid and remains valid until the count is read by the CPU or the timer is stopped.

At the terminal count the timer is reloaded and the count continues as long as the gate is active.

This mode can be used to time processor independent events and to interrupt the CPU when they occur. The prescale and modulus need to be longer than the expected event duration and the gate should go inactive at the event, to preserve the read buffer count for the CPU.

- **Restartable Timer (mode 3, TMR bits = 011)**

In this gated mode, the counter will decrement only when the gate input is active. If the gate becomes inactive, the counter will reload the modulus and hold this value until the gate again becomes active (see *Figure 6c*). If the timer is read when the gate is inactive, you will always read the value the timer has counted down to, not the value the timer has been reloaded with.

At terminal count the output becomes valid and the timer is reloaded. The timer will continue to run as normal, the only difference is the output is valid. The output remains valid until the count is read by the CPU or the timer stop register is written.

NOTE: The gate inactive time must be longer than the high time of the internal clock (INTCLK) on the chip. Therefore, with ÷64 prescale selected the gate inactive time must be 33 input clocks or greater.

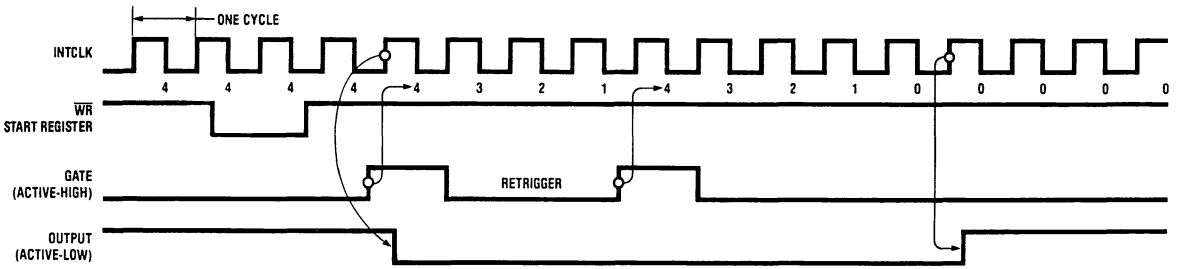

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FIGURE 6d. One Shot (Mode 4)

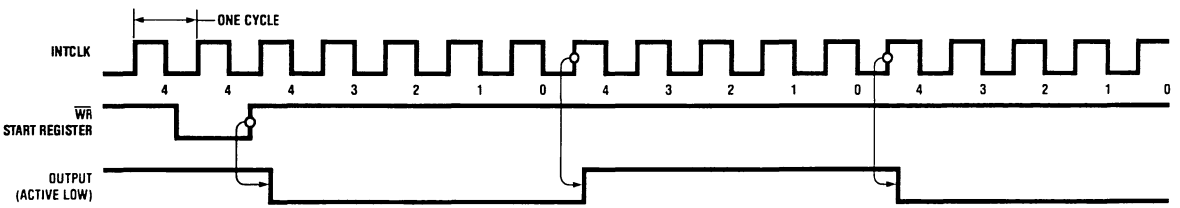

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FIGURE 6e. Square Wave (Mode 5)

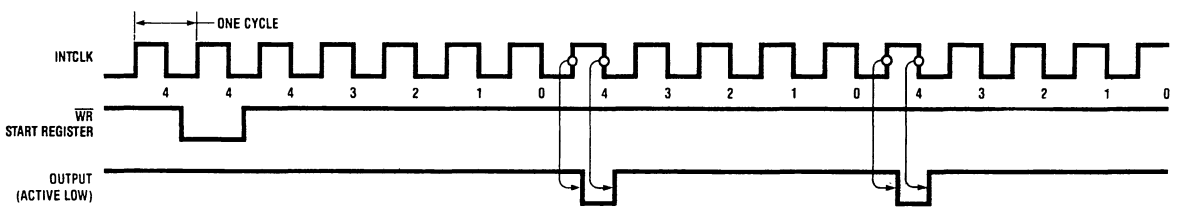

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FIGURE 6f. Pulse Generator (Mode 6)

9.0 Functional Description (Continued)

• One Shot Mode (mode 4, TMR bits = 100)

In this gated mode, the timer holds the modulus count until the active gate edge (see *Figure 6d*). The output immediately becomes valid and remains valid as the counter decrements. The gating signal may go inactive without affecting the count. If TG (the gate) becomes inactive and returns active prior to the terminal count, the modulus will be reloaded, retriggering the one shot period. When the timer reaches the terminal count, the output becomes inactive (see NOTE). The gate, in this mode, is edge sensitive; the active edge is defined by the TMR.

NOTE: The one shot cannot be retriggered during its last internal count (INTCLK) regardless of prescaler selected. Therefore, using the divide by 1 prescaler, it cannot be retriggered during the last clock (TIN), using the divide by 2 prescaler during the last two clocks (TIN) and using the divide by 64 prescaler during the last 64 clocks (TIN).

• Square Wave Mode (mode 5, TMR bits = 101)

In this non-gated mode, the output will go active as soon as the timer is started. The counter decrements for each clock period (INTCLK) and complements its output when zero is reached (see *Figure 6e*). The modulus is then reloaded and counting continues. Assuming a regular clock input, the output will then be a square wave with a period equal to twice the prescale value times the value loaded into the modulus +1 (see equation Timer section intro.). Therefore, varying the modulus will vary the period of the square wave.

• Pulse Generator (mode 6, TMR bits = 110)

In this non-gated mode, the counter decrements for each period of INTCLK (see *Figure 6f*). When the terminal count is reached the output becomes valid for ½ of the TIN clock width for a prescale of ÷1, for one full TIN clock width for a prescale of ÷2 and for 32 TIN clock widths for a prescale of ÷64. The modulus is then reloaded and the sequence is repeated. Varying the prescale and modulus varies the frequency of the pulse.

9.4.4 Timer Programming

The following is the proper sequence to program the timer and should always be used:

1. Write timer mode register selecting mode 0 or 7. This stops the timer, resets the prescaler, and sets internal clock high.
2. Write timer mode register again, this time loading it for your requirements.
3. Write the modulus values, low byte first, high byte second.
4. Start the timers.

The timer read buffer is only updated when the internal timer clock (INTCLK) makes a negative-going transition. Therefore, enough input clock cycles (TIN) must occur to cause a transition of INTCLK given the programmed pre-scaler. After the first transition, the new modulus will be loaded into the read buffer and it can then be read by the CPU.

To guarantee the integrity of the data during a read operation, updates to the timer read buffer are blocked out. If an update is blocked out due to a read, the read buffer will not be updated until the next active transition of INTCLK. Thus, it would appear as if a count was skipped between reads. For example, if the output latches were FF when a block out (read) occurred, the next update could occur at FD, thereby giving an appearance that the count FE was skipped. In actuality the correct number of clocks has occurred for the read buffer to hold FD.

Writing the modulus value when the timer is running does not update the timer immediately. The new value written will get into the timer when the timer reaches its terminal count and reloads its value. If the timer is stopped and a modulus is written the new modulus value will get into the timer when the internal clock is high during the modulus write or on the next low to high internal clock transition. The next time the timer reaches its terminal count it will load the new modulus into the timer. One way to guarantee the new modulus will get into the timer is to follow steps 1 through 4. Although this procedure guarantees that the data will get into the timer you will not be able to read it back until you get a negative-going transition on the internal clock.

Rewriting modulus does not reset the prescaler. The only way to reset the prescaler is to write the mode register and have the internal clock signal be high for some period between the write of the mode register and the start of the timer. Once again, steps 1 through 4 will reset the prescaler.

10.0 NSC810A/883 MIL-STD-883 Class B Screening

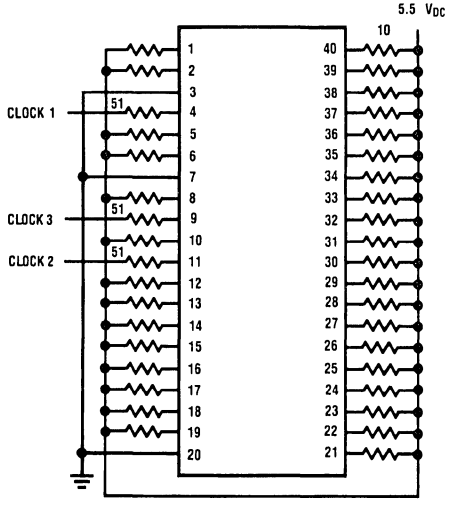
National Semiconductor offers the NSC810AD and NSC810AE with full class B screening per MIL-STD-883 for Military/Aerospace programs requiring high reliability. In addition, this screening is available for all of the key NSC800 peripheral devices.

Electrical testing is performed in accordance with RETS810AX, which tests or guarantees all of the electrical performance characteristics of the NSC810A data sheet. A copy of the current revision of RETS810AX is available upon request. The following table is the MIL-STD-883 flow as of the date of publication.

Test	MIL-STD-883 Method/Condition	Requirement
Internal Visual	2010 B	100%
Stabilization Bake	1008 C 24 Hrs. @ +150°C	100%
Temperature Cycling	1010 C 10 Cycles −65°C/ +150°C	100%
Constant Acceleration	2001 E 30,000 G's, Y1 Axis	100%
Fine Leak	1014 A or B	100%
Gross Leak	1014 C	100%
Burn-In	1015 160 Hrs. @ +125°C (using burn-in circuits shown below)	100%
Final Electrical	+25°C DC per RETS810AX	100%
PDA	5% Max	
	+125°C AC and DC per RETS810AX	100%
	−55°C AC and DC per RETS810AX	100%
	+25°C AC per RETS810AX	100%
QA Acceptance	5005	Sample per
Quality Conformance	5056	Method 5005
External Visual	2009	100%

11.0 Burn-In Circuit

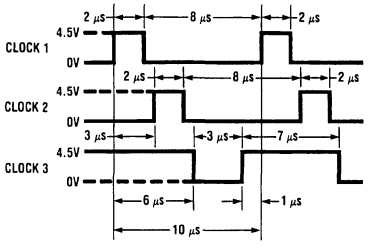
5242HR
NSC810AD/883B (Dual-In-Line)



TL/C/5517–23

12.0 Timing Diagram

Input Clocks



TL/C/5517–24

Note 1: All resistors ±5%, ¼ watt unless otherwise designated, 125°C operating life circuit.

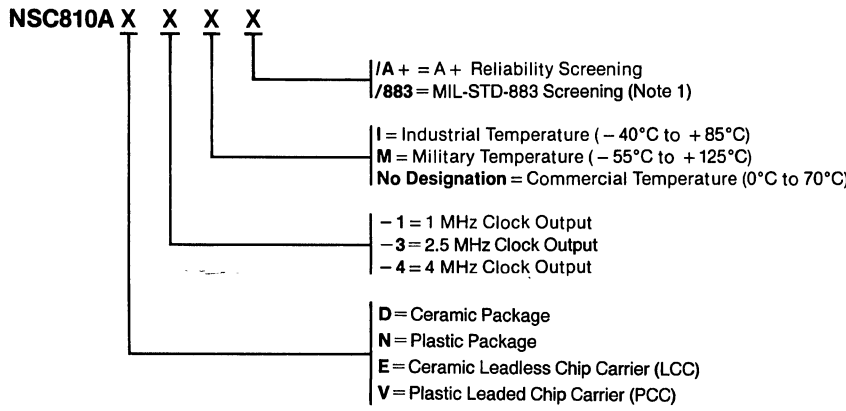
Note 2: E package burn-in circuit 5244HR is functionally identical to the D package.

Note 3: All resistors 2.7 kΩ unless marked otherwise.

Note 4: All clocks 0V to 4.5V.

Note 5: Device to be cooled down under power after burn-in.

13.0 Ordering Information



TL/C/5517–25

Note 1: Do not specify a temperature option; all parts are screened to military temperature.

14.0 Reliability Information

Gate Count	4000
Transistor Count	14,000

National Semiconductor

microCMOS

NSC831 Parallel I/O

General Description

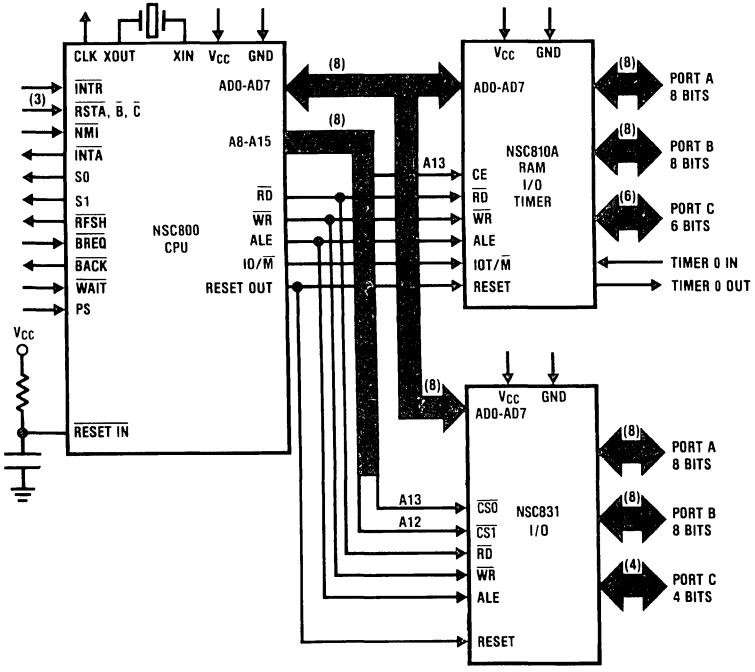
The NSC831 is an I/O device which is fabricated using microCMOS silicon gate technology, functioning as an input/output peripheral interface device. It consists of 20 programmable input/output bits arranged as three separate ports, with each bit individually definable as an input or output. The port bits can be set or cleared individually and can be written to or read from in bytes. Several types of strobed mode operations are available through Port A.

For military applications the NSC831 is available with class B screening in accordance with methods 5004 of MIL-STD-883.

Features

- Three programmable I/O ports
- Single 5V Power Supply
- Very low power consumption
- Fully static operation
- Single-instruction I/O bit operations
- Directly compatible with NSC800 family
- Strobed modes available on Port A

Microcomputer Family Block Diagram



TL/C/5594–1

Table of Contents

1.0 Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Storage Temperature Range	−65°C to +150°C
Voltage at Any Pin With Respect to Ground	−0.3V to V_{CC} + 0.3V
V_{CC}	7V
Lead Temp. (Soldering, 10 seconds)	300°C
Power Dissipation	1W

Note: *Absolute maximum ratings are those values beyond which the safety of the device cannot be guaranteed. Continuous operation at these limits is not intended; operation should be limited to those conditions specified under DC Electrical Characteristics.*

2.0 Operating Range V_{CC} = 5V ±10%

NSC831-1: 0°C to +70°C
−40°C to +85°C

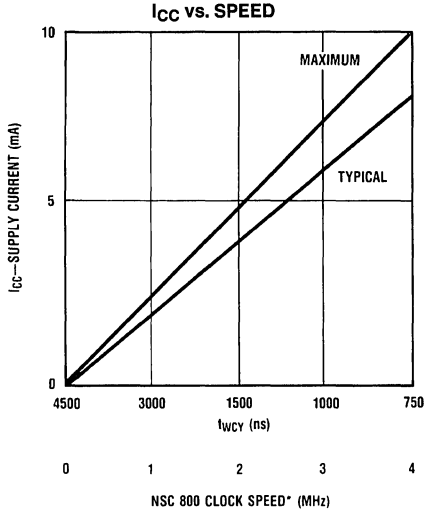
NSC831-3: −40°C to +85°C
−55°C to +125°C

NSC831-4: 0°C to +70°C
−40°C to +85°C
−55°C to +125°C

3.0 DC Electrical Characteristics V_{CC} = 5V ±10%, GND = 0V, unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{IH}	Logical 1 Input Voltage		0.8 V_{CC}		V_{CC}	V
V_{IL}	Logical 0 Input Voltage		0		0.2 V_{CC}	V
V_{OH}	Logical 1 Output Voltage	I_{OH} = −1.0 mA	2.4			V
		I_{OUT} = −10 μA	4.0V			V
V_{OL}	Logical 0 Output Voltage	I_{OL} = 2 mA	0		0.4	V
		I_{OUT} = 10 μA	0		0.1	V
I_{iL}	Input Leakage Current	0 ≤ V_{IN} ≤ V_{CC}	−10.0		10.0	μA
I_{OL}	Output Leakage Current	0 ≤ V_{IN} ≤ V_{CC}	−10.0		10.0	μA
I_{CC}	Active Supply Current	I_{OUT} = 0, t_{WCY} = 750 ns		15	20	mA
I_Q	Quiescent Current	RESET = 0, $\overline{RD}$ = 1, WR = 1, ALE = X, V_{IN} = 0, or V_{IN} = V_{CC} No Input Switching, T_A = 25°C		10	100	μA
C_{IN}	Input Capacitance			4	7	pF
C_{OUT}	Output Capacitance			6	10	pF
V_{CC}	Power Supply Voltage	(Note 1)	2.4	5	6	V

Note 1: Operation at lower power supply voltages will reduce the maximum operating speed. Operation at voltages other than 5V ±10% is guaranteed by design, not tested.



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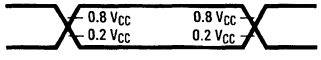
*When NSC831 is used with NSC800

4.0 AC Electrical Characteristics V_{CC} = 5V ±10%, GND = 0V

Symbol	Parameter	Test Conditions	NSC831-1		NSC831-3		NSC831-4		Units
			Min	Max	Min	Max	Min	Max	
t_{ACC}	Access Time from ALE	C_L = 150 pF		1000		400		250	ns
t_{AH}	AD0–AD7, CE, IO/$\overline{M}$ Hold Time		100		60		30		ns
t_{ALE}	ALE Strobe Width (High)		200		130		75		ns
t_{ARW}	ALE to $\overline{RD}$ or $\overline{WR}$ Strobe		150		120		75		ns
t_{AS}	AD0–AD7, CE, IO/$\overline{M}$ Setup Time		100		45		40		ns
t_{DH}	Data Hold Time		150		90		40		ns
t_{DO}	Port Data Output Valid			350		320		300	ns
t_{DS}	Data Setup Time		100		80		50		ns
t_{PE}	Peripheral Bus Enable			320		200		200	ns
t_{PH}	Peripheral Data Hold Time		150		125		100		ns
t_{PS}	Peripheral Data Setup Time		100		75		50		ns
t_{PZ}	Peripheral Bus Disable (TRI-STATE®)			150		150		150	ns
t_{RB}	$\overline{RD}$ to BF Output			300		300		300	ns
t_{RD}	Read Strobe Width		400		320		220		ns
t_{RDD}	Data Bus Disable		0	100	0	75	0	75	ns
t_{RI}	$\overline{RD}$ to $\overline{INTR}$ Output			320		300		300	ns
t_{RWA}	$\overline{RD}$ or $\overline{WR}$ to Next ALE		125		100		45		ns
t_{SB}	$\overline{STB}$ to BF Valid			300		300		300	ns
t_{SH}	Peripheral Data Hold With Respect to $\overline{STB}$		150		125		100		ns
t_{SI}	$\overline{STB}$ to INTR Output			300		300		300	ns
t_{SS}	Peripheral Data Setup With Respect to $\overline{STB}$		100		75		50		ns
t_{SW}	$\overline{STB}$ Width		400		320		220		ns
t_{WB}	$\overline{WR}$ to BF Output			340		300		300	ns
t_{WI}	$\overline{WR}$ to $\overline{INTR}$ Output			320		300		300	ns
t_{WR}	$\overline{WR}$ Strobe Width		400		320		220		ns
t_{WCY}	Width of Machine Cycle		3000		1200		750		ns

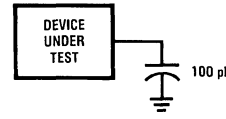
Note: Test conditions: t_{WCY} = 3000 ns for NSC831-1, 1200 ns for NSC831-3, 750 ns for NSC831-4

AC TESTING INPUT/OUTPUT WAVEFORM



TL/C/5594–3

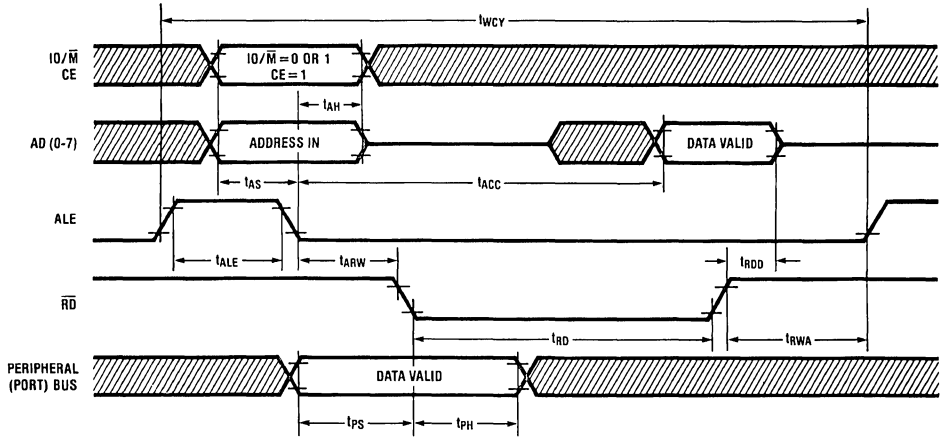
AC TESTING LOAD CIRCUIT



TL/C/5594–4

5.0 Timing Waveforms

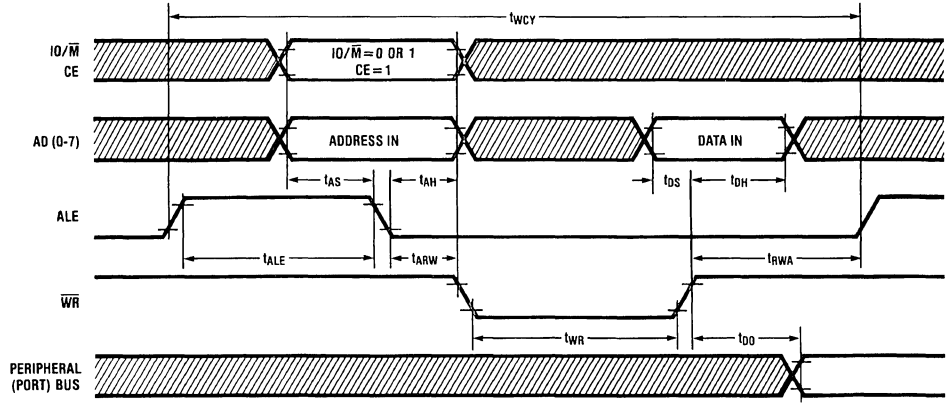
Read Cycle (Read from Port)



TL/C/5594–5

Note: Diagonal lines indicate interval of invalid data.

Write Cycle (Write to Port)

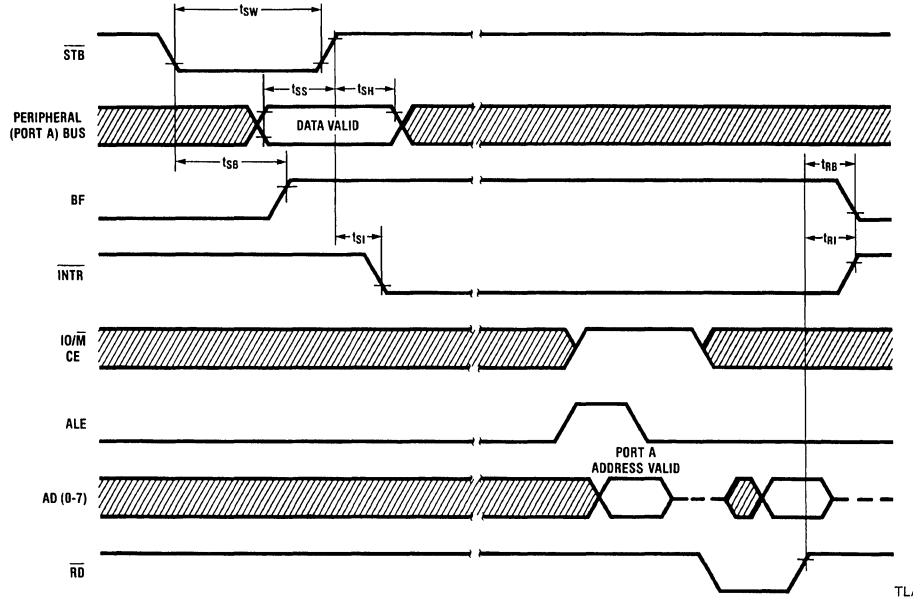


TL/C/5594–6

Note: Diagonal lines indicate interval of invalid data.

5.0 Timing Waveforms (Continued)

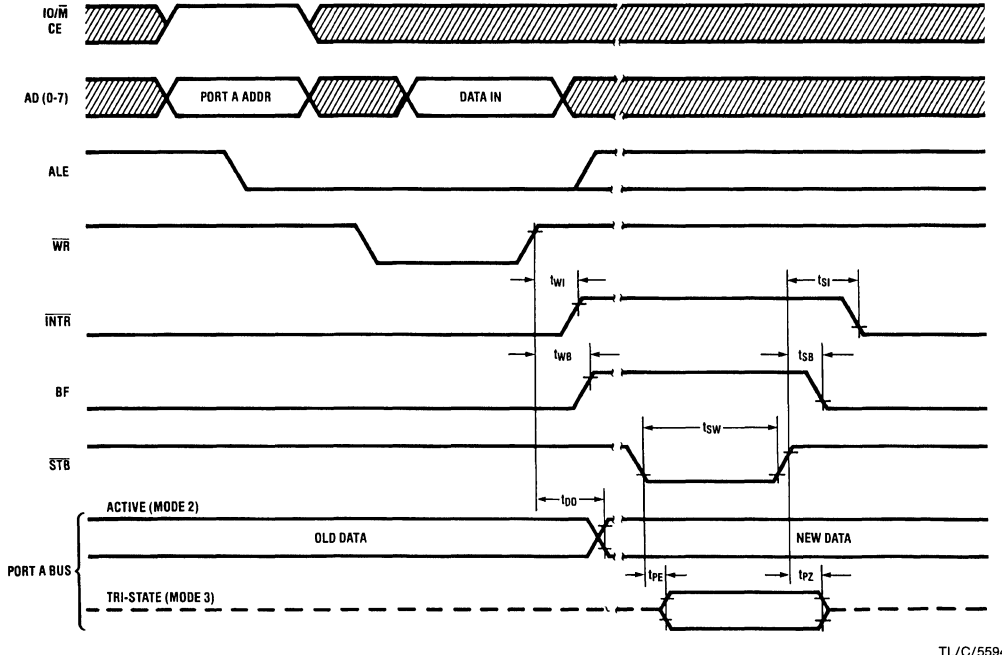
Strobed Mode Input



TL/C/5594–7

Note: Diagonal lines indicate interval of invalid data.

Strobed Mode Output



TL/C/5594–8

Note: Diagonal lines indicate interval of invalid data.

6.0 Pin Descriptions

The following describes the function of all NSC831 input/output pins. Some of these descriptions reference internal circuits.

6.1 INPUT SIGNALS

Master Reset (RESET): An active-high input on the RESET pin initializes the chip causing the three I/O ports (A, B and C) to revert to the input mode. The three ports, the three data direction registers and the mode definition register are reset to low (0).

Chip Enable ($\overline{CE_0}$, $\overline{CE_1}$): The CE inputs must be active at the falling edge of ALE. At ALE time, the CE inputs are latched to provide access to the NSC831.

Read ($\overline{RD}$): when the $\overline{RD}$ input is an active low, data is read from the AD0–AD7 bus.

Write ($\overline{WR}$): When the CE inputs are active an active low $\overline{WR}$ input causes the selected output port to be written with the data from the AD0–AD7 bus.

Address Latch Enable (ALE): The trailing edge (high to low transition) of the ALE input signal latches the address/data present on the AD0–AD7 bus, plus the input control signals on $\overline{CE_0}$ and $\overline{CE_1}$.

Power (V_{CC}): 5V power supply.

Ground (V_{SS}): Ground reference.

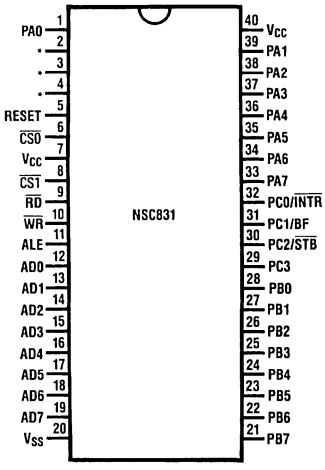
6.2 INPUT/OUTPUT SIGNALS

Bidirectional Address/Data Bus AD0–AD7: The lower 8 bits of the I/O address are applied to these pins, and latched by the trailing edge of ALE. During read operations, 8 bits are present on these pins, and are read when $\overline{RD}$ is low. During an I/O write cycle, Port A, B, or C is written with the data present on this bus at the trailing edge of the $\overline{WR}$ strobe.

Ports A, B, C (PA0–PA7, PB0–PB7, PC0–PC3): These are general purpose I/O pins. Their input/output direction is determined by the contents of the Data Direction Register (DDRs).

7.0 Connection Diagrams

Dual-In-Line Package



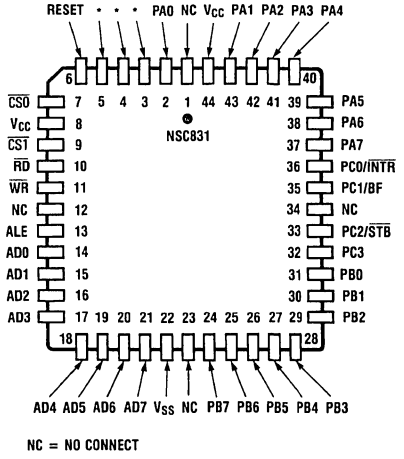
TL/C/5594–9

Top View

*Tie pins 2, 3, and 4 to either V_{CC} or V_{SS}.

Order Number NSC831D or N
See NS Package Number D40C or N40A

Leadless Chip Carrier



NC = NO CONNECT

TL/C/5594–10

Top View

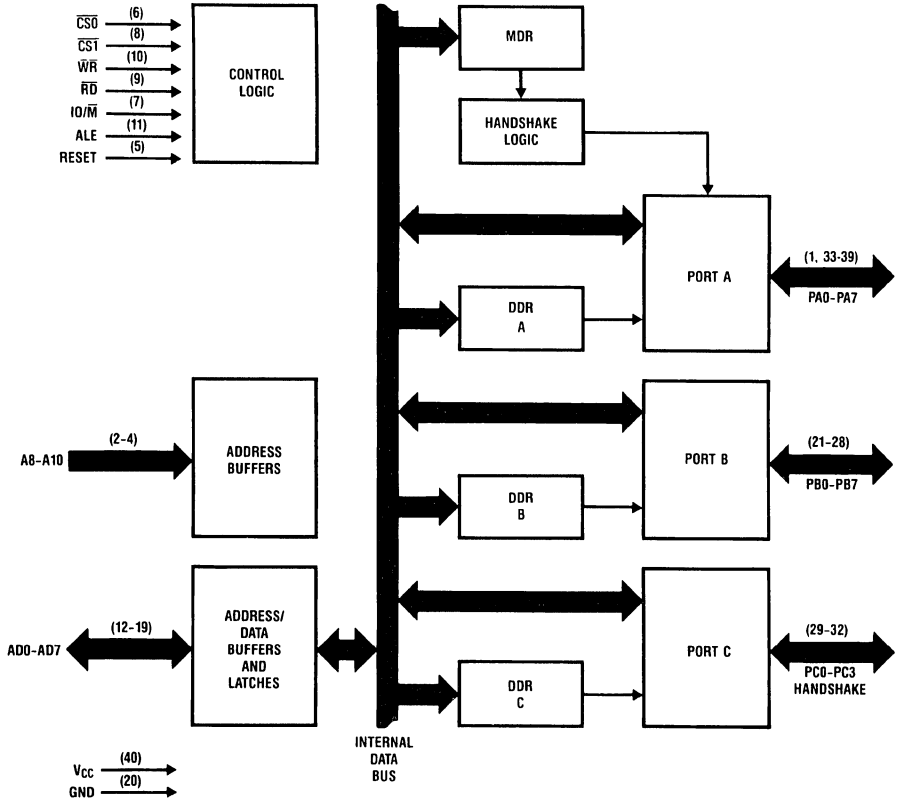
Order Number NSC831E
See NS Package Number E44A

8.0 Functional Description

Refer to *Figure 1* for a detailed block diagram of the NSC831, while reading the following paragraphs.

Input/Output (I/O): The I/O of the NSC831 contains three sets called Ports. There are two ports (A and B) which contain 8 bits each and one port (Port C) which has 4 bits. Any bit or combination of bits in a port may be addressed with Set or Clear commands. A port can also be addressed as an 8-bit word (4 bits for Port C). When reading Port C, bits 4–7 will be read as ones. All ports share common functions of Read, Write, Bit-Set and Bit-Clear. Additionally, Port A is programmable for strobed (handshake mode input or output. Port C has a programmable second function for each bit associated with strobed modes. Table I defines the address location of the ports and control registers.

8.1 BLOCK DIAGRAM



TL/C/5594–11

Note: Applicable pinout for 40 pin dual-in-line package within parentheses.

FIGURE 1

8.0 Functional Description (Continued)

8.2 I/O PORTS

There are three I/O ports (labeled A, B and C) on the NSC831. Ports A and B are 8-bits wide; port C is 4-bits wide. These ports transfer data between the CPU bus and the peripheral bus and vice versa. The way in which these transfers are handled depends upon the currently programmed operating mode.

The NSC831 can be programmed to operate in four different modes. One of these modes (Basic I/O) allows direct transfer of I/O data without any handshaking between the NSC831 and the peripheral. The other three modes (Strobed I/O) provide for timed transfers of I/O data with handshaking between the NSC831 and the peripheral.

Determination of the NSC831 port's mode, data direction and data is done by five registers which are under program control. The Mode Definition Register determines in which of the four I/O modes the chip will operate. Another register (Data Direction Register) establishes the data direction for each bit in that port. The Data Register holds data to be transferred or that which was received. The final two registers per port allow individual data register bits to be cleared (Bit-Clear Register) or data register bits to be set (Bit-Set Register).

Operation during Strobed I/O utilizes two of the port C pins for handshaking and one port C pin to interrupt the CPU.

8.3 REGISTERS

As indicated in the overview, programmable registers control the flow of data through the ports. Table I shows the registers of the NSC831. All registers affecting I/O transfers are in the first grouping of this table.

• Mode Definition Register (MDR)

The MDR determines the operating mode for port A and whether or not the lower 3-bits of port C will be used for handshaking (Strobed I/O). Port B always transfers data via the Basic I/O mode, regardless of how the MDR is programmed.

The four modes are as follows:

Mode 0—Basic I/O (Input or Output)

Mode 1—Strobed Mode Input

Mode 2—Strobed Mode Output (Active Peripheral Bus)

Mode 3—Strobed Mode Output (TRI-STATE Peripheral Bus)

The address assignment of the MDR is xxx00111 as shown in Table I. The upper 3 "don't care" bits are determined by the users decode logic (chip enable address). Table II specifies the data that must be loaded into the MDR to select the mode.

• Data Direction Registers (DDR)

Each port has a DDR that determines whether an individual port bit will be an input or an output. If DDR for the port bit is set to a 1, then that port bit is an output. If its DDR is reset to a 0, then it is an input. The DDR bits cannot be individually written to; the entire DDR register is affected by a write to the DDR. Thus, all data bits written must be consistent for all desired port bit directions.

TABLE I. I/O and Timer Address Designations

8-Bit Address Field Bits								Designation I/O Port, Timer, etc.	R (Read) W (Write)
7	6	5	4	3	2	1	0		
x	x	x	x	0	0	0	0	Port A (Data)	R/W
x	x	x	x	0	0	0	1	Port B (Data)	R/W
x	x	x	x	0	0	1	0	Port C (Data)	R/W
x	x	x	x	0	0	1	1	Not Used	**
x	x	x	x	0	1	0	0	DDR - Port A	W
x	x	x	x	0	1	0	1	DDR - Port B	W
x	x	x	x	0	1	1	0	DDR - Port C	W
x	x	x	x	0	1	1	1	Mode Definition Reg.	W
x	x	x	x	1	0	0	0	Port A - Bit-Clear	W
x	x	x	x	1	0	0	1	Port B - Bit-Clear	W
x	x	x	x	1	0	1	0	Port C - Bit-Clear	W
x	x	x	x	1	0	1	1	Not Used	**
x	x	x	x	1	1	0	0	Port A - Bit-Set	W
x	x	x	x	1	1	0	1	Port B - Bit-Set	W
x	x	x	x	1	1	1	0	Port C - Bit-Set	W
x	x	x	x	1	1	1	1	Not Used	**

x = don't care

LB = low-order byte

HB = high-order byte

* A write accesses the modulus register, a read the read buffer.

** A read from an unused location reads invalid data, a write does not affect any operation of NSC831.

TABLE II. Mode Definition Register Bit Assignments

Mode	Bit							
	7	6	5	4	3	2	1	0
0	x	x	x	x	x	x	x	0
1	x	x	x	x	x	x	0	1
2	x	x	x	x	x	0	1	1
3	x	x	x	x	x	1	1	1

8.0 Functional Description (Continued)

Any write or read to the port bits contradicting the direction established by the DDR will not affect the port bits output or input. However, a write to a port bit, defined as an input, will modify the output latch and a read to a port bit, defined as an output, will read this output latch. See *Figure 2*.

• Data Registers

These registers contain the actual data being transferred between the CPU and the peripheral. In Basic I/O, data presented by the peripheral (read cycle) will be latched on the falling edge of $\overline{RD}$. Data presented by the CPU (write cycle) will be valid after the rising edge of $\overline{WR}$ (see AC characteristics for exact timing).

During Strobed I/O, data presented by the peripheral must be valid on the rising edge of $\overline{STB}$. Data received by the peripheral will be valid on the rising edge of $\overline{STB}$. Data latched by the port on the rising edge of $\overline{STB}$ will be preserved until the next CPU read or $\overline{STB}$ signal.

• Bit Set-Clear Registers

The I/O features of the RAM-I/O-timer allow modification of a single bit or several bits of a port with the Bit-Set and Bit-Clear commands. The address selected indicates whether a Bit-Set or Clear will take place. The incoming data on the address/data bus is latched at the trailing edge of the $\overline{WR}$ strobe and is treated as a mask. All bits containing 1s will cause the indicated operation to be performed on the corresponding port bit. All bits of the mask with 0s cause the corresponding port bits to remain unchanged. Three sample operations are shown in Table III using port B as an example.

TABLE III. Bit-Set and Clear Examples

Operation Port B	Set B7	Clear B2 and B0	Set B4, B3 and B1
Address	xxx01101	xxx01001	xxx01101
Data	10000000	00000101	00011010
Port Pins			
Prior State	00001111	10001111	10001010
Next State	10001111	10001010	10011010

8.4 MODES

Two data transfer modes are implemented: Basic I/O and Strobed I/O. Strobed I/O can be further subdivided into three categories: Strobed Input, Strobed Output (active peripheral bus) and Strobed Output (TRI-STATE peripheral bus). The following descriptions detail the functions of these categories.

• Basic I/O

Basic I/O mode uses the $\overline{RD}$ and $\overline{WR}$ CPU bus signals to latch data at the peripheral bus. This mode is the permanent mode of operation for ports B and C. Port A is in this mode if the MDR is set to mode 0. Read and write byte operations and bit operations can be done in Basic I/O. Timing for these modes is shown in the AC Characteristics Table and described with the data register definitions.

When the NSC831 is reset, all registers are cleared to zero. This results in the basic mode of operation being selected, all port bits are made inputs and the output latch for each port bit is cleared to zero. The NSC831, at this point, can read data from any peripheral port without further set-up. If outputs are desired, the CPU merely has to program the appropriate DDR and then send data to the data ports.

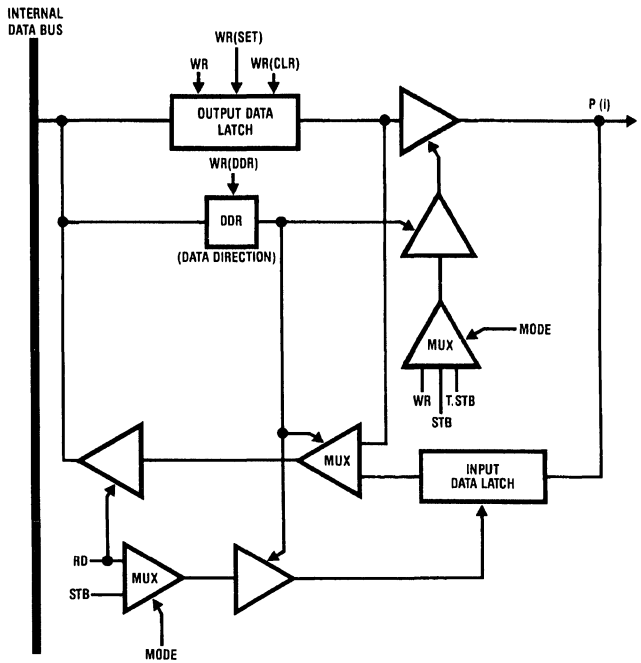


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FIGURE 2

8.0 Functional Description (Continued)

• Strobed I/O

Strobed I/O Mode uses the $\overline{STB}$, BF and $\overline{INTR}$ signals to latch the data and indicate that new data is available for transfer. Port A is used for the transfer of data when in any of the Strobed modes. Port B can still be used for Basic I/O and the lower 3-bits of port C are now the three handshake signals for Strobed I/O. Timing for this mode is shown in the AC Characteristic Tables.

Initializing the NSC831 for Strobed I/O Mode is done by loading the data shown in Table IV into the specified register. The registers should be loaded in the order (left to right) that they appear in Table IV.

TABLE IV. Mode Definition Register Configurations

Mode	MDR	DDR Port A	DDR Port C	Port C Output Latch
Basic I/O	xxxxxxx0	Port bit directions are determined by the bits of each port's DDR		
Strobed Input	xxxxxx01	00000000	xxx011	xxx1xx
Strobed Output (Active)	xxxxx011	11111111	xxx011	xxx1xx
Strobed Output (TRI-STATE)	xxxxx111	11111111	xxx011	xxx1xx

• Strobed Input (Mode 1)

During strobed input operations, an external device can load data into port A with the $\overline{STB}$ signal. Data is input to the PA0–7 input latches on the leading (negative) edge of $\overline{STB}$, causing BF to go high (true). On the trailing (positive) edge of $\overline{STB}$ the data is latched and the interrupt signal, $\overline{INTR}$, becomes valid indicating to the CPU that new data is available. $\overline{INTR}$ becomes valid only if the interrupt is enabled, that is the output data latch for PC2 is set to 1.

When the CPU reads port A, address x'00, the trailing edge of the $\overline{RD}$ strobe causes BF and $\overline{INTR}$ to become inactive, indicating that the strobed input cycle has been completed.

• Strobed Output—Active (Mode 2)

During strobed output operations, an external device can read data from port A using the $\overline{STB}$ signal. Data is initially loaded into port A by the CPU writing to I/O address x'00. On the trailing edge of $\overline{WR}$, $\overline{INTR}$ is set inactive and BF becomes valid indicating new data is available for the external device. When the external device is ready to accept the data in port A it pulses the $\overline{STB}$ signal. The rising edge of $\overline{STB}$ resets BF and activates the $\overline{INTR}$ signal. $\overline{INTR}$ becomes valid only if the interrupt is enabled, that is the output latch for PC2 is set to 1. $\overline{INTR}$ in this mode indicates a condition that requires CPU intervention (the output of the next byte of data).

• Strobed Output—TRI-STATE (Mode 3)

The Strobed Output TRI-STATE Mode and the Strobed Output active (peripheral) bus mode function in a similar manner with one exception. The exception is that the data signals on PA0–7 assume the high impedance state at all times except when accessed by the $\overline{STB}$ signal. Thus, in addition to its timing function, $\overline{STB}$ enables port A outputs to active logic levels. This Mode 3 operation allows other data sources, in addition to the NSC831, to access the peripheral bus. Strobed Mode 3 is identical to Strobed Mode 2, except as indicated above.

Example Mode 1 (Strobed Input):

Action Taken	$\overline{INTR}$	BF	Results of Action
INITIALIZATION			
Reset NSC831	H	L	Basic input mode all ports.
Load 01'H into MDR	H	L	Strobed input mode entered; no byte loads to port C after this step; bit-set and clear commands to $\overline{INTR}$ and BF no longer work.
Load 00'H into DDR A	H	L	Sets data direction register for port A to input; data from port A peripheral bus is available to the CPU if the $\overline{STB}$ signal is used, other handshake signals aren't initialized, yet.
Load 03'H into DDR C	H	L	Sets data direction register of port C; buffer full signal works after this step and it is unaffected by the bit-set and clear registers.
Load 04'H into Port C Bit-Set Register	H	L	Sets output latch (PC2) to enable $\overline{INTR}$; $\overline{INTR}$ will latch active whenever $\overline{STB}$ goes low; $\overline{INTR}$ can be disabled by a bit-clear to PC2.*
OPERATION			
$\overline{STB}$ pulses low	L	H	Data on peripheral bus is latched into port A; $\overline{INTR}$ is cleared by a CPU read of port A or a bit-clear of $\overline{STB}$.
CPU reads Port A	H	L	CPU gets data from port A; $\overline{INTR}$ is cleared; peripheral is signalled to send next byte via an inactive BF signal. Repeat last two steps until EOT at which time CPU sends bit-clear to the output latch (PC2).

*Port C can be read by the CPU at anytime, allowing polled operation instead of interrupt driven operation.

8.0 Functional Description (Continued)

Example Mode 2 (Strobed Output—active peripheral bus):

Action Taken	$\overline{INTR}$	BF	Results of Action
INITIALIZE			
Reset NSC831	H	L	Basic input mode all ports.
Load 03'H into MDR	H	L	Strobed output mode entered; no byte loads to port C after this step; bit-set and clear commands to $\overline{INTR}$ and BF no longer work.
Load FF'H into DDR A	H	L	Sets data direction register for port A to output; data from port A is available to the peripheral if the $\overline{STB}$ signal is used other handshake signals aren't initialized, yet.
Load 03'H into DDR C	H	L	Sets data direction register of port C; buffer full signal works after this step and it is unaffected by the bit-set and clear registers
Load 04'H into Port C Bit-Set Register	L	L	Sets output latch (PC2) to enable $\overline{INTR}$; active $\overline{INTR}$ indicates that CPU should send data; $\overline{INTR}$ becomes inactive whenever the CPU loads port A; $\overline{INTR}$ can be disabled by a bit-clear to $\overline{STB}$.*
OPERATION			
CPU writes to Port A	H	H	Data on CPU bus is latched into port A; $\overline{INTR}$ is set by the CPU write to port A; active BF indicates to peripheral that data is valid; Peripheral gets data from port A; $\overline{INTR}$ is reset active; The active $\overline{INTR}$ signals the CPU to send the next byte. Repeat last two steps until EOT at which time CPU sends bit-clear to the output latch (PC2).
$\overline{STB}$ pulses low	L	L	

*Port C can be read by the CPU at any time, allowing polled operation instead of interrupt driven operation.

• Handshaking Signals

In the Strobed mode of operation, the lower 3-bits of port C transmit/receive the handshake signals (PC0 = $\overline{INTR}$, PC1 = BF, PC2 = $\overline{STB}$).

$\overline{INTR}$ (Strobe Mode Interrupt) is an active-low interrupt from the NSC831 to the CPU. In strobed input mode, the CPU reads the valid data at port A to clear the interrupt. In strobed output mode, the CPU clears the interrupt by writing data to port A.

The $\overline{INTR}$ output can be enabled or disabled, thus giving it the ability to control strobed data transfer. It is enabled or disabled, respectively, by setting or clearing bit 2 of the port C output data latch ($\overline{STB}$).

PC2 is always an input during strobed mode of operation, its output data latch is not needed. Therefore, during strobed mode of operation it is internally gated with the interrupt signal to generate the $\overline{INTR}$ output. Reset clears this bit to zero, so it must be set to one to enable the $\overline{INTR}$ pin for strobed operation.

Once the strobed mode of operation is programmed, the only way to change the output data latch of PC2 is by using the Bit-Set and Clear registers. The port C byte write command will not alter the output data latch of PC2 during the strobed mode of operation.

$\overline{STB}$ (Strobe) is an active low input from the peripheral device, signalling a data transfer. The NSC831 latches data on the rising edge of $\overline{STB}$ if the port bit is an input and the peripheral should latch data on the rising edge of $\overline{STB}$ if the port bit is an output.

BF (Buffer Full) is a high active output from the NSC831. For input port bits, it indicates that new data has been received from the peripheral. For output port bits, it indicates that new data is available for the peripheral.

Note: In either input or output mode the BF may be cleared by rewriting the MDR.

9.0 NSC831/883B MIL-STD-883 Class B Screening

National Semiconductor offers the NSC831D and NSC831E with full class B screening per MIL-STD-883 for Military/ Aerospace programs requiring high reliability. In addition, this screening is available for all of the key NSC800 peripheral devices.

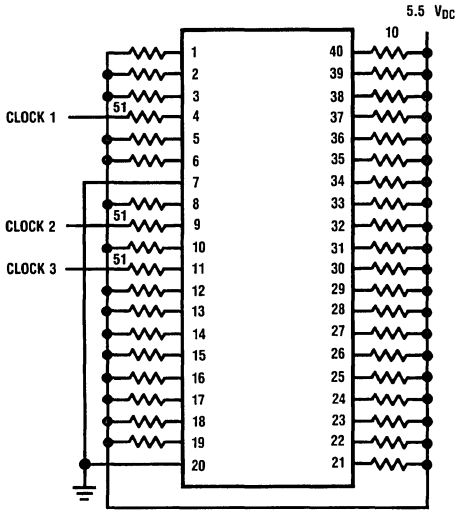
Electrical testing is performed in accordance with RETS831X, which tests or guarantees all of the electrical performance characteristics of the NSC831 data sheet. A copy of the current revision of RETS831X is available upon request. The following table is the MIL-STD-883 flow as of the date of publication.

100% Screening Flow

Test	MIL-STD-883 Method/Condition	Requirement
Internal Visual	2010 B	100%
Stabilization Bake	1008C 24 Hrs. @ +150°C	100%
Temperature Cycling	1010C 10 Cycles −65°C/ +150°C	100%
Constant Acceleration	2001E 30,000 Gs, Y1 Axis	100%
Fine Leak	1014 A or B	100%
Gross Leak	1014C	100%
Burn-In	1015 160 Hrs. @ +125°C (using burn-in circuits shown below)	100%
Final Electrical	+25°C DC per RETS831X	100%
PDA	5% Max	
	+125°C AC and DC per RETS831X	100%
	−55°C AC and DC per RETS831X	100%
	+25°C AC per RETS831X	100%
QA Acceptance	5005	Sample per
Quality Conformance		Method 5005
External Visual	2009	100%

10.0 Burn-In Circuit

5242HR
NSC831AD/883B (Dual-In-Line)



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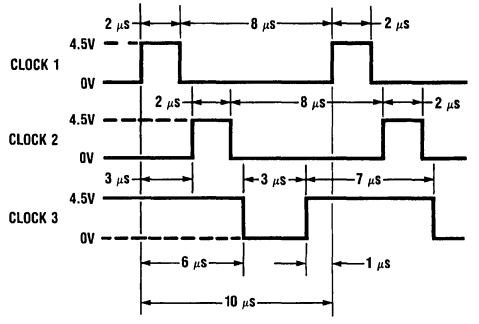
11.0 Timing Diagram

Input Clocks



TL/C/5594–14

Note 1: All resistors ±5%, 1/4 watt unless otherwise designated, 125°C operating life circuit.

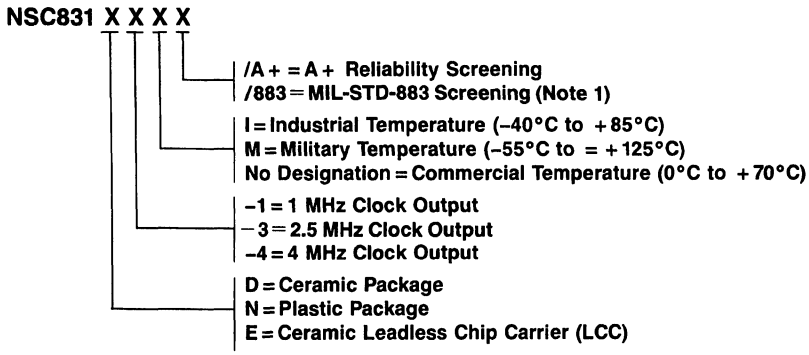
Note 2: E package burn-in circuit 5244HR is functionally identical to the D package.

Note 3: All resistors 2.7 kΩ unless marked otherwise.

Note 4: All clocks 0V to 4.5V.

Note 5: Device to be cooled down under power after burn-in.

12.0 Ordering Information



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Note 1: Do not specify a temperature option: all parts are screened to military temperature.

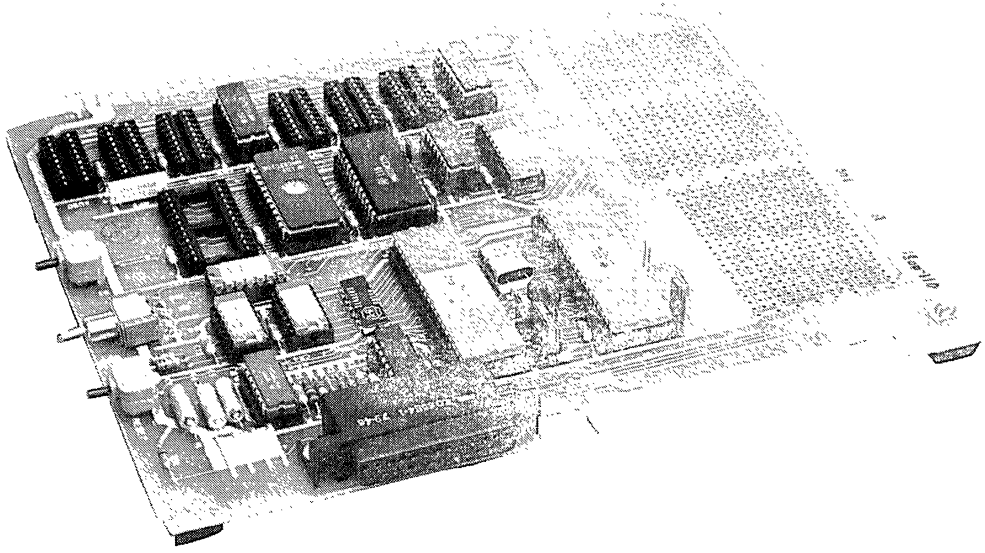
13.0 Reliability Information (NSC831)

Gate Count 1900
Transistor Count 7400

National Semiconductor

microCMOS

NSC888
NSC800™ Evaluation Board



TL/C/8533–1

- **NSC800 8-Bit microCMOS CPU**
- **Executes Z80® Instruction Set**
- **20 programmable parallel I/O lines**
- **Two 16-Bit programmable counters/timers**
- **Powerful 2k x 8 monitor program**
- **Five levels of vectored prioritized interrupts**
- **RS232 Interface**
- **1k x 8 microCMOS RAM with sockets for up to 4k x 8 RAM**
- **Socket for additional 2k x 8, 2716 compatible memory component**
- **Wire wrap area**
- **Edge connectors for system expansion**
- **Single-step operation mode**
- **Fully assembled and tested**

Product Overview

The NSC888 is a self-contained microprocessor board which enables the user to quickly evaluate the performance and features of the NSC800 product family. This fully assembled, tested board requires only the addition of a ±5V supply and an RS232 interface cable to the user's terminal to begin NSC800 evaluation.

A powerful system monitor is provided on the board which controls serial communications via the RS232 port. The monitor also includes command functions to load, execute and debug NSC800 programs.

The board includes an NSC800 CPU plus RAM, EPROM, I/O, Timers and interface components yet draws only 30 mA from the +5V supply and 3 mA from the −5V supply.

Although designed primarily as an assessment vehicle, the NSC888 can be readily programmed and adapted to a variety of uses. Wire wrap area is provided on-board for the user to build up additional circuitry or interfaces, thus tailoring this high-performance, low-power microprocessor board to meet individual needs.

Functional Description

Figure 1 and *Figure 2* provide information on the organization of the NSC888 board. Please refer to these figures for the following discussion.

Central Processor

The powerful NSC800 is the central processor for the NSC888. It provides bus control, clock generation and extensive interrupt capability. Featuring a multiplicity of programmable registers and sophisticated addressing modes, the NSC800 executes the Z80 instruction set.

Memory

- 128 bytes of RAM are provided by the NC810A RAM-I/O-Timer and are used by the monitor program for the system stack.
- 1024 bytes of RAM are provided by two 1k x 4 NMC6514's. Sockets are provided for six additional NMC6514's, for a total of 4k bytes of RAM.
- A 2k byte EPROM system monitor is provided on-board which includes facilities to load, execute and debug a users program.
- An additional EPROM socket is also on-board which accepts a 2k byte 2716 compatible memory component.

Input/Output

- **Parallel I/O**

  The NSC888 provides 20 programmable parallel I/O lines implemented using the I/O ports of the NSC810A RAM-I/O-Timer. The port bits may be individually defined as input or output, and can also be written to or read from in bytes. The I/O lines are conveniently brought to a 50 contact edge connector for user interface.

- **Serial I/O**

  An RS232 connector and accompanying support circuitry are provided on-board. Two I/O lines from the NSC810A RAM-I/O-Timer are used for the serial communications function, which is controlled exclusively by software. The baud rate is determined upon system initialization by the character bit rate from the users terminal. The maximum baud rate is 2400 baud.

Block Diagram

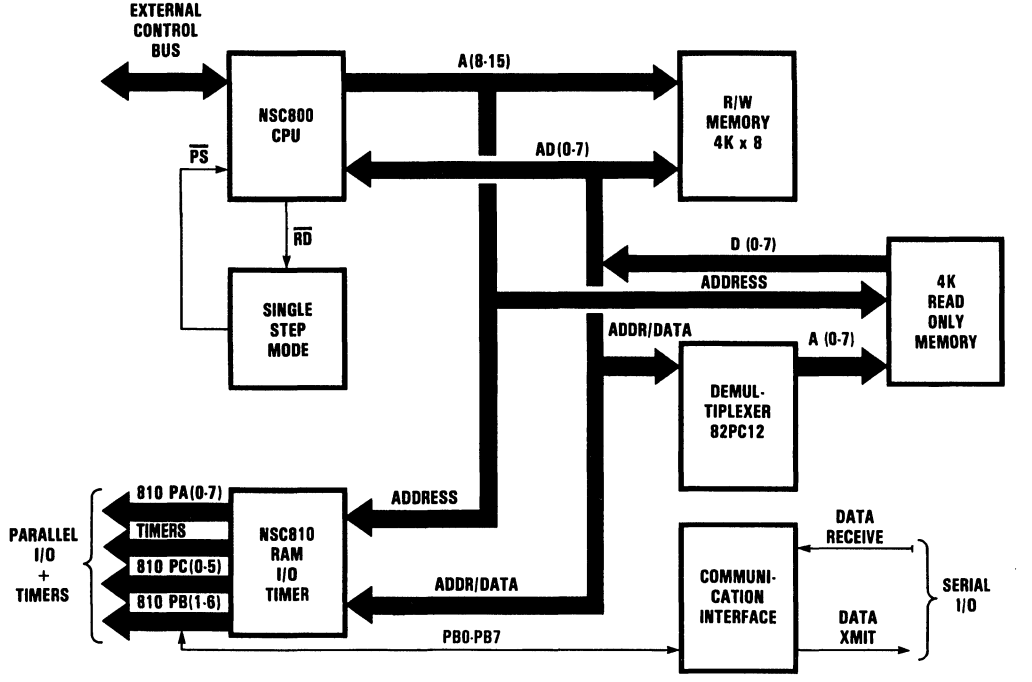


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FIGURE 1

Functional Description (Continued)

Timers

The NSC888 provides two fully programmable binary 16-bit counters/timers utilizing the NSC810A RAM-I/O-Timer. These signals are also brought to the parallel I/O connector. Each timer may operate in any of six different modes:

- Event Counter
- Accumulative Timer
- Restartable Timer
- One Shot
- Square Wave
- Pulse Generator

Connectors

- **Parallel I/O**

  The parallel I/O lines and timer lines from the NSC810A RAM-I/O-Timer, plus interrupt lines from the CPU are brought to this 50 contact edge connector.

- **System Bus**

  All NSC800 CPU lines except XIN are brought to this 86 contact edge connector. In addition, the −5V line is also brought to the system bus connector.

- **RS232**

  This connector is provided for system interface to the users terminal.

Interrupts

The NSC888 utilizes the powerful interrupt processing capability of the NSC800 CPU. Interrupts are routed via a jumper matrix to the five interrupt inputs of the NSC800. Each input, which may be from the NSC810A I/O ports, NSC810A timers or off board via the system bus connector, generates a unique memory address (see Table I). All interrupts with the exception of NMI can be masked via software. Interrupt lines are also brought to the parallel I/O connector.

TABLE I.

Interrupt Input	Memory Address	Type	Priority
NMI	0066H	Non-maskable	Highest
RSTA	003CH	Maskable	
RSTB	0034H	Maskable	
RSTC	002CH	Maskable	
INTR	0038H*	Maskable	Lowest

*mode 1

NSC888 Firmware

The NSC888 system monitor is provided by a preprogrammed EPROM. This comprehensive monitor includes facilities to load, execute and debug programs. The monitor allows the user to examine and modify any RAM memory location or CPU register. It permits the insertion of break points to facilitate debugging. Programs can be executed starting at any location.

The commands supported by the NSC888 system monitor are as follows:

- B - Select a new baud rate
- D - Display memory
- F - Fill memory between ranges
- G - Execute program with break points
- H - Hexadecimal math routine
- J - Non-destructive memory test
- K - Store 16-bit value in memory
- M - Move a block of data
- P - Put ASCII characters in memory
- Q - Query I/O ports
- S - Substitute and/or examine memory
- T - Type memory contents in ASCII
- V - Verify two blocks of data
- X - Examine or modify CPU registers
- Y - Memory search for string

These commands are fully explained in the NSC888 Hardware/Software Users Manual.

Single Step/Power Save

The NSC888 provides a unique single-step mode, utilizing the Power Save input of the NSC800 CPU. This input, when activated, reduces CPU power consumption from 50 mW to only 25 mW. It also allows the user to single-step through a program, checking and modifying code. This function is controlled via a switch on the board.

Specifications

Microprocessor

CPU—	NSC800
Data Word—	8 bits
Instruction Word—	8, 16, 24, 32 bits
Cycle Time—	2.00 μs (minimum instruction time)
System Clock—	2.00 MHz
Registers—	14 general purpose (8-bit) 2 index registers (16-bit) 1 stack pointer (16-bit) 1 program counter (16-bit)
Number of Instructions—	158
Address Capability—	64k bytes

Memory

RAM—	1152 bytes on-board plus sockets for an additional 3k bytes
ROM/EPROM—	Sockets for 4k bytes on-board
Access Time—	625 ns for opcode fetch 875 ns for memory read

Specifications (Continued)

Connectors

System Bus	86-pin double-sided card cage edge connector on 0.156 inch centers
Parallel I/O	50-pin double-sided edge connector on 0.1 inch centers Recommended mating connector: 3M 3415-0001 AMP 2-86792-3
Serial I/O	Standard RS232 connector
Power	+5V 30 mA (27C16 EPROM monitor) or 90 mA (2716 EPROM monitor) −5V 3 mA

Physical

Height	6.75 (17.15 cm)
Width	7.85 (19.94 cm)

Order Information

NSC888	Includes CPU, 1152 bytes of RAM, sockets for additional 3k bytes of RAM, 2k byte monitor with additional socket for 2k byte ROM/EPROM, 20 I/O lines, RS232 interface, wire wrap area.

Documentation

The NSC888 Hardware/ Software Users Manual and NSC800 Microprocessor Family Handbook are shipped with the NSC888 Evaluation Board

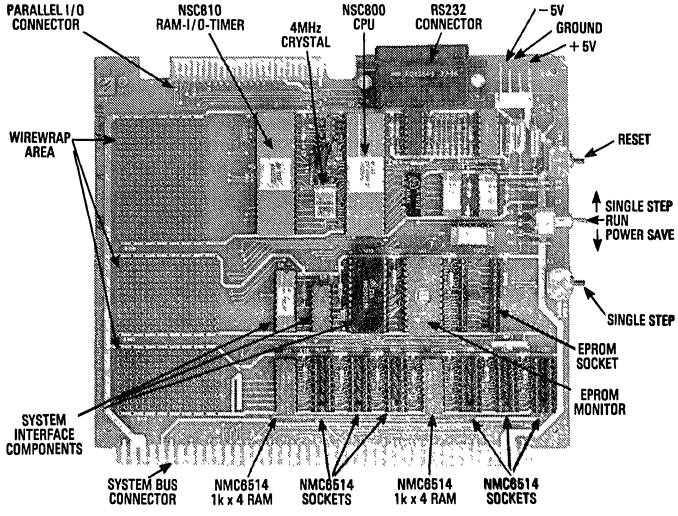

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FIGURE 2. NSC888 Evaluation Board

Comparison Study NSC800 vs. 8085/80C85 Z80®/Z80 CMOS

Introduction

The NSC800 is an 8-bit parallel processor with a Z80 compatible instruction set manufactured using National's micro-CMOS process. This process combines the speed of silicon gate NMOS with the low power inherent to CMOS.

The NSC800 has a 16-bit address bus which consists of the upper eight address bits (A8–A15) and the lower eight address bits (AD0–AD7). Address bits A0–A7 are time multiplexed on the 8-bit bidirectional address/data bus (AD0–AD7).

There are several advantages to using a multiplexed address/data bus. Multiplexing frees pins on the CPU and peripheral packages for other purposes, such as status outputs, DMA control lines, and multiple interrupts. This can reduce system component count. Fewer bus signal lines are required for device interconnections in most applications (16 lines for multiplexed bus systems vs. 24 lines for non-multiplexed systems). This reduces PC board complexity.

Peripherals of the NSC800 Family include:

NSC810A RAM I/O Timer

NSC831 I/O

NSC858 UART

In addition to the above parts, a complete family of low power speed compatible logic and interface parts is also available.

NSC800 vs. 8085

In terms of bus structure, the NSC800 is similar to the 8085. Both processors utilize a multiplexed bus and timing relationships are approximately the same. The 8085 does not guarantee that output data on AD0–AD7 are valid on both the leading and trailing edges of $\overline{WR}$. For the NSC800, data are valid on both the leading and trailing edges of $\overline{WR}$.

Both the NSC800 and the 8085 use ALE, S0, S1, and IO/$\overline{M}$ to indicate status. The lower eight address bits are guaranteed to be valid on the data bus at the trailing edge (high to low transition) of ALE (Address Latch Enable). This signal is used by the external system components to separate the address and data buses. When the only components utilized in the system are members of the NSC800 family (which contain on-chip demultiplexers), ALE needs only to be connected to the enable inputs. If non-NSC800 family components are used, ALE can be used to enable an 8-bit latch to perform the function of bus separation.

Decoding status bits S0 and S1, in conjunction with IO/$\overline{M}$, notifies the external system of the type of the ensuing M cycle. TABLE I shows a truth table of the encoded information. During a halt status the NSC800 will continue to refresh dynamic RAM.

TABLE I.
Machine Cycle Status - NSC800 and 8085

S0	S1	IO/M	Status
1	0	0	Memory Write
0	1	0	Memory Read
1	0	1	I/O Write
0	1	1	I/O Read
1	1	0	Opcode Fetch
0	1	0	Bus Idle*
0	0	0	Halt

*ALE not suppressed during Bus Idle

Direct Memory Access (DMA) control signals $\overline{BREQ}$ and $\overline{BACK}$ of the NSC800 perform the same functions as HOLD and HLDA on the 8085. The NSC800 allows simple wire ORing by using active low states for the DMA control signals. An active low on the $\overline{BREQ}$ (Bus Request) line, tested during the last T state of the current M cycle, initiates a DMA condition. The NSC800 will then respond with an active low $\overline{BACK}$ (Bus Acknowledge) signal causing the address, data and control buses (TRI-STATE® circuits) to go to the high impedance state, and notifies the interrupting device that the system bus is available for use. There is a difference in the timing relationship between these functions for the two processors. The 8085 responds with HLDA, one-half T state after it recognizes HOLD. The NSC800 responds with $\overline{BACK}$, one T state after it recognizes $\overline{BREQ}$.

During Input/Output cycles for peripherals, the NSC800 automatically inserts one wait state. This reduces the external hardware required for slow peripherals. The 8085 does not insert its own wait state during these I/O cycles. When they are needed, the 8085 user must design his system to contain the additional hardware required to do the wait state insertion. When more than one wait state is required, additional wait states can be added to the I/O cycles in a similar way on both the NSC800 and the 8085. On the NSC800, this is accomplished by bringing the $\overline{WAIT}$ control signal active low during T2 of an I/O or memory cycle. The 8085 is controlled in the same way through the use of the READY line.

The NSC800 instruction set is Z80 compatible and more powerful than the 8085's. The NSC800 does not support the RIM and SIM instructions of the 8085 (RIM and SIM can be emulated with I/O instructions), but has an improved instruction set for enhanced system performance. The NSC800 has two functions, $\overline{RFSH}$ and PS, instead of the two serial I/O lines SOD and SID. $\overline{RFSH}$ (Refresh) is a status signal which indicates that an eight bit refresh address is present on the address/data bus (AD0–AD7). The refresh address occurs during T3 of each M1 (opcode fetch) cycle. The internal refresh counter is incremented after

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each instruction cycle. This counter output can be employed by the user's dynamic RAM refresh circuits. The $\overline{PS}$ (Power Save) control input, when active, causes the CPU to stop all internal clocks at the end of the current instruction, which reduces power consumption. The on-chip oscillator and CLK remain active for any required external timing. The NSC800 leaves all buses unchanged during this time, which has the effect of reducing power consumption on other CMOS parts in the system since the buses are not changing states. All internal registers and status conditions are maintained, and when $\overline{PS}$ subsequently goes high, the opcode fetch cycle begins in a normal fashion.

TABLE II indicates the major differences between the NSC800 and the 8085 presented in tabular form for quick reference.

TABLE II.
NSC800 vs. 8085/80C85 Comparison

Item	NSC800	8085	80C85
Power Consumption	50 mW @ 5V	850 mW @ 5V	50 mW @ 5V
Bus Drive Capacity	1 std. TTL (100 pF)	1 std. TTL (100 pF)	1 std. TTL (150 pF)
Dynamic RAM Refresh Counter	Yes, 8-bit	No	No
Automatic WAIT State on I/O	Yes	No	No
Number of instruction types	158	80	80
Number of Programmer Accessible Registers	22	10	10
Block I/O and Search	Yes	No	No

NSC800 vs. Z80/Z80 CMOS

The NSC800 contains the same complement of internal registers as the Z80 and maintains instruction set and opcode compatibility.

Machine cycle timing for the standard speed version of the NSC800 compares directly with the Z80. Although the software execution speeds are comparable, the NSC800 offers architectural advantages.

The bus structures of the NSC800 and the Z80 are quite different. The NSC800 uses a multiplexed address/data bus. The Z80 has separate address and data buses. As stated earlier, the separate bus structure requires additional signal lines for interconnection and gives up some package pins which could be used for other purposes.

The main differences between the NSC800 and the Z80, in addition to the bus structures, are the refresh counter, on-chip clock generation, and the interrupt capability.

1. The NSC800 contains an 8-bit refresh counter as opposed to a 7-bit refresh counter in the Z80. (This enables refresh of a 64K dynamic RAM system memory). The refresh timing of the NSC800 is functionally identical to that of the Z80.
2. The on-chip clock generation reduces the system component count. In place of an external clock generator chip, the NSC800 needs only a crystal or RC circuit to produce the system clock.
3. The NSC800 provides three interrupts that are not available on the Z80: $\overline{RSTA}$, $\overline{RSTB}$, $\overline{RSTC}$. This gives the NSC800 five levels of vectored, prioritized interrupts with no external logic. The general purpose interrupt ($\overline{INTR}$) and Non-maskable Interrupt ($\overline{NMI}$) are identical to the Z80. $\overline{INTR}$ has the same three modes of operation in both processors: Modes 0, 1, and 2. Upon initialization, the NSC800 is in mode 0 to maintain 8080 code compatibility. $\overline{NMI}$, when active, causes a restart to location X'66 as is the case with the Z80. Being a non-maskable interrupt, $\overline{NMI}$ cannot be disabled. The additional interrupts $\overline{RSTA}$, $\overline{RSTB}$, and $\overline{RSTC}$ cause restarts to locations X'3C, X'34, and X'2C respectively. The priority levels of the five interrupts are: $\overline{NMI}$ (highest), $\overline{RSTA}$, $\overline{RSTB}$, $\overline{RSTC}$, and $\overline{INTR}$ (lowest). For the NSC800, Interrupt acknowledge ($\overline{INTA}$) is provided on a dedicated output pin and need not be decoded externally, as is the case with the Z80. With the status outputs (S0, S1, IO/$\overline{M}$), early read/write information is obtainable. This is impossible to derive from the Z80.

   Refer to TABLE III for comparison of the major differences between the NSC800 and the Z80.

TABLE III.
NSC800 vs. Z80/Z80 CMOS Comparison

Item	NSC800	Z80	Z80 CMOS
Power Consumption	50 mW @ 5V	750 mW @ 5V	75 mW @ 5V
Instruction Execution (Minimum)	1 μs	1 μs	1 μs
On-Chip Clock Generator	Yes	No	No
Number of On-Chip Vectored Interrupts	5	2	2
Early Read/Write Status	Yes	No	No
Dynamic RAM Refresh Counter	Yes, 8-bit	Yes, 7-bit	Yes, 7-bit

NSC800 Family Devices (microCMOS)

MM82PC08 8-Bit Bidirectional Transceiver

MM82PC12 Input/Output Port

Note: The above devices are pin for pin and function compatible with the standard TTL, CMOS or NMOS versions currently available.

SUMMARY

National's NSC800 has a Z80 compatible instruction set, which is more powerful than the 8085. NSC800 external hardware requirements are less because of on-chip automatic wait state insertion, clock generation and five levels of vectored prioritized interrupts.

The 8085 and the NSC800 have similar bus structures, and timing. The key advantages of the NSC800 over the 8085 are the larger instruction set, more registers accessible to programmers, low power consumption, and a dynamic RAM refresh counter.

The main advantages of the NSC800 compared to the Z80 are the multiplexed address/data bus, an 8-bit refresh counter for dynamic RAMs, on-chip clock generation, and five interrupts. The speed of the NSC800 and Z80 is the same but, the NSC800 has very low power consumption.

Software Comparison NSC800 vs. 8085, Z80®

Introduction

The NSC800 is an 8-bit parallel microprocessor fabricated using National's microCMOS process. This process allows fabrication of a microprocessor family that has the performance of silicon gate NMOS along with the low power inherent to CMOS. The NSC800 instruction set is a superset of the 8080's instruction set. It comprises over 900 operation codes falling into 158 instruction types. The instruction categories are:

- Load and Exchange
- Arithmetic and Logic
- Rotate and Shift
- Jump and Call
- Input/Output
- Bit manipulation (set, test, reset)
- Block Transfer and Search
- CPU control

The load instructions allow the movement of data into and out of the CPU, between internal registers, plus the capability to load immediate data into internal registers. The exchange instructions allow swapping of data between two registers.

The arithmetic and logic instructions operate on the data in the accumulator (primary working register) and in the other registers. Status flags are set or reset depending on the result of the particular operation executed. This group includes 8-bit and 16-bit operations.

The rotate and shift instructions allow any register or memory location to be rotated or shifted, left or right, with or without carry. These can be either an arithmetic or logic type.

The jump and call group includes several different types: one byte calls, two byte relative jumps, conditional branching, and three byte calls and jumps, which can reach any location in memory. Calls push the current contents of the Program Counter onto the stack before branching to the new program address to facilitate subroutine execution.

Input/Output instructions allow communications between the NSC800 and external peripheral devices. There are 255 (location X'BB is used for an interrupt mask) unique peripheral I/O locations available to the NSC800. I/O instructions can move data between any memory location or internal register and any I/O location. There are also block I/O instructions which allow moving data blocks of up to 256 bytes directly from memory to any peripheral location or from any peripheral location to a block of memory.

Bit manipulation instructions can set, test or reset any bit in the accumulator, any general purpose register or any memory location.

The block transfer instructions allow a single instruction to move any size block of memory to any other location in memory. Through the use of the block search instructions, any size block of memory can be searched for a particular byte of data.

Finally, the CPU control group allows user control over the various modes of CPU operation, such as enabling and disabling interrupts or setting modes of interrupt response.

The following sections will compare the instruction set of the NSC800 with those of the 8085 and the Z80.

NSC800 vs. 8085

The 8085 instruction set consists of 246 op codes falling into 80 instruction types. With the exception of RIM and SIM, the NSC800 is instruction and op code compatible with the 8085. The RIM and SIM instructions are not supported because the NSC800 does not have the SID and SOD serial I/O lines. The interrupt mask on the NSC800 is accessible by writing the mask word to I/O location X'BB. The bit positions for the interrupt enables are shown below:

Location X'BB Bit Assignments

Bit	Interrupt Enable for
7	N/A
6	N/A
5	N/A
4	N/A
3	$\overline{\text{RSTA}}$
2	$\overline{\text{RSTB}}$
1	$\overline{\text{RSTC}}$
0	$\overline{\text{INTR}}$

N/A = not used: a don't care bit.

As an example, to enable interrupts on the $\overline{\text{RSTA}}$ input, a logic '1' is written into bit 3 of I/O location X'BB. If the master interrupt enable has been set by executing the Enable Interrupt (EI) instruction, interrupts will now be accepted on $\overline{\text{RSTA}}$ only.

Other than the method of enabling and disabling individual interrupts and the RIM and SIM instructions themselves, the NSC800 instruction set is a superset of the 8085's instruction set.

The following benchmark demonstrates the code reduction and throughtput improvement obtained by using one of the special NSC800 instructions over the same function implemented with the limited 8085 instruction set. The function is to move a 512-byte block of data from one section of memory to another.

8085

Bytes		Mnemonics		Cycles
3		LXI	H,SOURCE	10
3		LXI	D,DEST	10
3		LXI	B,COUNT	10
1	LOOP:	MOV	A,M	7
1		STAX	D	7
1		INX	H	6
1		INX	D	6
1		DCX	B	6
1		MOV	A,C	4
1		ORA	B	4
3		JNZ	LOOP	10
Total: 19				Total: 80

NSC800

Bytes	Mnemonics		Cycles
3	LD	HL,SOURCE	10
3	LD	DE,DEST	10
3	LD	BC,COUNT	10
2	LDIR		21
Total: 11			Total: 51

The use of the LDIR instruction of the NSC800 results in a 47.5% increase in throughput and a 42% decrease in the number of bytes required to implement the function when compared with the 8085 implementation. The time required to make the move is approximately 2.69 ms for the NSC800 and approximately 5.12 ms for the 8085. Note that even though the 8085 runs at a faster cycle time (200 ns vs. 250 ns), the improved instruction set of the NSC800 produces an increase in system performance.

The NSC800 includes all 8085 flags plus some additional flags. The flag formats for the NSC800 and 8085 are:

NSC800 Flags (Z80 Flags)

7	6	5	4	3	2	1	0
S	Z	X	H	X	P/V	N	C

8085 Flags

7	6	5	4	3	2	1	0
S	Z	X	AC	X	P	X	CY

The differences between the flag registers on the NSC800 and the 8085 are identified below:

1. Bit position D1 (additional on the NSC800) contains an add/subtract flag that is used internally for proper operation of BCD instructions.

2. In the NSC800, the P/V flag will not match the 8085's P flag after an 8-bit arithmetic operation, since it acts as an overflow bit for the NSC800, but acts as a parity bit for these operations in the 8085.

3. Bit position D2 (changed for the NSC800) is a dual purpose flag; it indicates the parity of the result in the accumulator when logical operations are performed and also represents overflow when signed two's complement arithmetic operations are performed. An overflow occurs when the result of a two's complement operation within the accumulator is out of range.

4. For general Compare operations, the NSC800 uses the P/V flag as an overflow bit, while the 8085 uses the P flag for parity.

5. The H flag (bit position D4) on the NSC800 is functionally the same as the auxiliary carry on the 8085.

6. For Double Precision Addition, the NSC800 leaves the H flag undefined, while the 8085 does not affect the AC flag for this operation (DAD).

7. For Rotate operations, the NSC800 resets the H flag, while the 8085 leaves the AC flag unaffected for these operations.

8. When Complementing the Accumulator, the NSC800 sets the H flag (H = 1), while the 8085 leaves the AC flag unaffected.

9. When Complementing Carry, the NSC800 leaves the H flag undefined, while the 8085 leaves the AC flag unaffected.

10. When Setting the Carry, the NSC800 clears the H flag (H = 0), while the 8085 leaves the AC flag unaffected.

NSC800 vs. Z80

The instruction set and op codes of the NSC800 are identical to those of the Z80. Software written for the Z80 will run on the NSC800 without change, unless I/O location X'BB is used. Another location should be assigned since location X'BB is an on-chip write-only register used for the interrupt mask. Since the NSC800 executes code at the same cycle time as the Z80, any software timing loops will also remain the same, and no change is necessary. The NSC800 expanded interrupt capability is transparent to the user unless specifically evoked by the user software.

The NSC800 has 8-bit refresh rather than the 7-bit refresh scheme of the Z80. Therefore, the state of the 8th bit will be indeterminate since it is part of the R Register and so included in refresh operations.

The status flags on the NSC800 are identical to those on the Z80. There is no difference between the positions of the individual bits in the flag register, nor in the manner in which the flags are set or reset due to an arithmetic or logical operation. Testing of the flags is also the same.

Section 10

Physical Dimensions/ Appendices

Section 10 Contents

Glossary

In our efforts to be concise and precise, we often invent new words or acronyms to use as shorthand representations of "things" that require much longer names if the jargon is not used. Being humans, we then become very impressed with our ability to exclude those not in "the know" and another "in" group is formed. This glossary has been developed to help bridge this language gap. We know it will help. We hope you will use it.

Abort—The first step of recovery when an instruction or its operand(s) is not available in main memory. An Abort is initiated by the Memory Management Unit (MMU) and handled by the CPU.

Absolute Address—An address that is permanently assigned to a fixed location in main memory. In assembly code, a pattern of characters that identifies a fixed storage location.

Access Time—The time interval between when a request for information is made and the instant this information is available.

Access Class—The five Series 32000 access classes are memory read, memory write, memory read-modify-write, memory address, and register address. The access class informs the Series 32000 CPU how to interpret a reference to a general operand. Each instruction assigns an access class to each of it two operands, which in turn fully defines the action of any addressing mode in referencing that operand.

Accumulator—A register which stores the result of an ALU operation.

Ada—A high level language designed for the Department of Defense. It gives preference to full English words. It is meant to be the standard military language.

Address—An expression, usually numerical, which designates a specific location in a storage or memory device.

Address-Data Register—A register which may contain either address or data, sometimes referred to as a general-purpose register.

Address Strobe—Control signal used to tell external devices when the address is valid on the external address bus.

Address Translation—The process by which a logical address emanating from the CPU is transformed into a physical address to main memory. This is performed by the Memory Management Unit (MMU) in Series 32000 systems. Logical address to Physical address mapping is established by the operating system when it brings pages into main memory.

Addressing Mode—The manner in which an operand is accessed. Series 32000 CPUs have nine addressing modes: Register, Register Relative, Memory Relative, Immediate, Absolute, External, Top-of Stack, Memory Space, and Scaled Indexing.

Algorithm—A set of procedures to which a given result is obtained.

Alignment—The issue of whether an instruction must begin on a byte, double byte, or quad byte address boundary.

ALU—Arithmetic Logic Unit. A computational subsystem which performs the arithmetic and logical operations of a digital system.

Array—A structured data type consisting of a number of elements, all of the same data type, such that each data element can be individually identified by an integer index. Arrays represent a basic storage data type used in all high-level languages.

ASCII—(*American National Standard Code for Information Interchange,* 1968). This standard code uses a character set generally coded as 7-bit characters (8-bits when using parity check). Originally defined to allow human readable information to be passed to a terminal, it is used for information interchange among data processing systems, communication systems, and associated equipment. The ASCII set consists of alphabetic, numeric, and control characters. Synonymous with USASCII.

Assemble—To prepare a machine language program (also called machine code or object code) from a symbolic language program by substituting absolute operation codes for symbolic operation codes and absolute or relocatable addresses for symbolic addresses. Machine code is a series of ones and zeros which a computer "understands".

Assembler—This program changes the programmer's source program (written in English assembly language and understandable to the programmer) to the 1's and 0's that the machine "understands". In particular, the Assembler converts assembly language to machine code. This machine code output is called the OBJECT file.

Assembly Language—A step up in the language chain. This is a set of instructions which is made up of alpha numeric characters which, with study, are understandable to the programmer. Different type of machines have different assembly languages, so the assembly language programmer must learn a different set of instructions each time s/he changes machine.

Associative Cache—A dual storage area where each data entry has an associated "tag" entry. The tags are simultaneously compared to the input value (a logical address) in the case of the MMU, and if a matching tag is found, the associated data entry is output. An associative cache is present within the MMU in Series 32000 systems to provide logical-to-physical address translation.

Asynchronous Device—A device in which the speed of operation is not related to any frequency in the system to which it is connected.

BASIC—This acronym stands for Beginner's All-purpose Symbolic Instruction Code. BASIC is one of the most "English like" of the high level languages and is usually the first programming language learned.

Baud Rate—Data transfer rate. For most serial transmission protocols, this is synonymous with bits-per-second (bps).

BCD—Binary Coded Decimal. A binary numbering system for coding decimal numbers. A 4-bit grouping provides a binary value range from 0000 to 1001, and codes the decimal digits "0" through "9". To count to 9 requires a single 4-bit grouping; to count to 99 takes two groupings of 4 bits; to count to 999 takes three groupings of 4 bits, etc.

Benchmark—In terms of computers, this refers to a software program designed to perform some task which will demonstrate the relative processing speed of one computer versus another.

Glossary (Continued)

Bit—An abbreviation of "binary digit". It is a unit of information represented by either a one or a zero.

Bit Field—A group of bits addressable as a single entity. A bit field is fully specified by the location of its least significant bit and its length in bits. In Series 32000 systems, bit fields may be from one to 32 bits in length.

Branch—A nonsequential flow in a software instruction stream.

Breakpoint—A place in a routine specified by an instruction, instruction digit, or other condition, where the software program flow will be interrupted by external intervention or by a monitor routine.

Buffer—An isolating circuit used to avoid reaction of a driven circuit on the corresponding driver circuit. Buffers also supply increased current drive capacity.

Bus—A group of conductors used for transmitting signals or power.

Bus Cycle—The time necessary to complete one transfer of information requiring the use of external address, data and control buses.

Byte—Eight bits.

Byte Enable—$\overline{BE0}$ to $\overline{BE3}$. CPU control signals which activate memory banks, each bank providing one byte of data per address.

C—A highly structured high level language developed by Bell Laboratories to optimize the size and efficiency of the program. This language has gained much popularity because it allows the programmer to get close to the hardware (low level) as well as being a high level language. Before C, the programmer who had to address the hardware had to use assembly language or machine code.

Cache—See Associative Cache.

Cache Hit—In the MMU, logical-to-physical address translation takes place via the associative cache. For this to happen, the addressed page must be resident in physical memory such that a logical address tag is present in the MMU's translation cache.

Cache Miss—When a logical address is presented to the MMU, and no physical address translation entry is found in the MMU's associative cache.

Cascaded—Stringing together of units to expand the operation of the unit. Interrupt Control Units present in a Series 32000 system which are in addition the Master ICU are referred to as "cascaded" ICUs; i.e., interrupts cascade from a second-level ICU through the master ICU to the CPU.

Clock—A device that generates a periodic signal used for synchronization.

Clock Cycle—After making a low-to-high transition, the clock will have completed one cycle when it is about to make another low-to-high transition. This time is equal to 1/f where f = the clock frequency.

COBOL—This acronym stands for "Common Business Oriented Language". It is a language especially good for bookkeeping and accounting.

COFF-COMMON OBJECT FILE FORMAT is a standard way of constructing files developed by AT&T for the express purpose of making all files similar. This will help reduce the situation where large files developed by one organization won't run on another organization's equipment simply because the software interfaces are different. It provides a great potential for savings in both time and money.

Compile—To take a program written in a High-Level Language such as C, Pascal, or FORTRAN and convert it into an object-code format which can be loaded into a computer's main memory. During compilation, symbolic HLL statements, called source code, are converted into one or more machine instructions which the CPU "understands". A compiler also calls the assemble function.

Compiler—The program that converts from Source to Machine Code. The conversion is from a particular high level language to machine code. For example, the C compiler will convert a C source program written by a programmer to machine code. This machine code output is in the same format as that of the assembler and is also called an OBJECT file.

CPU—Central Processing Unit. The portion of a computer system that contains the arithmetic logic unit, register file, and other control oriented subsystems. It performs arithmetic operations, controls instruction processing, and provides timing signals and other housekeeping operations.

Cross Support—The alternative to using a "Native" development like SYS32 to develop your programs is to use Cross Support software. "Native" means that the CPU in the development system is the same as the CPU in the system being developed. Cross support software is all of the necessary programs for development that operate on one CPU, but generate code for another CPU. Use of the VAX to generate Series 32000 code is a good example of cross support.

Demand-Paged Virtual Memory—A virtual memory method in which memory is divided into blocks of equal size which are referred to as pages. These pages are then moved back and forth between main memory and secondary storage as required by the CPU. Demand paging reduces the problem of memory fragmentation which results in unused memory space.

Dispatch Table—In Series 32000 systems, this is an area of memory which contains interrupt descriptors for all possible hardware interrupts and software traps. The interrupt descriptor directs the CPU to the module descriptor for the procedure which is designed to handle that particular interrupt.

Displacement—A numerical offset from a known point of reference. Displacements are used in programming to facilitate position independent code, such that a given program can be loaded anywhere in memory. In Series 32000 processors, a displacement is contained in the instruction itself.

Glossary (Continued)

DMA—Direct Memory Access. A method that uses a small processor (DMA Controller) whose sole task is that of controlling input-output or data movement. With DMA, data is moved into or out of the system without CPU intervention once the DMA controller has been initialized by the CPU and activated.

Double-Precision—With reference to 32000 floating-point arithmetic, a double-precision number has a 52-bit fraction field, 11-bit exponent field and a sign bit (64-bits total).

Double Word—Two words, i.e., 32 bits.

Editor—A program which allows a person to write and modify text. This program can be as complicated as the situation requires, from the very simple line editor to the most complicated word processor. Letters, numbers and unprintable control characters are stored in memory so that they can be recalled for modification or printing. The programmer uses this device to enter the program into the computer. At this stage, the program is recognizable to both the programmer and the computer as lines of English text. This English version of the program is known as the SOURCE.

Emulate—To imitate one system with another, such that the imitating system accepts the same data, executes the same programs, and achieves the same results as the imitated system.

Exception—An occurrence which must be resolved through CPU intervention. An exception results in the suspension of normal program flow. In Series 32000 systems, exceptions occur as a result of a hardware reset, interrupt or software traps. Execution of floating-point instructions may also result in occurrences which must be resolved through CPU intervention.

Exponent—In scientific notation, a numeral that indicates the power to which the base is raised.

EXEC2—NSC's Real Time Executive for Series 32000.

FIFO—First-in first-out. A FIFO device is one from which data can be read out only in the same order as it was entered, but not necessarily at the same rate.

Floating-Point—A method by which computers deal with numbers having a fractional component. In general, it pertains to a system in which the location of the decimal/binary point does not remain fixed with respect to one end of numerical expressions, but is regularly recalculated. The location of the point is usually given by expressing a power of the base.

FORTRAN—A high level language written for the scientific community. It makes heavy use of algebraic expressions and arithmetic statements.

FP—Frame Pointer. CPU register which points to a dynamically allocated data area created at the beginning of a procedure by the ENTER instruction.

FPU—Floating-Point Unit is a slave processor in Series 32000 systems which implements in hardware all calculations needed to support floating-point arithmetic, which otherwise would have to be implemented in software. The NS32081 FPU provides high-speed floating point instructions for single (32-bit) and double (64-bit) precision. Supports IEEE standard for binary floating point arithmetic. Compatible with NS32032, NS32C032, NS32016, NS32C016 and NS32008 CPUs.

Fragmented—The term used to describe the presence of small, unused blocks of memory. The problem is especially common in segmented memory systems, and results in inefficient use of memory storage.

Frame—A block of memory on the stack that provides local storage for parameters in the current procedure.

GENIX—The NSC version of the UNIX operating system, ported to work with the Series 32000. It also has all of the necessary utilities added so that program development can be accomplished.

Hardware—Physical equipment, e.g., mechanical, magnetic, electrical, or electronic devices, as opposed to the software programs or method in which the hardware is used.

High Level Languages—These are languages which are not dependent on the type of computer on which they run. A program written in a high level language will generally run on any computer for which there is a compiler for that language. This feature makes high level languages "Portable", i.e., the same program will run on many different types of computers. A HLL requires a compiler or interpreter that translates each HLL statement into a series of machine language instructions for a particular machine.

ICU—Interrupt Control Unit. A memory-mapped microprocessor support chip in Series 32000 systems which handles external interrupts as well as additional software traps. The ICU provides a vector to the CPU to identify the servicing software procedure.

Indexing—In computers, a method of address modification that is by means of index registers.

Index Register—A register whose contents may be added to or subtracted from the operand address.

Indirect Addressing—Programming method where the initial address is the storage location of a word which is the actual address. This indirect address is the location of the data to be operated upon.

Instruction—A statement that specifies an operation and the values or locations of its operands, i.e., it tells the CPU what to do and to what.

Instruction Cycle—The period of time during which a programmed system executes a particular instruction.

Instruction Fetch—The action of accessing the next instruction from memory, often overlapped by its partial execution.

Instruction Queue—With Series 32000 CPUs, this is a small area of RAM organized as a FIFO buffer which stores prefetched instructions until the CPU is ready to execute them.

Interpreter—A program which translates HLL statements into machine instructions at run time, i.e., while the program is executing, and is co-resident with the user program.

Glossary (Continued)

Interrupt—To signal the CPU to stop a software program in such a way that it can be resumed and branch to another section of code. Interrupts can be caused by events external or internal to the CPU, and by either software or hardware.

INTBASE—Interrupt Base Register. In the Series 32000, a 32-bit CPU register which holds the address of the dispatch table containing addresses for interrupts and traps.

ISE—In-System Emulator. A computer system which imitates the operation of another in terms of software execution. In microprocessor system development, the ISE takes the place of the microprocessor by means of a connector at the end of an umbilical cable. Not only does the ISE perform all the functions of the microprocessor, but it also allows the engineer to debug his system by setting breakpoints on various conditions, permits tracing of program flow, and provides substitution memory which may be used in place of actual target system memory.

ISV—Independent Software Vendor. A vendor, independent from National Semiconductor, who ports or develops software for Series 32000 components. They in turn sell this software to our customers who are designing Series 32000 based products.

Kernel—This is the name given to the core of the operating system. Other programs are added to the kernel to provide the features of the operating system. The kernel provides control and synchronization.

Language—A set of characters and symbols and the rules for using them. In our context, it is the "English like" format of the instructions which are understood by both the programmer and the computer.

Library—High level languages as well as assembly language contain many routines which are used over and over again. To prevent the programmer from having to write the routine every time it is needed, these routines are stored in libraries to be referenced each time they are needed. These libraries are also OBJECT files.

Linear Address Space—An address space where addresses start at location zero and proceed in a linear fashion (i.e., with no holes or breaks) to the upper limit imposed by the total number of bits in a logical address.

Link Base—In the Series 32000, Module Descriptor entry which points to a table in memory containing entries which reference variables or entry points in Modules external to the one presently executing.

Linker—Large programs are generally broken down to component parts and farmed out to several programmers. Each one of these parts is called a MODULE. Each programmer will develop the module using either high level or assembly language, then "assemble" assembly language modules or "compile" high level language modules. A programmer tells the linker how to connect these modules to make the program run. The linker makes these connections, resolves all questions about data needed by one module, but contained in another, finds all library routines, and cleans up any other loose ends. The output from the linker is called BINARY file and is the file that will run on the computer.

Logical Address Space—The range of addresses which a programmer can assign in a software program. This range is determined by the length of the computer's address registers.

LSB—Least Significant Bit. The bit in a string of bits representing the lowest value.

Machine Code—The code that a computer recognizes. Specifies internal register files and operations that directly control the computer's internal hardware.

Machine Language—The ones and zeros which are "understood" by the machine. This is often called "Binary Code." The programmer must be able to understand the bit patterns to be able to decipher the language. Each machine has a unique machine language.

Main Memory—The program and data storage area in a computer system which is physically addressed by the microprocessor or MMU address lines.

Mantissa—In a floating-point number, this is the fractional component.

Mapping—The process whereby the operating system assigns physical addresses in main memory to the logical addresses assigned by the software.

Memory-Mapped—Referring to peripheral hardware devices which are addressed as if they were part of the computer's memory space. They are accessed in the same manner as main memory, i.e., through memory read/write operations.

Microcode—A sequence of primitive instructions that control the internal hardware of a computer. Their execution is initiated by the decoding of a software instruction. Microcode is maintained in special storage and often used in place of hardwired logic.

Microcomputer—A computer system whose Central Processing Unit is a Microprocessor. Generally refers to a board-level product.

Minicomputer—A "box-level" computer with system capabilities generally between that of a microcomputer and a mainframe.

MMU—Memory Management Unit. This is a slave processor in Series 32000 which aids in the implementation of demand-paged virtual memory. It provides logical to physical address translation and initiates an instruction abort to the CPU when a desired memory location is not in main memory.

MOD—Mod Register. In the Series 32000, a 16-bit CPU register which holds the address of the Module Descriptor of the currently executing software module.

Module—An independent subprogram that performs a specific function and is usually part of a task, i.e., part of a larger program.

Module Descriptor—In the Series 32000, a set of four 32-bit entries found in main memory. Three are currently defined and point to the static data area, link table, and first instruction of the module it describes. The fourth is reserved.

Glossary (Continued)

Modularity—A software concept which provides a means of overcoming natural human limitations for dealing with programming complexity by specifying the subdivision of large and complex programming tasks into smaller and simpler subprograms, or modules, each of which performs some well-defined portion of the complete processing task.

MSB—Most Significant Bit. The bit in a string of bits representing the highest value.

NET—Short for NETWORK and describes a number of computers connected to each other via phone or high speed links. A net is convenient for exchanging common information in the form of "mail" as well as for data exchange.

NMI—Nonmaskable Interrupt. A hardware interrupt which cannot be disabled by software. It is generally the highest priority interrupt.

Object Code—Output from a compiler or assembler which is itself executable machine code (or is suitable for processing to produce executable machine code).

Operand—In a computer, a datum which is processed by the CPU. It is referenced by the address part of an instruction.

Operating System—A collection of integrated service routines used by the computer to control the sequence of programs. The operating system consists of software which controls the execution of computer programs and which may provide storage assignment, input/output control, scheduling, data management, accounting, debugging, editing, and related services. Their sophistication varies from small monitor systems, like those used on boards, to the large, complex systems used on main frames.

Operating System Mode—In this mode, the CPU can execute all instructions in the instruction set, access all bits in the Processor Status Register, and access any memory location available to the processor.

Operator—In the description of an instruction, it is the action to be performed on operands.

Page Fault—A hardware generated trap used to tell the operating system to bring the missing page in from secondary storage.

Page Swap—The exchange of a page of software in secondary storage with another page located in main memory. The operating system supervises this operation, which is executed by the CPU and involves external devices such as disk and DMA controllers.

Page Table—A 1K-byte area in main memory containing 256 entries which describe the location and attributes of all pointer tables, i.e., a list of pointer table addresses.

Peripheral—A device which is part of the computer system and operates under the supervision of the CPU. Peripheral devices are often physically separated from the CPU.

Pascal—A high level language designed originally to teach structured programming. It has become popular in the software community and has been expanded to be a versatile language in industry.

Physical Address—The address presented to main memory, either by the CPU or MMU.

Pointer Table—A 512-byte page located either in main memory or secondary storage containing 128 entries. Each entry describes an individual page of the software program. Each page of the software program may reside in main memory or in secondary storage.

Pop—To read a datum from the top of a stack.

PORT—To port an operating system is to cause that particular operating system to operate with a defined hardware package. GENIX is the NSC version of UNIX which has been ported to SYS32. The operating system for other Series 32000 based systems will differ in some degree from SYS32 and the NSC GENIX binary will not operate. It is now necessary to modify GENIX to fit the situation caused by the new hardware. The GENIX SOURCE is used because this is the program that is most readily understood by the programmer. The source is changed, compiled, and linked to get a new binary for that particular machine.

Primitive Data Type—A data type which can be directly manipulated by the hardware. With Series 32000, these are integers, floating-point numbers, Booleans, BCD digits, and bit fields.

Procedure—A subprogram which performs a particular function required by a module, i.e., by a larger program; an ordered set of instructions that have a general or frequent use.

Process—A task.

Program Base—Module Descriptor entry which points to the first instruction in the module being described.

Program Counter—CPU register which specifies the logical address of the currently executing instruction.

Protection—The process of restricting a software program's access to certain portions of memory using hardware mechanisms. Typically done at the operating system and page level.

PSR—Processor Status Register. A 16-bit register on Series 32000 CPU's which contains bits used by the software to make decisions and determine program flow.

Push—to write a datum to the top of a stack.

Quad word—Four words, i.e., 64 bits.

Queue—A First-In-First-Out data storage area, in which the data may be removed at a rate different from that at which it was stored.

Real Time—The actual time in human terms, related to a process. In a UNIX system, real time is total elapsed time, CPU time is the percent of time a process is actually in the CPU. Sys time is the time spent in system mode, and user time is the time spent in user mode.

Glossary (Continued)

Real Time Operating Systems—An operating system which operates with a known and predictable response time limit, so that it can control a physical event.

Record—A structured data type with multiple elements, each of which may be of a different data type, e.g., strings, arrays, bytes, etc.

Register—A temporary storage location, usually in the CPU, which holds digital data.

Relative Address—The number that specifies the difference between the base address and the absolute address.

Relocatable—In reference to software programs, this is code which can be loaded into any location in main memory without affecting the operation of the program.

Return Address—The address to which a subroutine call, interrupt or trap subroutine will return after it is finished executing.

Routine—A procedure.

Royalty—Royalty is money paid to the inventor for each item of product sold. A good analogy to use is the music business. Any time a song is used, the songwriter is paid a royalty. Think of UNIX as a song and GENIX or SYSTEM V as special arrangements. For each shipment of GENIX or SYSTEM V, the customer pays a royalty to NSC who, in turn, pays a royalty to AT&T.

SB—In the Series 32000 Static Base Register. Points to the start of the static data area for the currently executing module.

Secondary Storage—This is generally slow-access, nonvolatile memory such as a hard-disk which is used to store the pages of software programs not currently needed by the CPU.

Segmented Address Space—Term used to describe the division of allocatable memory space into blocks of segments of variable size.

Setup Time—The minimum amount of time that data must be present at an input to ensure data acceptance when the device is clocked.

Slave Processor—A processor which cooperates with the main microprocessor in executing certain instructions from the instruction stream. A slave processor generally accelerates certain functions which increases overall system throughput. Examples of slave processors are the FPU and MMU of Series 32000.

Software—Programs or data structures that execute instructions or cause instructions to be executed and that will cause the computer to do work.

Software License—NSC does not sell software. Rather, we license the right to use our software. A software license is required for all Series 32000 software. We use the license to protect NSC's interests and to assist in honoring our commitment to AT&T. The license is also the vehicle which we use to track customers so that updates can be issued in a timely manner.

Software Q/A—It is the charter of the Quality Assurance people to ensure that when a software product reaches the customer that it is "bug" free. In the real world, it is impossible to test every combination of functions, so some bugs do get through. The Q/A engineer develops test programs which rigorously test the product prior to its introduction to the market place.

SP1—In the Series 32000, User Stack Pointer. Points to the top of the User Stack and is selected for all stack operations while in User Mode.

SP0—In the Series 32000, Interrupt Stack Pointer. Points to the top of the interrupt stack. It is used by the operating system whenever an interrupt or trap occurs.

Stack—A one-dimensional data structure in which values are entered and removed one datum at a time from a location called the Top-of-Stack. To the programmer, it appears as a block of memory and a variable called the Stack Pointer (which points to the top of the stack).

Stack Pointer—CPU register which points to the top of a stack.

Static Base Register—A 32-bit CPU register which points to the beginning of the static data area for the currently executing module.

String—An array of integers, all of the same length. The integers may be bytes, words, or double words. The integers may be interpreted in various ways (see ASCII).

Subroutine—A self-contained program which is part of a procedure.

Symmetry—A computer architecture is said to be symmetrical when any instruction can specify any operand length (byte, word or double word) and make use of any address-data register or memory location while using any addressing mode.

Synchronous—Refers to two or more things made to happen in a system at the same time, by means of a common clock signal.

Tag—A label appended to some data entry used in a look-up process whereby the desired datum can be identified by its tag.

Task—The highest-level subdivision of a user software program. The largest program entity that a computer's hardware directly deals with.

TCU—Timing Control Unit. A device used to provide system clocks, bus control signals and bus cycle extension capability for Series 32000.

Trap—An internally generated interrupt request caused as a direct and immediate result of the encounter of an event.

T-State—One clock period. If the system clock frequency is 10 MHz, one T-State will take 100 ns to complete. Operations internal and external to the CPU are synchronized to the beginning and middle of the T-States. There are four T-States in a normal Series 32000 CPU bus cycle.

Glossary (Continued)

UNIX™—An operating system developed at Bell Laboratories in the early 1970s. Software programs that run under UNIX are written in the high-level language C, making them highly portable. UNIX systems do not distinguish user programs from operating system programs in either capability or usage, and they allow users to route the output of one program directly into the input of another. This operating is unique and is becoming very popular in the microcomputer world.

USENET—A net to which UNIX systems in the United States connect. Some systems in Europe and Australia also use this net for the purpose of passing information.

User—A software program. The total set of tasks (instructions) that accomplish a desired result. Tasks are managed by the operating system.

User Mode—Machine state in which the executing procedure has limited use of the instruction set and limited access to memory and the PSR.

uucp—Software which allows UNIX computers to pass information to other UNIX systems.

Variable—A parameter that can assume any of a given set of values.

Vector—Byte provided by the ICU (Interrupt Control Unit) which tells the CPU where within the Descriptor table the descriptor is located for the interrupt it has just requested.

Virtual Address—Address generated by the user to the available address space which is translated by the computer and operating system to a physical address of available memory.

Virtual Memory—The storage space that may be regarded as addressable main storage by the system. The operating system maps Virtual addresses into physical (main memory) addresses. The size of virtual memory is limited by the method of memory management employed and by the amount of secondary storage available, not by the actual number of main storage locations, so that the user does not have to worry about real memory size or allocation.

VMS—This is the operating system designed by Digital Equipment Corporation for their VAX series of computers. The original Series 32000 software was developed on a VAX which was being controlled by the VMS Operating System.

Wait-State—An additional clock period added to a CPU memory cycle which gives an external memory device additional time to provide the CPU with data. Also used by bus arbitration circuitry to hold the CPU in an idle state until access to a shared resource is gained.

Winchester—Small, hard-disk media commonly found in personal computers.

Word—A character string or bit string considered as the primary data entity. For historical reasons, a word is a group of 16 bits in Series 32000 systems.

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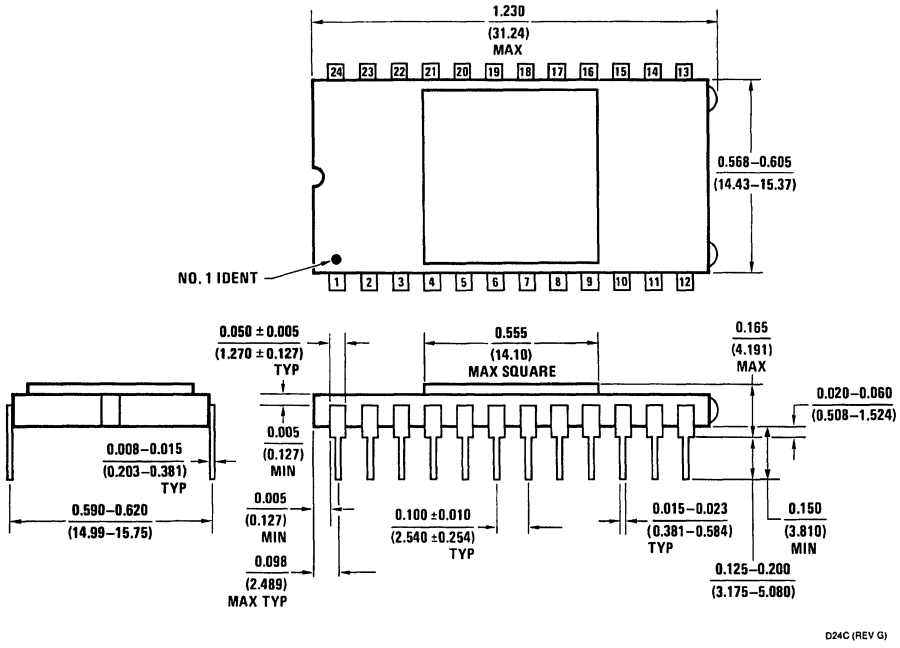

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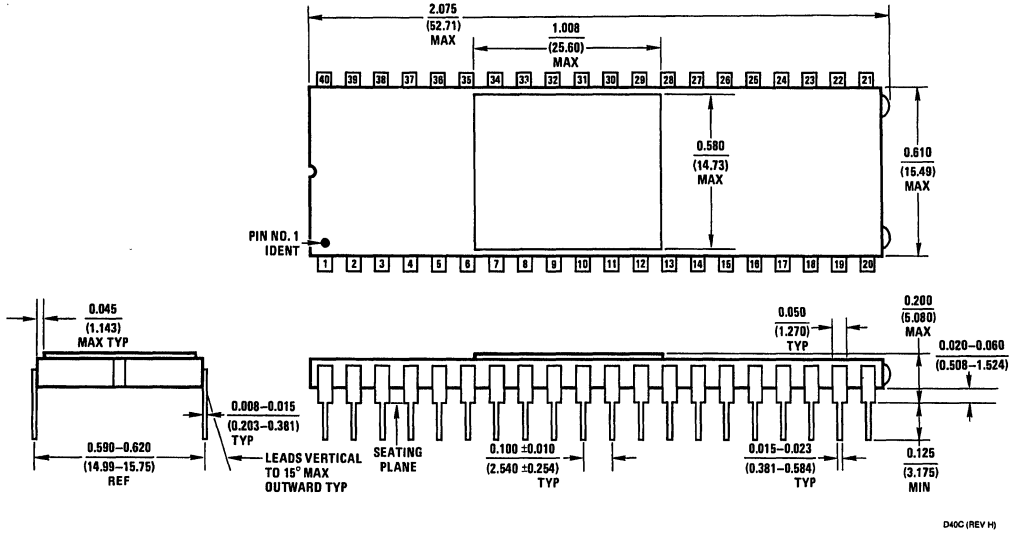

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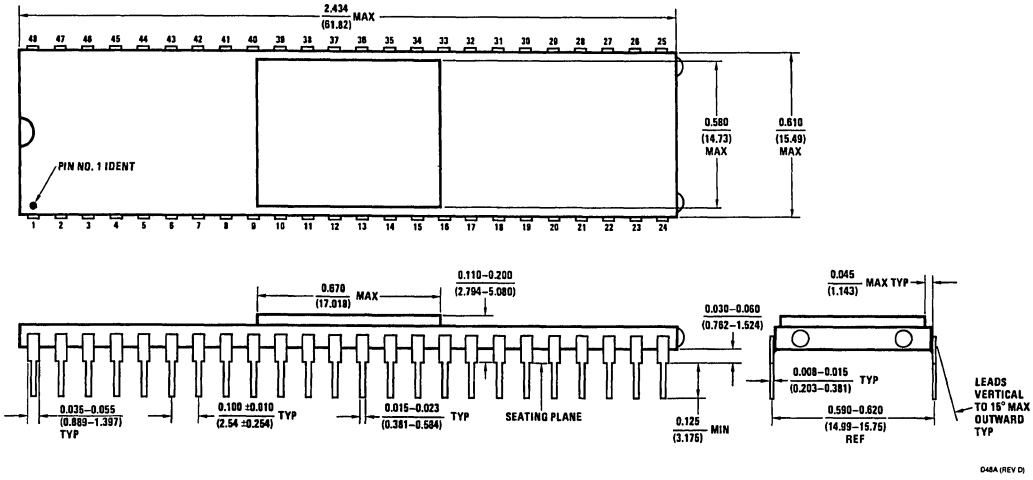

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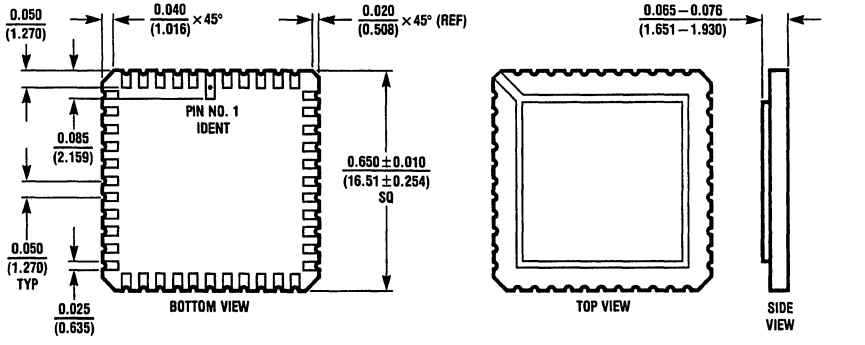

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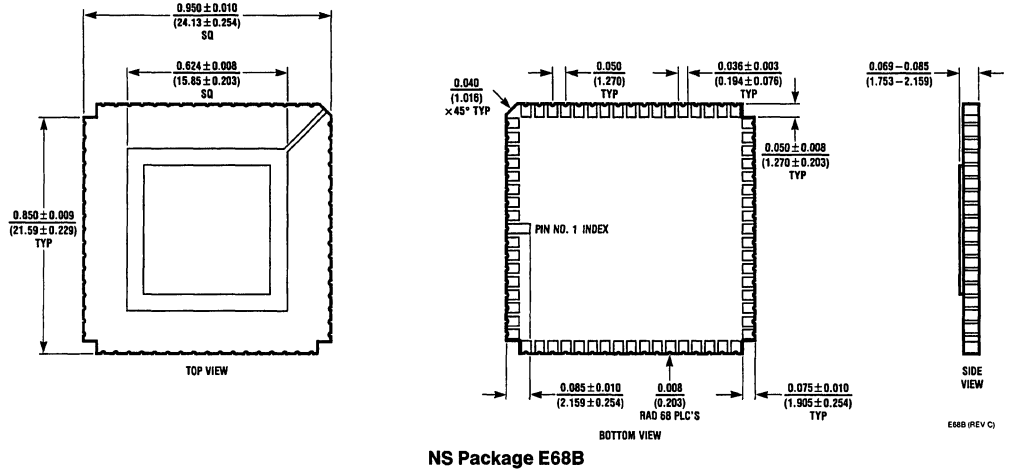

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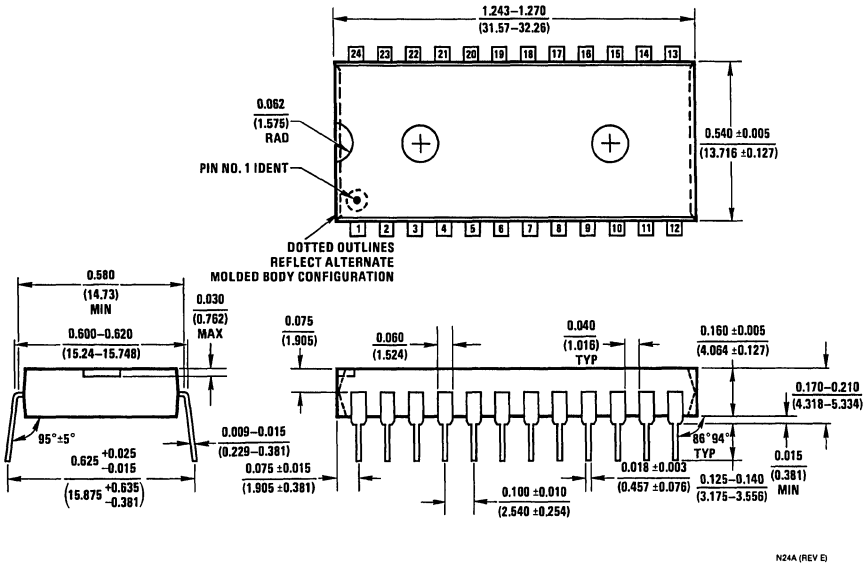

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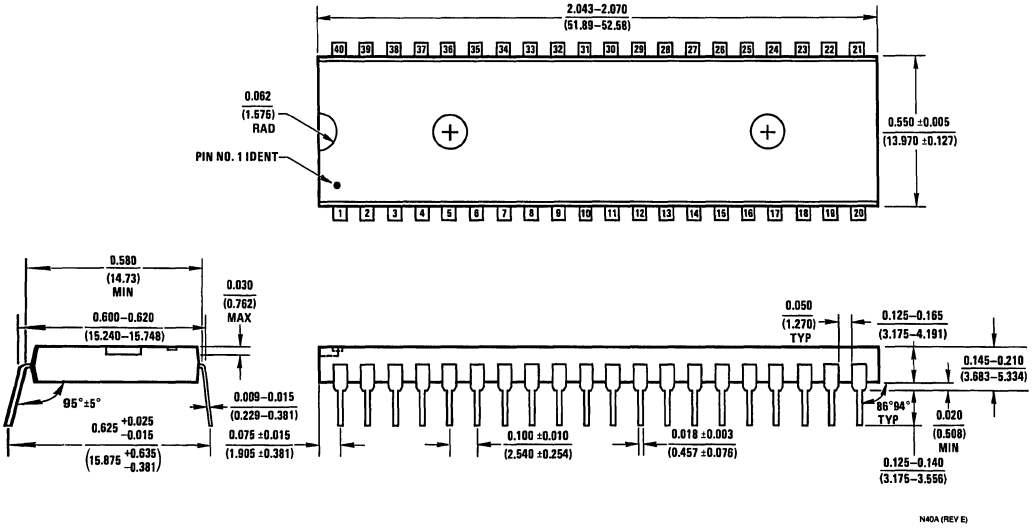

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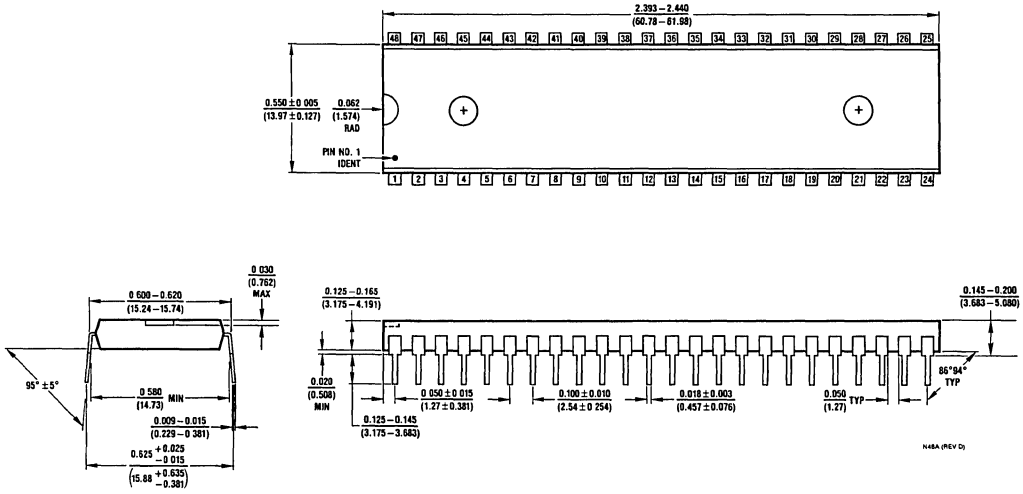

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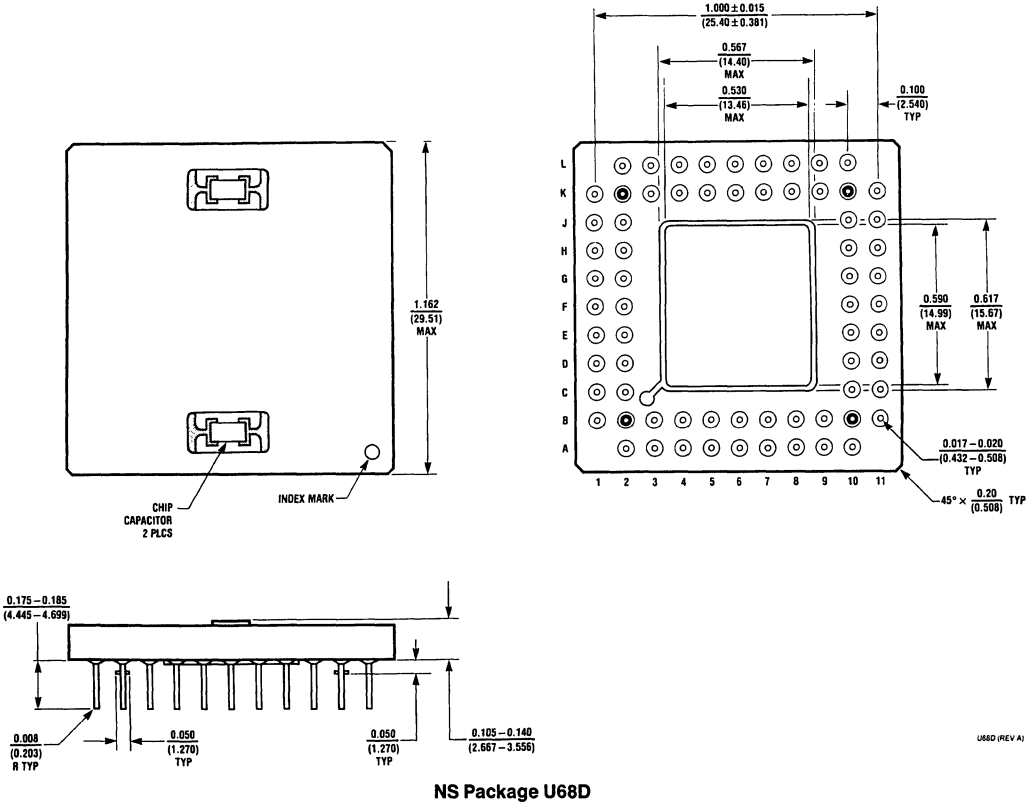

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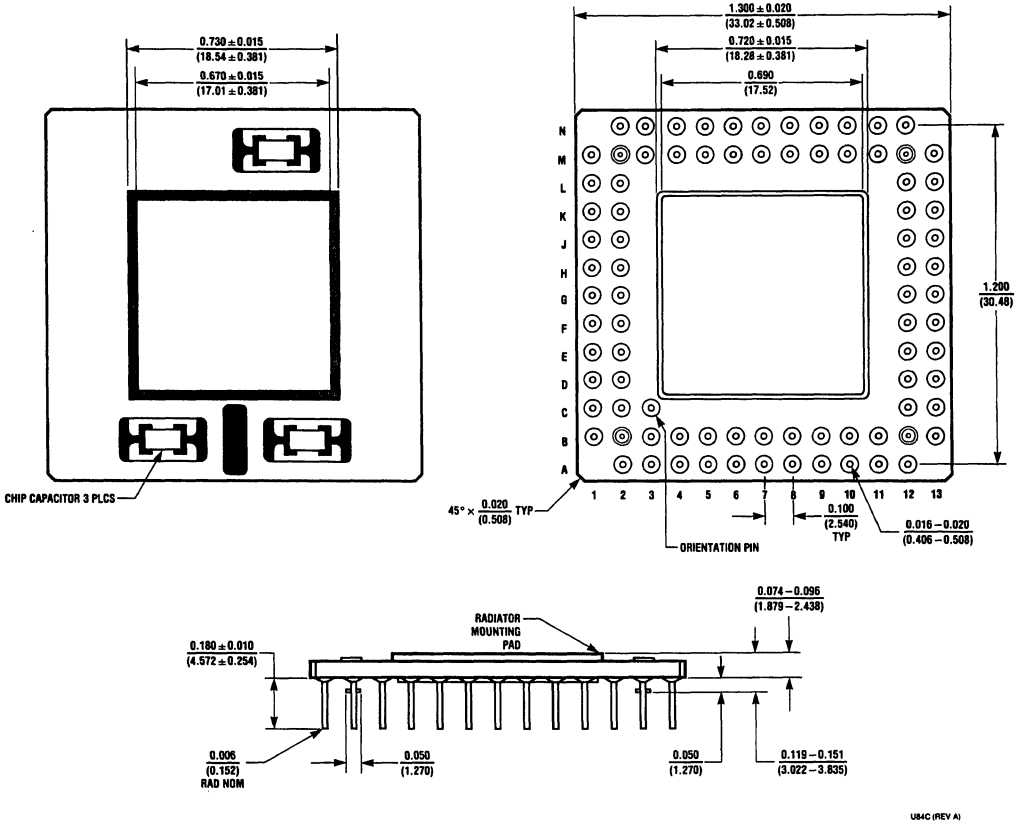

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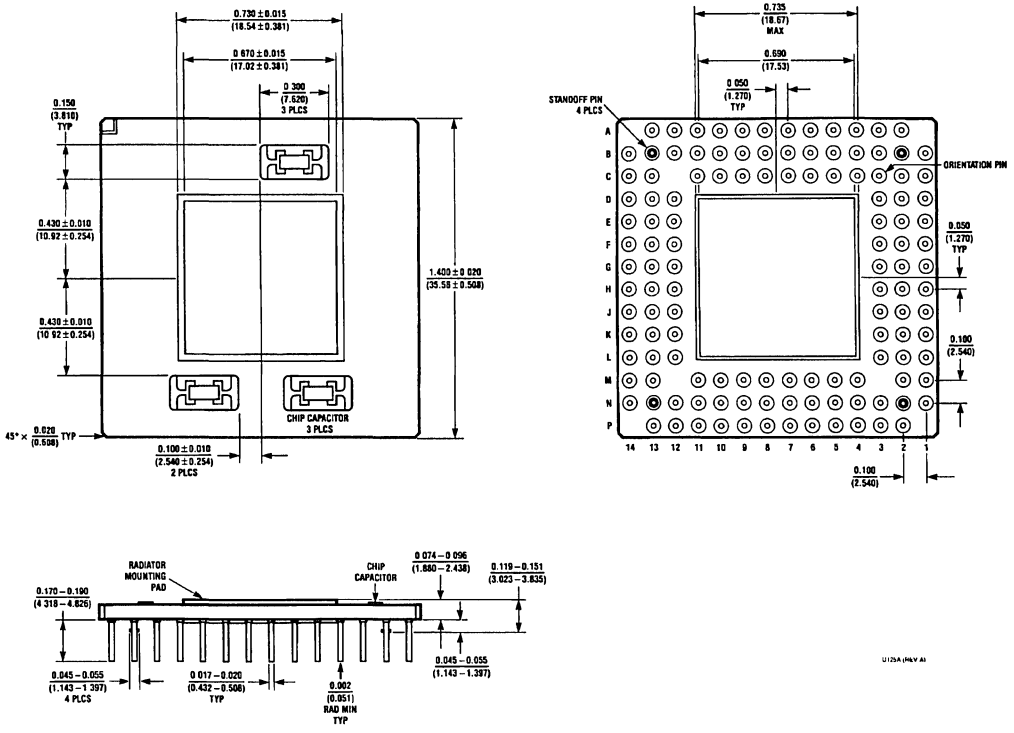

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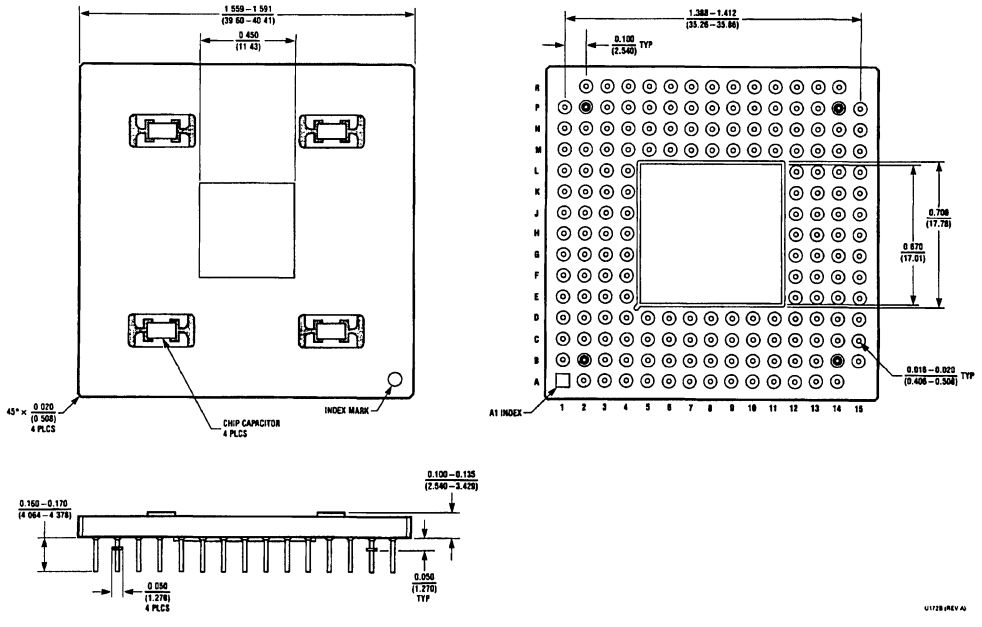

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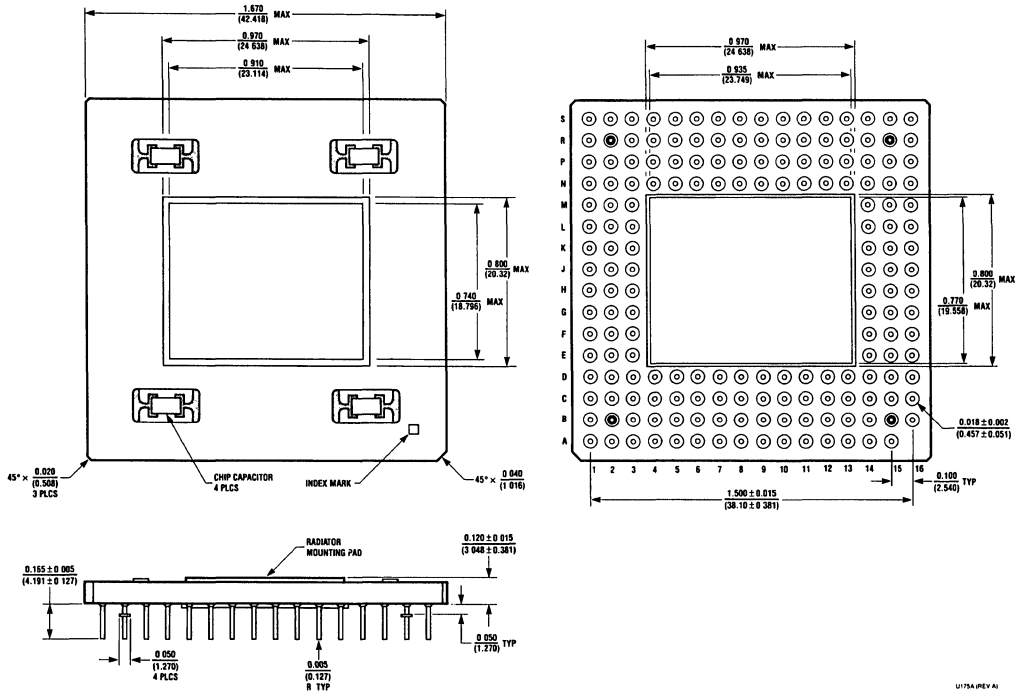

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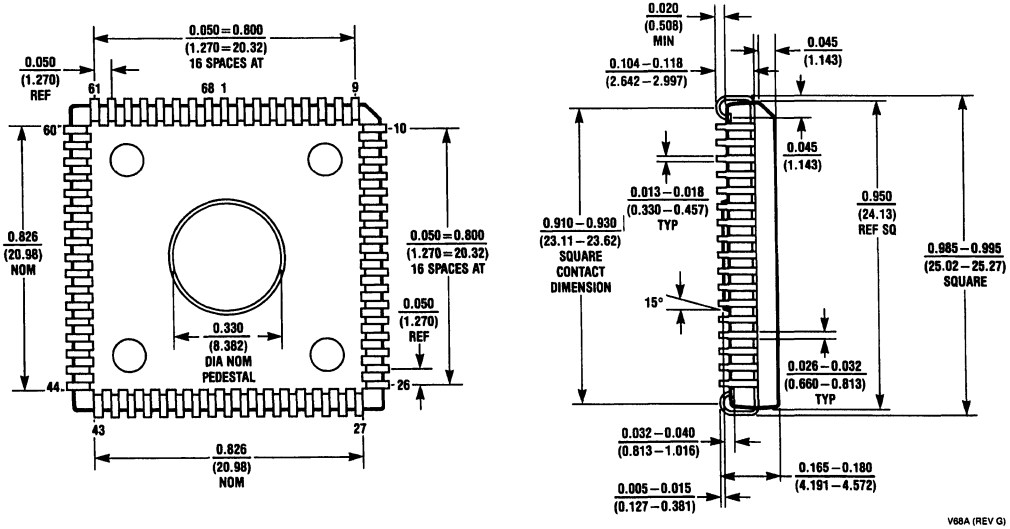

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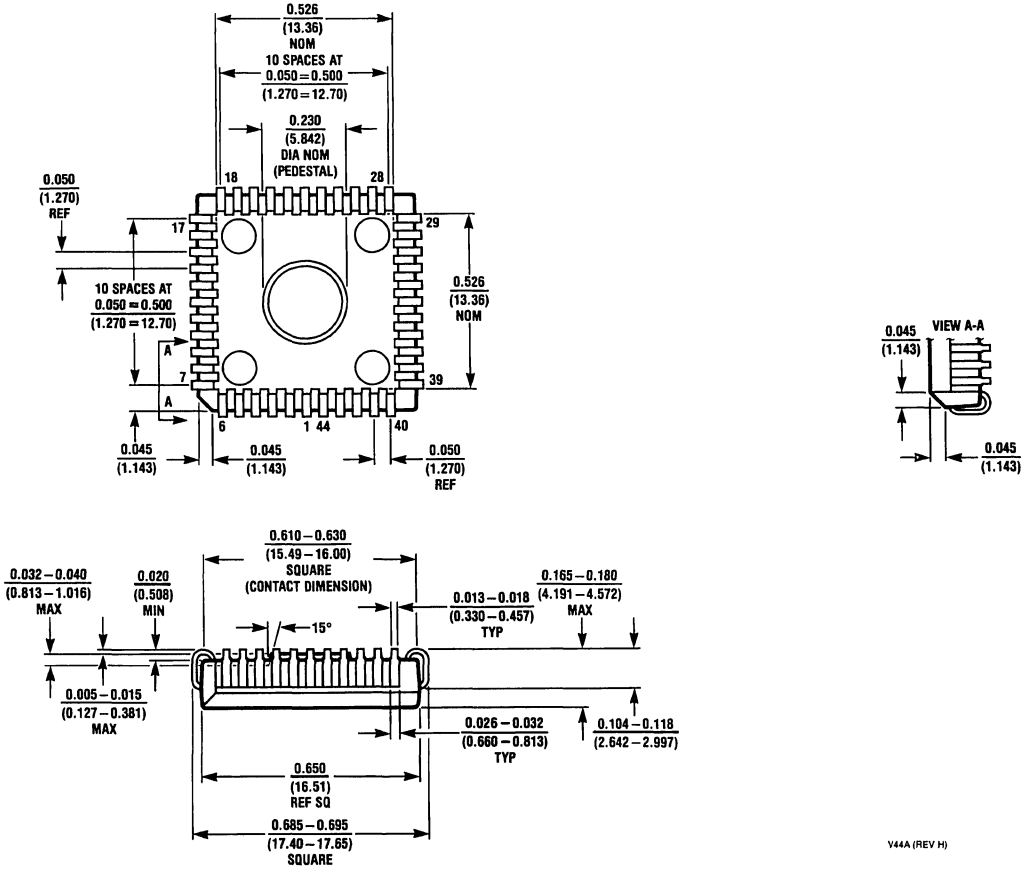

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