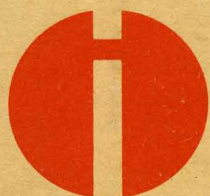# Olympia Service

The Better Service
The Higher Reputation
The More Favorable Sales

PEOPLE

Funktionsbeschreibung
Description of function
Description de fonctionnement
Descripción de Funciones

Olympia International

People

HARDWARE
MANUAL

Mai 1983

CONTENT

People

1. GENERAL

1. GENERAL

1.1 General Information

People is based on a 8086 CPU with basically a total of 264 KB of RAM-Memory, two Floppy Disk Drives, a typewriter style keyboard, several interfaces and various options like, disk extension, RS232C-extension, GPIB-interface, memory extension.

It's designed to be a field-upgradable system. It basically consists of three units: the main unit, the keyboard, the CRT, extensions may be housed separately. People is designed for applications such as data processing, office accounting and word processing. It also can handle educational, scientific, technical problems and also process control applications.

It is designed to be used by untrained people. There are no special installation requirements, it operates under the following conditions:

- Operating temperature   +5°C to +40°C
- Humidity   20% to 80%
                            (without condensation)
- Storage temperature   -22°C to +47°C
- Resistance against   5KV
  electrostatical discharges
  (Condenser method)

1.2 Configuration

PEOPLE has a 16-bit CPU (8086), with 256 KW RAM as the main memory and it is provided with a boot ROM (2732A) for program loading when power is switched on or REST operation, this having a capacity of up to 4Kwords. The peripheral control elements of the CPU include timer controller 8253 and interrupt controller 8259A. The following can be connected to PEOPLE:

(1) Floppy disk drive unit (5 1/4 inch type) 2 decks

(2) Micro disk

(3) CRT display (monochrom)

(4) CRT display (color)

(5) Printer (parallel I/F) Centronics specification

(6) RS232C I/F 3 channels

(7) Keyboard

(8) GPIB I/F

1.3 BUS CONNECTION

The CPU and the peripheral devices are connected together via data and address buses. The bus connection for PEOPLE appears in Fig. 1.3.1.
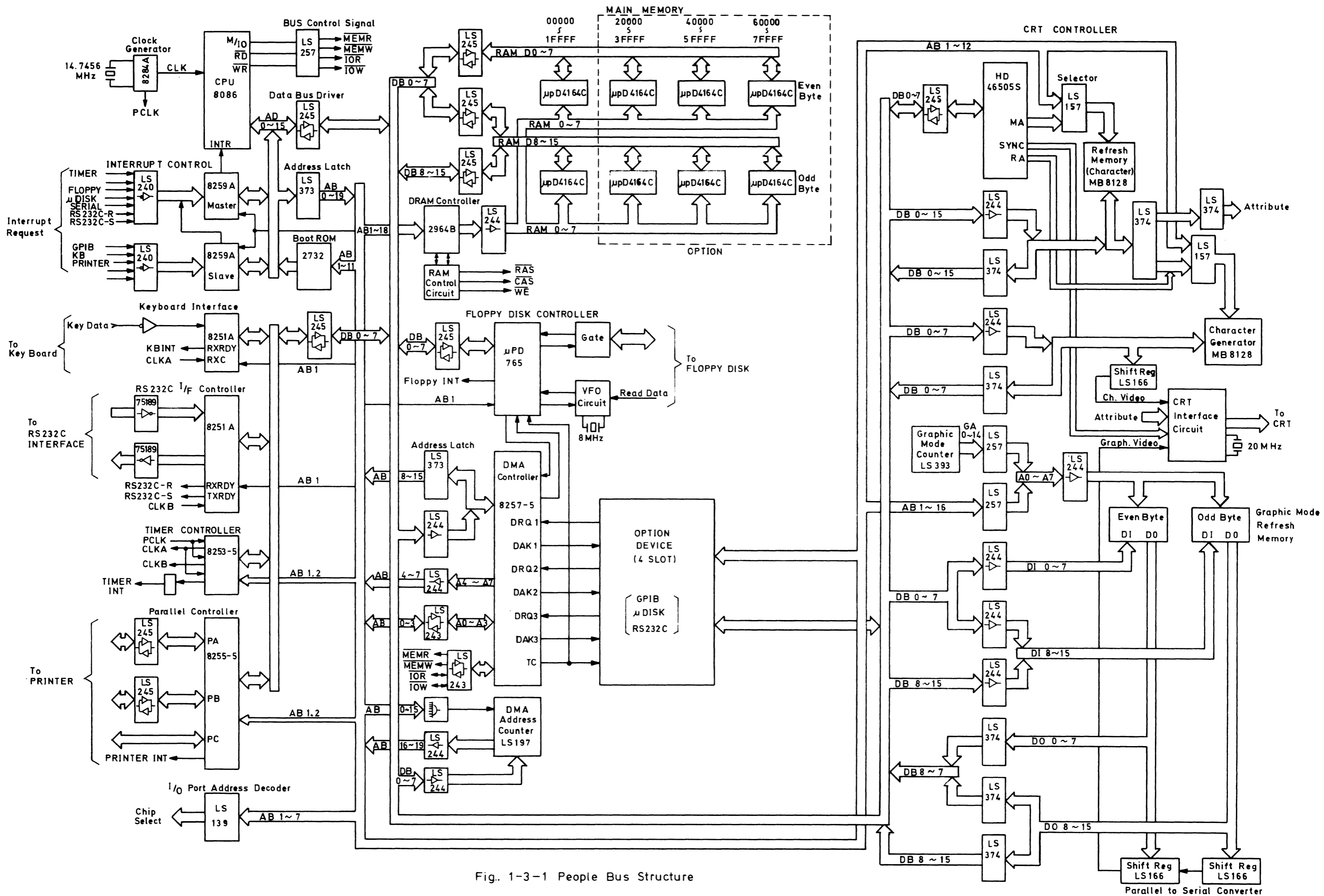
Fig. 1-3-1 People Bus Structure

OLYMPIA
PEOPLE

**Appendix
Part C/1-1**

The installation and environmental stipulations

The system contains a variety of measures designed to ensure the serviceability at all times, with particular attention being paid to the influence of factors such as power cuts and defects due to static discharge.

The installation and environmental stipulations listed have been compiled so as to ensure the maximum possible freedom of interference from external sources.

Connection to the local power supply

The design of the machine corresponds with the international radio interference suppression regulations.

However, due to the fact that not all electrical appliances on the market comply with such regulations, the system should only be connected to circuits to which other appliances are connected which comply with such regulations. Within the Federal Republic of Germany, such appliances bear the interference suppression symbol of the VDE or the FTZ test number of the Federal Postal Authorities.

Variations of the power supply

In order to ensure the correct functioning of the system, the voltage and frequency of the power supply to which the system is connected should not exceed the following variations :

Voltage   :   + 10   -   15%

Frequency   :   +/-   1%

The system is not affected by brief voltage variations up to a maximum of 2000 V, pulse widths of up to 300 ns or rise times of up to 5 ns.

In the event of the possibility of variations of the voltage occuring due to the connection of other appliances, either a voltage regulator or supplementary filter should be incorporated in the circuit.

Point of installation

The system should be set up at spots not subject to vibration, dampness and dust, as well as away from direct sunlight and/or radiators.

In connection with the above, the following stipulations must be complied with :

The angle of inclination of the system should not exceed 2°

Vibration during operation should not exceed
10 - 100 Hz 0.2 g

Vibration during transit should not exceed
10 - 100 Hz 2 g

Environmental temperature :

In operation :   between 5° and 40° C

In storage   :   between $- 22^{\circ}$ and $+ 47^{\circ}$ C

Relative humidity :   between 20 and 80 %

On no account should the ventilation slots of the system be covered in whatever manner, either by the documents or by being partially masked by office furniture.

Those cables connected externally to the system must be protected against damage and as well as being arranged to prevent possible tripping.

Electrostatic charging

Factors which influence electrostatic charging are the relative humidity, the material of the floor covering, wall to wall carpeting, and the soles of shoes, the material of the cushioning of chairs and the dress of the operator.

The systems are protected against defects brought about by electrostatic discharge within normal limits.

People

2. CPU AND PERIPHERALS

2. CPU AND PERIPHERALS

2.1 CPU

PEOPLE uses the 8086 CPU.

2.1.1 Use

(1)	Operation clock	4.9152 MHz
(2)	Mode	Minimum mode

Usually the RAM Read/write operations involve one wait each. Then CPU Cycle time is 1 μS.

2.1.2 The CPU

2.2 Clock Generator 8284A

2.4 Reset Circuit

This circuit outputs reset signals if the reset switch behind the main cabinet is pressed. When the reset circuit becomes active, the system program is read from the system disk, if it is mounted on floppy disk drive, and is then stored to the memory. This is known as initialization.

2.5 Bus Control Signal

Bus control signals include the memory read signal (MEMR), memory write signal (MEMW), I/O read signal (IOR), and I/O write signal (IOW). These signals control the timing of the opening and closing of the data bus for memory read/write, and I/O read/write operations.

2.6 WAIT CIRCUIT

When the CPU accesses memory or the I/O, this circuit generates the Wait signal to match CPU operation speed with the memory or I/O operation speed.

2.6.1 Circuit Configuration

Bus control signal
generating circuit

READ signal
WAIT signal

$\overline{RD}$
$\overline{WR}$
$\overline{M/IO}$

READY

CLOCK
GENERATOR

CPU

ALE

CLOCK
Reset signal

WAIT
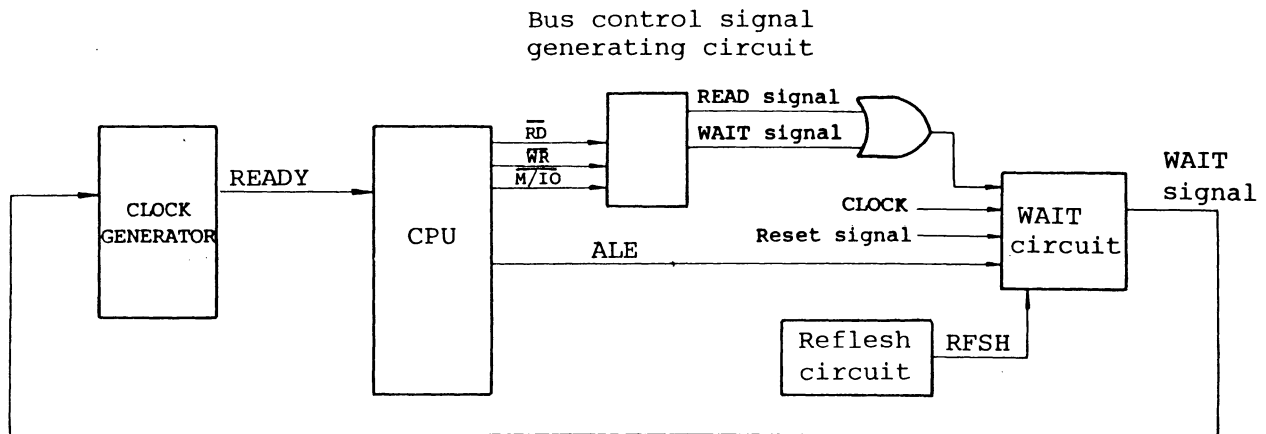circuit

WAIT
signal

Reflesh
circuit

RFSH

Fig. 2.6.1 Wait circuit

Operating speed of the I/O control IC is slower than the CPU's. Again, because of the refresh operation, the memory cycle time is slower than the CPU access time. When accessing the bus, therefore, the CPU requires one wait cycle.

2.6.2 RAM Access Timing

The main memory uses the dynamic RAM IC, making it necessary for the refresh circuit to refresh RAM periodically. The main memory is refreshed every time after a CPU memory access. However, if the next CPU memory access does not take more than 3.5μ sec, the next refresh cycle starts. In this case, CPU memory access and refresh operation may be over lapped. (Fig. 2.6.3).

2.6.2   Time Chart

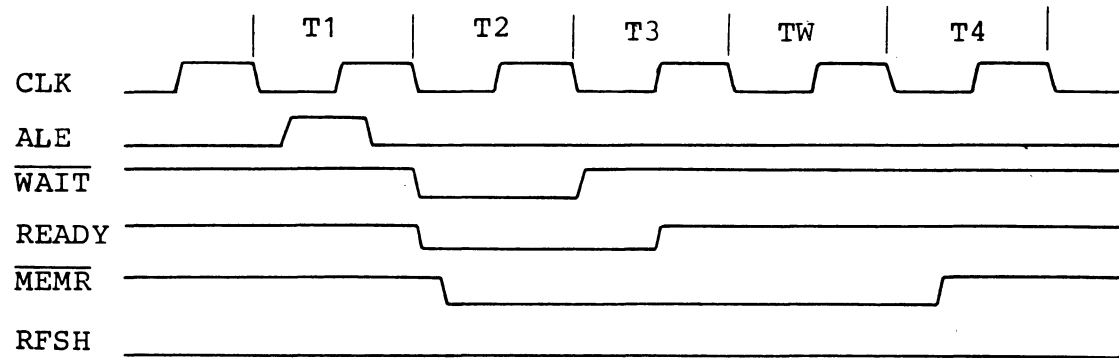(1)   If there is no contention between memory Ready/Write

and Refresh operations

	T1	T2	T3	TW	T4	

CLK

ALE

$\overline{\text{WAIT}}$

READY

$\overline{\text{MEMR}}$

RFSH

Fig. 2.6.2

(2)   If there is contention between memory Read/Write

and Refresh operations

	T1	T2	T3	TW	TW	T4	

CLK
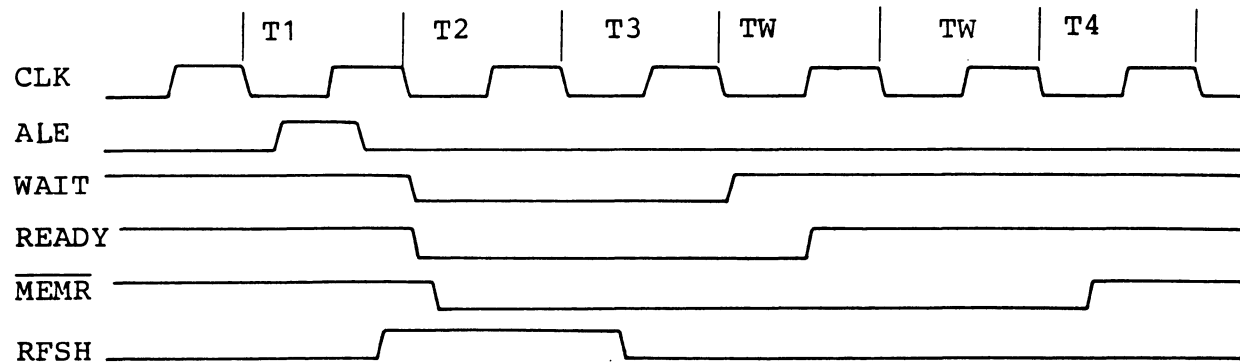
ALE

WAIT

READY

$\overline{\text{MEMR}}$

RFSH

Fig. 2.6.3

2.7 Interrupts

The interrupt signals are fed to the CPU via interrupt controller 8259A. When the CPU receives the interrupt signals, it sends the corresponding response signal (INTA) to 8259A.

When 8259A receives INTA, it sends an interrupt vector signal to CPU, according to the factor that caused the interrupt signal.

2.7.1 Interrupt Controller 8259A

2.7.2 Block Diagram

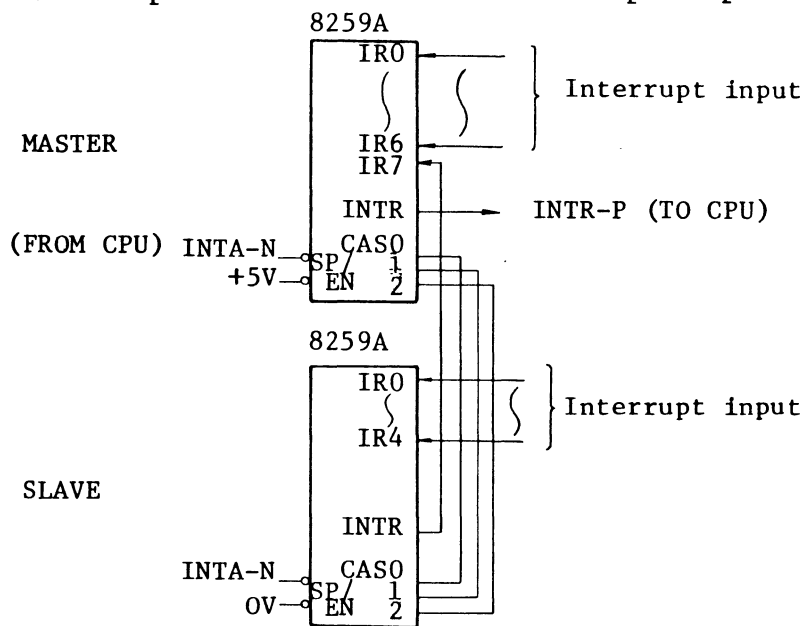PEOPLE uses two 8-level input interrupt controller 8259A for reception of 12-level interrupt inputs.

Fig. 2.7.1 Interrupt circuit block diagram

2.7.3 List of Interrupts

The factors causing interrupts in PEOPLE are listed in Table 2.7.1 according to their priorities.

Pri-ority	Signal name	Descripiton	Pri-ority	Signal name	Description
1	$\overline{\text{TIMER}}$	Timer interrupt	7	$\overline{\text{CCUS}}$	RS232C send
			8	$\overline{\text{GPINT}}$	GPIB interface
3	$\overline{\text{FDINT}}$	Floppy disk	9	$\overline{\text{KBINT}}$	KB interface
4	$\overline{\mu\text{INT}}$	Micro disk	10	$\overline{\text{PINT}}$	Parallel interface
5	$\overline{\text{CINT}}$	Serial interface	11	$\overline{\text{INTO}}$	Reserved
6	$\overline{\text{CCUR}}$	RS232C receive	12	$\overline{\text{INTI}}$	Reserved

Table 2.7.1 List of interrupts

2.8 I/O Port

The I/O ports in CPU are defined as follows:

Port No.	Device.	Output	Input
18H	8259A master		
1AH	"		
14H	8259A slave		
16H	"		
20H	8257	Channel 0 DMA address	
22H	"	Channel 0 Terminal counter	
24H	"	Channel 1 DMA address	
26H	"	Channel 1 Terminal counter	
28H	"	Channel 2 DMA address	
2AH	"	Channel 2 Terminal counter	
2CH	"	Channel 3 DMA address	
2EH	"	Channel 3 Terminal counter	
30H	"	Mode setting	
40H	8255	Data bus → port A	Port A → device
42H	"	Data bus → port B	Port B → device
44H	"	Data bus → port C	Port C → device
46H	"	Control word	
48H	8253	Loading counter 0	Reading from counter 0
4AH	"	Loading counter 1	Reading from counter 1

Port No.	Device	Output	Input
4CH	"	Loading counter 2	Reading from counter 2
4EH	"	Control word	
54H	8251		KB receive data
56H	"	Control data	Status data
5CH	"	RS232C send data	RE232C receive data
5EH	"	Control data	Status data
64H	μPD765		Status data
66H	"	Command data	
6CH	HD46505S	Address resister	
6EH	"	Data	Data
70H		Channel 0 DMA address, 4 high order bits	
72H		Channel 1 DMA address, 4 high order bits	
74H		Channel 2 DMA address, 4 high order bits	
76H		Channel 3 DMA address, 4 high order bits	
7CH		*1	RS232C status data
7AH			
80H	RESERVED		
⎰⎱			
8FH			

*1 2^0 = 1 Timer interrupt reset

2 = 1 Graphic mode 2 = 0 Character mode

2 = 1 CRT display inhibit

2 = 1 CRT color mode 2 = 0 Monochrome   mode

Table 2.7.1 Input-output port list

2.9 DMA

2.9.1 DMA Using Device

(1) Floppy disk interface   Channel 0

(2) GPIB interface (option)   Channel 1

(3) Microdisk interface (option)   Channel 2

2.9.2 DMA Controller

2.9.3 Address counter

The DMA controller 8257-5 has only 16-bit address counter. As a result, it can specify addresses within a 64KB memory space. On the other hand, 8086 can access a memory space of up to 1MB. Thus, a 4-bit counter must be added to 8257-5 to achieve a total of 20 bits.

For each DMA channel, a 4-bit address counter is added, making it possible to specify any address within the 1MB memory address range.
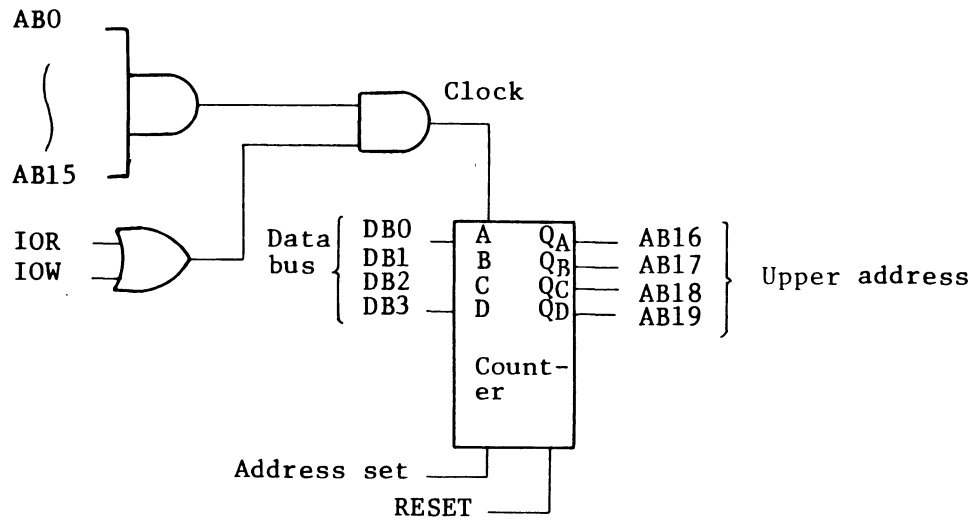

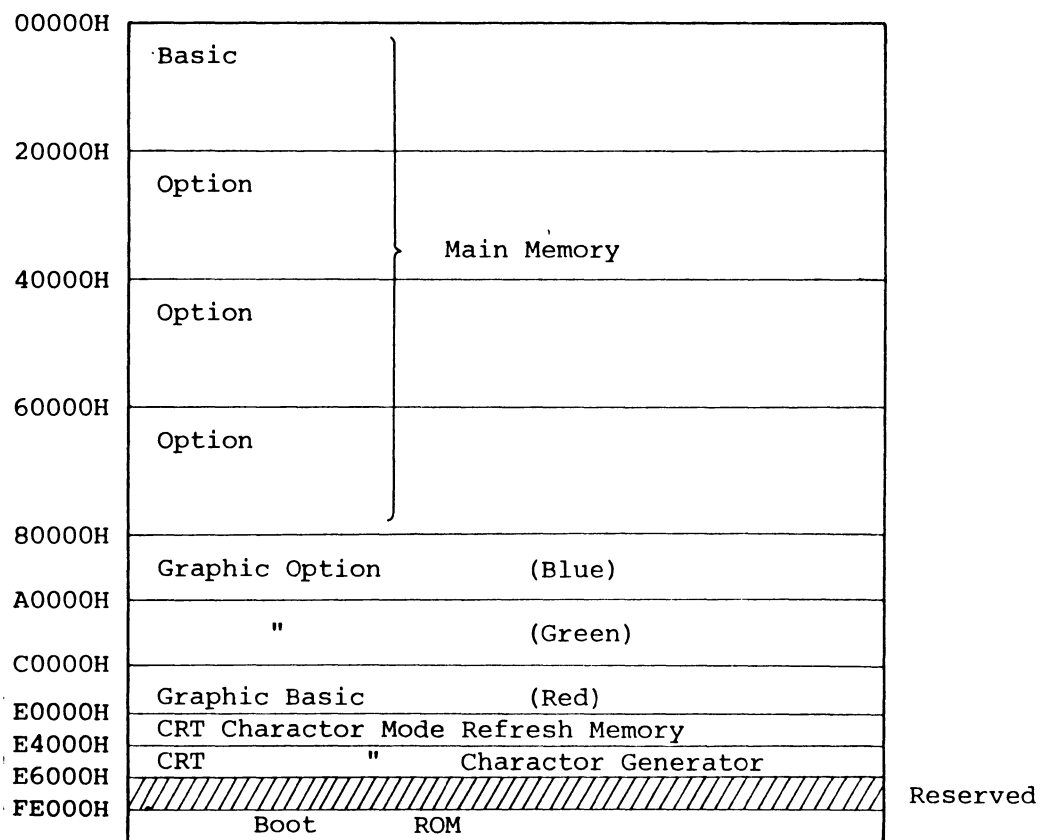Fig. 2.9.1   Address counter circuit

3.   MEMORY

3.   MEMORY

3.1   TYPE, CAPACITY

PEOPLE uses the following memory:

Type	IC	Capacity	Access time
Boot ROM	2732	4 kW	350 nS
Main Memory	µPD4164	Max 256 kW	200 nS
Character generator	MB8128	4 kB	100 nS
Refresh memory (for character mode)	MB8128	2 kW	100 nS
Refresh memory (for graphic mode)	MB8264	64 kW	100 nS

3.2 MEMORY MAP

Address	Content	
00000H	Basic	
20000H	Option	Main Memory
40000H	Option	
60000H	Option	
80000H	Graphic Option (Blue)	
A0000H	" (Green)	
C0000H	Graphic Basic (Red)	
E0000H	CRT Charactor Mode Refresh Memory	
E4000H	CRT " Charactor Generator	
E6000H	///////// Reserved /////////	
FE000H	Boot ROM	

3.3 MAIN MEMORY

Component of the main memory is a dynamic RAM IC having a capacity of 64K x 1 bits.

The OLP1 unit can be provided with a 128KByte memory and OLP3 with 128KBytes. The rest, that is 256 K Bytes, is provided through IC socket.

3.4 PRINCIPAL FEATURES OF DYNAMIC RAM

(1) Type   µPD4164C-2 or equivalent

(2) Access time   200 nS

(3) Refresh cycle   Max 2mS

3.5 DYNAMIC RAM CONTROLLER

The dynamic RAM controller is Am2964B.

The main functions of this controller are detailed

below:

(1) Dividing the 16-bit address bus line into 8 bits

each, and supplying these as, respectively, the ROW

and the Column addresses to the dynamic RAM.

(2) Controlling dynamic RAM refresh in response to

external refresh signals, using a built-in refresh

counter.

(3) Dynamic RAM controller 2964B

3.6 REFRESH CIRCUIT

Except during RAM Read or Write operations, the

refresh circuit controls refreshing of the dynamic memory

to prevent erasing of the RAM stored data. Refresh signals

are output by the refresh circuit, synchronizing them to

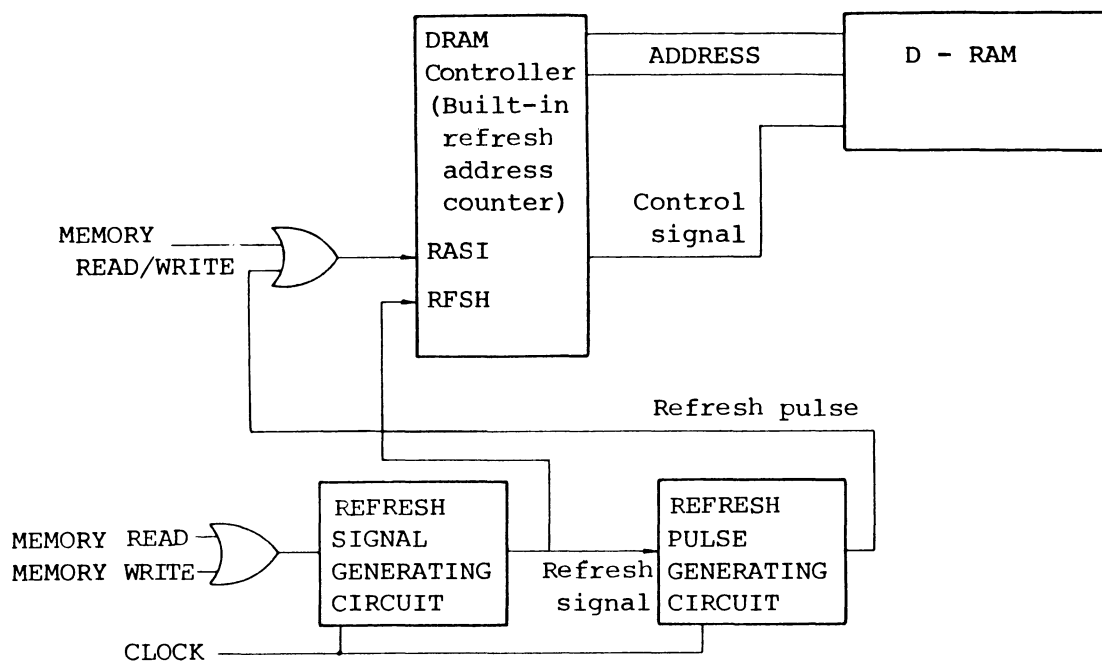the CPU DRAM access.

3.6.1 Circuit Block Diagram

Fig. 3.6.1   Refresh circuit block diagram

3.6.2 Time Chart

Unless the CPU is performing the Read/Write operation, the memory is refreshed successively at an interval of about 4 μs. When the CPU issues the Read or the Write signal, refreshing operation is stopped.

It starts again when the CPU ends the Read or Write operation.

4. KEYBOARD

4. KEYBOARD

4.1 KEYBOARD INTERFACE (KB)

A curled cord connects the PEOPLE's main cabinet and the keyboard. The interface specifications are listed below:

4.1.1 Specifications

(1) Signal names and terminal connections

Terminal number	Signal name	Function
1	RDATA-N	Key input data
2	GND	Signal ground
3	RESET-N	Keyboard reset
4	GND	Signal ground
5	GND	Power source (0V)
6	FG	Frame ground
7	+ 5V	Power source (+5V)
8	+ 5V	Power source (+5V)

Table 4.1.1 Keyboard connection

(2) Method of sending

The key input data is sent from the keyboard to the
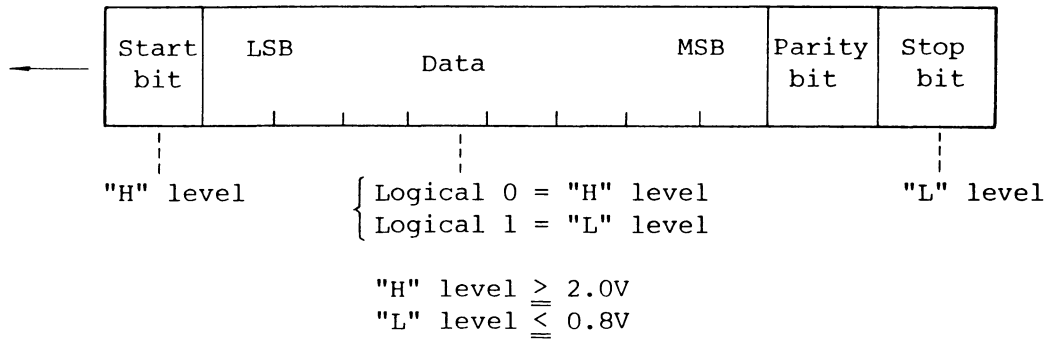mainframe controller according to the following
specifications:

(i)   Transmission rate   1200 BPS
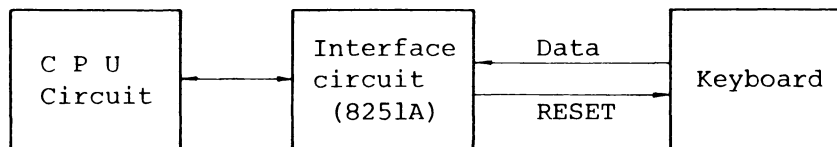
(ii) Synchronization method Start-Stop

(iii)   Transmission unit   11 bits

                                1 (start bit) + 8 (data bits) +

                                1 (even parity bit) + 1 (stop bit)

Start bit	LSB	Data	MSB	Parity bit	Stop bit

"H" level   Logical 0 = "H" level   "L" level
              Logical 1 = "L" level

              "H" level $\geq$ 2.0V
              "L" level $\leq$ 0.8V

(3) Connection block diagram

C P U Circuit	Interface circuit (8251A)	Data / RESET	Keyboard

(4) Operation

When 8251A receive 1 character (8 bits) of the serially sent keyboard data, it stores the data in the buffer register, and notifies the CPU (8086) about it by issuing an interrupt. Then the CPU receives the 8-bit keyboard data from the 8251A buffer.
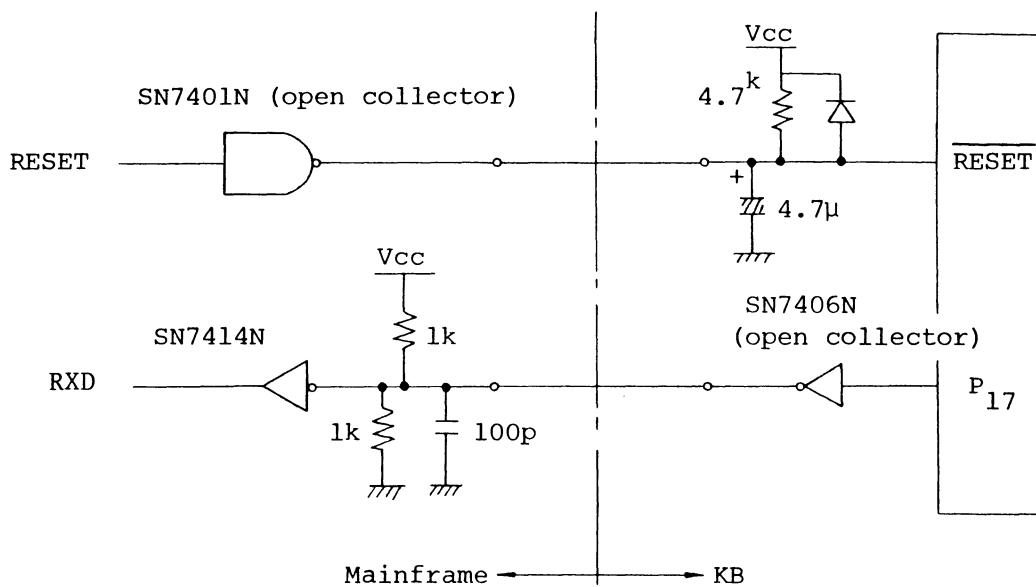
4.1.2 Interface Circuit
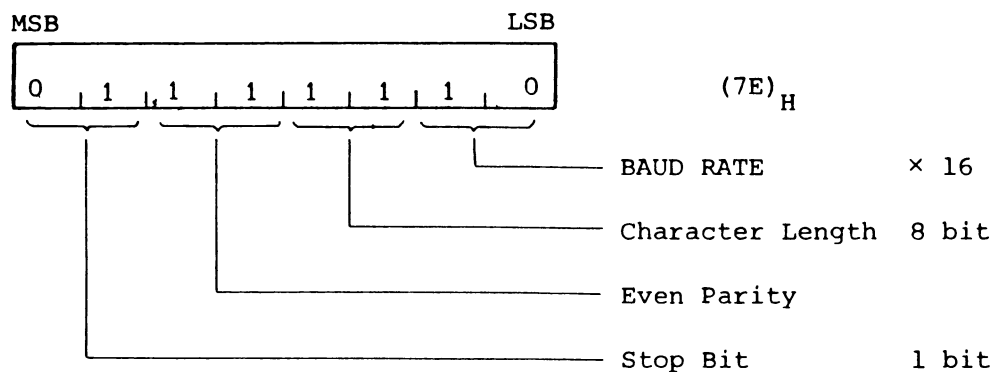

Fig. 4.1.1 KB Interface

4.2 MAINFRAME CONTROL CIRCUIT

4.2.1 Controller

The keyboard controller used for the mainframe is 8251A. This is a serial data communication controller

controlling data send and receive operations.

The operation modes in 8251A is programable. The mode

command, conforming to the keyboard interface, is (7E)$_H$.

```
MSB                              LSB
┌─────────────────────────────────┐
│ 0 ╷ 1 ╷ 1 ╷ 1 ╷ 1 ╷ 1 ╷ 1 ╷ 0 │     (7E)_H
└─────────────────────────────────┘
   └─────┘ └─────┘ └─────┘ └─────┘
      │       │       │       └──────── BAUD RATE        × 16
      │       │       └──────────────── Character Length  8 bit
      │       └──────────────────────── Even Parity
      └──────────────────────────────── Stop Bit          1 bit
```

The transmission rate is determined by (i) the frequency

of the clock pulses connected to the R×C terminal of

8251A, and (ii) Baud rate set for the mode commands

issued to 8251A.

Frequency of the clock* sent to the R×C terminal is

19.2kHz, Baud rate setting being ×16. Transmission

rate, therefore, is given by the following:

19.2 kHz ÷ 16 = 1.2 kHz

* The clock signal sent to the R×C terminal for the
  keyboard interface controller (8251A) is generated
  by the timer controller (8253). For the method of
  generation, see 9.3.

4.3 KEYBOARD CONTROL CIRCUIT

4.3.1 Overview

The keyboard uses a 1-chip microcomputer (8048). This microcomputer controls monitoring and encoding of the key inputs, and sending of the codes to PEOPLE mainframe.

4.3.2 8048

Microcomputer 8048 incorporates ROM and RAM. ROM stores the key code encode tables and the control program. The control program controls all the operations. RAM is used as the buffer for storing the input key codes. For its external interface, the microcomputer uses a 16-bit I/O port, to which two test bits are added. Furthermore, it has an 8-bit data bus. Of the 16-bit input port, $P_{10} \sim P_{13}$ (4bits) are used for row address of key matrix, P_{14} and P_{15} (2 bits) for shift control key, and P_{17} for send data output for PEOPLE mainframe. Test bits T_0 and T_1 are for ASCII lock key and CTRL key inputs. Data bus bits $DB_0 \sim DB_7$ are used for key matrix column data input.

4.3.3   Key Input Control

The 8048 output key matrix row addresses cyclically
thus: 0, 1, 2, ..., 15, 0, 1.   The row address
output at P_{10} ... P_{13} is decoded by the decoder driver
(SN74LS145N), one line (Y_i) alone being selected from
out of the 16 lines (Y_0...Y_{15}).   One of the terminals
of a maximum of eight keys is connected to a line.
The other terminal, divided into eight columns is
connected to the data bus of 8048 ($DB_0 \sim DB_7$).
If 8048 selects a line, status of a maximum of eight
keys connected to the line appears to the data bus.
Since 8048 reads this status, if it sequentially
outputs the line addresses corresponding to lines
0 $\sim$ 15 at $P_{10} \sim P_{13}$, and reads the contents of the
data bus, it can find out the status of the keys con-
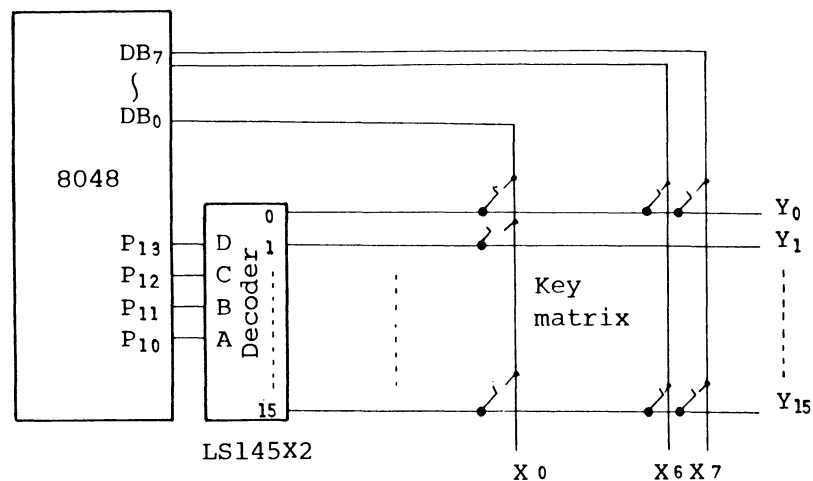nected to the 16 row 8 column matrix.

Fig. 4.3.1   KB BLOCK CHART

4.3.4 Key Input Code

Depending on its position, each key on the keyboard has an independent code. The key codes are shown in 4.3.6.

In its ROM, 8048 stores a table of these key codes. As described in 4.3.3, 8048 retrieves the code corresponding to this key from the table when the key is pressed, and stores it in the buffer.

4.3.5 Key Code Send Operation

From the buffer memory, 8048 sends the key codes to the CPU (PEOPLE mainframe) as a series of bits. Using the stored program, it sends data to conform to the specifications given in 4.1.1 (2). Terminal P_{17} of 8048 is the data outlet.

NOTE: The key codes are sent to the CPU as shown in table 4.3.1. These, however, are converted into other codes by the system program.

4.3.6 Key Codes

The key positions and the corresponding codes are shown below. For the key arrangement, see Fig. 4.3.6.

Key No.	Code	Key No.	Code	Key No.	Code	Key No.	Code
1	8E/8F*	24	38/28/28	47	53/73/13	70	2F/3F/2F
2	A4	25	39/29/29	48	44/64/04	71	SHIFT *4
3	90	26	30/20/20	49	46/66/06	72	CTRL *5
4	91	27	2D/3D/2D	50	47/67/07	73	A5
5	92	28	5C/7C/1C	51	48/68/08	74	B7
6	93	29	A0	52	4A/6A/0A	75	B8
7	94	30	A3	53	4B/6B/0B	76	B9
8	95	31	A1	54	4C/6C/0C	77	84/C4 *6
9	96	32	51/71/11	55	3B/2B/2B	78	83/C3
10	97	33	57/77/17	56	3A/2A/2A	79	B4
11	98	34	45/65/05	57	5D/7D/1D	80	B5
12	99	35	52/72/12	58	A2	81	B6
13	9A	36	54/74/14	59	SHIFT *4	82	AD
14	9B	37	59/79/19	60	5F/7F/1F	83	85/C5
15	9C	38	55/75/15	61	5A/7A/1A	84	B1
16	5E/7E/1E**	39	49/69/09	62	58/78/18	85	B2
17	31/21/21	40	4F/6F/0F	63	43/63/03	86	B3
18	32/22/22	41	50/70/10	64	56/76/16	87	A7
19	33/23/23	42	40/60/00	65	42/62/02	88	81// C1
20	34/24/24	43	5B/7B/1B	66	4E/6E/0E	89	B0
21	35/25/25	44	A6	67	4D/6D/0D	90	AE
22	36/26/26	45	SHIFT *** LOCK	68	2C/3C/2C	91	82//C2
23	37/27/27	46	41/61/01	69	2E/3E/2E		

All codes are in hexadecimal.

Table 4.3.1 KEY CODE TABLE

NOTE: *   Key No. 1 is the ASCII lock key codes as
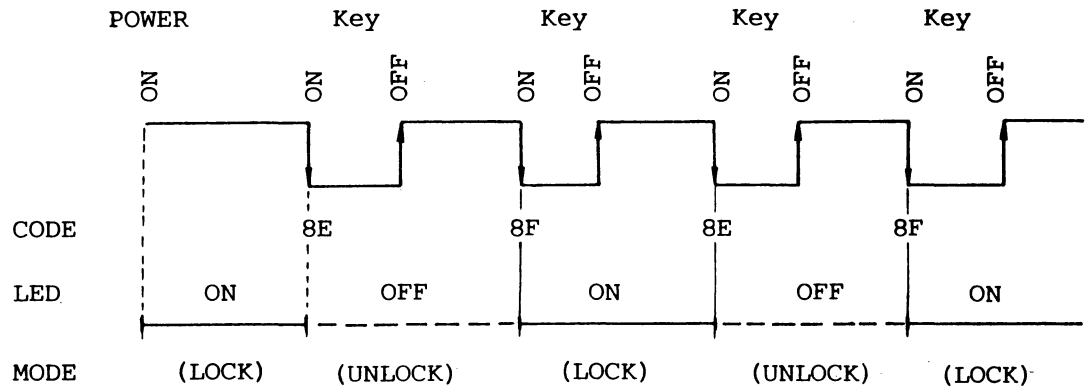
shown below:

Fig. 4.3.2   ASCII LOCK OPERATION

**   Keys marked A/B/C output three codes depending

on the shift status and the status (on/off)

of the control key.

NORMAL / SHIFT / CTRL (Shifted or Unshifted)

***   Key No. 45 is the shift lock. If pressed, this

key causes a   shift state unconditionally (LED

lights now).

*4   Keys 59 and 71 are shift keys. If pressed,

shift and unshift states alternate. If these

are pressed in the shift lock mode, the system

enters the unshift status.

*5 Key 72 is the CTRL key. If a key is pressed
    with key 72 held pressed, the code corres-
    ponding to the key is output in the CTRL mode.

*6 Keys marked A // B outputs codes in the CTRL
    mode if the CTRL key is pressed. Otherwise,
    they output codes in other modes (Normal Modes).
    Not CTRL // CTRL

4.3.7 Repeat Function

All code output keys (except the ASCII LOCK, SHIFT LOCK,
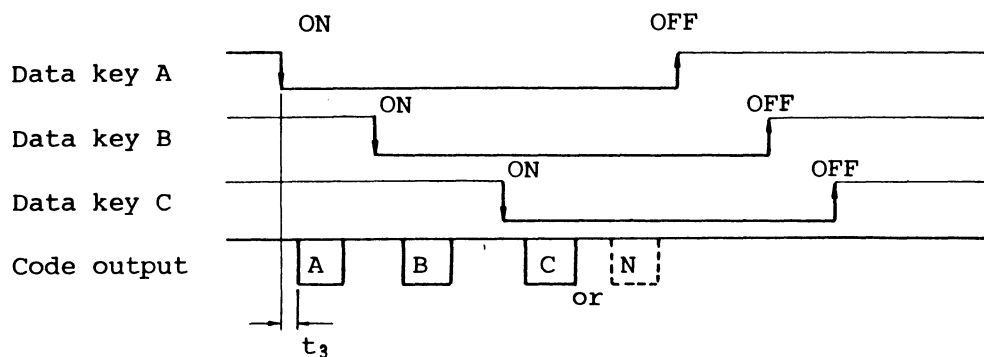SHIFT, AND CTRL keys) have the following repeat function.
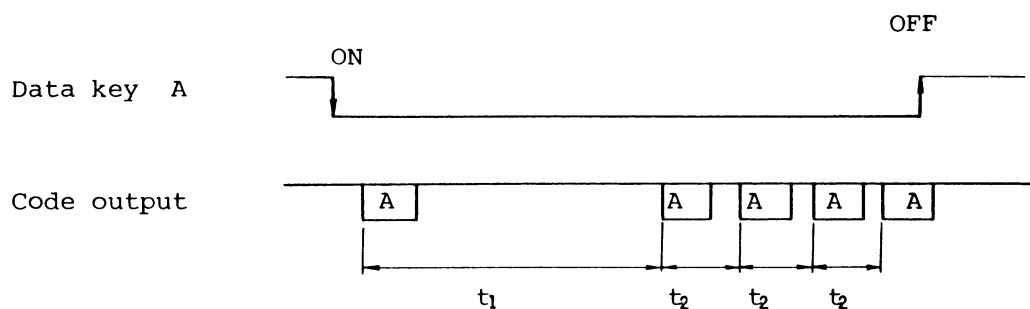
$$t_1 = 500 \pm 100 \text{ mS}$$
$$t_2 = 70 \pm 20 \text{ mS}$$

Fig. 4.3.3   REPEAT FUNCTION

4.3.8 N Key Roll Over


```
              ON                    OFF
Data key A  ___|‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾|_____

                   ON                    OFF
Data key B  _____|‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾|_____

                        ON                    OFF
Data key C  _____|‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾|___

Code output  | A |   | B |      | C |  ¡ N ¡
                                       └──┘
             |_                         or
           ─→| |←─
             t₃
```

If three keys are pressed together, an unspecified key code may be sent.

$$t_3 = 30 \text{ mS max}$$

Fig. 4.3.4   2 KEY ROLL OVER

4.3.9 Keyboard Layout

Fig. 4.3.5 shows the layout of the key tops (ASCII).

4.3.10 Key Matrix

Each key on the keyboard is assigned a number as shown in Fig. 4.3.6. The keys are wired in the form of matrix as shown in Table 4.3.2.
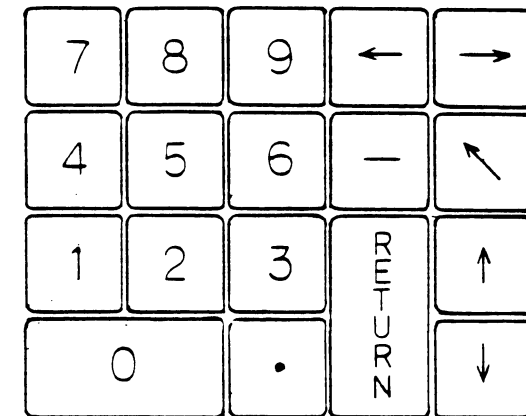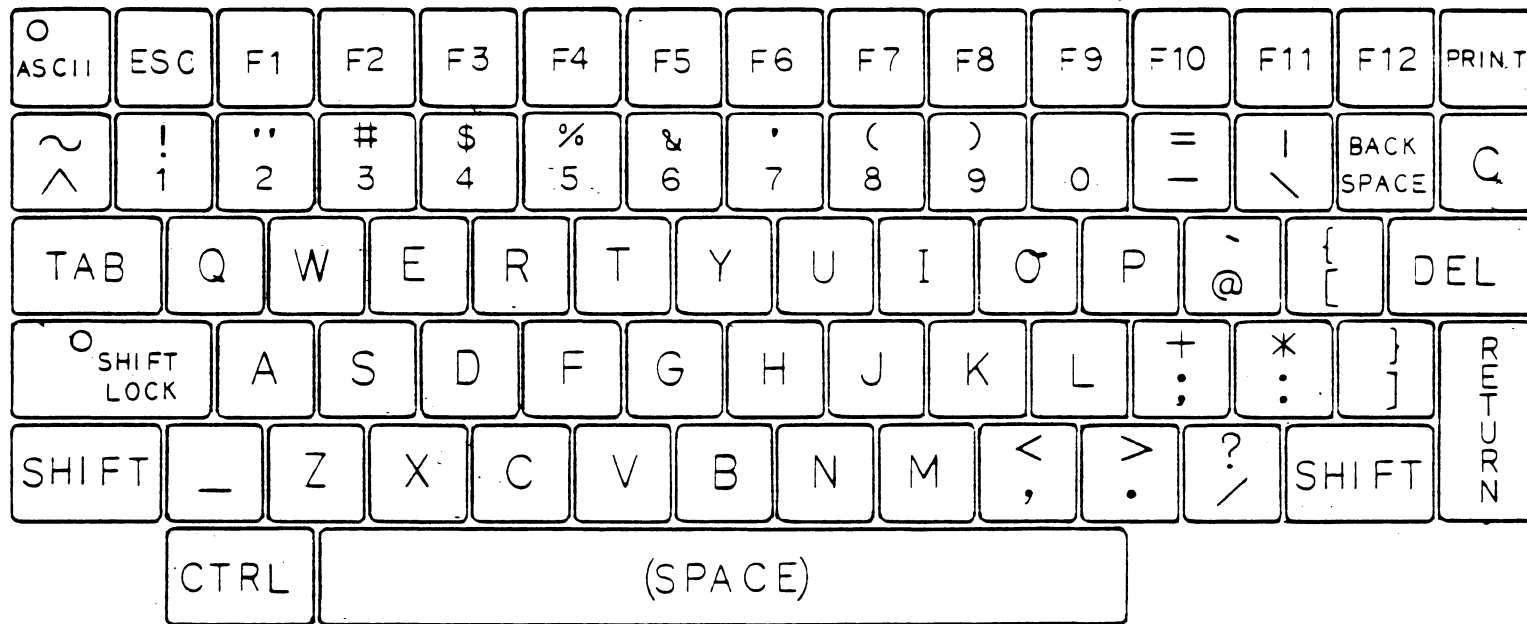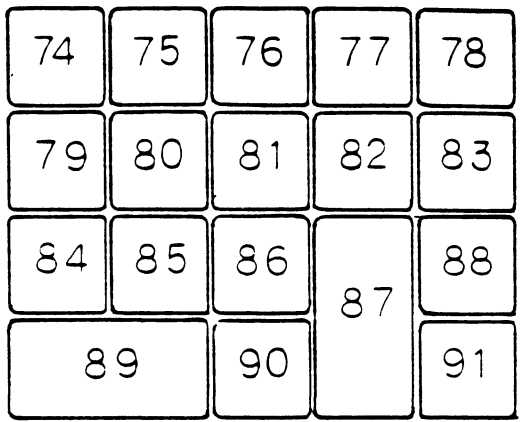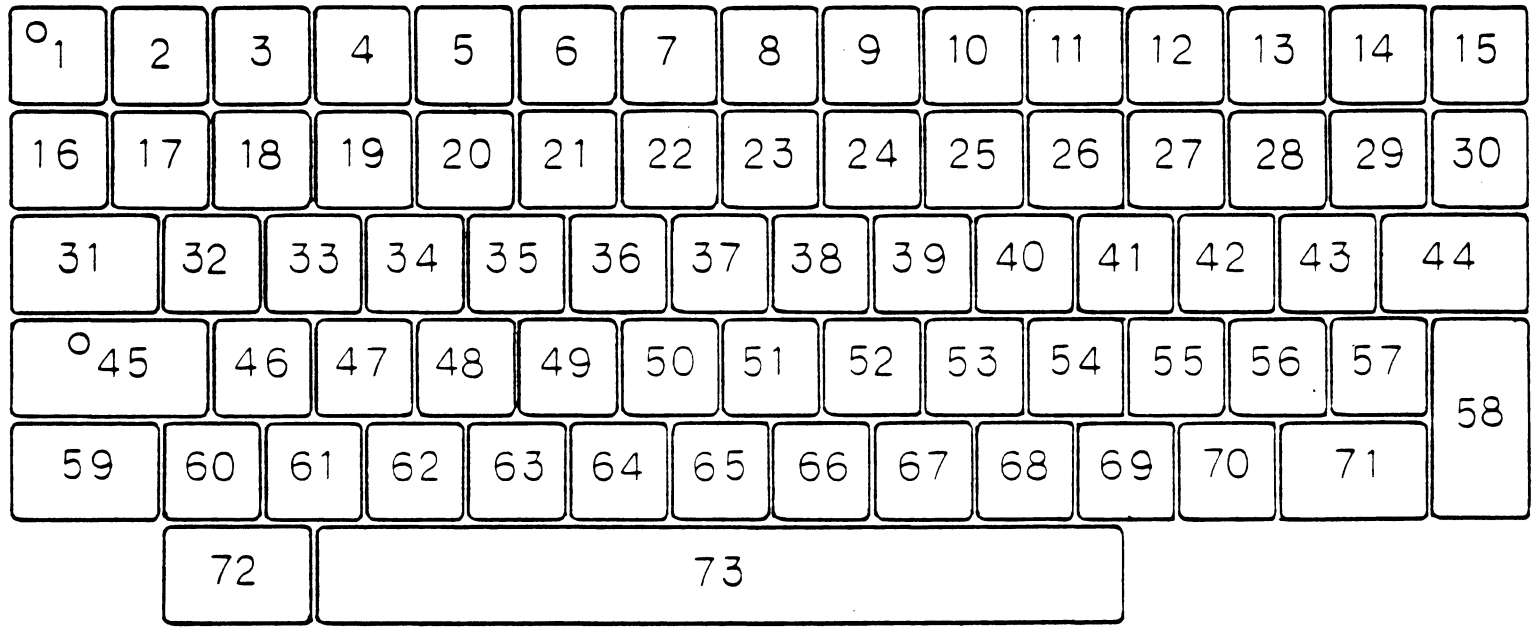
Fig4-3-5 KEY LAYOUT (ASCII)

Fig.4-3-6 KEY NO. & MATRIX

X\Y	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0																
1	77					78	91						82	83	88	87
2	80	79	76	75	74	81	90						84	85	86	89
3	70		58			69	68		60	61	62	63	64	65	66	67
4	55	56	57			54	53		73	46	47	48	49	50	51	52
5	41	42	43	44		40	39		31	32	33	34	35	36	37	38
6	26	27	28	29	30	25	24		16	17	18	19	20	21	22	23
7	11	12	13	14	15	10	9			2	3	4	5	6	7	8

People

5. CRT CONTROL

5. MONOCHROME CRT CONTROL SECTION

5-1 Overview

The CRT control section is connected to the monochrome CRT in the format explained in Section 5-6 and designed to control in the mode described in Section 5-2.

In the CRT control section, the CRT controller (CRTC) LSI (HD 46505SP) is used.

5-2 Control Mode

In the CRT control section, both the character mode (semigraphic mode) and the full-graphic mode can be specified.

5-2-1 Character mode

o One-cell configuration	8 dots x 19 dots
o One character configuration	7 dots x 15 dots
o One-screen configuration	80 cells x 25 cells
o Character generator mode	The character generator mode is specified in the character mode and the dot pattern of characters can be changed in programming. The patterns up to the maximum 128 can be stored in the character generator

o Attributes   Reverse for each cell

Brightness control for

each cell (4 phases)

Underline for each cell

(17, 18 lines fixed)

o Cursor   One-cell-painted mode

5-2-2 Full-graphic mode

o One-screen configuration   640 dots x 475 dots

There is no attribute and no cursor function.

5-3 Control Section Configuration
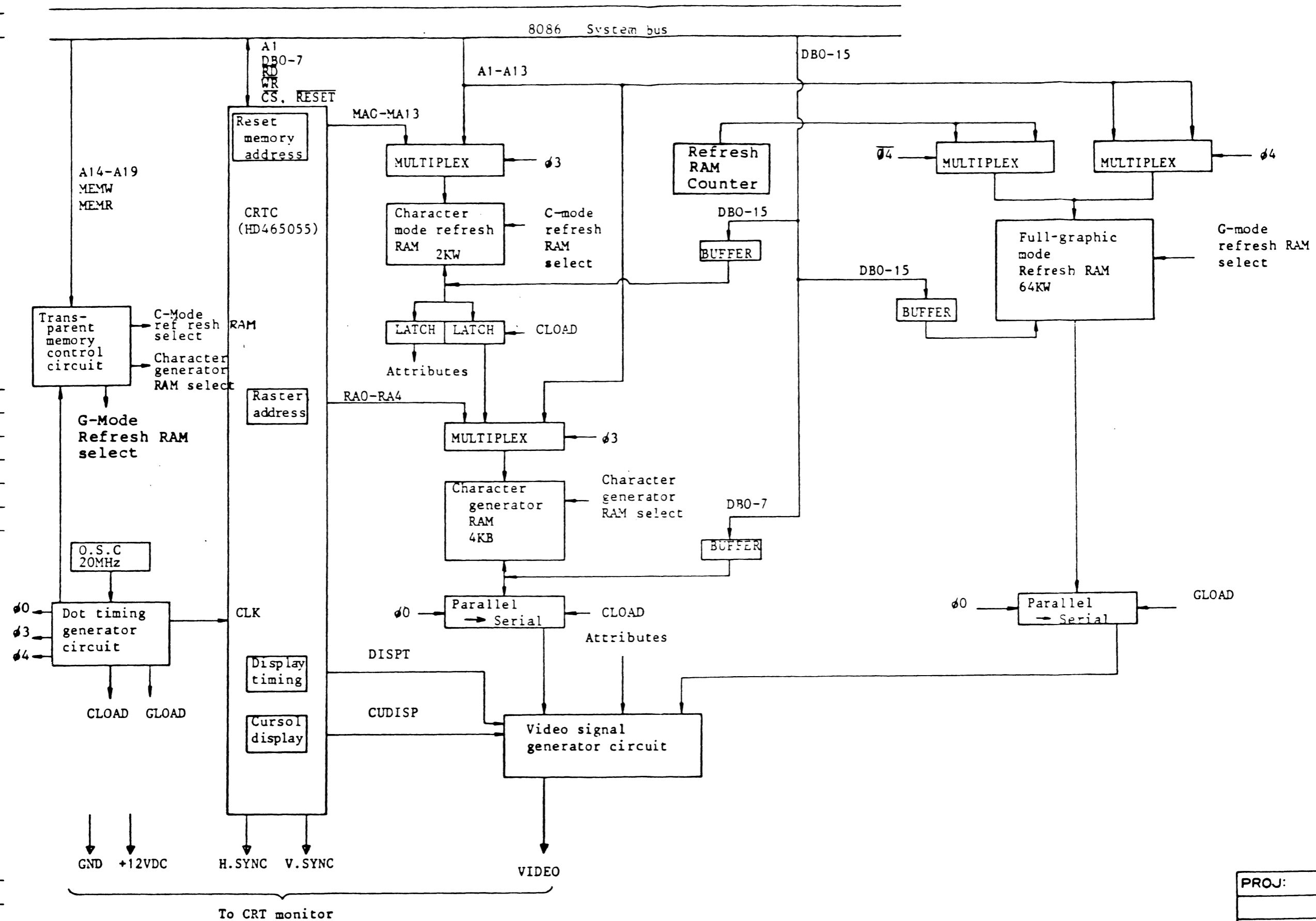
5-3-1 Block diagram

For details, see Fig. 5-3-1 "CRT controller Block Diagram".

5-3-2 CRT controller LSI

5-3-3 Character mode refresh RAM

The Character Mode Refresh RAM can specify the characters displayed in the CRT screen.

8086 System bus

A1
DB0-7
RD
WR
CS, RESET

DB0-15

A1-A13

Transparent memory control circuit

A14-A19
MEMW
MEMR

C-Mode refresh RAM select

Character generator RAM select

G-Mode Refresh RAM select

Reset memory address

CRTC (HD465055)

Raster address

RAM

MAC-MA13

MULTIPLEX — φ3

Character mode refresh RAM 2KW

C-mode refresh RAM select

LATCH **LATCH** — CLOAD

Attributes

RA0-RA4

MULTIPLEX — φ3

Character generator RAM 4KB

Character generator RAM select

Refresh RAM Counter

DB0-15

BUFFER

DB0-15

BUFFER

DB0-7

BUFFER

φ̄4 — **MULTIPLEX**   **MULTIPLEX** — φ4

Full-graphic mode Refresh RAM 64KW

G-mode refresh RAM select

DB0-15

O.S.C 20MHz

φ0
φ3
φ4

Dot timing generator circuit

CLK

CLOAD   GLOAD

Display timing

Cursol display

DISPT

CUDISP

φ0 → **Parallel → Serial** — CLOAD

Attributes

Video signal generator circuit

φ0 → **Parallel → Serial** — GLOAD

GND   +12VDC   H.SYNC   V.SYNC

VIDEO

To CRT monitor

NOTE:

OLYMPIA PEOPLE

TITLE:
CRT controler block diagram

DRG. NO.
Fig. 5-3-1

UNIT IN mm
PROJ: SCALE /

The characters are specified by one word and consists of the character code and the attribute bits.

(Bit configuration is shown as below.)

The capacity of C-Mode R-RAM is 2KW. (Two 2K x 8 bit-Static RAMs are used.)

CPU can access to C-Mode R-RAM for each word or each byte at any time.

The address space of C-Mode R-RAM is $E0000_H$ to $E07FF_H$.
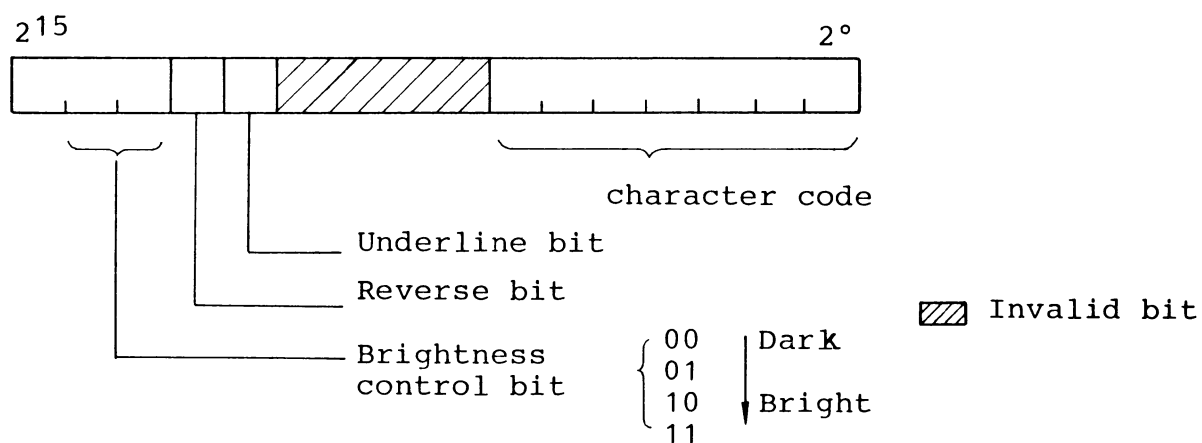

Fig. 5-3-2 Character mode refresh RAM BIT configuration

5-3-4 Character Generator RAM (CG-RAM)

The Character Generator RAM stores the character dot pattern and consists of the byte configuration.

The capacity of CG-RAM is 4K Bytes (two 2K x 8 bit-static RAMs are used) and CPU can access to CG-RAM only for each byte (in the even-numbered addresses).
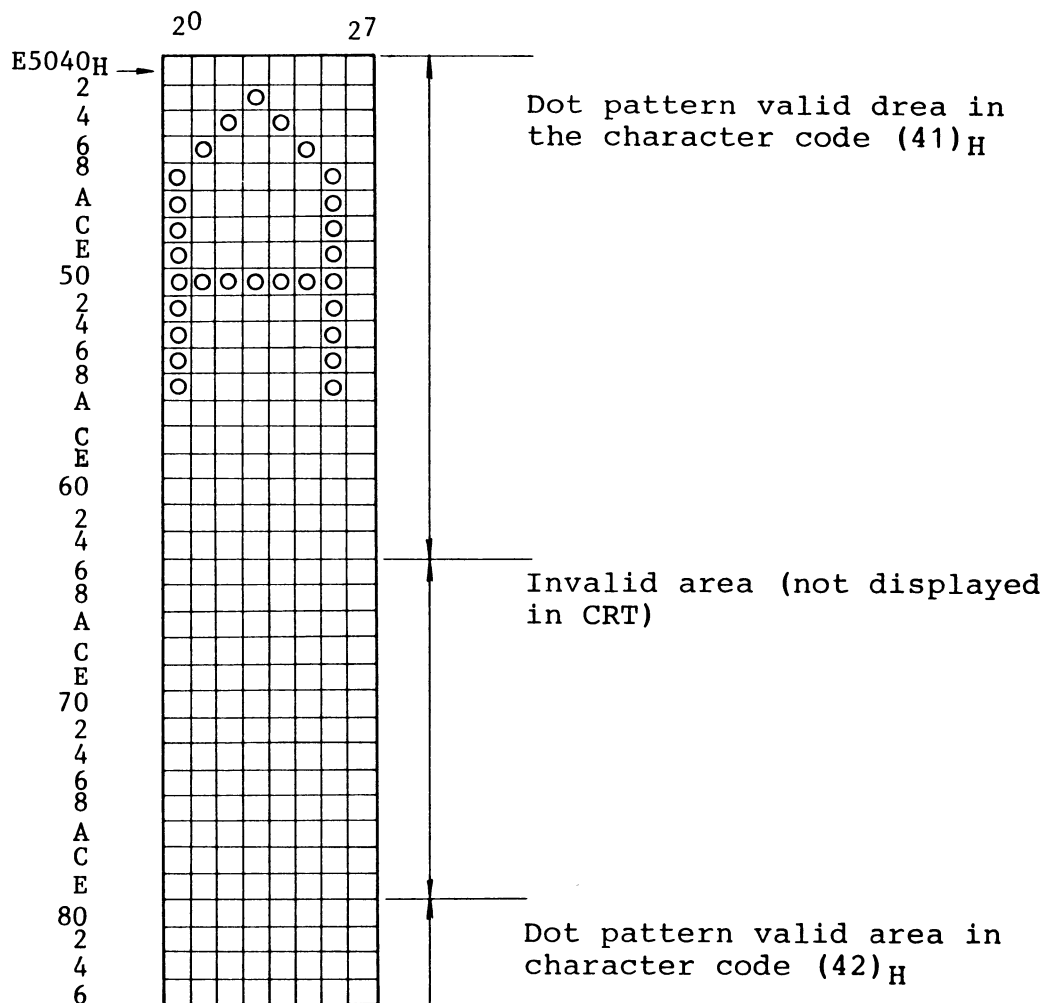
The address space is E4000$_H$ to E4FFF$_H$.

[Example]

When character code 41$_H$ is specified, CG-RAM stores the dot pattern indicating character "A".

The header address in CG-RAM for CPU is E4000$_H$.
The header address in RAM storing the dot pattern is shown as follows:

E4000$_H$ + (100 0001 00000 0)$_B$ ⟶ E5040$_H$

　　　　　　Character　Line └─⟶ At any time, 0 is
　　　　　　code　　　counter　　specified.

Dot pattern valid area in the character code (41)$_H$

Invalid area (not displayed in CRT)

Dot pattern valid area in character code (42)$_H$

5-3-5   Full-graphic mode refresh RAM (FG-Mode R-RAM)

Full-graphic mode refresh RAM (FG-Mode R-RAM) is valid when the full-graphic mode is specified, the memory in FG-mode R-RAM is the refresh memory in which one bit corresponds to one dot in the CRT screen.

The memory capacity is 64KW (in which sixteen 64K x 1 bit-dynamic RAMs are used).

CPU can   access   to FG-Mode R -RAM for each byte or each word.

The following table shows the correspondence of the RAM addresses to the CRT screen from CPU. The addresses within the part bordered with a bold line are displayed in the CRT screen.

People

6. FDD CONTROL

6. FDD CONTROL PART

6-1 Overview

FDD control part is designed to control the double-density (in both sides) and double-track-type minifloppy disk up to the maximum two, using Floppy Disk Controller (FDC) LSI (μPD765A).
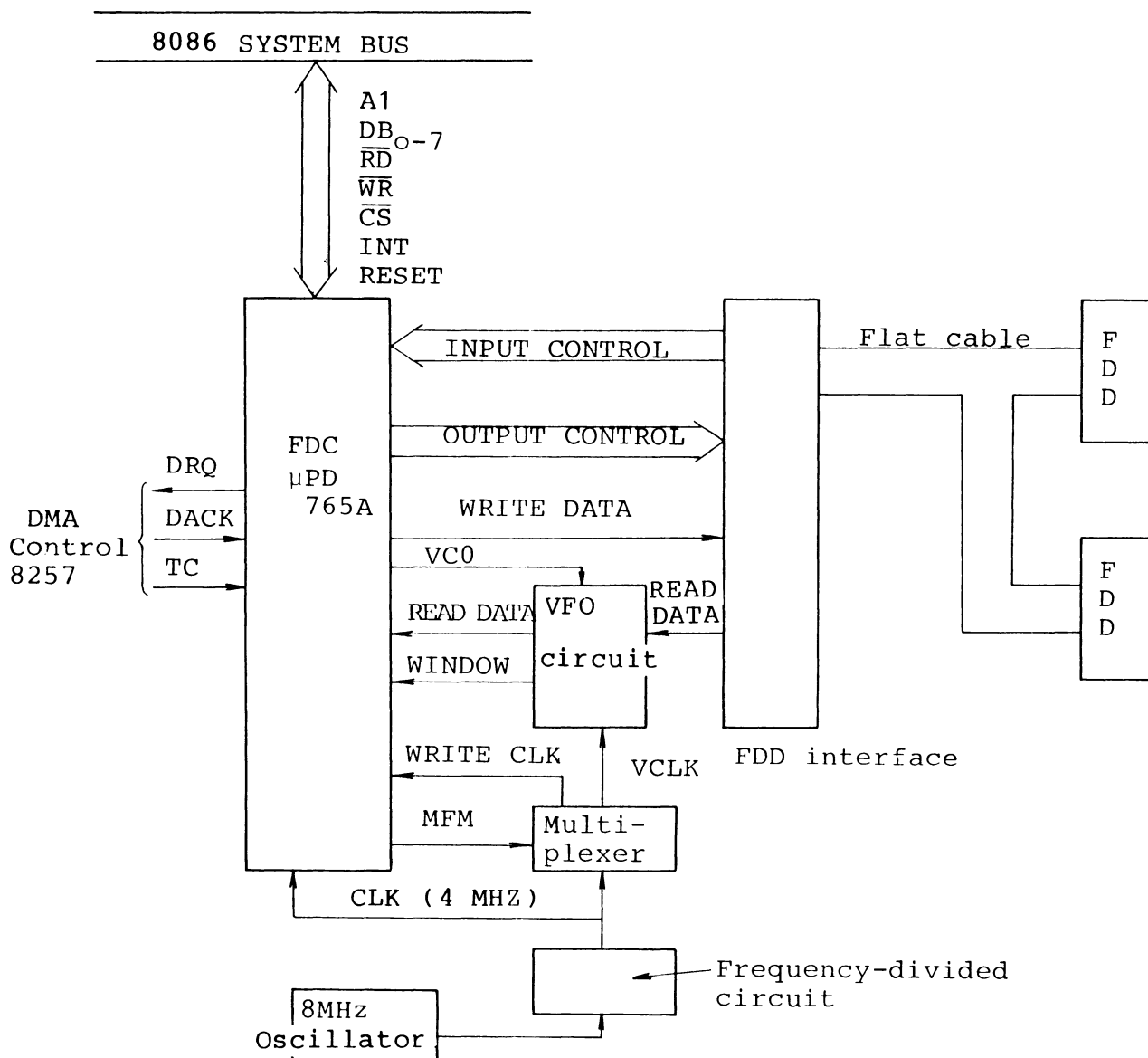
6-2 BLOCK DIAGRAM

Fig. 6-2-1 FDD control block diagram

6-3 Floppy Disk Controller (FDC)

6-4 Clock Generation Circuit

The clocks used in the FDD control part are shown as follows:

o μPD 765A clock (CLK)

o WRITE clock

o VFO clock (VCLK)

The above clocks are generated by dividing the frequency of the 8-MHz oscillator. These frequencies depend on the densities, such as single-density and double-density. (The frequency is selected depending on the MFM mode signal from FDC.)

Table 6-4-1

	Single density	Double density
CLK	4MHz	4MHz
WRITE CLK	4MHz	8MHz
V CLK	250KHz	500KHz

6-5 V.F.O Circuit

The Variable Frequency Oscillator (V.F.O) circuit consists of PROM (MB7051) with the capacity of 32 words x 8 bits, Address Latch (74LS174), and two flip-flops (74LS74). (See Fig. 6-5-1)

The thirty-two-word micro code (from addresses 00H to 1FH, for the contents of it, see Table 6-5-1) is stored in PROM.

When the read-mode is not specified in FDC (when the VCO signal is "L"), or even if the read-mode is specified in FDC (when the VCO signal is "H"), when the read-data (RD) is not received, the free-run mode is specified in PROM and Address Latch (Repeat the processings using the data from addresses 10H to 1FH).

When the read-mode is specified in FDC and RD is received from FDD, the mode to be specified changes from the free-run mode to the V.F.O mode.

When the flip-flop is set by the rise edge signal of RD, address A4 is low-level and the address to be specified next jumps to one of low-order address 16 (addresses 00H to 0FH) in PROM.

The data to delay or advance the Read Data Window(RDW) signal by one or two clocks is stored in the jump address. (See Table 6-5-1).

The distance from the generated RD to the center of the
RDW signal determines the selection either to delay, or to
advance the RDW signal.

When adress A_4 is high-level, the free-run mode is
specified again.

For details, refer to Fig. 6-5-1 "V.F.O Circuit" and
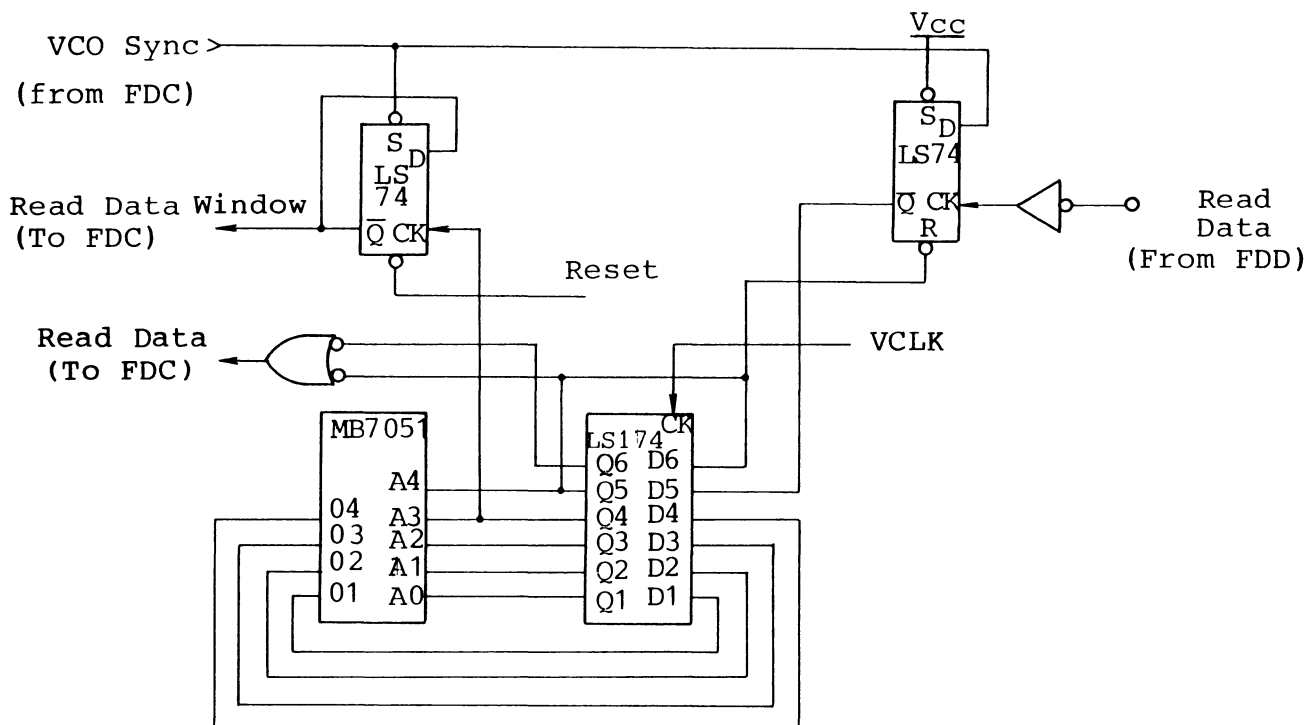Fig. 6-5-2 "V.F.O Circuit Timing Chart."
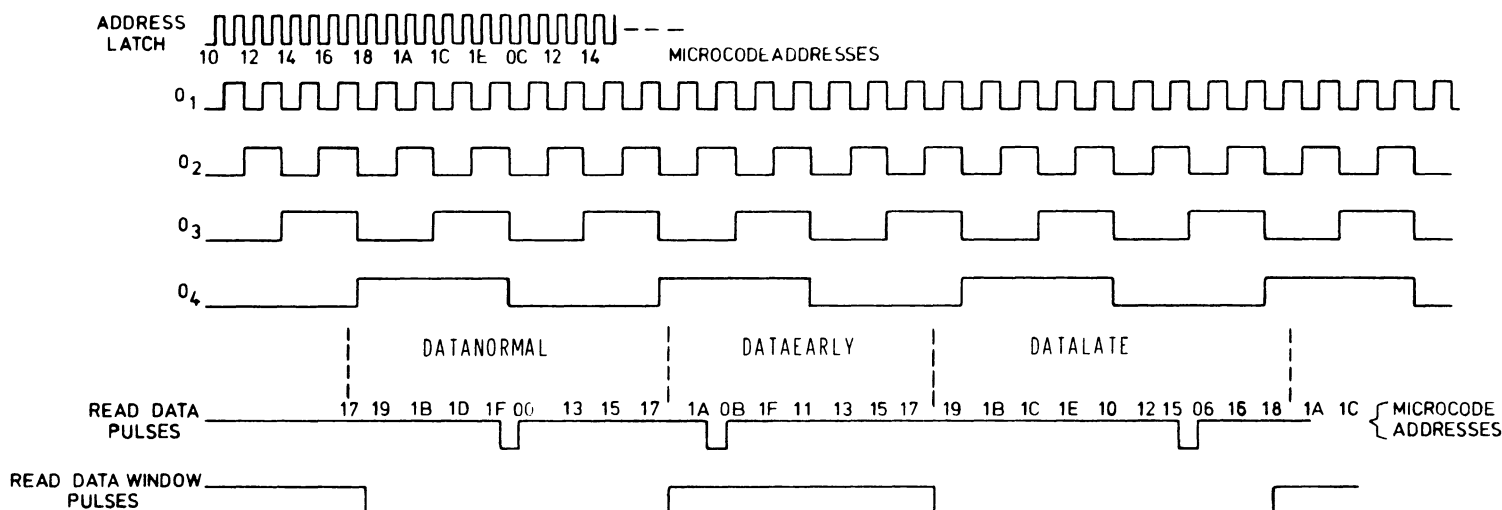
Fig. 6-5-1 V.F.O Circuit

Circuit timing

Fig. 6-5-2 V.F.O Circuit timing chart

Table 6-5-1

PROM MICROCODE

FOR DISK DRIVE DATA RECOVERY

ADDRESS$_H$	DATA$_H$	CLOCK ACTION TAKEN
00:	01	:NONE
01:	01	:RETARD BY ONE COUNT
02:	02	: " " " "
03:	03	: " " " "
04:	03	:RETARD BY TWO COUNTS
05:	04	: " " " "
06:	05	: " " " "
07:	06	: " " " "
08:	0B	:ADVANCE BY TWO COUNTS
09:	0C	: " " " "
0A:	0D	: " " " "
0B:	0E	:ADVANCE BY ONE COUNT
0C:	0E	: " " " "
0D:	0F	:ADVANCE BY ONE COUNT
0E:	00	: " " " "
0F:	01	: " " " "
10:	01	:FREE RUN
11:	02	: " "
12:	03	: " "
13:	04	: " "
14:	05	: " "
15:	06	: " "
16:	07	: " "
17:	08	: " "
18:	09	: " "
19:	0A	: " "
1A:	0B	: " "
1B:	0C	: " "
1C:	0D	: " "
1D:	0E	: " "
1E:	0F	: " "
1F:	00	: " "

7.   SERIAL INTERFACE

7. SERIAL INTERFACE

7-1 Overview

PEOPLE has the serial interface according to the RS232C standard as one of the general interfaces. The units connected to the serial interface are shown as follows.

MODEM, Printer, Keyboard Typewriter, Tape Reader, Tape Puncher, or the composite device combinated with some of the above devices.

Therefore, programming according to the unit connected to the serial interface allows People to apply to the various application program.
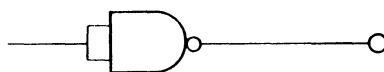
7-2 Specification

7-2-1 Standard

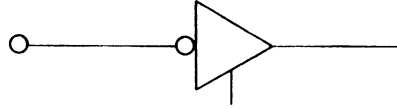RS-232C

7-2-2 Interface circuit

(1) Output

Driver I.C. is SN75188N (T.I. or equivalent)

(2)　Input
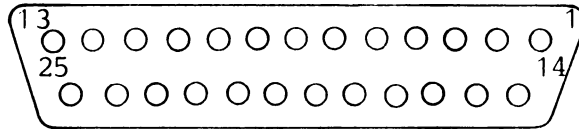
Receiver I.C. is SN75189N (T.I. or equivalent)

7-2-3　Cable length

Cable must be 10m long maximum.

7-2-4　Connector (PEOPLE side)

DB-25SA-J4-2-L　(JAE or equivalent)

As seen from connecting side

7-4 Transmission Speed

The methods of synchronizing the transmission timing are classified into Internal Synchronization and External Synchronization. Switching External Synchronization or Internal Synchronization depends on the jumper line. It is set to INTERNAL when the unit is shipped out. Printed foil is used for INTERNAL setting ; when shifting to External,cut the foil and connect to EXTERNAL with a jumper.

```
        J12                 J13

     o   o—o             o   o—o
     1   C 2             1   C 2
   (EXT) (INT)         (EXT) (INT)
```

7-4-1 External synchronization

The transmission speed is determined by the clock pulse which are transmitted from the external units. In this case, the mode command specified to 8251A set BAUD RATE to X1.

7-4-2 Internal synchronization

The transmission speed can be programmed by timer controller (8253), and can be set on software basis to either one of 150, 300, 600, 1200, 2400, 4800 and 9600 BPS.

For Timer Controller 8253, refer to Chapter 9. In this section, how to set it explains as below.

7-2-5 Interface signals

Table 7-2-1 Serial I/F signals

Pin No.	Signal name	Direction CPU EXT	Remarks
1	FG		Frame ground
2	$\overline{SD}$	────────▶	Transmission data
3	$\overline{RD}$	◀────────	Receiving data
4	RS	────────▶	Request to send
5	CS	◀────────	Clear to send
6	DR	◀────────	Data set ready
7	SG		Signal ground
8	CD	◀────────	Carrier detect
15	ST2	◀────────	Transmission signal element timing
17	RT	◀────────	Receiving signal element timing
20	ER	────────▶	Terminal ready
22	CI	◀────────	Calling indicator

7-3 Interface Controller

The serial interface employs 8251A as controller.

(1) How to set timer controller

One of the three timer counters on timer controller (8253) is used for setting the serial interface baud rate.

Since 2.4576 MHz clock is applied to the clock input terminal of the corresponding timer counter,

2.4576 MHz ÷16÷N(Timer setting)=Transmission speed

N =	16	9600 BPS
=	32	4800 BPS
=	64	2400 BPS
=	128	1200 BPS
=	256	600 BPS
=	512	300 BPS
=	1024	150 BPS

In this case, the baud rate for serial controller (8251) must be set to 1/16.

The mode of timer controller (8253) must be set to 3 (binary count mode).

8.   PARALLEL INTERFACE

8. PARALLEL INTERFACE

8-1 Overview

The parallel 8-bit data is output or input.

The interface controller (8255) and the bidirectional driver are used. The circuit is set to output or input by switching the 8255A program and the jumper wire on the seat.

8-2 Interface Circuit
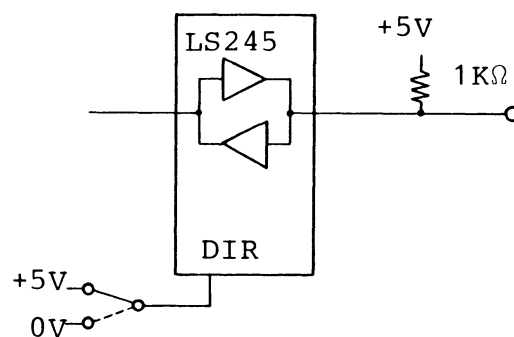

Fig. 8-2-1

8-3 Connector

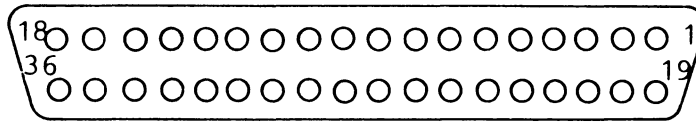(1) Connector   57LE-40360-2700 (D3)

(2) Pin array

Fig. 8-3-1 Pin array

(The figure viewed from the

connector-connected section.)
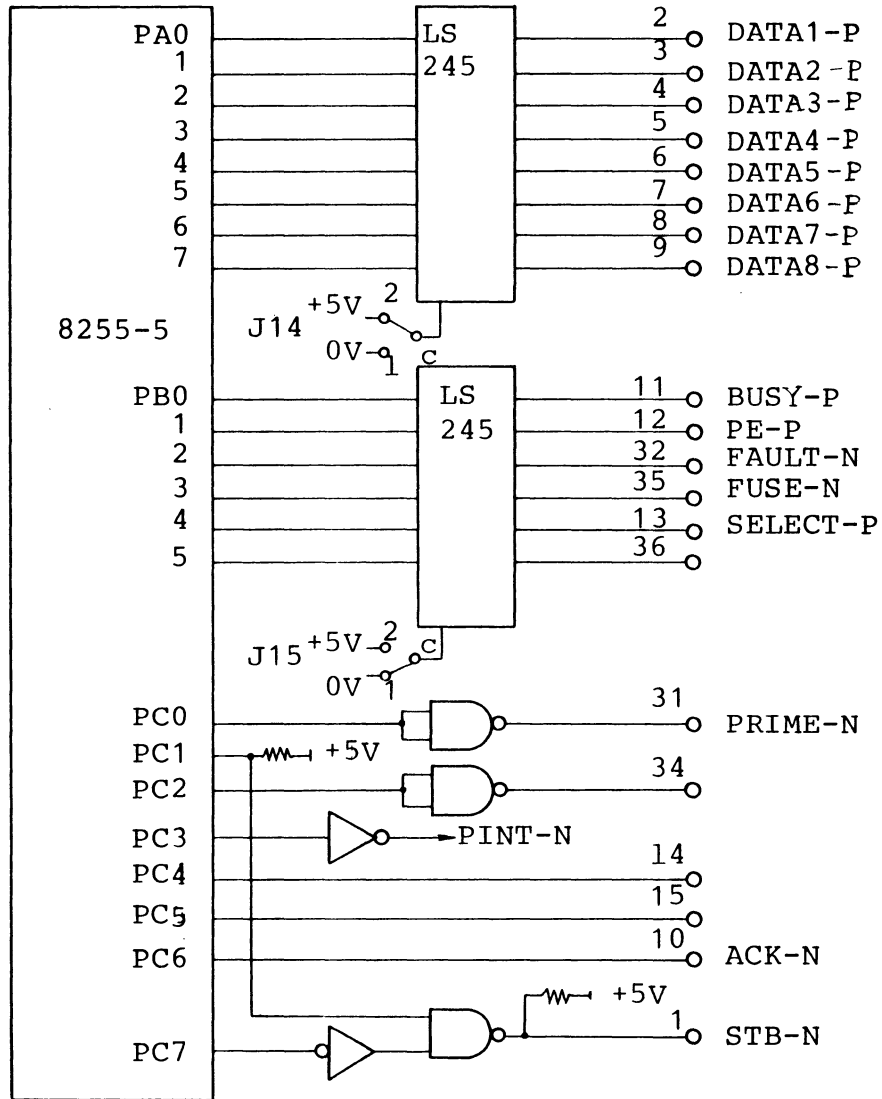
Fig. 8-4-1 Interface circuit

8-4-1   Data output circuit

The following are set when the interface circuit is used as a data output circuit.

(1)   The output direction is the signal direction of the bidirectional bus drive LS245 (14N).
Set J14 connection to C to 2.   (When shipped from the factory, the interface circuit is set with the print foil.)

(2)   The input direction is the signal direction of the bidirectional bus drive LS245(17N).
Set J15 connection to C to 1.   (When shipped from the factory, the interface circuit is set with the print foil.)

(3)   Set control IC8255-5 to the data output operating mode by the program.

8-4-2   Data input circuit

The following are set when the interface circuit is used as a data input circuit.

(1)   The input direction is the signal direction of the bidirectional bus driver LS245(14N).
Set J14 connection to C to 1.   (Cut the print foil in C to 2).

(2) The output direction is the signal direction of the
     bidirectional bus driver LS245(17N).
     Set J15 connection to C to 2.
     (Cut the print foil in C to 1.)

(3) Set control IC 8255A to the data input operating
     mode by the program.

8-4-3 Interface Controller

8-5 Printer Interface

The examples for using this circuit as a printer interface
are shown as below.

8-5-1 Setting the circuit

When shipped from the factory, this circuit is set for
the printer interface as follows:
    J14: C to 2
    J15: C to 1

8-5-2 Setting the controller by the program

Set the controller as shown in Table 8-5-1 by the
program.

Table 8-5-1   Example for setting the ports in the
printer interface

Control words	Group A									Group B
$D_7D_6D_5D_4D_3D_2D_1D_0$	Port A	Port C								Port B
		PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	
1 0 1 0 1 0 1 0	OUT	$\overline{OBF}_A$	$\overline{ACK}_A$	IN		$INTR_A$	OUT			IN

8-5-3 Interface signals

Table 8-5-2   List of the printer interface signals

Pin No.	Signal-name	Direction CPU Exterior	Contents
1	STB-N	⟶	Sample the data
2	DATA 1-P	⟶	
3	2	⟶	
4	3	⟶	
5	4	⟶	
6	5	⟶	Output data
7	6	⟶	
8	7	⟶	
9	8	⟶	
10	ACK-N	⟵	Request the subsequent data.
11	BUSY-P	⟵	The external unit cannot receive the data.
12	PE-P	⟵	The forms are short when the circuit is connected to the printer
13	SELECT-P	⟵	The SELECT state occurs.
14			
15			
16	0V		SIGNAL GROUND
17	FG		FRAME GOUND
18	+5V	⟶	Power
19-30	TWIST PAIR GND		TWIST PAIR RETURN
31	PRIME-N	⟶	Set the external unit to the initial state.
32	FAULT-N	⟵	When one of the PE, SELECT, and FUSE state occurs, the circuit is low-level.
33			
34			
35	FUSE-N	⟵	When the fuse is off, the circuit is low-level.
36			

9.   TIMER CONTROLLER

9. TIMER CONTROLLER

9-1 Overview

The timer controller (8253-05) has three timer counters. These three timer counters are independent respectively and used as follows:

(1) Interval timer

(2) Clock for setting BAUD RATE of RS232C Serial Controller

(3) Clock for receiving to the keyboard interface controller

9-2 Generating the Clock for KB Interface (Channel 0)

The series data transmission format is specified in the interface with KB, as described in Section 4-1-1.

The data transfer rate is 1200 BPS and the data transmission is controlled by 8251A.

As described in Section 4-2-1, the clock of 19.2 KHz must be given to 8251A.

The clock of 2.4576 MHz (PCLK) is given to Channel 0 in 8253-5. Therefore, when the timer counter in channel 0 is set to 128, the clock of 19.2 KHz is output as follows:

$$2.4576 \ (MHz) \div 128 = 19.2 \ (KHz)$$

The mode to be specified in the timer (Channel 0) is as below.

Mode = 3

binary-count

9-3 Setting the Transfer Rate in the Serial Interface (CHANNEL 1)

Channel 1 in 8253-5 output the clock determining the transfer rate to the serial interface controller (8251A).

The input clock is the same clock of 2.4576 MHz (PCLK) as that in channel 0. The operating mode is 3, and the binary count mode.

For the timer-set value for determining the transfer rate, refer to Section 7-4-2.

9-4 Interval Timer (CHANNEL 2)

Channel 2 in 8253-5 is used as an interval timer.

The clock output (CLKA) in channel 0 is given to the input clock. (The frequency is 19.2 KHz).

The interval timer interrupts to CPU (8086) periodically, and the cycle depends on the value set in the timer counter in Channel 2. When the set value is N,

$$N \div 19200 = T \text{ [sec]},$$

that is, T is the cycle of the interval timer.

The optional value from 0 to $(FFFF)_{16}$ is set in N, however, value 0 is equivalent to value $(10000)_{16}$.
Therefore, the following are obtained.

$$1 \leq N \leq 65536$$

$$52 \ \mu s < T < 3.42 \text{ sec}$$

The value from 52 μs to 3.42 sec can be set in T, for each unit of about 52 μs.

The operating mode is 2, and set to binary count mode.

People

10. Power Supply Unit

10. Power Supply Unit

10-1 Power Supply Unit

This unit was composed for obtaining stabilized D.C. output from the commercial A.C. voltage. The conditions of input and output are stated in Para. 2.

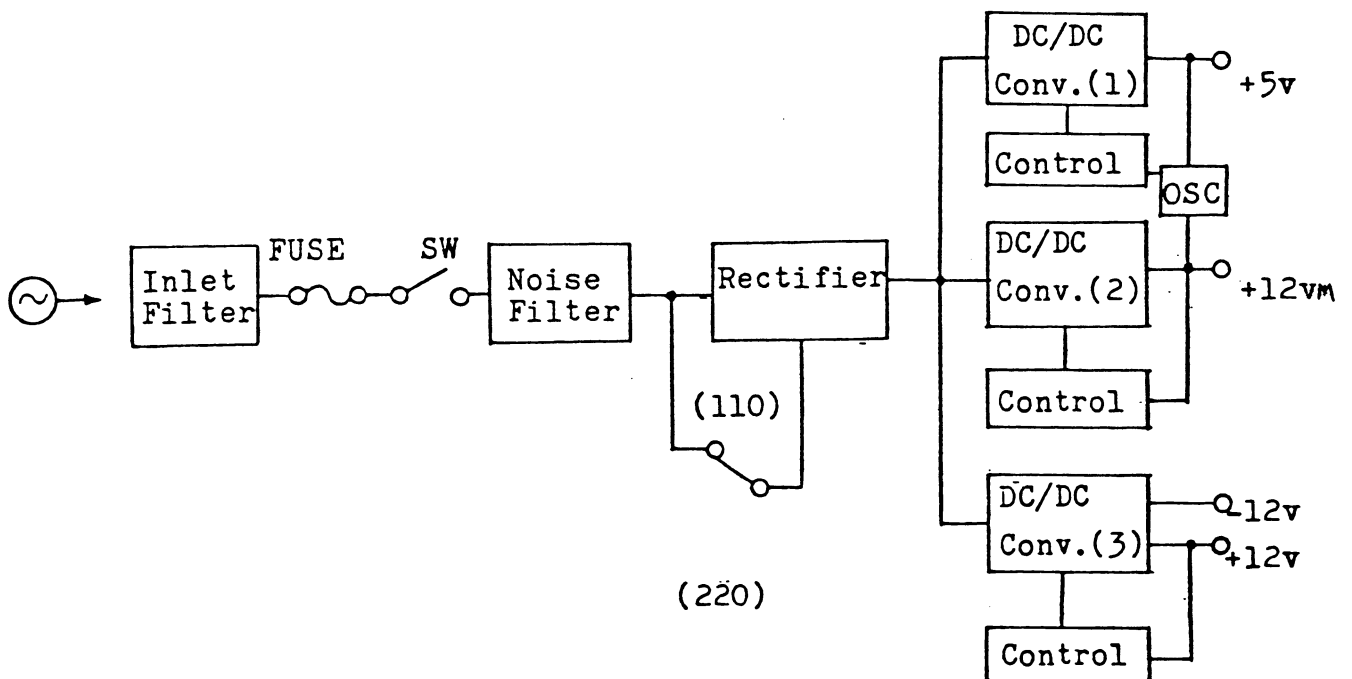### 10-2 Input - Output

Input.   AC 110V   50/60 Hz
         AC 220V/240V   50/60 Hz

Output.   +5V   15A max
          +12V M   3A (6A Peak)
          +12V   1.7A max
          -12V   0.1A max

Range selection is manually performed by the use of an input voltage selector in this unit.

10-3 Block Diagram

10-4   Filter

This block is composed of inlet type filter and L, C that are installed in PK1 unit. This block protects the main unit from the noise that is transmitted from outside via AC input cable. And also, this filter prevents the outgoing noise generated in the main unit.

10-5   Switch and Fuse

The input after passing the inlet-type filter is connected to the on-board filter through the fuse and both line ON/OFF switch.

10-6   Rectifier

When the input voltage selector in this power supply unit is at AC 220V, the rectifier circuit is operating as normal full wave rectifier.

The primary DC voltage, which is obtaining by wave filtering, is approximately 300V DC at both AC 110V and AC 220V.

10-7   Fly-back converter circuit(12VM, 12V)

The DC/DC convertors (2) and (3) are a circuit formed to obtain the outputs by the blocking oscillator.

The separation of the primary and secondary is done by the Photo-Coupler.

+12V M output is controlling the On-Pulse width of DC/DC convertor (2) to detect the output voltage.

In the same form, +12V output is controlling the On-Pulse width of DC/DC convertor (3) to detect the output voltage.

-12V output is stabilized by the series regulator IC to be taken out from output transformer of the DC/DC convertor (3).

+5V output is coming to stabilized voltage output by the DC/DC convertor (1), pulse width modulated forward convertor.

10-8 Over voltage protection

Over voltage detection level is set up at 6 - 7V by zener diode(DZ101). If output voltage exceed the level, SCR101 becomes ON state, and the terminal 14 (9) of control IC is forced to grand level, stopping oscillation.

1. Application

This manual is applicable only for the maintenance and repair of the PSS166-1801 power supply Units.

2. Troubleshooting and Repair Procedure

2-1. Disassembly

a) Unplug the AC input cord.
   Unscrew 10 flat head screws and remove both top and rear covers

b) Unscrew 3 screws shown marked with a dot symbol (.) and the 2 screws marked with arrows (←) (5 screws in all). Then pull the plate in the direction of the large arrow (⇒).

2-2. No+5V generated

Confirm the presence of +5V on the load side. If OK,
mechanically disassemble the power supply, unit by unit.
Check for the presence of cracks, rubbish, or obviously
faulty parts. Then perform the following tests in sequence.

Remove CN2

| Is there voltage on HIC1-15? |

YES → | Do HIC pins have the following voltages? 1-5:Approx.15V 6-15:Approx.8V |

NO → Replace Tr203

YES → | Do HIC pins14-15 have more than 2V? |

NO → Replace HIC101

YES → Connect a 1K resistor between HIC pins 1 and 2

NO → Replace SCR101,DZ101

| Do HIC pins 2-5 have waveform as shown at right? |

$t/T \geqq 20\%$ $V=15v$ approx.

YES

NO → Replace HIC101

Replace Tr1 and/of faulty parts
(R9,R10,D3) of pk3.
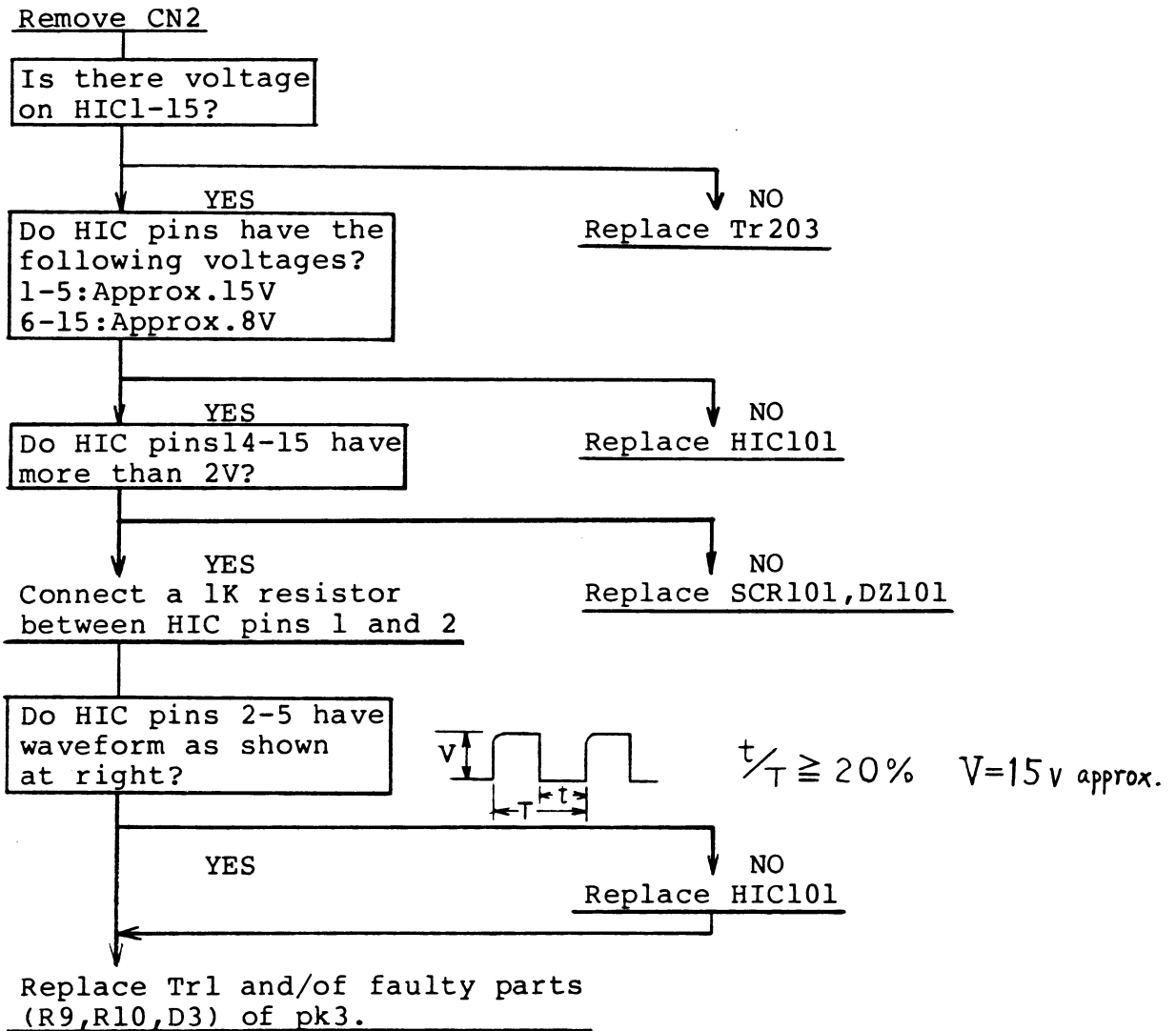
2-3. No+12V, -12V generated

Confirm the presence of 12V on the load side. If OK, mechanically disassemble the power supply, unit by unit. Check for the presence of cracks, rubbish, or obviously faulty parts. Then perform the following tests in sequence.

```
┌────────────────────┐
│How much voltage does│
│+12V supply generate?│
└────────────────────┘
        │ 0V<                              │ 0V
┌────────────────────┐           Replace Tr3 and/or faulty
│Note position of RV401.│        parts ( R51,R56) of pk3.
│Can Voltage be raised│
│or varied with RV401?│
└────────────────────┘
        │ NO                               │ YES
Return RV401 to its               Adjust the Voltage. Repair
former setting.                   completed
        │
Check Tr52, Tr53, D56
of PC401 and pk3.
Replace if faulty.
+12V output generated?
        │ NO                               │ YES
Replace IC401                     Repair Completed
```
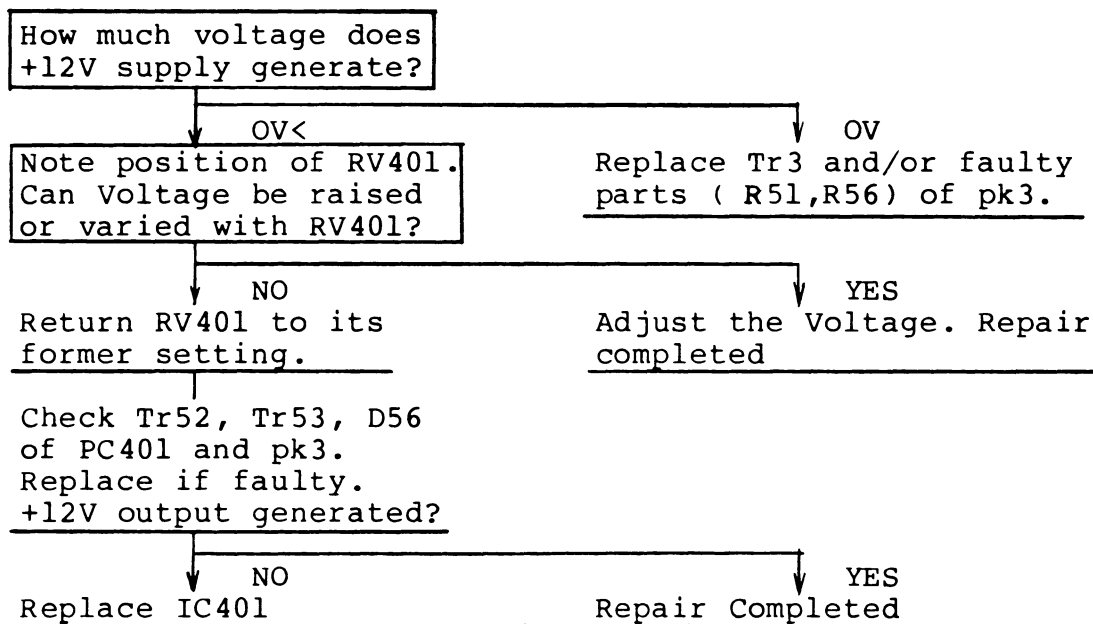
2-4. No-12Vgenerated

Confirm the presence of -12V on the load side. If OK, mechanically disassemble the power supply, unit by unit. Check for the presence of cracks, rubbish, or obviously faulty parts. Then perform the following tests in sequence.

```
┌────────────────────┐
│Is there Voltage on C301?│
└────────────────────┘
        │ YES                              │ NO
┌────────────────────┐           Replace D301
│Does D302 check good?│
└────────────────────┘
        │ YES                              │ NO
Replace IC301                     Replace D302
```

2-5. No+12V(M), +5Vgenerated

Confirm the presence of +12V(M) If OK, mechanically
disassemble the power supply, unit by unit. Check for the
presence of cracks, rubbish, or obviously faulty parts.
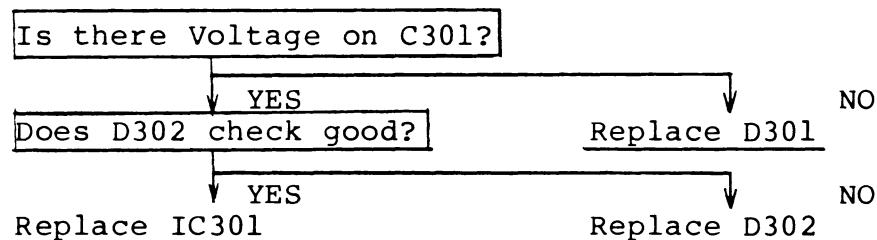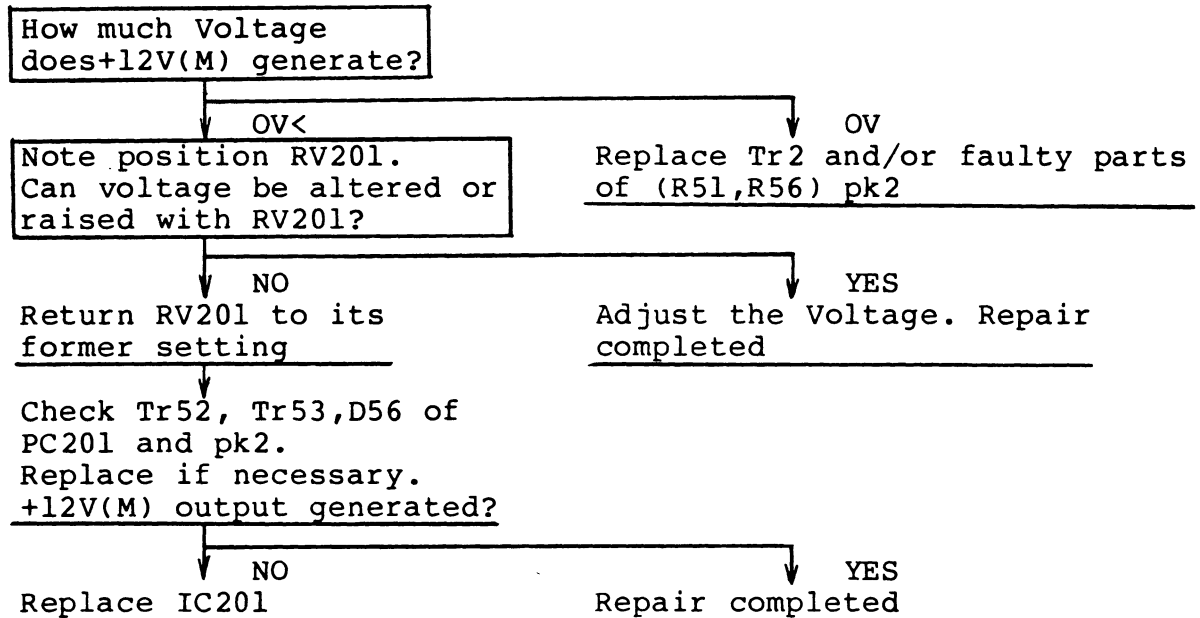Then perform the following tests in sequence.

```
┌──────────────────────────┐
│ How much Voltage         │
│ does+12V(M) generate?    │
└──────────────────────────┘
         │ OV<                              │ OV
┌──────────────────────────┐    Replace Tr2 and/or faulty parts
│ Note position RV201.     │    of (R51,R56) pk2
│ Can voltage be altered or│
│ raised with RV201?       │
└──────────────────────────┘
         │ NO                               │ YES
Return RV201 to its              Adjust the Voltage. Repair
former setting                   completed
         │
Check Tr52, Tr53,D56 of
PC201 and pk2.
Replace if necessary.
+12V(M) output generated?
         │ NO                               │ YES
Replace IC201                    Repair completed
```

2-6. When a fuse is blown

Mechanically disassemble the power supply, unit by unit.
Check for the presence of cracks, rubbish, or obviously
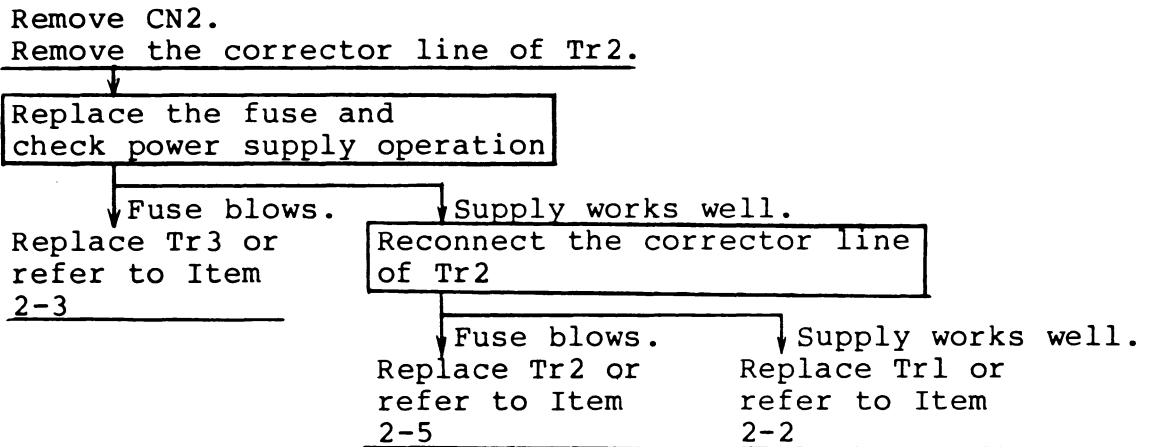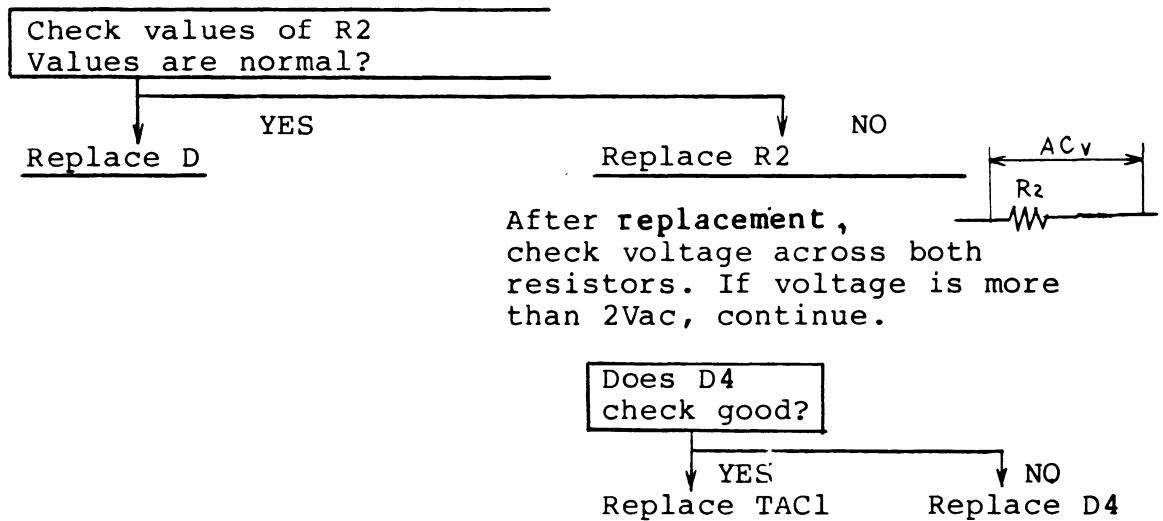faulty parts. Then perform the following tests in sequence.

Remove CN2.
Remove the corrector line of Tr2.

| Replace the fuse and
check power supply operation |

↓Fuse blows.

Replace Tr3 or
refer to Item
2-3

↓Supply works well.

| Reconnect the corrector line
of Tr2 |

↓Fuse blows.

Replace Tr2 or
refer to Item
2-5

↓Supply works well.

Replace Tr1 or
refer to Item
2-2

2-7. No output generated, but fuse is OK

Mechanically disassemble the power supply, unit by unit.
Check for the presence of cracks, rubbish, or obviously
faulty parts. Then perform the following tests in sequence.

| Check values of R2
Values are normal? |

↓ YES

Replace D

↓ NO

Replace R2

After replacement,
check voltage across both
resistors. If voltage is more
than 2Vac, continue.

| Does D4
check good? |

↓ YES

Replace TAC1

↓ NO

Replace D4

People

MAINTENANCE
MANUAL

Mai 1983

1. UNPACKING AND PACKING

1-1 Unpacking

1-1-1 Unpacking procedures

(See Figs. 1-1-1 and 1-1-2.)

(1) Remove the tapes attached to three packed planes.

(2) Loosen, two strings fastend at the rivets.

(3) Unwrap the packed planes.

(4) Take out styrofoam ① from the box.

(5) Take out the AC cable, CRT Cable, Operating manual etc. from the box.

(6) Take out styrofoam ② from the box.

(7) Take out the P.C.B option from the box.

(8) Take out styrofoam ③ from the box.

(9) Take out styrofoam ④ and ⑤ from the box.

(10) Take out Key Board from the box.

(11) Take out styrofoam ⑥ from the box.

(12) Take out Main Unit from the box.

(13) Take out styrofoam ⑦ from the box.

(14) Take out each component from the unwrapped packages.

1-1-2 Notes on unpacking

(1) Handle the parts according to the notes written on the corrugated cardboard box.

(2) Check whether there is a damaged part or not.

(3) Check whether there is a flaw in the rust or not.

(4) Check whether there are such parts unnecessary for constructing as wire scobs, screws, etc. or not.

1-2 Packing

1-2-1 Packing procedures

Pack the corrugated cardboard box in the reverse order
of the unpacking procedures.

1-2-2 Notes on packing

(1) Check whether the set of components to be packed is
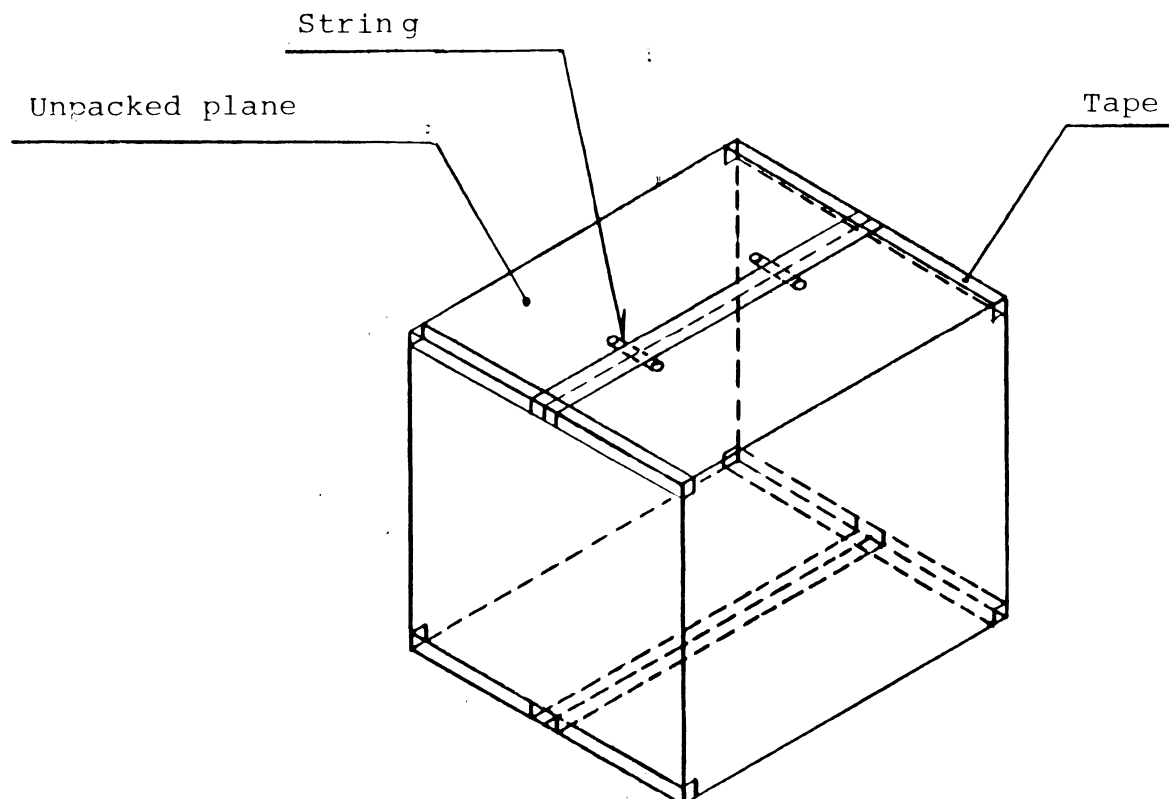complete or not, before packing.

String

Unpacked plane   Tape

Fig. 1-1-1 Unpacking and packing

Operating manual
etc.

AC cable
CRT cable etc.

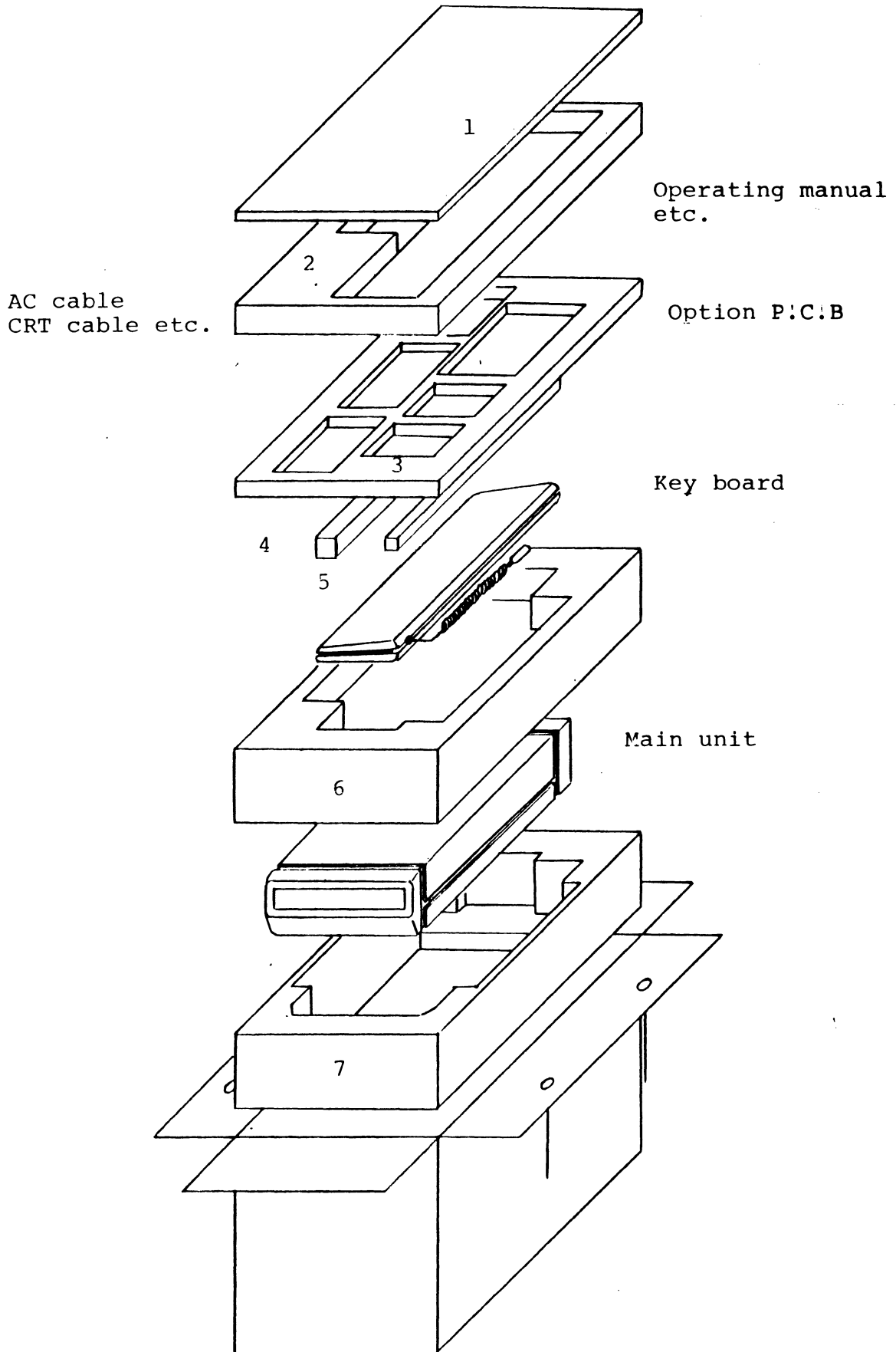Option P:C:B

Key board

Main unit

Fig. 1-1-2 Unpacking and packing

2. CRITERIA FOR MAINTENANCE

This maintenance standard prescribes the rules on PEOPLE maintenance.

2-1 Installation Criteria

These criteria explains on procedures or notes when users unpack the box, construct and adjust the components packed depending on the packing specification by manufacturers.

2-1-1 Installation conditions

(1) Standard layout

The standard layout on PEOPLE is shown in Fig. 2-1-1.

The cord for power source is connected to the back of PEOPLE.

(2) Maintenance area

For the maintenance work, the area within one meter around PEOPLE is required as a maintenance area. However, if there is another space for maintenance work, the maintenance area is not required.
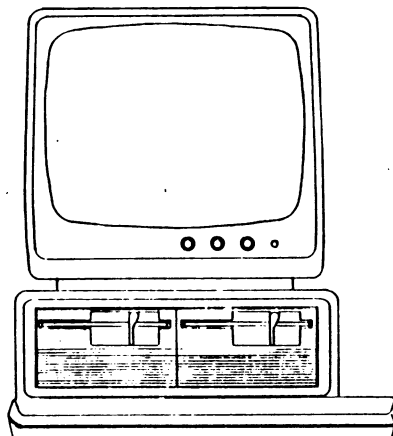
Fig. 2-1-1

2-2 Disassembly, Assembly, and Adjustment

2-2-1 Disassembly and Assembly

An explanation is given here as to the parts whose handling requires a specific knowledge and technique. Please refer to Fig. 4-1 page-2035 and Fig. 4-3 page-2036, which show the disassembled parts stereoscopically, with regard to the handling of other parts.

(1) Cover (See Fig. 4-1 page-2035)

Remove the cover (No. 23) as follows:

(a) Dismount the Panel R (No. 24).

(b) Pull the cover slightly backward, then lift it out of its place, and set it aside.

Note: Install the cover by reversing the procedure mentioned above.

(2) Power Supply (See Fig. 4-1 page-2035)

Remove the power supply (No. 15) according to the following procedure:

(a) Dismount the panel R (No.24).

(b) Remove the cover (NO.23).

(c) Remove the two screws on the rear side and loosen the two screws on the lateral sides on the screw and washer assembly (NO.10) which fastens the back panel (No.11).

(d) Loosen all the screws on the screw and washer assembly (NO.6) which fastens the bracket P (NO.16).

(3) Key Top (See Fig. 2-2-1)

Removal of the key top (No.2-4 to 2-46, No.2-48 to 2-93) is effected by drawing it out with the use of a drawing clamp A. Drawing should be carried out by keeping the drawing clamp A in the range of angles shown in Fig. 2-2-1.

Note: Caution should be exercised in inserting the key top not to tilt it.

(4) Key Top with LED (See Fig. 2-2-2)

Remove the key top with LED (NO. 2-3, No.2-47) by drawing it out with the use of a drawing clamp B. In drawing it out, utilize the principles of the lever and fulcrum at the point "A".

In assembling, insert the key top first from LED Side.

Drawing Clamp

Key Top

Drive Rod

Panel

Housing

Key Top

Fig. 2-2-1

45°

Drawing Clamp B

"A"

LED

Key Top

Panel

LED Side
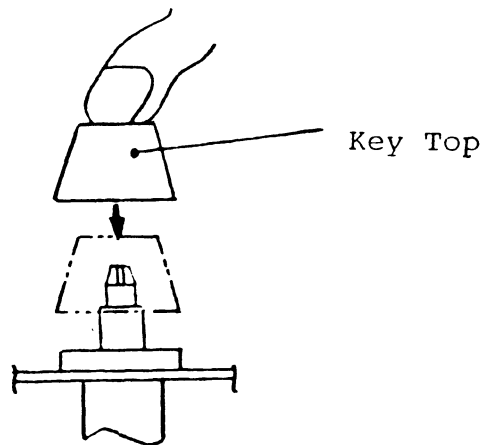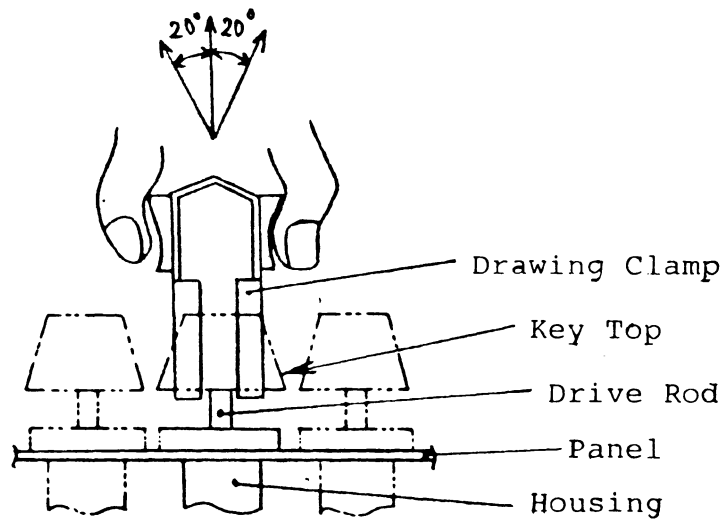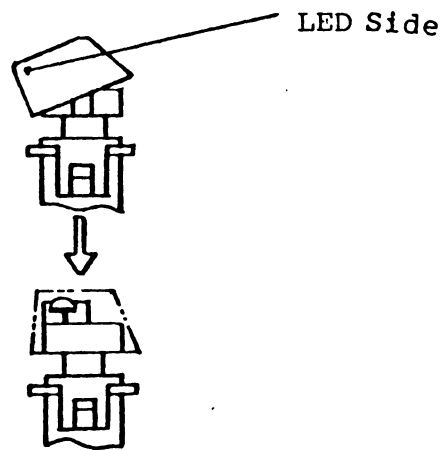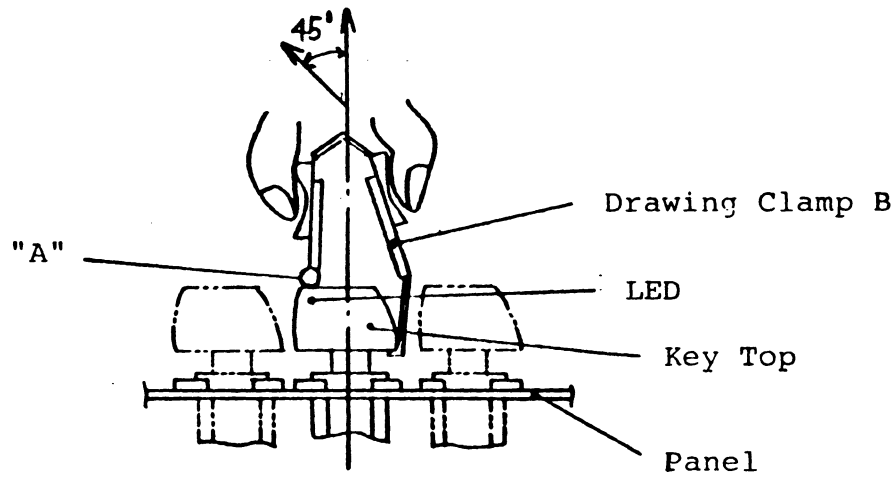
Fig. 2-2-2

(5) Switch (See Fig.2-2-3)

Replacement of the switches is conducted as follows.

(a) Suck up the solder of the terminals of the switch to be replaced from the land of the P.C.B. with the use of a suction solder disposer. Since the terminals are bent, the terminals must be straightened before the solder is sucked up.

The solder must be removed thoroughly, because the land is apt to be damaged if the removal of solder is not satisfactory.

(b) Hold the switch firmly by the drive rod with pliers and pull out the switch from the panel.

(c) After smoothing the soldered parts on the land of the P.C.B., insert a new switch into the holes on the land of the P.C.B. securely, paying close attention to the position of the switch on the panel and bend of the terminals.

(d) Check and confirm that the terminals are surely put out through the P.C.B. and solder the terminals with a soldering iron and solder. Soldering should be completed in the shortest possible time.

(e) Finalize the soldering work by wiping off the flux from the soldered parts with a piece of cloth soaked with alcohol.

O   X

Pliers

Drive Rod

Panel

P.C.B

Panel

P.C.B

Terminal
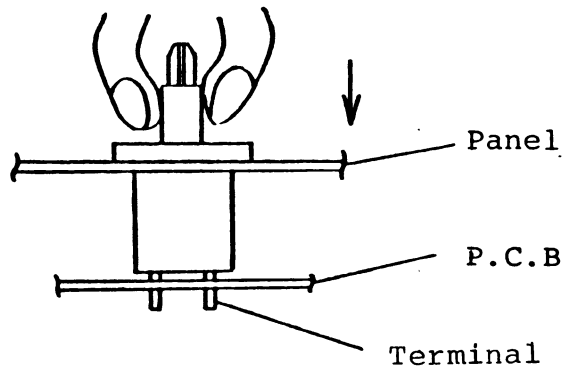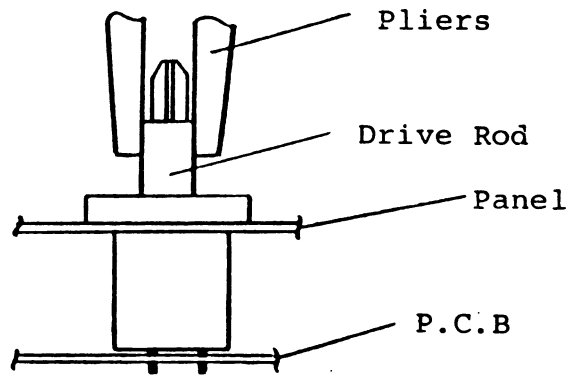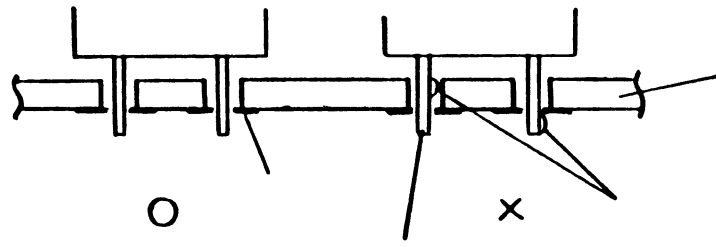
Fig. 2-2-3

(6) Space Key Top (See Fig. 4-3)

Removal of the space key top (No. 2-75) is carried out as follows:

(a) Pull out the key top holding it both sides.

(b) Remove the link from the link holder.

(c) Remove the link from the drive rod.

(d) Remove the drive rods from the key top.

Assembly of the space key top is carried out as follows:

(f) Insert the two drive rods into the key top. The rear side and front side of the drive rod can be known by the size of the holes. The hole of smaller size should be on your side.

(g) Fix the link holder to the panel.

(h) Insert the spring into the link. One end of the spring has a U-bend and the other end has an L-bend and insertion should be made from the L-bend. The spring should be fixed to the left side.

(k) Hook on the U-bend of the spring to the bottom of the link.

(l) Insert the link into the hole on the drive rod of the space key top, exercising caution not to let the spring fall out of the link.

(m) Insert the space key top fitted with the link into the link holder. At this time, put the L-bend of the spring into the spring hole of the link holder.

2-2-2   Adjustment

Adjustment is made by running a test program after loading the test program chosen from the floppy disks for testing use.
As for the procedure of the operation, please refer to the Test Program Operating Manual.

2-3 Criteria for Regular Maintenance

2-3-1 Criteria for cleaning

The following parts must be clean when the maintenance
for PEOPLE is served, or when PEOPLE is checked
regularly.

Item	Part to be cleaned	Contents of cleaning	Time necessary for cleaning
1	Outer surfaces	Wipe the dust etc, with the soft cloth. For the parts much stained, wipe them softly using the soft cloth soaked with alcohol. Thinner, benzine, etc, must not be used.	For five to ten minutes
2	CRT	Wipe the dust or the stain on the Braun tube. When it is much stained, wipe it softly with the soft cloth soaked with alcohol.	For one minute
3	FDD	The magnetic head must not be cleaned with an applicator, etc. directly. Clean the magnetic head using a double sided cleaning disk. In this case, the test program only for cleaning is operated in the unit.	For five minutes

2-3-2   Notes on others

Check the following parts when PEOPLE is checked

regularly.

Item	Part to be Checked	Contents of checking	Time necessary for checking
1	Looseness of the screw in each section of PEOPLE	Check whether the power-source-fixed, OLP2-unit-fixed, fan-fixed, and floppy-disk-fixed screws are loosened or not.	Fow two to three minutes
2	Looseness of the connectors (Inside PEOPLE)	o OLP1 unit power cable connector o OLP2 unit power cable connector o Floppy unit power cable connector o Floppy unit to OLP2 unit connection cable connector o Fan connection connector	For two to three minutes

Item	Part to be cleaned	Contents of cleaning	Time necessary for cleaning
3	Looseness of the connectors (Outside PEOPLE)	o KB unit connection connector o CRT unit connection connector o Printer connection connector	For two to three minutes
4	Check of the function	All functions are checked by operating the test program.	The maximum forty minutes

2-3-3   Changing the parts for maintenance

(1)   Floppy disk

Some of the sub-assemblies in the floppy disk must

be Changed depending on the operating time and the

number of operation. The part-names and the

changing cycle are shown as below.

(a) Head carriage ass'y   7000 head load & motor on

hrs. or 1×10^7 seeks

(b) Guide shaft   Replace with head

carriage ass'y

(c) Stepping motor ass'y 1×10^7 seeks

(d) Steel belt   Replace with stepping

Belt spring   motor ass'y

(e) DD motor ass'y   30000 motor on hrs.

(f) Collet ass'y 3×10^5 clamps

(g) Head load solenoid 1×10^7 head loads

ass'y

For details, refer to MINI FLEXIBLE DISK DRIVE

MAINTENANCE MANUAL.

2-4 Maintenance Parts

2-4-1 Criteria for preparing the maintenance parts.

The number and the level of the maintenance parts to be prepared are prescribed as follows, depending on the reliability of parts, the number of used parts etc.

    Q'TY .... Number of the parts used in a unit

    * Number to be prepared ..... Number of the maintenance parts necessary for a unit (for a year)

    Level to be prepared ...... Level A: Must be stored in the agencies at any time.

    Level B: Must be stored in the service centers at any time.

    * The rate of damages is referred to for calculating the number of maintenance, parts to be prepared. However, the operating time is assumed to be 8 hours a day, or 300 days a year. (2,400 hours a year.)

3. TROUBLESHOOTING

3.1 Introduction

When a trouble occurs in a user's house, in order to reduce systemdown time, the system is basically recovered with unit replacement and failing units carried and repaired at the service center.

The troubleshooting in this section is a manual for maintenance personnel to identify failing units. (Refer to the repair manual for repairing failing units.)

Furthermore, refer to 2.2 breakdown, assembly, and adjustment for breakdown and assembly.

3.2 Failing Units

This section identifies troubles of the following units.

- OLP1 unit	- OLP2 unit
- Power supply unit	- FDD unit
- Fan	- Keyboard unit
- Cables	- CRT unit

3.3 Identifying Troubles

There are two methods of identifying troubles: (1) according to conditions at bootstrap time and (2) by running the test program.

3.3.1 Bootstrap

Troubles are identified according to the condition of each unit in bootstrap actions when the PEOPLE system is powered on or when the reset key is pressed.

See the flowcharts. Refer to the operating manual for bootstrap procedures.

3.3.2 Test program

The test program refers to the RAM Resident Test Program and is used to identify troubles of RS232C, parallel interfaces, and optional units. Since these units become operational after bootstrap is completed, it is prerequisite that the CPU's peripheral (OLP1 unit), CRT, CRT controller (part of OLP 2 unit), FDD, and its controller (OPL2 unit) should operate normally. Refer to the test program operating manual for the test program running procedures.

3.3.1 Trouble indentification at bootstrap time

POW ON = RESET

```
           ┌──────────────────┐
           │ Driven with the  │  No    ╭───╮
           │ fan turning      ├───────→│ A │
           │ normally ?       │        ╰───╯
           └──────────────────┘

           ┌──────────────────┐
           │ Is CRT POW LED   │  No    ╭───╮
           │ lit ?            ├───────→│ B │
           └──────────────────┘        ╰───╯

           ┌──────────────────┐
           │ Is the buzzer    │  Yes   ╭───╮
           │ sounding ?       ├───────→│ C │
           └──────────────────┘        ╰───╯

           ┌──────────────────┐  Yes
           │ Not displayed on │──────────────────────┐
           │ on the CRT ?     │                       │
           └──────────────────┘            ┌──────────────────┐
                                           │ Is FDD LED lit   │  No   ╭───╮
           ┌──────────────────┐  No        │ thinnly ?        ├──────→│ F │
           │ Is memory size   │────────┐   └──────────────────┘       ╰───╯
           │ displayed on the │        │            │ Yes
           │ CRT correct ?    │        │          ╭───╮
           └──────────────────┘        │          │ E │
                                       │          ╰───╯
           ┌──────────────────┐  No  ╭───╮   ┌──────────────────┐
           │ Is FDD LED lit   ├─────→│ D │   │ OLP1 unit or OLP3│
           │ thinnly ?        │      ╰───╯   │ unit is faulty   │
           └──────────────────┘              └──────────────────┘

           ┌──────────────────┐  No
           │ Are input        │────────────────────────┐
           │ characters       │                        │
           │ displayed correct│              ┌──────────────────┐
           │ -ly on the CRT   │              │ Is nothing       │  Yes  ╭───╮
           │ with keying-in ? │              │ displayed on the ├──────→│ H │
           └──────────────────┘              │ CRT with         │       ╰───╯
                                             │ keying-in ?      │
           ┌──────────────────┐  No  ╭───╮   └──────────────────┘
           │ Is the bootstrap ├─────→│ X │            │
           │ device FDD ?     │      ╰───╯          ╭───╮
           └──────────────────┘                     │ G │
                                                     ╰───╯
           ┌──────────────────┐
           │ Insert a system  │
           │ diskette into FDD │
           │ for bootstrap    │
    ╭──╮   └──────────────────┘
    │I'├──→
    ╰──╯   ┌──────────────────┐
           │ Specify the      │
           │ bootstrap device │
           │ by keying-in     │
           └──────────────────┘

           ┌──────────────────┐  Yes   ╭───╮
           │ Is DEVICE NOT    │───────→│ I │
           │ READY' displayed ├         ╰───╯
           │ on the CRT ?     │
           └──────────────────┘

           ┌──────────────────┐  Yes   ╭───╮
           │ Is the error     │───────→│ J │
           │ message displayed │        ╰───╯
           │ on the CRT ?     │
           └──────────────────┘

                ╭─────╮
                │ END │
                ╰─────╯
```
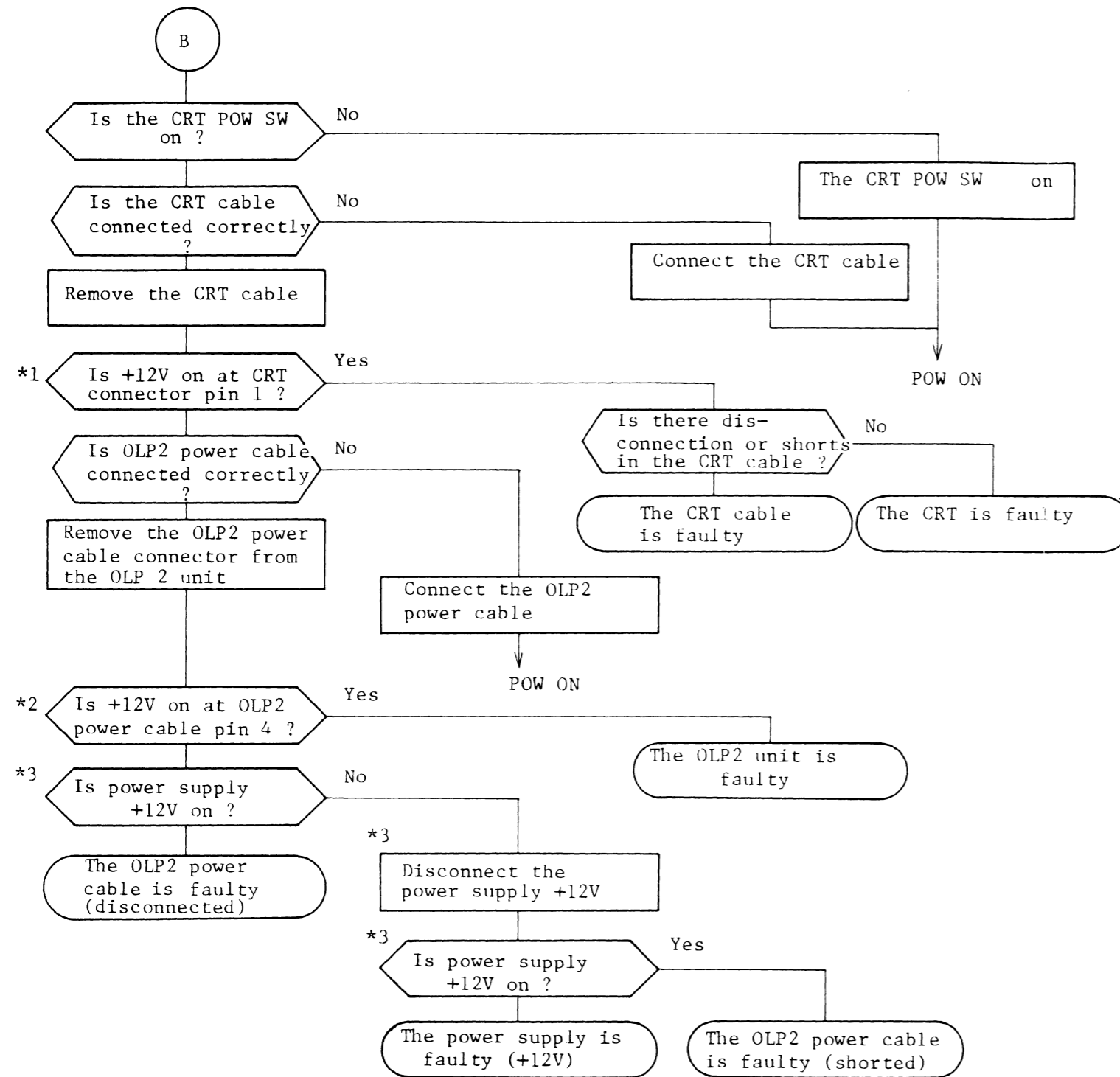
A. The fan does not turn normally

*1   See Fig. 3.3.1 Power supply for power supply +12VM.

B. The CRT POW LED does not light

B

Is the CRT POW SW on ? — No → The CRT POW SW   on

Is the CRT cable connected correctly ? — No → Connect the CRT cable

Remove the CRT cable

POW ON

*1 Is +12V on at CRT connector pin 1 ? — Yes → Is there dis-connection or shorts in the CRT cable ? — No → The CRT is faulty

The CRT cable is faulty

Is OLP2 power cable connected correctly ? — No → Connect the OLP2 power cable

Remove the OLP2 power cable connector from the OLP 2 unit

POW ON

*2 Is +12V on at OLP2 power cable pin 4 ? — Yes → The OLP2 unit is faulty

*3 Is power supply +12V on ? — No →

The OLP2 power cable is faulty (disconnected)

*3 Disconnect the power supply +12V

*3 Is power supply +12V on ? — Yes → The OLP2 power cable is faulty (shorted)

The power supply is faulty (+12V)

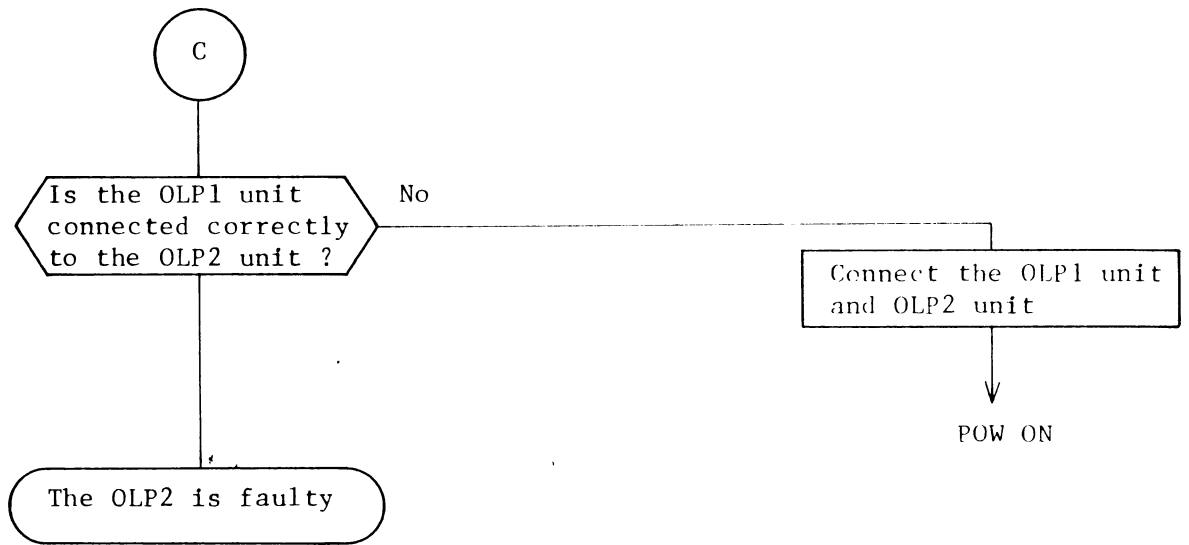*1 CRT connector pin 1

OLP2 unit

OLP2 power
*2   cable connector pin 4

*3 See Fig. 3.3.1 power supply for power supply +12V.

C. The buzzer is sounding

(C)

```
/ Is the OLP1 unit    \        No
< connected correctly   >------------------------------------------------+
\ to the OLP2 unit ?   /                                                 |
         |                                      +---------------------------+
         |                                      | Connect the OLP1 unit     |
         |                                      | and OLP2 unit             |
         |                                      +---------------------------+
         |                                                  |
         |                                                  v
 ( The OLP2 is faulty )                              POW ON
```

D. FDD is not driven (CRT displays correctly)

```
        ( D )
          │
    ┌─────┴─────┐           No
   ⟨ Is the FDD  ⟩───────────────────────┐
   ⟨ cable       ⟩                        │
   ⟨ connected   ⟩                        │
   ⟨ correctly ? ⟩                        │
          │                               │
    ┌─────┴─────┐           No       ┌──────────────────┐
   ⟨ Is the FDD  ⟩─────────────────► │ Connect the FDD  │
   ⟨ power cable ⟩                   │ cable            │
   ⟨ connected   ⟩                   └──────────────────┘
   ⟨ correctly ? ⟩
          │
*1 ┌──────┴──────┐       No     ┌────────────────────┐
   ⟨ Is +5V       ⟩───────────► │ Connect the FDD    │
   ⟨ supplied to  ⟩             │ power cable        │
   ⟨ FDD ?        ⟩             └────────────────────┘
          │               ┌──────────────────┐
          │               │ The FDD power    │
          │               │ cable is faulty  │          POW ON
          │               └──────────────────┘
*2 ┌──────┴──────┐       Yes
   ⟨ Is signal    ⟩───────────┐
   ⟨ 'DEVICE      ⟩           │
   ⟨ SELECT' on ? ⟩    ┌──────────────────┐
          │           │ The FDD is faulty │
   ┌──────┴──────┐    └──────────────────┘
   │ Remove the   │
   │ FDD cable    │
   │ from the     │
   │ OLP2 unit    │
   └──────┬──────┘
*3 ┌──────┴──────┐       Yes
   ⟨ Is a signal   ⟩──────────┐
   ⟨ on at FDD     ⟩          │
   ⟨ connector pin ⟩   ┌──────────────────┐
   ⟨ 10 of the     ⟩   │ The FDD cable is │
   ⟨ OLP2 unit ?   ⟩   │ faulty           │
          │           └──────────────────┘
   ┌──────┴──────┐
   │ The OLP2     │
   │ unit is      │
   │ faulty       │
   └─────────────┘
```

*3 See Fig. 3.3.3 OLP2 unit parts location for FDD connector pin 10 or 12.

Front bezel fixing screw
PCBA DD motor servo
DD motor Ass'y
J7(Spindle motor)
DD motor Ass'y fixing screws
J6(Stepping motor)
DD motor Ass'y fixing screw
PCBA fixing screw
PCBA fixing screws
PCBA MFD control

External view

*2
IC U201
Pin 1

Connector
J2
Pin 4
*1

PCBA MFD CONTROL, PARTS LOCATION

E. The CRT does not display (FDD is driven)

E

Is the CRT screen flowing horizontally ? — **Yes** →

Is the CRT screen flowing vertically ? — **Yes** →

* Is signal VSYNC on at the OLP2 unit TP8 ? — **No** → The OLP2 unit is faulty

Yes ↓

Is there dis-connection or shorts in the CRT cable ? — **Yes** → The CRT cable is faulty

Yes ↓

The CRT is faulty or poorly adjusted

* Is signal HSYNC on at the OLP2 unit TP9 ? — **No** → The OLP2 unit is faulty

Is there dis-connection or shorts in the CRT cable ? — **Yes** → The CRT cable is faulty

No ↓

The CRT is faulty or poorly adjusted

* Is signal VIDEO on at the OLP2 unit TP7 ? — **No** → The OLP2 unit is faulty

Is there dis-connection or shorts in the CRT cable ? — **Yes** → The CRT cable is faulty

No ↓

The CRT is faulty

* See Fig. 3.3.3 OLP2 unit parts location for TP7, TP8, and TP9.

F. The CRT does not display and the FDD is not driven

F

Does the buzzer sound lowly when the power is turned on ? — Yes → D E

*1 Is power supply +5V on ? — No

Is the OLP1 power cable connected correctly ? — No → Connect the OLP1 power cable

Is the OLP2 power cable connected correctly ? — No → Connect the OLP2 power cable

Is the OLP1 unit connected correctly to the OLP2 unit ? — No → Connect the OLP1 unit and OLP2 unit

*2 Is the OLP1 unit 8086·ROM inserted correctly into the IC receptacle ? — No → Insert the 8086·ROM into the IC receptacle

*3 Is OLP1 unit signal RESETSW at low level ? — Yes → The OLP2 unit is faulty

*4 Is OLP1 unit signal WAIT2 at low level ? — Yes → The OLP 2 unit is faulty

*5 Is OLP1 unit signal HREQ at low level ? — Yes → The OLP2 unit is faulty

The OLP1 unit or OLP2 unit is faulty

POW ON

Remove the FDD power cable from the FDD

*1 Is power supply +5V on ? — Yes → The FDD unit is faulty

Remove the OLP1 power cable from the OLP1 unit

*1 Is power supply +5V on ? — Yes → The OLP1 unit is faulty

Remove the KB cable from the main unit

*1 Is power supply +5V on ? — Yes → The KB unit is faulty

Remove the OLP2 power cable from this OLP2 Unit

*1 Is power supply +5V on ? — Yes → The OLP2 unit is faulty

Remove the OLP1 power cable from the power supply +5V

*1 Is power supply +5V on ? — Yes → The OLP1 cable is faulty

Remove the OLP2 power cable from the power supply +5V

*1 Is power supply +5V on ? — Yes → The OLP2 cable is faulty

Remove the FDD power cable from the power supplies +5V and +12VM

*1 Is power supply +5V on ? — Yes → The FDD power cable is faulty

The power supply is faulty

*1 See Fig. 3.3.1' power supply for power supply +5V.

*3
IC 1J pin 12

*4
IC 2F
pin 13

*2

*5
IC
2C pin 3

OLP1 UNIT PARTS LOCATION

G.   Erroneous key codes have been entered

```
                    ( G )
                      |
  *    / Is the specified \
      / code output to the  \  Yes
      \ OLP2 unit TP4 when  /--------------------+
       \ the key is pressed,?/                    |
                 |                      ( The OLP2 unit is )
                 |                      (     faulty      )
        ( The KB unit is )
        (    faulty      )
```

*   See Fig. 3.3.3 OLP2 unit parts location for TP4.

H. Keying-in is not possible

```
                    ( H )
                      |
        ┌─────────────────────────┐
        │ Is keying-in only       │  Yes
        │ with a particular       │──────────────────────────────────┐
        │ key                     │                                  │
        │ impossible ?            │                      ┌─────────────────────────┐
        └─────────────────────────┘                      │  The KB unit is faulty  │
        ┌─────────────────────────┐                      └─────────────────────────┘
        │ Is the KB cable         │  No
        │ connected correctly     │──────────────┐
        │ ?                       │              │
        └─────────────────────────┘     ┌─────────────────────────┐
        ┌─────────────────────────┐     │ Connect the KB cable    │
        │ Is the key #1 LED       │     └─────────────────────────┘
        │ lit ?                   │──────────┐           │
        └─────────────────────────┘          │          ▼
             │                    ┌─────────────────────────┐   POW ON
             │                    │ Turn the key #1 LED      │
             │◄───────────────────│ from on to off          │
             │                    └─────────────────────────┘
   *1 ┌─────────────────────────┐  No
      │ 4.75V < KB unit         │──────┐
      │ power voltage < 5.25V   │  Yes │  ┌─────────────────────────┐
      └─────────────────────────┘      └──│ Is the key #1 LED        │
             │ Yes                         │ on ?                     │
             │                            └─────────────────────────┘
             │                                   │ No
             │                                   ▼
             │              ┌─────────────────────────┐  Yes
             │              │ The KB cable is dis-     │──────────┐
             │              │ connected or shorts     │          │
             │              └─────────────────────────┘    ┌─────────────────────────┐
             │              ┌─────────────────────────┐    │ The KB cable is faulty  │
             │              │   The KB unit is        │    └─────────────────────────┘
             │              │       faulty            │
             │              └─────────────────────────┘
   *3 ┌─────────────────────────┐  Yes
      │ Is a signal output      │──────────┐
      │ to the OLP2 unit TP4    │          │
      │ when the key is         │   ┌─────────────────────────┐
      │ pressed ?               │   │   The OLP2 unit is      │
      └─────────────────────────┘   │       faulty            │
             │ No                    └─────────────────────────┘
   *2 ┌─────────────────────────┐  No
      │ Is KB unit signal       │──────────┐
      │ TXD output when the     │          │
      │ key is pressed ?        │   ┌─────────────────────────┐
      └─────────────────────────┘   │   The KB unit is        │
             │ Yes                   │       faulty            │
             │                       └─────────────────────────┘
      ┌─────────────────────────┐  No
      │ Is the KB cable         │──────────┐
      │ disconnected or         │          │
      │ shorted ?               │   ┌─────────────────────────┐
      └─────────────────────────┘   │   The OLP2 unit is      │
             │                       │       faulty            │
             │                       └─────────────────────────┘
      ┌─────────────────────────┐
      │ The KB cable is faulty  │
      └─────────────────────────┘
```

*3 See Fig. 3.3.3 OLP2 unit parts location for TP4.

*1
Connector pin 8

*2
Connector pin 1

KB PARTS LOCATION

I. When a diskette is inserted into the FDD, 'DEVICE NOT READY' is displayed

I

Is the diskette inserted into the FDD in a correct direction ? —No→ Set the diskette into the FDD in a correct direction → I'

*1 Is the FDD DD motor turning ? —No→

*2 Is power supply +12VM on ? —No→ Remove the FDD power cable from the FDD

Yes

*3 Is +12V$_M$ supplied to the FDD ? —No→ The FDD power cable is faulty

Yes

The FDD is faulty (DD motor drive is faulty)

*2 Is power supply +12V$_M$ on ? —Yes→ The FDD is faulty (+12V$_M$ shorts in the FDD)

*3 Is signal READY in the FDD on ? —No→ The FDD is faulty

*2 Remove the FDD power cable from the power supply +12VM

*2 Is the power supply +12VM on ? —Yes→ The FDD power cable is faulty

—No→

Is the FDD cable disconnected or shorted ? —Yes→ The FDD cable is faulty

The power supply is faulty (+12VM)

The OLP2 unit is faulty

*2 See Fig. 3.3.1 power supply for power supply +12VM.

Front bezel fixing screw — — PCBA DD motor servo

DD motor Ass'y

J7(Spindle motor) — — DD motor Ass'y fixing screws

— J6(Stepping motor)

DD motor Ass'y Fixing screw

— PCBA fixing screw

PCBA fixing screws — PCBA MFD control

External view

*3 IC U202 pin 8

PCBA MFD CONTROL. PARTS LOCATION

J. Error messages are displayed on the CRT at bootstrap time

```
                    ( J )
                      |
*1   ┌────────────────────────┐
     │Clean the FDD magnetic   │
     │head                     │
     └────────────────────────┘
                      |
     ┌────────────────────────┐
     │Execute bootstrap        │
     │action again with the    │
     │same device              │
     └────────────────────────┘
                      |
      ╱Is the error message╲   No    ( END )
      ╲displayed on the CRT╱──────►
              ?
                      |
     ┌────────────────────────┐
     │Execute bootstrap        │
     │action with another      │
     │system diskette          │
     └────────────────────────┘
                      |
      ╱Is the error message╲   No
      ╲displayed on the CRT╱──────────────────┐
              ?                     ╭──────────────────────╮
                      |             │The system diskette    │
     ┌────────────────────────┐     │is faulty              │
     │Execute bootstrap        │     ╰──────────────────────╯
     │action with a different  │
     │FDD as a specified       │
     │bootstrap device         │
     └────────────────────────┘
                      |
      ╱Is the error message╲   No
      ╲displayed on the    ╱──────────────────┐
              CRT ?                 ╭──────────────────────╮
                      |             │The first bootstrap    │
*2   ┌────────────────────────┐     │device FDD is faulty   │
     │Run the main memory      │     ╰──────────────────────╯
     │checking program         │
     └────────────────────────┘
                      |
      ╱Is there an error ?╲   Yes
      ╲                   ╱──────────────────┐
                      |             ╭──────────────────────╮
                      |             │The OLP1 unit is       │
     ╭──────────────────────╮       │     faulty            │
     │The OLP2 unit is       │       ╰──────────────────────╯
     │     faulty            │
     ╰──────────────────────╯
```

*1 See the section on FDD magnetic head cleaning of 2.3.1 cleaning standards.

*2 Run test program bootstrap loader ROM RESIDENT.

3.3.2 Trouble indentification with the test program

```
    RS232C device is
        inferior
          │
    ┌─────────────┐
   ╱ Is the RS232C device ╲  No
   ╲ cable connected      ╱────────┐
    ╲ correctly          ╱    ┌──────────────────┐
          │               │ Connect the RS232C │
          │               │ device cable       │
    ┌──────────────┐      └──────────────────┘
    │ Remove the RS232C │
    │ device cable from the │
    │ main unit         │
    └──────────────┘
*1 ┌──────────────┐
    │ Load the RS232C test │
    │ connector to run the │
    │ test program      │
    └──────────────┘
          │
   ╱ Is there an error ? ╲  No
   ╲                    ╱────────┐
          │                   │
          │            ╱ Is there disconnection ╲
          │            ╲ or shorts in the        ╱── No
          │             ╲ RS232C device cable ?  ╱    │
          │                   │            ┌──────────────┐
          │                   │            │ The RS232C device │
          │                   │            │ is  faulty       │
          │             ┌──────────────┐   └──────────────┘
          │             │ The RS232C device │
          │             │ cable is faulty   │
          │             └──────────────┘
     Yes *2
      ╱ Is power supply ╲
      ╲ -12V on ?       ╱
          │
        *2
    ┌──────────────┐
    │ Disconnect the power │
    │ supply -12V       │
    └──────────────┘
        *2
      ╱ Is power supply -12V ╲  No
      ╲ on ?                 ╱────────┐
          │                     ┌──────────────┐
          │                     │ The power supply is faulty │
          │                     └──────────────┘
   ╱ Is there disconnection ╲
   ╲ or shorts in the OLP2   ╱───── No
    ╲ power cable ?          ╱    │
          │              ┌──────────────┐
          │              │ The OLP2 unit is │
          │              │ faulty          │
          │              └──────────────┘
    ┌──────────────┐
    │ The OLP2 cable is │
    │ faulty           │
    └──────────────┘
```

```
    The parallel interface
        is inferior
          │
   ╱ Is the parallel inter- ╲  No
   ╲ face device cable       ╱────────┐
    ╲ connected correctly ?  ╱    ┌──────────────────┐
          │               │ Connect the parallel │
          │               │ interface device cable │
    ┌──────────────┐      └──────────────────┘
    │ Remove the parallel │
    │ interface device cable │
    │ from the main unit │
    └──────────────┘
*1 ┌──────────────┐
    │ Load the parallel │
    │ interface test connect- │
    │ or to run the test program │
    └──────────────┘
          │
   ╱ Is there an error ? ╲  No
   ╲                    ╱────────┐
          │                   │
          │            ╱ Is there disconnec- ╲
          │            ╲ tion or shorts in    ╱── No
          │             ╲ the parallel inter-  ╱    │
          │              ╲ face device cable ? ╱  ┌──────────────┐
          │                   │          │ The parallel │
          │                   │          │ interface device │
          │                   │          │ is faulty       │
          │             ┌──────────────┐ └──────────────┘
          │             │ The parallel │
          │             │ interface device │
          │             │ cable is faulty │
          │             └──────────────┘
    ┌──────────────┐
    │ The OLP2 unit is │
    │ faulty          │
    └──────────────┘
```

*1 Refer to TEST 4 in the test program operating manual.

*2 See Fig. 3.3.1 power supply for power supply -12V.

Fig. 3.3.1   POWER SUPPLY

A
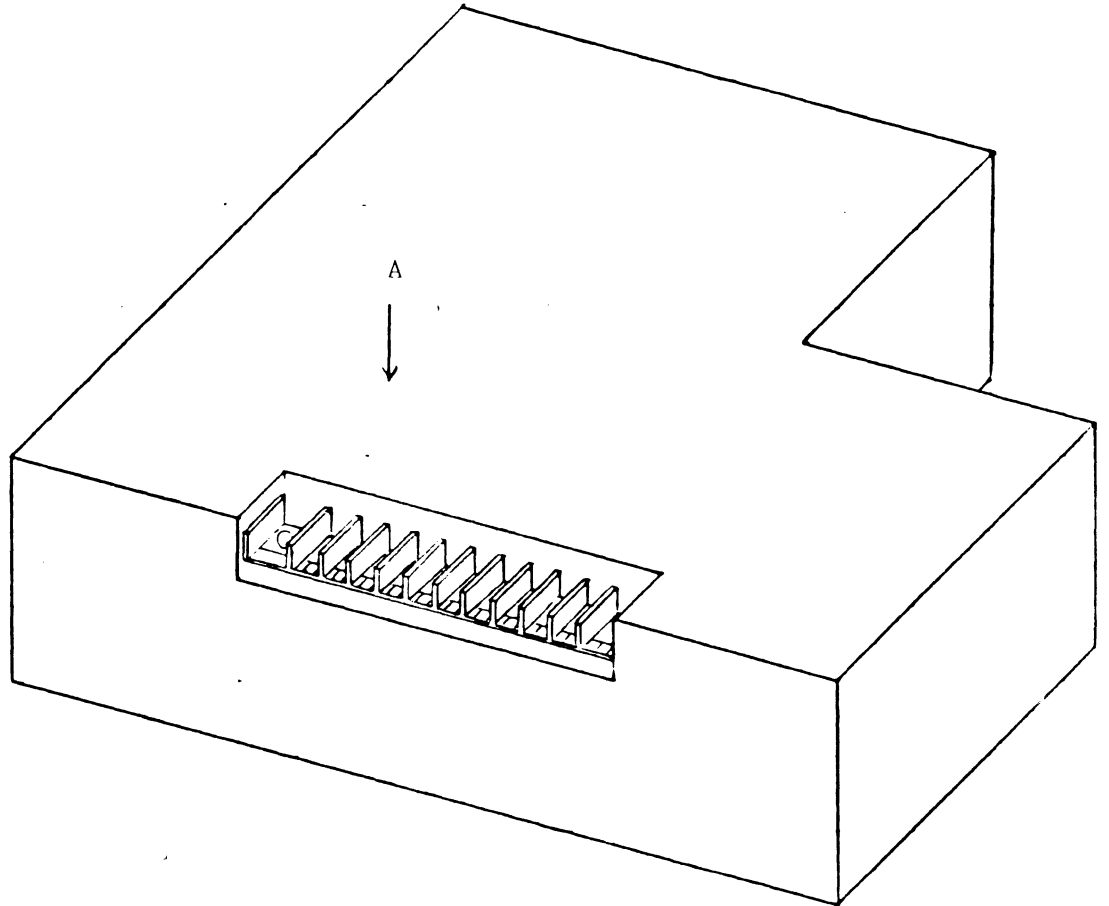
Note: Colors of cables to the power supply:
GND ----- Black   +12V ----- Red
+5V ----- Yellow   -12V ----- Orange
+12VM --- Red

As viewed from A
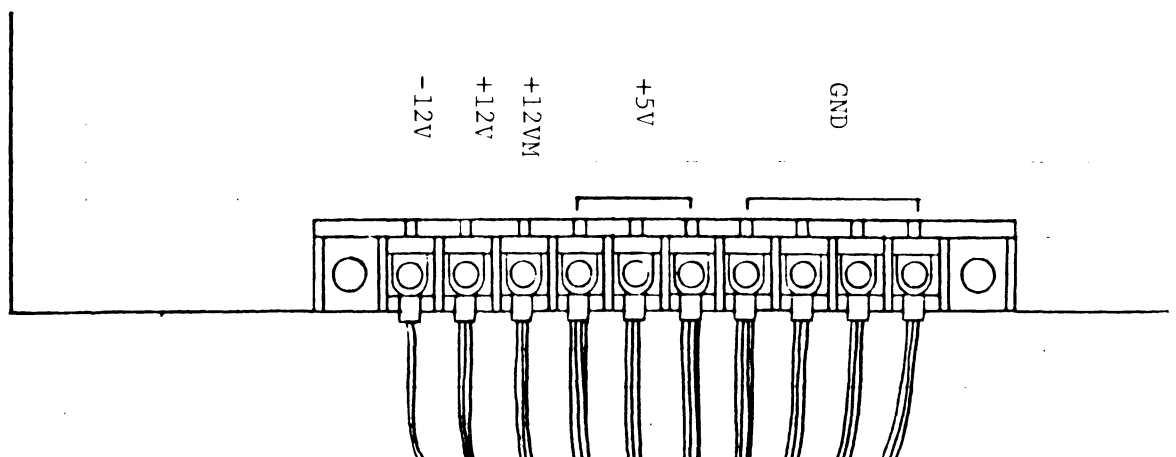
-12V +12V +12VM +5V GND
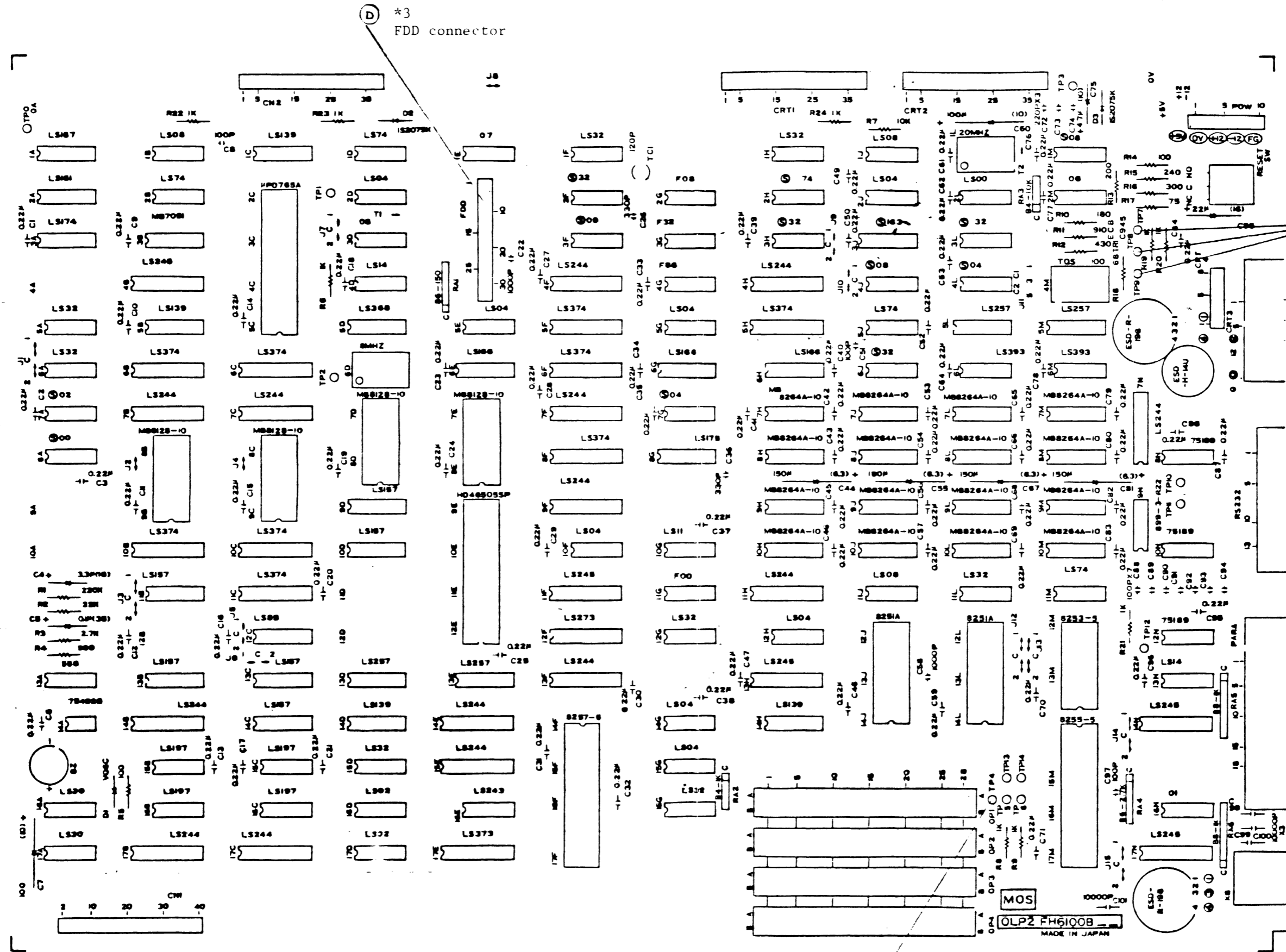
Fig. 3.3.3 OLP2 UNIT PARTS LOCATION

Appendix

(1) Keyboard troubles

The keyboard trouble modes are:

(1) Keying-in is impossible.

(2) Erroneous key codes are entered.

The checking procedures for a failing unit in each mode follow. The CPU is assumed to operate normally and the keyboard test program (TEST1) to operate.

When an error is detected in keying-in, the keyboard test program displays its contents on the CRT screen, from which its trouble mode can be known.

In the mode (1) above, the CRT screen displays the following message:

EXPECTED=XX ... XX, RECEIVED=00000000, ERROR=11111111

$$X=0 \text{ or } 1$$

With RECEIVED=00000000, ERROR=11111111, the error cause is whether key depression enters no key codes or the key is not pressed even with an elapse of 10 seconds after keying-in wait state is entered.

In the mode (2),

EXPECTED=XX ... XX, RECEIVED=YY ... YY, ERROR=ZZ ... ZZ

$\qquad$ X,Y,Z=0 or 1

Error is shown in the bit, where Z=1.

is displayed.

A list of data codes displayed is bit 2^7, bit 2^6, ..., bit 2^0 in this order from the leftmost. When an erroneous code is entered only into bit 2^6 with most keys, the KB unit CTRL key (key No. = 72) or the controller IC is considered to be faulty.

In addition, when an erroneous code is entered only with keys connected to a particular X line or Y line of the key matrix, the KB unit controller IC or Y matrix decoder driver IC is considered to be faulty.

Fig. 4-1

2
2-97
2-96
2-95
2-94
2-2
2-3~2-75
2-1
1
5
2-76
~2-93
3
4
8
6
7
9

Fig. 4-3

203
401
401
401
401
401
401
403
301
401
401
204
202
D
405
404
306
C1
E
B
404
404
A
302
404
C2
205
303
402
304
305
402
201
401

Power Supply Unit

People
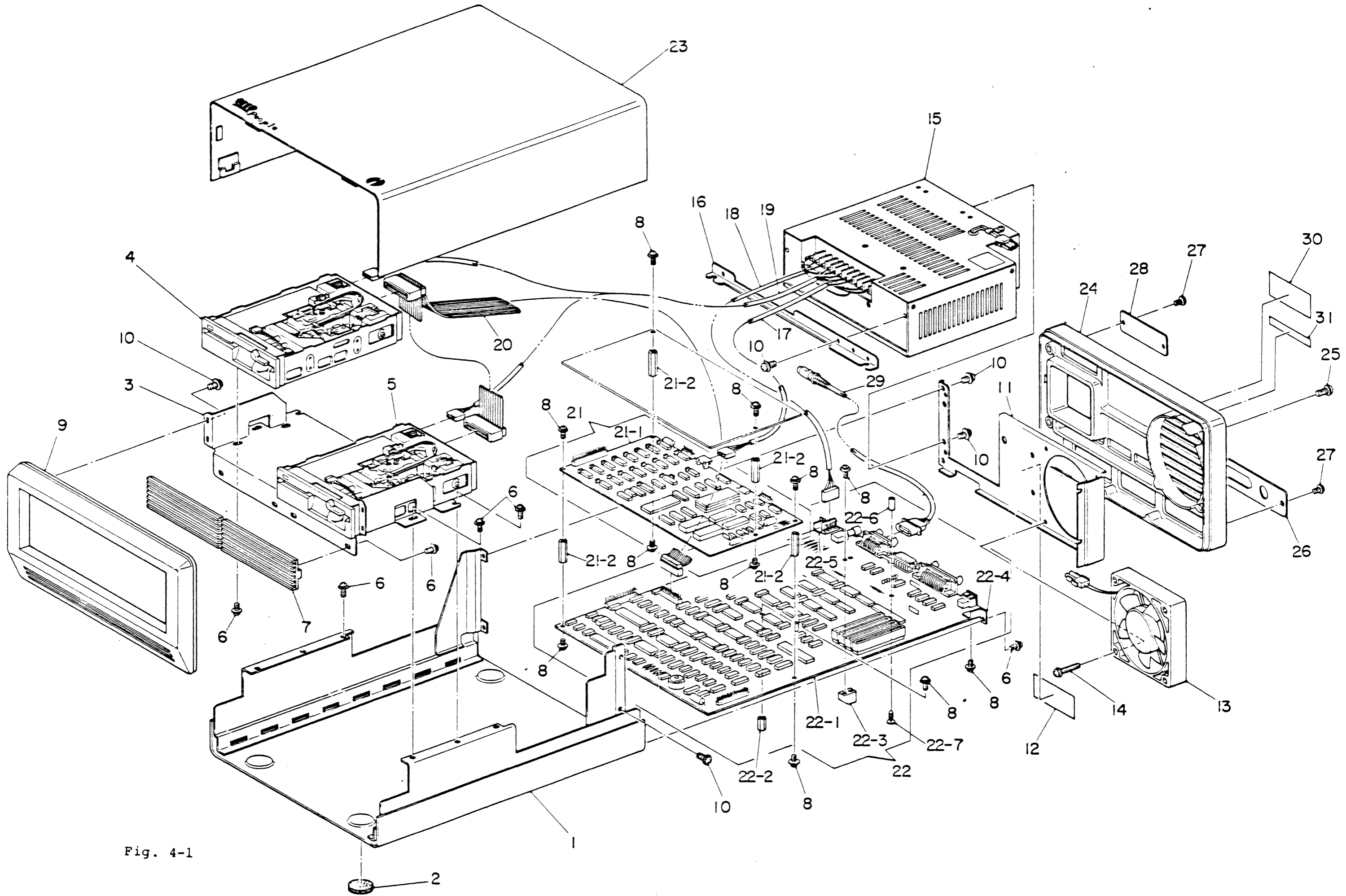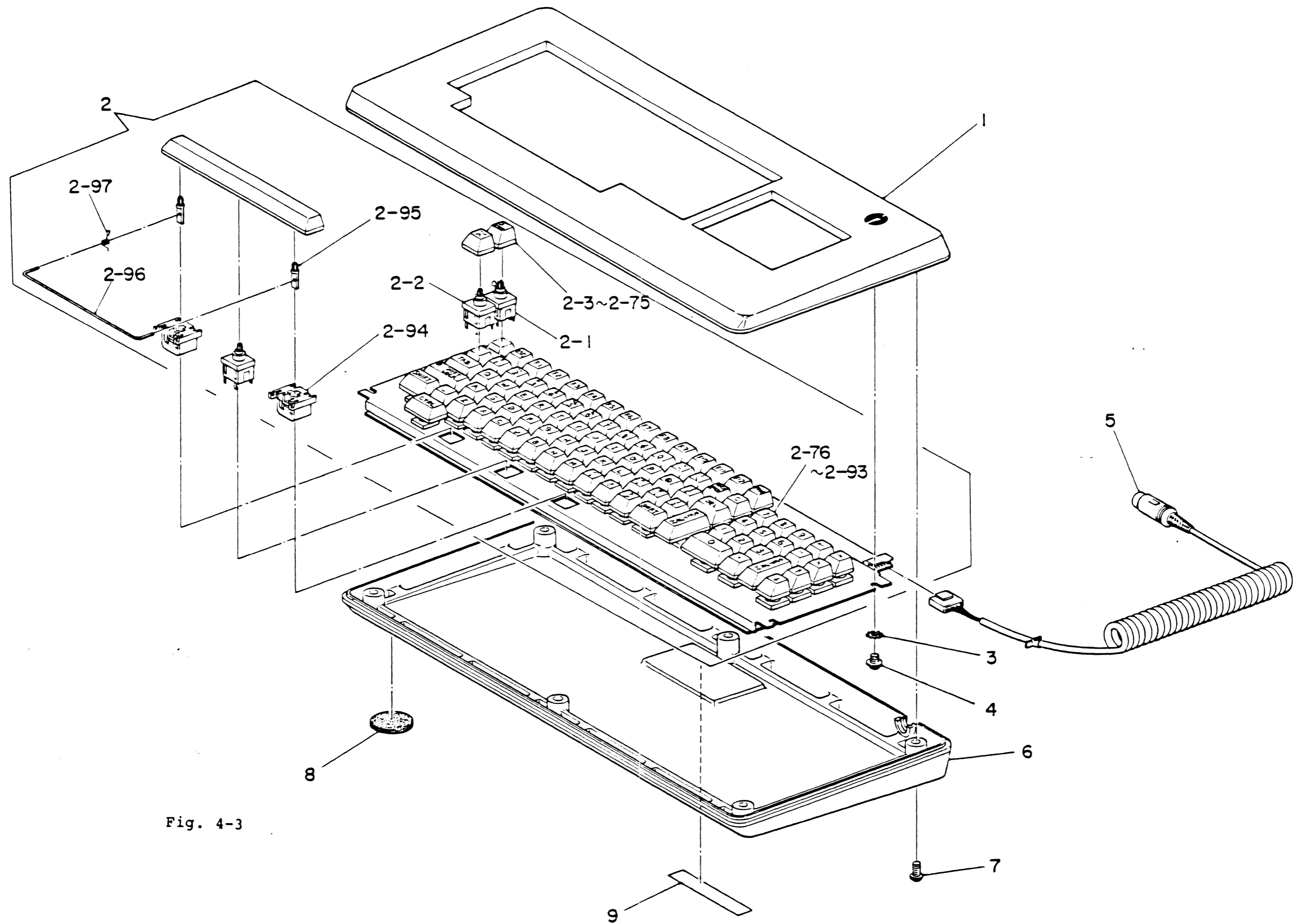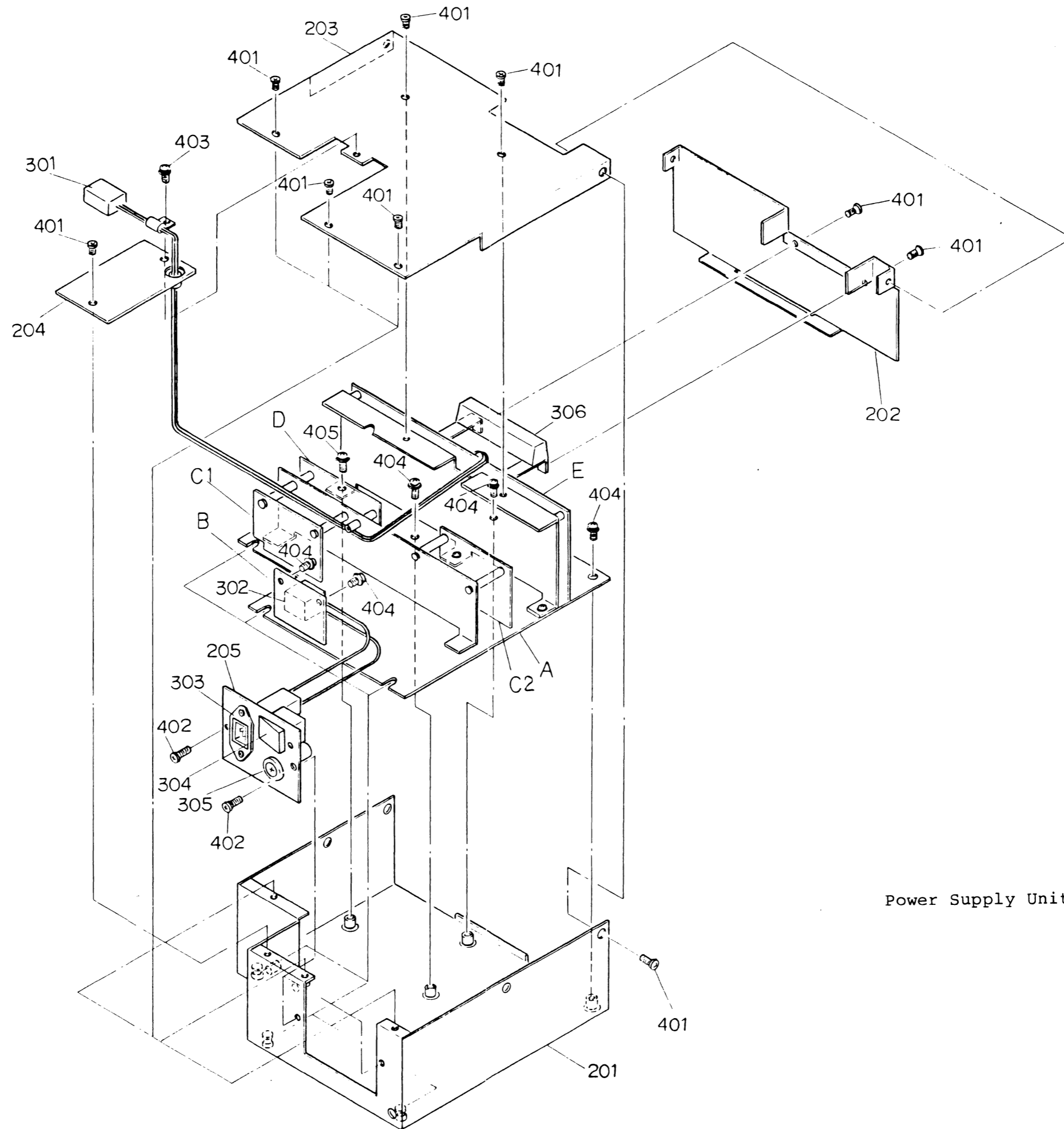
TEST PROGRAM

OPERATING MANUAL

Contents

1. Introduction

PEOPLE Test program is divided into five individual test programs, each of which is a non-resident program to be operated under the CP/M-86 Operating system as described below.

Name of Test Program	Function
TEST0	Memory Test
TEST1	Keyboard Test
TEST2	CRT Test
TEST3	Floppy Disk Test
TEST4	Interface Test

These test programs each consisting of several functions (except the KEYBOARD TEST), are capable of being freely selected or of repeating the same function. Each program can also be interrupted during the test of a particular function.

Meanings of the symbols employed in this manual are as follows:

Symbol	Meaning
(Underline)	Message displayed on CRT by test program or OS (Operating System)
⎵	Space key
<CR>	Return key
[---]	Option

2. General Operations

2-1 Starting the Program

Two methods are available for starting the program:

Process (1) A program is started first, then a function
is selected. (Serial type)

Process (2) Program start and function selection are
performed simultaneously. (Parallel type)

2-1-1   Starting Process (1)

A> TEST n <CR>   ; Start a program
                                          (n=0 to 4)

program description VERSION x.y   ; Program outline
                                           displayed.
FUNCTION# FUNCTION

        0   function-1

        1   function-2   ; Function menu displayed
        |
        |
        |
        m   function-m

TYPE IN FUNCTION#(S):   function# [, function#] <CR>

                                        ; Select function

    function name TEST -- PASSED   ; Function test operated

                or   FAILED

 ┌ function name TEST -- PASSED ┐   ;   ditto

 | or   FAILED |
 └   ┘

FUNCTION#   FUNCTION
       | |
       | |
       | |
TYPE IN FUNCTION#(S)

At the point to select functions, entering either CTRL/C or

<CR> will cause the test program to terminate.

Example

A> TEST0 <CR>

MEMORY TEST   VERSION 1.0

FUNCTION#   FUNCTION

    0   RAM TEST

    1   REFRESH TEST

    2   ADDRESS TEST

TYPE IN FUNCTION#(S): 0, 2 <CR>

    RAM TEST -- PASSED

  ADDRESS TEST -- PASSED

FUNCTION#   FUNCTION
    | |
    | |
    | |
TYPE IN FUNCTION#(S): <CR>

A>

2-1-2   Starting Process (2)

A> TEST n ␣ function# [, function#] <CR> ; Program start
                                                 and function
                                               selection
    function name TEST -- PASSED   ; Function test
                                          operation
             or   FAILED

  [function name TEST -- PASSED]   ; ditto

  [or   FAILED]

A>

Upon completion of all the tests of selected functions, the
test program will terminate automatically.

Example

A> TEST0 ⌣ 0, 2 <CR>

      RAM TEST -- PASSED

   ADDRESS TEST -- PASSED

A>

2-2 Selecting Functions

In this program, as shown in the example below, it is
possible to select a single individual function or a
number of simultaneous functions, and also to select the
same function repeatedly by using 'R'.

Example

1)	2 <CR>	; Function 2 is selected
2)	0, 1, 2 <CR>	; FUNCTIONS 0, 1, and 2 are selected
3)	0-2 <CR>	; Same result as 2)
4)	1R <CR>	; Repeating selection of FUNCTION 1 (1, 1, 1, ...)
5)	(1-3)R <CR>	; Repeating selection of FUNCTION 1 thru 3 (1, 2, 3, 1, 2, 3, ...)
6)	1-3R <CR>	; Selection of FUNCTION 1 & 2, and repeating 3. (Same as 1, 2, 3R <CR>) (1, 2, 3, 3, ...)

Note 1): Infinite repetition of functions by the
repeating selection 'R' can be released by
pressing ESC key, enabling the program to
proceed to the next step.

Note 2): Operation when a function not included in the
test program is selected or a wrong selecting
sequence entered is as follows:

a) When selecting process 2-1-1, another key
must be entered to select a function.

b) When selecting process 2-1-2, the program
will terminate.

2-3 Error Processing

If a failure is detected during test program operation,
the following message is displayed on the CRT and a
buzzer sounds, interrupting the test.

function name TEST -- FAILED

error description

At this point, by inputting a key (any key), the buzzer
stops sounding, enabling the program to proceed to
succeeding functions.

Note: The description of this section cannot be applied
to TEST1 (Keyboard test).

2-4 **Function Interruption**

Pressing the ESC key during operation of any test program will cause the function to interrupt, displaying the following message on the CRT.

<u>function name TEST -- ABORTED</u>

3. TEST 0 (Memory Test)

This test program is intended to test all the memory (except ROM, character generator memory, and CRT refresh memory). It is divided into the following three functions:

1) RAM test
2) Refresh test
3) Address test

3-1 Operation

1) <u>A></u> TEST0 <CR>   ; Start the program

   MEMORY TEST VERSION 1.1

MEMORY SIZE#	MEMORY SIZE
2	128K bytes
3	192K bytes
4	256K bytes
5	320K bytes
6	384K bytes
7	448K bytes
8	512K bytes

   TYPE IN MEMORY SIZE#:   ; Input the memory size number

FUNCTION#	FUNCTION
0	RAM TEST
1	REFRESH TEST
2	ADDRESS TEST

   TYPE IN FUNCTION# (S):   ; Input the function number
                                        to be tested

2) A> TEST0 memory size#/function# [,function#,---] <CR>

3-2 Function

3-2-1 RAM Test

TYPE IN FUNCTION#(S): 0 <CR>   ; Start the program

In this test, memory read/write check is carried out.

RAM TEST --   ; During the test

Upon test termination

RAM TEST -- PASSED   ; Normal termination

or

RAM TEST -- FAILED   ⎫ ;
BANK NO.   FAILURE BIT   ⎬ ; Abnormal termina-
                                        tion
    X   YY .... YY ⎭ ;

where, X: Memory bank number in hexadecimal notation.

YY ...YY: Sixteen-column data in binary

notation.

High-order position is 2^{15} bit,

and low-order position is 2^0

bit. Failure is shown at bit Y=1.

Note: In a memory test, the memory read/write check is performed with 64K bytes set as one memory bank to display the failed memory bank number (0 to F) and the location of the failure-detected data bit.

Memory Bank Number	Memory Address	Use
0	00000H - 0FFFFH	
1	10000H - 1FFFFH	
2	20000H - 2FFFFH	
3	30000H - 3FFFFH	
4	40000H - 4FFFFH	User memory
5	50000H - 5FFFFH	
6	60000H - 6FFFFH	
7	70000H - 7FFFFH	
8	80000H - 8FFFFH	Color CRT graphic
9	90000H - 9FFFFH	memory (Blue)
A	A0000H - AFFFFH	Color CRT graphic
B	B0000H - BFFFFH	memory (Green)
C	C0000H - CFFFFH	Graphic memory
D	D0000H - DFFFFH	(When color CRT: Red)
E	E0000H - EFFFFH	CRT refresh memory, character generator memory
F	F0000H - FFFFFH	Boot Strap ROM

(Banks 0 through B marked "Option" along the right edge.)

Table 3-1 Memory Bank Number and Memory Address

3-2-2   Refresh Test

TYPE IN FUNCTION#(S):   1 <CR>   ; Start the program

Memory refresh function check is performed.

        REFRESH TEST --   ; During the test

The test termination message is the same as that which

appears in paragraph 3-2-1.

3-2-3   Address Test

TYPE IN FUNCTION#(S):   2 <CR>   ; Start the program

The address bus line check is performed displaying

messages on CRT as follows:

        ADDRESS TEST --   ; During the test

Upon termination of test,

        ADDRESS TEST -- PASSED   ; Normal termination
or
        ADDRESS TEST -- FAILED   ; Abnormal
                                       termination

FAILURE ADDRESS LINE : XXXXXX XXXXXX

where, XX ... XX: Twenty-column address line in binary

notation.

High-order position is 2^{19} bit, and

low-order position is 2^0 bit.

Failure is shown at the line where

bit X=1.

4. TEST 1 (Keyboard Test)

This test program is intended to perform the keyboard check.

4-1 Operation

A> TEST 1 <CR>   ; Start the program

KEYBOARD TEST VERSION 1.0

Starting the program, the key arrangement drawing as shown in Fig. 4-2 (without key numbers) is displayed on the key arrangement area of the CRT as shown in Fig. 4-1.

Operation procedure:

a) Observing the comments in the comment area of the CRT, press the key indicated by the blinking cursor in the key arrangement area, in the order of the numbers shown in the key arrangement drawing (Fig. 4-2), from 1 thru 87. (Enter the key #1 twice simultaneously.)

b) After the 87th key is pressed perform the same procedure as above with the shift key held down. Repeat the same procedure once more with the CTRL key held down. The following comments are displayed in the comment area of the CRT respectively.

KEEP DEPRESSING THE SHIFT KEY

KEEP DEPRESSING THE CTRL KEY

c) When a key code other than that expected is inputted, the key code and the wrong bit are displayed in binary eight-column expression in the key code area of the CRT, and also the display of corresponding incorrectly pressed key turns to X in the key arrangement area.

EXPECTED=XX..XX, RECEIVED=YY..YY, ERROR=ZZ..ZZ

; Data: high-order position=2^7

bit low-order position=2^0 bit

; Error is shown in the bit,

where Z=1

d) Then, the buzzer sounds for about one second. Any keys pressed during this time period, are all ignored. Once the buzzer stops sounding, then succeeding keyboard operations can be continued.

If a key is not pressed for about 10 seconds, the program will be processed in the same way as for inputting an incorrect key code.

e Upon completion of all the key codes checks, the following message is displayed on the CRT to automatically terminate the program.

KEYBOARD TEST ... PASSED ; When all keys normal

or

KEYBOARD TEST ... FAILED ; When one or more error

keys are detected

```
┌─────────────────────────────────────────┐
│ KEYBOARD TEST VERSION 1.0    (1 line)    │
│─────────────────────────────────────────│
│                                          │
│         Keyboard Layout Display          │
│                    (16 lines)            │
│                                          │
│─────────────────────────────────────────│
│         Comment Area      (1 line)       │
│─────────────────────────────────────────│
│                                          │
│         Key Code Area ( 7 lines)         │
│                                          │
└─────────────────────────────────────────┘
```
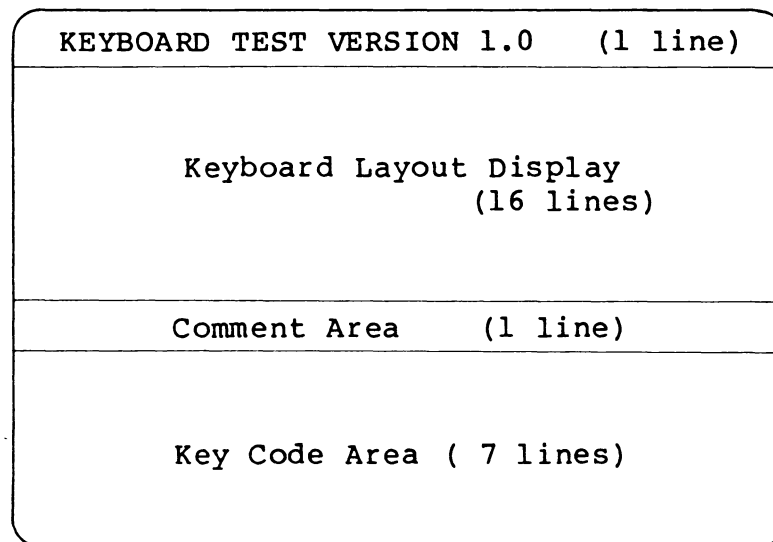
Fig. 4-1 Display Division on CRT
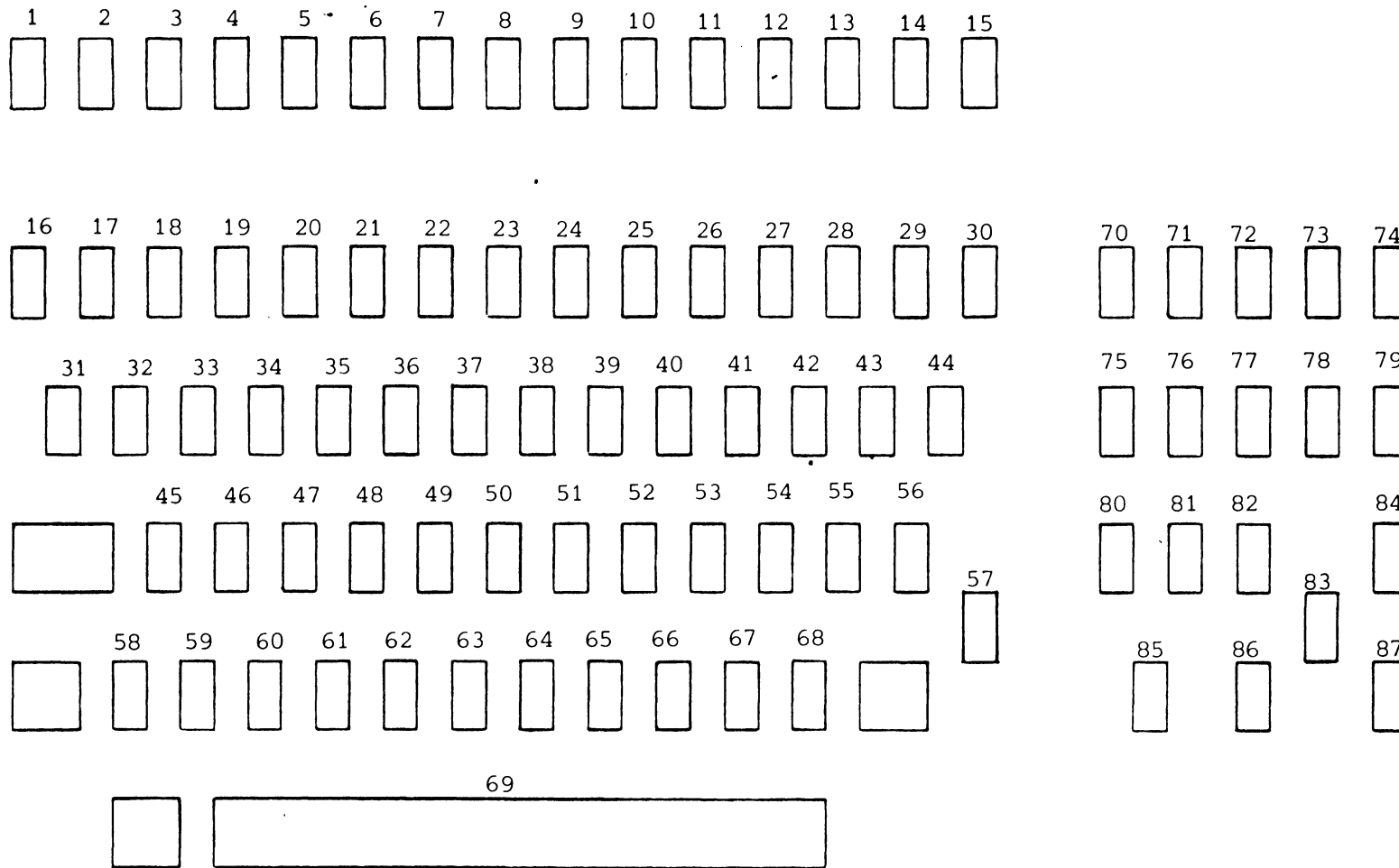
Fig. 4-2   Key Arrangement Drawing

5. **TEST 2 (CRT Test)**

    This test program is intended to perform a display test on
    the CRT, as divided into the following seven functions:

    1) Character test

    2) Screen test

    3) Cursor test

    4) Intensity test (For monochrome CRTs only)

    5) Color character test (For color CRTs only)

    6) Pattern test

    7) Color pattern test (For color CRTs only)

    In these tests, the displayed characters' quality is
    checked visually.

    Note: As described above, some functions are available
           only for color CRTs or monochrome CRTs. Incorrect
           selection of color or monochrome CRT's is ignored.

5-1 Operation

A> TEST 2 <CR>   ; Start the program

CRT TEST   VERSION 1.0

FUNCTION#   FUNCTION

      0   CHARACTER TEST

      1   SCREEN TEST

      2   CURSOR TEST

      3   INTENSITY TEST

      4   COLOR CHARACTER TEST

      5   PATTERN TEST

      6   COLOR PATTERN TEST

TYPE IN FUNCTION#(S):   ; Input the desired

                                       function number to be

                                       tested.

5-2 Function

5-2-1 Character Test

TYPE IN FUNCTION#(S): 0 <CR>   ; Start the function

All the characters which can be displayed are displayed
on CRT in the pattern shown in Fig. 5-1 for about 20
seconds, then the following message is displayed at
function termination.

CHARACTER TEST -- END

The data in Fig. 5-2 is displayed (6 lines)

The underlined data in Fig. 5-2 is displayed,
(6 lines)

Inverse data in Fig. 5-2 is displayed (6 lines)

Underlined inverse data in Fig. 5-2 is displayed
(6 lines)

Fig. 5-1 Display Pattern-1

⊔⊔⊔!⊔"⊔#⊔$⊔%⊔&⊔'⊔(⊔)⊔*⊔+⊔,⊔-⊔.⊔/⊔

⊔0⊔1⊔2⊔3⊔4⊔5⊔6⊔7⊔8⊔9⊔:⊔;⊔<⊔=⊔>⊔?

⊔@⊔A⊔B⊔C⊔D⊔E⊔F⊔G⊔H⊔I⊔J⊔K⊔L⊔M⊔N⊔O⊔

⊔P⊔Q⊔R⊔S⊔T⊔U⊔V⊔W⊔X⊔Y⊔Z⊔[⊔\⊔]⊔^⊔_⊔

⊔`⊔a⊔b⊔c⊔d⊔e⊔f⊔g⊔h⊔i⊔j⊔k⊔l⊔m⊔n⊔o⊔

⊔p⊔q⊔r⊔s⊔t⊔u⊔v⊔w⊔x⊔y⊔z⊔{⊔|⊔}⊔~⊔⊔⊔

Fig. 5-2 Displayed Data-1

5-2-2 Screen Test

TYPE IN FUNCTION#(S) : 1 <CR>   ; Start

The character 'H' is displayed all over the CRT screen
for about 20 seconds, thereafter the following message
is displayed to terminate this function.

SCREEN TEST -- END

5-2-3 Cursor Test

<u>TYPE IN FUNCTION#(S):</u> 2 <CR>   ; Start the function

The cursor is checked for read/write functions by
constructing quadrangle on the CRT.
Upon completion of the test, the following message is
displayed at function termination.

    <u>CURSOR TEST -- PASSED</u>   ; Normal termination

    or

    <u>CURSOR TEST -- FAILED</u>   ; Abnormal termination

When abnormal termination occurs, the '$' mark is
displayed at it's normal cursor position and the '#'
mark is displayed at the cursor position where the
abnormality is found.

5-2-4 Intensity Test (for Monochrome CRTs only)

TYPE IN FUNCTION#(S): 3 <CR>   ; Start the function

Changing the intensity, characters are displayed on the CRT in a pattern as shown in Fig. 5-3 for about 20 seconds, then the following message is displayed at function termination.

INTENSITY TEST -- END

```
Data of Fig. 5-4 is displayed (6 lines)

Data of Fig. 5-4 is underlined are displayed
(6 lines)

Inverse data in Fig. 5-4 is displayed (6 lines)

Inverse data of Fig. 5-4 is underlined and
displayed (6 lines)
```

Fig. 5-3 Display Pattern-2

Intensity 0 — Intensity 1 — Intensity 2 — Intensity 3

```
⌴0  1  2  3  4  5  6  7  8  9  0 ～ 9  0 ～ 9  0 ～9⌴
              "                    "       "       "
              "                    "       "       "ˇ
              "                    "       "       "
              "                    "       "       "
              "                    "       "       "
```

Fig. 5-4 Display Data-2

5-2-5 Color Character Test (for color CRTs only)

TYPE IN FUNCTION#(S):   4 <CR>   ; Start the function

Changing the color, characters are displayed on the CRT in a pattern as shown in Fig. 5-5 for about 20 seconds, then the following message is displayed at function termination.

COLOR TEST -- END

8 lines	{	⌴ 0 ~ 9 0 ~ 9 Blue	0 ~ 9 0 ~ 9 Red	0 ~ 9 0 ~ 9 ⌴ Green
8 lines	{	⌴ 0 ~ 9 Cyanic	0 ~ 9 0 ~ 9 Magenta	0 ~ 9 0 ~ 9 Yellow	0 ~ 9 ⌴ Cyanic
8 lines	{	⌴ 0 ~ 9 0 ~ 9 0 ~ 9 White		

Fig. 5-5 Display Pattern-3

For each 8 lines, normal, underlined, reverse, and underlined reverse data are displayed on two lines, respectively.

5-2-6 Pattern Test

TYPE IN FUNCTION#(S): 5 <CR> ; Start the function

The overall page display and grid display are performed
in graphic mode in the patterns shown in Fig. 5-6 and
Fig. 5-7 for about 20 seconds respectively, then the
following message is displayed at function termination.

PATTERN TEST -- END
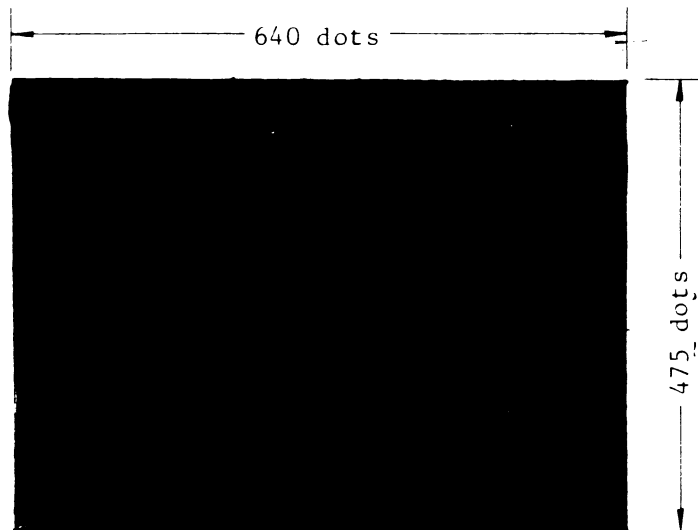
Fig. 5-6 Display Pattern-4
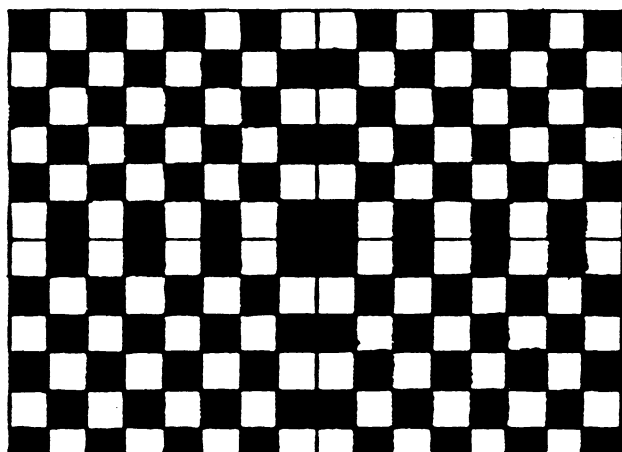
	Vertical	Horizontal
Each Grid	40 dots	40 dots
Bottom Grid	35 dots	40 dots

Fig. 5-7 Display Pattern-5

5-2-7 Color Pattern Test (For Color CRT only)

<u>TYPE IN FUNCTION#(S)</u>:   6 <CR>   ; Start

The color pattern is displayed in graphic mode as shown in Fig. 5-8 for about 20 seconds, then the following message is displayed when the function is terminated.

<u>COLOUR PATTERN TEST ... END</u>
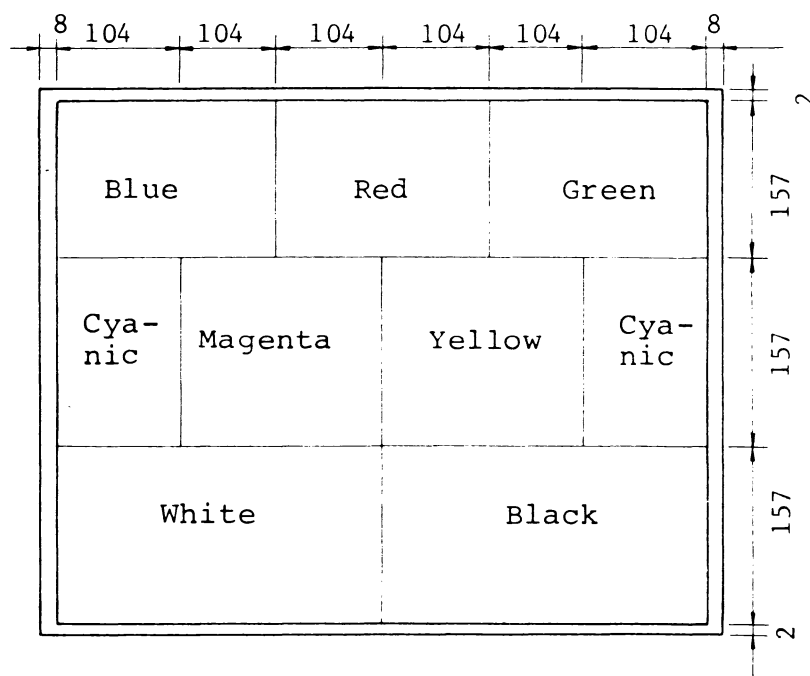
Figures shown here represent number of dot used.

Fig. 5-8   Display Pattern-6

6. TEST 3 (Floppy Disk Test)

This test program is intended to perform a functional check of the floppy disk drive. It is divided into the following nine functions:

1) Drive A recalibration test

2) Drive A formatting and CRC test

3) Drive A seek test

4) Drive A read/write test

5) Drive B recalibration test

6) Drive B formatting and CRC test

7) Drive B seek test

8) Drive B read/write test

9) Copy test on drive A and B

Note: Since diskette contents are destructed by this test, after the test program is loaded, the mounted diskette should be replaced with a work diskette. (A message instructing diskette replacement is displayed on the CRT)

6-1 Operation

A > TEST3 <CR>   ; Start the program

FLOPPY DISK TEST VERSION 1.0

ALL DISKETTE FILES ON DRIVES TO BE TESTED WILL BE DESTROYED.

LOAD WRITE ENABLED WORK DISKETTE INTO ANY DRIVE TO BE TESTED.

DEPRESS RETURN KEY WHEN READY TO CONTINUE.

                                    ; Replace the present

                                      diskette with the work

                                      diskette, then press the

                                      return key to proceed to

                                      the next step.

FUNCTION#   FUNCTION

    0   A: RECALIBRATE TEST

    1   A: FORMATTING & CRC TEST

    2   A: SEEK TEST

    3   A: READ/WRITE TEST

    4   B: RECALIBRATE TEST

    5   B: FORMATTING & CRC TEST

    6   B: SEEK TEST

    7   B: READ/WRITE TEST

    8   A: & B: COPY TEST

<u>TYPE IN FUNCTION#(S):</u>   ; Input the function number

                                             to be tested

6-2 Function

6-2-1 Recalibration Test

<u>TYPE IN FUNCTION#(S):</u> 0 <CR> or 4 <CR> ; Start the

                                                      function

The read/write head is checked for the return to track 0.

<u>d: RECALIBRATE TEST --</u>   ; During the test

Upon completion of the test, the following message is
displayed on CRT.

<u>d: RECALIBRATE TEST -- PASSED</u>   ; Normal termination occured

or

<u>d: RECALIBRATE TEST -- FAILED</u> ⎫   ; Abnormal termination

      <u>error description</u>   ⎬

                                   ⎭

where, d denotes the name of drive A or B, to be tested.

      Refer to Section 6-4 for details of error

      descriptions.

6-2-2   Formatting and CRC Test

TYPE IN FUNCTION#(S):   1 <CR> or 5 <CR> ; Start the function

The diskette formatting function and the CRC function of the
ID field and the data field are checked.
The test termination message corresponds to paragraph 6-2-1,
"Recalibrate test".

6-2-3   Seek Test

TYPE IN FUNCTION#(S):   2 <CR> or 6 <CR> ; Start the function

The seek function of read/write head is tested.
The test termination message corresponds to paragraph 6-2-1,
"Recalibrate test".

6-2-4   Read/Write Test

TYPE IN FUNCTION#(S):   3 <CR> or 7 <CR> ; Start the function

Data read and write functions are checked.
The test termination message corresponds to paragraph 6-2-1,
"Recalibrate test".

6-2-5 Copy Test

TYPE IN FUNCTION#(S): 8 <CR> ; Start the function

The data copy function is checked for drives A and B.

The test termination message corresponds to paragraph 6-2-1,

"Recalibrate test".

6-3 Terminate Operation

Upon test program termination the following message is

displayed on the CRT.

FLOPPY DISK TEST COMPLETED. NOW, REMOVE WORK DISKETTE(S)

AND LOAD THE CERTAIN DISKETTE INTO ITS DRIVE.

DEPRESS RETURN KEY WHEN READY TO CONTINUE.

; Here, replace the diskette, then press the return key to

   terminate the test program.

6-4   Error Messages

When a failure is detected by the floppy disk test program, one of the following error messages is displayed on the CRT.

1) d: DRIVE NOT READY

2) d: RECALIBRATE ERROR

3) d: SEEK ERROR

4) d: DATA ADDRESS MARK NOT FOUND

5) d: ID ADDRESS MARK NOT FOUND

6) d: WRITE PROTECTED

7) d: BAD TRACK MARK DETECTED

8) d: SECTOR NOT FOUND

9) d: DATA FIELD CRC ERROR

10) d: ID FIELD CRC ERROR

11) d: DELETED DATA ADDRESS MARK DETECTED

12) d: READ/WRITE DATA UNMATCHED

7. **TEST 4 (Interface Test)**

This test program is intended to carry out the following interface test:

1) Parallel port test

2) Serial port test

3) Timer test

4) Interrupt test

Prior to carrying out the tests; 1), 2), or 4), connect the two testing connectors for the printer and the RS232C terminal to parts ① and ② in Fig. 7-1 respectively.

Note: Two connectors used for the above tests must be previously prepared connecting the corresponding pins of each connector in the manner shown in Table 7-1 and 7-2.

Table 7-1 Connecting Pin No. of the Printer Connector	Table 7-2 Connecting Pin No. of the RS232C Connector
o 2 - 11	o 2 - 3
o 3 - 12	o 4 - 5
o 4 - 32	o 6 - 20
o 5 - 35	
o 6 - 13	
o 7 - 36	
o 8 - 15	
o 9 - 10	
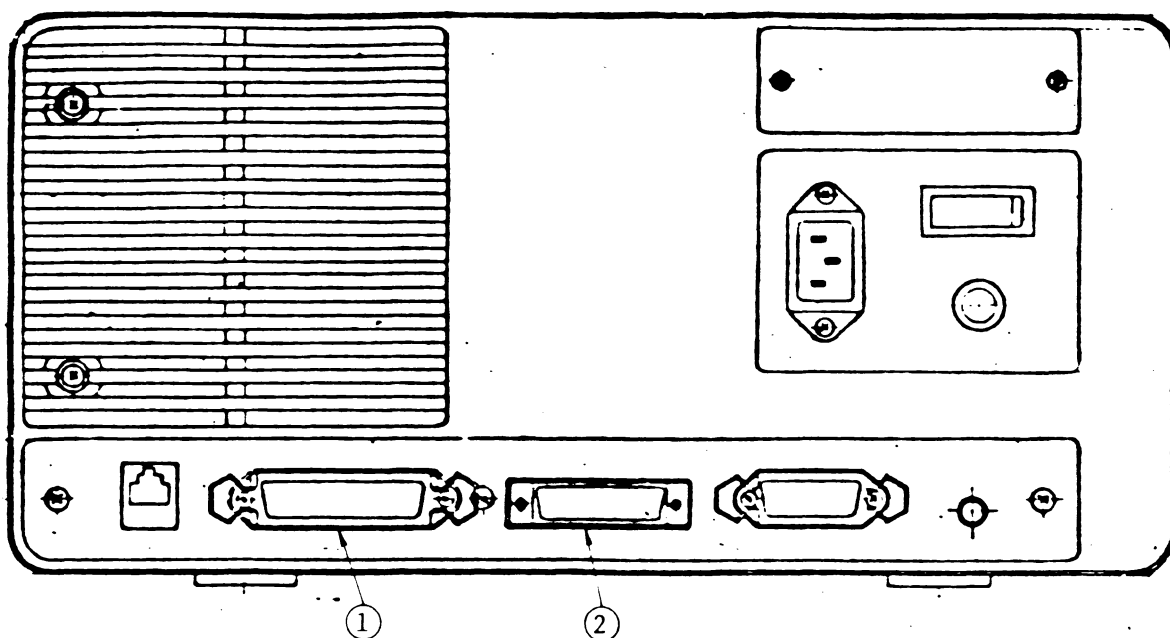
Fig. 7-1   Back View of PEOPLE Body

<u>PARALLEL PORT TEST -- PASSED</u>   ; Normal termination

or

<u>PARALLEL PORT TEST -- FAILED</u>   ⎤   ; Abnormal termination

<u>FAILURE BIT(S) = XXXXXXXX</u>   ⎦

where, XX...XX is a 8-position in binary number.

The high-order position is 2^7 bit, and the

low-order position is 2^0 bit.

A failure in the parallel port input/output is shown

where X=1.

7-2-2   Serial Port Test

<u>TYPE IN FUNCTION#(S):</u>   1 <CR>   ; Start the function

The transmission circuit is checked at a transmission speed
of 9600 bauds and with a data item length of 256 bytes.

<u>SERIAL PORT TEST --</u> ;   During the test

On test termination, the following message is displayed on
the CRT:

<u>SERIAL PORT TEST -- PASSED</u> ; Normal termination

or

<u>SERIAL PORT TEST -- FAILED</u>

<u>TIME OUT ERROR</u>

or   ; Abnormal termination

<u>SERIAL PORT TEST -- FAILED</u>

<u>ERROR = n1</u>

<u>FE = n2</u>

<u>OE = n3</u>

<u>PE = n4</u>

where, n1: Unmatched item count

   n2: Framing error count

   n3: Overrun error count

   n4: Parity error count

7-2-3 Timer Test

<u>TYPE IN FUNCTION#(S):</u> 2 <CR> ; Start the function

The timer test is performed.

  <u>TIMER TEST --</u>   ; During the test

On test termination, the following message is displayed on the CRT:

TIMER TEST -- PASSED   ; Normal termination

or

TIMER TEST -- FAILED   ; Abnormal termination

7-2-4 Interrupt Test

TYPE IN FUNCTION#(S):   3 <CR>   ; Start the function

The interface test is carried out for the floppy disk drive, transmission, and timer in that order.
Every time the   interruption check terminates, the following message is displayed on the CRT.

dev. INTERRUPT TEST -- PASSED   ; Normal termination

or   FAILED   ; Abnormal termination

where, dev. denotes FD, SERIAL, or TIMER.

People

FLOPPY DISK DRIVE   TEAC FD-55
MAINTENANCE MANUAL

People

TABLE OF CONTENTS

Title	Page

CONSTRUCTION AND FUNCTION

General Block Diagram

READ DATA — Read circuit

SIDE ONE SELECT

WRITE PROTECT
WRITE GATE — Write circuit
WRITE DATA

Indi-cator

File protect sensor
File protect sensor LED
Disk
Index sensor
Index sensor LED
Spindle motor

DRIVE SELECT 0∿3

MOTOR ON
STEP
DIRECTION SELECT

Control circuit

Servo circuit

IN USE or HEAD LOAD

TRACK 00
INDEX
READY

Magnetic head
Head load solenoid
Track 00 sensor
Stepping motor

+12V,+5V,0V

(Fig.301) General block diagram

Magnetization
on disk

Pre-amp.output
(TP7)

Shoulder

6V
approx.

Pre-amp.output
(TP8)

6V
approx.

Saddle

Differentiation
amp.output
(TP9)

6V,approx.

Zero-cross point

Differentiation
amp.output
(TP10)

6V,approx.

Peak detector
output
(U304,pin7)
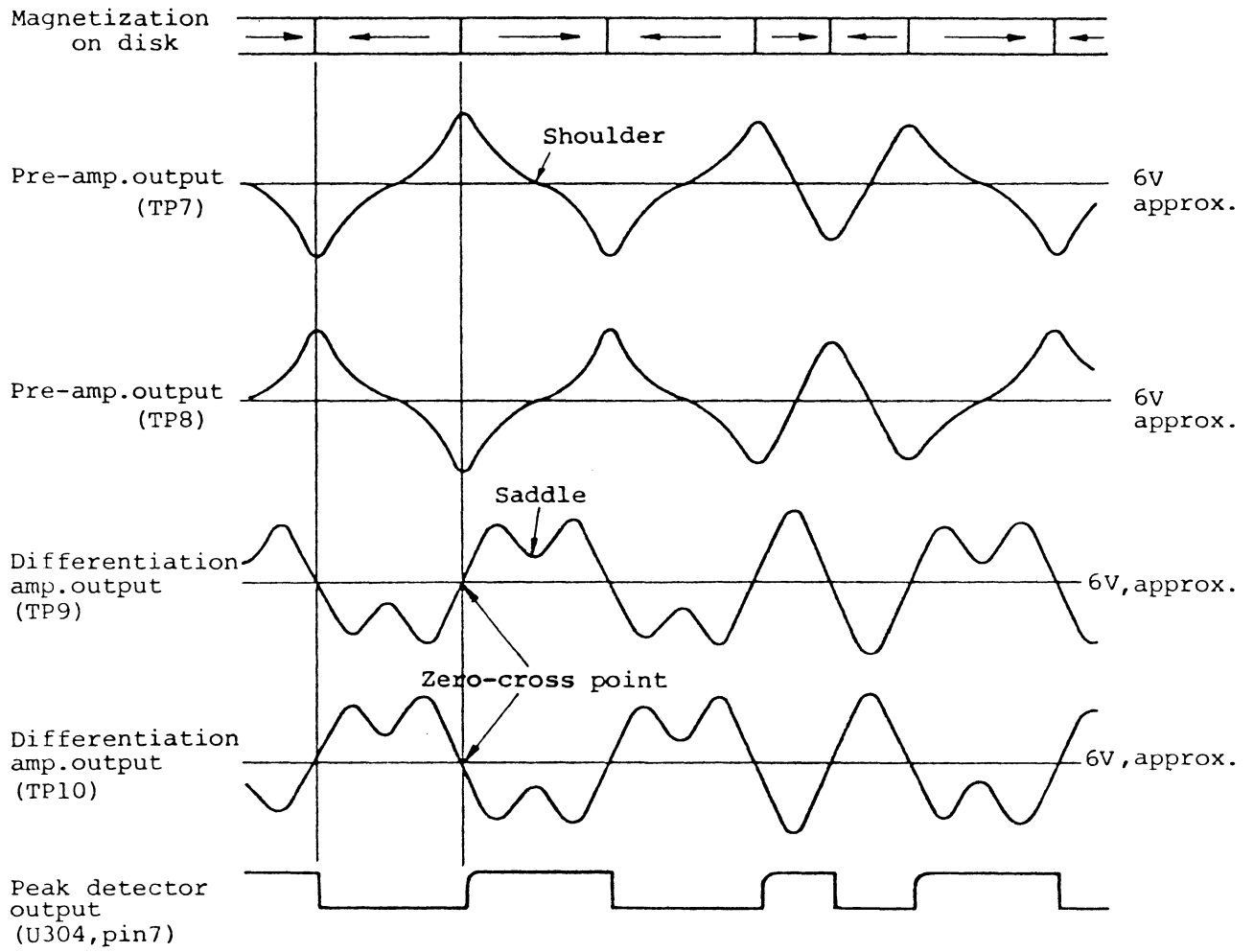
(Fig.303) Read amp. and peak detector waveforms

⌐ Virtual pulse (drop-in)

Peak detector
output   ____⎍__⎍⎍__⎍__⎍____⎍__⎍__⎍_____⎍____
(U304,pin7)

Bidirectional S.S.
#1 output   ___⎍__⎍⎍_⎍_____⎍___⎍_⎍_⎍____⎍____
(U303,pin11)
                       ⊢⊣⊢ 2.4μs,approx.

2.4μs delay S.S.
Q̄ output   ⎍_⎍_⎍_⎍___⎍_⎍_⎍_⎍⎍_⎍____⎍_
(U301,pin4)

Data latch output   ____⎍____⎍____⎍__⎍__⎍____⎍_
(U302,pin5)

Bidirectional S.S.
#2 output   ___⎍___⎍___⎍__⎍_⎍_⎍____⎍__
(U303,pin8)
                       ⊢⊣⊢ 1μs,approx.

READ DATA   ⎍___⎍___⎍___⎍_⎍_⎍____⎍_
(U202,pin6)
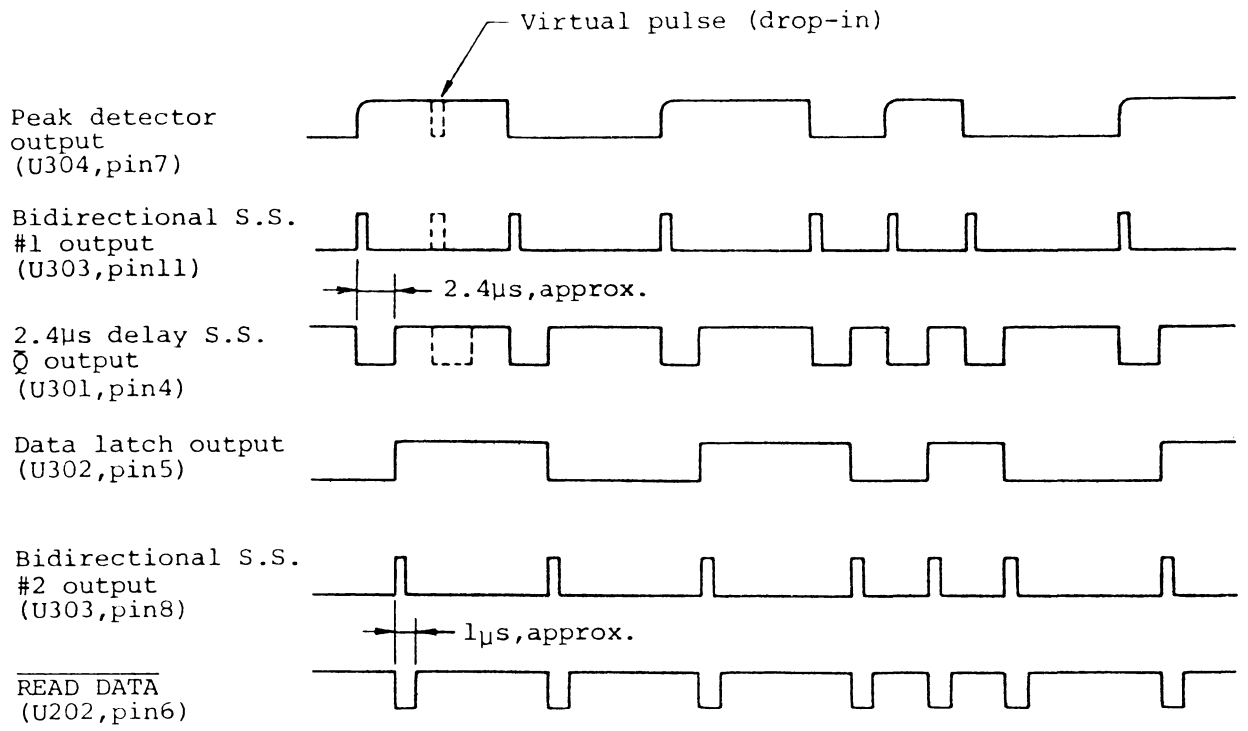
        (Fig.304) Time domain filter and read gate waveforms

Erase off
delay

Write gate output
(U213,pin6)

Erase gate output
(TP2)

Side select gate
output
(Head common)

Write data input
(U302,pin11)

Data latch output
(U302,pin9)

Data latch output
(U302,pin8)

TP11

Write current

Magnetization on
disk

Magnetized
previously
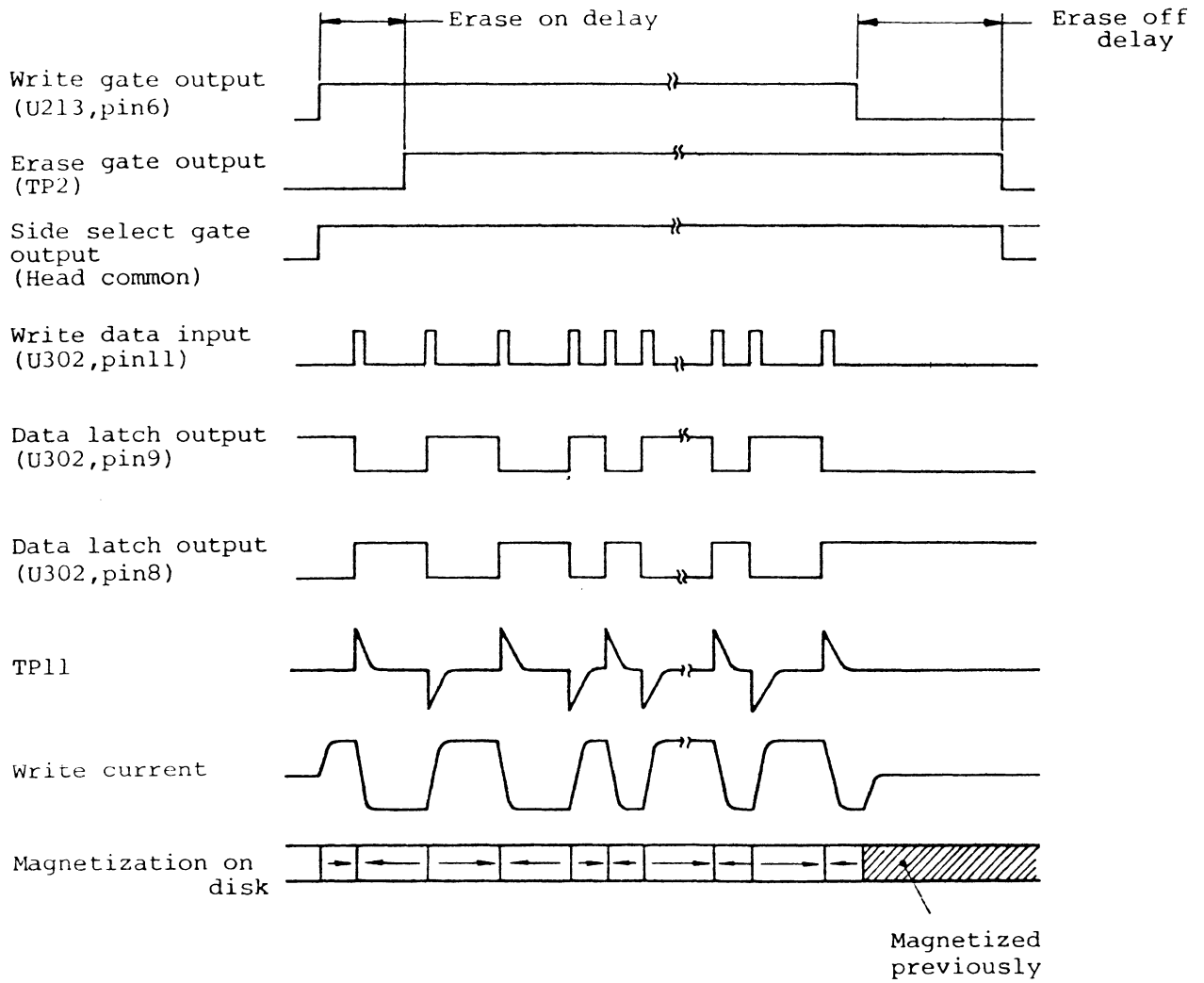
(Fig.305) Write circuit waveforms

FUNCTION OF TEST POINTS AND VARIABLE RESISTORS

Fig.309 shows the mounting positions of the test points and variable
resistors.

PCBA read write amp.

PCBA MFD control

PCBA DD motor servo
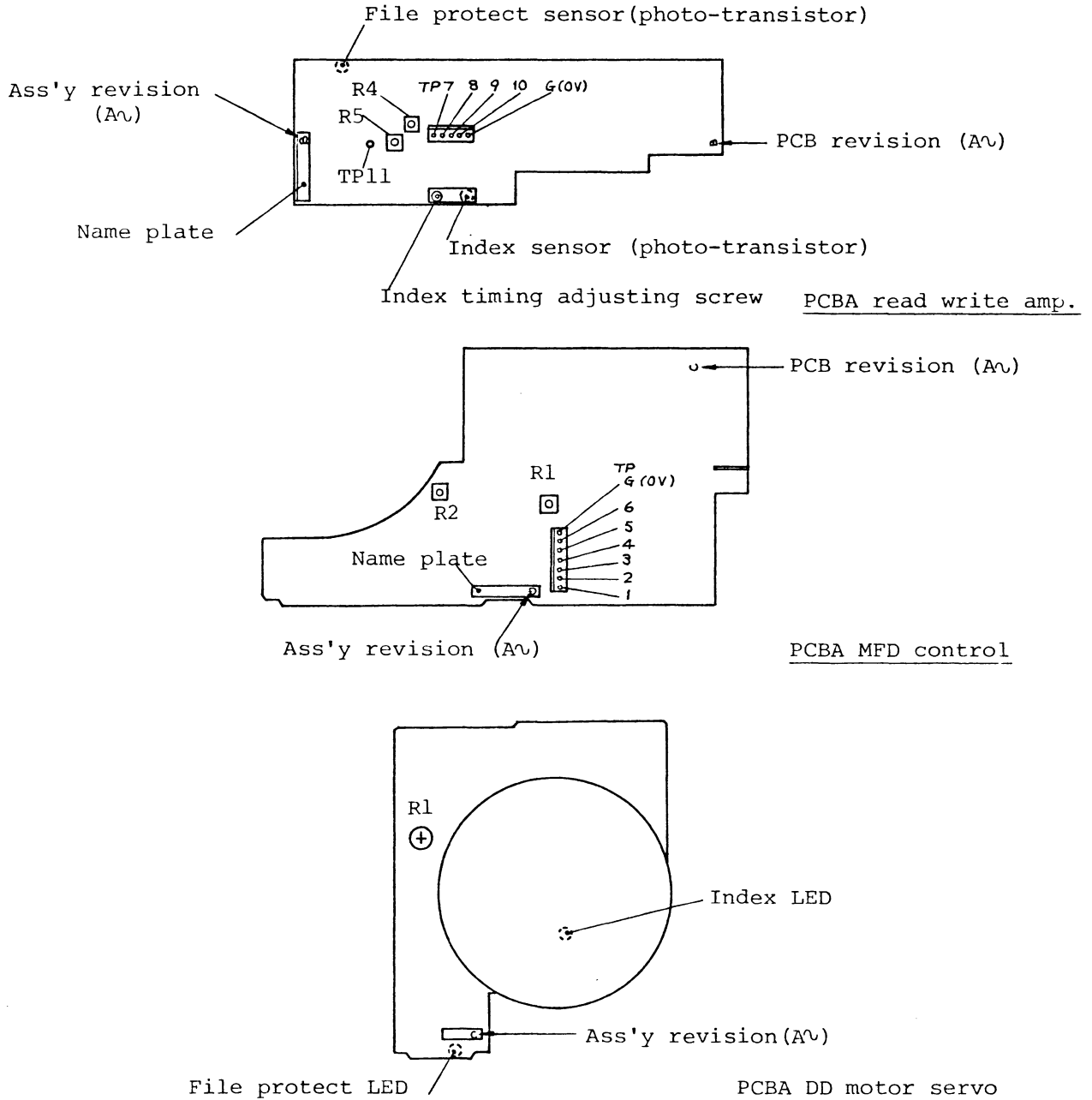
Note: Some versions have not all the test points (TP) and all the
variable resistors (R) above.

(Fig.309) Location of test points and variable resistors

TP4 (Index) -- PCBA MFD control

Test point to observe the output of the index detection photo-transistor
after inverting the level by the Schmitt inverter.
The signal level at this TP is opposite to that of the INDEX output
signal. When the index hole or sector hole (hard sectored disk) is
detected, HIGH going pulse is observed at TP4. The photo-transistor is
mounted on the PCBA read write amp. and the LED is mounted on the PCBA
DD motor servo.
The test point is used for the following purposes.

(a) Confirmation and ajustment of the disk rotational speed. Speed is
    adjusted by the variable resistor R1 on the PCBA DD motor servo.
(b) Confirmation and adjustment of the index burst timing. Burst timing
    is adjusted by the index adjusting screw on the PCBA read write amp.

TP4 (Index)

Index
interval   Pulse width
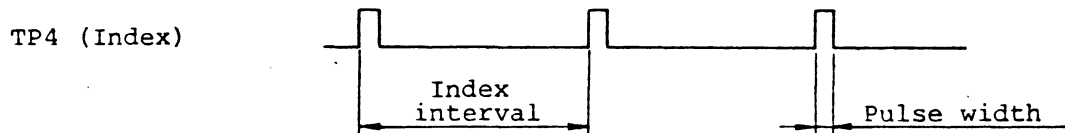
(Fig.313) Typical waveform of TP4 (speed observation)

Items	FD-55A ∿ F
Index interval	200±3ms
Pulse width	2 ∿ 5.5ms
Burst delay	200±200µs

(Table 302) Index timing

TP4(Index)

TP7 or 8
(Pre-amp. output)

Index burst delay
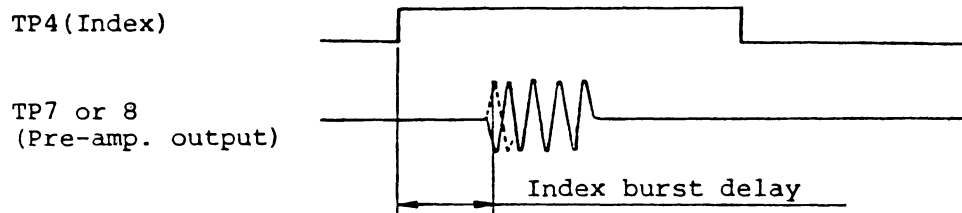
(Fig.314) Typical waveform of TP4 (Burst timing observation)

TP5 (Read data) -- PCBA MFD control

Test point to observe the read data pulse.
The signal level at this TP is opposite to that of the READ DATA output signal.

TP5 (Read data)

2F interval

4/3F interval

1F interval

Pulse width
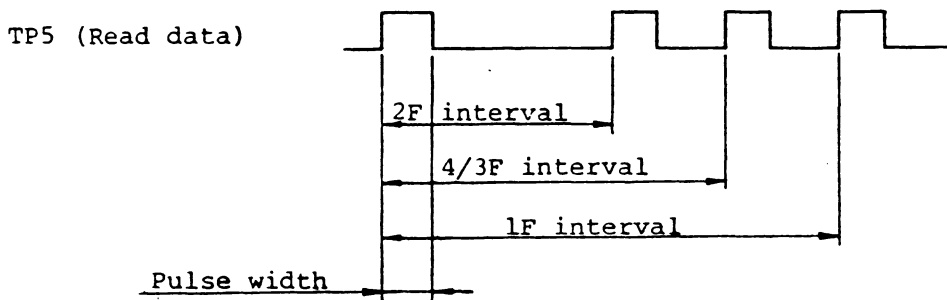
(Fig.315) Typical waveform of TP5

Fig.315 shows the waveform at TP5 in normal data read operation.
In the FM method, 2F and 1F intervals are observed, while 2F, 4/3F, and 1F intervals are observed in the MFM method.

Items	FD-55A ∿ F
2F interval	4μs, Nom.
4/3F interval	6μs, Nom.
1F interval	8μs, Nom.
Pulse width	1±0.5μs

(Table 303) Read data pulse timing

TP6 (File protect sensor) -- PCBA MFD control

Test points to observe the output of the file protect detection photo-
transistor.

The signal level at this TP is opposite to that of the WRITE PROTECT
output signal. When a disk with the masked write protect notch (write
operation cannot be done) is installed, TP6 becomes HIGH level.

The voltage of TP6 should be more than 3V at masked notch and less
than 0.5V at open notch (write enable condition).

TP6(File protect sensor)

                                                    ———————— 3.0V,Min.

                              ———————————┤   ———————— 0.5V,Max.

              Notch open ◄———┤   ┝——► Notch masked
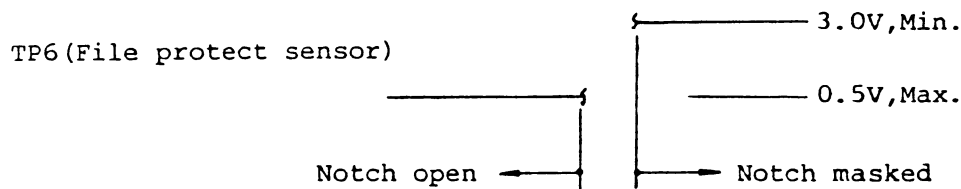
(Fig.316) Typical waveform of TP6

TP7, TP8 (Pre-amplifier) -- PCBA read write amp.

Test point to observe the read pre-amplifier output signals.

The pre-amplifier has two outputs of the order of several dozen to
several hundred mVp-p, and they differ in phase by 180° (opposite phase).
Both outputs are observed at TP7 and TP8 respectively.

For an accurate observation of the read waveforms, use two channels of
an oscilloscope with one channel set to Invert mode and Add mode of

both channels. Use G (OV) test point for the oscilloscope ground.
TP7 and TP8 are sued for checking various characteristics of the
read/write head and also for the check and adjustment of the head seek
mechanism such as track alignment.

TP7,TP8
(Pre-amp.)

6V,approx.
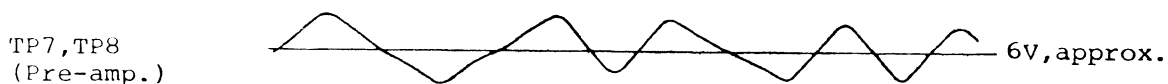
(Fig.317) Typical waveform of TP7 and TP8

TP9, TP10 (Differentiation amplifier) -- PCBA read write amp.

Test points to observe the differentiation amplifier output signals.
Like the pre-amplifier, the differentiation amplifier also has two
outputs of the order of several hundred mVp-p to several to several
V_p-p which differ in phase by 180°. Both outputs are observed at TP9
and TP10 respectively.
For an accurate observation of the waveforms, use two channels of
the oscilloscope with one channel set to Invert mode and Add mode
of both channels.
Use G (OV) test point for the oscilloscope ground.
TP9 and TP10 are used for checking the total operation of the read/write
head and the read amplifier and for the check and adjustment of the head
seek mechanism such as track alignment.

TP9,TP10
(Differentiation
amp.)

6V,approx.
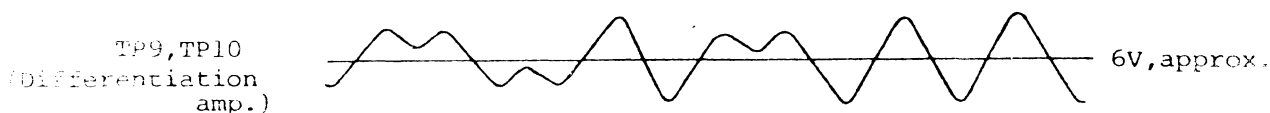
(Fig.318) Typical waveform of TP9 and TP10

TP11 (Write termination) -- PCBA read write amp.

Test point to observe the write waveform of the read/write head coil
during write operation.
This test point is equipped only for the versions which have the variable
resistor, R5 for write termination adjustment is mounted on the PCBA
read write amp. TP11 is not equipped for any units without R5.
During write operation, adjust the variable resistor, R5 by observing
the waveform at TP11 so that the waveform shows the critical damp
condition as in Fig.319.
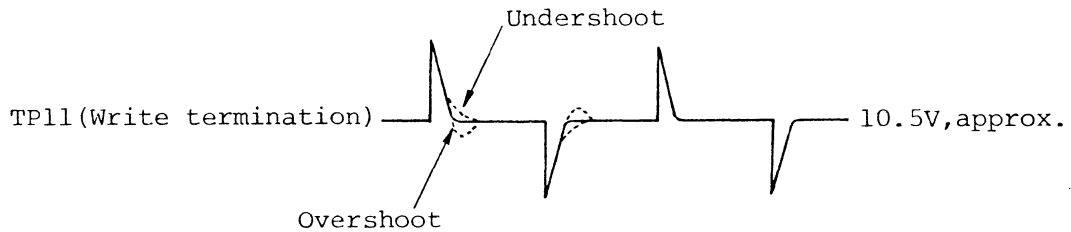
(Fig.319) Typical waveform of TP11

TP G (0V) -- PCBA MFD control, PCBA read write amp.

TP G is equipped respectively for the PCBA MFD control and PCBA read
write amp. They are used as the ground terminals for measurement
equipment. Be sure to use a small size clip to obtain a probe ground
of the equipment.

Function of Variable Resistors

On the PCBA read write amplifier, PCBA MFD control, and PCBA DD motor servo, maximum five variable resistors are mounted.
The variable resistors are correctly adjusted before the shipment of the FDD and fundamentally they shall not be readjusted except for by a trained technicians.

(1) Rl on PCBA DD motor servo (Disk rotational speed adjustment)

Variable resistor for adjusting the rotational speed of the disk.
It is adjusted so that the index pulse interval at TP4 or at the INDEX output signal is 200msec±3msec for FD-55A $\sim$ F (see Fig.313).

(2) Rl on PCBA MFD control (Erase off delay adjustment)

Variable resistor for adjusting the off delay of the erase gate.
It is adjusted so that the off delay in Fig.311 takes the value in Table 301 by observing the WRITE GATE input signal and TP2.

(3) R4 on PCBA read write amp. (Read data asymmetry adjustment)

Variable resistor for adjusting the asymmetry of the read data pulse.
Some versions have this variable resistor and others have fixed resistor
instead of it.

For a version with the variable resistor, R4, write 1F data and observe
the pulse intervals at TP5 or at the READ DATA output signal during
read operation. Then adjust the variable resistor so that the read
data asymmetry in Fig.320 takes the minimum value. For a double sided
FDD, repeat this operation alternately for side 0 and side 1 heads to
obtain the minimum asymmetry for both sides.
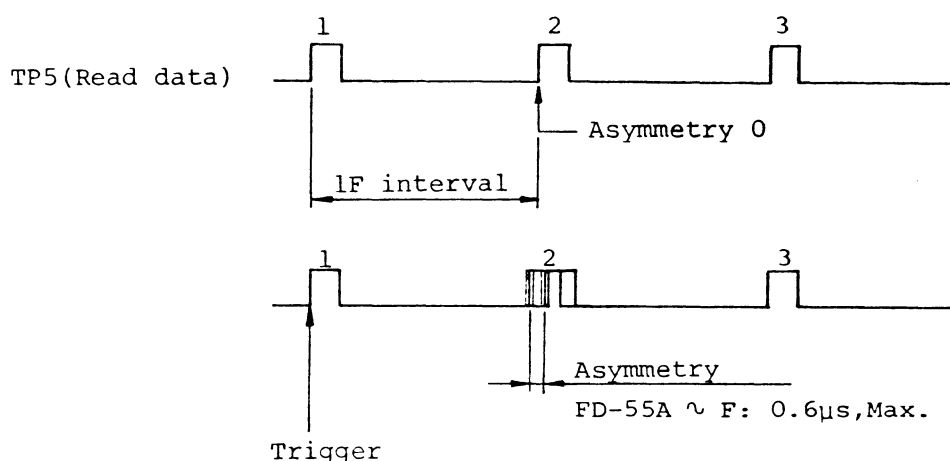
(Fig.320) Read data asymmetry

(4) R5 on PCBA read write amp. (Write termination adjustment)

Variable resistor for adjusting the terminator resistor of the read
write head during write operation.
Some versions have this variable resistor and others have fixed resistor
instead.

For a version with the variable resistor, R5 , observe the waveform at
TP11 (on the read write amp., see Fig.309) during 1F write operation.
Then set the variable resistor so that the TP11 waveform shows the
critical damp condition (sligntly overshooting is allowed) as in Fig.319.
For a double sided FDD, repeat this operation alternately for side 0
and side 1 heads to obtain the critical damp condition without
undershooting for both sides.

CHECK AND ADJUSTMENT

Adjustment of Set Arm Position

(A) Equipment

(1) Cross point screwdriver, M3
(2) Locking paint

(B) Adjustment procedure

(1) Loosen two fixing screws of the set arm (see Fig.413) so that the set
arm can be moved manually without getting out of place.

(2) Close the set arm by turning the front lever.

(3) In this condition (item (2)), adjust the set arm so that the visual
distance of the gap between the collet shaft and the set arm hole
becomes even.

(4) Tighten the installing screws of the set arm with the specified torque,
apply a drop of locking paint on the screw head.

(5) Open and close the set arm by turning the front lever and confirm that
it does so smoothly.

Orientation of the FDD

Position the FDD as shown in Fig.411 unless otherwise specified.
Horizontal and vertical orientations with lever side up should be used.

Horizontal setting   Vertical setting
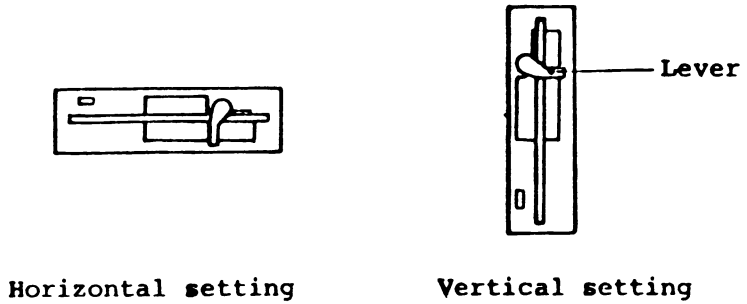
(Fig.411) General orientation of the FDD during maintenance
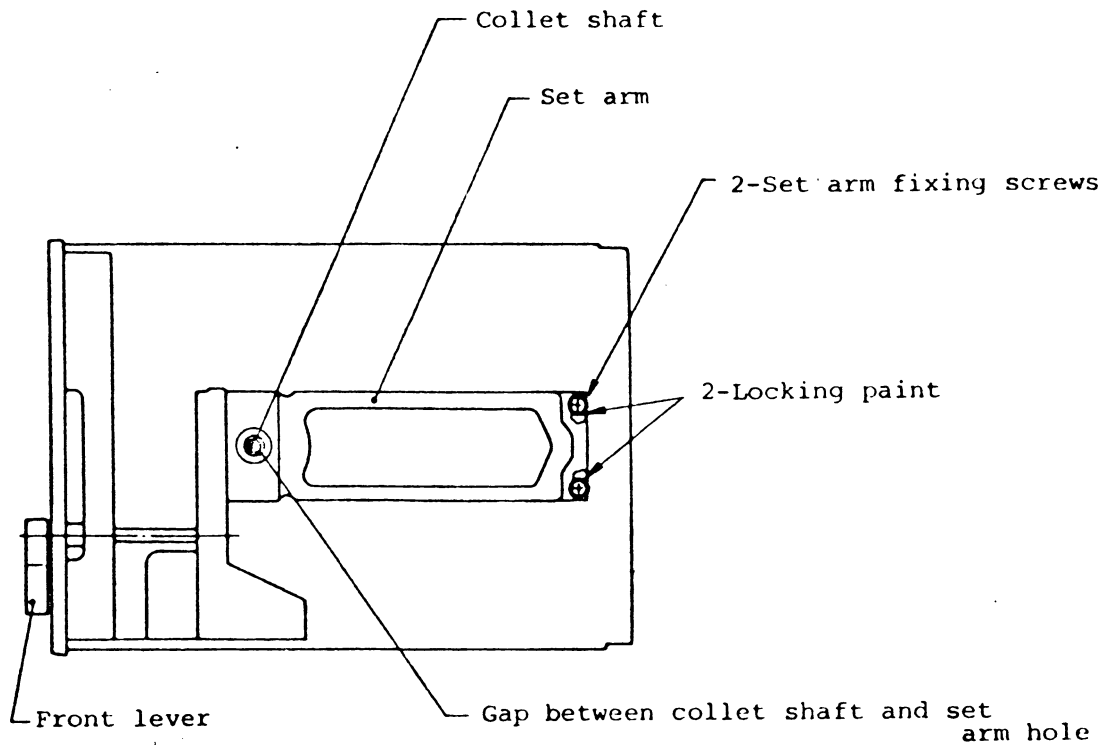
(Fig.413) Adjustment of set arm position

Adjustment of Clamp Arm Position

(A) Equipment

   (1) Cross point screwdriver, M3

   (2) SKA or user's system

   (3) Work disk

(B) Adjustment procedure

   (1) Loosen four holder fixing screws (see Fig.414) so that the holder can be moved manually without getting out of place.

   (2) Close the set arm by turning the front lever.

   (3) Push down the holder against the frame so that narrow gap is spaced between the E-ring on the collet shaft and the set arm plate, then tighten the four screws at both sides.
Narrow gap should be confirmed by a very easy manual turning of the E-ring.

   (4) Install a work disk.

   (5) Start the spindle motor and confirm that the disk rotates smoothly.

   (6) Place the FDD vertically (refer to Fig.411).

   (7) Nip the disk edge firmly with fingers which appears a little from the front bezel, and confirm that the rotor of the spindle motor stops.

   (8) If the spindle motor does not stop completely, push down the holder

further against the frame at item (3). Then execute the procedure
from item (4) through (7) again.

(9) Eject the work disk.

(10) Adjust the front lever position according to page-2116

E-ring

Clamp arm

Holder

Set arm plate

Holder fixing screws
(two for each side)
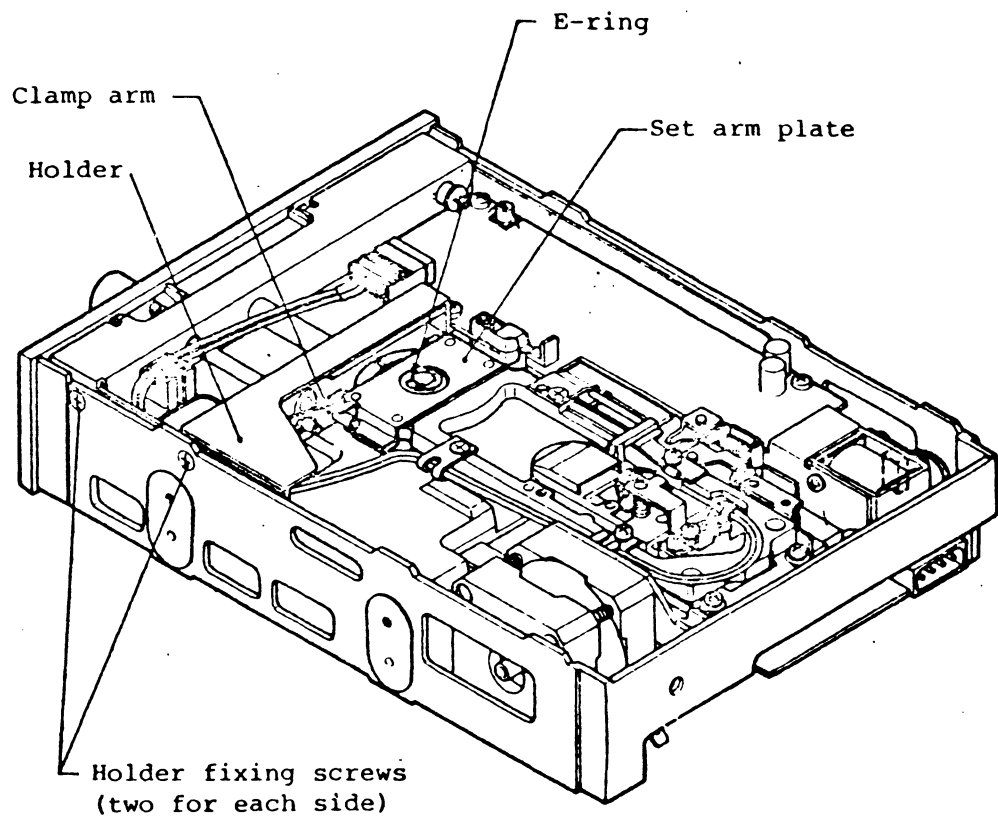
(Fig.414) Adjustment of clamp arm position

Adjustment of Front Lever Position

(A) Equipment

(1) Hexagon wrench key, 1.5mm
(2) MAX media jig

(B) Adjustment procedure

(1) Turn the front lever to open position and loosen a lever fixing set screw (see Fig.415).

(2) Turn the front lever to close position and loosen another fixing screw. Then pull out the lever for 0.5mm, approx.

(3) Tighten the screw in item (2).

(4) Open the front lever and insert the MAX media jig from the notch side. (See Fig.415).

(5) Turn the front lever to close position and loosen the lever fixing screw again. Then push the lever against the MAX media jig.

(6) Position the handle of the front lever forms right angle against the longitudinal side of the front vessel. And tighten the set screw with the specified torque. (see Fig.416).

(7) Turn the front lever to open position and tighten another set screw in the same manner.

(8) Close the front lever and confirm that the blade of the lever does not nip the MAX media jig.

(9) Open the front lever and remove the jig.

Front bezel

2-lever fixing screws

Front lever

MAX media jig
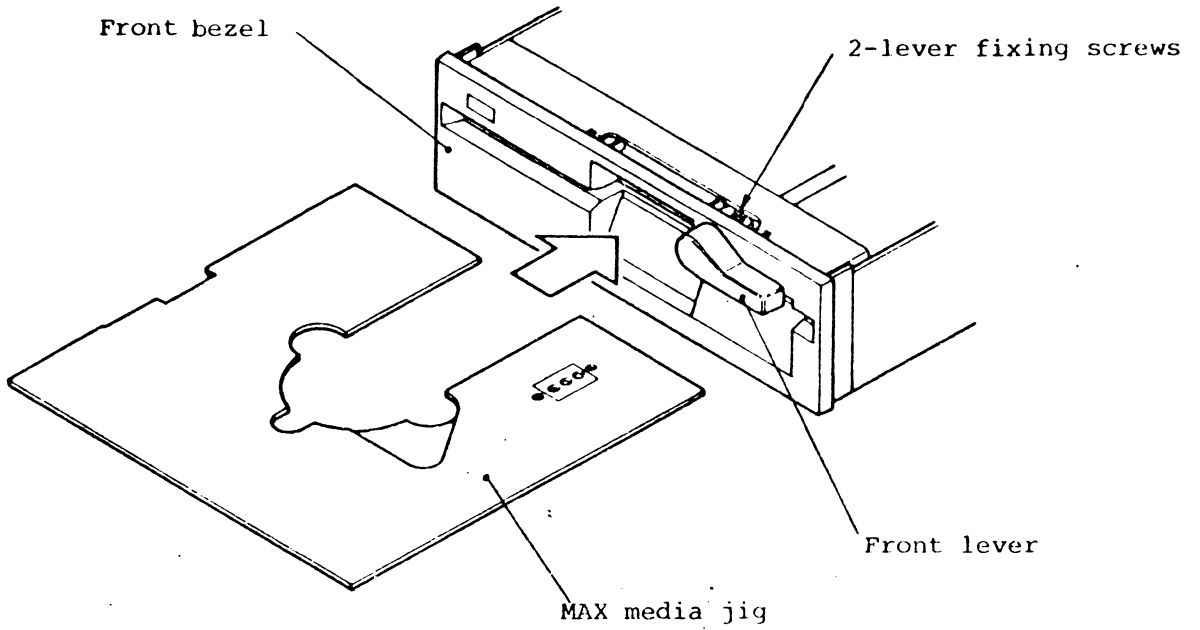
(Fig.415) Adjustment of front lever

Sectional view of front bezel

Front bezel

Front lever

MAX media jig

Form right angle

Blade
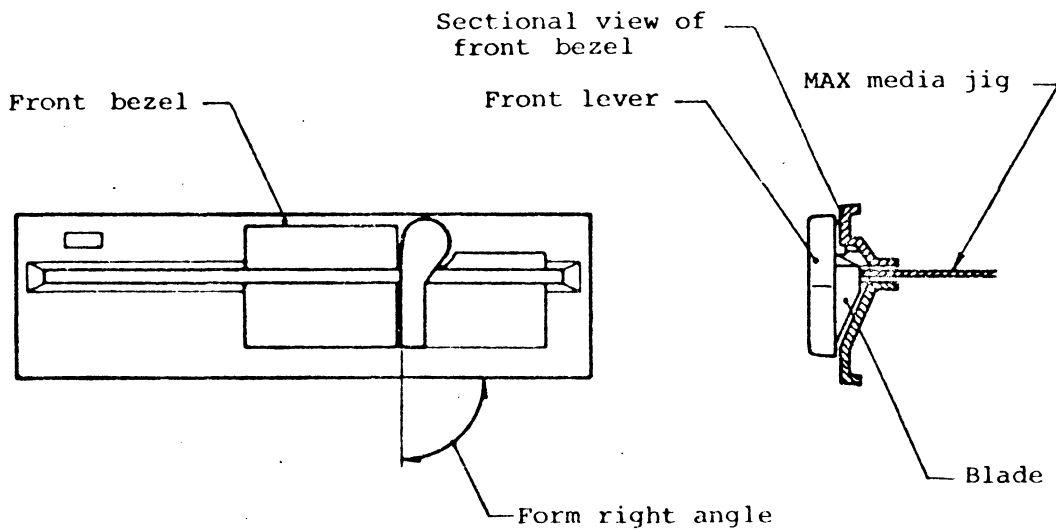
(Fig.416) Front lever position

Adjustment of Head Protector (Double sided only)

This item applies only to a double sided FDD.

(A) Equipment

(1) Hexagon wrench key, 1.5mm
(2) Work disk
(3) Locking paint

(B) Adjustment procedure

(1) Open the set arm by turning the front lever.

(2) Turn the adjusting screw (set screw) attached to the head protector
    and adjust the lifting height of the disk.
    Adjust the screw so that the head protector lifts the disk 1.0 through
    1.5mm high from the platform surface. (See Figs. 417 and 418).

(3) Insert the disk slowly and confirm that the disk jacket does not touch
    the side 0 nor side 1 head and goes into the pocket smoothly with
    appropriate space margin.

(4) After closing and opening the front lever, pull out the disk slowly.
    In the process of pulling out, side 0 and side 1 heads shall not touch
    the head window edge of the disk jacket (opening area of the jacket to
    make the head in contact with the disk surface). The jacket must be
    pulled out smoothly with appropriate space margin.

Note : 1. If the adjustment above is not done correctly, head will catch
          the disk jacket at the insertion or ejection of the disk, which
          will damage the head.

Platform

Arm lifter adjustment
screw

Head load solenoid
Ass'y

Head carriage Ass'y

Head protector adjustment screw
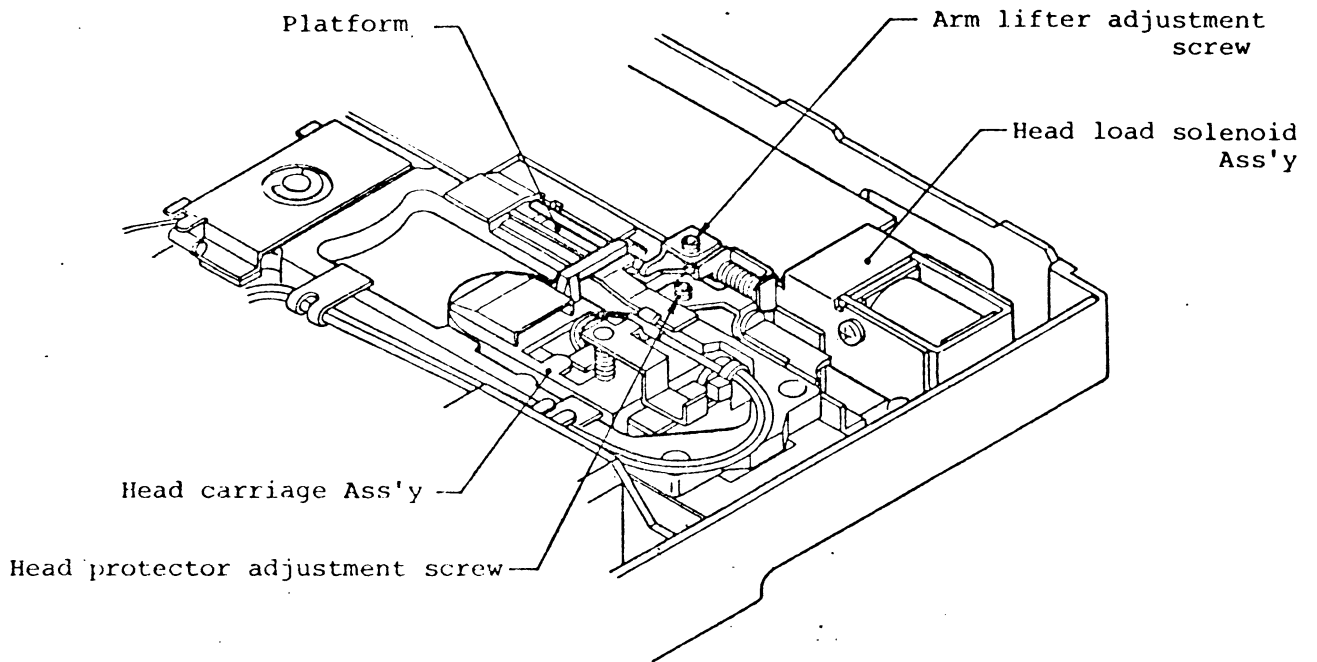
(Fig.417) Adjustment of head protector

Head protector

Platform

Disk lifting surface

Side 0 head

Head carriage Ass'y

1.0∿1.5mm
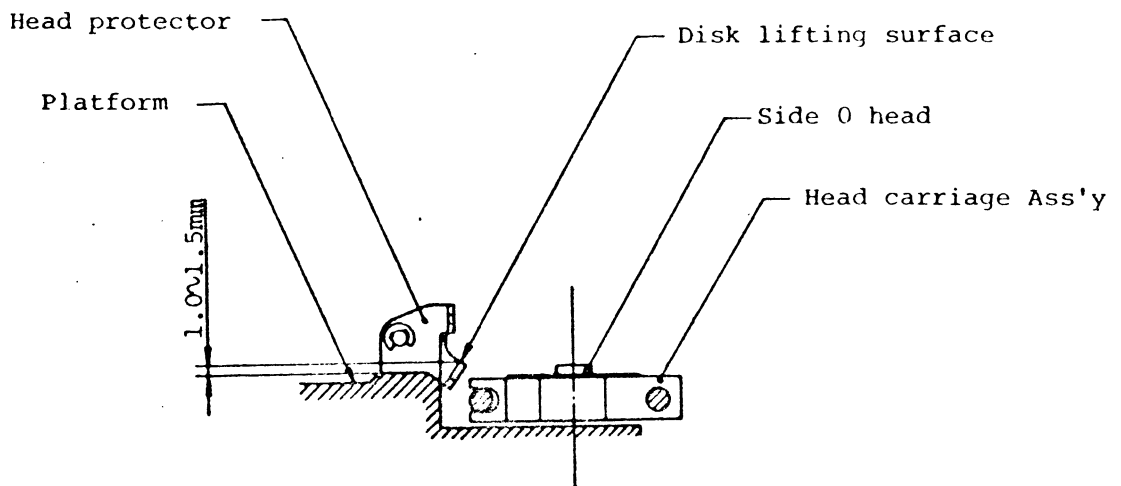
Note: Viewed from front vessel side

(Fig.418) Height of head protector

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Adjustment of Arm Lifter

(A) Equipment

(1) Hexagon wrench key, 1.5mm

(2) SKA or user's system

(3) Work disk

(4) Locking paint

(B) Adjustment procedure

(1) General method

(a) Start the spindle motor and insert a work disk.

(b) Set the head to track 00.

(c) Execute head loading.

(d) Turn the adjusting screw (set screw) of the arm lifter so that the gap between the upper arm (double sided) or the pad arm (single sided) and the arm lifter becomes 0.2mm, Min. (See Figs. 419 and 420).

(e) Unload the head.

(f) Confirm that the upper arm (double sided) or the pad arm (single sided) is lifted slightly by the arm lifter.

(g) Make the head move to the innermost track.

(h) Load the head and repeat the procedure from item (d) to (f).

(i) Again set the head to track 00.

(j) Repeat the procedure from item (c) to (f).

Arm lifter

Arm lifting part

Arm lifter adjusting
screw

Head carriage Ass'y

Head protector adjusting
screw

Head load
solenoid Ass'y

(Fig.419) Adjustment of arm lifter

Arm lifting part

0.2mm, Min.

Upper arm(double sided)
or Pad arm (single sided)

Head carriage Ass'y
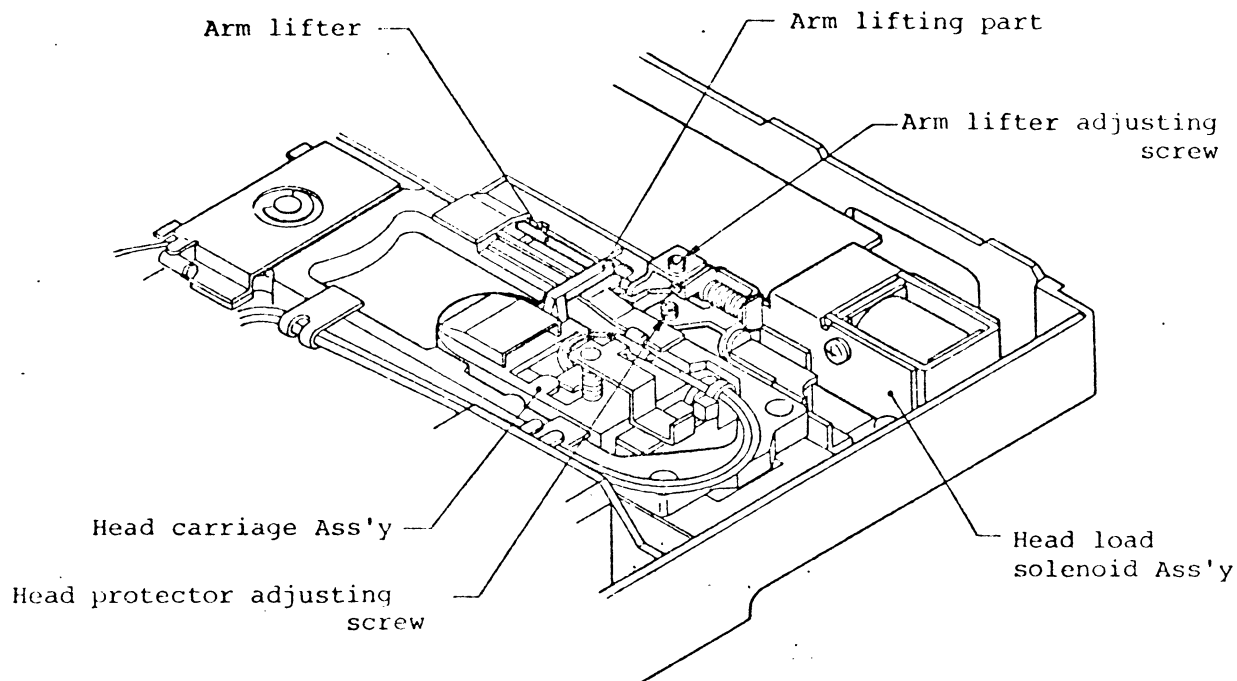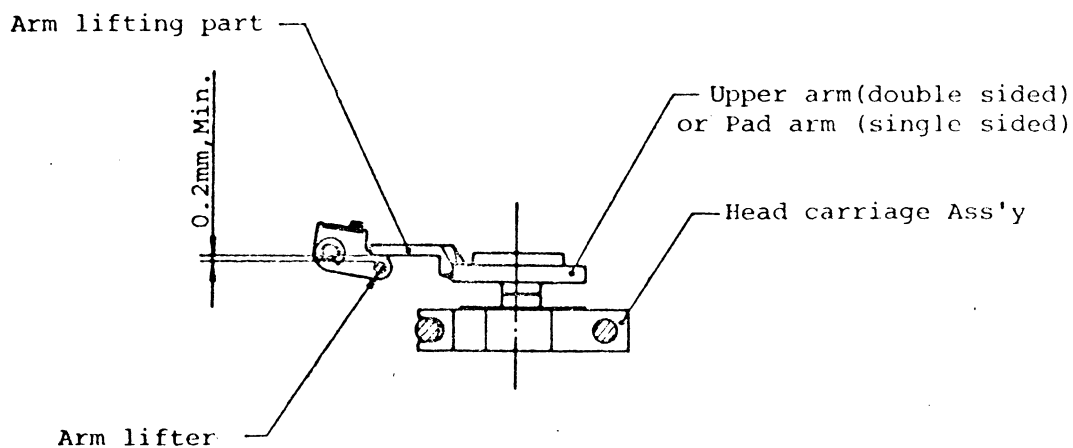
Arm lifter

Note: Viewed from front vessel side

(Fig.420) Gap of arm lifter

Check and Adjustment of File Protect Sensor

(A) Equipment

(1) MAX media jig
(2) Digital voltmeter (or oscilloscope)
(3) SKA or user's system

(B) Check procedure

(1) General method

(a) Place the FDD on the work bench with the LED indicator up and the front lever down. (See Fig.421).

(b) Connect a digital voltmeter or an oscilloscope (DC range,1V/div) to TP6 (File protect sensor) on the PCBA MFD control.

(c) Install the MAX media jig from the notch side and set it so that the notch A area is located on the light pass from the file protect sensor LED. (See Fig.421).

(d) Adjust the orientation of the FDD so that it is not exposed with strong light outside.

(e) Confirm that the voltage measured at TP6 when power is supplied to the FDD is within the following range.
Notch A position TP6 voltage: 3.0V, Min.

(f) Pull out the jig a little so that the notch B area is located on the light pass.

(g) Confirm that the voltage measured at TP6 when power is supplied to the FDD is within the following range.

Notch B position TP6 voltage: 0.5V, Min.

LED indicator

MAX media jig

Notch A

Notch B

File protect
sensor

Front lever
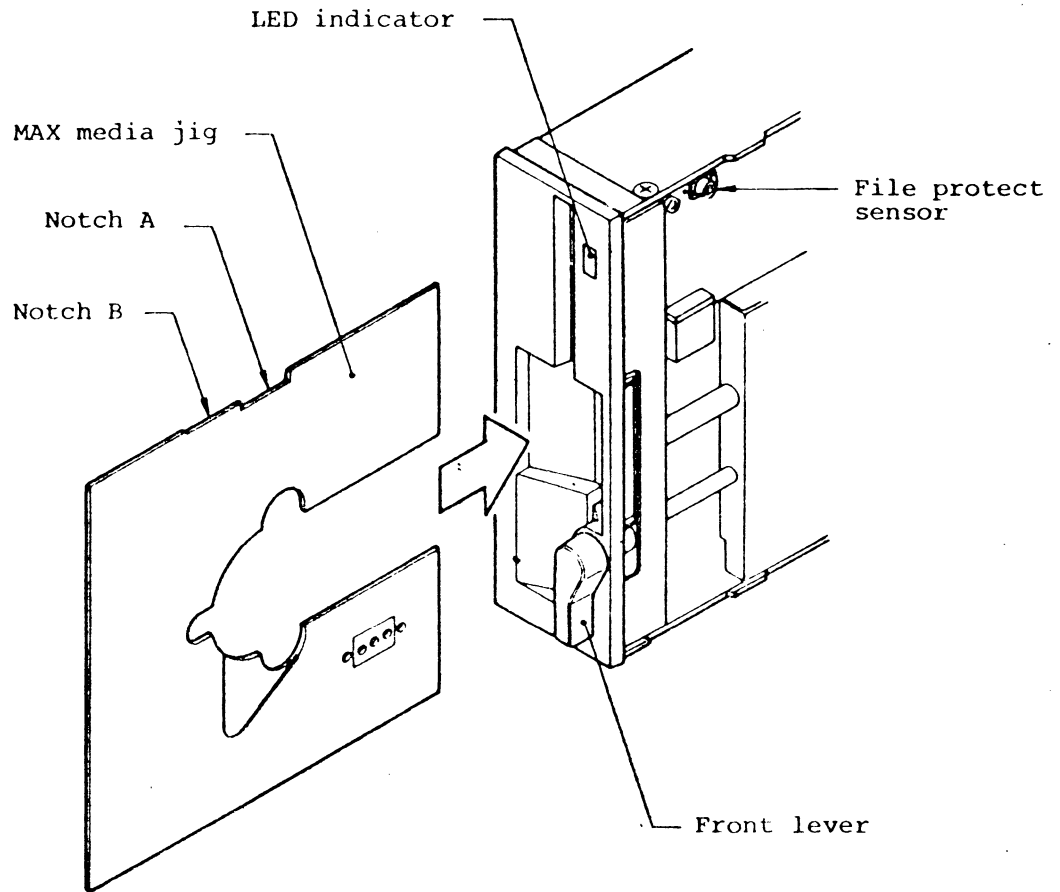
(Fig.421) Check of file protect sensor

Check and Adjustment of Disk Rotation Speed

(A) Equipment

  (1) Common screwdriver, small size

  (2) SKA or user's system

  (3) Frequency counter (not required when the SKA is used)

  (4) Work disk (soft sectored)

(B) Check and adjustment procedure

  (1) General method

    (a) Connect the frequency counter to TP4 (Index) of the PCBA MFD control or to the INDEX interface signal line.

    (b) Start the spindle motor and install a work disk.

    (c) Set the head to track 00.

    (d) Execute the head loading.

    (e) Confirm that the pulse interval at TP4 is within the following range.
       FD-55A ∿ F: 200±3msec

    (f) If the value in item (e) is out of the specified range, adjust the variable resistor R1 on the PCBA DD motor servo to obtain the median value in the specified range in item (e).

Check and Adjustment of Erase Gate Delay

(A) Equipment

(1) Common screwdriver, small size

(2) Work disk

(3) SKA or user's system

(4) Oscilloscope (not required when the SKA is used)

(B) Check and Adjustment procedure

(1) General method

(a) Use two channels of oscilloscope. Connect the trigger channel to WRITE GATE interface line and the other channel to TP2 (Erase gate delay) on the PCBA MFD control.
Oscilloscope range: For both channels, DC mode, 5V, 100μsec

(b) Start the spindle motor and install a work disk.

(c) Execute head loading.

(d) Set the oscilloscope to the negative trigger (-) mode. Make the WRITE GATE signal TRUE (write command).

(e) Confirm that "t" (Erase on delay) in Fig.423 is within the following range.
t(Erase on delay): 200 ∿ 320μsec (FD-55A ∿ F)

(f) Set the oscilloscope to the positive trigger (+) mode. Make the WRITE GATE signal FALSE.

```
WRITE GATE          ⌐─────────────────────────────

TP2              ·      ┌──────────────────────
(Erase gate delay)──────┘
                        ·
                   ├──t──┤── Erase on delay
```
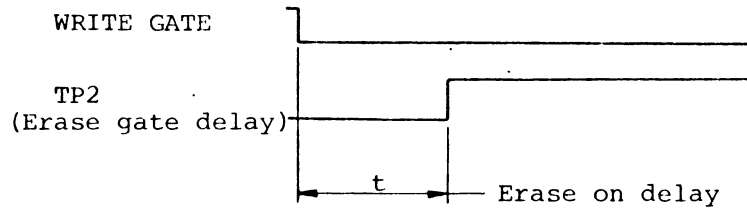
(Fig.423) Erase on delay

(g) Confirm that "t" (Erase off delay) in Fig.424 is within the following
    range.
    t(Erase off delay): 890+60-30μsec (FD-55A ∿ F)


```
WRITE GATE          ┌───────────────────────────

TP2(Erase gate delay)──────────────────────┐   ┌──────
                                            └───┘
                    ├──────────t──────────┤
                    Erase off delay
```
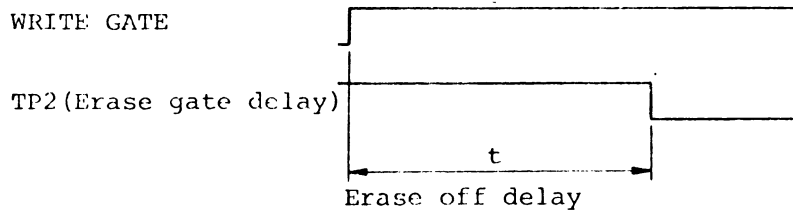
(Fig.424) Erase off delay

(h) If the value in item (g) is out of the specified range, adjust the
    variable resister Rl on the PCBA MFD control to obtain the median
    value in the specified range in item (g).

Check and Adjustment of Head Touch

Note: The adjustment applies to a single sided FDD only.

(A) Equipment

(1) Work disk

(2) Common screwdriver, small size

(3) SKA or user's system

(4) Oscilloscope (not required when the SKA is used)

(5) DC clip on ammeter (not required when the SKA is used)

(6) Locking paint

(B) Adjustment procedure

(1) General method

  (a) Connect an oscilloscope to TP9 or TP10 (Differentiation amp.) on the
      PCBA read write amplifier.
      Oscilloscope
            96tpi,100tpi: AC mode, 0.1V

  (b) Start the spindle motor and install a work disk.

  (c) Set the head to the innermost track.

  (d) Execute head loading.

  (e) Repeat the cycle of one rotation of write and one rotation of read.
      Write data should be a fixed pattern of 2F (250KHz of WRITE DATA
      frequency for FD-55A ∿ F).

  (f) Write down the average read level measured during the read operation
      of item (e).

- 2127 -

(g) Execute item (e) and (f) with a slight depression (very slight depression easy to release: 10 ∿ 20g) by a finger on the top of the upper head (double sided) and measure the average read level as in item (f).

(h) Confirm that the read level measured in item (f) is greater than 80% of that in item (g).

(i) For a double sided FDD, execute items (e) through (h) respectively for side 0 and side 1 heads.

(j) After making the head move to track 00, execute items (e) through (i).

(L) Possible causes for the insufficient head touch in a double sided FDD:

Following causes are assumed for the insufficient result in items (h) through (j) on a double sided FDD.

i) Inferior disk:
Disk and/or jacket is deformed or damaged. Replace the work disk with a new one.

ii) Inferior head flexture:
Because of the failed adjustment of the head protector the flexture on which the head piece is located may be deformed.
Remove the disk. Then open and close the front lever slowly to observe the gap between the side 1 and side 0 heads from the front bezel. If the two head surfaces are not in parallel each other, it is considered to be the deformation.
Replace the head carriage Ass'y

iii) Inferior pressure of the jacket pads:
    Refer to item   ① ～ ③ and "Caution".

① Inferior head pad:
  Replace the pad

② Inferior disk:
  Disk and /or jacket is deformed or damaged. Replace the work
  disk with a new one.

③ Inferior pressure of the jacket pads:
  Confirm that the jacket pad attached under the set arm
  does not touch the disk jacket surface. If item (h) is
  improved when the jacket surface is touched by a common
  screwdriver very lightly, execute the adjustment of the clamp arm
  position , or replace the pad 9B or attach another pad
  (the equivalent to the head pad).

Caution: If the jacket surface is excessively pressed, it might be
        deformed or the spindle motor might be overloaded because
        of increasing the rotation torque. If item ③ is done, measure
        the +12V current consumption of the FDD and confirm that the
        current does not exceed 350mA by an DC clip-on ammeter. For
        a commercially available general disks, the desirable current
        is 250mA, Max.

Check and Adjustment of Write Termination

(A) Equipment

(1) Work disk

(2) SKA or user's system

(3) Oscilloscope

(B) Check and adjustment procedure

(1) General method

   (a) Connect an oscilloscope to TP11 (Write termination, see Fig.309) on
       the PCBA read write amp.
       Oscilloscope range: AC mode, 0.5V, 0.5 ∿ 2μsec.

   (b) Start the spindle motor and install a work disk.

   (c) Execute head loading.

   (d) Execute 2F write operation (250KHz of WRITE DATA frequency for
       FD-55A ∿ F).

   (e) Confirm that the waveform at TP11 during the execution of item (d)
       shows the critical damp condition as in Fig.426. A little over-
       shooting is allowed.

   (f) For a double sided FDD, execute item (e) for side 1 head and side 0
       head respectively.

TP11(Write termination)

Undershoot
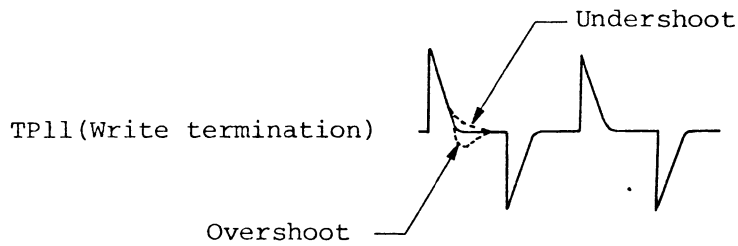
Overshoot

(Fig.426) Measurement of write termination

(g) If considerable undershoot or overshoot is observed in item (e) or
(f), readjustment shall be done according to the following procedure.

   i) Adjust the variable resistor, R5 on the PCBA read write amp., so
      that the waveform at TP11 during write operation shows the
      critical damp (a slight overshooting is allowable).

  ii) For a double sided FDD, repeat the adjusting operation in item
      i) alternately for side 0 and side 1 heads until both waveforms
      show critical damp without undershooting (a slight overshooting
      is allowed).

Check and Adjustment of Asymmetry

(A) Equipment

(1) Work disk

(2) SKA or user's system

(3) Oscilloscope

(B) Check and adjustment procedure

(1) General method

(a) Connect an oscilloscope to TP5 (Read data) on the PCBA MFD control
or to the READ DATA interface line.
Oscilloscope range   FD-55A ∿ F: DC mode, 2V,1μsec

(b) Start the spindle motor and install a work disk.

(c) Set the head to the innermost track.

(d) Execute head loading.

(e) Execute 1F write operation (125KHz of WRITE DATA frequency for
FD-55A ∿ F).

(f) Measure the asymmetry referring to Fig.427.

Note: Oscilloscope should be so set that three read data pulses can be
observed. Asymmetry width should be measured at the second read
data pulse from the trigger pulse.

(g) Confirm that the asymmetry is within the following range.
Innermost track 1F asymmetry FD-55A ∿ F: 0.6μsec, Max.

```
           1                2             3
TP5(Read data)  ⎍_____  ⎍⎍___⎍_____  ⎍____
                          ┊ ┊
READ DATA       ⎍_____  ⎍⎍___⎍_____  ⎍____
                          ┊ ┊
                │         ┊┊┊  Asymmetry
                │         ┊ ┊
                │─────────────┊  1F interval
                │
              Trigger
```
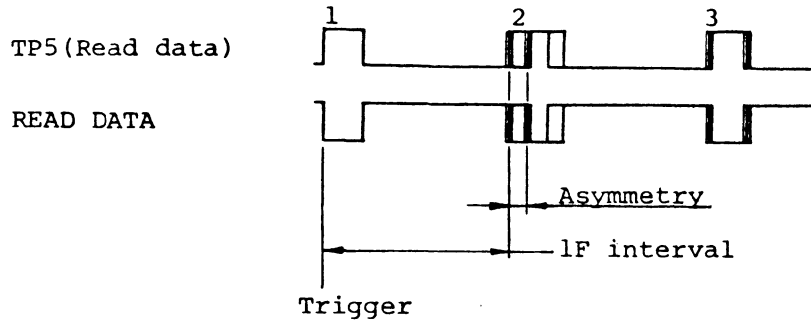
(Fig.427) Measurement of asymmetry

(h) For a double sided FDD, execute items (e) through (g) for side 0
    and side 1 heads respectively.

    If the value in item (g) or (h) is out of the specified range, adjust
    according to the following procedure.
    i) Adjust the variable resistor, R4 so that the asymmetry takes the
       minimum value while repeating 1F write and 1F read operations
       alternately.
    ii) For a double sided FDD, repeat the operation in item i) for
        side 0 and side 1 heads alternately. The variable resistor shall
        be so adjusted that both asymmetry for side 1 and side 0 heads
        take the minimum value.

(j) If the values in items (g) and (h) are out of the specified range
    in the PCBA versions without the variable resistor, R4, or if the
    adjustment in item (i) cannot be done sufficiently even if R4 is
    mounted, following causes are assumed.

    i) Leakage flux density in the environmental condition of the FDD

       is high:
       If there is some flux source near the FDD such as magnet,
       transformer, motor, Brown tube, magnetized iron plate, etc., take
       it apart from the FDD. Then measure the asymmetry and adjust again.
    ii) Inferior disk:
        Replace the work disk.
    iii) Inferior head:
         Replace the head carriage Ass'y
    iv) Inferior PCBA read write amp.:
        Replace the PCBA

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Check of Read Level

(A) Equipment

(1) Level disk

(2) SKA or user's system

(3) Oscilloscope (not required when the SKA is used)

(B) Check procedure

(1) General method

    (a) Use two channels of an oscilloscope and connect them to TP9 and TP10 (Differentiation amp.) on the PCBA read write amp.
Oscilloscope range   96tpi,100tip: AC mode, 0.2V
Set both channels, 1 and 2 to the above range. Set either of the channels to Invert mode and ADD both channels.

    (b) Start the spindle motor and install a level disk.

    (c) Make the head move to the innermost track.

    (d) Execute head loading.

    (e) Execute 2F write operation for one rotation of the disk (250KHz of WRITE DATA frequency for FD-55A ∿ F).

    (f) Measure the average amplitude (Vp-p) of the read waveform as in Fig.429.

    (g) Calculate the read level by substituting the following expression with the measured value in item (f) and READ LEVEL calibration value (see level disk label).

$$\text{Read level (true value)} = \text{Measured value} \times \frac{100}{\text{Calibration value}}$$

TP9,TP10(ADD)
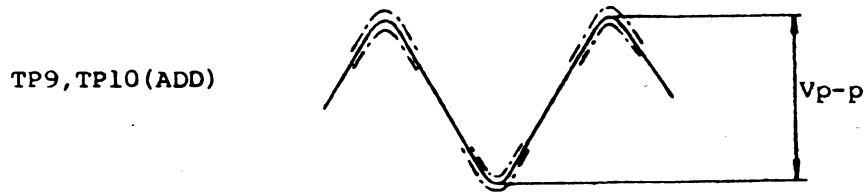
(Fig.429) Measurement of average read level (2F)

(h) Confirm that the true value of the read level is within the following range.

Innermost track read level   96tpi,100tpi: 0.6Vp-p, Min.

(i) For a double sided FDD, execute items (e) through (h) for side 0 and side 1 heads respectively.

(j) If the value in item (h) or (i) is out of the specified range, following causes are assumed.

    i) Inferior disk:

      Disk and/or jacket is deformed or damaged. Replace the level disk with a new one.

    ii) Abnormal disk rotational speed:

      Check and adjust

    iii) Inferior head touch:

      Check and adjust

    iv) Inferior head:

      Replace the head carriage Ass'y

    v) Inferior PCBA read write amp.:

      Replace the PCBA read write amp.

Check of Resolution

(A) Equipment

(1) Level disk

(2) SKA or user's system

(3) Oscilloscope (not required when the SKA is used)

(B) Check procedure

(1) General method

(a) Use two channels of an oscilloscope and connect them to TP7 and TP8 (Pre-amp.) on the PCBA read write amp.
Oscilloscope range   96tpi,100tpi: AC mode, 20mV ∿ 50mV

Set both channels, 1 and 2 to the above range. Set either of the channels to Invert mode and ADD both channels.

(b) Start the spindle motor and install a level disk.

(c) Make the head move to the innermost track.

(d) Execute head loading.

(e) Execute 1F write operation for one rotation of the disk (125KHz of WRITE DATA frequency for FD-55A ∿ F).

(f) Measure the average amplitude (V1F) as in Fig.430.

(g) Execute 2F write operation as in item (e) (double in frequency to that in item (e)).

(h) Measure the average amplitude (V2F) as in Fig.430.

- 2136 -
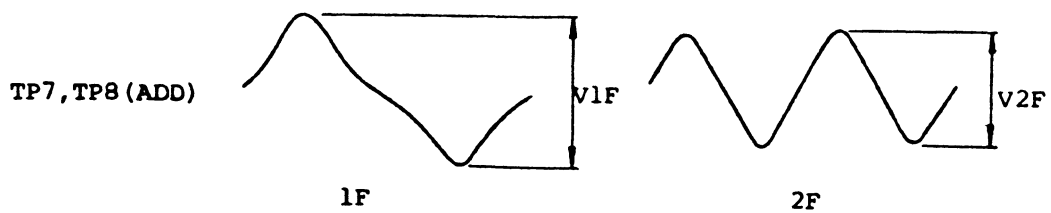
(Fig.430) Measurement of resolution

(i) Calculate the resolution by substituting the following expression with the measured values V1F, V2F, and RESOLUTION calibration value (see level disk label).

Resolution (true value) = V2F/V1F x 100/Calibration value (%)

(j) Confirm that the true value is within the following range.
Innermost track resolution: 55%, Min.

(k) For a double sided FDD, execute items (e) through (j) for side 0 and side 1 heads respectively.

(L) If the value in item (j) or (k) is out of the specified range, following causes are assumed.

   i) Inferior disk:
      Disk and/or jacket is deformed or damaged. Replace the level disk with a new one.
  ii) Inferior disk rotational speed;
      Check and adjust
 iii) Inferior head touch:
      Check and adjust
  iv) Inferior head: Replace the head carriage Ass'y

   v) Inferior PCBA read write amp.:
      Replace the PCBA read write amp.

Check and Adjustment of Track Alignment

(A) Equipment

(1) Cross point screwdriver, M3

(2) Alignment disk

(3) Alignment adjustment jig or M3 screw of 15mm long

(4) SKA or user's system

(5) Oscilloscope

(6) Hygrometer.

(7) Locking paint

(B) Check and adjustment procedure

Note: Check and adjustment of track alignment should be done in an
environment of general room temperature and humidity. Even if the
environmental condition is within the specified operational condition,
extreemly high or low temperature, or extreemly high or low humidity
should be avoided. Check and adjustment should be done after two
hours, Min. of storing in the above mentioned condition.
It is recommended that the orientation of the FDD for the track
alignment check is the same as when the FDD is actually installed
in the user's system.

(1) General method

(a) Use two channels of an oscilloscope and connect them to TP9 and TP10
(Differentiation amp.) on the PCBA read write amp. Also connect
the external trigger of the oscilloscope to TP4 (Index) and apply
positive trigger.
Oscilloscope range   96tpi, 100tpi: AC mode, 0.2V, 20msec

Set both channels, 1 and 2 to the above range. Set either of the
channels to Invert mode and Add both channels.

(b) Start the spindle motor and install an alignment disk.

(c) Execute head loading.

(d) Set the head to the following alignment check track.
    96tpi: track 32

(e) Confirm that two lobe patterns as in Fig.431 can be observed (it is
    not necessary that the levels of VA and VB are equal).
    If only one lobe pattern can be observed or if two lobes become one
    pattern, the head is not on the alignment check track.
    In such event, execute step-out or step-in as mentioned below to
    obtain the most similar waveform to that in Fig.431.
    96tpi, 100tpi: 4 tracks

    Note: The above number of tracks to be stepped is required to make the
          alignment track position be fit with the magnetized condition of
          the basic magnetized phase A of the stepping motor. If the stepped
          track numbers are inassured, set it again from track 00 (TRACK 00
          output signal becomes TRUE). For a 96tpi or 100tpi FDD, the lobe
          pattern should be observed at the track of multiple number of
          four (4).

(f) After one or several step-outs from the check track, step in the
    head to the check track again and measure VA and VB at that time.

(g) Calculate the true value of misalignment by substituting the value
    in item (f) and ALIGNMENT calibration value(see alignment disk label,
    attention to the side).
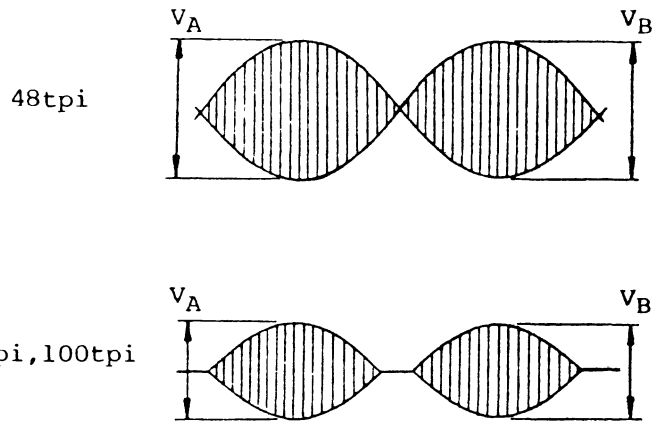
(Fig.431) Alignment check lobe pattern

$$\text{Misalignment (true value)} = \frac{\text{VA-VB}}{\text{Larger value in VA \& VB}} \times 100$$

$$-\text{(Calibration value)} - \text{(Relative humidity-50)} \times K$$

K is humidity compensation factor.

96tpi, 100tpi: K=0.42

e.g. VA=0.58V, VB=0.61V, Calibration value=-6(%),
     Relative humidity=65%, 96tpi:

$$\text{Misalignment (true value)} = \{\frac{0.58 - 0.61}{0.61} \times 100-(-6)\} - (65-50)$$

$$\times 0.42 \simeq -5.2 (\%)$$

If the calculated value is positive, the magnetic head is shifted
inward from the reference position, while the head is shifted outward
from the reference position when the value is negative.

(h) Conversely, measure VA and VB when the head is on the alignment check
track by stepping-out after one or several step-ins.

(i) Calculate the true value of misalignment as described in item (g).

(j) Confirm that both of the calculated values in items (g) and (i) are within the following range.
True value of misalignment: 30%, Max.

(k) For a double sided FDD, execute items (d) through (j) for side 0 and side 1 heads respectively.

(L) If the value in item (j) or (k) is out of the specified range, adjust the track alignment according to the following procedure:

  i) Loosen two fixing screws of the stepping motor a little.
  ii) Insert the alignment adjustment jig or M3 screw from the back side of the FDD as shown in Fig.432.
  iii) Repeat step-in and step-out operations and adjust the misalignment to be the smallest on the alignment check track during both step-in and step-out operations by turning the jig or the screw (stepping motor moves little by little).

Note: When you adjust the alignment by observing the lobe pattern using the oscilloscope, pay attention to the calibration value on the alignment disk label and the ambient relative humidity.

① Calibration value + (Relative humidity - 50) x K $\geq$ 0:
When the left side lobe pattern level, VA is assumed as "1", lobe pattern ratio should be so adjusted that the right side lobe pattern level VB takes the following value:

$$VB = 1 - \frac{\text{Calibration value + (Relative humidity - 50) x K}}{100}$$

② Calibration value + (Relative humdity - 50) x K $\leq$ 0:
When the right side lobe pattern level, VB is assumed as "1", lobe pattern ratio should be so adjusted that the left side lobe pattern level VA takes the following value.

$$VA = 1 - \frac{\text{Calibration value} + (\text{Relative humidity} -50) \times K}{100}$$

e.g. Calibration value = -6%, Relative humidity = 35%, 96tpi:

-6+(35-50)x0.42=-12.3 < 0

$$VA = 1 - \frac{-6+(35-50)\times0.42}{100} = 0.88$$

Therefore, the target value of VA when VB is assumed as "1" is 0.88.

iv) For a double sided FDD, repeat the adjusting operation in item iii) alternately for side 0 and side 1 heads until the both misalignment take the smallest value.

v) Tighten the two fixing screws of the stepping motor little by little for adjusting the true value of misalignment after tightening the screws with the specified torque to be within ±20%.

vi) Remove the alignment disk.

vii) Apply a drop of locking paint to the head of the stepping motor fixing screws.

viii) Check and adjust the track 00 sensor

ix) Check and adjust the track 00 stopper

(m) Release the Invert and Add modes of the oscilloscope.

Stepping motor

Alignment adjustment jig
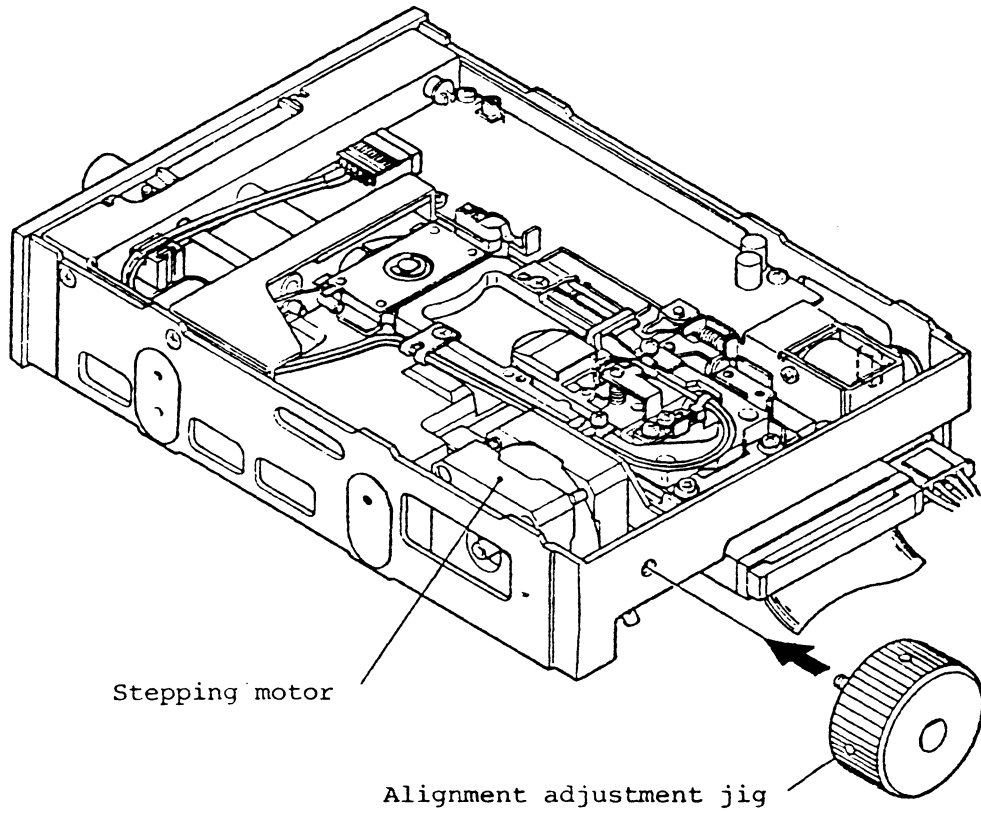
(Fig.432) Adjustment track alignment

Check and Adjustment of Track 00 Sensor

(A) Equipment

(1) Cross point screwdriver, M3

(2) Work disk

(3) Alignment disk

(4) SKA or user's system

(5) Oscilloscope (or digital volt meter)

(6) Locking paint

(B) Check and adjustment procedure

(1) General method

    (a) Connect a digital volt meter or an oscilloscope to TP1 (Track 00
        sensor) on the PCBA MFD control.
        Oscilloscope range: DC mode, 1V

    (b) Start the spindle motor and install a work disk.

    (c) Execute head loading.

    (d) Confirm that the voltage at TP1 is within the following range when
        the head is set to track 00.
        Track 00 position TP1 voltage: 3V, Min.

    (e) Turn the power off of the FDD and then turn it on again. Confirm
        that the position of head carriage did not change at power on or off.
        This item aims to confirm that the track 00 position matches the
        basic magnetized phase A of the stepping motor.

    (f) Make the head move to the following track.

96tpi, 100tpi: 04 track

(g) Confirm that the voltage at TP1 is within the following range at
the track position in item (f).
TP1 voltage at track, 04(96tpi,100tpi): 0.5V,Max.

Note: For some units of FDDs shipped at the initial stage of production,
TP1 is not directly connected to the output line of the track 00
sensor. The sensor output is supplied to TP1 through schmitt
inverter U208 (output pin 8). In these units, the voltage of TP1 is
TTL HIGH level (2.5V, Min.) at the track 00 position and TTL LOW
level (0.4V, Max.) at the track position in item (f).
Change the connection of the oscilloscope or the digital voltmeter
from TP1 to the pin 9 of IC, U208 on the PCBA MFD control and
execute items (d) through (g) again.

(h) If the value in item (d), (e), or (g) is out of the specified range,
adjust the position of the track 00 sensor according to the following
procedure.

   i) Loosen the fixing screw of the track 00 stopper and
      shift the stopper in the step-out direction (make apart from the
      rear side of the head carriage).
  ii) Connect the oscilloscope to TP9 or TP10 (Differentiation amp.)
      of the PCBA read write amp.
      Oscilloscope range: AC mode, 0.2V, 20msec
 iii) Install an alignment disk. The track alignment should be adjusted
      correctly
  iv) Make the head move to the position where the lobe pattern as in
      Fig.431 can be observed.
   v) Remove the alignment disk.
  vi) Connect the digital voltmeter or the oscilloscope to TP1 (Track 00
      sensor) on the PCBA MFD control. In the case mentioned in item (g),
      "Note", connect it to pin 9 of U208.
      Oscilloscope range: DC mode, 1V

vii) Step out the head for the following track space from the position
where the normal lobe pattern is observed.

96tpi: 30 tracks (head will be on track 02)

viii) Install a work disk.

ix) Loosen the fixing screws of the track 00 sensor (see Fig.433)
and move the sensor a little so that the voltage at TP1 falls
within the following range.

TP1 voltage at track 02 (96tpi,100tpi):

0.5 ~ 3V (0.8 ~ 1.2V, approx.center)

x) Confirm the items (d) through (g).

xi) Adjust the track 00 sensor position so that the values in items
(ix) and (x) satisfy the specification when the screw has been
tightened with the specified torque.

xii) Apply a drop of locking paint on the fixing screw head.

xiii) Adjust the track 00 stopper

Head carriage Ass'y

Track 00 sensor

Head load solenoid Ass'y
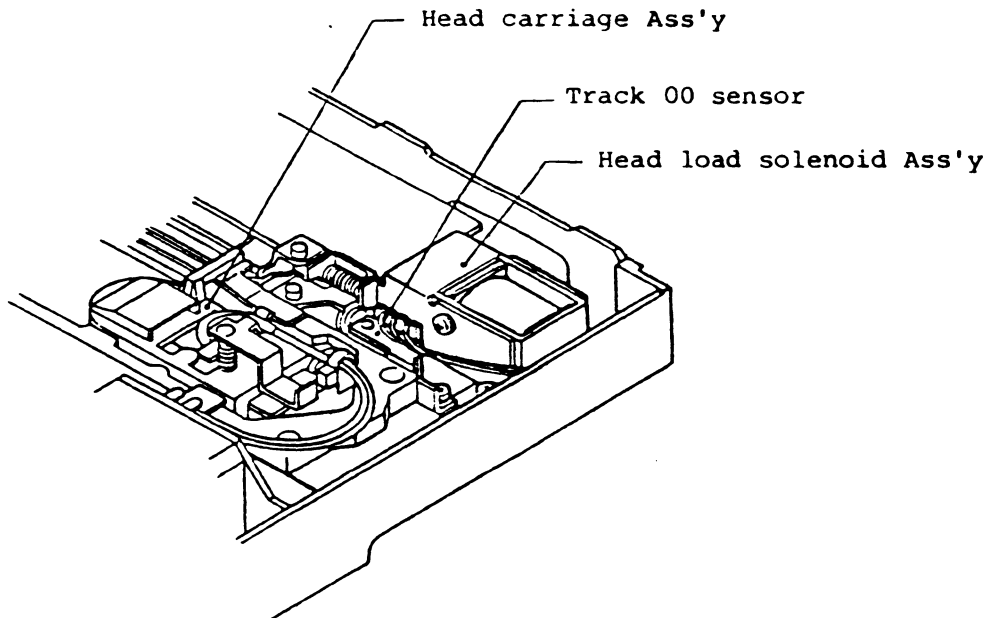
(Fig.433) Adjustment of track 00 sensor

Check and Adjustment of Index Burst Timing

(A) Equipment

 (1) Hexagon wrench key, 1.5mm

 (2) Alignment disk

 (3) SKA or user's system

 (4) Oscilloscope (not required when the SKA is used)

 (5) Locking paint

(B) Check and adjustment procedure

 (1) General method

  (a) Use two channels of the oscilloscope. Connect the 1st channel to TP4
      (Index) on the PCBA MFD control and the 2nd channel to TP7 or TP8
      (Pre-amp). Apply positive trigger by TP4.
      Oscilloscope range
            The 1st channel: DC mode, 2V, 50μsec

            The 2nd channel 96tpi,100tpi: AC mode, 0.5V, 50μsec

  (b) Start the spindle motor and install an alignment disk.

  (c) Execute head loading.

  (d) Set the head to the following track.
      96tpi: Track 02

  (e) Measure "t" in Fig.436

TP4 (Index)

TP7 or TP8

t | Index burst delay
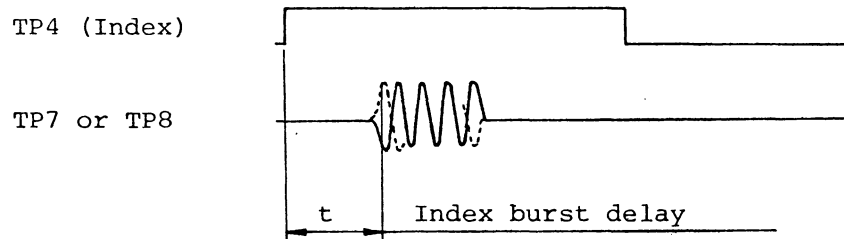
(Fig.436) Index burst timing

(f) Substitute the following equation with the measured value in item
(e) and INDEX TIMING calibration value (see alignment disk label).

Index burst timing (true value)=Measured value - Calibration value (μs)

(g) Confirm that the true value of the index burst timing is within the
following range.

FD-55A $\sim$ F: 200$\pm$200μsec

(h) If the value in item (g) is out of the specified range, adjust the
index sensor Ass'y position according to the following procedure.

i) Loosen the fixing screw (see Fig.437) of the index sensor on the
PCBA read write amp. and adjust its position to make the true value
of the index burst timing fall in the specified range in item (g).
ii) Repeat the adjustment so that the true value of the index burst
timing falls in the range of item (g) when the fixing screw has
been tightened with the specified torque.
iii) Apply a drop of locking paint on the fixing screw head.

(i) Remove the alignment disk.

Adjusting direction of
    sensor position

Index sensor fixing screw

Index sensor

PCBA read write amp.
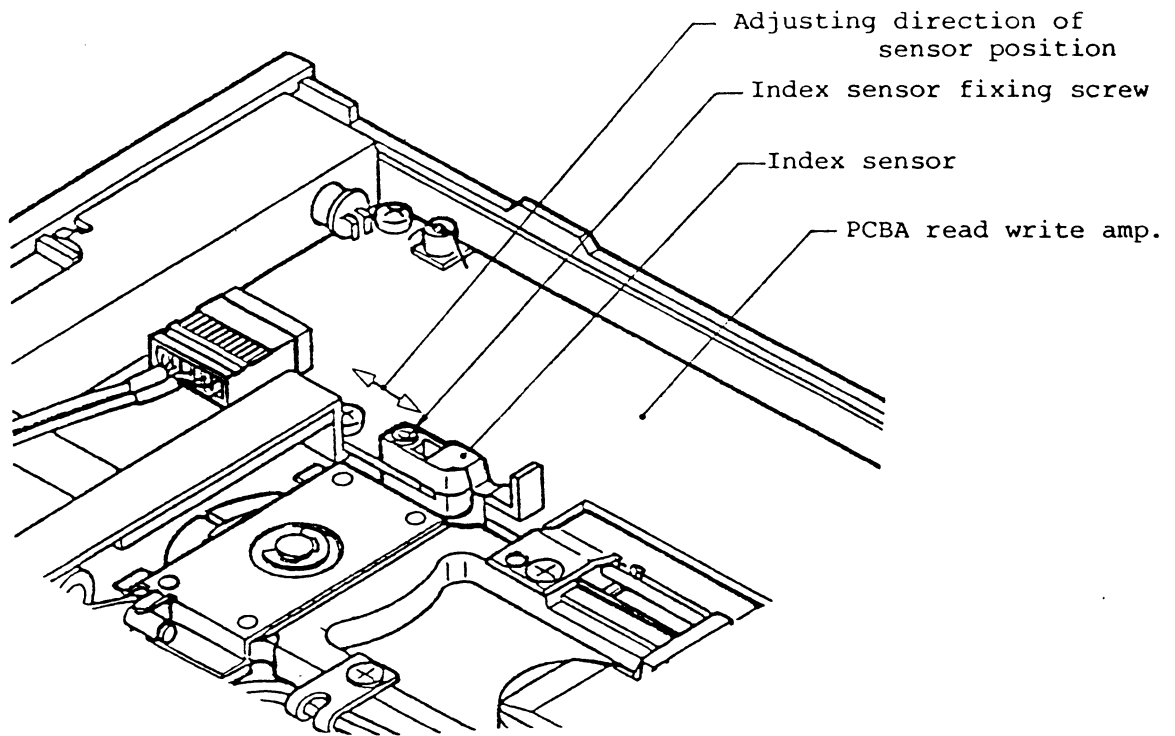
(Fig.437) Adjustment of index sensor

≡≡ People ≡≡

MONITOR

POWER	AC ●DC
VOLTAGE & FREQUENCY	12.0 V Hz
CURRENT	1.6 A (max) 1.3 A (ave)
CONSUMPTION	19.2 Watt
RUSH CURRENT	20 A mS
DISPLAY CHARACTER FORMAT	80 chrs X 25 rows
CHARACTER MATRIX	7 dots X 12 lines
CHARACTER BLOCK	8 dots X 19 lines
DISPLAY FORMAT	640 dots X 475 lines
DISPLAY SIZE	210 mm X 155 mm
CONNECTOR (SIGNAL,POWER)	DIN 8a TYPE
WEIGHT NET (GROSS)	Kg (Kg)
TEMPERATURE OPERATING	+4 °C +40 °C
NON-OPERATING	-25 °C +65 °C
HUMIDITY OPERATING	4 % 85 %
NON-OPERATING	15 % 95 %
VIBRATION OPERATING	G
NON-OPERATING	G
DROP (with Box)	80 cm
CONTROL OUTER FRONT	POWER SW , BRIGHTNESS , CONTRAST
OUTER BACK	H.HOLD , V.HOLD , V.LIN , V.HEIGHT
	SUB BRIGHTNESS
INTERNAL	SUB CONTRAST , FOCUS , H.WIDTH
SCAN LINEARITY Horizontal	< 10 %
Vertical	< 10 %
RASTER DISTORTION Horizontal	< 5 %
Vertical	< 5 %
AUDIO	●NONE , W (input mV)
LICENCE (SAFETY)	●NONE , UL , CSA , VDE ,
LICENCE (INTERFERENCE)	●NONE , FCC-class A , FCC-class B ,FTZ

1. VIDEO AMPLIFIER CIRCIUT

The VIDEO INPUT of 1.0Vp-p (75Ohm) is on Pin 7 from DIN8a CONNECTOR on PWD-265, then added to the base of TR201 of 1st VIDEO AMP. Subsequently, it is amplified to about 3.5Vp-p by TR201 and TR202. Between the output side of TR202 and the amplifier of the next stage, VR1 and VR202 is installed. The input to TR203 and TR204 of the next stage is increased or decreased by the changes in this division ratio, and the adjustment of the picture contrast is made. Each stage of the image portion is connected with capacitors, so the direct current portion will be reduced.

The horizontal synchronous pulses are on the base of TR208.
This period on the base of TR208 is equivalent to the height of the video signal. When TR208 is in operation the height of the video signals on the collector side is clamped by the electrical potential on the emitter side of TR208.

In this way, VIDEO signal of which the direct current portion has been regenerated by TR208 limits the luminosity by D201.
Next stage is sufficiently amplified by TR205, TR206, TR207.
These are cascade amplifiers, and it modulates the cathode of the CRT.

2. SYNCHRONOUS SIGNAL INVERTING BUFFER CIRCUIT

HORIZONTAL (Pin3) and VERTICAL (Pin5) SYNCHRONOUS of TTL level signal goes to the IC501 of open collector inverters. HORIZONTAL SYNCHRONOUS is feeded to base of TR501, and these are feeded to IC401, TR208, and AFC circuits.

3. VERTICAL DEFLECTION CIRCUIT
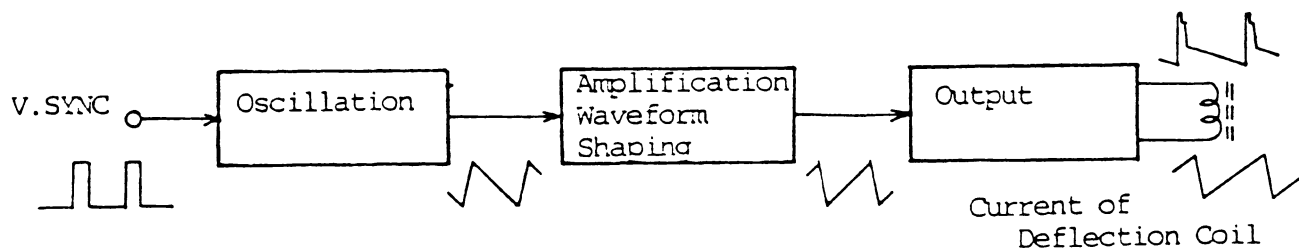
FIG. 3.1 Composition of Vertical Deflection Circuit

As shown in the block diagram, the base circuit of the vertical deflection circuit is composed of vertical oscillation circuit which generates saw tooth wave voltage, amplification waveform shaping, and output circuit.
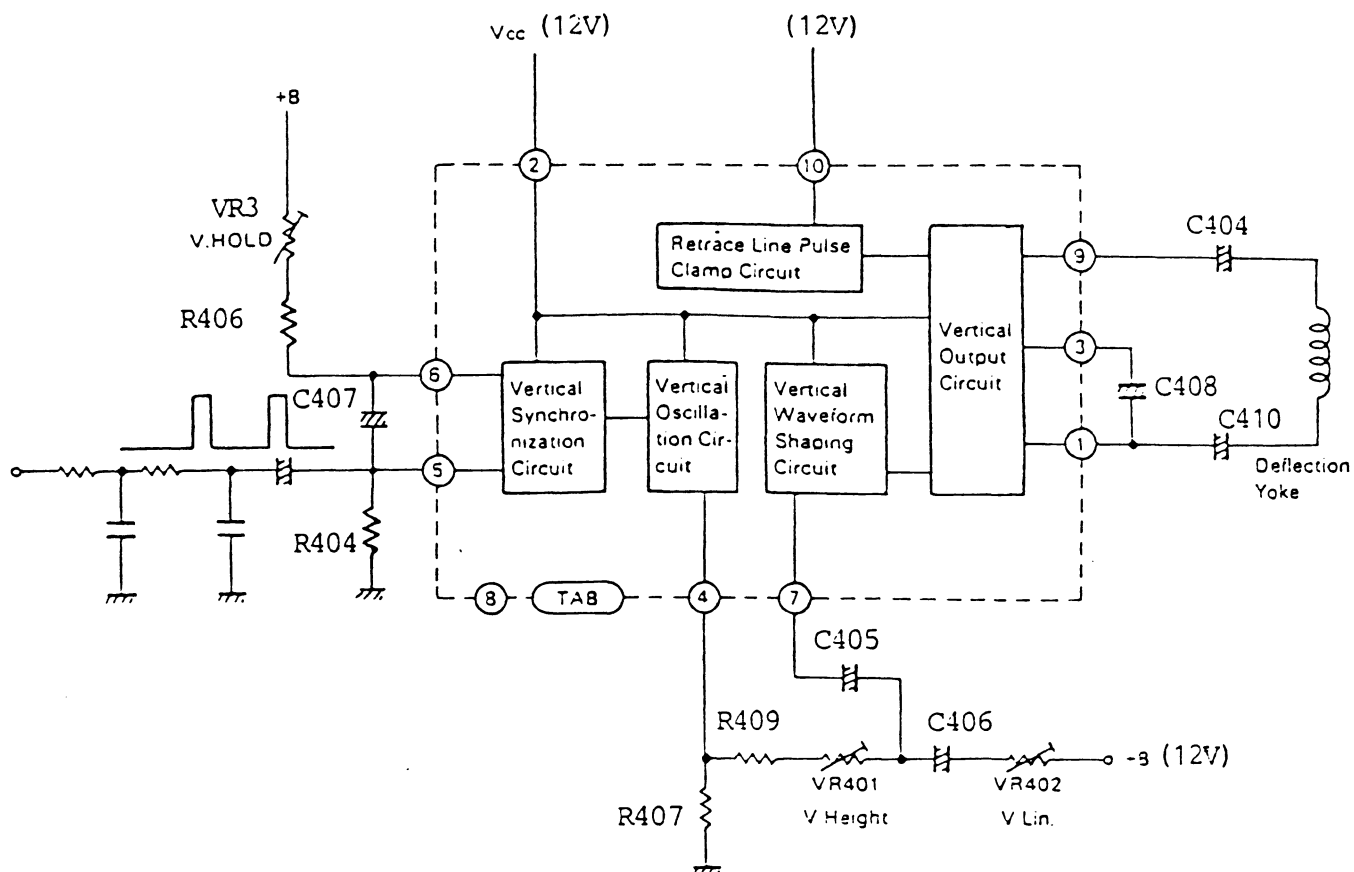
Fig. 3.2 VERTICAL SYNCHRONOUS CIRCUIT

The vertical synchronous signal is inverted by IC501 which has passed through the integration circuit is added to the vertical synchronous circuit by pin 5 of IC401.

The saw tooth wave of 45.5Hz which has been generated by the vertical oscillation circuit is taken from pin 4, and after passing through R409, VR401 and C405, it is added to pin 7 then after the waveform shaping, it is amplified, and added to the vertical output. R404, R406, VR3 and C407 are time constants which determine the oscillation. The vertical output waveform is a waveform in which pulse is superposed with sawtooth wave as it is clear from C410 for Deflection Yoke (DY) side.

This is designed so that high voltage is added to retrace line period, and low voltage is added to scanning period in order to decrease the power consumption of vertical deflection circuit by retrace line pulse clamp circuit.

In the above mentioned way, the circuit power consumption is reduced and the operation is done efficiently.

VR401 is for adjustment of V. Height and VR402 is for adjustment of V. Lin, and they are connected to pin 4 and pin 7, respectively. Vertical synchronization is done by VR3 connected to pin 6.

4. BLANKING CIRCUIT

During the retrace line period, if the CRT is operating, white
slantwise lines vertical retrace (flyback) lines will appear on the
tube and become obstacle to the picture, so they must be eliminated.
Such a phenomenon occurs when the black level adjusted to the cut-
off and below the picture tube moves, and the scanning lines in the
vertical retrace (flyback) line period appears in the picture.
In order to prevent this, is will be sufficient if the CRT does not
operate during the retrace (flyback) line period.
As an actual circuit operation, positive polarity pulse generated
during the retrace (flyback) period is added to the base of Blanking
Transistor TR209 from IC401 pin 1 and the collector of Horizontal
Output transistor TR504, and negative polarity pulse is taken out
to the collector of TR209, and this is added to the control grid
G1 of CRT via C213.
During the retrace (flyback) line period, the bias of CRT is made
deeper, and cut-off.
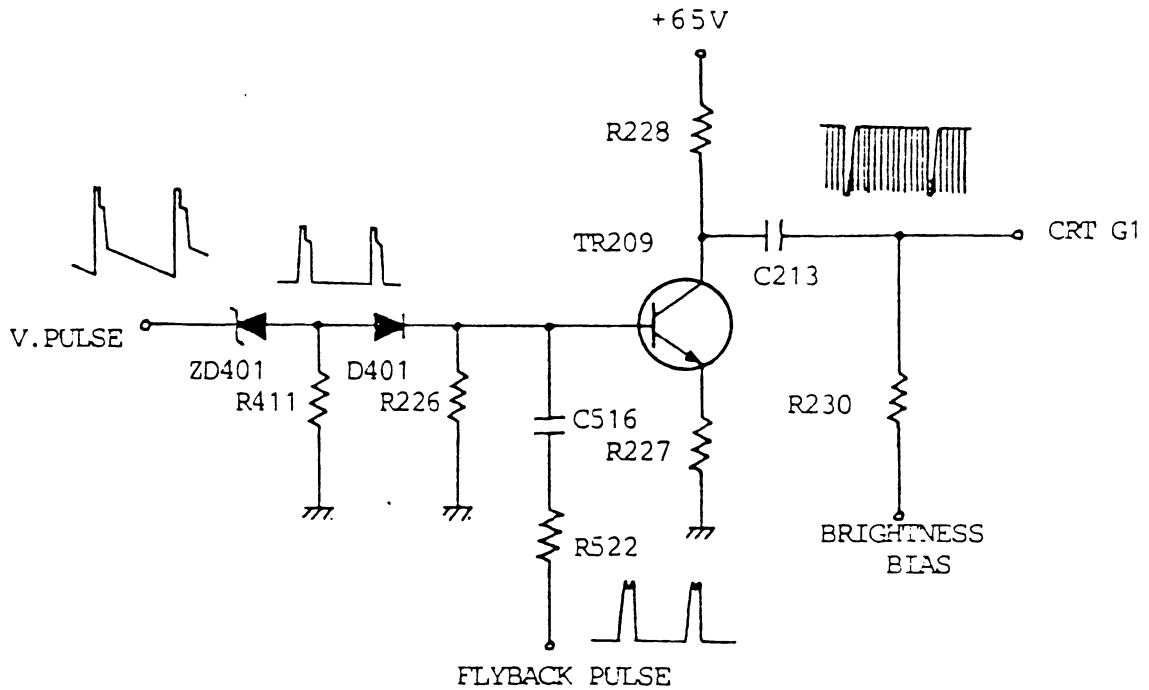
Fig. 4.1 BLANKING CIRCUIT

5. HORIZONTAL DEFLECTION CIRCUIT

As shown in Fig. 5.1, the horizontal deflection circuit is
composed of AFC circuit, Oscillation circuit, and Output circuit,
and its function is to pass sawtooth wave current synchronized
with the horizontal synchronization signal to the deflection coil.

H.SYNC. ──→ │ AFC │ ←─ │ H.OSC. │ →│ H.DRIVE │ →│ H.OUTPUT │ D.Y.

Sample Signal
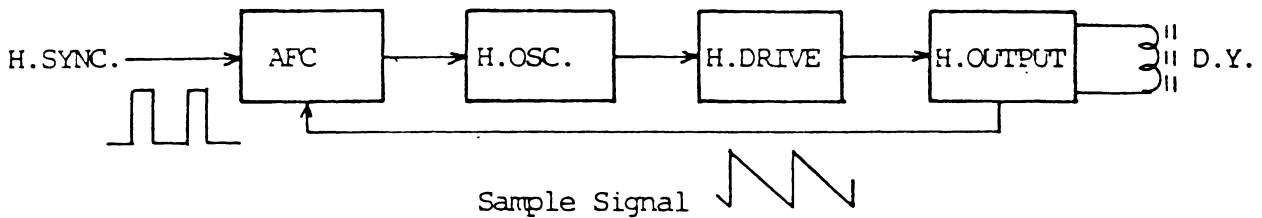
Fig. 5.1 Horizontal Deflection Circuit

Function of AFC Circuit

The AFC circuit will compare the phase of the oscillation circuit
and the phase of the synchronous signal, then generate direct
current output voltage proportionate to the phase difference.
This voltage is added to the oscillation circuit, and the
oscillation frequency and its phase will be coincided with the
horizontal synchronous signal.
The horizontal oscillation signal feed back to the AFC circuit
is normally done by changing the pulse generated in the horizontal
output circuit into sawtooth wave (This is called comparative
waveform signal).

6. HORIZONTAL OSCILLATION CIRCUIT

The horizontal oscillation circuit generates frequency of 23.58KHz.
The oscillation time constant is smaller than the time constant
of the vertical oscillation circuit at C505 and L1.
The Oscillation Transformer is designed so that positive feedback
and oscillation will be made at T501.
When the base voltage of the oscillation transistor becomes high,
the oscillation frequency also becomes high, when the base
voltage becomes low, then the oscillation frequency becomes low.
Therefore, the frequency control will function as follows.
If the oscillation frequency begins to get low (The phase is
delayed) the output of AFC increases. Since this voltage is added
to the base of the horizontal oscillation, it will function as
raising the oscillation frequency (The phase is advanced).
If the oscillation frequency begins to get high (the phase
advances), then the output of AFC will become low, and this will
be added to the oscillation circuit. Consequently, it will function
as lowering the oscillation frequency (The phase is delayed). In
the above mentioned way, the horizontal oscillation frequency
and its phase will always coincide with the horizontal synchronous
signal.
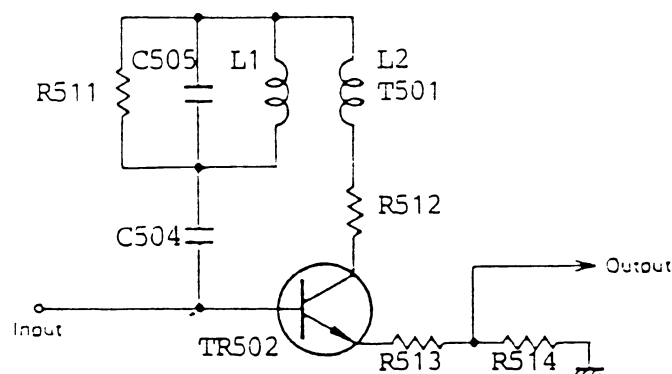
Fig. 6.1 HORIZONTAL OSCILLATION CIRCUIT

7. HORIZONTAL DRIVE CIRCUIT

The horizontal oscillation drive circuit is located between
the oscillation circuit and the output circuit, and its function
is to amplify the oscillation output and drive the output circuit.

In Fig. 8.1, its circuit is shown.

The oscillation output is applied to the base of TR503 which
amplifies it with switching. Since transformers are used, sharp
pulses generate when the transistors become ON/OFF. C507 and
C515 are inserted to absorb such pulses.
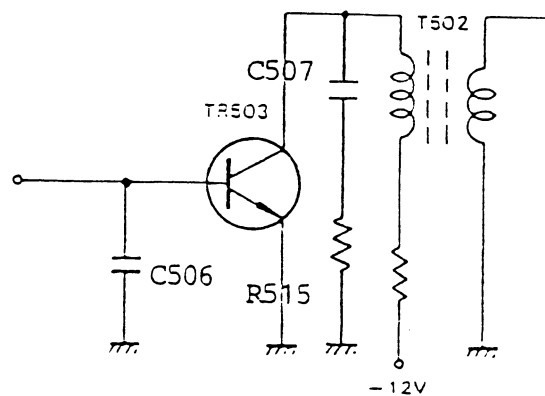
Fig. 7.1 HORIZONTAL DRIVE CIRCUIT

8. HORIZONTAL OUTPUT CIRCUIT

The horizontal output circuit has the function of sending sawtooth waves of 23.58KHz to the horizontal deflection coil. However, unlike the vertical output circuit, this is done by the switch operation of the transistors. Fig. 8.1 shows the horizontal output circuit.

F.B.T. makes about +18.4V of +12.0V (Vcc) using this switching mode, C512 and L504 improve horizontal linearity.
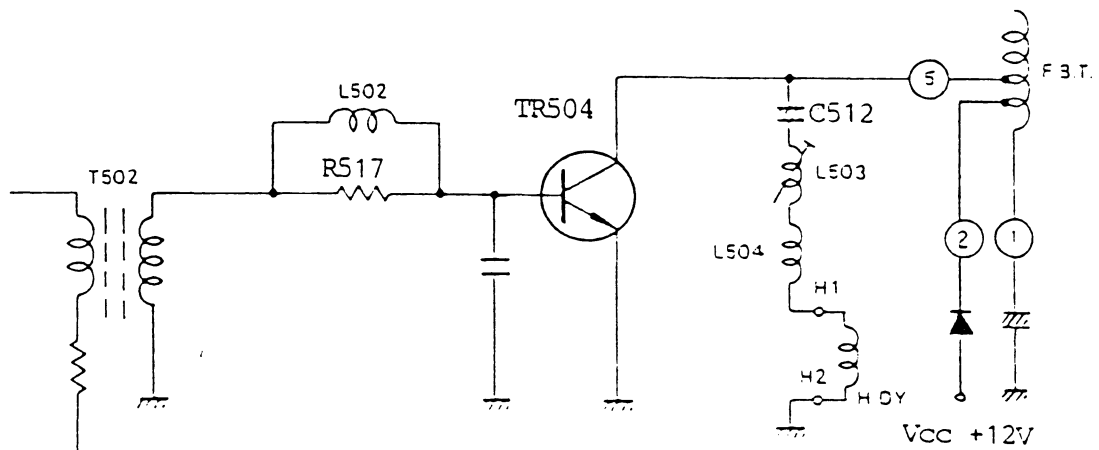
Fig. 8.1 HORIZONTAL OUTPUT CIRCUIT

PARTS LOCATION

CONNECTOR "C"
to CONTRAST VR   SUB CONTRAST VR 202

CONNECTOR "H"
to D.Y.

H. WIDTH L 503

FOCUS
VR 901

CONNECTOR "CE"
to C.R.T. EARTH

CONNECTOR "K"
to L.E.D.

CONNECTOR "L"
to BRIGHTNESS VR

CONNECTOR "S"
to POWER SW

| INPUT | SUB BRIGHTNESS | V. LIN | V. HEIGHT | V. HOLD | H. HOLD |
| CONNECTOR 8 P | VR 201 | VR 402 | VR 401 | VR 3 | T 501 |
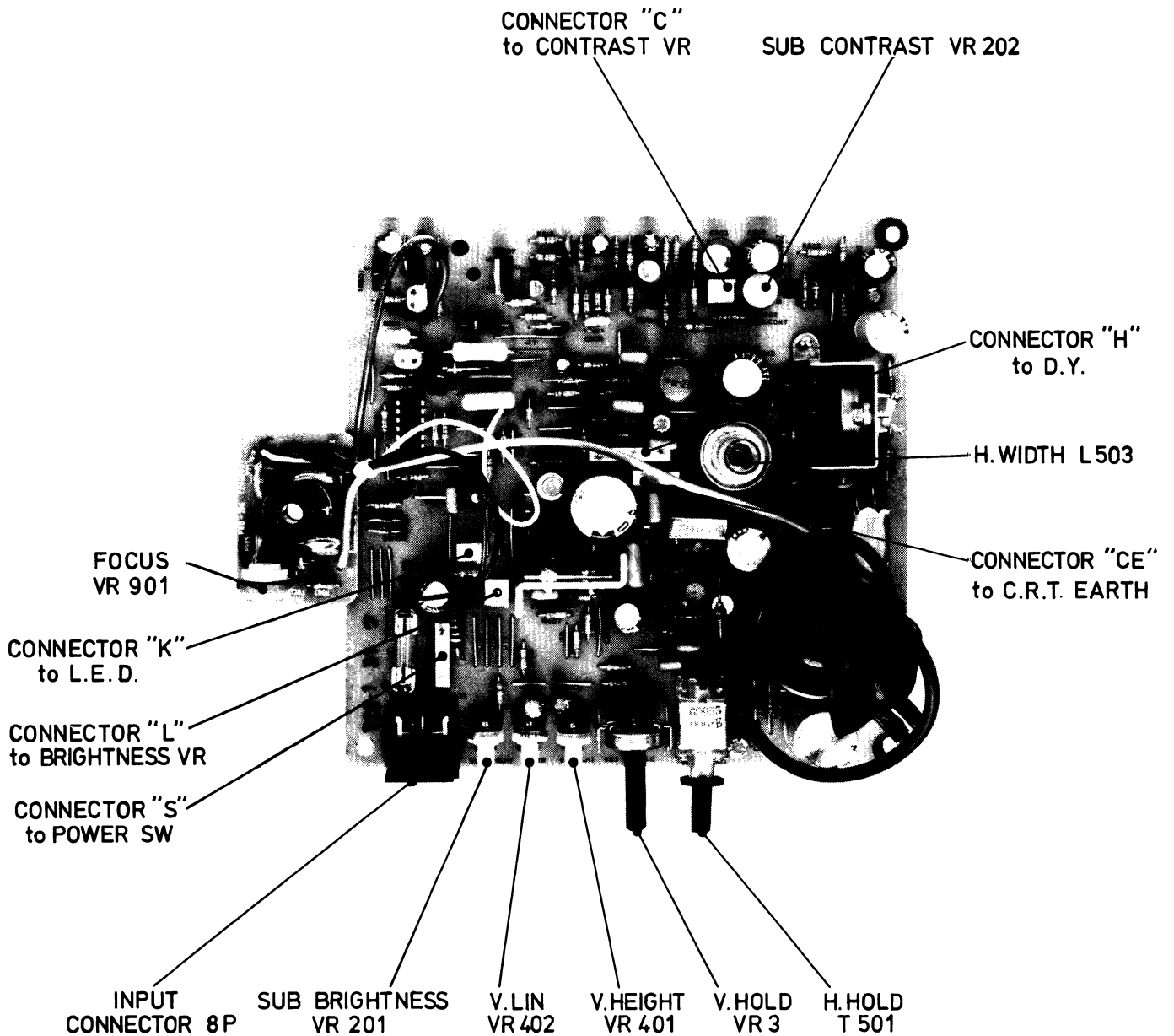
"PEOPLE" PARTS LOCATION (MAIN PWB , CRT PWB)

WARNING

CRT

ANODE CAP

SHORT CIRCUIT LEAD

* DANGER *
HIGH VOLTAGE

CRT EARTH WIRE
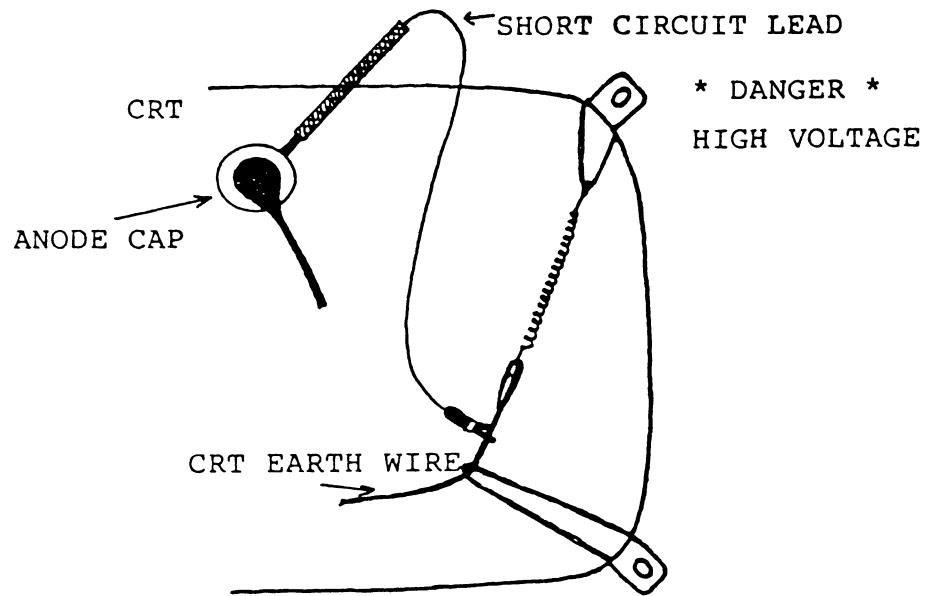
WARNING ---

Arcing ANODE LEAD to chassis or main PWB may damage transistors and IC.
When discharging picture tube (ANODE LEAD), arc to picture tube mounting
wire or picture tube tag only.·

The picture tube in this employs integral implosion protection. Replace
with a tube of the same type number for continued safety.

INPUT CONNECTOR PIN ASSIGNMENT

PWD-265
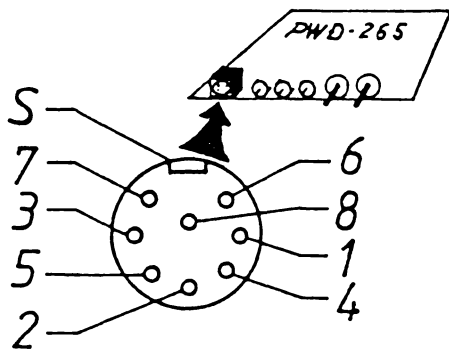
CONNECTOR: DIN 8a TYPE.

S is Sleeve.(Cable Shield)

Use twist pair cable to connect.

Pin No.	FUNCTION
S	FRAME GROUND
1	Vcc (+12.0V)
2	SIGNAL GROUND
3	H.SYNC.
4	SIGNAL GROUND
5	V.SYNC.
6	Vcc (+12.0V)
7	VIDEO
8	SIGNAL GROUND

"PEOPLE" BLOCK DIAGRAM
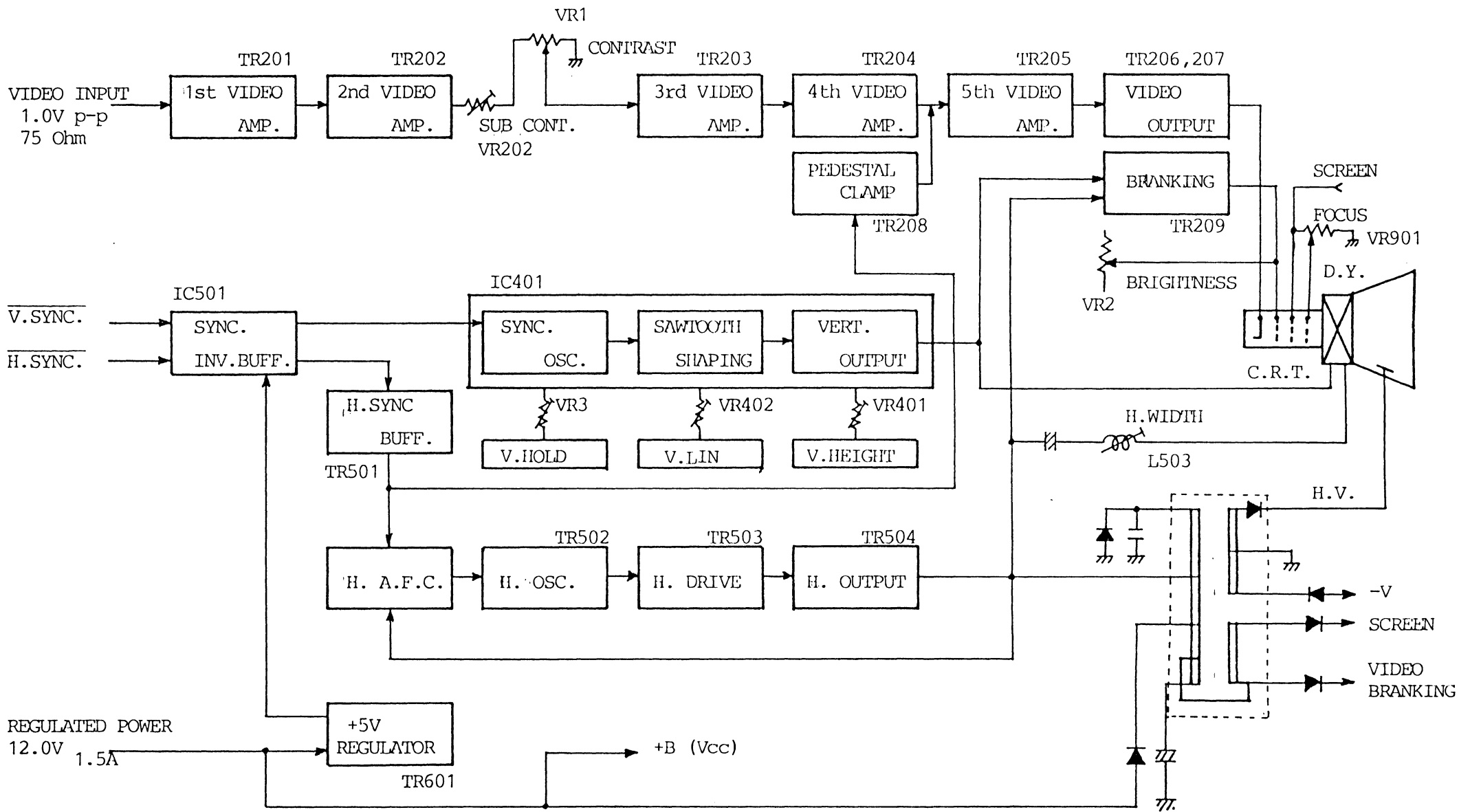
" P E O P L E "   SIGNAL TIMING CHART

HORIZONTAL

VIDEO

2.4u   4.0u   32.0u

SYNC.

4.0u   42.4u (23.58KHz)

VERTICAL

VIDEO

0.890m
(21H)   0.975m   20.14mS (475H)
(23H)

SYNC.

0.212m
(5H)   22.22mS (524H)   45.0Hz
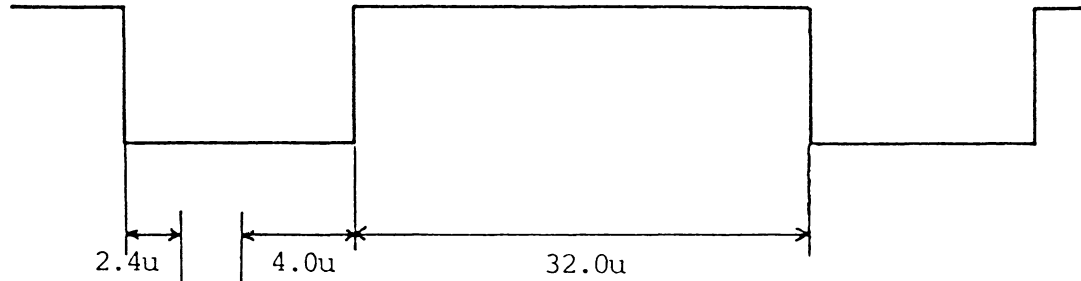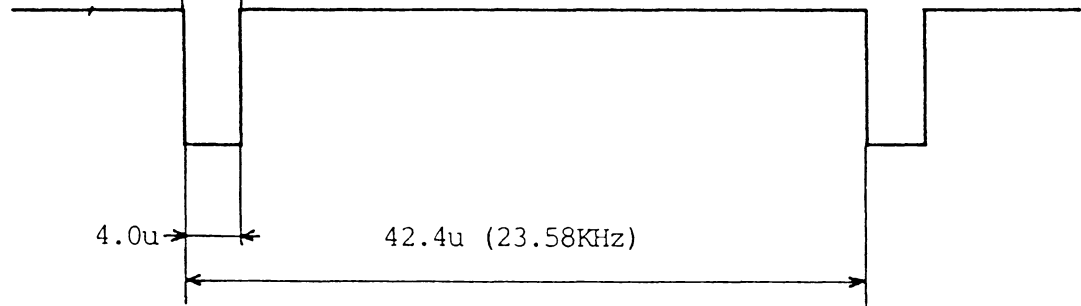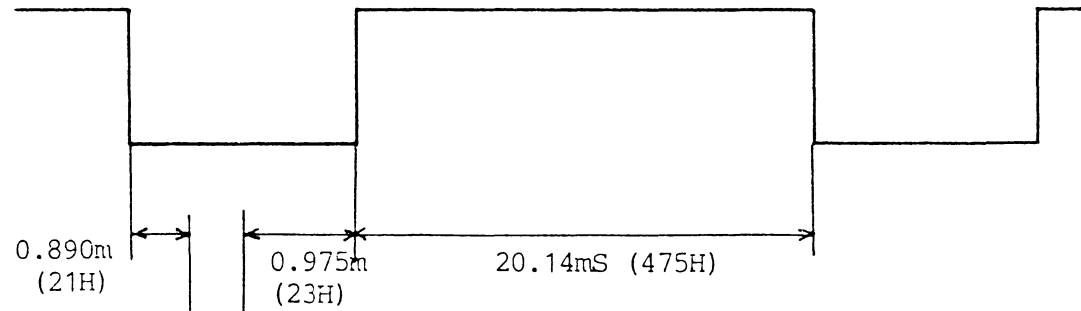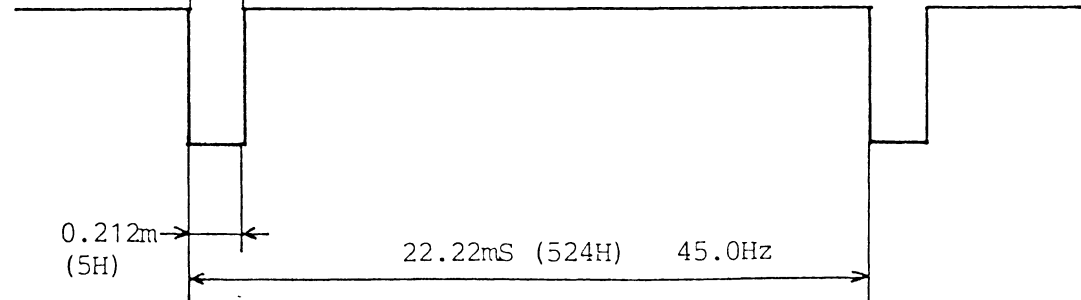
MONITOR ADJUSTMENT:

1. Display an all white pattern on the screen of the cathode ray tube (CRT).

2. Turn the CONTRAST and BRIGHTNESS knob fully clockwise,and then turn the SUB-BRIGHT (VR201) knob from its rightmost extremity until the background is no longer luminous.

3. Turn the SUB-CONTRAST (VR202) knob to a point where the CRT screen is 40Ft-L luminous.

4. HORIZONTAL SYNC. ADJUSTMENT: T501 (H.HOLD)

   (1) Receive a signal.
   (2) Short circuit between the PWD-265, base of TR501 and ground with capacitors of 100uF. Or H.SYNC signal cutoff.
   (3) Adjust T501 so that uniform picture is obtained.
   (4) Confirm that the picture does not change with power switch ON/OFF.

5. HORIZONTAL WIDTH ADJUSTMENT: L503 (H.WIDTH)

   (1) Display a character signal (for example: the letter 'H') fully on the CRT screen and adjust the BRIGHTNESS and CONTRAST to the maximum.
   (2) Turn the hexagonal core of L503 until the optimum horizontal amplitude is 210mm.

6. VERTICAL HEIGHT ADJUSTMENT (VR401,V.HEIGHT)
   VERTICAL LINEARITY ADJUSTMENT (VR402,V.LIN)

   (1) Display a character signal (for example: the letter 'H') fully on the CRT screen and adjust the BRIGHTNESS and CONTRAST to the maximum
   (2) Turn VR401 and VR402 until the optimum vertical amplitude is 155mm, and linearity is obtained.

7. FOCUS ADJUSTMENT (VR901)
   Bring the picture to the best focus by adjusting VR901.

People-Monitor
PARTS LOCATION

VR 202
SUB.CONT

L 503
H.WIDTH

VR 201
SUB BRIGHT

VR 401
V.HEIGHT

VR 402
V.LIN

VR 3
V.HOLD

T 501
H.HOLD

VR 901
FOCUS
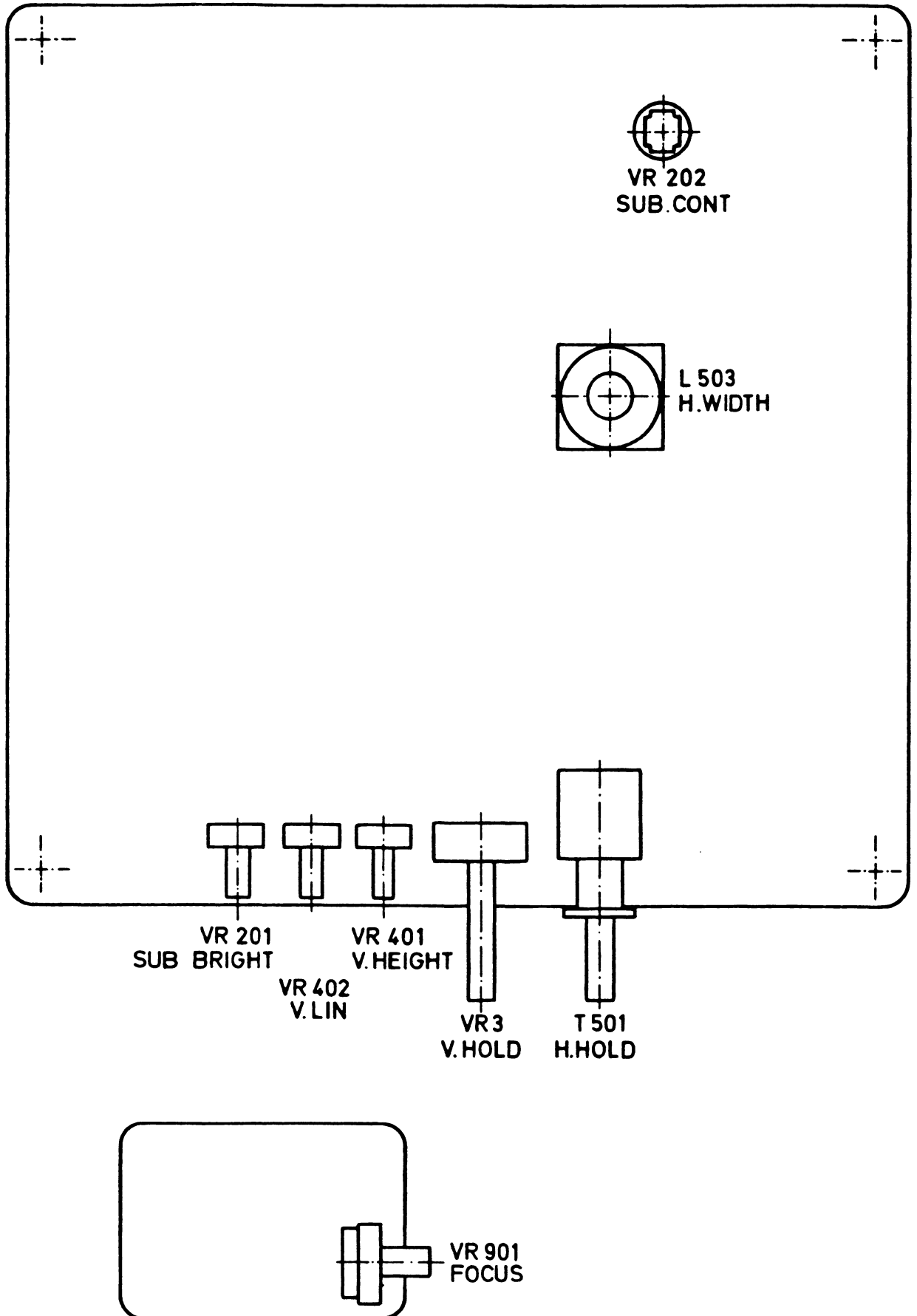
" PEOPLE " TROUBLESHOOTING

1. No POWER INDICATOR emitted & No Raster.

* Check Voltage of INPUT CONNECTOR. (pin 1,6   +12.0V±0.2V)

    (pin 2,4,8   Ground   )

* Check FUSE F1 (T2A 250V)

```
         ┌─── OPEN
         │                   ┌── OK
         ├──────── Replace ──┤
         │                   └── Breaks easily.
         └── OK                      │
                                     │
                           Failure of TR504,D503,
                              D504,C513,C515,C602,
                              C603,C604,C512
```
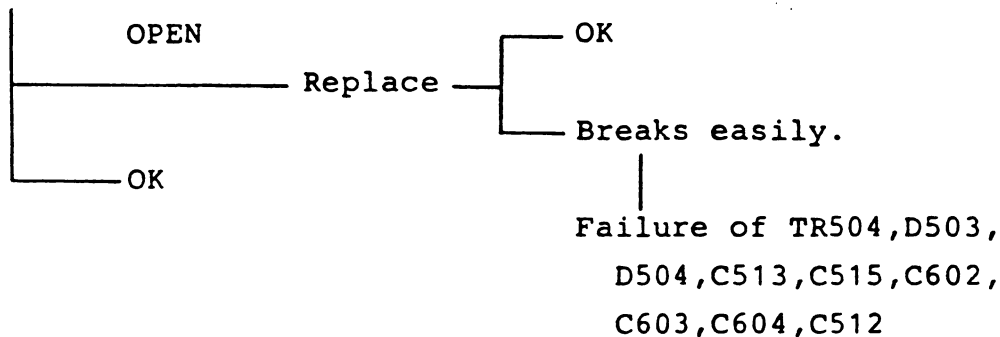
2. POWER INDICATOR EMITTED , BUT NO RASTER.

* Check the Waveform at INPUT CONNECTOR. (pin 3   H.SYNC)

    (pin 5   V.SYNC)

    (pin 7   VIDEO)

* Check CRT Heater

```
   ┌───── No Heater ───────────── CRT HEATER open.
   └───── Heater OK────────────── Next item.
```
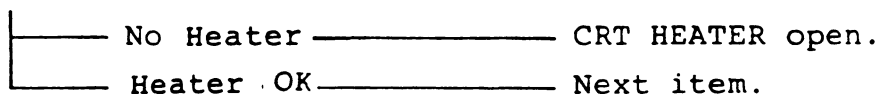
* Check BASE Voltage of TR504   NOTE(1)

```
   ┌───── 0V ─────── Failure of IC501,TR501,TR502,TR503,
   │                            T501,T502,R516
   └───── OK ─────── Next item.
```
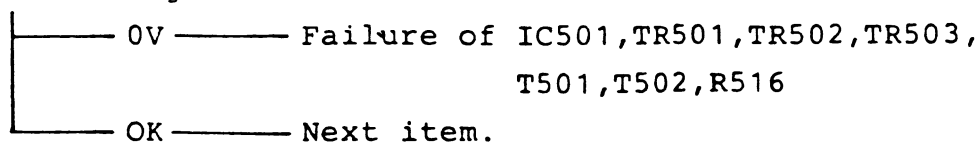
* Check Correct   Voltage of TR503

```
   │              ┌── LESS ─────────── Failure of R516,T502
   └──── 10V ─────┤
                  └── OK ───────────── Next item.
```
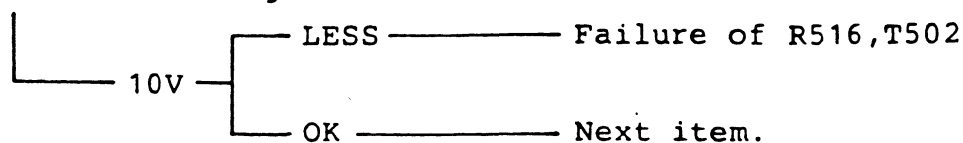
* Check Voltage of C211 positive side.

```
   │              ┌── LESS ─────────── Failure of R521,D507,
   └──── 60V ─────┤                              F.B.T.
                  └── OK ───────────── Next item.
```
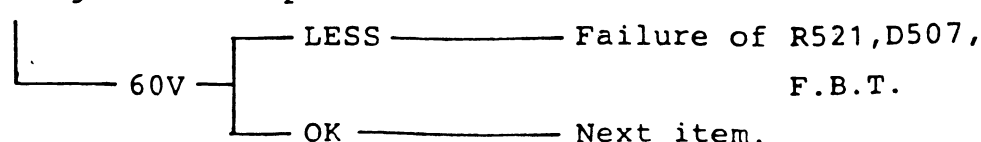
* Check Voltage of point SG.
```
        |                 ┌─ LESS ──────── Failure of R520,D505,
        └── 500V ──┤                              F.B.T.
                   └─ OK ──────── Next item.
```
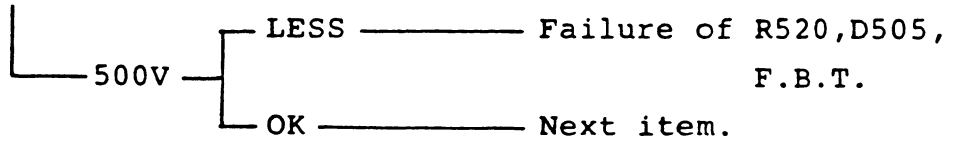
* Check Voltage of C513 positive side.
```
        |                 ┌─ LESS ──────── Failure of TR503,TR504,
        └── 18V ──┤                          D504,C513,F.B.T.
                  └─ OK ──────── Next item.
```
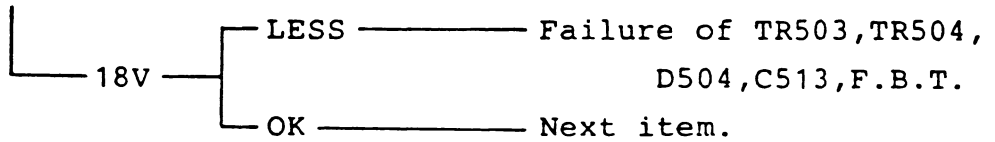
* Check Voltage of CRT ANODE.
```
        |                    ┌─ LESS ────── Failure of F.B.T.
        └── 12.5KV±1KV ──┤
                         └─ OK ────── Failure of CRT,
                                   circuit on PWD-266
```
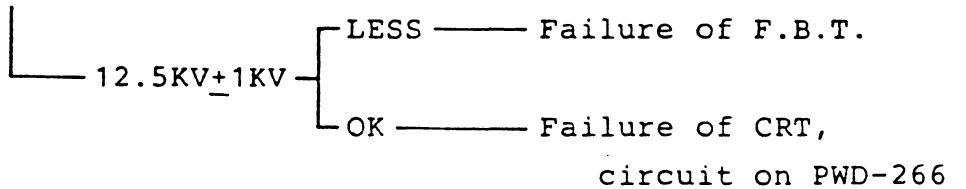
* All Voltage less ────────── Failure of TR504,D503,C511,D504

3. RASTER IS NORMAL , BUT NO PICTURE.

* Check the waveform at CRT PWB (PWD-266) Point K.
```
        ├──── No Output ─ Failure of Video Amplifier.
        |                          D204,D205,C201,C202,C203
        |                          C205,TR201 TR208
        |                          and Ambient circuit.
        └──── NORMAL ──── Failure of circuit on PWD-266.
                          Failure of TR209,CRT
```
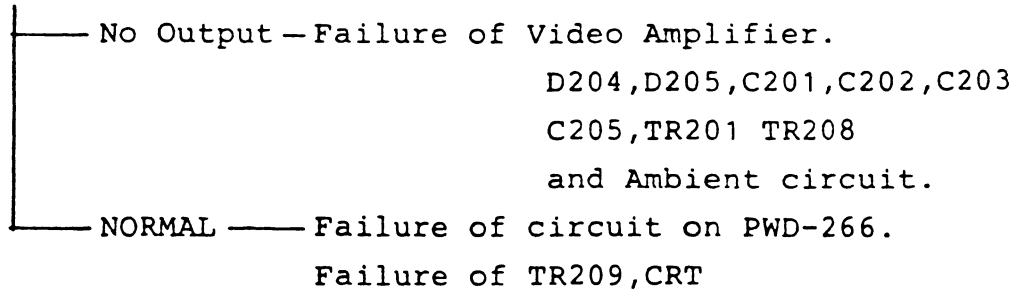
4. NO SWEEPING OR UNSTABLE VERTICAL.

* Check frequency variation by rotating V.HOLD (VR3).

```
├──── No Sweep ── Failure of deflection Yoke.
│                 Failure of IC-401 and ambient circuit.
│
└──── Oscillation frequency shifts.
                  └─ Failure of IC-401 and ambient circuit.
                  Failure of IC-501,ZD-490
```
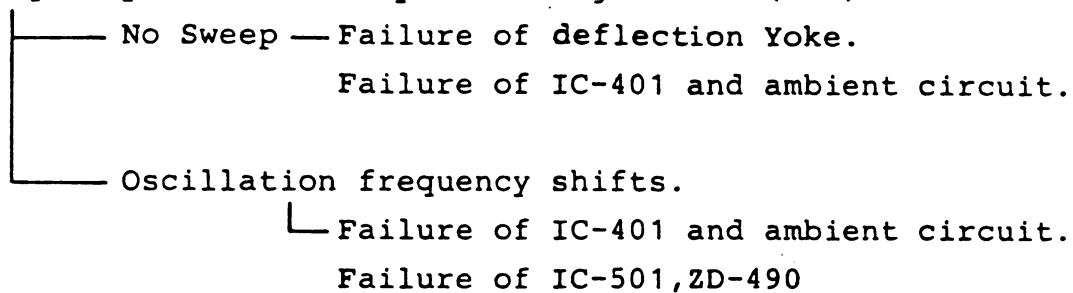
5. UNSTABLE HORIZONTAL.

* Check frequency variation by rotating H.HOLD (T501).

```
├──── Ok
│
└──── Oscillation frequency shifts.
                  └─ Failure of IC-501,TR501,TR502,C501,
                     C509,D501,D502,ZD590
```
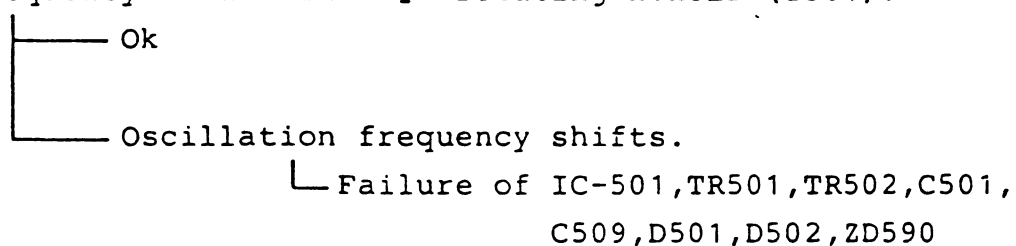
Note(1): In case AC10V range voltmeter is connected to the base
of TR504,the meter will deflect when the horizontal
oscillating circuit is oscillating,so it can be judged
whether the trouble exists before the oscillating circuit
or after the oscillating circuit.

*** Use Oscilloscope,Volt meter,High Voltage meter
and SCHEMATIC DIAGRAM. ***

ERSATZTEILE

Ersatzteile für People

Lfd.-Nr.	Bestell-Nummer	Benennung
1	53.501-1008.2	Floppy Drive
2	53.501-1016.2	Floppy Steuerkabel
3	53.501-1005.2	PCB OLP-1
4	53.501-1131.2	Ram-Erweiterung OLP-3
5	53.501-1019.2	Stromzuleitung für OLP-2
6	53.501-1020.2	Stromzuleitung für Floppy
7	53.501-1021.2	Stromzuleitung für OLP-1
8	53.501-1009.2	Stromversorgung
9	53.501-1018.2	Monitor Steuerkabel
10	53.501-1011.2	Lüfter
11	53.501-1136.2	Centronics-Steuerkabel
12	53.501-1137.2	V 24-Steuerkabel
13	53.501-1006.2	PCB OLP-2
14	53.501-1017.2	Tastatur-Steuerkabel
15	53.501-1007.2	Tastatur
16	53.501-1013.2	Bildschirm-Gehäuse
17	53.501-1015.2	Röhrenplatine
18	53.501-1010.2	Bildschirmplatine
19	53.501-1014.2	Bildschirmröhre
	nicht im Bild	
20	53.501-1012.2	Einstellwerkzeug für Floppy Drive
	siehe Blatt 2143	

19

16   17   18

1   2   3   4   5   6   7   8   9

12   11   10

13

15   14
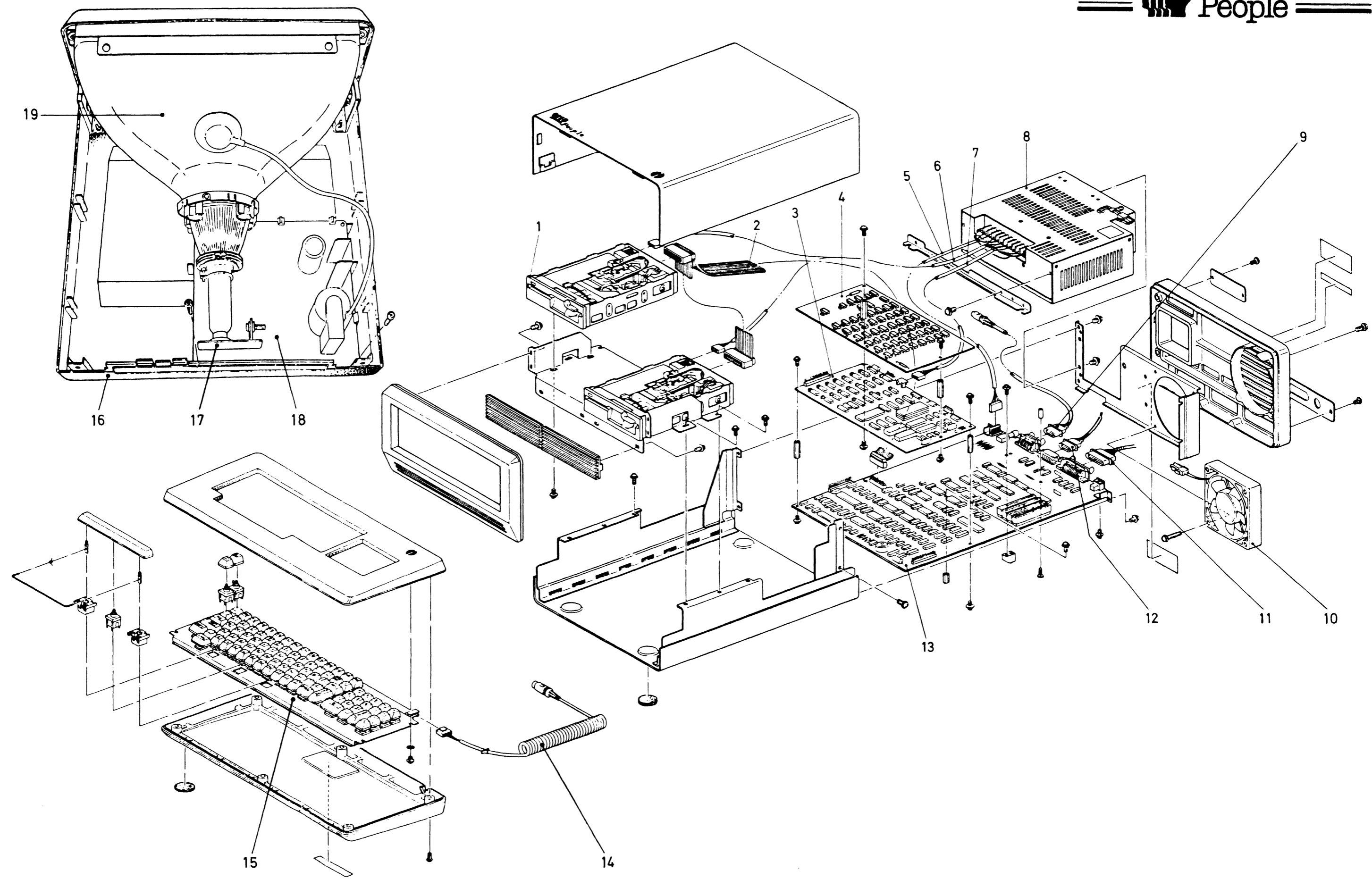
MODEL **OLYMPIA PEOPLE**
SCHEMATIC DIAGRAM
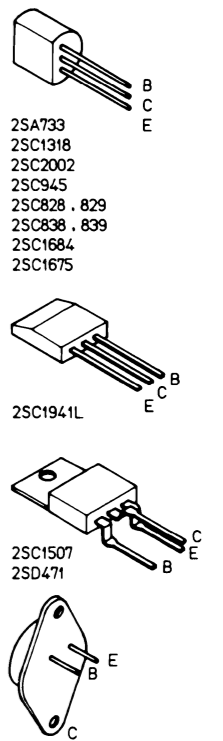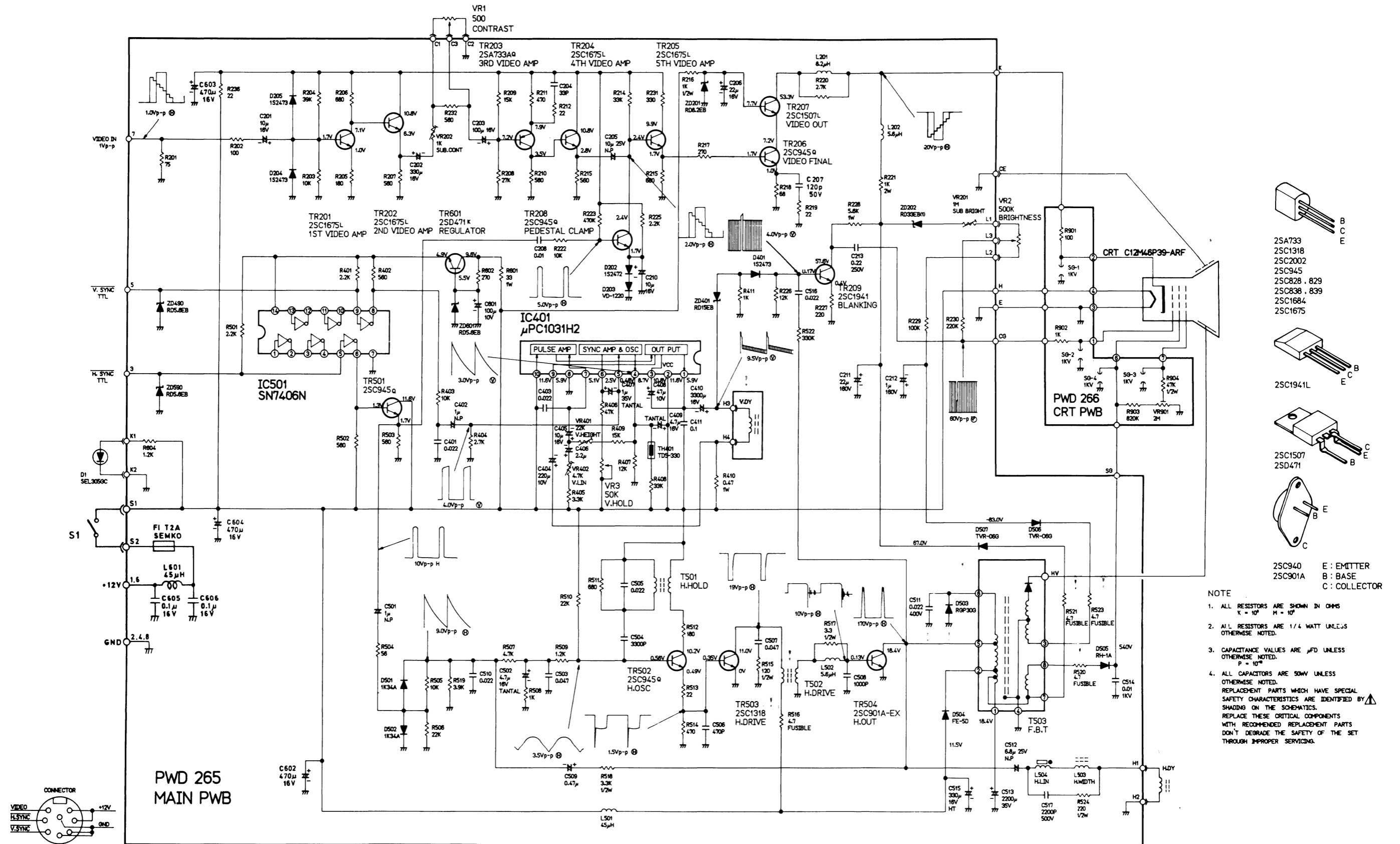
PWD 265
MAIN PWB

PWD 266
CRT PWB

CRT C12M45P39-ARF

2SA733
2SC1318
2SC2002
2SC945
2SC828 . 829
2SC838 . 839
2SC1684
2SC1675

2SC1941L

2SC1507
2SD471

2SC940
2SC901A

E : EMITTER
B : BASE
C : COLLECTOR

NOTE
1. ALL RESISTORS ARE SHOWN IN OHMS
   K = 10³   M = 10⁶
2. ALL RESISTORS ARE 1/4 WATT UNLESS
   OTHERWISE NOTED.
3. CAPACITANCE VALUES ARE µFD UNLESS
   OTHERWISE NOTED.
   P = 10⁻⁶
4. ALL CAPACITORS ARE 50WV UNLESS
   OTHERWISE NOTED.
   REPLACEMENT PARTS WHICH HAVE SPECIAL
   SAFETY CHARACTERISTICS ARE IDENTIFIED BY △
   SHADING ON THE SCHEMATICS.
   REPLACE THESE CRITICAL COMPONENTS
   WITH RECOMMENDED REPLACEMENT PARTS
   DON'T DEGRADE THE SAFETY OF THE SET
   THROUGH IMPROPER SERVICING.

CONNECTOR
VIDEO
H.SYNC
V.SYNC
+12V
GND

PEOPLE

PWS
A.C. CORD

1
2 OT
3
4
5 +5T
6
7
8 +12T(M)
9 +12U
10 -12U

CN4
CN3 CN1

OLP1   OLP3

CN1   CN2
CN1   CN2

POW

CLP2

FAN

FDD
A   FAC1
FBC1

FDD
B   FAC2
FBC2

FDD

CRT1   CRT2   CRT4

OLP4

KB

KB

RS232C

PARA

CRT3

CRT
(Monochrome
CRT or
color)
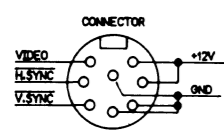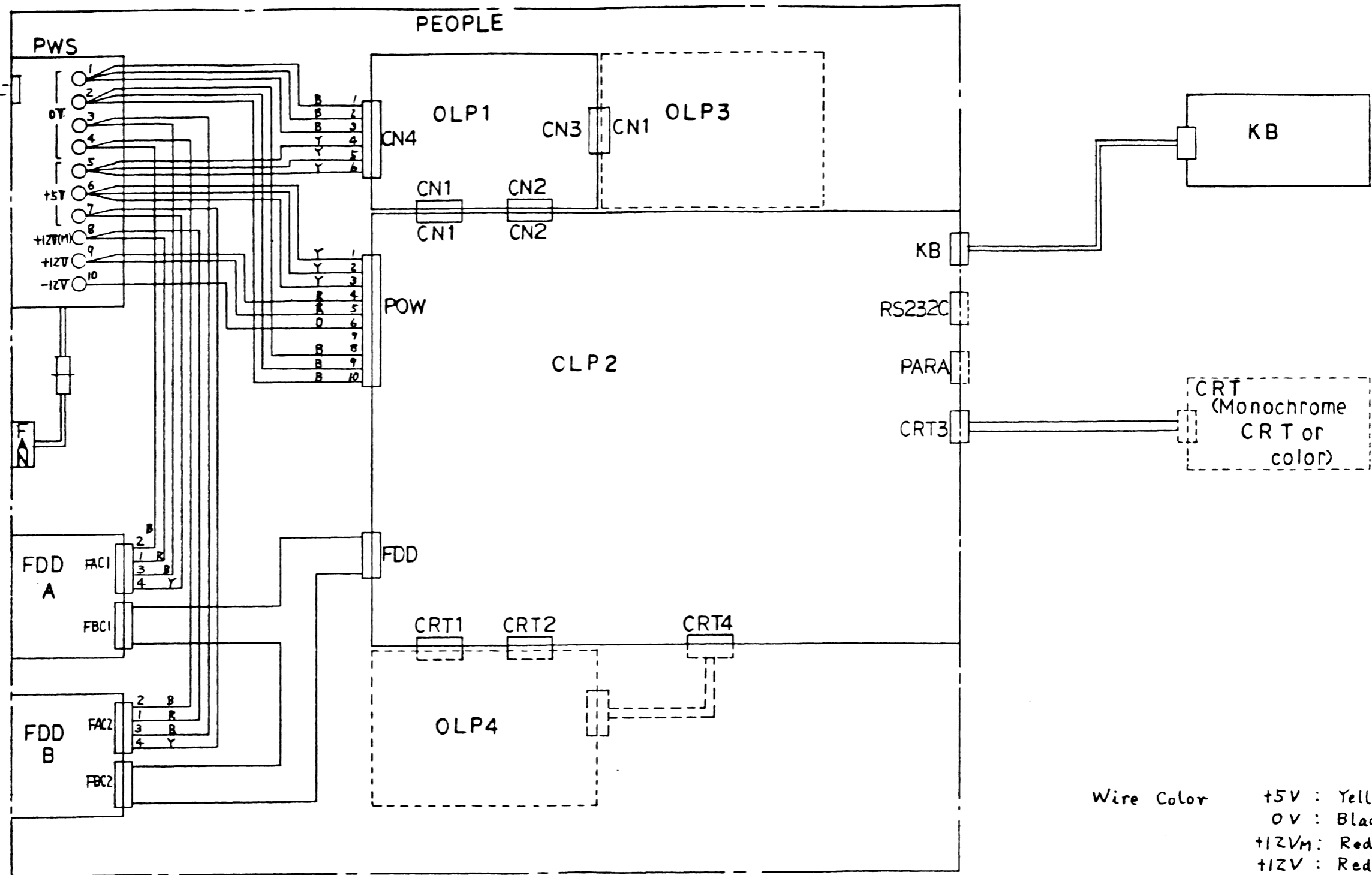
Wire Color   +5V : Yellow
              0V   : Black
              +12Vm: Red
              +12V : Red
              -12V : Orange

UNIT IN mm
PROJ: SCALE /

NOTE:

OLYMPIA
PEOPLE

TITLE:
CIRCUIT DIAGRAM
DRG. NO.
FC5048D_071
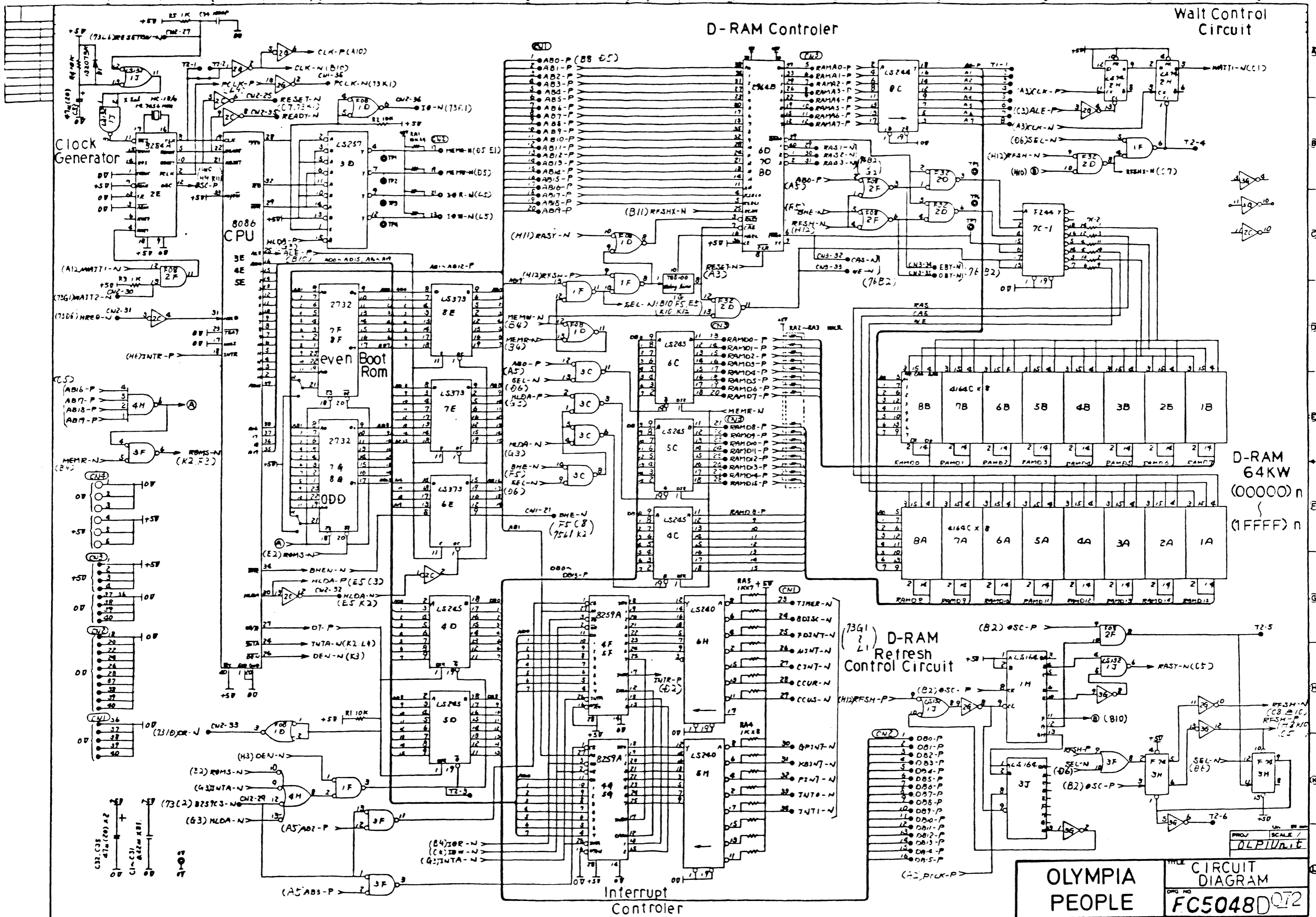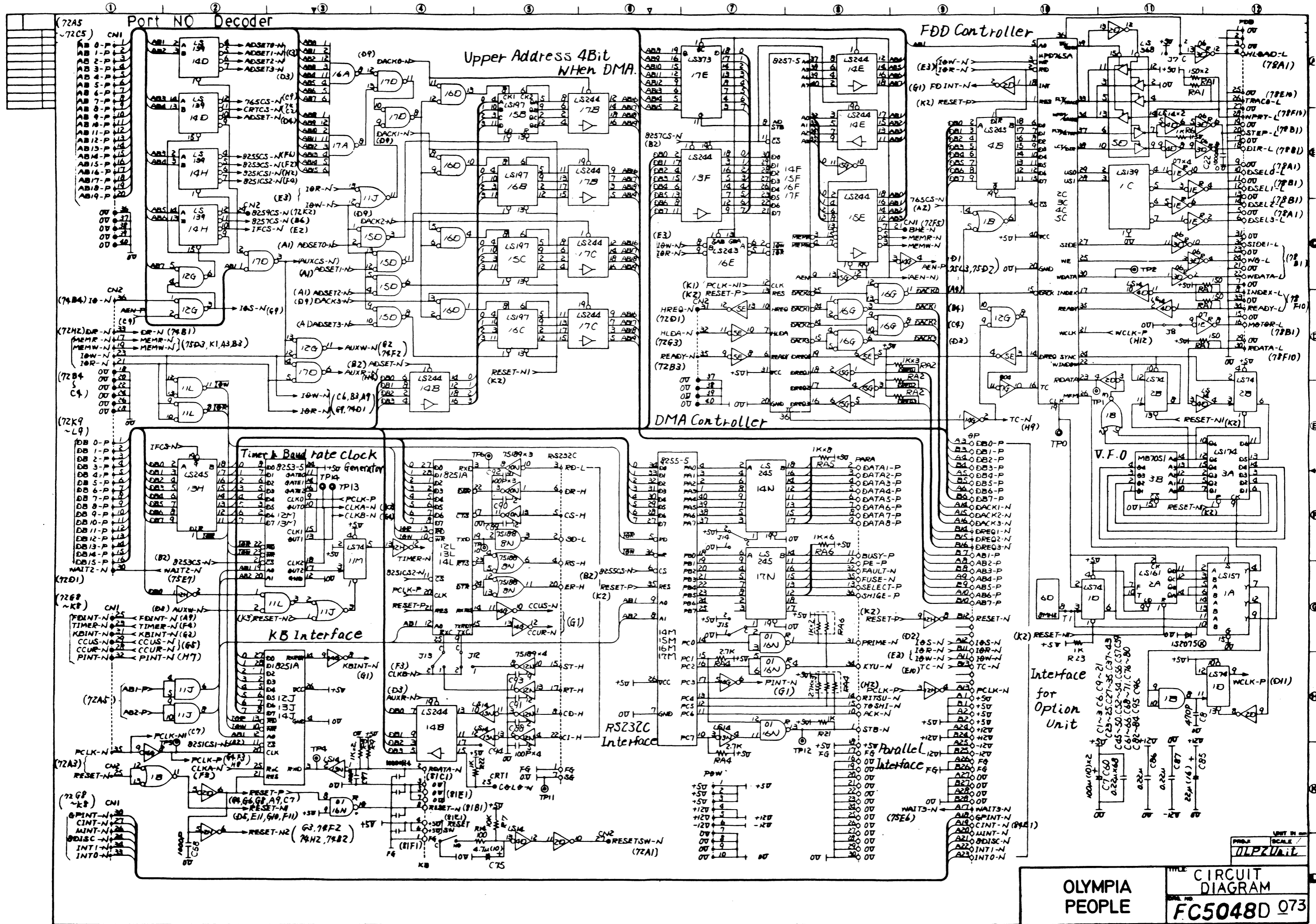
CIRCUIT DIAGRAM

OLYMPIA PEOPLE

FC5048D

Character Generator
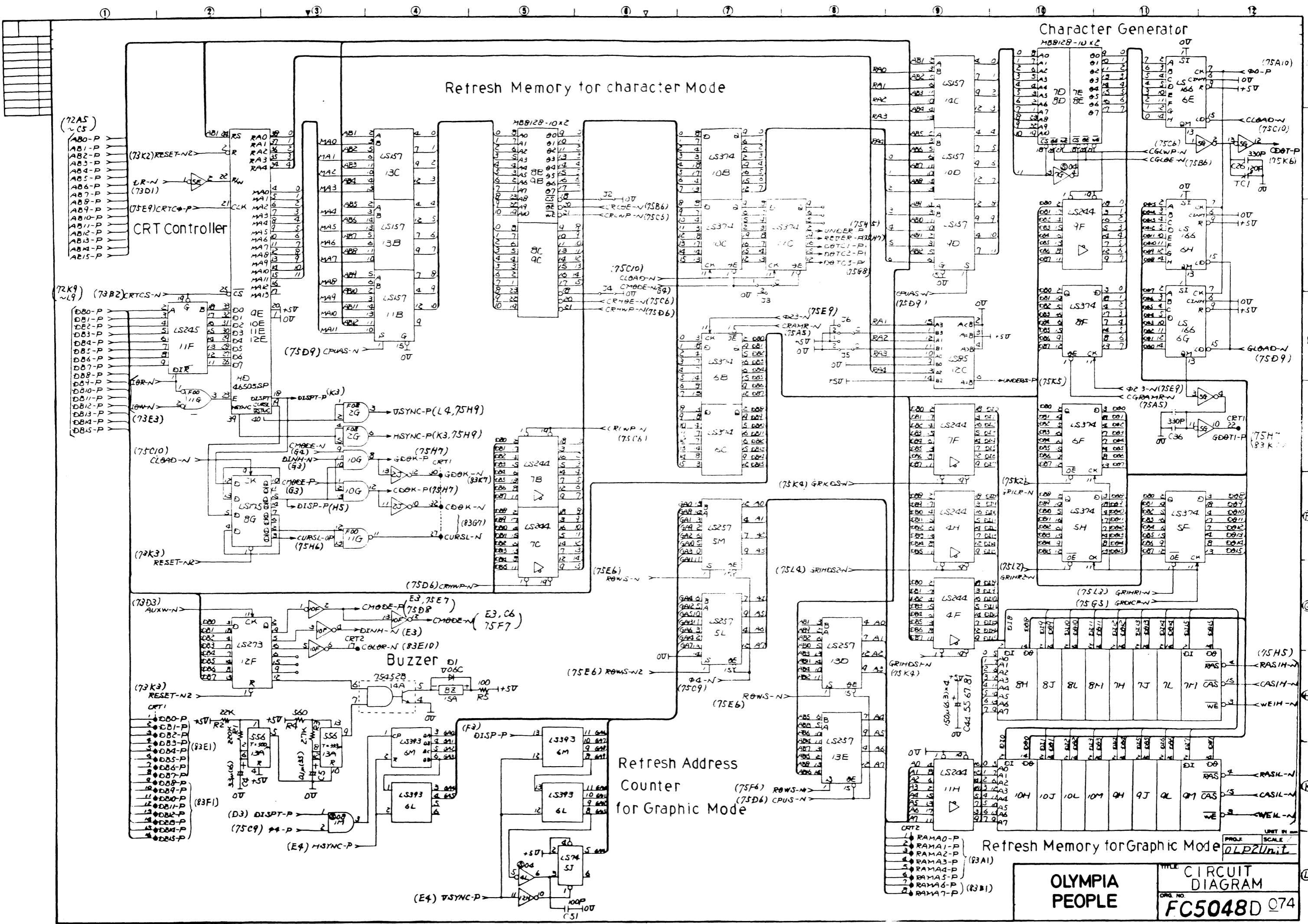
Retresh Memory for character Mode

CRT Controller

Retresh Address Counter for Graphic Mode

Buzzer

Retresh Memory for Graphic Mode

OLYMPIA
PEOPLE

CIRCUIT
DIAGRAM

FC5048D Q74
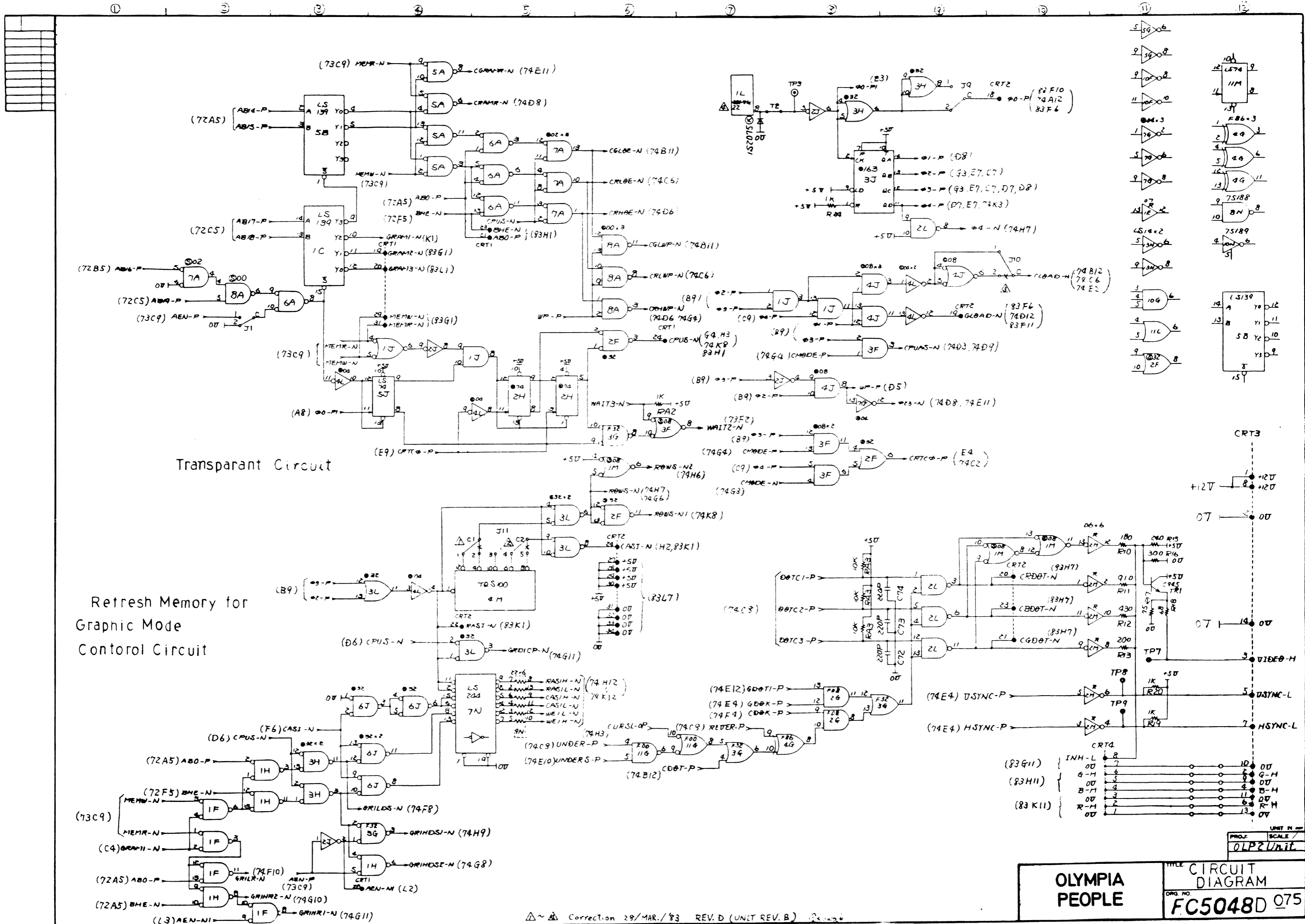
Transparant Circuit

Retresh Memory for
Graphic Mode
Contorol Circuit

OLYMPIA
PEOPLE

TITLE CIRCUIT
DIAGRAM

ORG. NO. FC5048D 075

OLP2Unit

△ ~ △ Correction 28/MAR./'83   REV. D (UNIT REV. B)

OLYMPIA
PEOPLE

CIRCUIT
DIAGRAM

FC5048D 076

HEAD CARRIAGE ASSY

PCBA MFD CONTROL
15531860-24

HLOAD-L	J1-4	
DSEL3-L	J1-6	
INDEX-L	J1-8	
DSEL0-L	J1-10	
DSEL1-L	J1-12	
DSEL2-L	J1-14	
MOTOR-L	J1-16	
DIR-L	J1-18	
STEP-L	J1-20	
WDATA-L	J1-22	
WG-L	J1-24	
TRAC0-L	J1-26	
WPRT-L	J1-28	
RDATA-L	J1-30	
SIDE1-L	J1-32	
READY-L	J1-34	
SIGNAL GROUND	J1-1~33 ODD NOS	

$(23 A/2 \sim D12)$

PCBA READ WRITE AMP
15531870-30

FPT SENSOR	J5-3	J5-3	$(79A1 \sim C1)$ J9-4	SIDE0 SHIELD
INDEX SENSOR	J5-7	J5-7	J9-12	SIDE0 R/W START
W GATE	J5-6	J5-6	J9-2	SIDE0 R/W FINISH
12 V	J5-13	J5-13	J9-10	SIDE0 COMMON
SIDE 1 SELECT	J5-8	J5-8	$(79F10)$ J9-8	SIDE0 ERASE
W DATA	J5-10	J5-10	J9-3	SIDE1 SHIELD
ERASE GATE	J5-9	J5-9	$(79C1 \sim D1)$ J9-11	SIDE1 R/W START
INDICATOR	J5-4	J5-4	J9-1	SIDE1 R/W FINISH
POWER SENSE	J5-1	J5-1	J9-9	SIDE1 COMMON
R DATA	J5-5	J5-5	$(79F10)$ J9-7	SIDE1 ERASE
5 V	J5-12	J5-12		
0 V	J5-14	J5-14		

SIDE0 HEAD

SIDE1 HEAD

FRONT LED

+12 V	J2-1	
0 V	J2-2	$(78G1 \sim H1)$
0 V	J2-3	
+5 V	J2-4	

$(78D1)$

TRACK 00 SENSOR LED	J4-4
TRACK 00 SENSOR	J4-5
0 V	J4-6

TRACK 00 SENSOR

$(78B10)$

HEAD LOAD SOL GND	J4-1
HEAD LOAD SOL POWER	J4-2

HEAD LOAD SOLENOID

$(80C8 \sim E8)$

DC MOTOR ON	J7-3
0 V	J7-2
+5 V	J7-4
+12 V	J7-1

PCBA DD MOTOR SERVO

DD MOTOR ASSY

$(78C10 \sim D10)$

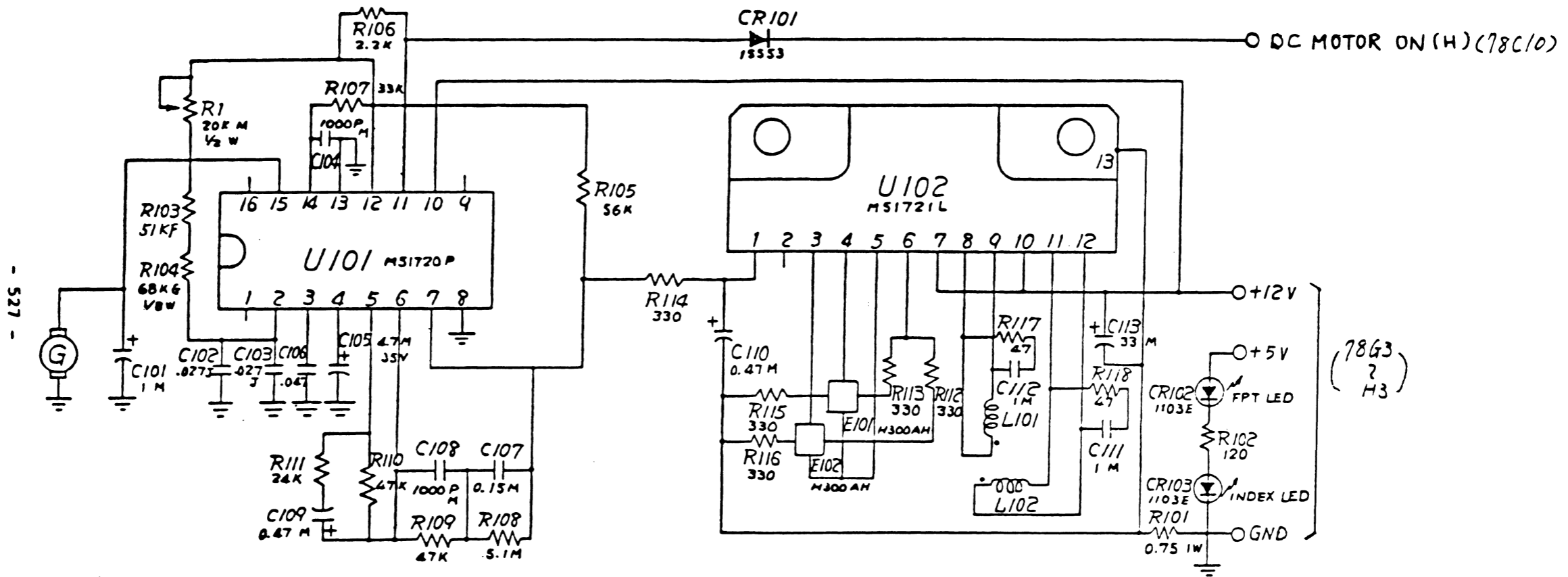| PHASE A	J6-1
PHASE Ā	J6-3
PHASE B	J6-2
PHASE B̄	J6-4
COMMON A	J6-5
COMMON B	J6-6

STEPPING MOTOR ASSY

FRAME GND

UNIT IN

PROJ: SCALE /
FDD Unit

OLYMPIA PEOPLE

TITLE: CIRCUIT DIAGRAM

DRG. NO. FC5048D 077

PCBA MFD CONTROL

OLYMPIA PEOPLE

TITLE: CIRCUIT DIAGRAM

DRG NO. FC5048D 078

PCBA READ WRITE AMP

OLYMPIA PEOPLE
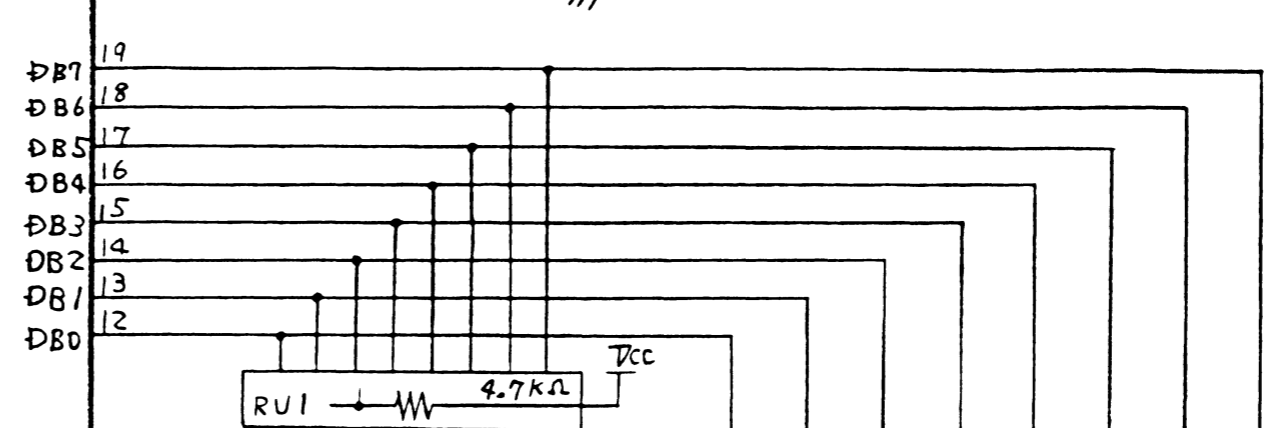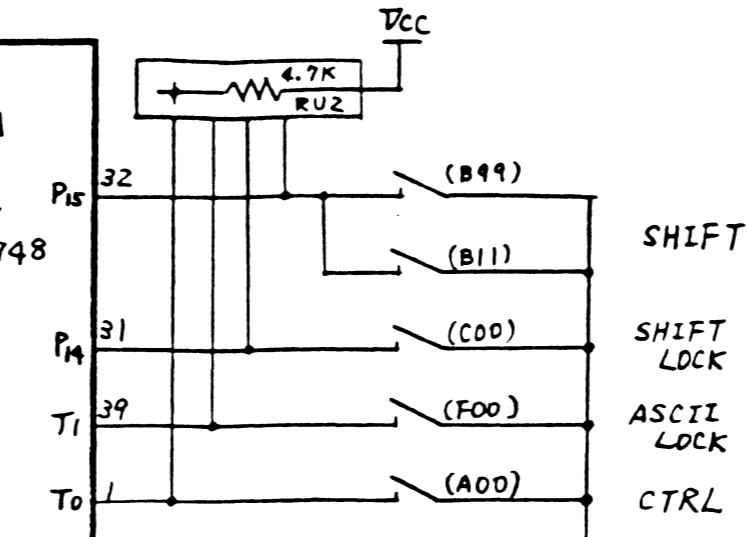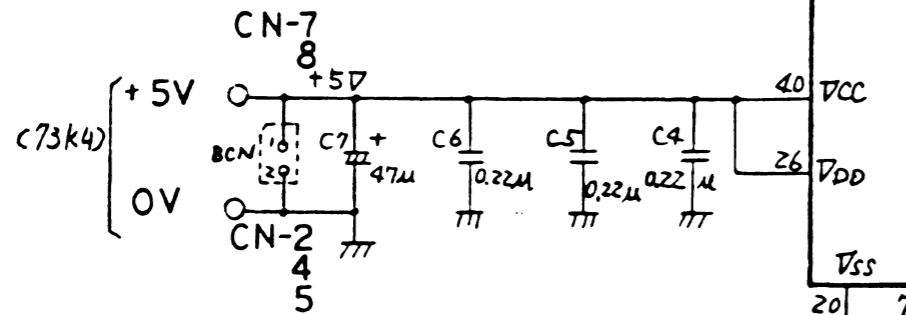
TITLE: CIRCUIT DIAGRAM

FDD Unit

DRG NO: FC5048D 079

R106 2.2K

CR101 1SS53

○ DC MOTOR ON (H) (78C10)

R107 33K

R1 20K M ½ W

C104 1000P M

R105 56K

U102 MS1721 L

13

1 2 3 4 5 6 7 8 9 10 11 12

R103 51KF

R104 68KG V8W

16 15 14 13 12 11 10 9

U101 MS1720P

1 2 3 4 5 6 7 8

R114 330

○ +12V

(G)

C101 1M

C102 .0275 J

C103 .027 J

C106 .047

C105 4.7M 35V

C110 0.47M

R115 330

E101 H300AH

R113 330

R112 330

R117 47

C112 1M

L101

C113 33M

R118 47

+5V

CR102 1103E FPT LED

R102 120

R111 24K

R110 47K

C108 1000P M

C107 0.15M

R116 330

E102 H300AH

C111 1M

CR103 1103E INDEX LED

C109 0.47M

R109 47K

R108 5.1M

L102

R101 0.75 1W

○ GND

(78G3 2 H3)

PCBA DD MOTOR SERVO,

- 527 -

UNIT IN mm

PROJ: SCALE /

FDD Unit

OLYMPIA PEOPLE

TITLE: CIRCUIT DIAGRAM

DRG. NO. FC5048D 080

Key layout : refer to Hardware Manual page H-4-13

M 1
8048/8748

2
C1 20p   XL
3
C2 20p

Vcc
D1   RU2 4.7K
(73k4)RESET-N○ CN-3   4 RESET
C3 4.7µ

4.7K RU2   Vcc
P15 32
(B99)
(B11) SHIFT
P14 31   (C00) SHIFT LOCK
T1 39   (F00) ASCII LOCK
T0 1   (A00) CTRL

(73k4)RDATA-N○ CN-1 8 >9 7406   34 P17
Vcc R2 180Ω M4 2 M4 1   21 P20
      C00
R3 180Ω F00 4 M4 3   22 P21
                            6 INT

Vcc
4.7k RU2
25 PROG
5   SS

CN-7
8
+5V +5V
(73k4) BCN 10 39 C7 47µ C6 0.22µ C5 0.22µ C4 0.22µ
0V
CN-2
4
5

(73L4) F6 CN-6 FG
Pt LAND

40 Vcc
26 VDD
Vss EA
20 7

DB7 19
DB6 18
DB5 17
DB4 16
DB3 15
DB2 14
DB1 13
DB0 12

RU1 4.7kΩ   Vcc

P13 30   12 D
P12 29   13 C   M2 LS145
P11 28   14 B
P10 27   15 A

11 M4 Vcc
10   RI 4.7K
12 D
13 C   M3 LS145
14 B
15 A

Key No.

Y0 ... Y15

X0 X1 X2 X3 X4 X5 X6 X7

Xn   Yn

UNIT IN mm
PROJ: SCALE /
KB Unit

NOTE:

OLYMPIA PEOPLE

TITLE:
CIRCUIT DIAGRAM
DRG. NO.
FC5048D_081
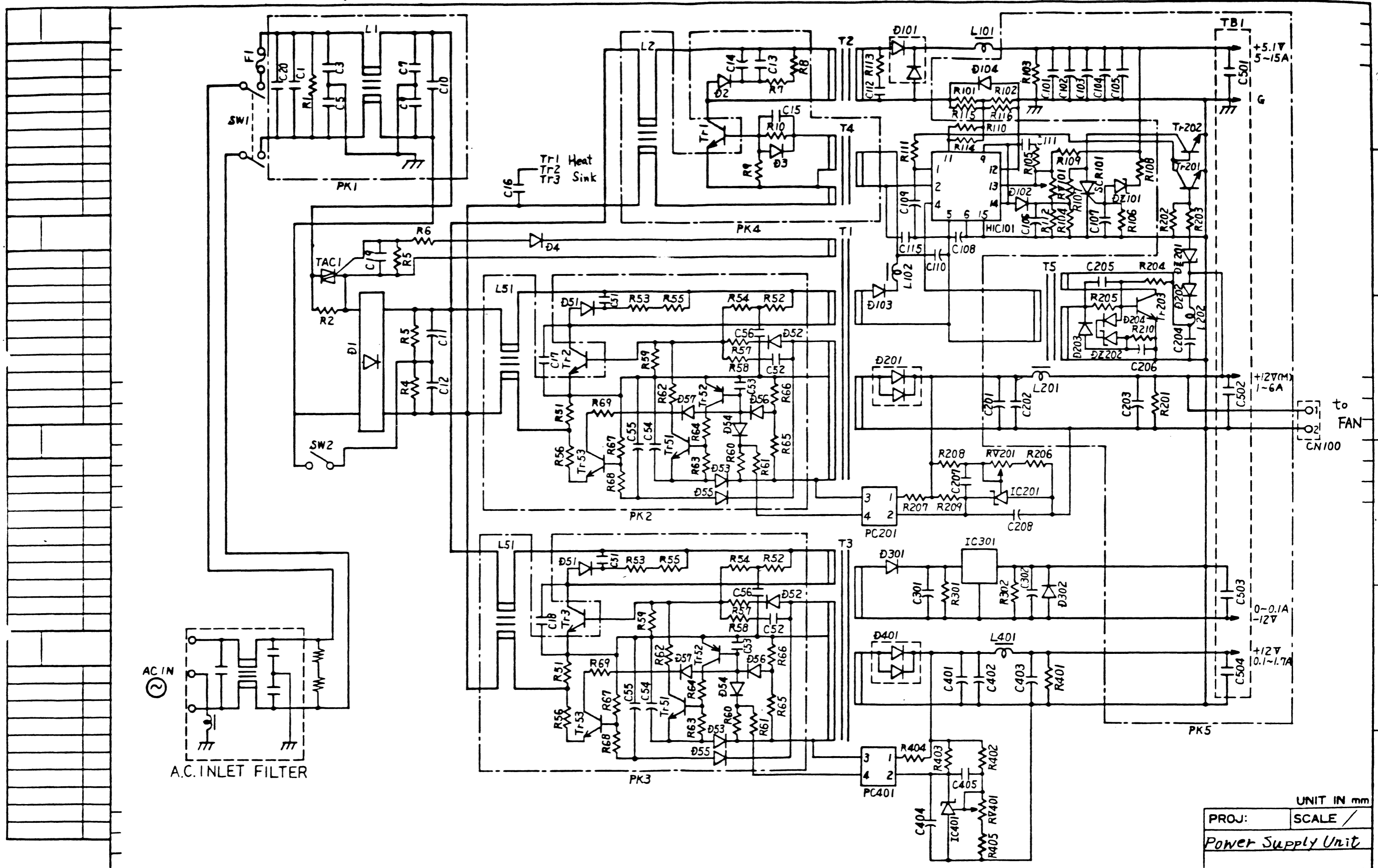
UNIT IN mm

PROJ:	SCALE /
Power Supply Unit	

OLYMPIA PEOPLE

TITLE:

CIRCUIT DIAGRAM

DRG. NO.

FC5048D _082

NOTE:

A.C. INLET FILTER

AC IN