NCR

Personal Computer

Pc 6

Technical Reference

First Edition, April 1985

PREFACE

The NCR **TECHNICAL REFERENCE** manual is designed for programmers, engineers, designers, technical personnel, and others whose use of the NCR PERSONAL COMPUTER PC6 requires knowledge of its general architecture and system design. This publication provides specific information for sophisticated programming as well as interfacing and expanding the hardware.

The first three chapters describe the system components and include functional block diagrams, operating characteristics, hardware and software information, connector specifics, and pin configurations. Chapter 4 is included as a convenient location for filing the ROM information, and the appendices contain quick reference material on the character set, op-codes, switch and pin-out configurations, component specifications, and logic diagrams. A glossary and an index are also included.

Requests for copies of this manual and for technical information about the system should be made to your authorized NCR Personal Computer dealer.

The **TECHNICAL REFERENCE** manual is part of a library of NCR PERSONAL COMPUTER PC6 documentation. User information is provided in the following documents:

NCR Owner's Manual (PN: 150-0000591)

NCR-DOS (PN: 150-0000596)

GW-BASIC (PN: 150-0000602)

NCR-DOS PROGRAMMER'S MANUAL (NCR order number G6B1-0204-0000)

TECHNICAL REFERENCE MANUAL (PN: 150-0000610; NCR order number D1-0315-A)

HARDWARE MAINTENANCE AND SERVICE MANUAL (PN: 150-0000614; NCR order number D1-0314-A)

PARTS CATALOG (PN: 150-0000620; NCR order number D1-0313-A)

The integrated circuit chips that are used in the NCR Personal Computer are produced by Intel Corporation, Motorola Semiconductor Products Inc., NEC Electronics USA Inc., and Western Digital Corporation. Descriptions of the chips in this document are adaptations of specifically furnished information by these manufacturers.

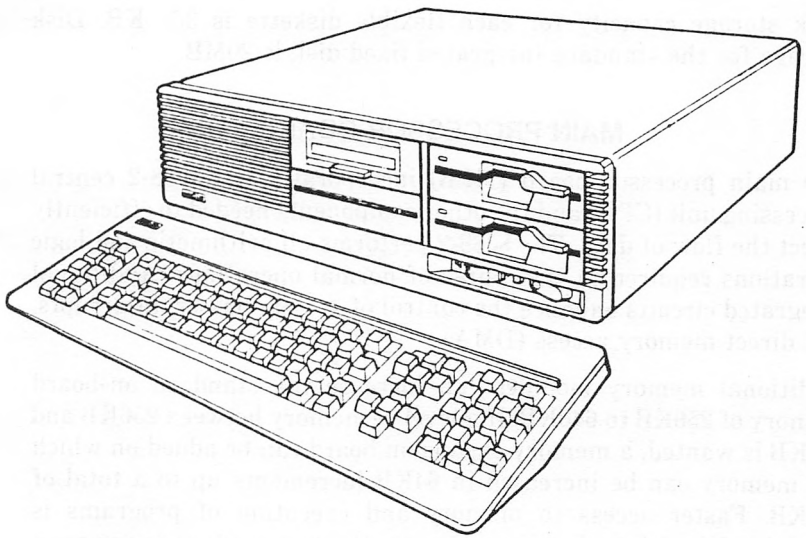
Technical Reference

Contents

Primary System Components

This chapter contains technical reference information about the primary system components of the NCR PERSONAL COMPUTER PC6. Primary components are the internal subsystems that are basic and required by the personal computer.

The PC6, a modular unit consists of a base unit with the central processor and memory storage systems, and a separate keyboard. It is intended to operate on 110/120 volt AC power source except when equipped to operate on 220 volt power.



MODEL DESCRIPTION

The NCR PERSONAL COMPUTER PC6 is available in several models which vary by disk drive and other memory storage device combinations. Three of the standard combinations are:

Model	Memory Storage Device
1012	Two flexible disk drives
1014	One flexible disk drive, one fixed disk drive
1015	One flexible disk drive; one fixed disk drive, one magnetic tape drive

The main memory of all models can be either 256KB or more, determined by memory modules mounted on the main processor board. Also, an optional memory expansion card can be added to increase the 256KB memory mounted on the main board to a system total of 640KB in 64KB increments.

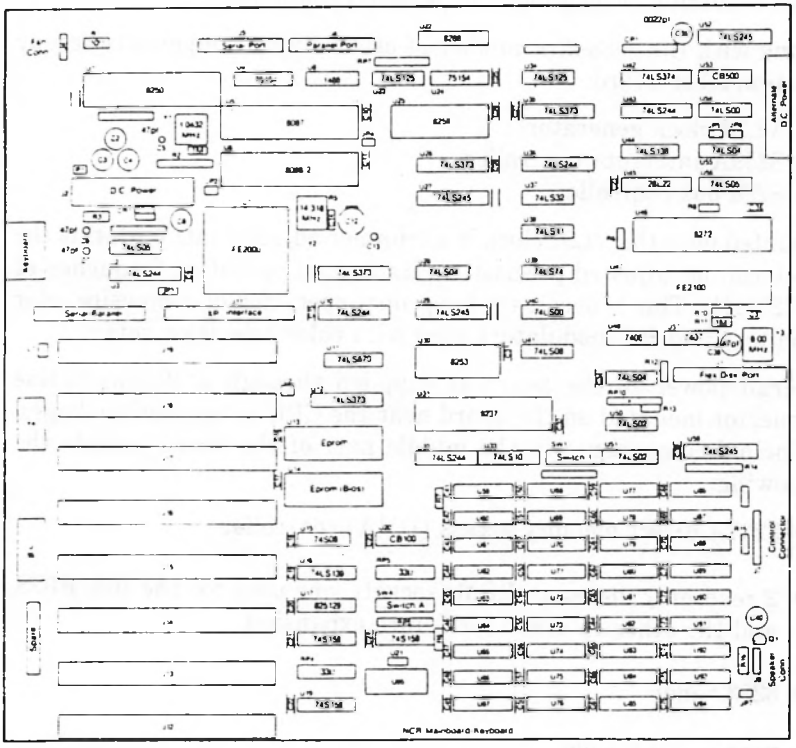
Disk storage capacity for each flexible diskette is 360 KB. Disk storage for the standard integrated fixed disk is 20MB.

MAIN PROCESSOR BOARD

The main processor board (MPB) incorporates the 8088-2 central processing unit (CPU) and the other components needed to efficiently direct the flow of data. The 8088-2 performs all arithmetic and logic operations required in the course of normal operations. Additional integrated circuits enhance the control of system busses, interrupts, and direct memory access (DMA).

Additional memory modules can increase the standard on-board memory of 256KB to 640KB. If a level of memory between 256KB and 640KB is wanted, a memory expansion board can be added on which the memory can be increased in 64KB increments up to a total of 640KB. Faster access to memory and execution of programs is possible with on-board memory because the memory board requires a wait state when the system is operating at the faster of its two speeds. Memory populated on the MPB will run at either speed.

Eight 62-pin expansion slots provide plug-in compatibility for special-function boards. On-board connectors link the boards to various input/output devices.



The main processor board mounts horizontally in the lower part of the computer. Access to the expansion slots and sockets for pluggable memory chips is straightforward and easy by removing the upper cover of the computer.

PHYSICAL DESCRIPTION

The main processor board is a multilayered printed circuit measuring 11.00 by 12.00 inches. The board is mounted horizontally in the lower part of the personal computer chassis. The board fits into slides on the bottom of the chassis. To align the board precisely, there is a keyed slot in the chassis slide. Two machine screws are threaded into the chassis frame to anchor the board securely.

Mounted on the board are the components involved in the central processing activities of the personal computer. The primary operating component is the Intel 8088-2 16-bit microprocessor. This powerful integrated circuit oversees and directs virtually all operations occurring throughout the personal computer.

Along with the 8088-2, a number of other major components occupy the processor board:

- VLSI clock generator
- 8259A interrupt controller
- 8288 bus controller

Mounted near the VLSI clock is a trimmer adjustment. With this the clock can be adjusted precisely to its normal operating frequency of 4.7727MHz. This is necessary for proper operation of composite color monitors and RF modulators used with color television sets.

Overall power to the board is supplied through a 12-pin, in-line connector mounted on the board near the CPU integrated packages. Principal components in the middle part of the board include the following:

- 8237A direct memory access (DMA) controller
- 2 read-only memory (ROM) sockets, one used for the 16K BIOS, and the other reserved for future expansion
- 8253 timer
- 8250 serial UART

Also on the board are a number of connectors for the following devices:

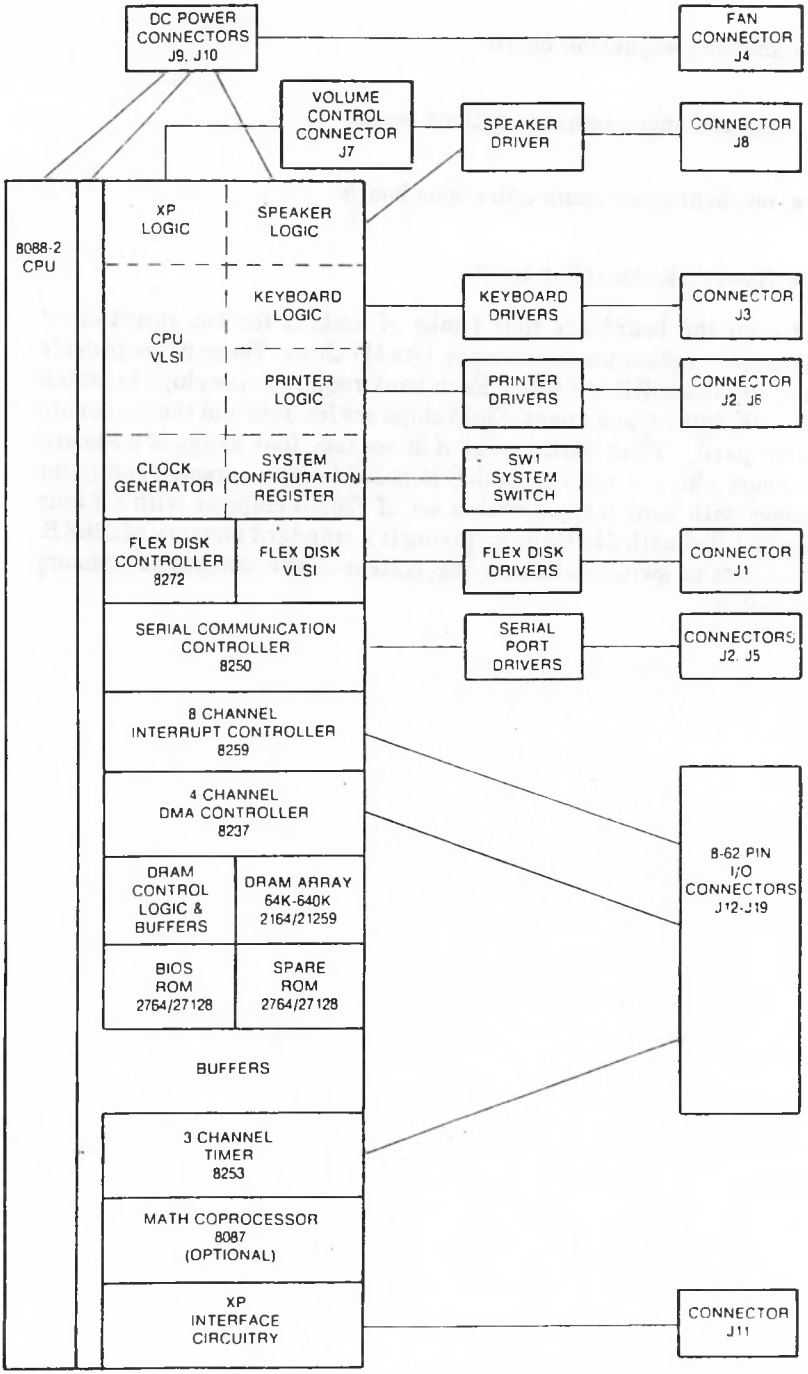
- serial peripheral (RS 232C) — 34-pin header connector
- parallel (Centronics) peripheral — 26-pin header connector
- keyboard — 5-pin, DIN, female connector

To the left of the RAM chip area of the board are eight 62-pin board-edge connectors. These are used for the expansion and enhancement of various board functions such as:

- color display/graphics board
- monochrome display board

- memory expansion board
- asynchronous communications board
- bisynchronous communications board
- fixed disk controller board

Also on the board are four banks of sockets for the insertion of dynamic random access memory (RAM) chips. These chips provide memory of 256KB or 640KB. Each bank requires nine chips to match the 64K byte arrangement. Eight chips are for data and the ninth chip is for parity. Thus, with a total of 36 sockets, four banks of on-board memory chips, a total of 640KB is possible. The personal computer comes with bank 0 filled with a set of 256KB chips or with all four banks filled with 64KB chips , giving it a standard memory of 256KB. Two sets of switches inform the system of the amount of memory installed.



Main Processor Board Block Diagram

FUNCTIONAL DESCRIPTION

The main processor board consists of five main functional areas as determined by the functions of the major components. These various sections operate as follows:

- MAIN PROCESSOR BOARD and SUPPORT COMPONENTS Board Sector 1

  This section processes and controls all data entering and leaving the PC by means of the 8088-2 main central processor unit (CPU) and other special purpose integrated circuits.

- CONFIGURATION SWITCHES Board Sector 2

  These two switches are set to indicate to the main processor board the current parameters of the system, such as memory capacity, type of peripherals attached, etc.

- RAM Board Sector 3

  This segment provides on-board memory storage through 36 64k-by-1 bit dynamic RAM chips, both soldered and pluggable. There are thirtytwo (32) chips for data and four (4) chips for parity.

- EXPANSION SLOTS Board Sector 4

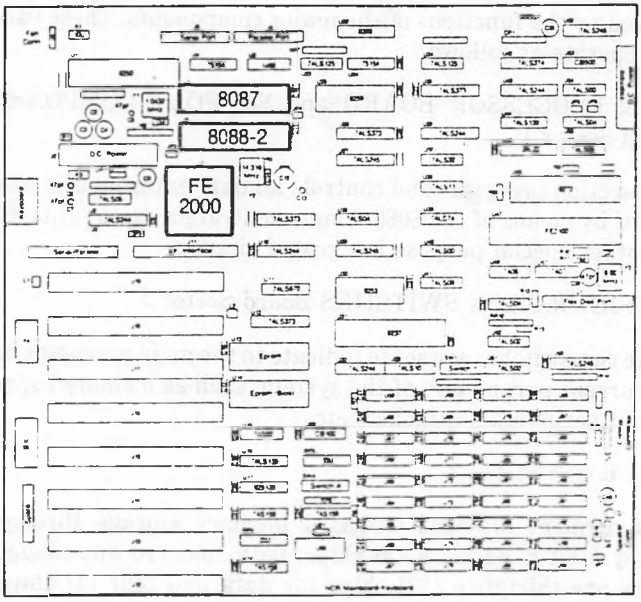
  Eight 62-pin slots furnish the physical interface for special-purpose boards providing memory expansion, added graphics capability, and other system enhancements.

- CONNECTORS Board Sector 5

  Various in-line, DIN, and multiple pin connectors provide the physical link between the board and the several peripheral devices.

Detailed descriptions of the operation and interrelationships of the major functional areas are contained in the following pages.

Main Processor Board Sector 1



The Intel 8088-2 is a microprocessor with 16-bit internal architecture and an 8-bit data bus interface. The 8088-2 has the ability to directly address up to one megabyte of memory.

Operational speed and efficiency are enhanced by the addition of pipelined architecture. This arrangement frees the execution unit of the 8088-2 from actually fetching data. Between the execution hardware and the system bus is a bus interface unit. This unit continues to obtain instructions while the execution unit carries out commands already fetched. The resultant increase in operational speed from the standard fetch-execute-fetch-execute sequence is considerable. Moreover, the system bus can be used more fully.

There are 14 register sets in the 8088-2, each of which is 16-bits. The total of 14 includes 4-stack arrangements for both data and segment registers and 2-stack arrangements for index, pointer, and control registers. The upper and lower halves of the data registers are separately addressable. Consequently, each data stack can serve either as a single 16-bit register or as two 8-bit registers.

Flag registers and instruction pointers are included in the control registers. Operating in conjunction with the 8088-2 pipelined archi-

tecture, these registers have specialized functions. The instruction pointer indicates the next instruction to be fetched, not the next instruction to be executed as in other microprocessors. The flag register displays codes that indicate the results of operations performed by the arithmetic-logic unit in the 8088-2.

The board has provision for the operation of an extra-performance (XP) feature which allows operation at 8.000 MHz. The 8.000 MHz mode is selected by a switch mounted on the front of the computer, labeled "XP". The interface is a 40-pin header for connection of the extra performance feature board to the main processor board. The extra performance feature hardware consists of a plug-in board which fits any of the expansion slots in the main processor board and a ribbon cable for the 40-pin interface connector. On some models the plug-in board is replaced by a chip mounted on the MPB thus freeing the slot for any other expansion board needed.

Addresses and Offset Format — The segment registers are used to determine the memory addresses. These are special-purpose registers related to the other registers. The segment registers are divided into code, stack, data, and extra segment. Specific combinations of these segments allow the 8088-2 to directly address up to 1 megabyte of memory simultaneously by offsetting the sections. Further control and enhancement of both on-board and external memory access is provided by the 8237 DMA (direct memory access) controller across four DMA channels.

8088-2 Interrupts — Interrupts in the 8088-2 can originate externally in peripheral devices or internally in software. Under certain conditions, the 8088-2 itself generates interrupt commands. Each interrupt is identified by a type code that directs the 8088-2 to the proper interrupt routine. These routines are stored by address in an interrupt vector table (capacity 256 addresses). Normal interrupts enter the 8088-2 as interrupt requests prioritized into eight levels by the 8259 controller. Under certain conditions, an NMI (non-maskable interrupt) is generated. This happens in situations such as loss of system power or memory parity error. NMIs have the highest priority and cannot be disabled.

8088-2 Maximum Mode — The 8088-2 has the added capability to function in the so-called maximum mode. This allows the microprocessor to operate in concert with special-purpose processor extensions, such as the 8087 numeric coprocessor. The use of processor extensions

allows sections of the 8088-2 previously dedicated to specific functions such as bus control or computation to be reassigned. As with the pipelined architecture, the result is greater processor speed and efficiency.

8259A Programmable Interrupt Controller — The PERSONAL COMPUTER PC6 is an interrupt-driven microcomputer. As previously mentioned, the 8088-2 CPU can operate on a number of interrupt levels and perform many interrupt routines. To manage the interrupts that may be occurring in the system at a given time, the main processor board is equipped with the 8259A programmable interrupt controller. This chip regulates up to eight levels of interrupt requests.

8288 Bus Controller — The flow of data along the I/O and system busses is controlled by the 8288 chip. Operating in conjunction with the 8088-2, this component generates command and control signals that direct the attention of the main processor board to the proper data at the proper time. The 8288 functions in either the I/O bus or system bus mode depending on the number of processors in a system.

8237A Programmable DMA Controller — The 8237A circuitry enables peripherals to transfer data directly to and from system memory, interrupt controller, main processor, and the control bus. Operating on four independent channels, the DMA controller can manage the transfer of blocks of data with minimal involvement from the main processor board.

The 8237A operates in either idle or active cycles. The controller is idle when there are no requests coming in on its f ur channels. Once a request is received, the 8237A begins to transfer memory in one of various transfer modes. These modes include:

- Single transfer
- Block transfer
- Demand transfer

Actual transfers within the modes are of three types: read, write, and verify. A read transfer shifts information from memory to an I/O device while a write transfer drives data from an I/O device into memory. The verify operation serves as a check on the transfer function. As an added functional feature, the 8237A can perform memory-to-memory transfers.

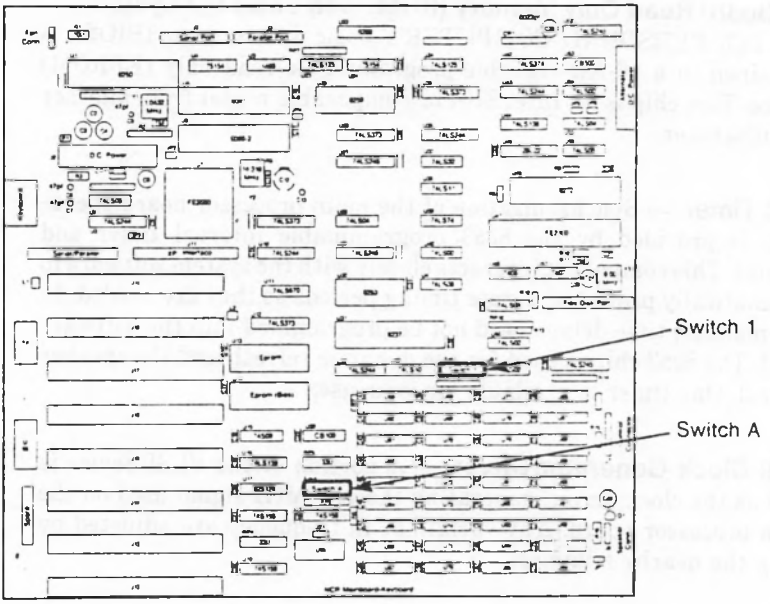
On-Board Read Only Memory (ROM) with Basic I/O System — The PC6 PERSONAL COMPUTER's basic I/O system (BIOS) is contained in a 16-KB erasable-programmable read only (EPROM) device. This chip is an Intel 2764 or comparable model from another manufacturer.

8253 Timer — Synchronization of the main processor board operations is provided by the 8253 programmable interval timer and counter. This component interacts closely with the system software to automatically provide accurate timing periods as they are needed. In this manner, time delays need not be programmed into the software itself. The 8253 chip is used for the dynamic refresh and the speaker control. One timer is available for your use.

VLSI Clock Generator/Driver — A portion of the VLSI device is used as the clock driver, generating the 4.77 MHz signal used on the main processor board. Any variations in frequency are adjusted by using the nearby trimmer.

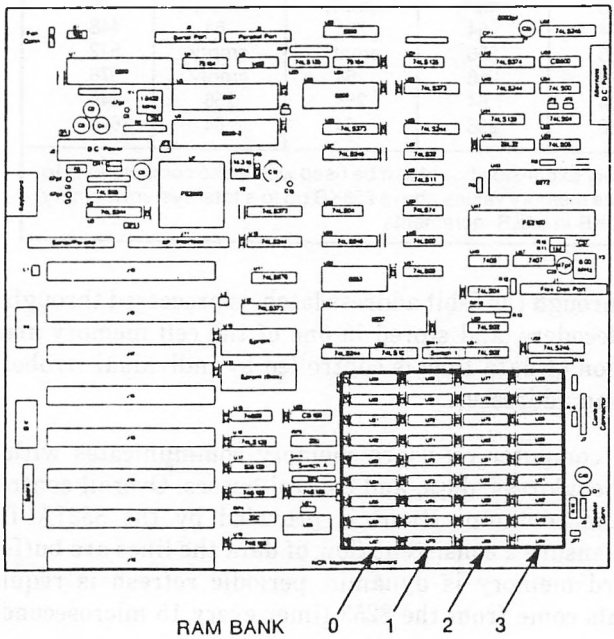
Configuration Switches Board Sector 2

There are two system configuration switches mounted on the main processor board . Switches 1 and 2 are 8-position. The positions of the various switches define the configuration of the system. Different combinations are set depending on the number and kind of peripherals attached, the amount of memory available, and other system parameters.



The switches are port addressed and their positions are read as input by the 8088-2. The various switch-selectable settings are listed in the "Software Considerations" section in this chapter and in Appendix C.

Main Processor Board Sector 3 RAM



On-board RAM Sector 3

The random access memory (RAM) on the main processor board is furnished by four banks of 64K by 1 byte or one bank of 256K by 1 byte dynamic RAM (DRAM) chips. Each bank consists of nine chips, eight chips for data, one for parity. Standard memory capacity of the personal computer loads 4 banks each with 64KB for a total of 256 KB. (Some models load 256KB chips in only one bank as the initial standard configuration of on-board memory.) Filling the four banks in the arrangement shown in the chart below will provide a maximum of 640KB of on-board memory. The arrangements shown below are the only allowable configurations.

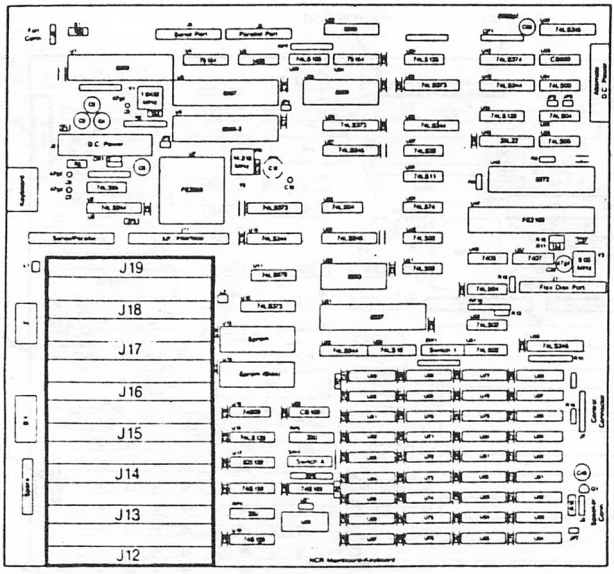
Bank 0	Bank 1	Bank 2	Bank 3	Total
64	64	64	64	256 *
256	empty	empty	empty	256 *
64	64	256	64	448
256	256	empty	empty	512
256	256	64	empty	576
64	64	256	256	640
256	256	64	64	640

* Memory expansion board can be used with these combinations to provide memory values above 256KB up to a total system memory of 640KB in 64KB increments.

Data enters through the 8-bit address latch, is processed through row and column decoders, and stored in one of the cell memory arrays. Synchronization of data flow is controlled by individual strobes for row and column addresses.

The personal computer on-board memory communicates with the 8088-2 over the address, data, and control busses. Overall control of these lines and communications is provided by the 8327A DMA controller. To ensure a consistent flow of data the lines are buffered. Since on-board memory is dynamic, periodic refresh is required. Refresh signals come from the 8253 timer every 15 microseconds.

Expansion Slots Board Sector 4

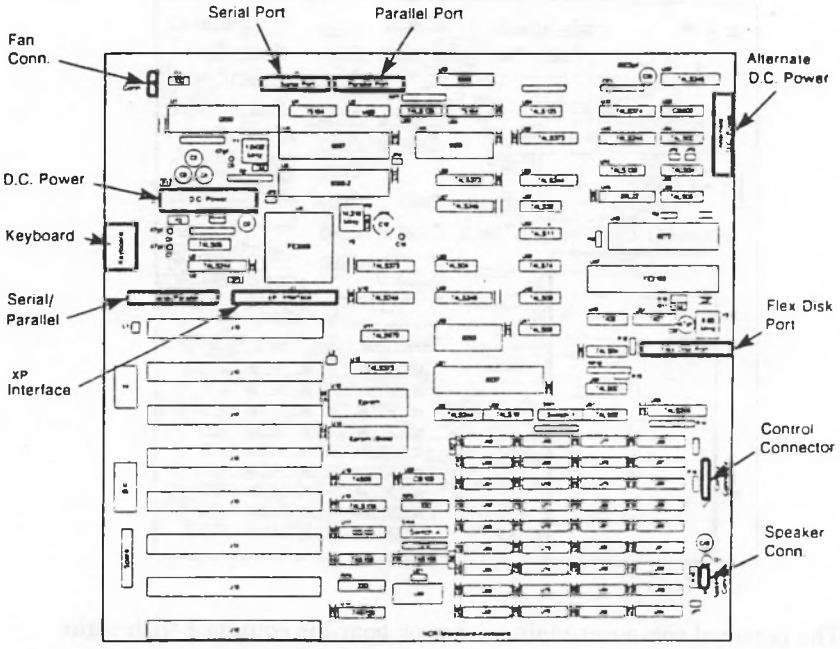


The personal computer main processor board is equipped with eight 62-pin slots designed to mate with compatible board-edge connectors. Optional special-function boards for memory expansion, color/graphics, and other system enhancements slide directly into these slots. The slots themselves are connected to system busses to route data to and from the proper on-board components, including the 8288 bus controller, 8259A interrupt controller, various address and data buffers, and the 8088-2 CPU.

Any system expansion board installed in the personal computer communicates with the 8088-2 over the 62 lines of the expansion slot I/O channel. There are lines for address, data, and control. All lines are buffered and operate in parallel. Any board can be plugged into any open slot except two. The available space for the boards in those positions is slightly shorter than that of the rest of the positions. Eight lines are dedicated to various levels of electrical power and ground. An additional eight lines service the 8-bit data bus.

Twenty lines are used for addressing purposes. For memory, all twenty lines are used; for I/O devices, nine lines are used. Up to 512 different I/O devices can be addressed over these nine lines. The expansion cards are secured by means of a small metal tang on one

corner. This tang is fastened to the corresponding board support arm by a hex head slotted screw.



Connectors Board Sector 5

Serial Communications — The serial connector is a 34-pin header connector on the main processor board which is connected by a ribbon cable to a DB-25 male plug mounted on the housing of the computer. It follows the RS 232C industry standard. The 8250 asynchronous communications interface is the on-board controller for this connector. Any device communicating serially with the personal computer is attached at this connector. The "Internal Asynchronous Communications Interface" section contains additional information describing 8250 serial communication.

Parallel Communications — The parallel connector is a 26-pin header connector on the main processor board. It is connected by a ribbon cable to a DB-25 female connector mounted on the housing of the computer providing the physical link between the on-board parallel (Centronics) interface and external parallel devices. Further details on the operation of parallel communications on the system board are given in the "Internal Centronics Interface" section of this chapter.

Keyboard Communications — The personal computer keyboard cable attaches to the main processor board at the 5-pin DIN female plug which is mounted at a right angle to the board and is accessed through a hole in the computer housing. Signals from the keyboard enter the main processor board at this point, are encoded or decoded through keyboard logic, bussed to the appropriate controller chip (for example, the 8259A interrupt controller), and then to the main processor board .

OPERATING CHARACTERISTICS

The capacities and ranges of the major components on the main processor board are outlined in the following pages.

Intel 8088-2 Microprocessor

- N-channel, silicon gate, NMOS construction
- 16-bit on-board architecture/8-bit data bus interface
- Direct addressing to 1 Megabyte of memory
- 16-bit stacked registers
- Total of 24 operand addressing modes
- 8-bit and 16-bit arithmetic
  - Binary and decimal
  - Signed and unsigned
- 4.77MHz clock rate
- Input voltage: .5V low; 2V high
- Power supply current: 340mA
- Clock cycle: 200 ns

8259A Programmable Interrupt Controller

- Standard levels of priority: 8
- Expandable levels of priority: 64

- NMOS construction
- Input voltage: .5V low; 2V high
- Input current: 85mA
- Duration of interrupt acknowledge cycle: 160 ns

8288 Bus Controller

- Bipolar bus driving capability
- 3 status lines
- Input voltage: .8V low; 2V high
- Supply current: 230mA
- Duration of clock cycle: 100 ns minimum
- Power consumption: 1.5W

8237A Programmable DMA Controller

- 4 independent channels
- Designed for use with an external 8-bit address register
- 64K address and word capacity on each channel
- Input voltage: .8V low; 2V high
- Duration of clock cycle: 210 ns
- Duration of DMA transfer: five 210 ns clock cycles

2764 EPROM — 16K Byte Capacity BIOS

- Access time: 350 ns maximum
- Power consumption: 525mW maximum
- Input voltage: .8V low; 2V high

8284A Clock Generator and Driver

- Crystal frequency: 14.31818 MHz
- Counter: divide by 3
- Duty cycle: 33%
- Input voltage: .8V low; 2V high
- Duration of clock cycle: 125 ns

2164 DRAM On-Board Memory

- N-channel, HMOS construction
- 64K by 1 bit format
- Input voltage: 0.8V low; 2V high
- Access time: 200 ns maximum
- Duration of read, write cycle: 300 ns
- Duration of read, modify, write cycle: 345 ns
- Power consumption: 1W

Expansion Slots (8 Available)

- 62-pin design
- Lines for:
  - Power
  - Address
  - Data
  - Control
- Compatible with:

- NCR expansion boards
- Other manufacturers' expansion boards

Parallel Communications (Centronics) Connector

- DB-25 female connector on computer housing
- 34-pin header connector on main processor board
- Operates on industry standard signals

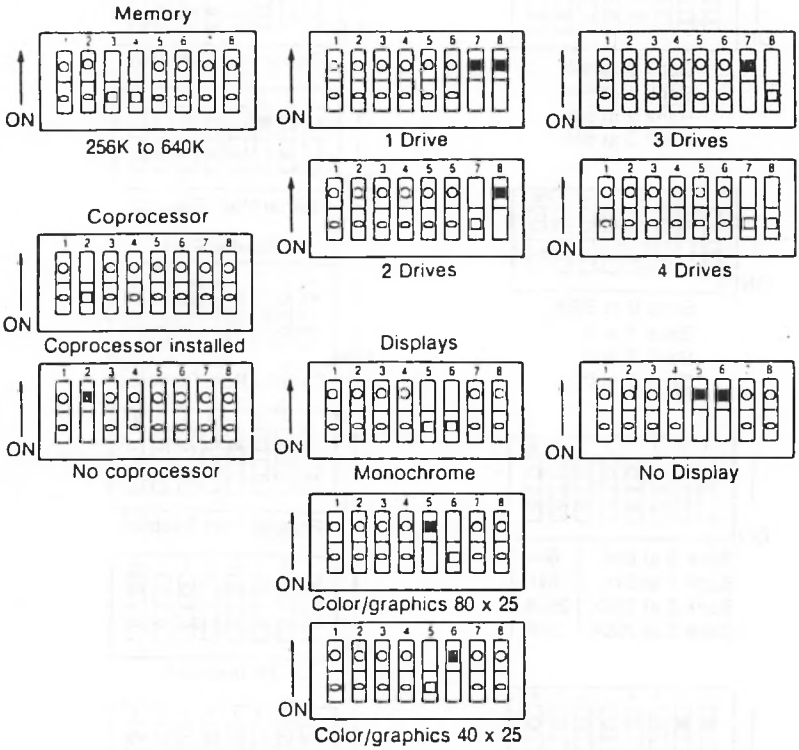
Serial Communications (RS 232C) Connector

- DB-25 male connector
- 34-pin header connector on main processor board
- Baud range
  - 50 baud minimum
  - 19.2K baud maximum

SOFTWARE CONSIDERATIONS

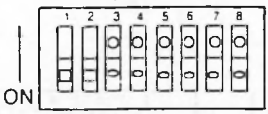
The NCR Personal Computer can be configured in many ways. The presence of peripheral devices, expansion boards, and other system enhancements must be made known to the main processor board. This information is provided through the configuration switches. The following pages list the switch settings for all possible system configurations on the standard PERSONAL COMPUTER PC6 followed by other helpful software-related information.

Switch Number 1 Settings

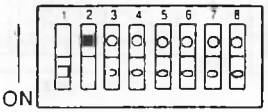


Switch Number A Settings

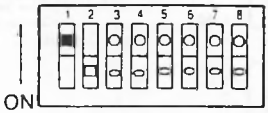
Memory Bank Options



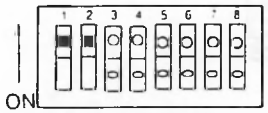
Bank 0 at 64K
Bank 1 at 64K
Bank 2 at 64K
Bank 3 at 64K



Bank 0 at 256K
Bank 1 at 0
Bank 2 at 0
Bank 3 at 0

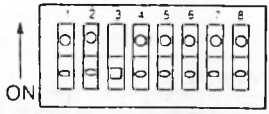


Bank 0 at 64K	64K	
Bank 1 at 64K	64K	
Bank 2 at 256K	256K	
Bank 3 at 256K	64K	

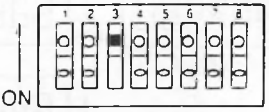


Bank 0 at 256K	256K	256K
Bank 1 at 256K	256K	256K
Bank 2 at 64K	64K	0
Bank 3 at 64K	0	0

Serial Port

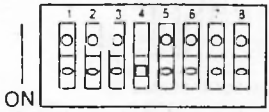


Serial Port Disabled

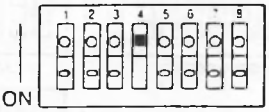


Serial Port Enabled

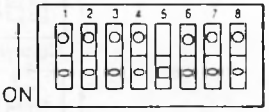
Parallel Port



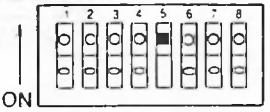
Parallel Port Disabled



Parallel Port Enabled



XP Installed



XP Not Installed

* A Memory Expansion Board can be used with these settings.

System Memory Address Ranges

The table below provides the address ranges for various amounts of system memory.

Start Address		Function
Decimal	Hex	
0	00000	128 to 256 KB Read/Write Memory on System Board
128 KB	20000	
192 KB	30000	
256 KB	40000	
320 KB	50000	Up to 384 KB Read/Write Memory in I/O Channel
384 KB	60000	
448 KB	70000	
512 KB	80000	
576 KB	90000	
640 KB	A0000	
656 KB	A4000	128 KB Reserved
672 KB	A8000	
688 KB	AC000	
704 KB	B0000	Monochrome
720 KB	B4000	
736 KB	B8000	Color/Graphics
752 KB	BC000	
768 KB	C0000	192 KB Read Only Memory Expansion and Control
784 KB	C4000	
800 KB	C8000	Fixed Disk Control
816 KB	CC000	
832 KB	D0000	
848 KB	D4000	
864 KB	D8000	
880 KB	DC000	
896 KB	E0000	
912 KB	E4000	
928 KB	E8000	
944 KB	EC000	
960 KB	F0000	Reserved
976 KB	F4000	48 KB Base System ROM
992 KB	F8000	
1008 KB	FC000	

System Configuration Address Ranges

The following table provides the hexadecimal address ranges for various personal computer system configurations.

I/O ADDRESS MAP *

ADDRESS (HEX)	DEVICE (MAIN PROCESSOR BOARD)
000-00F	DMA (8237A-5)
020-021	INTERRUPTS (8259A)
040-043	TIMER (8253A)
060-063	PIO (8255A-5)
080-083	DMA PAGE REGISTERS
0A0	NMI ENABLE REGISTERS
2F8-2FF	SERIAL PORT RS-232 COMM2
378-37F	PARALLEL PORT
3F8-3FF	SERIAL PORT RS-232 COMM1

ADDRESS (HEX)	DEVICE (IN EXPANSION BUS)
3B0-3BF	MONOCHROME DISPLAY ADAPTER CARD
3D0-3DF	COLOR/GRAPHICS DISPLAY ADAPTER CARD
3F0-3F7	FLEXIBLE DISK ADAPTER CARD

* 768 device locations maximum

The CPU controller accepts Read/Write commands initiated by the processor.

Write PIO Control Register

PIO CS	A1	A0	IOW
0	0	1	0

D0 = +Gate speaker
D1 = +Speaker data
D2 = Select system configuration switch 2 low bits
D3 = N/A
D4 = -Enable RAM parity
D5 = -Enable I/O check
D6 = +Enable keyboard clock
D7 = +Clear keyboard

Write Switch Register

PIO CS	A1	A0	IOW
0	1	0	0

D0 = Not used
D1 = +8087 installed
D2, D3 = System memory
D4 = Display configuration Jumper 1 (DISP 1)
D5 = Display configuration Jumper 2 (DISP 2)
D6, D7 = Number of floppies.

Write PIO Configuration Lock Register:

PIO CS	A1	A0	IOW
0	1	1	0

D0 = -Enable parity
D1 = +8087 installed
D2 thru D4 = Not used
D5 = +Lock system switch register
D6, D7 = Not used

Read PIO Control Register

PiO CS	A1	A0	IOR
0	0	1	0

Read Switch Register

PIO CS	A1	A0	IOR
0	1	0	0

D0-D3 depends on PIO control register Bit 2
When PIO control register Bit 2 = 1
D0 = Not used
D1 = +8087 installed
D2, D3 = System memory

When PIO control register Bit 2 = 0
D0 = Display configuration Jumper 1
D1 = Display configuration Jumper 2
D2, D3 = Number of floppies

D4 = +Timer 2 terminal count
D5 = +Timer 2 terminal count
D6 = +I/O CH check
D7 = +PTY check

Printer Port Programming

PRINT CS	A1	A0	IOR	IOW	OPERATION
0	0	0	0	1	Read back printer data port
0	0	0	1	0	Write printer data port
0	0	1	0	1	Read printer status
0	0	1	1	0	N/A
0	1	0	0	1	Read back printer control port
0	1	0	1	0	Write printer control port
0	1	1	0	1	N.C.
0	1	1	1	0	N.C.

Read Printer Status Port Data Bit Definition:

D0 thru D2 not used
D3 = -Error
D4 = +SLCT
D5 = +Paper empty
D6 = -ACK
D7 = +Busy

Write Printer Control Port Data Bit Definition

D0 = Strobe
D1 = -Auto FDXT
D2 = +Init
D3 = -SCLT in
D4 = +Printer interrupt enable

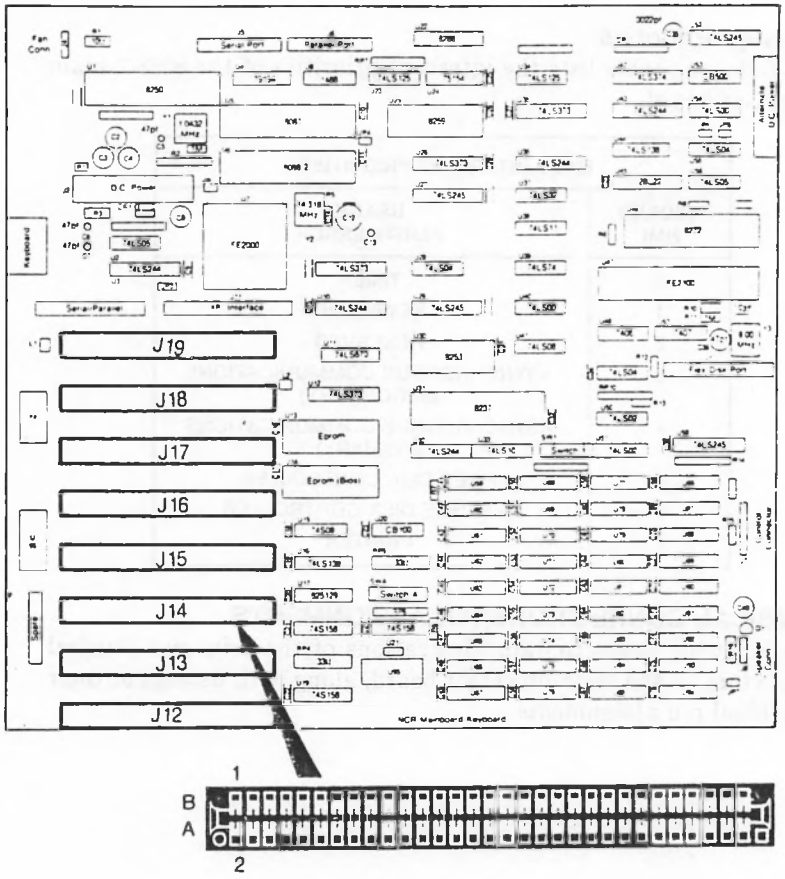
Interrupt Priorities

The following table lists the interrupt priorities of the 8088-2 main processor board.

8088-2 INTERRUPT PRIORITIES	
PRIORITY NMI	USAGE PARITY ERROR
0	TIMER
1	KEYBOARD
2	RESERVED
3	ASYNCHRONOUS COMMUNICATIONS (SECONDARY)
4	ASYNCHRONOUS COMMUNICATIONS (PRIMARY)
5	FIXED DISK CONTROLLER
6	FLEXIBLE DISK CONTROLLER
7	PRINTER

PHYSICAL CONNECTIONS/PIN ASSIGNMENTS

The following pages contain illustrations of the principal physical connectors on the main processor board, along with listings of their individual pin assignments.



Main processor board-expansion slots

Expansion Slot Pin Assignments

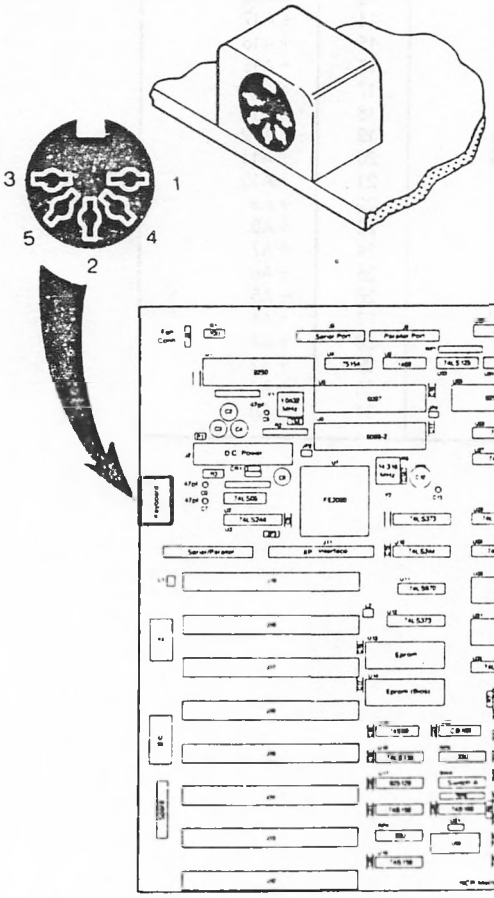
B	FUNCTION	A	FUNCTION
1	GND	1	- I/O CHECK
2	+RESET DRIVE	2	+D7
3	+5V	3	+D6
4	IRQ2	4	+D5
5	- 5V	5	+D4
6	+DRQ2	6	+D3
7	- 12V	7	+D2
8	- HRQ I/O	8	+D1
9	+12V	9	+D0
10	GND	10	+I/O CH RDY
11	- MEMW	11	+BAEN
12	- MEMR	12	+A19
13	- IOW	13	+A18
14	- IOR	14	+A17
15	- DACK3	15	+A16
16	+DRQ3	16	+A15
17	- DACK1	17	+A14
18	+DRQ1	18	+A13
19	- BDACK0	19	+A12
20	+BCLOCK	20	+A11
21	+IRQ7	21	+A10
22	+IRQ6	22	+A9
23	+IRQ5	23	+A8
24	+IRQ4	24	+A7
25	+IRQ3	25	+A6
26	- DACK3	26	+A5
27	+T/C	27	+A4
28	+ALE	28	+A3
29	+5V	29	+A2
30	+OSC	30	+A1
31	GND	31	+A0

- Asserts low
+ Asserts high

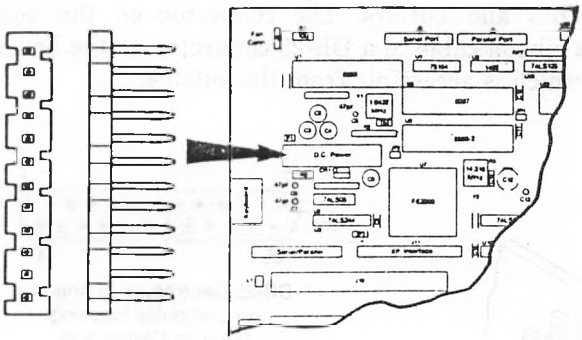
Main Processor Board Keyboard Connector Pin Assignments

	Pin	Function	
PC	1	+Clock	Keyboard
	2	+Data	
	3	-Reset	
	4	GND	
	5	+5V	

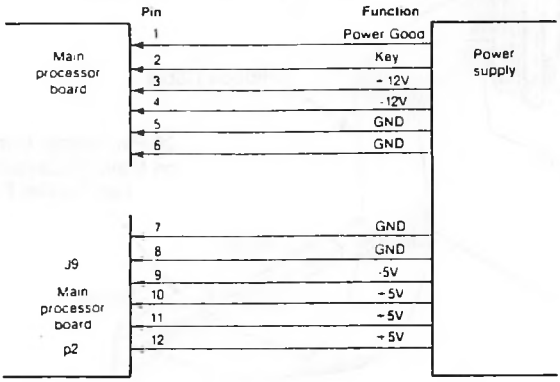
Keyboard Interface Signals



Main Processor Board Power Connector



Main Processor Board DC Power Connector



DC Power Cable Voltages

ON-BOARD CENTRONICS INTERFACE

The on-board Centronics interface provides a parallel port for the attachment of an external input/output device. The interface provides eight TTL-buffered data lines, four TTL-buffered control lines, and five steady-state status lines. The interface, under processor control, performs three operations:

- Writes data to attached device
- Reads data from attached device
- Reads status of attached device

The interface is the default printer port unless changed by the software.

Physical Description

The on-board Centronics interface (physically part of the main processor board) is comprised of a 26-pin header connector and additional latches and buffers. The connector on the board is connected by a ribbon cable to a DB-25 connector on the housing of the computer which is accessible from the outside.

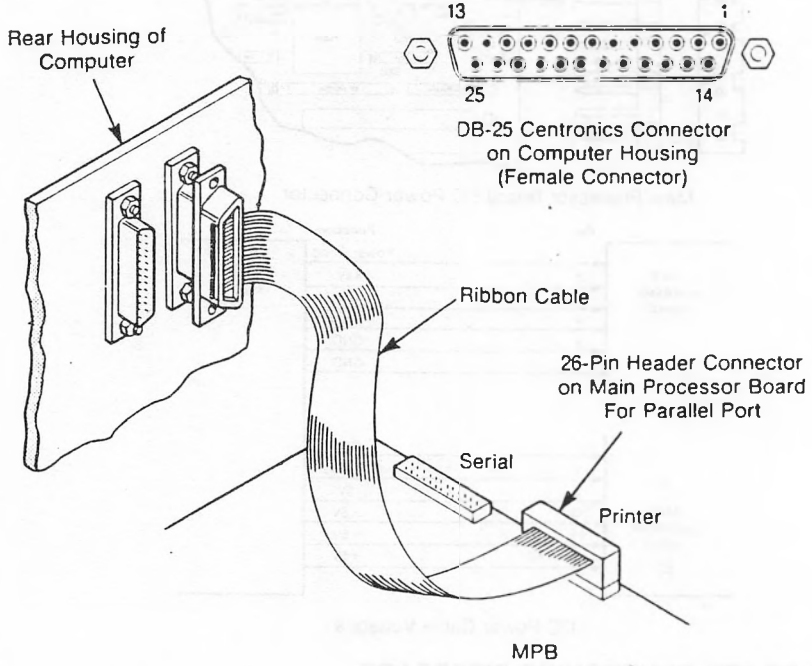
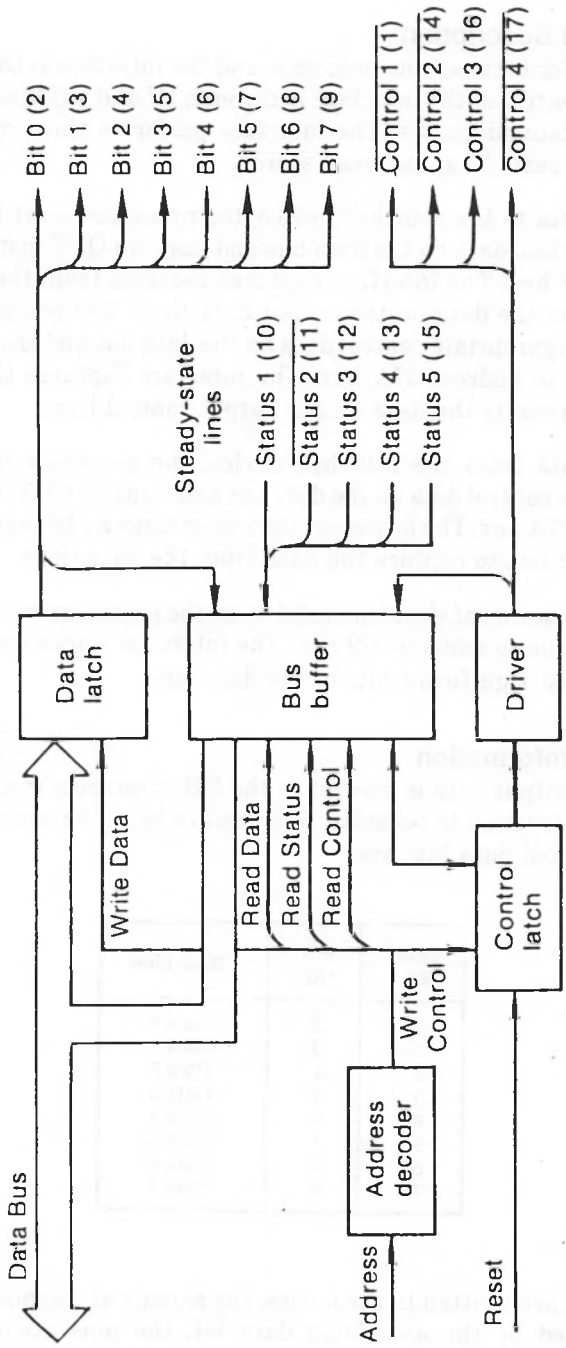


Chart of pin assignments is shown on page 1-37.



On-Board Centronics Interface Block Diagram

Functional Description

Data transfer between the processor and the interface is through the data bus; control of the interface is through IN and OUT instructions to appropriate addresses. The interface performs three operations: write data, read data, and read status.

To write data to the attached device, the processor must first place the appropriate data on the data bus and issue an OUT instruction to address 378 hex. The interface captures the data from the data bus and presents the data on the output data lines. The processor must then place appropriate control data on the data bus and issue an OUT instruction to address 37A hex. The interface captures the control data and presents the data on the output control lines.

To read data from the attached device, the processor must place appropriate control data on the data bus and issue an OUT instruction to address 37A hex. The processor then must issue an IN instruction to address 378 hex to capture the data from the data lines.

To read the status of the attached device, the processor must issue an IN instruction to address 379 hex. The interface places the status in the five most significant bits of the data bus.

Software Information

Input and output data is present at the DB-25 connector when an IN or OUT instruction is issued at address 378 hex. The connector pins and associated data bits are:

Date Bit	Pin No.	Data Line
0	2	Data 0
1	3	Data 1
2	4	Data 2
3	5	Data 3
4	6	Data 4
5	7	Data 5
6	8	Data 6
7	9	Data 7

When data are written to the device, the signals at the pins go to the level defined by the associated data bit; the pins are capable of sourcing 2.6mA and sinking 24mA. When data are read from the device, the resulting data are presented to the data bus.

The control data are presented to four pins of the DB-25 connector. The connector pins and the associated data bus bits are shown in the following illustration:

Data Bit	Pin No.	Control Line
0	1	Control 1
1	14	Control 2
2	16	Control 3
3	17	Control 4

These pins are driven by open-collector drives that pull to +5 VDC through 4.7K-ohm resistors. The pins can sink approximately 7mA and maintain 0.8 volts down-level.

NOTE: The control port drivers invert the signals on pins 1, 14, and 17. Also, the status bit 7 signal on pin 11 is inverted.

If the interface is being used to attach a printer to the processor, the control data are:

- Pin 1 STROBE
- Pin 14 AUTO FEED
- Pin 16 INITIALIZE
- Pin 17 SELECT INPUT

The status data are present at five pins on the DB-25 connector. The connector pins and the data bus bits associated with the pins are shown in the following illustration.

Data Bit	Pin No.	Status Line
3	15	Status 1
4	13	Status 2
5	12	Status 3
6	10	Status 4
7	11	Status 5

These pins are capable of sourcing 2.6mA and sinking 24mA.

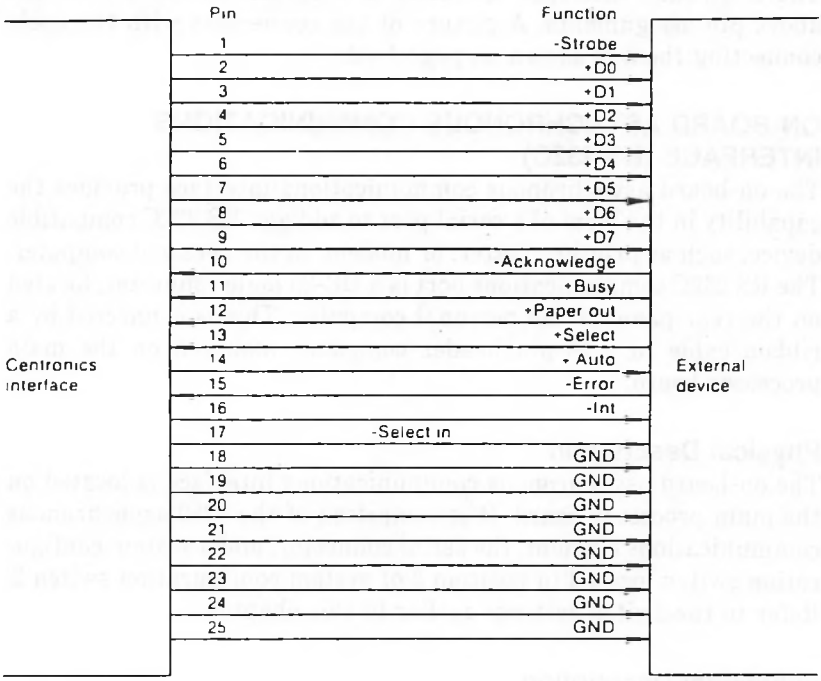
If the interface is being used to attach a printer to the processor, the status lines indicate the following realtime status:

- Pin 15 ERROR
- Pin 13 SELECT
- Pin 12 PE (Out of Paper)
- Pin 11 BUSY
- Pin 10 ACK

If data bit 4 is set to 1 by the processor and the processor issues an OUT instruction to address 37A (hex), the interface interrupts the processor if pin 10 (status 1) goes from high to low.

Physical Connections/Pin Assignments

The pin assignments of the DB-25 connector are shown in the following illustration.


Pin
Function
1 -Strobe
2 +D0
3 +D1
4 +D2
5 +D3
6 +D4
7 +D5
8 +D6
9 +D7
10 -Acknowledge
11 +Busy
12 +Paper out
13 +Select
14 - Auto
15 -Error
16 -Int
17 -Select in
18 GND
19 GND
20 GND
21 GND
22 GND
23 GND
24 GND
25 GND
Centronics interface
External device

The Centronics interface connector is a header connector with the above pin assignments. A picture of the connectors with the cable connecting them is shown on page 1-32.

ON-BOARD ASYNCHRONOUS COMMUNICATIONS INTERFACE (RS 232C)

The on-board asynchronous communications interface provides the capability in the form of a serial port to add any RS 232C compatible device, such as printer, plotter, or modem, to the personal computer. The RS 232C communications port is a DB-25 male connector, located on the rear panel of the personal computer. This is connected by a ribbon cable to a 34-pin header connector mounted on the main processor board.

Physical Description

The on-board asynchronous communications interface is located on the main processor board. It is comprised of the 8250 asynchronous communications element, the serial connector, and a system configuration switch located in position 3 of system configuration switch 2. Refer to the switch settings earlier in this chapter.

Functional Description

This section provides an explanation of the functional characteristics of the on-board asynchronous communications interface.

Features — The on-board asynchronous communications adapter uses an 8250 40-pin asynchronous communication element with the following features:

- Full double buffering
- Independently-controlled interrupt
- Programmable baud rate generator
- Fully-programmable serial interface characteristics:
  - 5, 6, 7, or 8-bit characters
  - Even, odd, or no parity
  - 1, 1-1/2, or 2 stop bit generation

- False start bit detector
- Status reporting
- Tri-state TTL drive capabilities for bidirectional data bus and control bus
- Line break generation/detection
- Internal diagnostic capabilities
- Fully prioritized interrupt system controls
- Independent receiver clock input

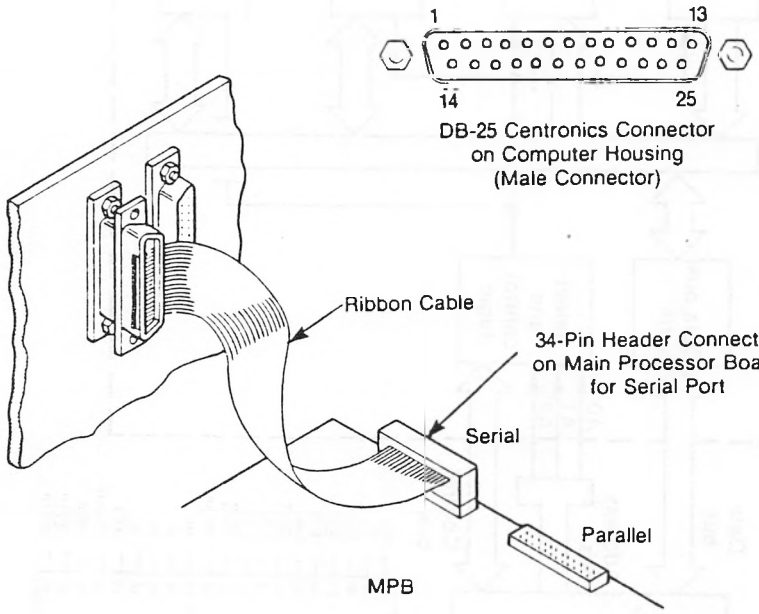
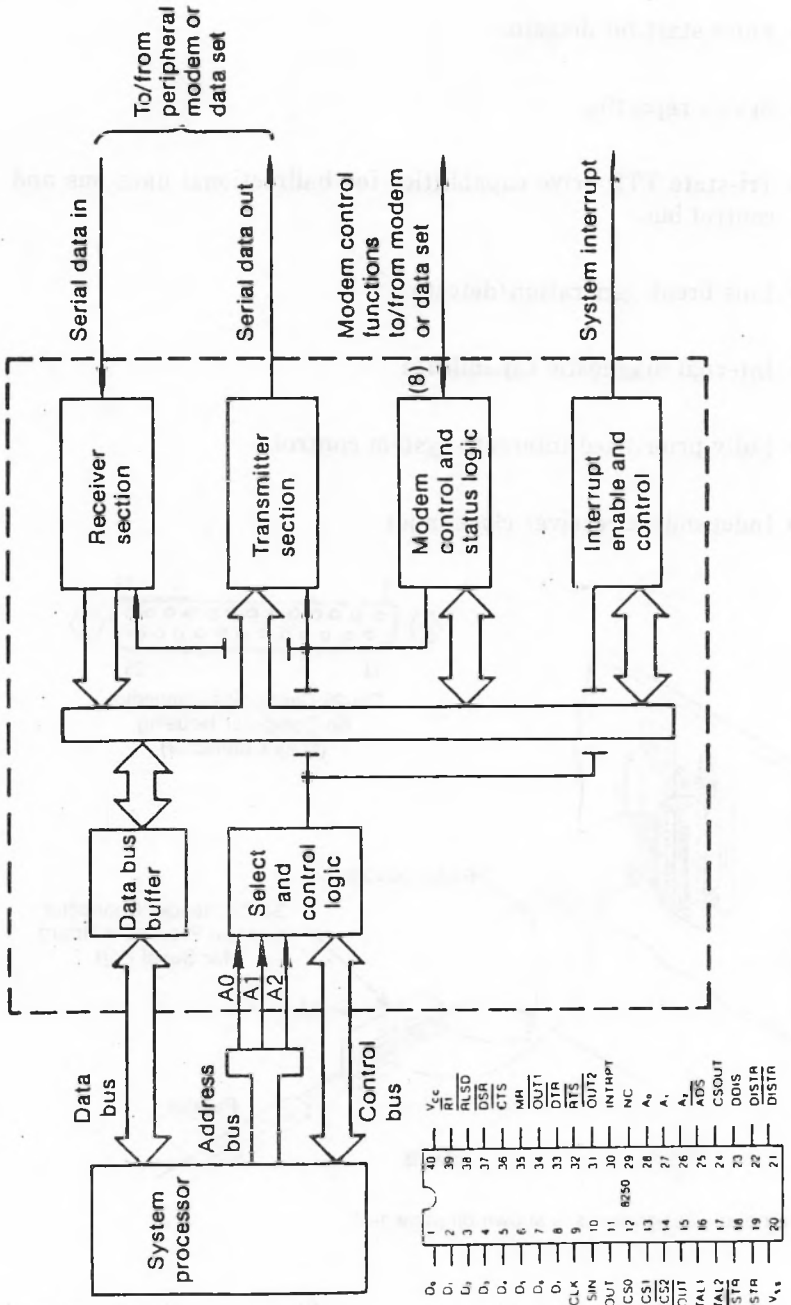


Chart of pin assignments is shown on page 1-41.

The block diagram on the next page illustrates the functional characteristics of the on-board asynchronous communications interface:



On-Board Asynchronous Communications Adapter (RS 232C) and 8250 Signals

Physical Connections/Pin Assignments

The following figure illustrates the location of the RS 232C communications port (on-board asynchronous) and the pin assignments for the connectors.

On board asynchronous communications adapter (RS-232C)

Pin	Function
1	Ground
2	Transmitted data
3	Received data
4	Request to send
5	Clear to send
6	Data set ready
7	Signal ground
8	Received line signal detector
9	NC
10	NC
11	NC
12	NC
13	NC
14	NC
15	NC
16	NC
17	NC
18	NC
19	NC
20	Data terminal ready
21	NC
22	Ring indicator
23	NC
24	NC
25	NC

External device

Operating Configurations — The 8250 converts parallel data to serial on the transmit side and serial to parallel on the receive side.

Various operating configurations can be selected by setting the Com1 (hex 3F8 through 3FF) or Com2 (hex 2F8 through 2FF) configuration switches, and writing data to the 8250.

These configurations are defined by various registers that are selected by address bit A0, A1, A2, and the Divisor Latch Access bit (DLAB), bit 7 of the Line Control Register. The following figure defines the register selection used in the 8250.

Port Hex Addr.		DLAB	A0	A1	A2	Register
Comm1	Comm2					
3F8	2F8	0	0	0	0	Receiver Buffer (Read), Transmitter Holding Register (Write)
3F9	2F9	0	1	0	0	Interrupt Enable
3FA	2FA	X	0	1	0	Interrupt Identification (Read Only)
3FB	2FB	X	1	1	0	Line Control
3FC	2FC	X	0	0	1	Modem Control
3FD	2FD	X	1	0	1	Line Status
3FE	2FE	X	0	1	1	Modem Control Status
3FF	2FF	X	1	1	1	Not Used
3F8	2F8	1	0	0	0	Divisor Latch (Least Signigicant Bit)
3F9	2F9	1	1	0	0	Divisor Latch (Most Significant Bit)

Software Information

The 8250 contains a programmable baud rate generator and several accessible registers. This section provides information on these software-controlled components.

Programmable Baud Rate Generator — The 8250 contains a programmable baud rate generator that has the capability of dividing the clock input (1.8432MHz) by any value from 1 through 2 to the 16th power minus 1. The divisor is stored in two 8-bit latches in a 16-bit binary format; these divisor latches must be loaded during initialization in order to ensure that the baud rate generator will operate properly. Whenever either of the 8-bit divisor latches is loaded, a 16-bit baud counter is also immediately loaded. The output frequency of the baud rate generator is 16 times the baud rate. The baud rate generator has maximum operating frequency of 3.1MHz; however,

the data rate should never exceed 19,200 baud. The following table illustrates baud rates up to 19,200 baud and the divisor required to generate each baud rate:

Desired Baud Rate	Divisor (16 x Clock) DLAB=1		
	Decimal Value	Hex Value	
		DLM Address 3F9	DLL Address 3F8
50	2304	09	00
75	1536	06	00
110	1047	04	17
134.5	857	03	59
150	768	03	00
300	384	01	80
600	192	00	00
1200	96	00	60
1800	64	00	40
2000	58	00	3A
2400	48	00	30
3600	32	00	20
4800	24	00	18
7200	16	00	10
9600	12	00	00
19.200	6	00	06

Accessible Registers — The 8250 contains a number of registers that may be accessed or controlled through the processor. These registers control 8250 operations and are also used to transmit and receive data. The following table summarizes the accessible registers in the 8250.

Table 2. Summary of ED8250 Accessible Registers

	Register Address									
	0 DLAB = 0	0 DLAB = 0	1 DLAB = 0	2	3	4	5	6	0DLAB = 1	1DLAB = 1
Bit No.	Receiver Buffer Register (Read Only)	Transmitter Holding Register (Write Only)	Interrupt Enable Register	Interrupt Identification Register	Line Control Register	MODEM Control Register	Line Status Register	MODEM Status Register	Divisor Latch (LS)	Divisor Latch (MS)
0	Data Bit 0*	Data Bit 0*	Enable Received Data Available Interrupt (ERBFI)	"0" if Interrupt Pending	Word Length Select Bit 0 (WLS0)	Data Terminal Ready (DTR)	Data Ready (DR)	Delta Clear to Send (DCTS)	Bit 0	Bit 8
1	Data Bit 1	Data Bit 1	Enable Transmitter Holding Register Empty Interrupt (ETBEI)	Interrupt ID Bit (0)	Word Length Select Bit 1 (WLS1)	Request to Send (RTS)	Overrun Error (OR)	Delta Data Set Ready (DDSR)	Bit 1	Bit 9
2	Data Bit 2	Data Bit 2	Enable Receiver Line Status Interrupt (ELSI)	Interrupt ID Bit (1)	Number of Stop Bits (STB)	Out 1	Parity Error (PE)	Trailing Edge Ring Indicator (TERI)	Bit 2	Bit 10

*Bit 0 is the least significant bit. It is the first bit serially transmitted or received.

Table 2. Summary of WD8250 Accessible Registers Cont.

	Register Address								
3	Data Bit 3	Data Bit 3	Enable MODEM Status Interrupt (EDSSI)	0	Parity Enable (PEN)	Out 2	Framing Error (FE)	Delta Receive Line Signal Detect (DSLSD)	Bit 3	Bit 11
4	Data Bit 4	Data Bit 4	0	0	Even Parity Select (EPS)	Loop	Break Interrupt (BI)	Clear to Send (CTS)	Bit 4	Bit 12
5	Data Bit 5	Data Bit 5	0	0	Stick Parity	0	Transmitter Holding Register Empty (THRE)	Data Set Ready (DSR)	Bit 5	Bit 13
6	Data Bit 6	Data Bit 6	0	0	Set Break	0	Transmitter Shift Register Empty (TSRE)	Ring Indicator (RI)	Bit 6	Bit 14
7	Data Bit 7	Data Bit 7	0	0	Divisor Latch Access Bit (DLAB)	0	0	Received Line Signal Detect (RLSD)	Bit 7	Bit 15

* Bit 0 is the lease significant bit. It is the first bit serially transmitted or received.

Line-Control Register (LCR) — The LCR contains the programmer-specified values for the format of the asynchronous communications exchange. The contents of this register may also be retrieved and checked; this eliminates the need for storing line characteristics in a separate system memory storage area. The following table defines the functions of the LCR bits.

<table>
<tr><th>Hex Address 3FB</th><th>Line Control Register (LCR)</th></tr>
<tr><th>Bit</th><th>Function/Explanation</th></tr>
<tr><td>0,1</td><td>Word length selection Specifies number of bits in each transmitted or receive serial character.
<table>
<tr><th>Bit 0</th><th>Bit 1</th><th>Word Length</th></tr>
<tr><td>0</td><td>0</td><td>5 Bits</td></tr>
<tr><td>1</td><td>0</td><td>6 Bits</td></tr>
<tr><td>0</td><td>1</td><td>7 Bits</td></tr>
<tr><td>1</td><td>1</td><td>8 Bits</td></tr>
</table></td></tr>
<tr><td>2</td><td>Number of Stop bits
<table>
<tr><th>Bit 2 Value</th><th>Word Length</th><th>Stop Bits</th></tr>
<tr><td>0</td><td>N/A</td><td>1</td></tr>
<tr><td>1</td><td>5 Bits</td><td>1-1/2</td></tr>
<tr><td>1</td><td>6, 7, or 8 Bits</td><td>2</td></tr>
</table></td></tr>
<tr><td>3</td><td>Parity enable If equal to 1, a parity bit will be generated or checked between the last data word bit and the stop bit(s). Sum of data word bits and parity bit equals odd or even number of 1's as specified in bit 4.</td></tr>
<tr><td>4</td><td>Even parity select. Bit 3 must be set equal to 1 for odd or even parity. Bit 4 equal to 0 selects odd parity; but 4 equal to 1 selects even parity.</td></tr>
<tr><td>5</td><td>Stick parity. Enabled only when bits 3 and 5 are set equal to 1. Parity bit is transmitted and received as 0 if bit 4 is set equal to 1; transmitted and received as 1 if bit 4 is set equal to 0.</td></tr>
<tr><td>6</td><td>Set break control bit. Enables processor to alert a terminal in the system. Serial output (SOUT) is forced to the spacing (0) state when bit 6 is set equal to 1; this does not change, regardless of other transmitter activity. Bit 6 equal to 0 disarms the set break.</td></tr>
<tr><td>7</td><td>Divisor latch access bit (DLAB). Bit 7 must be set equal to 1 to access the divisor latches of the baud rate generator during a read/write operation. This bit must be set equal to 0 to access the interrupt enable register the receiver buffer, or the transmitter holding register.</td></tr>
</table>

Line Status Register (LSR) — The LSR is an 8-bit register that provides data transfer status information to the processor. The following table defines the functions of the LSR bits:

Hex Address 3FD	Line Status Register (LSR)
Bit	**Function/Explanation**
0	**Receiver data ready (DR)** Set equal to 1 when a complete character has been received and transferred into the receiver buffer register. DR is reset to 0 when the processor reads the data in the receiver buffer register or when the processor writes a 0 into DR.
1	**Overrun error (OE)** Indicated that the next character was transferred into the receiver buffer register before the previous data was read, destroying the previous character. This indicator is reset whenever the processor reads the contents of the line status register.
2	**Parity error (PE)** Received data character parity is incorrect; parity is different from parity specified by the even parity select bit. PE is set equal to 1 when a parity error is detected; it is reset to 0 when the processor reads the content of the line status register.
3	**Framing error (FE)** Received character did not have a valid stop bit. Set equal to 1 whenever the stop bit following the last data bit or parity is detected as a zero bit.
4	**Break interrupt (BI)** Set equal to 1 whenever the received data input is held in the spacing state (logical 0) for a longer time than that required for full word transmission. NOTE: Bits 1-4 are error indicators that produce a receiver line status interrupt whenever the corresponding condition is detected.
5	**Transmitter holding register empty (THRE)** Set equal to 1 when a character is transferred from the transmitter holding register into the transmitter shift register; indicates that the 8250 is ready to accept a new character for transmistion. This causes the 8250 to send an interrupt to the processor when the transmit holding register empty interrupt enable is set high. THRE is reset to 0 concurrent with the loading of the transmitter holding register by the processor.
6	**Transmitter shift register empty (TSRE)** Set equal to 1 whenever the transmitter shift register is idle. This is a read-only bit and is reset to 0 whenever a data transfer from the transmitter holding register to the transmitter shift register occurs.
7	**Permanently set equal to logical zero** (0).

Interrupt Identification Register (IIR) — The 8250 contains an on-chip interrupt capability that assigns four different priority levels to interrupts:

- 1 Receiver line status
- 2 Receiver data ready
- 3 Transmitter holding register empty
- 4 Modem status

Assigning priorities to interrupts keeps software overhead to a minimum during data character transfers. The IIR stores information indicating that a prioritized interrupt is pending; it also stores information on the type of interrupt. When the IIR is addressed during chip selection, it freezes the highest-level interrupt that is pending and ignores all other interrupts until the frozen interrupt is serviced by the processor. The following tables define the functions of the IIR bits and the interrupt set/reset functions.

Hex Address 3FA	Interrupt Identification Register (IIR)
Bit	**Function/Explanation**
0	**Interrupt pending** Set equal to 0 when an interrupt is pending; when set equal to 1, indicates that no interrupt is pending and polling (if used) continues. May be used in either a hard-wired prioritized or polled environment; may also be used as a pointer to an appropriate interrupt service routine.
1,2	**Highest priority interrupt.** Use to identify the highest-priority pending. Use of these bits for identification is illustrated in the Interrupt Control Functions Table.
3-7	**Always equal to 0.**

Interrupt Identification Register			Interrupt Set/Reset Functions			
Bit 0	Bit 1	Bit 2	Priority Level	Interrupt Flag	Interrupt Source	Interrupt Reset Control
1	0	0	—	None	None	—
0	1	1	1 (Highest)	Receiver Line Status	Overrun, Parity, or Framing Error; Break Interrupt	Reading the Line Status Register
0	0	1	2	Received Data Available	Receiver Data Available	Reading the Receiver Buffer Register
0	1	0	3	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (of source of interrupt) or Writing into the Transmitter Holding Register
0	0	0	4	Modem Status	Clear to Send, Data Set Ready, Ring Indicator, or Received Line Signal Detect	Reading the Modem Status Register

Interrupt Enable Register (IER) — The IER, An 8-bit register in the 8250, enables the four interrupt levels to separately activate the chip interrupt (INTRPT) output signal. The interrupt system can be totally disabled by resetting bits 0-3 of the IER. Selected interrupt can be enabled by setting appropriate bits in this register to logical 1. Disabling the interrupt system inhibits the active (high) INTRPT output from the chip as well as the interrupt identification register (IIR). All other functions in the system continue to operate normally;

these include setting modem status registers and the line status register (LSR). The table below defines the functions of the IER bits.

Hex Address 3F9	Interrupt Enable Register (IER)
Bit	**Function/Explanation**
0	Set equal to 1 to enable the received data available interrupt.
1	Set equal to 1 to enable the transmitter holding register empty interrupt.
2	Set equal to 1 to enable the receiver status interrupt.
3	Set equal to 1 to enable the modem status interrupt.
4-7	Always equal to 0.

Modem Control Register (MCR) — The MCR,an 8-bit register, controls the interface with a modem, data set, or peripheral device that emulates a modem. The following table defines the functions of the MCR bits.

Hex Address 3FC	Modem Control Register (MCR)
Bit	Function/Explanation
0	**Data terminal ready (DTR) output** hn-When this bit is set equal to 0, the DTR output is forced to logical 1; when this bit is set equal to 1, the DTR output is forced to a logical 0. NOTE: DTR output from the 8250 may be applied to an EIA inverting line driver (such as the DS 1488) to get the proper polarity input at the modem or data set.
1	**Request to send (RTS) output** Functions in same manner as bit 0.
2	**Output 1 signal (OUT 1)** Auxiliary user-designated output. Functions in same manner as bit 0.
3	**Output 2 signal (OUT 2)** Auxiliary user-designated output. Functions in same manner as bit 0.
4	**Diagnostic loopback for 8250** When this bit is set equal to 1, the following events occur: • Transmitter serial output (SOST) is set to 1 • Receiver serial input (SIN) is disconnected • Transmitter shift register output is "looped" back into the receiver shift register input • Modem control inputs (CTS, DRES, RLSD, and RI) are disconnected • Modem control outputs (DTR, RTS, OUT1, and OUT2) are internally connected to the modem control inputs. Transmitted data is immediately received in the diagnostic mode; this allows the processor to verify the transmit and receive data paths of the 8250. Receiver and transmitter interrupts are fully operational in the diagnostic mode. Modem control interrupts are also operational; however, the interrupt sources are now the lower control inputs. The interrupt enable register continues to control the interrupts. The interrupt system is tested by writing into the lower six bits of the line status register and the lower four bits of the modem status register. Setting any of these bits equal to 1 generates the corresponding interrupt (if enabled); interrupts are reset in the same manner as during normal 8250 operation. To return to normal operation the register must be re-programmed for normal operation and bit 4 of the modem control register must be reset to 0.
5-7	Always equal to 0.

Modem Status Register (MSR — The MSR,an 8-bit register, indicates the current state of the control lines from the modem or other peripheral device to the processor. Four bi s of the MSR also provide change information. These bits are set equal to 1 whenever a control input from the modem changes state and are reset to 0 whenever the processor reads the MSR. The following table defines the functions of the MSR bits:

Hex Address 3FE	Modem Status Register (MSR)
Bit	**Function/Explanation**
0	**Delta clear-to-send (DCTS)** Indicates that CTS input to the chip has changed state since the last time it was read by the processor.
1	**Delta data set ready (DDSR)** Indicates that DSR input to the chip has changed state since the last time it was read by the processor.
2	**Trailing edge of ring (TERI)** Indicates that RI input to the chip has changed state since the last time it was read by the processor.
3	**Delta received line signal detector (DRLSD)** Indicates that the RLSD input to the chip has changed state.
4	Complement of the clear-to-send (CTS) input.
5	Complement of the data-set-ready (DSR) input.
6	Complement of the ring indicator (RI) input.
7	Complement of the received-line-signal-detect (RLSD) input.

Receiver Buffer Register (RBR) — The RBR, an 8-bit register, contains the received data characters. The following table defines the functions of the RBR bits:

Hex Address 3F8 Receiver Buffer Register DLAB=0 Read Only	
Bit	**Function/Explanation**
0	Data bit 0
1	Data bit 1
2	Data bit 2
3	Data bit 3
4	Data bit 4
5	Data bit 5
6	Data bit 6
7	Data bit 7
	NOTE: Bit 0 is the first bit serially received; it is the least significant bit.

Transmitter Holding Register (THR) — The THR, an 8-bit register, contains the next character to be transmitted. The following table defines the functions of the THR bits:

Hex Address 3F8 Transmitter Holding Register DLAB=0 Write Only	
Bit	**Function/Explanation**
0	Data bit 0
1	Data bit 1
2	Data bit 2
3	Data bit 3
4	Data bit 4
5	Data bit 5
6	Data bit 6
7	Data bit 7
	NOTE: Bit 0 is the first bit serially transmitted; it is the least significant bit.

Hardware Information

Interrupts/Bit Sequences — IRQ4 (used for Com 1) or IRQ3 (used for Com 2) provides a positive active interrupt to the system; this is the only interrupt line provided. It is functional only when bit 3 of the modem control register (MCR) is set equal to 1 (high).

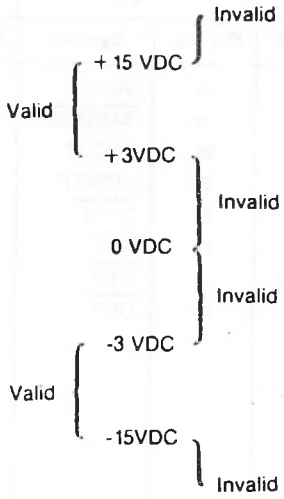
The data format is illustrated in the following figure:

Start Bit	D0	D1	D2	D3	D4	D5	D6	D7	Parity Bit	Stop Bits

The D0 (data bit 0) is the least significant bit and is the first bit to be transmitted or received. Start, stop, and parity bits are inserted as required if the adapter is programmed to do so. Five to eight data bits may be transmitted or received, followed by one or two stop bits; 1-1/2 stop bits may also be used, but only with the five-bit format.

Voltage Interchange Circuit — Signal voltages are measured at the interface point. Voltage must fall within the ranges of -3 to -15VDC or +3 to +15VDC, with respect to signal ground. The plus (+) range is considered to be the "spacing" condition and denotes a "0" binary state; it also defines the ON condition for interface control circuit functions. The minus (-) range is considered to be the "marking" condition and denotes a "1" binary state; it also defines the OFF condition for interface control circuit functions.

The range between +3VDC and -3VDC is considered to be an invalid signal level: any signal voltage exceeding +15VDC or -15VDC is also considered to be invalid.



Port Addressing — Serial-parallel port addressing is under software control, rather than under switch control; the power-up default is the serial port.

COM 1 or COM 2 serial port addressing is done through switches on the main processor board. Refer to Appendix C for complete information on proper switch settings.

8250 Input/Output Signals — The following table summarizes 8250 signals according to whether they are input, output, or I/O signals.

Input		Output		Input/Output	
Pin No.	Symbol	Pin No.	Symbol	Pin No.	Symbol
9	RCLK	11	SOUT	1-8	D0-D7
10	SIN	15	$\overline{\text{BAUDOUT}}$	16	XTAL1
12	CS0	24	CSOUT	17	XTAL2
13	CS1	30	INTRPT		
14	$\overline{\text{CS2}}$	31	$\overline{\text{OUT2}}$		
18	$\overline{\text{DOSTR}}$	32	$\overline{\text{RTS}}$		
19	DOSTR	33	$\overline{\text{DTR}}$		
20	VSS	34	$\overline{\text{OUT1}}$		
21	$\overline{\text{DISTR}}$				
22	DISTR				
25	$\overline{\text{ADS}}$				
26	A2				
27	A1				
28	A0				
35	MR				
36	$\overline{\text{CTS}}$				
37	$\overline{\text{DSR}}$				
38	$\overline{\text{RSLD}}$				
39	$\overline{\text{RI}}$				
40	VCC				

NOTE: Pin 23 (DDIS) is not used.

8250 Pin Definition — The Pin Definition Table defines the pin number, name symbol, and function for each pin on the 8250. In these definitions, a low represents a logical 0 (0VDC NOMINAL) and a high represents a logical 1 (+2.4VDC nominal).

Pin Number	Pin Name	Symbol	Function
1-8	DATA BUS	D0-D7	3-state input/output lines. Bi-directional communication lines between 8250 and Data Bus. All assembled data TX and RX, control words, and status information are transferred via the D0-D7 data bus.
9	RECEIVE CLK.	RCLK	This input is the 16X baud rate clock for the receiver section of the chip (may be tied to BAUDOUT pin 15).
10	SERIAL INPUT	SIN	Received Serial DAta in from the communications link (Peripheral device, modem or data set).
11	SERIAL OUTPUT	SOUT	Transmitted Serial Data Out to the communication link. The SOUT signal is set to a (logic 1) marking condition upon a MASTER RESET.
12 13 14	CHIP SELECT CHIP SELECT CHIP SELECT	CS0 CS1 $\overline{CS2}$	When CS0 and CS1 are high, and $\overline{CS2}$ is low, chip is selected. Selection is complete when the address strobe $\overline{ADS}$ latches the chip select signals.
15	BAUDOUT	$\overline{BAUDOUT}$	16X clock signal for the transmitter section of the 8250. The clock rate is equal to the oscillator frequency divided by the divisor loaded into the divisor latches. The BAUDOUT signal may be used to clock the receiver by tying to (pin 9) RCLK.
16 17	EXTERNAL CLOCK IN EXTERNAL CLOCK OUT	XTAL 1 XTAL 2	These pins connect the crystal or signal clock to the WD8250 baud rate divisor circuit. See Fig. 3 and Fig. 4 for circuit connection diagrams.

Pin Number	Pin Name	Symbol	Function
18 19	DATA OUT STROBE DATA OUT STROBE	$\overline{\text{DOSTR}}$ DOSTR	When the chip has been selected, a low $\overline{\text{DOSTR}}$ or high DOSTR will latch data into the selected 8250 register (a CPU write). Only one of these lines need be used. Tie unused line to its inactive state. $\overline{\text{DOSTR}}$ — high or DOSTR — low.
20	GROUND	VSS	System signal ground.
21 22	DATA IN STROBE DATA IN STROBE	$\overline{\text{DISTR}}$ DISTR	When chip has been selected, a low $\overline{\text{DISTR}}$ or high DISTR will allow a read of the selected WD8250 register (a CPU read). Only one of these lines need be used. Tie unused line to its inactive state. $\overline{\text{DISTR}}$ — high or DISTR — low.
23	DRIVER DISABLE	DDIS	Output goes low whenever data is being read from the 8250. Can be used to reverse data direction of external transceiver.
24	CHIP SELECT OUT	CSOUT	Output goes high when chip is selected. No data transfer can be inititated until CSOUT is high.
25	ADDRESS STROBE	$\overline{\text{ADS}}$	When low, provides latching for register. Select (A0, A1, A2) and chip select (CS0, CS1, $\overline{\text{CS2}}$) NOTE: An active $\overline{\text{ADS}}$ signal is required when the Register Select (A0, A1, A2) signals are not stable for the duration of a read or write operation. If not required, the $\overline{\text{ADS}}$ input can be tied permanently low.
26 27 28	REGISTER SELECT A2 REGISTER SELECT A1 REGISTER SELECT A0	A2 A1 A0	These three inputs are used to select a 8250 internal register during a data read or write. See Table below.
29	NO CONNECT	NC	No Connect
30	INTERRUPT	INTRPT	Output goes high whenever an enabled interrupt is pending.

Pin Number	Pin Name	Symbol	Function
31	OUTPUT 2	$\overline{OUT2}$	User-designated output that can be programmed by Bit 3 of the modem control register = 1, causes $\overline{OUT2}$ to go low.
32	REQUEST TO SEND	$\overline{RTS}$	Output when low informs the modem or data set that the 8250 is ready to transmit data. See Modem Control Register.
33	DATA TERMINAL READY	$\overline{DTR}$	Output when low informs the modem or dataa set that the 8250 is ready to communicate.
34	OUTPUT 1	$\overline{OUT1}$	User designated output can be programmed by Bit 2 of Modem Control Register = 1 causes $\overline{OUT1}$ to go low.
35	MASTER RESET	MR	When high clears the registers to states as indicated in the following table.
36	CLEAR TO SEND	$\overline{CTS}$	Input from DCE indicating remote device is ready to transmit. See Modem Control Register.
37	DATA SET READY	$\overline{DSR}$	Input from DCE used to indicate the status of the local data set. See Modem Control Register.
38	RECEIVED LINE SIGNAL DETECT	$\overline{RSLD}$	Input from DCE indicating that it is receiving a signal which meets its signal quality conditions. See Modem Control Register.
39	RING INDICATOR	$\overline{RI}$	Input, when low, indicates that a ringing signal is being received by the modem or data set. See Modem Control Register.
40	+5V	VCC	+5 Volt Supply.

Reset Control of Registers and Pinout Signals		
Register/Signal	**Reset Control**	**Reset State**
Receiver Buffer Register	First Word Received	Data
Transmitter Holding Register	Writing into the Transmitter Holding Register	Data
Interrupt Enable Register	Master Reset	All Bits low (0-3 forced and 4-7 permanent)
Interrupt Identification Register	Master Reset	Bit 0 is High and Bits 1-7 are Permanently Low
Line Control Register	Master Reset	All Bits Low
MODEM Control Register	Master Reset	All Bits Low
Line Status Register	Master Reset	All Bits Low Except Bits 5 and 6 are High
Modem Status Register	Master Reset MODEM Signal Inputs	Bits 0-3 Low Bits 4-7 — Input Signal
Divisor Latch (low order bits)	Writing into the Latch	Data
Divisor Latch (high order bits)	Writing into the Latch	Data
SOUT	Master Reset	High
BAUDOUT	Writing into either Divisor Latch	Low
CSOUT	ADS Strobe Signal and State of Chip Select Lines	High/Low
DDIS	DDIS — CSOUT • RCLK • DISTR (At Master Reset, the CPU sets RCLK and DISTR low.)	High
INTRPT	Master Reset	Low

KEYBOARD

PHYSICAL DESCRIPTION

The keyboard is the means by which the user communicates with the system. Ninety-five keys are provided for maximum operating flexibility.

Function Keys Reference 1 on keyboard illustration

The ten function keys on the far left of the keyboard are programmable by the user.

Typewriter Keypad Reference 2 on keyboard illustration

The typewriter section of the keyboard is a standard layout of alphanumeric keys with the addition of a few function keys. The keys are software defined. The keyboard features n-key-rollover which allows additional keys to be depressed before previously depressed keys are released. Also, all keys have an auto-repeat feature which allows keys to generate their functions repeatedly as long as they are held down.

Cursor Control Keypad Reference 3 on keyboard illustration.

The cursor control keypad permits easy cursor movement and screen editing. In addition, the function keys are redefinable by software.

Calculator Keypad Reference 4 on keyboard illustration.

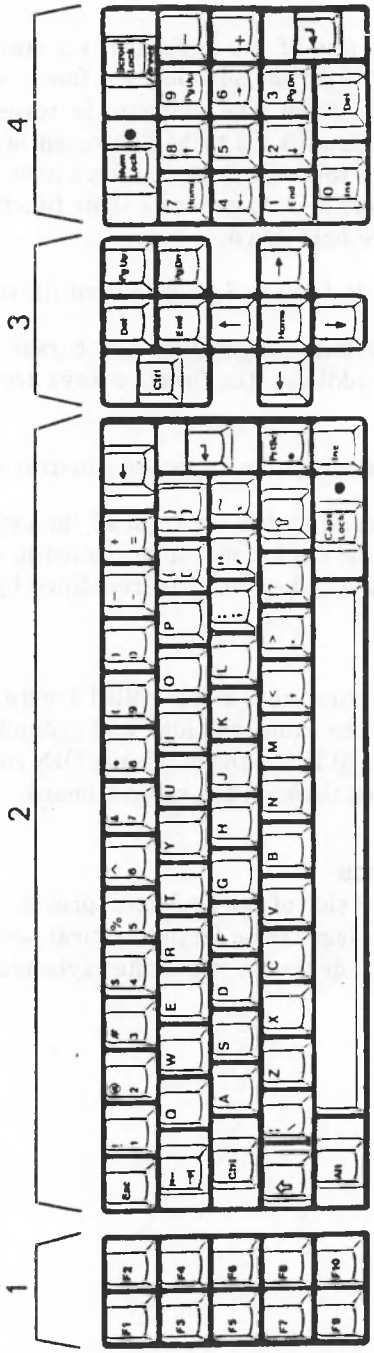
The calculator keypad on the far right of the keyboard supplies calculator functions, cursor movement control, numeric entry, and edit functions. The keys may be redefined by software.

Cabling

The keyboard is hard-wired to a 6-foot coiled 4-wire cable with two bidirectional signals. The cable, shielded and grounded, connects to the main processor board by means of a 5-pin DIN connector. Power at +5.2VDC is supplied through the system board.

Keyboard Ergonomics

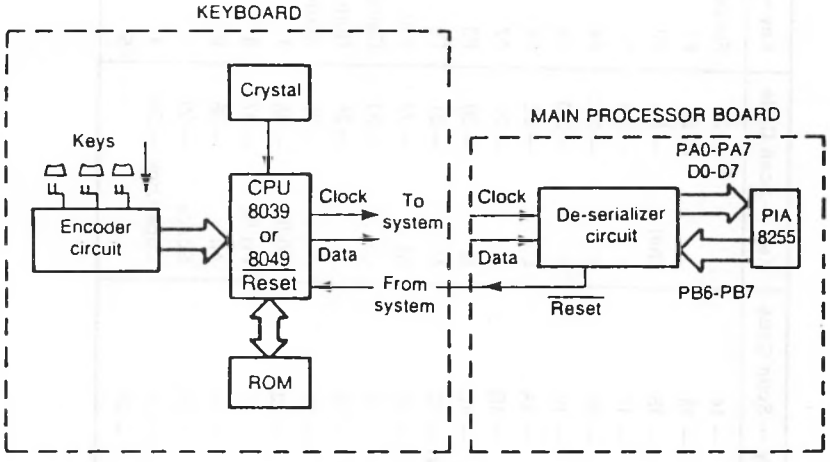
Two "legs", one on each side of the keyboard, provide tilt adjustment for typing comfort. The legs can be set in a vertical position or in other positions to provide the degree of tilt to the keyboard that best suits the operator.



Keyboard Layout

FUNCTIONAL DESCRIPTION

The keyboard functions by means of full-travel mechanical keys returning scan codes to an Intel 8039 or an 8049 microprocessor in the keyboard. The 8039 is an 8-bit, microprocessor with 1K by 8-bit program memory, 64 by 8-bit RAM data memory, 27 I/O lines, and an 8-bit timer/counter. The 8039 uses an external ROM while the 8049 has an internal ROM. Either of the microprocessors can store up to 16 scan codes in a buffer, perform a self-test for malfunctioning keys, test memory, and check its own ROM. Either one scans the keyboard and handles the two signals for the bidirectional lines and the handshaking for the scan-code transfer.



Keyboard Block Diagram

During operation, the keys generate a make and a break scan code. (The break code is the make code plus 80 hex; see the scan code diagram on the next page.)

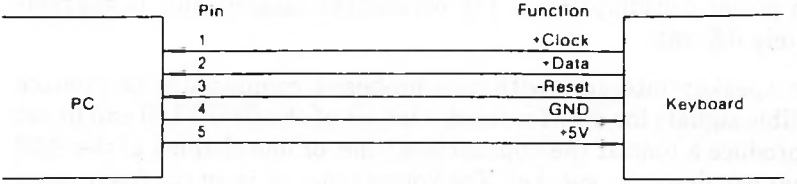
KEYBOARD SCAN CODES

The following list shows the keyboard reference positions and the hex scan code for each:

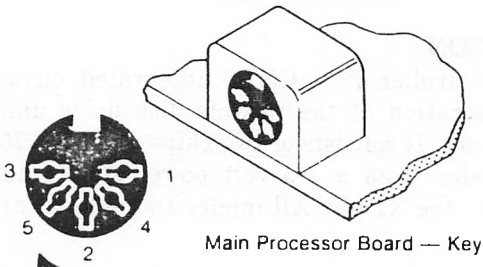
Key — Scan Code	Key — Scan Code	Key — Scan Code	Key — Scan Code	Key — Scan Code
Typewriter Keys	T — 14	' — 28	Function Keys	6 — 4D
Esc — 01	Y — 15	, — 29	F1 — 3B	+ — 4E
1 — 02	U — 16	Shift — 2A	F2 — 3C	1 — 4F
2 — 03	I — 17	\ — 2B	F3 — 3D	2 — 50
3 — 04	O — 18	Z — 2C	F4 — 3E	3 — 51
4 — 05	P — 19	X — 2D	F5 — 3F	Ins — 52
5 — 06	[— 1A	C — 2E	F6 — 40	Del — 53
6 — 07	] — 1B	V — 2F	F7 — 41	Cursor Control Keys
7 — 08	↵ — 1C	B — 30	F8 — 42	Ctrl — 1D
8 — 09	Ctrl — 1D	N — 31	F9 — 43	Del — 53
9 — 0A	A — 1E	M — 32	F10 — 46	Pg Up — 49
0 — 0B	S — 1F	, — 33	Calculator Keys	End — 4F
- — 0C	D — 20	. — 34	Num Lock — 45	Home — 47
= — 0D	F — 21	/ — 35	Scroll Lock — 44	Ins — 52
* — 0E	G — 22	Shift — 36	7 — 47	
++ — 0F	H — 23	Prt Sc — 37	8 — 48	
Q — 10	J — 24	Alt — 38	9 — 49	
W — 11	K — 25	Space — 39	- — 4A	
E — 12	L — 26	Caps Lock — 3A	4 — 4B	
R — 13	; — 27		5 — 4C	

PHYSICAL CONNECTIONS/PIN ASSIGNMENTS

The 5-pin DIN connector has the following pin configuration. The signal level is +5VDC:



Keyboard Interface Signals



Main Processor Board — Keyboard Connector

SPEAKER SYSTEM

A 2-inch diameter speaker is mounted inside the chassis of the PERSONAL COMPUTER PC6. It is driven by a 2N3906 transistor

and power consumption of the permanent magnet unit is approximately 0.8 watt.

The speaker interacts with two on-board components to produce audible signals for user feedback. One bit of the CPU VLSI can be set to produce a tone at the appropriate time, or one channel of the 8253 timer can drive the speaker. The volume control is on the front panel of the computer.

FLEXIBLE DISK DRIVE CONTROLLER

FUNCTIONAL DESCRIPTION

The flexible disk drive controller is a CMOS integrated circuit designed to control the operation of the flexible disk drive units during the disk I/O operations. It consists of two chips, the NEC 765 and the FE 2100. It operates from a +5 volt power supply and requires an 8 MHz signal to the X1 pin. All inputs and outputs are TTL compatible.

Input to the controller is buffered on the I/O bus and uses the DMA chip on the processor board to transfer data records. A level 6 DMA interrupt is used to report the completion of an operation and any status conditions that require resolution by the 8088-2 processor on the main processor board.

The disk drive parameters on the controller are programmable, allowing the support of up to four flexible disk drive units: 5.25 inch half-height double density (MFM Format).

SOFTWARE INFORMATION

Software Command Sequence

The flexible disk controller can perform 15 different operational commands. Every operation (command) is initiated by a transfer of a byte or string of bytes from the 8088-2 to the data register of the UPD765 on the disk controller. The cyclic nature of commands, execution of the commands, and the return of results, are more easily understood when discussed as three sequential events: the command, execution, and result phases.

- Command Phase

  During the command phase, the flexible disk controller receives all the required information (data and parameters for execution of the command) from the 8088-2 on the main processor board.

- Execution Phase

  During the execution phase, the flexible disk controller performs the operation (command) ordered, using the data passed to it from the main processor board.

- Result Phase

  During the result phase, operational status and data (if a READ operation) is made available to the main processor board. Data bytes are accessed from the data register, and the status byte is accessed from the status register of the UPD765.

With the three phases of each command defined, the actual operation of the 15 commands used by the flexible disk drive controller is shown in the command summary. The abbreviations used in the tables are listed at the end of the command summary tables.

Port Information

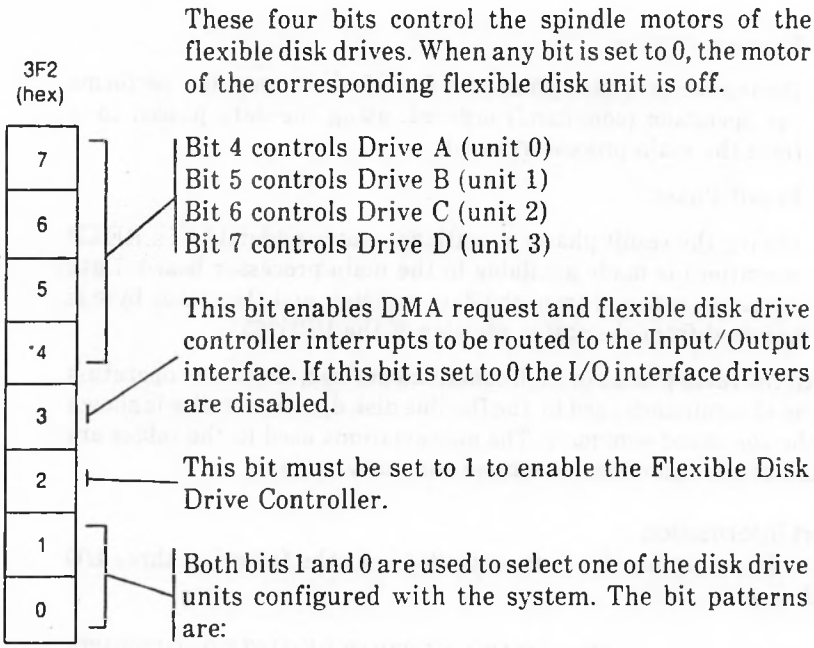
I/O addressing for the disk controller is at the following three I/O addresses:

3F2	(HEX) DATA OUTPUT REGISTER (OUTPUT)
3F4	(HEX) STATUS REGISTER (INPUT) COMMAND REGISTER (OUTPUT)
3F5	(HEX) RESULT STACK (INPUT) INPUT (7 RESULTS MAXIMUM) COMMAND STACK (OUTPUT) OUTPUT (9 COMMANDS MAXIMUM)

Digital Output Register

The digital output register, a write-only register byte located at I/O port address 3F2 (hex) is used to: (1) select disk drive units, (2) control the motors of those units, and (3) enable controller interrupts and DMA requests. All bits are set to 0 by the I/O reset and have the following functions:

These four bits control the spindle motors of the flexible disk drives. When any bit is set to 0, the motor of the corresponding flexible disk unit is off.



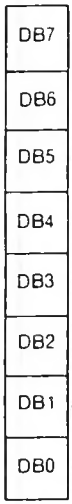
Bit 0	Bit 1	
0	0	Select Drive A
1	0	Select Drive B
0	1	Select Drive C
1	1	Select Drive D

Internal Registers

The flexible disk controller (UPD765) has two internal registers: a status register and a data register; each may be accessed by the main processor board at any time.

Status Register

The status register is an 8-bit read-only register, located at port address 3F4 (hex), that contains the current status of the flexible disk controller. The following descriptions define the status register bits and their meanings:



DB7 = If 1, this bit indicates that the data register is READY to send or receive data to, or from, the flexible disk controller. The direction of data transfer is determined by the DB6 status.

DB6 = If 0, directions of data transfer is from the main processor board to the controller data register; If 1, the direction of data transfer is from the controller data register to the main processor board.

DB5 = If 1, controller is executing in a non-DMA mode; if 0, execution is completed. (This bit used only during non-DMA mode operations.)

DB4 = If 1, a READ or WRITE command is in progress.

DB3 = If 1, flexible disk drive 3 (D) is presently in the SEEK Mode. (Applicable only for external drive units)

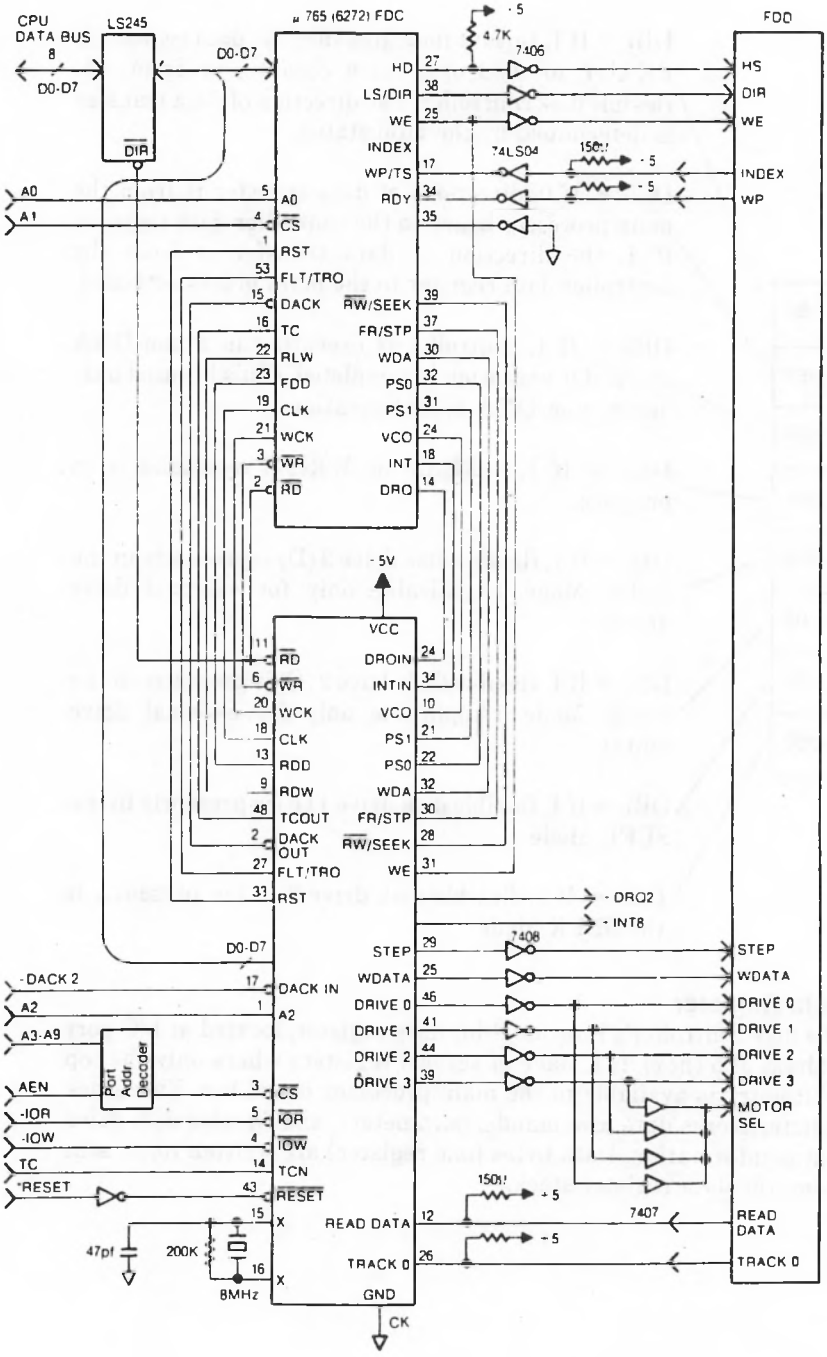
DB2 = If 1, flexible disk drive 2 (C) is presently in the SEEK Mode. (Applicable only for external drive units)

DB1 = If 1, flexible disk drive 1 (B) is presently in the SEEK Mode.

DB0 = If 1, flexible disk drive 0 (A) is presently in the SEEK Mode.

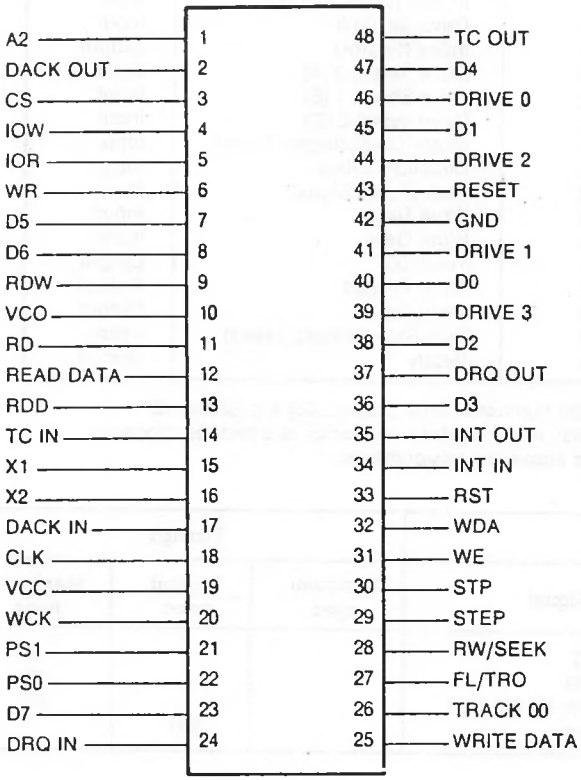
Data Register

The disk controller's internal 8-bit data register, located at I/O port address 3F5 (hex), is a stack of several registers where only the top 8-bit entry is available to the main processor board bus. This stack register stores data, commands, parameters, and flexible disk drive status information. Data bytes (one register) are written to, or sent from, the data register stack.


CPU DATA BUS
8
D0-D7
LS245
DIR
D0-D7
µ 765 (6272) FDC
+5
4.7K
7406
HD
LS/DIR
WE
INDEX
WP/TS
RDY
74LS04
150Ω
+5
+5
FDD
HS
DIR
WE
INDEX
WP
A0
A1
A0
CS
RST
FLT/TRO
DACK
RW/SEEK
TC
FR/STP
RLW
WDA
FDD
PS0
CLK
PS1
WCK
VCO
WR
INT
RD
DRQ
-5V
VCC
RD
DROIN
WR
INTIN
WCK
VCO
CLK
PS1
RDD
PS0
RDW
WDA
TCOUT
FR/STP
DACK OUT
RW/SEEK
FLT/TRO
WE
RST
-DRQ2
-INT8
D0-D7
7408
STEP
WDATA
DRIVE 0
DRIVE 1
DRIVE 2
DRIVE 3
STEP
WDATA
DRIVE 0
DRIVE 1
DRIVE 2
DRIVE 3
MOTOR SEL
-DACK 2
A2
A3-A9
AEN
-IOR
-IOW
TC
*RESET
DACK IN
A2
Port Addr Decoder
CS
IOR
IOW
TCN
RESET
150Ω
+5
7407
READ DATA
TRACK 0
READ DATA
TRACK 0
47pf
200K
8MHz
X
X
GND
CK

Pin Configuration

Disk Drive Controller Chip



Pin Number	Signals	Direction
(odd)*		
2	(Not Connected)	(N/C)
4	In Use (Drive Active)	Input
6	Drive Select 3	Input
8	Index (Sector)	Output
10	Drive Select 0 (A)	Input
12	Drive Select 1 (B)	Input
14	Drive select 2 (C)	Input
16	Motor On (Selected Drive)	Input
18	Direction Select	Input
20	Step (Pulse Signal)	Input
22	Write Data	Input
24	Write Gate	Input
26	Track 00	Output
28	Write Protect	Output
30	Read Data	Output
32	Side Select (Head Select)	Input
34	Ready	Output

*All odd numbered Pins (1,3,5,7,...33) are GROUND
The disk drive interface connector is a header connector with the above pin assignments.

	Timings		
Signal	Minimum nsec	Typical nsec	Maximum nsec
IOR to RD			91
IOW to WR			86
DACK IN to DACK OUT			101
CLK period		250	

Environmental Specifications

Operating Temperature Range: 0° to 70°
Supply Voltage: +4.75 V Minimum, +6.00 V Maximum

PHYSICAL CONNECTIONS/PIN ASSIGNMENTS

System Interface

The following signals are input to the flexible disk controller on the main processor board:

Pin Function Table:

PIN	TYPE	SYMBOL	FUNCTION
1	I	+A2	CPU I/O address A2
2	O	- DACK OUT	DMA cycle active to FDC
3	I	- CS	FDC and FFDC chip select
4	I	- IOW	I/O write from CPU
5	I	- IOR	I/O read from CPU
6	O	- WR	Control signal to transfer data from data bus to FDC
7	I	+D5	CPU data bus bit 5
8	I	+D6	CPU data bus bit 6
9	O	+RDW	Generated by PLL to sample data from floppy disk drive
10	O	+VCO	Enables VCO in PLL
11	O	- RD	Control signal to transfer data from FDC to data bus
12	I	- READ DATA	Raw read data from disk drive
13	O	+RDD	Read data containing clock and data to FDC
14	I	+TC IN	End of DMA cycle
15	I	+X1	Crystal clock input
16	O	+X2	Crystal clock output
17	I	- DACK IN	DMA acknowledge from CPU I/O bus
18	O	+CLK	4 MHz clock to FDC
19	—	VCC	+5 volts D.C. power
20	O	+WCK	Write data rate to disk drive
21	I	+PS1	Pre compensation select in MFM mode from FDC
22	I	+PS0	Pre compensation select in MFM mode from FDC
23	I	+D7	CPU data bus bit 7
24	O	+DRQ IN	DMA request from FDC
25	O	+W DATA	Serial CLK and data to disk drive
26	O	- TRACK 00	Track 0 condition from disk drive
27	I	+FLT/TRO	Indicates disk drive fault condition in RD/WR mode or track 0 in seek mode
28	O	- RW/SEEK	Select RD/WR mode or seek mode
29	O	+STEP	Step signal to disk drive
30	O	+STP	Step signal from FDC
31	O	+WE	Enables WR data to disk drive
32	O	+WDA	Serial CLK and data from FDC
33	O	+RST	Reset to FDC
34	I	+INT IN	INT request from FDC
35	O	+INT OUT	INT request to CPU
36	I	+D3	CPU data bus bit 3
37	O	+DRQ OUT	DMA request to CPU
38	I	+D2	CPU data bus bit 2
39	O	+DRIVE 3	Disk drive select 3
40	I	+D0	CPU data bus bit 0
41	O	+DRIVE 1	Disk drive select 1
42	—	GROUND	
43	I	- RESET	Initialize data separator and drive select register
44	O	+DRIVE 2	Disk drive select 2
45	I	+D1	CPU data bus bit 1
46	O	+DRIVE 0	Disk drive select 0
47	O	+D4	CPU data bus bit 4
48	OP	+TC OUT	End of DMA transfer to FDC

Command Summary Tables

In the following command summary tables, 0 indicates "logical 0" for that bit, 1 means "logical 1," and X means "any."

Phase	R/W	Data Bus Bits D7	D6	D5	D4	D3	D2	D1	D0	Comments
		Read Data								
Command	W	MT	MF	SK	0	0	1	1	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W				C					Sector ID information
	W				H					prior to command
	W				R					execution.
	W				N					
	W				EOT					
	W				GPL					
	W				DTL					
Execution										Data transfer between the FDD and the main system.
Result	R				ST0					Status information
	R				ST1					after command
	R				ST2					execution.
	R				C					Sector ID information
	R				H					after command
	R				R					execution.
	R				N					
		Read Deleted Data								
Command	W	MT	MF	SK	0	1	1	0	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W				C					Sector ID information
	W				H					prior to command
	W				R					execution.
	W				N					
	W				EOT					
	W				GPL					
	W				DTL					
Execution										Data transfer between the FDD and the main system.
Result	R				ST0					Status information
	R				ST1					after command
	R				ST2					execution.
	R				C					Sector ID information
	R				H					after command
	R				R					execution.
	R				N					

Command Summary (1 of 6)

Command Abbreviations

The following tables define the symbols used in the command summary:

Phase	R/W	Data Bus Bits D7	D6	D5	D4	D3	D2	D1	D0	Comments
		Write Data								
Command	W	MT	MF	0	0	0	1	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W				C					Sector ID information
	W				H					prior to command
	W				R					execution.
	W				N					
	W				EOT					
	W				GPL					
	W				DTL					
Execution										Data transfer between the FDD and the main system.
Result	R				ST0					Status information
	R				ST1					after command
	R				ST2					execution.
	R				C					Sector ID information
	R				H					after command
	R				R					execution.
	R				N					
		Write Deleted Data								
Command	W	MT	MF	0	0	1	0	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W				C					Sector ID information
	W				H					prior to command
	W				R					execution.
	W				N					
	W				EOT					
	W				GPL					
	W				DTL					
Execution										Data transfer between the FDD and the main system.
Result	R				ST0					Status information
	R				ST1					after command
	R				ST2					execution.
	R				C					Sector ID information
	R				H					after command
	R				R					execution.
	R				N					

Command Summary (2 of 6)

Command Status Register

The following tables define the values of ST0, ST1, ST2, and ST3, which are the status values from the command summary.

Phase	R/W	Data Bus Bits D7	D6	D5	D4	D3	D2	D1	D0	Comments
		Read a Track								
Command	W	MT	MF	SK	0	0	0	1	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information
	W	H								prior to command
	W	R								execution.
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and the main system. FDC reads all of cylinder's contents from index hole to EOT.
Result	R	ST0								Status information
	R	ST1								after command
	R	ST2								execution.
	R	C								Sector ID information
	R	H								after command
	R	R								execution
	R	N								
		Read ID								
Command	W	MT	MF	0	0	1	0	1	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
Execution										The first correct ID information on the cylinder is stored in data register.
Result	R	ST0								Status information
	R	ST1								after command
	R	ST2								execution.
	R	C								Sector ID information
	R	H								during execution
	R	R								phase.
	R	N								

Command Summary (3 of 6)

Phase	R/W	Data Bus Bits D7	D6	D5	D4	D3	D2	D1	D0	Comments
					Format a Track					
Command	W	MT	MF	0	0	1	1	0	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W				N					Bytes/Sector
	W				SC					Sector/Track
	W				GPL					Gap 3
	W				D					filler byte.
Execution										FDC formats an entire cylinder.
Result	R				ST0					Status information
	R				ST1					after command
	R				ST2					execution.
	R				C					In this case, the ID
	R				H					information has no
	R				R					meaning.
	R				N					
					Scan Equal					
Command	W	MT	MF	SK	1	0	0	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W				C					Sector ID information
	W				H					prior to command
	W				R					execution.
	W				N					
	W				EOT					
	W				GPL					
	W				STP					
Execution										Data compared between the FDD and the main system.
Result	R				ST0					Status information
	R				ST1					after command
	R				ST2					execution.
	R				C					Sector ID information
	R				H					after command
	R				R					execution.
	R				N					

Command Summary (4 of 6)

Phase	R/W	Data Bus Bits D7	D6	D5	D4	D3	D2	D1	D0	Comments
		Scan Low or Equal								
Command	W	MT	MF	SK	1	1	0	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information
	W	H								prior to command
	W	R								execution.
	W	N								
	W	EOT								
	W	GPL								
	W	STP								
Execution										Data compared between the FDD and main system.
Result	R	ST0								Status information
	R	ST1								after command
	R	ST2								execution.
	R	C								Sector ID information
	R	H								after command
	R	R								execution.
	R	N								
		Scan High or Equal								
Command	W	MT	MF	SK	1	1	1	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information
	W	H								prior to command
	W	R								execution.
	W	N								
	W	EOT								
	W	GPL								
	W	STP								
Execution										Data compared between the FDD and main system.
Result	R	ST0								Status information
	R	ST1								after command
	R	ST2								execution.
	R	C								Sector ID information
	R	H								after command
	R	R								execution.
	R	N								

Command Summary (5 of 6)

Phase	R/W	Data Bus Bits D7	D6	D5	D4	D3	D2	D1	D0	Comments
Recalibrate										
Command	W	MT	MF	SK	0	0	1	1	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
Execution No Result Phase										
Sense Interrupt Status										
Command	W	0	0	0	0	1	0	0	0	Command Codes
Result	R				ST0					Status information at the end of seek operation about the FDC
	R				PCN					
Specify										
Command	W	0	0	0	0	0	0	1	1	Command Codes
	W		SRT					HUT		
	W			HLT					ND	
No Result Phase										
Sense Drive Status										
Command	W	0	0	0	0	0	1	0	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
Result					ST3					Status information about FDD.
Seek										
Command	W	0	0	0	0	1	1	1	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
					NCN					
Execution										Head is positioned over proper cylinder on diskette
No Result Phase										
Invalid										
Command	W				Invalid Codes					Invalid command codes (NoOp - FDC goes into standby state).
Result	R				ST0					ST0 = 80.

Command Summary (6 of 6)

Symbol	Name	Description
A0	Address Line 0	A0 controls selection of main status register (A0 = 0) or data register (A0 = 1).
C	Cylinder Number	C = the current/selected cylinder (track) number of the medium.
D	Data	D = the data pattern that is going to be written into a sector.
D7-D0	Data	8-bit data bus, where D7 = most significant bit, and DO least significant bit.
DTL	Data Length	When N is defined as 00, DTL = the data length that users are going to read from or write to the sector.
EOT	End Of Track	EOT = the final sector number on a cylinder.
GPL	Gap Length	GPL = the length of gap 3 (spacing between sectors excluding VCO sync field).
H	Head Address	H = head number 0 or 1, as specified in ID field.
HD	Head	HD = a selected head number 0 or 1. (H = HD in all command words.)
HLT	Head Load Time	HUT = the head unload time after a read or write operation has occurred (0 to 480 ms in 32-ms increments).
MF	FM or MFM Mode	If MF is low,, FM mode is selected; if it is high, MFM mode is selected only if MFM is implemented.
MT	Multi-Track	If MT is high, a multi-track operation is to be performed. (A cylinder under both HDO and HD1 will be read or written.)
N	Number	N = the number of data bytes written in a sector.

Command Symbols (1 of 2)

Symbol	Name	Description
NCN	New Cylinder Number	NCN = a new cylinder number, which is going to be reached as a result of the seek operation. (Desired position of the head.)
ND	Non-DMA Mode	ND = operation in the non-DMA mode.
PCN	Present Cylinder Number	PCN = cylinder number at the completion of sense-interrupt-status command indicated the position of the head at present time.
R	Record	R = the sector number, which will be read or written.
R/W	Read/Write	R/W = either (R) or write (W) signal.
SC	Sector	SC indicates the number of sectors per cylinder.
SK	Skip	SK = skip deleted-data address mark.
SRT	Step Rate Time	SRT = the stepping rate for the FDD (2 to 32 ms in 2-ms increments).
ST 0 ST 1 ST 2 ST 3	Status 0 Status 1 Status 2 Status 3	ST 0-3 = one of four registers that store the status information after a command has been executed. This information is available during the result phase after command execution. These registers should not be confused with the main status register (selected by A0 = 0). ST 0-3 may be read only after a command has been executed and contain information relevant to that particular command.
STP	Scan Test	During a scan operation, if STP = 1, the data in contiguous sectors is compared byte-by-byte with data sent from the processor (or DMA), and if STP = 2, then alternate sectors are read and compared.
US0, US	Unit Select	US = a selected drive number encoded the same as bits 0 and 1 of the digital output register (DOR).

Command Symbols (2 of 2)

Data Bit			
No.	Symbol	Name	Data Bit Description
7 6	IC	Interrupt Code	Bit 7 = 0 and bit 6 = 0 Normal termination of command (NT). Command was completed and properly executed. Bit 7 = 0 and bit 6 = 1 Abnormal termination of command (AT). Execution of command was started, but was not successfully completed. Bit 7 = 1 and bit 6 = 0 Invalid command issue (1C). Command that was issued and was never started. Bit 7 = 1 and bit 6 = 1 Abnormal termination because, during command execution, the ready signal from FDD changed state.
5	SE	Seek End	When the FDC completes the seek command, this flag is set to 1 (high).
4	EC Check	Equipment	If a fault signal is received from the FDD, or if the track 0 signal fails to occur after 77 step pulses (recalibrate command), then this flag is set.
3	NR	Not Ready	When the FDD is in the not-ready state and a read or write command is issued, this flag is set. If a read or write command is issued to side 1 of a single-sided drive, then this flag is set.
2	HD	Head Address	This flag is used to indicate the state of the head at interrupt.
1 0	US 1 US 0	Unit Select 1 Unit Select 0	These flags are used to indicate a drive unit number at interrupt.

Command Status Register 0

Bit			Data Bit Description
No.	Symbol	Name	
7	EN	End of Cylinder	When the FDC tries to access a sector beyond the final sector of a cylinder, this flag is set.
6	—	—	Not used. This bit is always 0 (low).
5	DE	Data Error	When the FDC detects a CRC error in either the ID field or the data field, this flag is set.
4	OR	Over Run	If the FDC is not serviced by the main system during data transfers within a certain time interval, this flag is set.
3	—	—	Not used. This bit is always 0 (low).
2	ND	No Data	During execution of a read data, write deleted data, or scan command, if the FDC cannot find the sector specified in the ID register, this flag is set. During execution of the read ID command, if the FDC cannot read the ID field without an error, then this flag is set. During the execution of the read a cylinder command, if the starting sector cannot be found, then this flag is set.
1	NW	Not Writeable	During execution of a write data, write deleted data, or format-a-cylinder command, if the FDC detects a write-protect signal from the FDD, then this flag is set.
0	MA	Missing Address Mark	If the FDC cannot detect the ID address mark, this flag is set. Also, at the same time, the MD (missing address mark in the data field) of status register 2 is set.

Command Status Register 1

Data Bit			Data Bit Description
No.	Symbol	Name	
7	—	—	Not used. This bit is always 0 (low).
6	CM	Control Mark	During execution of the read data or scan command, if the FDC encounters a sector that contains a deleted data address mark, this flag is set.
5	DD	Data Error in Data Field	If the FDC detects a CRC error in the data, then this flag is set.
4	WC	Wrong Cylinder	This bit is related to the ND bit, and when the contents of C on the medium are different from that stored in the ID register, this flag is set.
3	SH	Scan Equal Hit	During execution of the scan command, if the condition of "equal" is satisfied, this flag is set.
2	SN	Scan Not Satisfied	During execution of the scan command, if the FDC cannot find a sector on the cylinder that meets the condition, then this flag is set.
1	BC	Bad Cylinder	This bit is related to the ND bit, and when the contents of C on the medium are different from that stored in the ID register, and the contents of C is FF, then this flag is set.
0	MD	Missing Address Mark in Data Field	When data is read from the medium, if the FDC cannot find a data address mark or deleted data address mark, then this flag is set.

Command Status Register 2

Data Bit			Data Bit Description
No.	Symbol	Name	
7	FT	Fault	This bit is the status of the fault signal from the FDD.
6	WP	Write Protected	This bit is the status of the write-protected signal from the FDD.
5	RY	Ready	This bit is the status of the ready signal from the FDD.
4	T0	Track 0	This bit is the status of the track 0 signal from the FDD.
3	TS	Two Side	This bit is the status of the two-side signal from the FDD.
2	HD	Head Address	This bit is the status of the side-select signal from the FDD.
1	US 1	Unit Select 1	This bit is the status of the unit-select-1 signal from the FDD.
0	US 0	Unit Select 0	This bit is the status of the unit-select-0 signal from the FDD.

Command Status Register 3

Flexible Disk Controller Constants

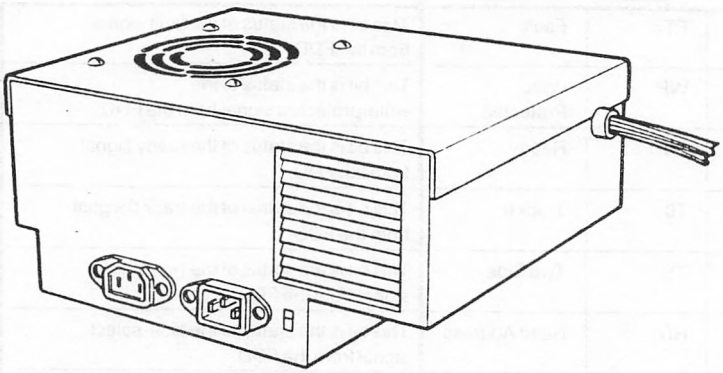
The following are the physical constants used on flexible disk drive:

- Number of data bytes written in a sector = 02 (hex)
- Number of sectors per cylinder (track) = 08 (hex)
- Track step rate time (6 milliseconds track to track) = C (hex)

POWER SUPPLY

PHYSICAL DESCRIPTION

The power supply converts AC current to regulated DC power for use by the main processor board, disk drives, keyboard, and plug-in options. The unit is mounted at the side of the cabinet bottom, above the main processor board.



FUNCTIONAL DESCRIPTION

AC current (120VAC) travels through an RFI line filter and a 3-amp in-line fuse to the power switch, and finally into the power supply. The output of the power supply is DC regulated.

Output	Supplies Power To*
+5.2VDC at 15A ±4%	Main Processor Board, Disk Drives Keyboard Expansion Adapters
+ 12.2VDC at 4.2A ±5%	Main Processor Board, Disk Drives (one at a time), Expansion Slots
-5.0VDC at 300MA ±3%	Expansion Slots
-12.2VDC at 250MA ±5%	Main Processor Board and Expansion Slots

* All voltages are bussed across the eight expansion slots.

A 3-amp in-line fuse between the line filter and the power switch protects the system. The DC outputs shut down at over-voltage and over-current conditions.

OPERATING CHARACTERISTICS

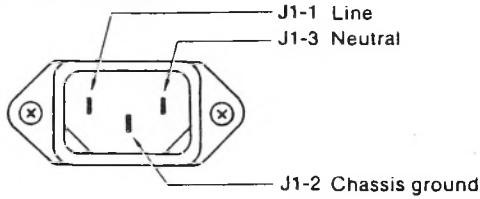
- Input: 120VAC (min. 104, max. 127)
  59 — 60.6Hz frequency
  6.0 A max. @ 120VAC

- Continuous operation at 130 watts

- Cooled by air movement from an internal built-in fan.

Physical Connectors/Pin Assignments

Power Supply Input Connections



Secondary Storage Components

This section provides information about secondary storage components and the necessary adapter boards that are available for use with the NCR PERSONAL COMPUTER PC6. Specifically, technical reference information is presented about the flexible disk drive, the fixed disk drive and its adapter board, the tape back-up drive unit, and the diskettes that are used with the flexible disk drive.

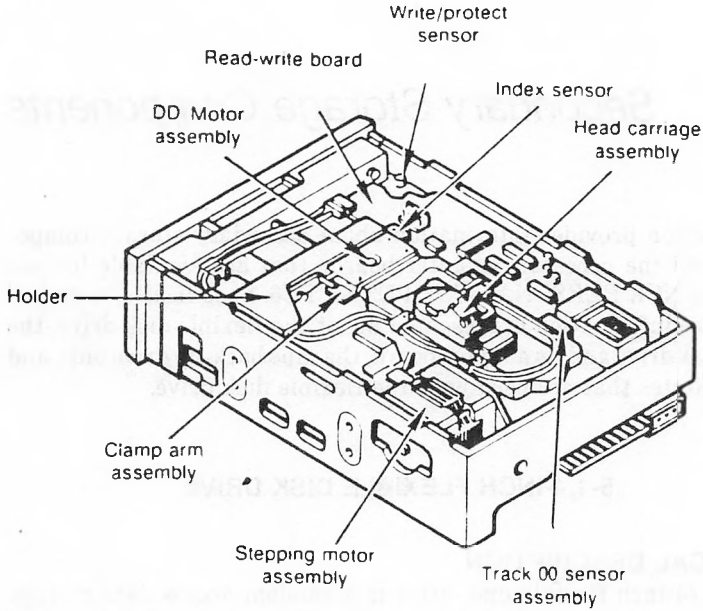
5-1/4-INCH FLEXIBLE DISK DRIVE

PHYSICAL DESCRIPTION

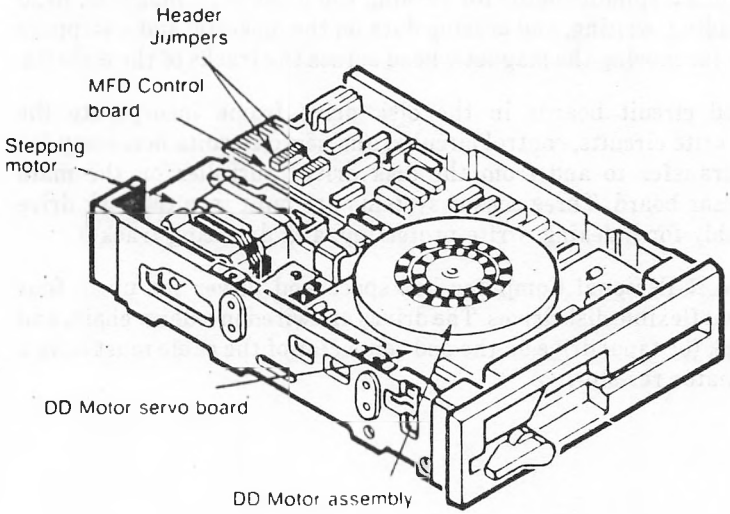
The 5-1/4-inch flexible disk drive is a random access data storage device that records data on 5-1/4-inch flexible magnetic diskettes in double-density format with modified frequency modulation. The drive has a spindle motor for turning the diskette; a magnetic head for reading, writing, and erasing data on the diskette; and a stepping motor for moving the magnetic head across the tracks of the diskette.

Printed circuit boards in the disk drive frame incorporate the read/write circuits, control circuits, and servo circuits necessary for data transfer to and from the disk drive controller on the main processor board. Three sensor systems are built into the disk drive assembly for indexing, write-protecting, and detecting track 0.

The NCR Personal Computer has space and power for up to four internal flexible disk drives. The drives are wired in a daisy chain, and the disk (or tape) drive on the end connector of the cable must have a terminator resistor.

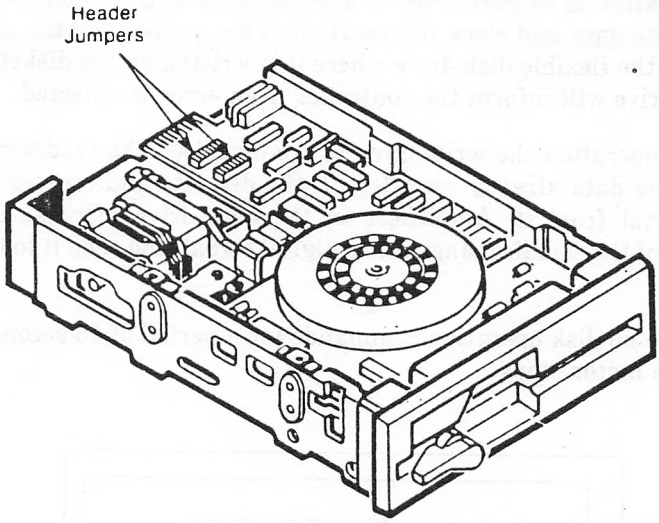


Top View

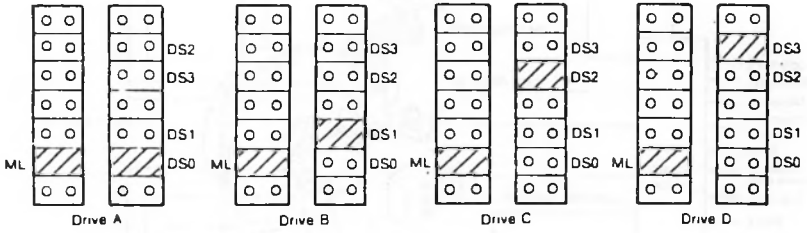


Bottom View

Flexible Disk Drive



Bottom View



Flexible Disk Drive Jumper Headers

The first flexible disk drive in the computer must be designated "Drive A", the second "Drive B", and so on.

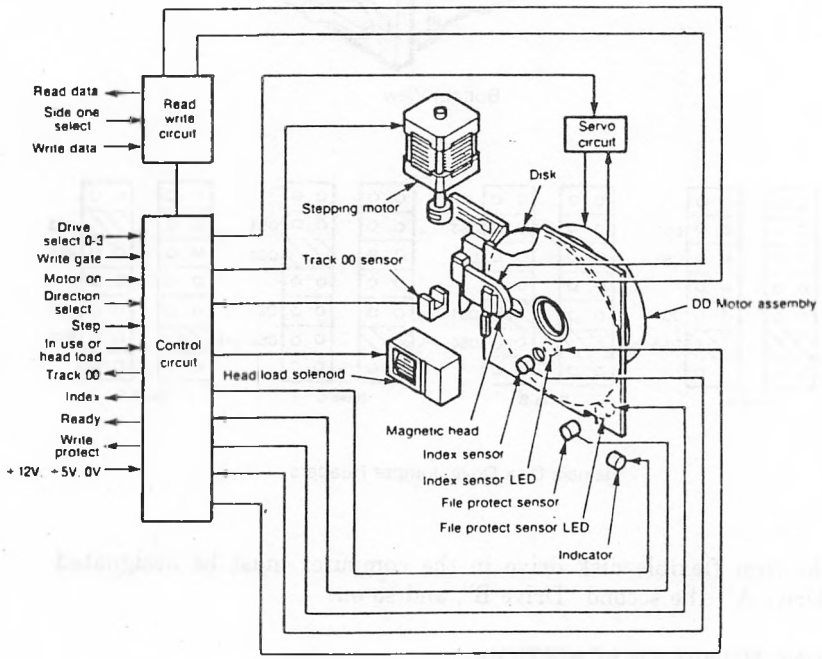
FUNCTIONAL DESCRIPTION

The flexible disk drive has two basic functions: write data on the flexible diskette and read data from the flexible diskette. When the diskette is installed and rotating at the prescribed 300 rpm, the drive sends a ready signal to the controller. The controller selects the drive and causes the read/write heads to move to the appropriate track on the diskette. Other signals select which of the two heads will be used and cause the heads to be loaded.

If the operation to be performed is a write operation, the controller arranges the data and clock information in the proper format, and sends it to the flexible disk drive where it is written on the diskette. The disk drive will inform the controller if an error is detected.

On a read operation the write circuits are disabled. The read/write head detects data already recorded on the diskette and creates an analog signal from it. Amplifiers in the disk drive increase the amplitude of the signal, change it to a digital signal, and send it to the controller.

If there are no disk operation commands for a period of 15 seconds, the spindle motor stops.



5-1/4-inch Flexible Disk Drive Block Diagram

Spindle

The collet and step arm assembly make up a mechanism that holds the diskette tightly against the spindle when the lever on the disk door is closed. The spindle motor turns the diskette at a constant 300 rpm.

Read/Write Heads and Head Carriage

The read/write magnetic heads, one for each side of the diskette, include a read/write gap for reading and writing data and two erase gaps for tunnel erasing. The magnetic head carriage is moved along the guide shafts by a four-stage motor through a steel belt. For each step instruction received from the controller, the motor turns two steps (for 48tpi) and causes the heads to move to the desired track.

Sensors

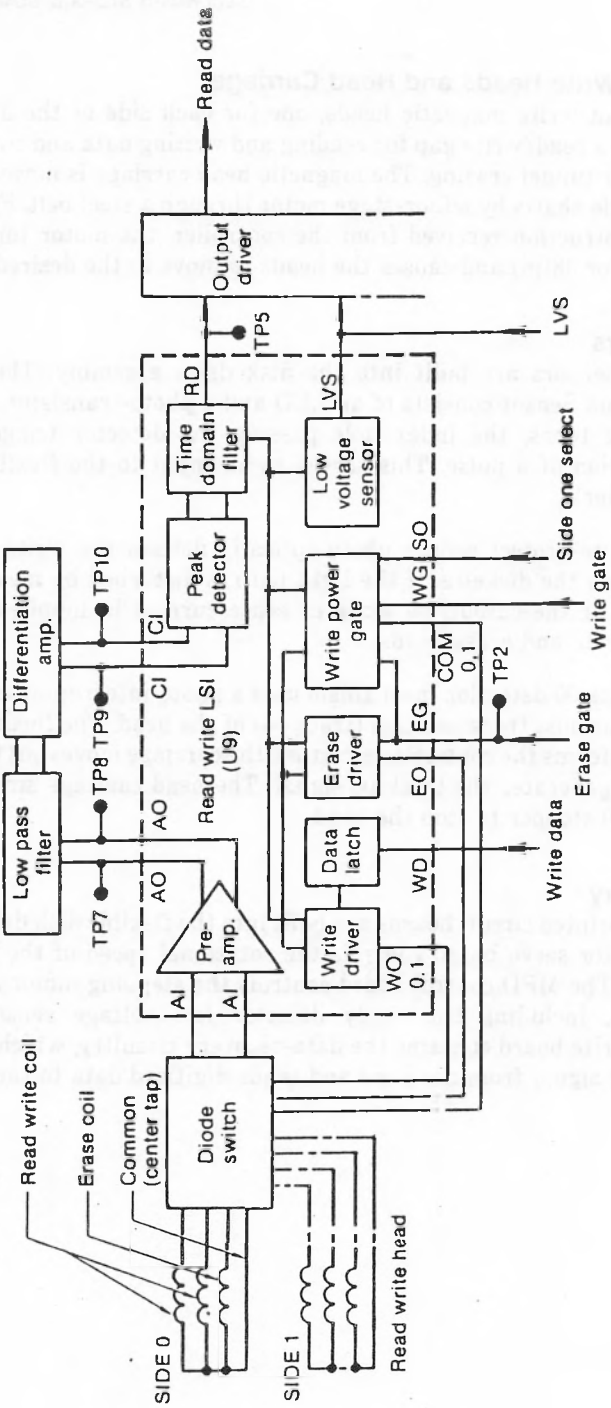
Three sensors are built into the disk drive assembly. The Index Detection Sensor consists of an LED and a photo-transistor. As the diskette turns, the index hole passing the detector triggers the generation of a pulse. This serves as an input to the flexible disk controller.

The write-protect sensor photo-optically detects the write-protect cutout on the diskette. If the light path is disturbed by means of a label over the cutout, no write or erase current is supplied to the read/write and erase heads.

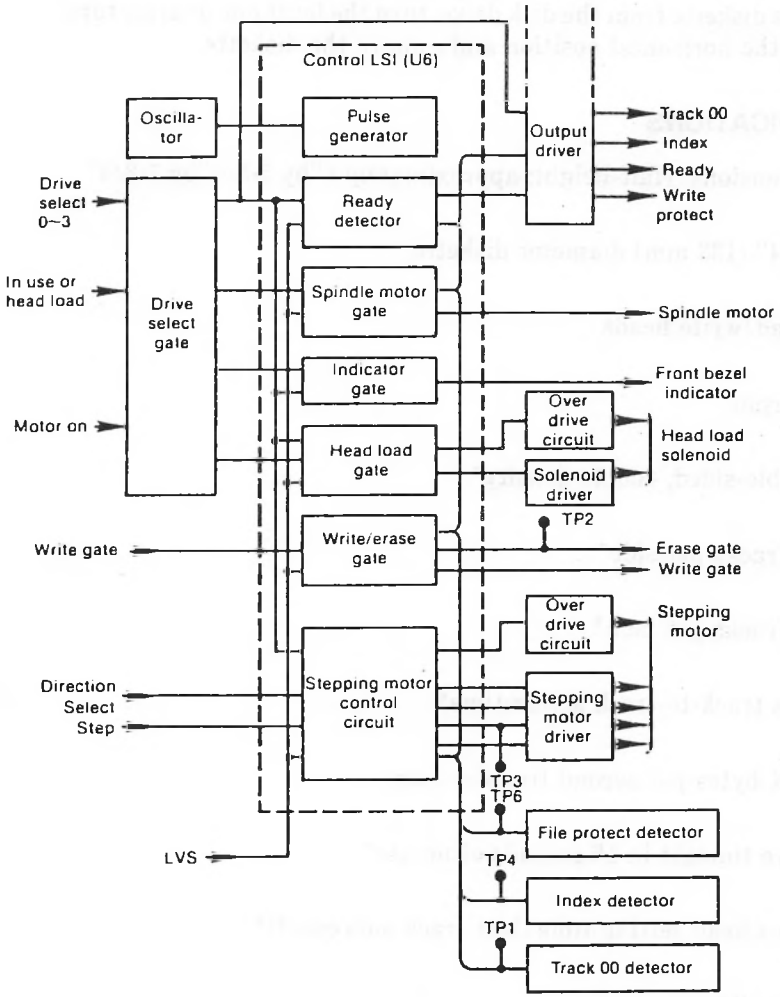
The track 00 detection mechanism uses a photo-interrupter to detect the outermost track position (track 00) of the head. The flexible disk drive informs the controller each time the carriage moves out to track 00 and generates the track 00 signal. The head carriage strikes the track 00 stopper to stop the head.

Circuitry

Three printed circuit boards are built into the flexible disk drive. The DD motor servo board controls the rotational speed of the spindle motor. The MFD control board controls the stepping motor and the sensors, including the ready detector low voltage sensor. The read/write board contains the data-recovery circuitry, which amplifies the signal from the head and sends digitized data to the MPB.



Read/Write Circuit Block Diagram



Control Circuit Block Diagram

OPERATION

The flexible disk drive receives operating instructions from the controller, so it requires no action by the operator except to load or unload the diskette. The set arm assembly lever should be in the open position when a diskette is not in the disk drive. After inserting the diskette in the slot, turn the lever one quarter turn clockwise. This moves the drive hub into position through the spindle access hole,

which centers the diskette and starts the spindle drive motor. To remove a diskette from the disk drive, turn the lever one quarter turn back to the horizontal position and remove the diskette.

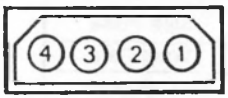
SPECIFICATIONS

- Dimensions: Half-height; approximately 8"by 5-3/4"by 1-3/4"
- 5-1/4" (133 mm) diameter diskette
- 2 read/write heads
- 300 rpm
- Double-sided, double-density*
- 40 Tracks per side*
- 48 Tracks per inch*
- 6 ms track-to-track access time*
- 250K bytes-per-second transfer rate
- Drive timeout in 15 seconds of no use*
- 15 ms head setting time (last track addressed)*
- Error Rate:
  1 per 10^9 (recoverable)
  1 per 10^{12} (non-recoverable)
  1 per 10^6 (seeks)
- Power:
  +12.2VDC ±0.6V, 900 mA average
  +5.2VDC ±0.25V, 600 mA average

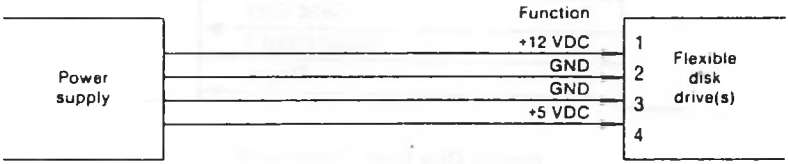
* Software-controlled by flexible disk drive controller on main processor board .

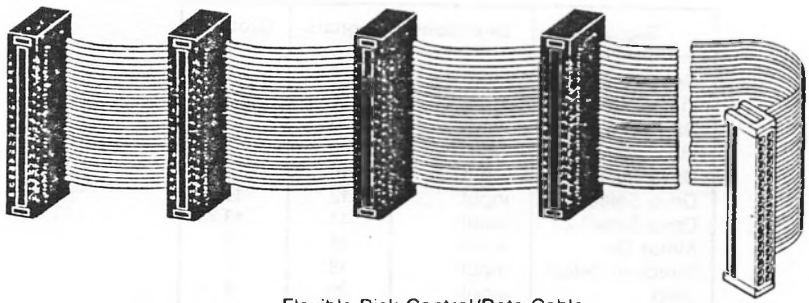
PHYSICAL CONNECTIONS/PIN ASSIGNMENTS

DC Power Connector

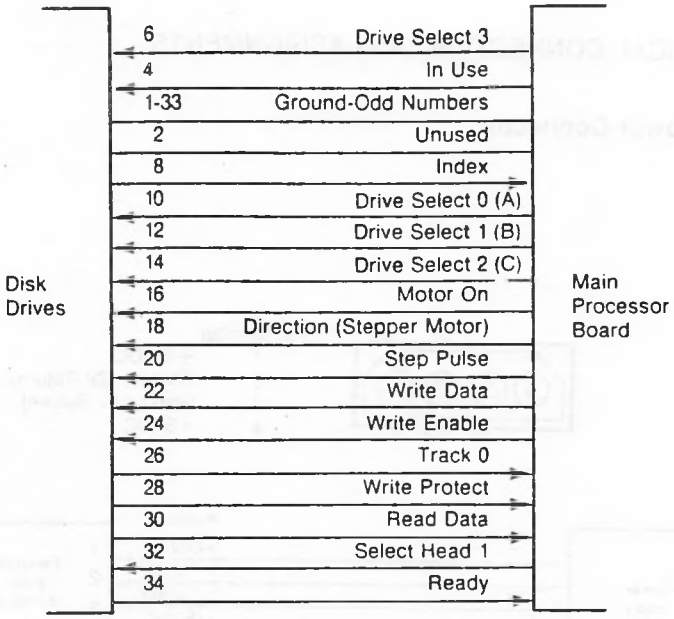


Pin Number	
1	+12VDC
2	GND (+12V Return)
3	GND (+5V Return)
4	+5VDC





Flexible Disk Control/Data Cable



Flexible Disk Drive Connections

Pin Assignments (at disk drive)

Signals	Directions	Signals	Ground
Reserved	Input	2	1
In Use	Input	4	3
Drive Select 3	Input	6	5
Index/Selector	Output	8	7
Drive Select 0	Input	10	9
Drive Select 1	Input	12	11
Drive Select 2	Input	14	13
Motor On	Input	16	15
Direction Select	Input	18	17
Step	Input	20	19
Write Data	Input	22	21
Write Gate	Input	24	23
Track 00	Output	26	25
Write Protect	Output	28	27
Read Data	Output	30	29
Side One Select	Input	32	31
Ready	Output	34	33

DISKETTES

PHYSICAL DESCRIPTION

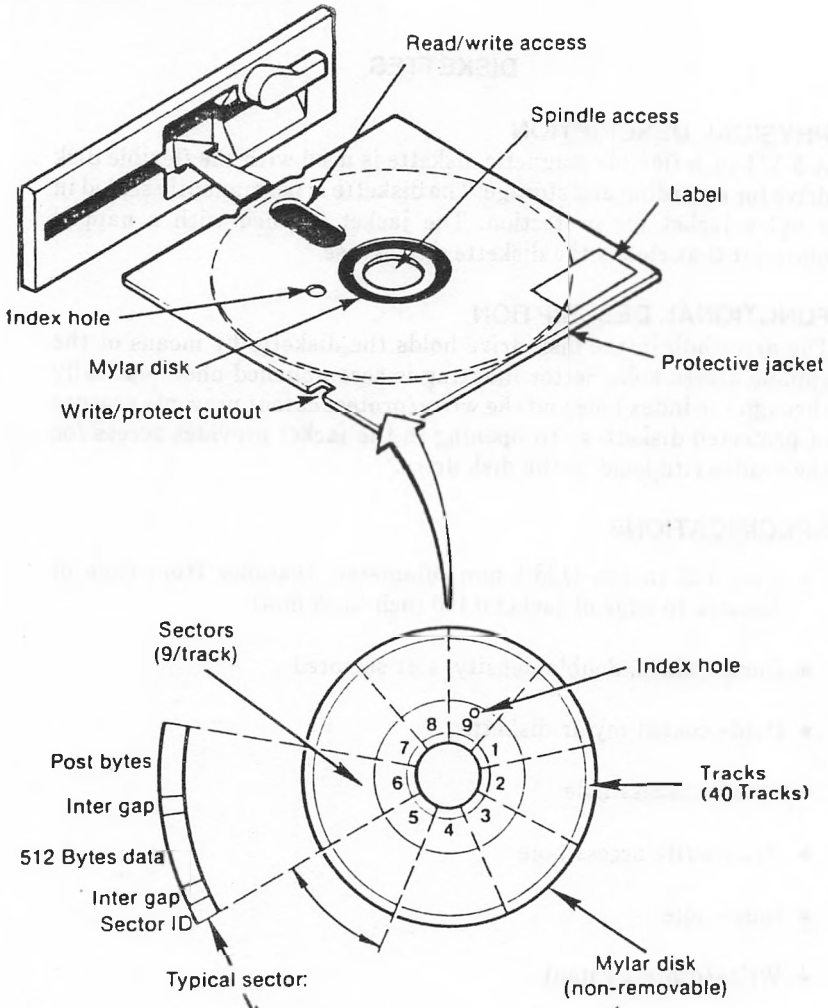
A 5-1/4-inch flexible magnetic diskette is used with the flexible disk drive for recording and storage. The diskette is permanently sealed in a nylex jacket for protection. The jacket is lined with a napped material that cleans the diskette during use.

FUNCTIONAL DESCRIPTION

The drive hub in the disk drive holds the diskette by means of the spindle access hole. Sector indexing is accomplished photo-optically through the index hole and the write/protect cutout prevents erasure of protected diskettes. An opening in the jacket provides access for the read/write head in the disk drive.

SPECIFICATIONS

- Size: 5.25 inches (133.4 mm) diameter. Distance from edge of diskette to edge of jacket:0.140 inch (3.56 mm)
- Double-sided, double-density, soft sectored
- Oxide-coated mylar diskette
- Spindle access hole
- Read/write access hole
- Index hole
- Write/protect cutout
- 48 tracks per inch (TPI)
- 40 tracks/surface
- 9 or 8 sectors to a track (360/328K bytes)
- 512 bytes per sector
- diskette layout
  Tracks 0-2 operating system
  Track 3 directory
  Tracks 4 — 79 user files

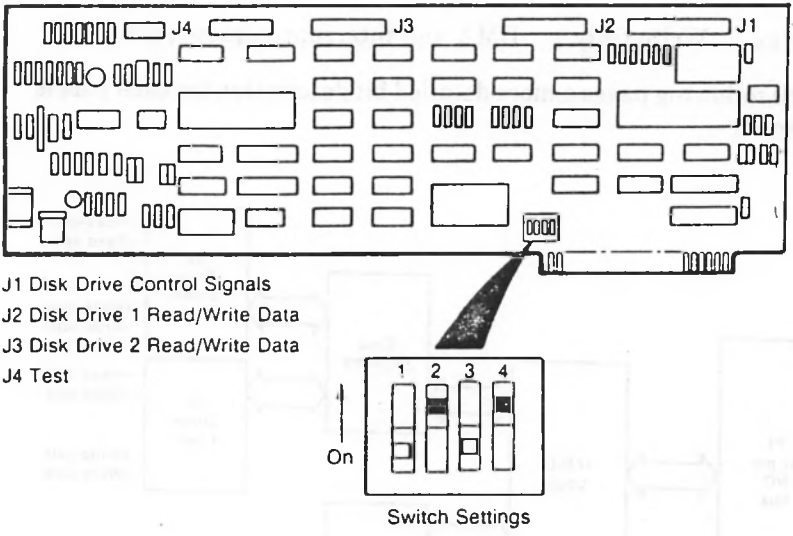


Typical Flexible Disk Track Format

FIXED DISK CONTROLLER BOARD

PHYSICAL DESCRIPTION

The fixed disk controller board is 13 inches by 4.2 inches. Four connectors are provided on this board. The 62-pin board edge connector provides for interface to the system board. Three other connectors consist of a 34-pin drive control connector (J1), and two 20-pin drive data connectors (J2 and J3).



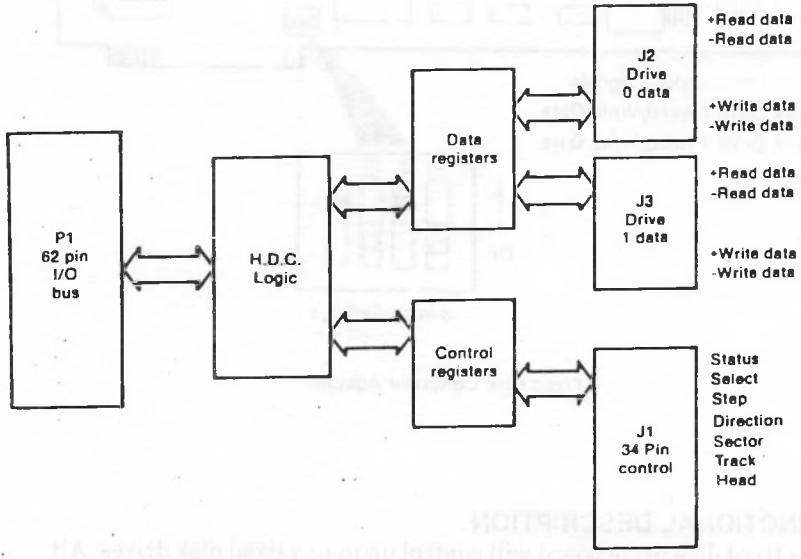
Fixed Disk Controller Adapter

FUNCTIONAL DESCRIPTION

The fixed disk drive board will control up to two fixed disk drives. All necessary receivers and drivers are included as well as address, data, and control circuitry buffering. There are two interface busses, a 20-bit address bus and an 8-bit bidirectional data bus. The main processor board accesses the controller through I/O ports as described on the next page:

Port		Function
320 Hex	Read	Data is read from the controller
	Write	Data is written to the controller
321 Hex	Read	Controller hardware status
	Write	Reset drive controller board
322 Hex	Read	Drive configuration byte
	Write	fixed disk drive controller select
323 Hex	Write Only	DMA and interrupt request port

On the following pages a more detailed bit description for each port is presented.



Functional Block Diagram

Read/Write Port 320 Hex

Bit	7	6	5	4	3	2	1	0
Data	d	d	d	d	d	d	d	d

When used as input, this port reads data from the drive; when used as an output it writes data to the drives.

BIT	FUNCTION
0	DATA
1	DATA
2	DATA
3	DATA
4	DATA
5	DATA
6	DATA
7	DATA

Read Status Port 321 Hex

Bit	7	6	5	4	3	2	1	0
Data	x	x	IRQ	DRQ	BSY	+C/-D	+I/-O	REQ

When Port 321 is read, the data bit meanings are as follows:

Bit	Bit Name	Function
0	REQ Request	Host and controller handshake bit. When active, (1) indicates that the controller is ready to transfer data to or from host.
1	+I/-O +Input -Output	Defines the direction for transfer between host and controller, from the host's point of view.
2	+C/-D +Control-Data	Indicates to the host which type of transfer the controller is expecting, either a command/status, or data transfer.
3	BSY Busy	Indicates the controller is busy executing a command.
4	DRQ DMA Request	Indicates the controller is ready for a DMA transfer, direction determined by bit 1.
5	IRQ Interrupt Request	Signifies an interrupt is pending.
6		Ignored
7		Ignored

Write Control Port 321 Hex

Bit	7	6	5	4	3	2	1	0
Data	x	x	x	x	x	x	x	x

Writing to Port 321 generates a hardware reset. When writing to this port the data byte written is ignored.

BIT	FUNCTION
0	Ignored
1	Ignored
2	Ignored

3	Ignored
4	Ignored
5	Ignored
6	Ignored
7	Ignored

Read Port 322 Hex

Bit	7	6	5	4	3	2	1	0
Data	x	x	x	x	config. drive 1	config. drive 1	config. drive 0	config. drive 0

This byte is read to determine the drive configuration.

BIT	FUNCTION
0	Configuration Drive 0
1	Configuration Drive 0
2	Configuration Drive 1
3	Configuration Drive 1
4	Ignored
5	Ignored
6	Ignored
7	Ignored

Write Port 322 Hex

Bit	7	6	5	4	3	2	1	0
Data	x	x	x	x	x	x	x	x

Writing to Port 322 when the controller is not busy selects the controller and prepares it to receive a command. The controller will respond to selection by setting the busy bit in the status register. Any data may be written to this port, since the controller ignores the data.

BIT	FUNCTION
0	Ignored
1	Ignored
2	Ignored
3	Ignored
4	Ignored
5	Ignored
6	Ignored
7	Ignored

Write Port 323 Hex

Bit	7	6	5	4	3	2	1	0
Data	x	x	x	x	x	x	IRQEN	DRQEN

This byte is a write only port.

Bit	Bit Name	Function
0	DRQEN	DMA request enable bit. When set, enables DMA requests to the host.
1	IRQEN	Interrupt request enable bit. When set, enables interrupts to the host.
2		Ignored
3		Ignored
4		Ignored
5		Ignored
6		Ignored
7		Ignored

SPECIFICATIONS

Drive Interfaces

Data encoding method:	MFM (Double-density)
Cylinders per drive:	Programmable to 1024
Bytes per sector:	512
Sectors per track:	17
Head selects:	8
Drive selects:	2
Data transfer rate:	5 m bits/sec
Write precompensation time:	12 nanoseconds

Main Processor Board Interface

Type: Board Edge	62-pin standard I/O channel
Power: + 5VDC @ 1.5 amps	Supplied via 62-pin connector

+ 12VDC @ 100 ma

Connectors

P1	62-pin board edge
J1	Drive control 34-pin
J2, J3	Drive 0 and drive 1 data connector
J4	Test connector

P1 Connections
62-Pin Card Edge Connector

B	FUNCTION	A	FUNCTION
1	GND	1	- I/O CHECK
2	+ RESET DRIVE	2	+ D7
3	+ 5V	3	+ D6
4	IRQ2	4	+ D5
5	- 5V	5	+ D4
6	+ DRQ2	6	+ D3
7	- 12V	7	+ D2
8	- HRQ I/O	8	+ D1
9	+ 12V	9	+ D0
10	GND	10	+ I/O CH RDY
11	- MEMW	11	+ BAEN
12	- MEMR	12	+ A19
13	- IOW	13	+ A18
14	- IOR	14	+ A17
15	- DACK3	15	+ A16
16	+ DRQ3	16	+ A15
17	- DACK1	17	+ A14
18	+ DRQ1	18	+ A13
19	- BDACK0	19	+ A12
20	+ BCLOCK	20	+ A11
21	+ IRQ7	21	+ A10
22	+ IRQ6	22	+ A9
23	+ IRQ5	23	+ A8
24	+ IRQ4	24	+ A7
25	+ IRQ3	25	+ A6
26	- DACK2	26	+ A5
27	+ T/C	27	+ A4
28	+ ALE	28	+ A3
29	+ 5V	29	+ A2 P1
30	+ OSC	30	+ A1
31	GND	31	+ A0 62 PIN

(-ASSERTS LOW) I/O

(+ASSERTS HIGH)

CARD BUS CONNECTIONS

Bus Expansion

Board Bus Connections

Sig. Gnd.	Sig. Pin	Signal Mnemonic	Signal Description
1	2	RWC-	Reduced Write Current-, when asserted with WG- reduces the write current to the drive for writing on inner disk cylinders.
3	4	HS 22	Head Select 22 is the most significant bit of the binary coded head select address.
5	6	WG-	Write Gate-, when asserted, allows write data to be written on the disk.
7	8	SC-	Seek Complete- signals that the heads have settled on the final track at the end of a seek.
9	10	TR 00-	Track 00- indicates that the heads are positioned on cylinder zero.
11	12	WF-	Write Fault- prohibits writing to the disk when a condition exists that may cause improper writing on the disk.
13	14	HS 20	Head Select 20 is the least significant bit in the binary coded head select address.
15	16	Reserved	
17	18	HS 21	Middle bit of the binary coded head select address.
19	20	INDEX-	Index- is asserted once per disk revolution, indicating the beginning of a track.
21	22	RDY-	Ready-, when asserted with SC-, indicates when the selected drive is ready to perform a read, write, or seek command.
23	24	STEP-	Step-, when asserted, causes the head selected to move in or out one track based on the state of DIRIN-.
25	26	DS 1-	Drive Select 1- indicates that drive #1 is to respond to the control signals on the disk drive control bus.
27	28	DS 2-	Drive Select 2- indicates that drive #2 is to respond to the control signals on the disk drive control bus.
29	30	Reserved	
31	32	Reserved	
33	34	DIRIN-	Direction In- indicates which direction the heads will move during a seek command (low = in,high = out).

Disk Drive Control Connector J1 Pin Description

Signal Pin	Signal Mnemonic	Signal Description
1	DSEL-	Not used.
2, 4, 6, 8, 11, 12, 15, 16, 19, and 20	GROUND	Data line ground returns.
3, 5, 7, 9, 10	Spare	
13	MFMWD+	MFM Write Data+ is MFM encoded write data to be written to the disk. This data must be precompensated for inner disk cylinders. The beginning cylinder for write precompensation is to be programmable. The amount of precompensation for both early and late bits should be 12 nsec. This line shall be disabled (Tri-stated) except when writing.
14	MFMWD-	MFM Write Data- is MFM encoded write data to be written to the disk. This data must be precompensated for inner disk cylinders. The beginning cylinder for write precompensation is to be programmable. The amount of precompensation for both early and late bits should be 12 nsec. This line shall be disabled (Tri-stated) except when writing.
17	MFMRD+	MFM Read Data+ is MFM encoded read data from the disk.
18	MFMRD-	MFM Read Data- is MFM encoded read data from the disk.

Disk Drive Data Connectors J2 and J3 Pin Description

Signal Pin	Description
1	Oscillator
2	GND
3	VCO In
4	GND
5	Delay Data
6	GND
7	N.C.
8	GND
9	N.C.
10	GND
11	N.C.
12	GND
13	N.C.
14	GND
15	Read Clock R
16	GND

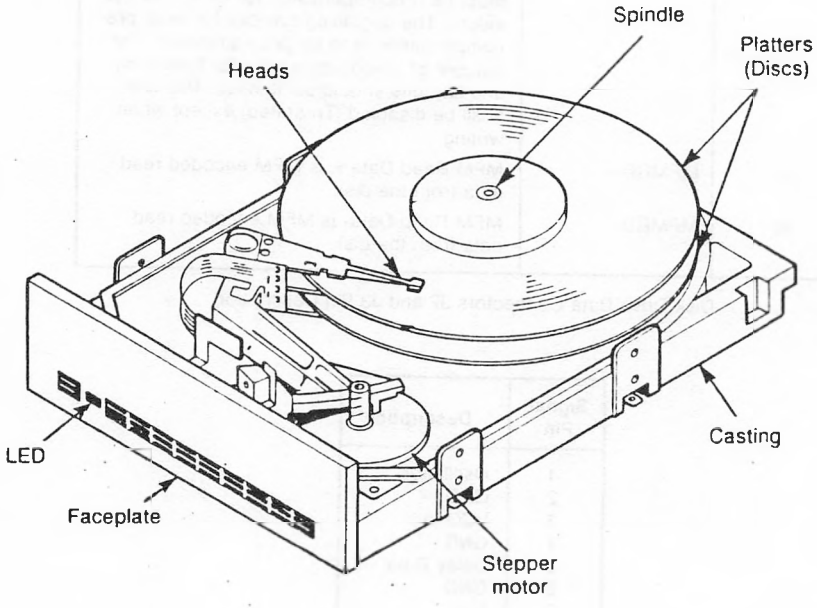
Disk Drive Test Connectors J4 Pin Description

FIXED DISK DRIVE

The NCR half-high 20MB disk Drive provides high density mass storage using the same voltages as the 5-1/4-inch flexible disk drive. The fixed 5-1/4-inch double platter stores data on four surfaces of 612 tracks each, 2,448 tracks total.

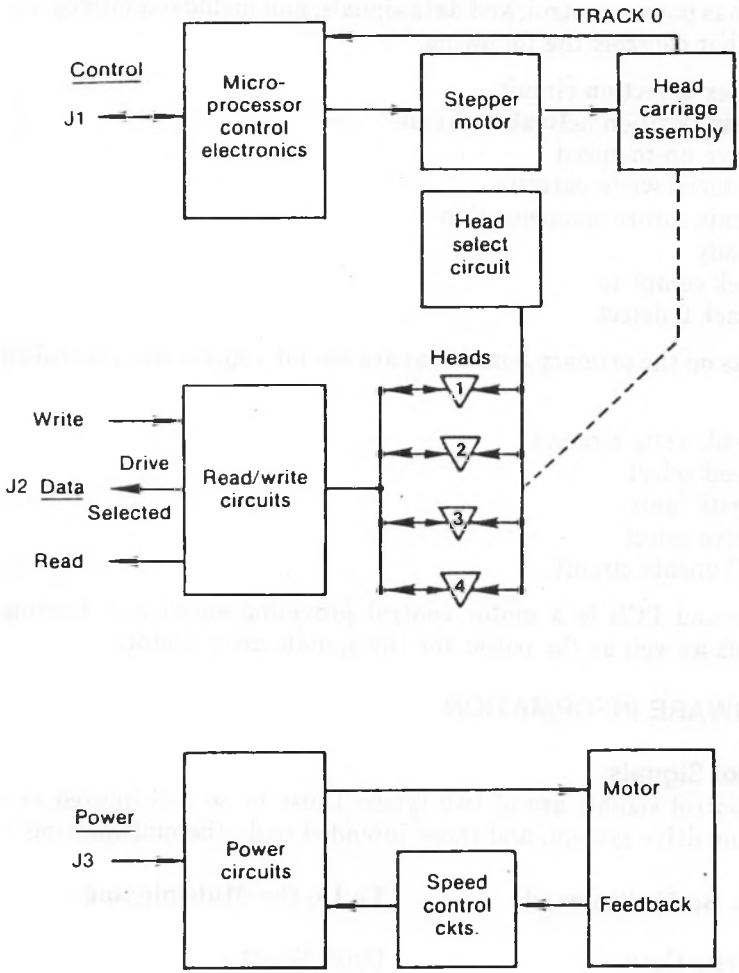
PHYSICAL DESCRIPTION

Enhanced reliability is provided by microprocessor electronic control and a band-actuated stepper mechanism. The two PC boards in the unit are mounted outside the head disk assembly (HDA) for ease of field servicing. A 0.3 micron air filter protects the heads, actuator, and disk platter from contamination. (The air filter is not a serviceable item.) A provision for air pressure equalization is built in.



Fixed Disk Assembly View .

NOTE: Although there are enough slots on the computer to install more than two fixed disks, it is not feasible to do so because the power supply can support no more than two fixed disks along with one or two flexible disk and tape drives.



Fixed Disk Block Diagram

FUNCTIONAL DESCRIPTION

The drive consists of read/write control electronics, read/write heads, a track positioning activator, a spindle motor, the disks and an air filtration system. These components: (1) interpret and generate control signals, (2) rotate the disks at a constant 3600 RPM, (3) position the heads, (4) read and write data, and (5) provide a contamination-free environment.

The electronics package is on two printed circuit boards. The primary board has power, control, and data signals, and includes a microprocessor that controls the following:

- Index detection circuit
- Head position activator circuit
- Drive up-to-speed
- Reduced write current
- Temperature compensation
- Ready
- Seek complete
- Track 0 detect

Circuits on the primary board that are not microprocessor controlled are:

- Read/write circuits
- Head select
- Write fault
- Drive select
- DC unsafe circuit

The second PCB is a motor control providing speed and braking controls as well as the power for the spindle drive motor.

HARDWARE INFORMATION

Control Signals

The control signals are of two types: Those to be multiplexed in a multiple drive system, and those intended to do the multiplexing.

To Be Multiplexed	To Do the Multiplexing
Write Gate	Drive Select 1
Head Select 2a0	Drive Select 2
Head Select 2a1	Drive Select 3
Head Select 2a2	Drive Select 4
Step	
Recovery Mode	
Direction In	

Data Signals

Data signals are differential in nature and may not be multiplexed. Two pairs of lines are provided at J2 connector and are selected to transfer data to and from the drive's read/write electronics in the drive.

To Drive	From Drive
+ MFM Write Data	+ MFM Read Data
- MFM Write Data	- MFM Read Data
Ground	- Drive Selected

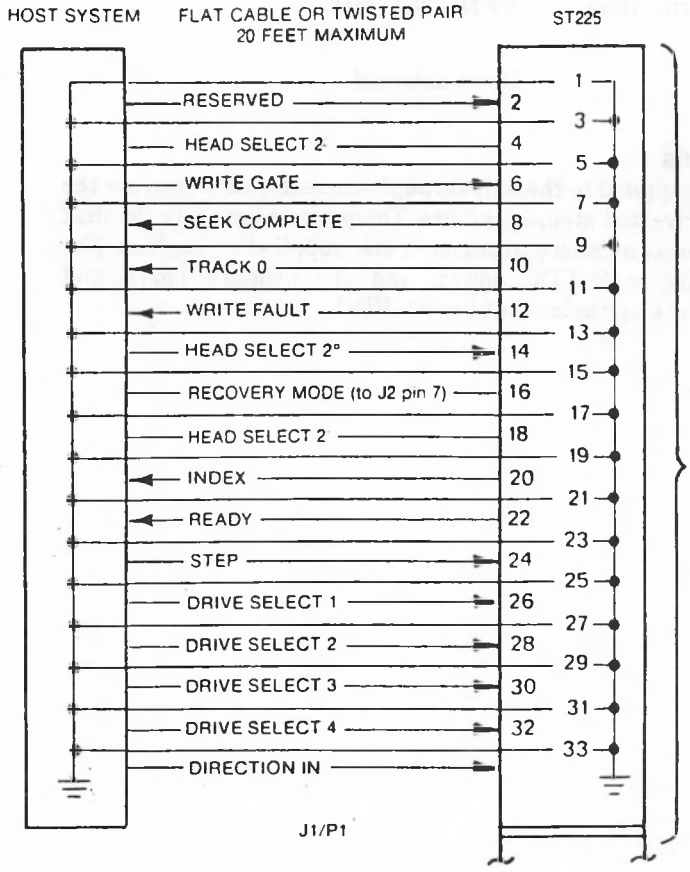
Power Signals

The power is supplied to the unit through connector J3 to operate the DC spindle drive and stepper motors. The power to operate the disk drive electronics and microprocessor is also supplied through J3. The motors require +12 VDC power, and the primary board and microprocessor electronics require +5 VDC.

To Drive
+ 5VDC
+ 12VDC
Ground

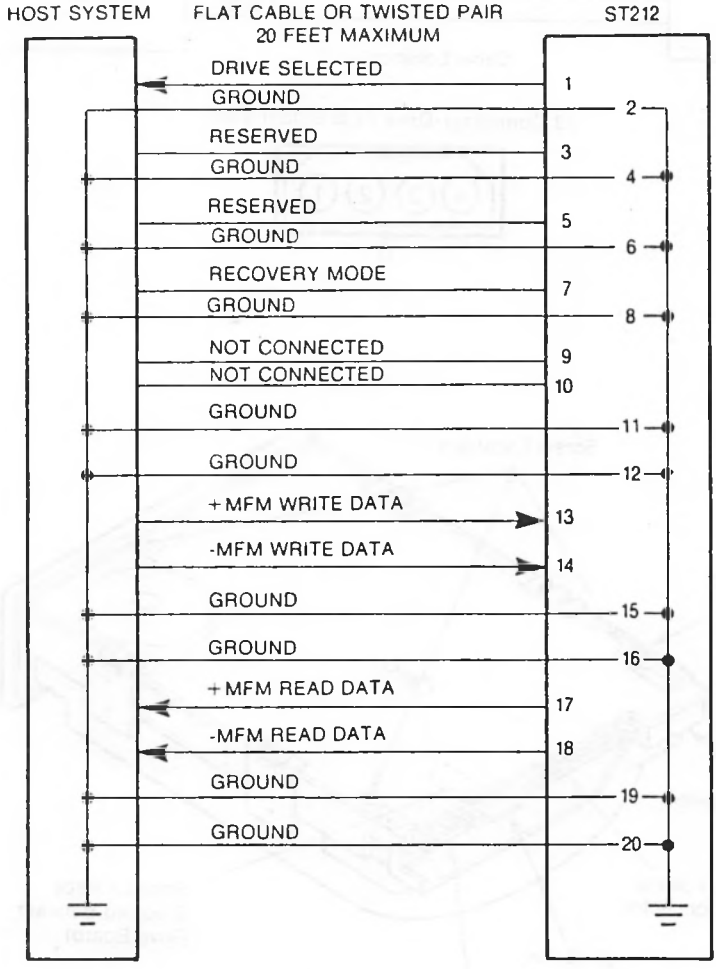
PHYSICAL CONNECTIONS/PIN ASSIGNMENTS

34-Pin Board Edge Connection (odd-numbered pins grounded)

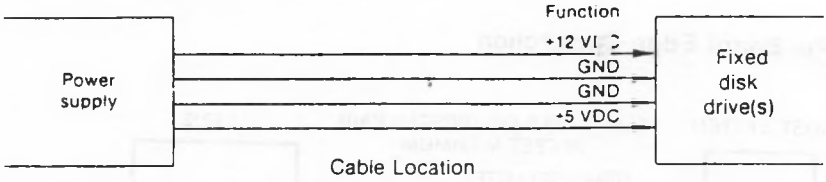


Fixed Disk Control Signals

20-Pin Board Edge Connection

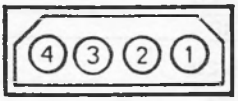


Fixed Disk Data Signals

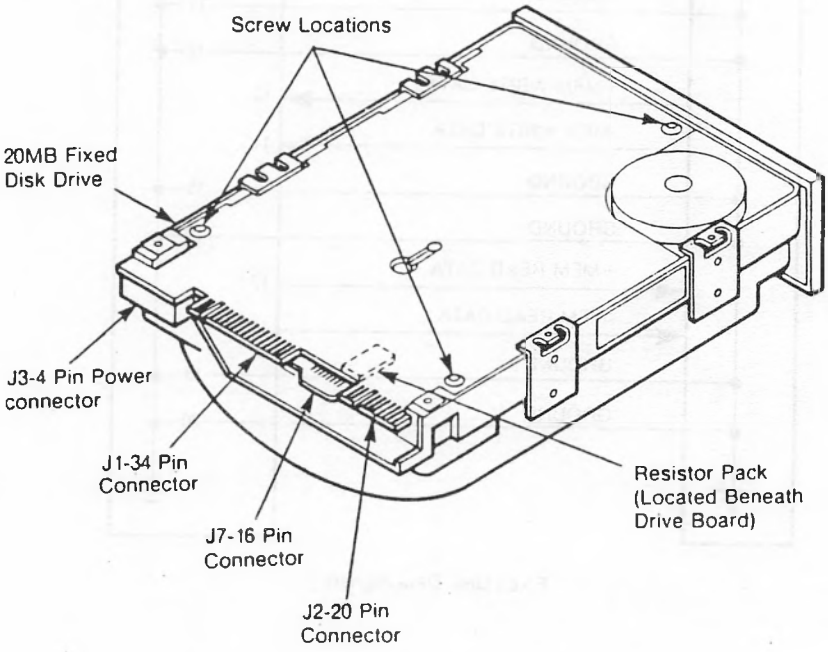


Cable Location

J3 Connector-Drive PCB Solder Side



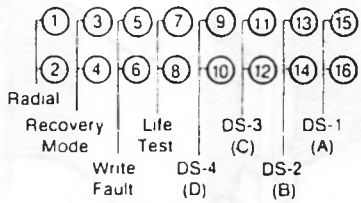
J3

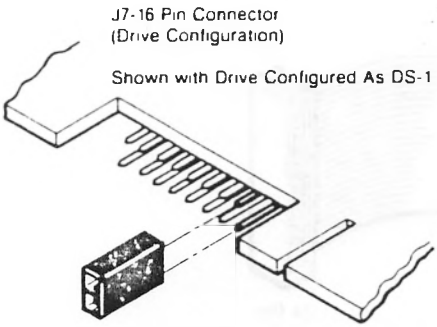


Fixed Disk Connectors

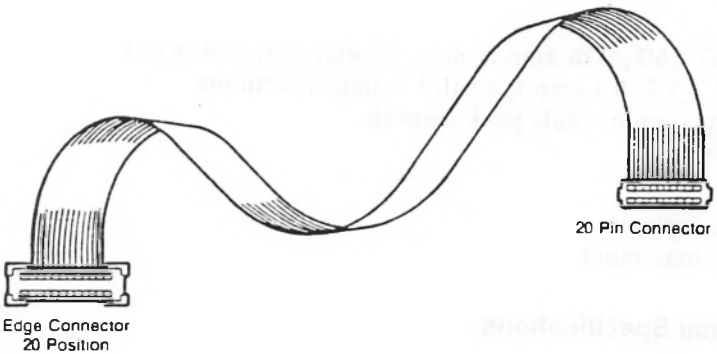
Drive Select Chart

Placing the jumper plug on the appropriate pair of pins on the designator connector, J7, determines which select line activates that drive. The following chart indicates which drive select pins must be connected by the jumper plug to assign the drive designation wanted:

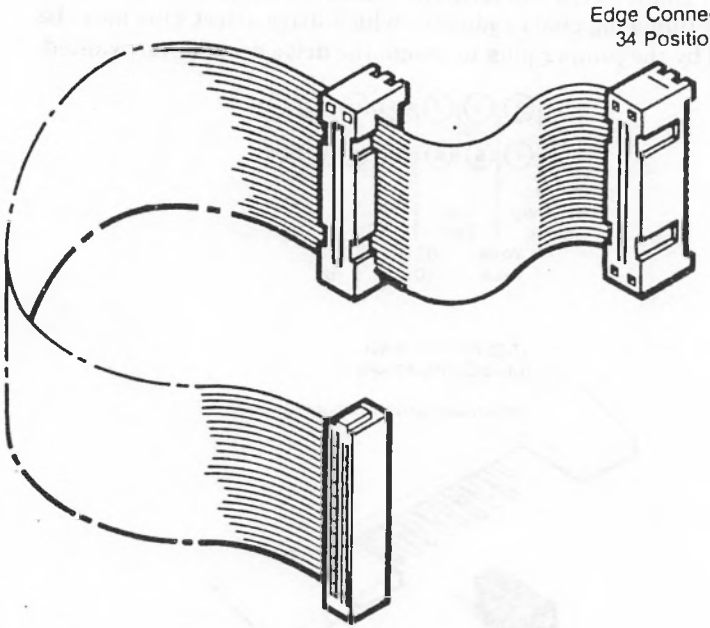




NOTE: The first fixed disk drive in the computer must be designated "Drive DS-1", the second "Drive DS-2". Drive DS-1 will then be automatically assigned one letter higher than the highest flexible disk drive letter above "B". Drive DS-2 will be automatically assigned the next higher letter above Drive DS-1.



Fixed Disk Data Cable



Fixed Disk Control Signal Cable

SPECIFICATIONS

DC Power

+ 12VDC ±5%, 0.75 amp typical, 2.5 amps (at power on)
+ 5VDC ±5%, 0.9 amp typical, 1.2 amps maximum
100mV maximum ripple peak-to-peak
(12/5 volts)

14 watts, typical
16 watts, maximum

Functional Specifications

Capacity per formatted drive 20.0 MB

Capacity per unformatted drive	25.52 MB
Capacity per formatted surface	5.0 MB
Capacity per unformatted surface	6.38 MB
Capacity per formatted track	8,192 bytes
Capacity per unformatted track	10,416 bytes

Performance Specifications

Rotational speed	3,600 RPM +-1%
Recording density	9,784 BPI
Flux density	9,784 FCI
Track density	588 TPI
Cylinders	612
Tracks	2,448
Read/write heads	4
Disks	2
Track-to-track access time	20 ms
Average access time	85 ms
Maximum access time	205 ms
Transfer rate	5.0 Mbits/sec
Average latency	8.33 ms

OPTIONAL STORAGE DEVICES

NCR provides a complete line of storage options. External fixed disk drives, built-in fixed disk drives, built-in and external tape drives, and external 8-inch flexible disk drives, allow the user to meet any storage requirement. Below is a list of the available NCR storage options along with the NCR option kit number:

Built-In Options

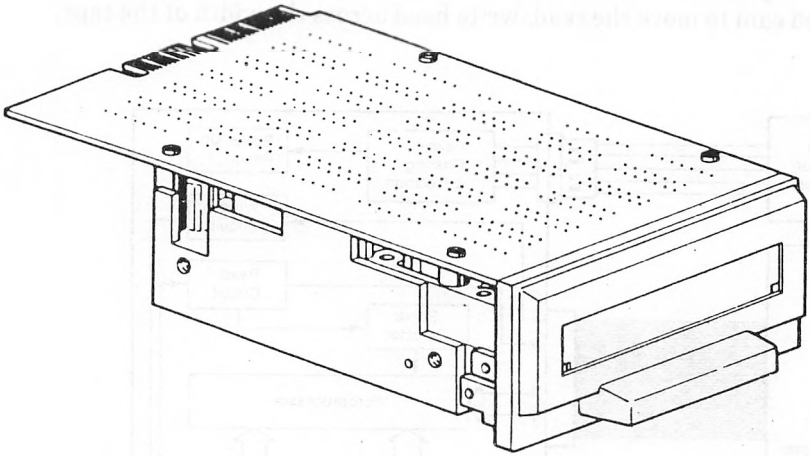
3285-K113	10MB FIXED DISK DRIVE
3285-K114	20MB FIXED DISK DRIVE
3285-K115	10MB BACKUP STREAMER TAPE
3285-K116	1.2MB FLEXIBLE DISK DRIVE
3285-K117	40MB FIXED DISK DRIVE
3285-K119	20MB BACKUP TAPE DRIVE

External Options

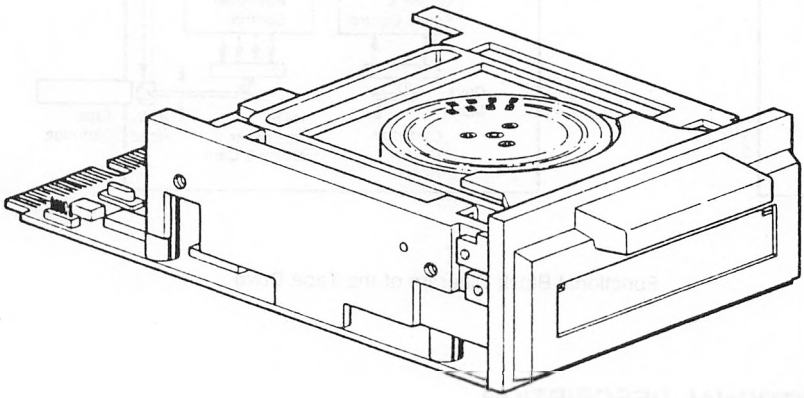
6097-4341	10MB WINCHESTER HARD DISK DRIVE
6097-4441	20MB WINCHESTER HARD DISK DRIVE
6097-6341	37MB WINCHESTER HARD DISK DRIVE
6097-6441	74MB WINCHESTER HARD DISK DRIVE
6097-7040	DATA BACK-UP TAPE DRIVE
6097-7141	10MB WINCHESTER W/TAPE DRIVE
6097-7241	37MB WINCHESTER W/TAPE DRIVE
6097-6561	DUAL 8" FLEXIBLE DISK DRIVE

TAPE CARTRIDGE DRIVE (Winchester Disk Back-Up System)

The NCR tape drive unit provides a reliable backup system for a Winchester fixed disk. It uses the same cabling and electrical power and control as the flexible disk drive units and can be mounted in one of the spaces for disk drives in the front panel of the computer. A diskette, provided with the unit, incorporates the software needed to read and write data on the tape.



Top view



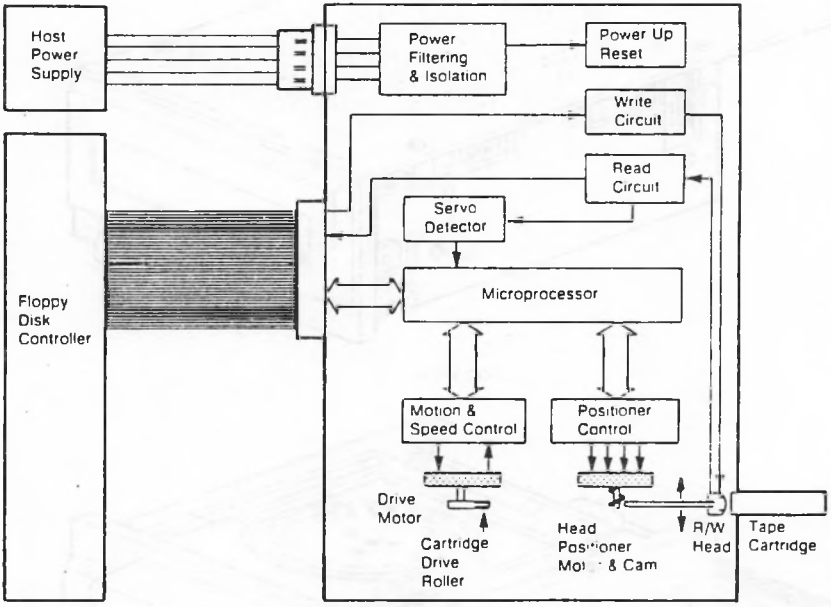
Bottom View

Tape Cartridge Drive

PHYSICAL DESCRIPTION

The tape drive unit is a tape recording drive that operates either as a mirror-image streamer or as a file selectable mode recorder to back up data that are stored on a Winchester disk. It uses the same cables used to control flexible disk drives and can be "daisy chained" with one or more such drives. The motion of the tape is provided through a capstan from a brushless DC drive motor and the motion of the

recording head is controlled by a separate motor which drives a spiral shaped cam to move the read/write head across the width of the tape.



Functional Block Diagram of the Tape Drive

FUNCTIONAL DESCRIPTION

The portion of the MPB which controls the flexible disk drives also controls the tape drive. It transmits commands to the drive over the same cable. Each command is a series of pulses transmitted at the standard 3 or 6 millisecond stepper pulse rate. The drive's command interpreter counts the number of pulses received during a command sequence and implements the command. Most of the commands deal with motion control or status reporting. Three commands control the mode of the drive; two switch between the data and the format mode, while the third invokes a program module that records a servo pattern on blank tapes.

The drive executes a number of motion commands that permit operation in either the streaming, mirror-image mode; or the start/stop, file-selectable mode. The tape's drive motor is controlled

by the built-in microprocessor, which uses precision counters to continuously monitor and adjust the speed of the drive motor.

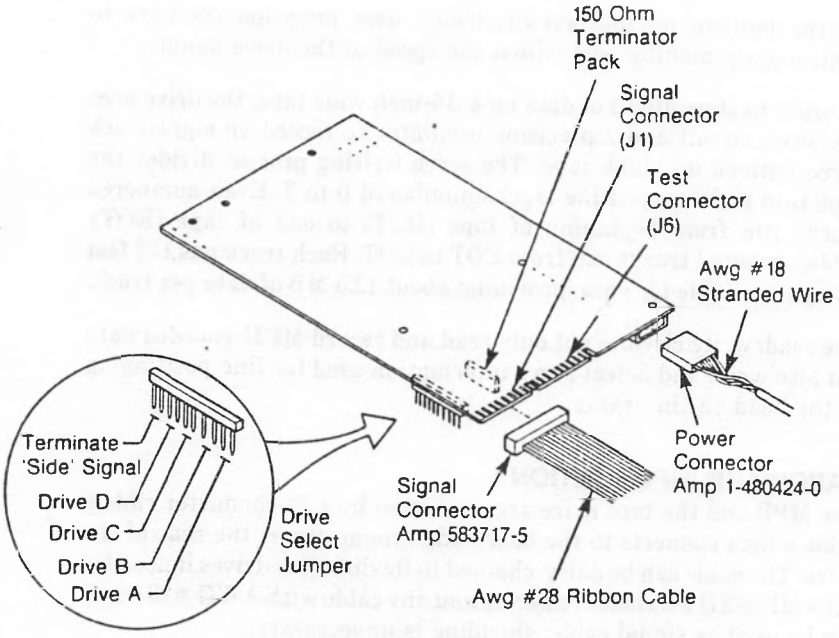
In order to store 10MB of data on a .15-inch wide tape, the drive uses the write circuit and a precision oscillator to record an eight-track servo pattern on blank tape. The servo writing process divides the tape into eight serpentine tracks numbered 0 to 7. Even-numbered tracks run from beginning of tape (BOT) to end of tape (EOT). Odd-numbered tracks run from EOT to BOT. Each track has 177 feet of tape available for data, providing about 1.25 MB of data per track.

The read/write circuits not only read and record MFM-encoded data but also write and detect servo information used for fine-positioning of the head on the tracks.

HARDWARE INFORMATION

The MPB and the tape drive are connected by a 34-conductor ribbon cable which connects to the board edge connector at the rear of the drive. The cable can be daisy-chained to flexible disk drives if need be. An AMP 583717-5 cable connector and any cable with AWG #28 wires can be used as signal cable; shielding is unnecessary.

The DC power connector connects to an AMP 641737-1 connector that is mounted parallel to the tape drive board at the rear. (See the following illustration.)



Tape Drive Connections

Cable Connections for Tape Drive

Any tape drive/flexible disk drive combination of up to four devices can be attached to the flexible disk controller on the MPB with the following restrictions:

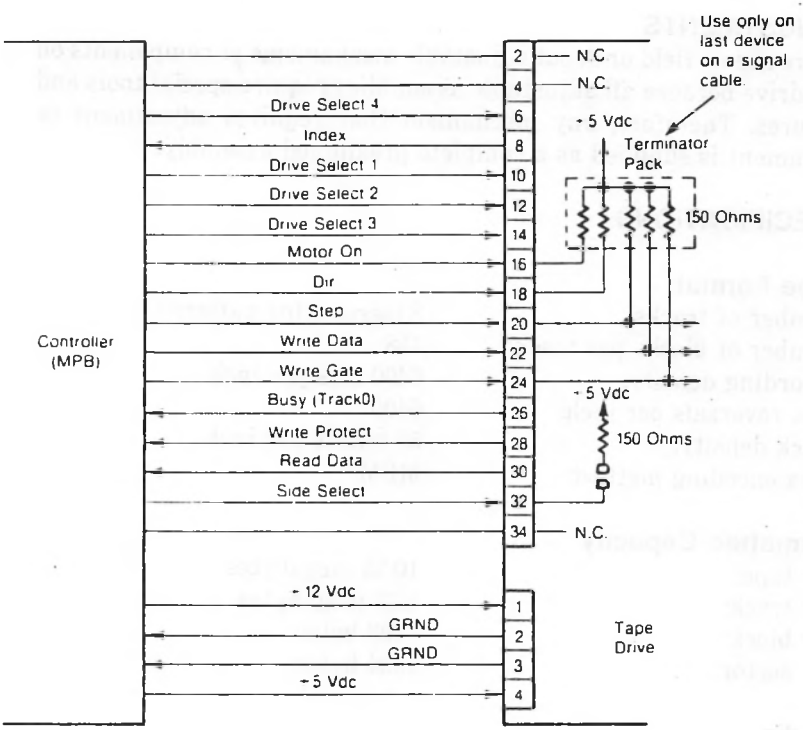
- Each unit on one cable must have a unique address.
- Total cable length must not exceed 10 feet.
- A terminator resistor pack must be installed on the drive on the last connector on the cable. Terminator resistors must be removed from any intermediate drives.

A device select jumper determines the address of the drive. The location of the jumper strap pin set is shown in the illustration for the cable connections, and the specific location of the drive select jumper is shown in the inset of that illustration.

Each drive is shipped with a jumper on the last two pins of the select set. If a select jumper is used and the device is in an intermediate position on the cable, remove this jumper. If the drive is the last or only device on the cable, leave this jumper in place.

Each drive is equipped with a 150-ohm terminator pack installed as shown in the illustration for the cable connections. If the drive is the last or the only device on the signal cable, leave the terminator pack in place; if the drive is an intermediate device, remove the pack.

The following chart shows the pin assignments on the signal cable connector:



Tape Drive Signals

MAINTENANCE

The only maintenance that should be performed on the drive outside of the factory is the periodic cleaning of the read/write head. This should be done at least once every six months to remove any oxide build-up accumulated through use. The head is accessible from the front through the flip-up door where the cartridge is inserted, so that

the drive can be cleaned without removing the assembly from the computer.

Use isopropyl alcohol on a nonabrasive, nonlinting, cotton-tipped applicator to clean the head. Do not use ordinary hygenic cotton applicator swabs because they leave lint on the head. After you clean the head with alcohol, allow the residual moisture to evaporate before using the drive.

ADJUSTMENTS

There are no field or depot adjustable mechanisms or components on the drive because all adjustable assemblies require special tools and fixtures. Therefore, any mechanism that requires adjustment or alignment is supplied as a complete prealigned assembly.

SPECIFICATIONS

Tape Format

Number of tracks:	8 (serpentine pattern)
Number of blocks per track:	158
Recording density:	6400 bits per inch
Flux reversals per inch:	6400
Track density:	59 tracks per inch
Data encoding method:	MFM

Formatted Capacity

Per tape:	10.35 megabytes
Per track:	1.29 megabytes
Per block:	8192 bytes
Per sector:	1024 bytes

Media

Type:	DC-600 media in DC-100A size cartridge
Width:	0.15 inch
Length:	185 feet

Performance Characteristics

Read/write modes supported:	streaming (mirror image) start/stop (file selectable) random access (file update)
Time to dump/restore 10 megabytes of data:	8 minutes in streaming mode, single pass.

Electrical interface:	standard flexible disk
Disk controller:	NEC 765 and FE 2100
Data transfer rate:	250,000 bits per second
Tape speed	
Read/write operations:	39 inches per second
Reverse/fast forward:	70 inches per second
Maximum speed variation	
Instantaneous (ISV):	3.5 percent
Long term:	1.5 percent
Start/stop time	400 milliseconds
Head positioning time:	
Adjacent tracks:	250 milliseconds
Maximum:	1 second
End-to-end positioning time	
Read/write speed:	57 seconds
Reverse/fast forward speed:	31 seconds

Reliability

Error rate	
Soft error:	1 in 10^9 bits read
Hard error:	1 in 10^{11} bits read
Seek error:	1 in 10^6 seeks
Mean time between failures:	12,000 hours
Mean time to repair:	30 minutes
Preventive maintenance:	Clean head every 6 months
Shock	
Operating:	0.5 G at 5 to 55 Hertz
Not operating:	3 G at 5 to 200 Hertz

Power Requirements

+12 volts DC	
Tolerance:	within 5 percent
Current	
Average:	1 ampere
Surge (400 ms):	3.5 ampere
Total power dissipation:	14.5 watts

Optional Equipment

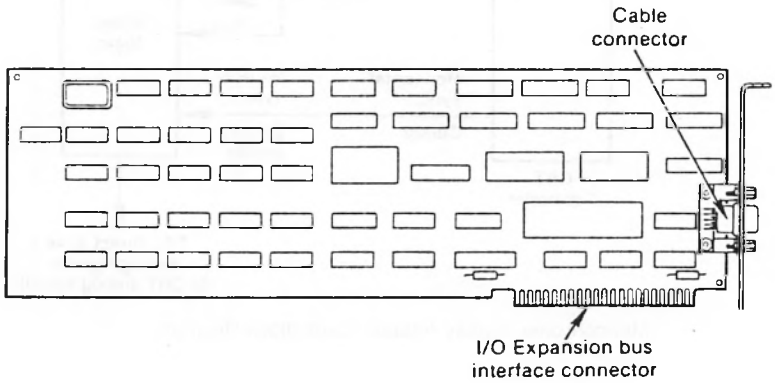
The sections in this chapter contain technical reference information about the equipment offered as options with the NCR PERSONAL COMPUTER PC6.

MONOCHROME DISPLAY ADAPTER BOARD

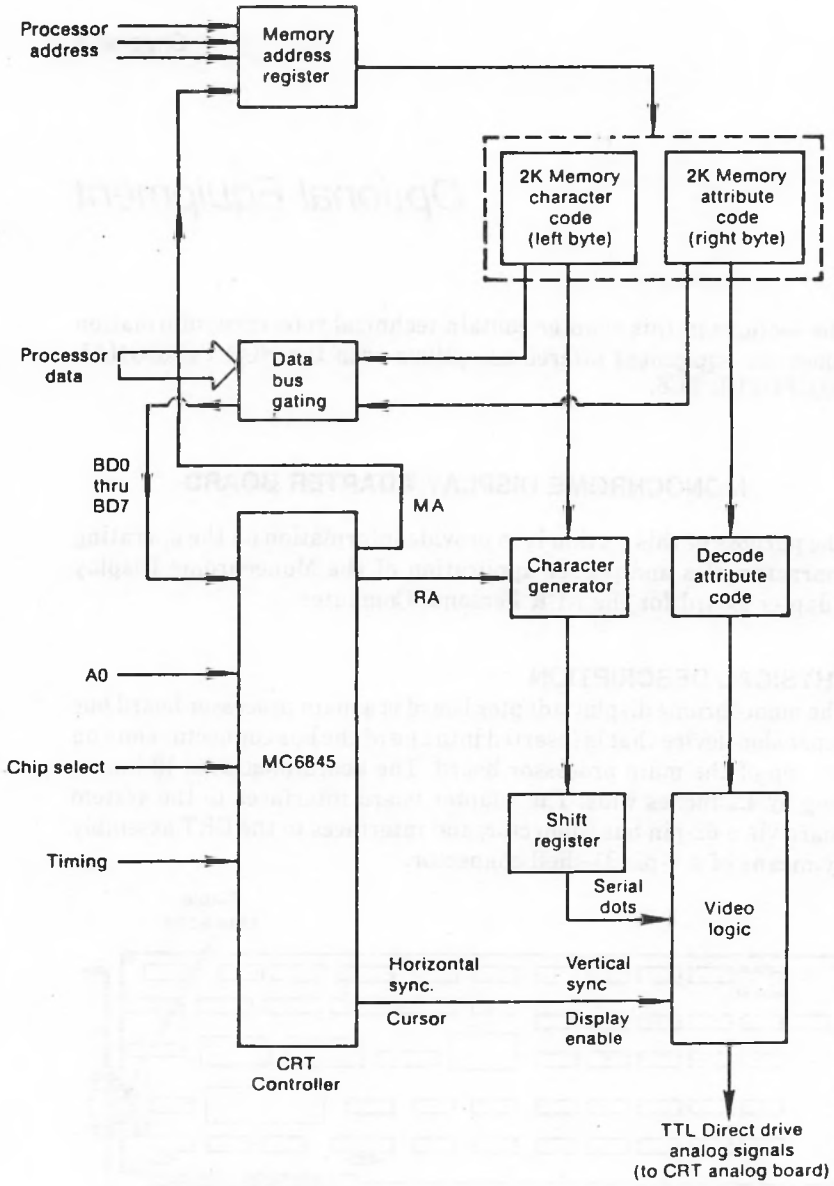
The purpose of this section is to provide information on the operating characteristics and proper application of the Monochrome Display Adapter Board for the NCR Personal Computer.

PHYSICAL DESCRIPTION

The monochrome display adapter board is a main processor board bus expansion device that is inserted into one of the bus connector slots on the top of the main processor board. The board measures 13 inches long by 4.2 inches wide. The adapter board interfaces to the system board via a 62-pin bus connector, and interfaces to the CRT assembly by means of a 9-pin D-shell connector.



Monochrome Display Adapter Card



Monochrome Display Adapter Card Block Diagram

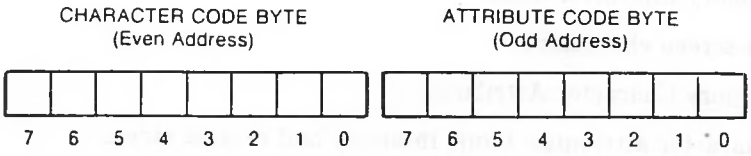
FUNCTIONAL DESCRIPTION

This adapter board is inserted into one of the bus expansion I/O connectors on the main processor board. It will drive one mono-

chrome display device. The outputs to the analog board of the video display are routed to a 9-pin video cable connector mounted on the adapter board mounting bracket.

The adapter board accepts digital signal information from the main processor board bus and, by decoding these signals, generates the proper analog signals necessary to drive the analog board of a raster-scan monochrome CRT.

The character information stored in the character code memory of the adapter board is in the form of ASCII codes. A character generator ROM is used to convert the ASCII codes to the dot patterns that form each character. Each of the 256 characters produced by the character generator is one byte in length and has an attribute byte associated with it. The attribute byte is capable of being controlled separately so each character can have multiple display features.



The analog signals for each displayed character and its attributes are transmitted to the monochrome CRT analog board 50 times each second to refresh the display. Using a 9 x 14 pixel matrix with a 7 x 9 character matrix cell, the board's 4K byte ROM character generator provides 256 resident character codes. This character generator provides the features listed below.

The character generator provides:

- Upper-case alphabetic characters
- Lower-case alphabetic characters with descenders
- Punctuation and special characters such as *, $, @, #, \, /, [,], etc.
- Numeric characters
- Special foreign language characters
- Block graphics using the 9 X 14 matrix

The complete character set with their associated values are listed in Appendix A, Character Set and Color Attributes.

OPERATING CHARACTERISTICS/SPECIFICATIONS

Operating Characteristics

The monochrome display adapter board operates under total software control, supporting:

- Reverse video
- Intensity (brightness)
- Character blink and rate of blink
- Underscoring

CRT Display: 80 character columns x 25 lines (one screenful)

ROM Character Generator: 4K bytes (256 Character Codes)

- Character matrix: 7 x 9 pixels
- Block graphics matrix: 9 x 14 pixels

2K Memory Character Codes

- On-screen characters

2K Memory Character Attributes

- Character attributes: blink, intensity and reverse video.

Specifications

- Nominal dimensions = 13 inches long, 4.2 inches wide
- Cathode ray tube (CRT) controller IC = Motorola MC6845
- 4K ROM character generator providing 256 resident character patterns
- 62 contact main processor board bus expansion connector
- DB-9 video cable connector
- Power requirement = +5VDC @ 1.0 Amp (maximum)

Input signal operating ranges are as follows:

Video Input

- level low: 0 to 0.4V
- level high: 3V (typical)

Horizontal Drive

- Level low: 0 to 0.4V
- Level high: 3V (typical)

Vertical Drive

- Level low: 0 to 0.4V
- Level high: 2.00 to 5.25V
- Display Buffer Memory: 4K bytes
- Dot Clock Frequency: 16.257MHz
- Sweep Rates: 18.432KHz (horizontal); 50Hz (Vertical), which provides a screen refresh rate of 50Hz
- Logic Levels: TTL compatible
- Power Requirement: +5VDC ±0.5V at 1.0A (max.)

ASSOCIATED SOFTWARE INFORMATION

Attribute Byte

The possible bit patterns of the attribute byte are shown in the following illustration:

	Attribute Byte							
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
No Display	any	0	0	0	any	0	0	0
Underline	any	0	0	0	any	0	0	1
Normal Video	any	0	0	0	any	1	1	1
Reverse Video	any	1	1	1	any	0	0	0
Blink	1	any	any	any	any	any	any	any
Intensity (High)	any	any	any	any	1	any	any	any

Switch Settings

The switch settings on the main processor board for systems using a monochrome display adapter board should have positions 5 and 6 on S1 (located on the main processor board) set to OFF (OPEN). Refer to Appendix C, Switch Configurations, in this manual.

Internal Register Information

Software control of the monochrome display adapter board is possible by accessing the internal registers of 6845 through the Input/Output ports.

The starting memory address of the adapter board is B000 (hex). The Input/Output address for the adapter board is 3B0 (hex) to 3BF (hex).

The I/O Port assignments for the monochrome adapter board are:

- 3B4 (hex) = CRT Controller Index Register
- 3B5 (hex) = CRT Controller Data Register
- 3B8 (hex) = CRT Controller Port

  Bit 0 = (1) High Resolution Mode

  Bit 1 = (unassigned)

  Bit 2 = (unassigned)

  Bit 3 = (1) Video Enable

  Bit 4 = (unassigned)

  Bit 5 = (1) Blink Enable

  Bit 6 = (unassigned)

  Bit 7 = (unassigned)
- 3BA (hex) = CRT Status Port

  Bit 0 = (1) Horizontal Drive Enable

  Bit 1 = (not available)

  Bit 2 = (not available)

  Bit 3 = (1) Monochrome Video Enable

  Bit 4 = (unassigned)

  Bit 5 = (unassigned)

Bit 6 = (unassigned)

Bit 7 = (unassigned)

The following diagram illustrates the internal register assignments of the 6845 controller chip on the adapter board:

Register Number	Parameter Affected	Register Address Value in Hex
R0	Horizontal Total	61
R1	Horizontal Displayed	50
R2	Horizontal Sync. Position	52
R3	Horizontal Sync. Width	0F
R4	Vertical Total	19
R5	Vertical Total Adjust	06
R6	Vertical Displayed	19
R7	Vertical Sync. Position	19
R8	Interlace Mode	02
R9	Max Scan Line Address	0D
R10	Cursor Start Scan Line	0B
R11	Cursor End Scan Line	0C
R12	Start Address (High)	XX
R13	Start Address (Low)	XX
R14	Cursor Address (High)	XX
R15	Cursor Address (Low)	XX
R16	Reserved	—
R17	Reserved	—

Chart of Internal Registers & Addresses

PHYSICAL CONNECTIONS/PIN ASSIGNMENTS

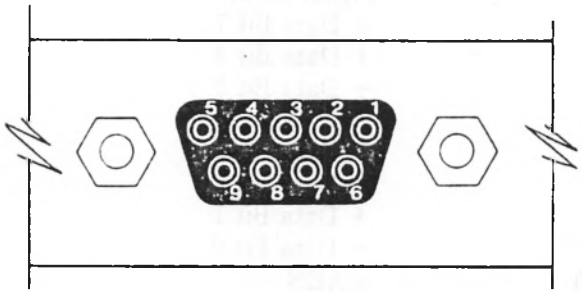
The monochrome display adapter board is connected to the system by inserting the 62-pin board-edge connector of the adapter board into one of the empty expansion slots on the main processor board. Refer to the illustration on page 3-1 of this manual to see how the board and its connector are arranged.

Video Signals

The monochrome display adapter board connects to the video display unit by means of a female 9-pin D-shell connector located on the board support bracket. This connector accepts the male video cable connector from the analog board of the monochrome display device.

Physical Connections/Pin Assignments

The analog signals output from the adapter board are assigned to the D-connector pins of the video cable:



Monochrome Display Adapter — Output Connection

Monochrome display adapter card	Pin	Function	Monochrome display
	1	Ground	
	2	Ground	
	3	(Not used)	
	4	(Not used)	
	5	(Not used)	
	6	+Intensity	
	7	+Video	
	8	+Horizontal drive	
	9	+Vertical drive	

CAUTION

Many third-party CRT monitors are claimed to be TTL compatible but have input circuits which require the controller chip on the adapter board to exceed the maximum drive current rating of the video circuits. The adapter board outputs are three direct-drive signals and CRT's using a composite video input (one signal line and one ground) are incompatible with the output lines (vert., horiz., video, and ground) of the adapter board.

BUS SIGNALS

The following signals are input to the monochrome display adapter board:

BUS CONNECTOR PIN	BUS SIGNAL
A1	17(not used)
A2	+ Data Bit 7
A3	+ Data Bit 6
A4	+ Data Bit 5
A5	+ Data Bit 4
A6	+ Data Bit 3
A7	+ Data Bit 2
A8	+ Data Bit 1
A9	+ Data Bit 0
A10	+AEN
A11	+A19
A12	+A18
A13	+A17
A14	+A16
A15	+A15
A16	+A14
A17	+A13
A18	+A12
A19	+A11
A20	+A10
A21	+A9
A22	+A8
A23	+A7
A24	+A6
A25	+A5
A26	+A4
A27	+A3

A28	+A2
A29	+A1
A30	+A0
B1	Ground
B2	+ Reset
B3	+ 5V
B4 thru B8	(not used)
B9	+ 12V
B10	Ground
B11	- Memory Write
B12	- Memory Read
B13	- I/O Write
B14	- I/O Read
B15 thru B19	(not used)
B20	Clock
B21 thru B28	(not used)
B29	+ 5V
B30	+ 5V
B31	Ground

MONOCHROME VIDEO DISPLAY

The NCR Personal Computer Monochrome Display, Option Kit 3285-K150, is a solid-state, raster-scan CRT display. The display is divided into a rectangular grid of many small picture elements (pixels). An analog circuit board interfaces with the display and activates an electron beam. The beam travels through a standard pattern of scan lines that fills the entire screen. When energized, the beam scans the phosphor surface of the tube causing the CRT screen dots to glow. Illuminated pixels form alphanumeric dot or graphic characters on the screen.

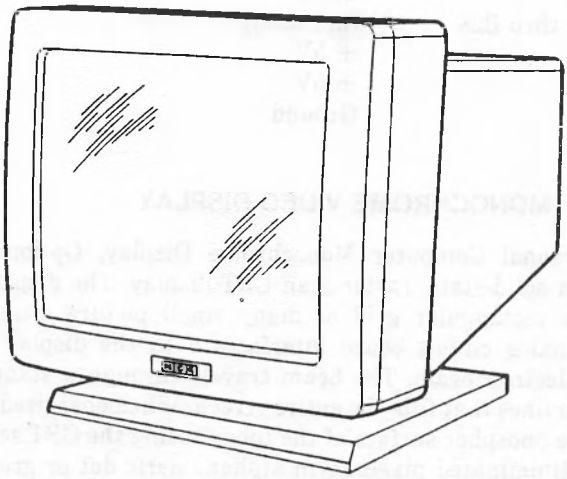
Two cables connect the display to the computer: a signal cable, which connects the adapter board to the display; and a power cable, which provides AC power from the computer.

PHYSICAL DESCRIPTION

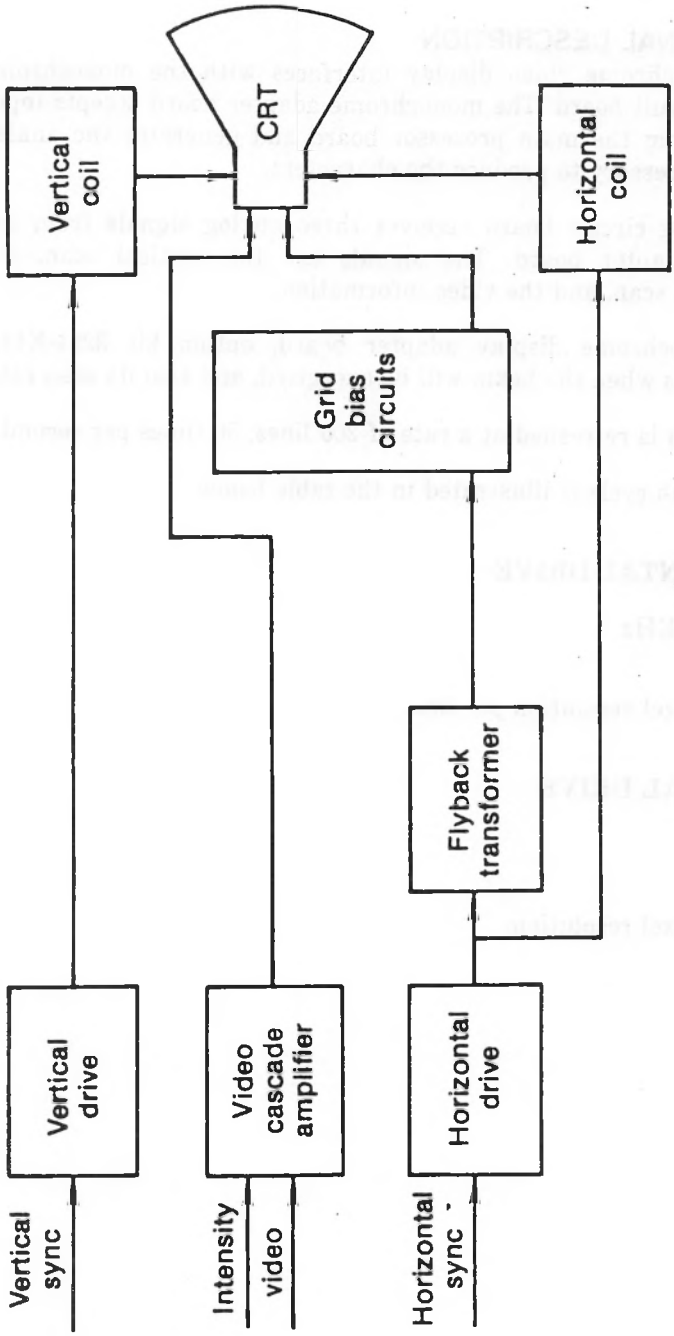
Components of the monochrome raster-scan display are a monochrome cathode ray tube (CRT) and a monochrome display analog circuit board.

CRT features:

- 14-inch (345 millimeters) measured diagonally
- 90 degrees deflection angle
- P39 phosphor



Monochrome Display



Monochrome Display Block Diagram

FUNCTIONAL DESCRIPTION

The monochrome video display interfaces with the monochrome analog circuit board. The monochrome adapter board accepts input signals from the main processor board and generates the analog signals necessary to produce the characters.

The analog circuit board receives three analog signals from the display adapter board. The signals are the vertical scan, the horizontal scan, and the video information.

The monochrome display adapter board, option kit 3284-K141, determines when the beam will be energized, and also its scan rate.

The screen is refreshed at a rate of 200 lines, 50 times per second.

The refresh cycle is illustrated in the table below.

HORIZONTAL DRIVE

- 15.750KHz
- 640 pixel resolution per line

VERTICAL DRIVE

- 59 Hz
- 200 pixel resolution

SPECIFICATIONS

Monochrome Functional Area	Measurement	Value	Remarks
Video Input	Amplitude	4.0 ± 1.5V	Into internal 500 ohms or less contrast control: TTL
	Rise Time	10ns	Maximum leading edge (10-90%)
	Fall Time	10ns	Maximum trailing edge (90-10%)
	Frequency	Up to 20MHz Data Rate	Standard Unit
	Maximum Bandwidth	16.257MHz	
Horizontal Drive Input	Amplitude	4.0 ± 1.5V	Sync Positive
	Rise/Fall Times	40ns Maximum	
	Resolution	18.432KHz/ 640 PIXEL Resolution	
	Blanking Time	9.965μ Sec	
Vertical Drive Input	Amplitude	4.0 ± 1.5V	Sync negative
	Rise/Fall Times	40ns Maximum	
	Resolution	50Hz/200 PIXEL Resolution	
	Refresh Rate	200 lines 50 times per second	
	Blanking Time	1.085 ms	
Input Power	Voltage/ Amperage Requirements	+12 Volts ± 5% 1.25 amps nom. 1.50 amps max.	
	Maximum Ripple	100mv p-p	Refresh Synchronous with power supply
		10mv p-p	Refresh non-synchronous with power supply
		50mv p-p	High Frequency power

SPECIFICATIONS

Monochrome Functional Area	Measurement	Value	Remarks
Controls	Internal (Factory Preset)		PC Label below:
		Horizontal Hold	"HORIZ HOLD"
		Video Centering	"HORIZ CENT"
		Linearity	"LINEARITY"
		Width	"WIDTH"
		Focus	"FOCUS"
		Brightness (Limiting)	BRT
		Contrast	CTRS
	External	Brightness	100K ohm potentiometer
CRT Display Characteristics	Diagonal Measurement	12 inches	—
	Deflection Angle	90°	
	CRT Type	20 inch	Sperical Radius
	High Voltage	13.0KV	Nominal
	Useable Screen Area	6.7 x 9.0 inches	
	Horizontal	800 @ 70 cd/m²	Center
	Resolution	650 @ 70 cd/m²	Corners
	Linearity	10% Maximum Height/Width Variance	Adjacent Characters
		20% Maximum Height/Width Variance	All Screen Characters
	Screen Surface	P39 Green Phosphor	
	Characters Per Line:	80	
	Number of Lines:	25	
	Character Boxes:	9 dots x 14 dots	

SPECIFICATIONS

Monochrome Functional Area	Measurement	Value	Remarks
Mechanical Specification	Weight	10.0 lbs. (4.54 kg)	
	Height Width Depth	7.49 in. 11.1 in. 11.4 in.	
Environment	Ambient Termperature	5° to 50°C (41° to 131°F)	Operating
		-40° to 65°C (-40° to 150°F)	Non-operating
	Humidity (Non-condensing)	5% to 90%	Operating/Non-operating
	Altitude (Maximum)	10,000 ft. (3.048 km)	Operating
		30,000 ft. (9.144 km)	Non-operating

COLOR/GRAPHICS DISPLAY BOARD

PHYSICAL DESCRIPTION

The Color/Graphics Adapter Board, option kit 3284-K140, controls the display of alphanumerics and graphics on an attached video display. The board is functionally compatible with most industry-standard color displays. The board also controls the operation of an optional light pen. The color/graphics display board is 13.00 inches wide and 4.25 inches high.

FUNCTIONAL DESCRIPTION

The color/graphics display board operates in two display modes selectable by the processor software: alphanumerics and graphics. The board is capable of displaying alphanumerics and graphics in black-and-white and color; the type of display is specified when the mode is selected.

When the board is in the alphanumeric mode characters are displayed as dot patterns provided by an on-board character generator; the generator produces dot patterns for 256 characters (Appendix A identifies the character set). The dot pattern is an 8 x 8 pattern; lower case letters are displayed in a 7 x 7 pattern with a descender. The screen size for the alphanumeric mode is also switch selectable: 40 column x 25 row (use with T.V.) and 80 column x 25 row (use with RGB, Composite or Internal Monitors)

When the board is in the graphics mode characters are displayed as picture elements. The graphics may be displayed at three-leveled resolution: 160 pixels x 100 row (low resolution); 320 pixels x 200 rows (medium resolution), or 640 pixels x 200 rows (high resolution). Pixel size for the graphics display depends on the resolution.

- 160 pixels x 100 rows; pixel size is 2 x 2 (or other combination can be done by user-written software)

- 320 pixels x 200 rows; pixel size is 1 x 1 (supported by NCR Operating System)

- 640 pixels x 200 rows; pixel size is 1 x 1

Although the board supports the low-resolution graphics mode (160 x 100), the BIOS does not. Therefore, if low resolution is used, special assembly language software must be developed to implement low-resolution graphics.

The board is capable of blinking characters in the alphanumeric mode and blinking foregrounds in the graphics mode; the blinking attribute is specified by software. For black-and-white displays, the board is capable of reversing the video; the video reverse attribute is software-selectable. The color attributes selectable by the software depend on the operating mode.

- 16 border colors for 40-column x 25-row alphanumeric screens are selectable
- 16 character colors for both alphanumeric screens are selectable
- 16 background colors for graphic screens (except high-resolution) are selectable
- 6 background colors for both alphanumeric screens are selectable
- 8 foreground colors for graphic screens (except high-resolution) are selectable

The software-selectable colors are defined in the following chart:

Color	Color Available For				
	Border	Characters	Alpha B'ground	Graphics F'ground	Graphics B'ground
Black	x	x	x		x
Blue	x	x	x		x
Green	x	x	x	x	x
Cyan	x	x	x	x	x
Red	x	x	x	x	x
Magenta	x	x	x	x	x
Brown	x	x	x	x	x
White	x	x	x	x	x
Gray (HI)	x	x	x		x
Light Blue (HI)	x	x			x
Light Green (HI)	x	x			x
Light Cyan (HI)	x	x			x
Light Red (HI)	x	x			x
Light Magenta (HI)	x	x			x
Light Brown (HI)	x	x			x
White (HI)	x	x			x

HI = High Intensity

Characters displayed on the monochrome display with the underline attribute are displayed on the color display as a blue character.

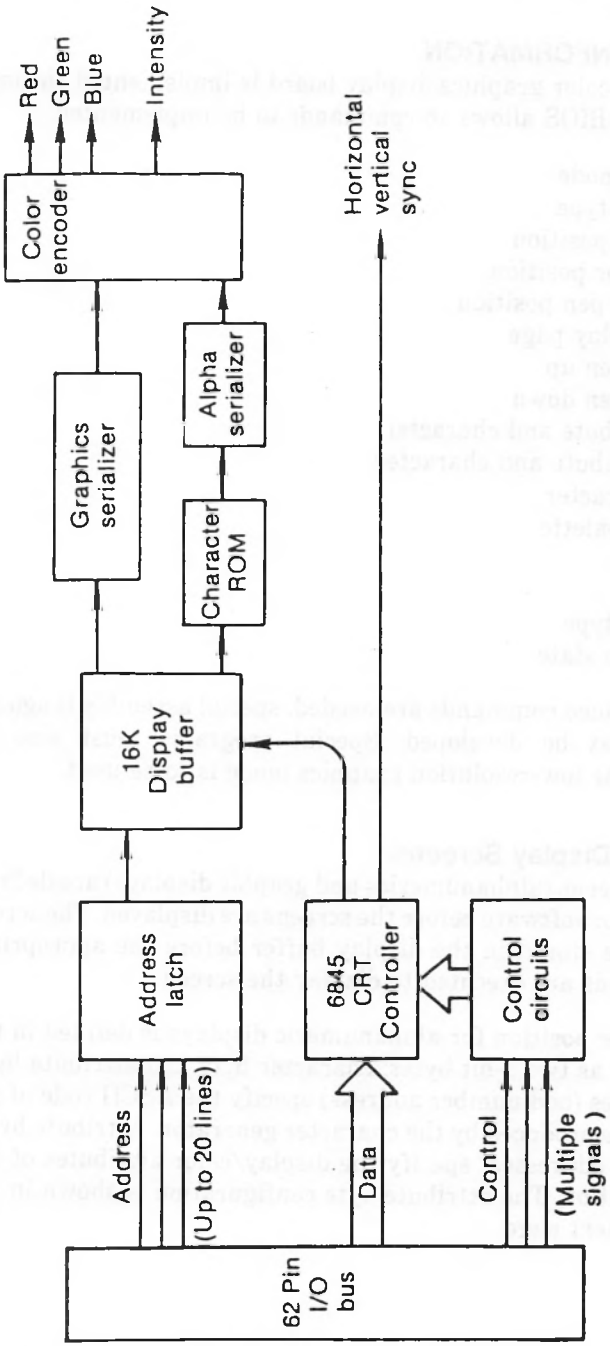
Characters displayed on the color display as a blue character are displayed on the monochrome display as a white character on a black background with a white underline.

On-board storage is eight 16K x 1 DRAMs. These RAMs are used as the display buffer. The display buffer size (16K) allows it to store multiple alphanumeric screens:

- Up to eight 40-column x 25-row alphanumeric screens
- Up to four 80-column x 25-row alphanumeric screens

A timing generator within the display controller produces the timing signals used by the display controller and the display buffer. These timing signals resolve processor/color graphic board conventions for accessing the display buffer.

The interface to the direct drive color display is through the 9-pin D-Shell type connector.



Color/Graphics Display Card Block Diagram

SOFTWARE INFORMATION

Control of the color graphics display board is implemented through the BIOS. The BIOS allows 16 commands to be implemented:

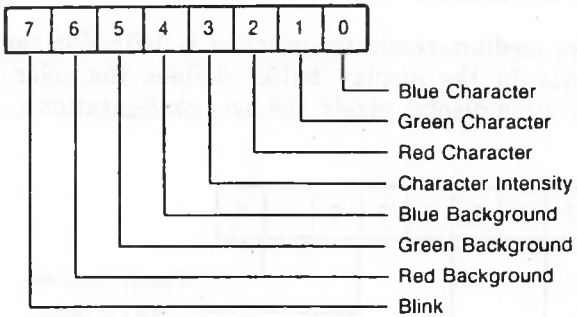
- Set video mode
- Set cursor type
- Set cursor position
- Read cursor position
- Read light pen position
- Select display page
- Scroll screen up
- Scroll screen down
- Read attribute and character
- Write attribute and character
- Write character
- Set color palette
- Write dot
- Read dot
- Write teletype
- Read video state

If additional video commands are needed, special assembly language programs must be developed. Special programs must also be developed if the low-resolution graphics mode is to be used.

Definition of Display Screens

All display screens (alphanumerics and graphic displays) are defined by the processor software before the screens are displayed. The screen definitions are stored in the display buffer before the appropriate BIOS commands are executed to display the screen.

Each character position for alphanumeric displays is defined in the display buffer as two 8-bit bytes: character byte and attribute byte. Character bytes (odd number address) specify the ASCII code of the character to be produced by the character generator. Attribute bytes (even number addresses) specify the display/color attributes of the character position. The attribute byte configuration is shown in the chart on the next page:



- Bits 0-3 identify the character color. Bit values and associated colors are:

	Bit Value				Dec. Value	Hex. Value
	3	2	1	0		
Black	0	0	0	0	00	00
Blue	0	0	0	1	01	01
Green	0	0	1	0	02	02
Cyan	0	0	1	1	03	03
Red	0	1	0	0	04	04
Magenta	0	1	0	0	05	05
Brown	0	1	1	0	06	06
White	0	1	1	1	07	07
Gray	1	0	0	0	08	08
Light Blue	1	0	0	1	09	09
Light Green	1	0	1	0	10	0A
Light Cyan	1	0	1	1	11	0B
Light Red	1	1	0	0	12	0C
Light Magenta	1	1	0	1	13	0D
Yellow	1	1	1	0	14	0E
White (HI)	1	1	1	1	15	0F

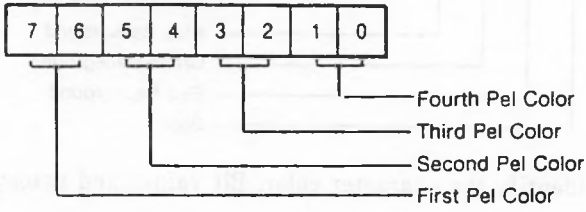
- Bits 4-6 identify the background color. The selectable colors are 0-8 as defined for character colors.

- Bit 7 indicates if the displayed character is to be blinking (1) or non-blinking (0).

- The meaning of Bit 7 depends on the state of Bit 5 of Mode Control Register (Port 3D8). If Bit 5 = 0, then a "1" state for Bit 7 indicates high intensity, and a "0" indicates normal intensity. If

Bit 5 = 1, then a "1" state for Bit 7 indicates activation of the blink attribute, and a "0" state indicates non-blink.

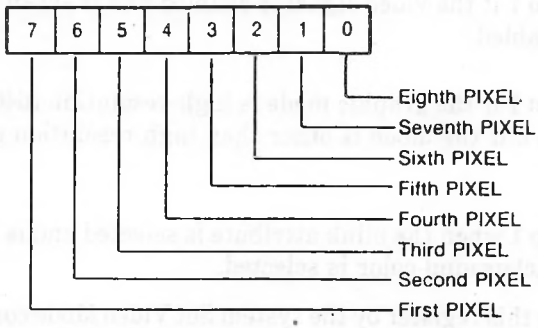
Each pixel for medium-resolution graphics is defined in the display buffer. A byte in the display buffer defines the color of four medium-resolution display pixels; the byte configuration is:



The value of each pixel-bit pair determines the color to be displayed:

- 00 indicates the pixel is displayed in the selected background color (color selected in bits 0 through 3 of the color selection register)
- 01 indicates the display color is selected by bit 5 of the color selection register: bit 5 = 1 (cyan) or bit 5 = 0 (green).
- 10 indicates the display color is selected by bit 5 of the color selection register; bit 5 = 1 (magenta) or bit 5 = 0 (red)
- 11 indicates the display color is selected by bit 5 of the color selection register; bit 5 = 1 (white) or bit 5 = 0 (brown)

Each pixel for high-resolution graphic displays is defined in the display buffer. A byte in the display buffer defines the on/off condition of eight pixels; the byte configuration is:

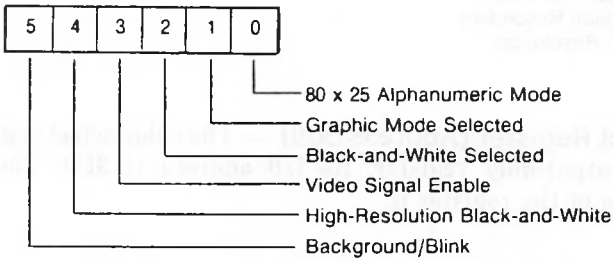


Each pixel bit indicates whether the pixel is to be displayed as background (0) or as foreground (1).

Selection of Video Modes

When the system executes the set video mode, it initializes the mode control register, color select register, and CRT controller registers R0 through R15 on the board according to the specified video mode (1-7).

Mode Control Register (Address 3D8) — The mode control register is a 6-bit output-only register; its I/O address is hexadecimal 3D8. The bit configuration of the register is:



- Bit 0 is set to 1 if the alphanumeric mode is 80 x 25 and is set to 0 if the alphanumeric mode is 40 x 25
- Bit 1 is set to 1 if the graphic mode is medium-resolution (320 x 200) and is set to 0 if an alphanumeric mode is selected.
- Bit 2 is set to 1 if black-and-white is selected and is set to 0 if color is selected.

- Bit 3 is set to 1 if the video signal is enabled and is set to 0 if the signal is disabled.

- Bit 4 is set to 1 if the graphic mode is high-resolution (640 x 200) and is set to 0 if the mode is other than high resolution graphic mode.

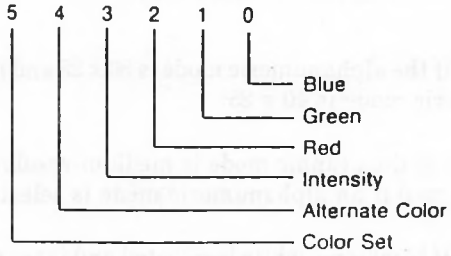
- Bit 5 is set to 1 when the blink attribute is selected and is set to 0 when the background color is selected.

The values set in this register by the system Set Video Mode command are:

Mode	Mode No.	Bit Value						Dec. Value	Hex Value
		5	4	3	2	1	0		
40 x 25 B/W	1	1	0	1	1	0	0	44	2C
40 x 25 Color	2	1	0	1	0	0	0	40	28
80 x 25 B/W	3	1	0	1	1	0	1	45	2D
80 x 25 Color	4	1	0	1	0	0	1	41	29
Graphic-MR Color	5	1	0	1	0	1	0	42	2A
Graphic-MR B/W	6	1	0	1	1	1	0	46	2E
Graphic-HR B/W	7	0	1	1	1	1	0	30	1E

B/W = Black and White
RM = Medium Resolution
HR = High Resolution

Color Select Register (Address 3D9) — The color select register is a 6-bit output-only register; its I/O address is 3D9. The bit configuration of the register is:



- Bits 0 through 3 are set to 1 if the appropriate color has been selected for the following:

- 40 x 25 alphanumeric border
- 320 x 200 graphics background
- 640 x 200 graphics foreground

- Bit 4 is set to 1 if the alternate, intensified set of colors is selected for the graphics mode and is set to 0 if the alphanumeric background color is selected.
- Bit 5 is set to 1 if the color set for 320 x 200 graphics is cyan, magenta, and white; it is set to 0 if the color set is green, red, and brown.

The values set in this register by the system set video mode command are:

Mode	Mode No.	Bit Value						Dec. Value	Hex Value
		5	4	3	2	1	0		
40 x 25 B/W	1	1	1	0	0	0	0	48	30
40 x 25 Color	2	1	1	0	0	0	0	48	30
80 x 25 B/W	3	1	1	0	0	0	0	48	30
80 x 25 Color	4	1	1	0	0	0	0	48	30
Graphic-MR Color	5	1	1	0	0	0	0	48	30
Graphic-MR B/W	6	1	1	0	0	0	0	48	3D
Graphic-HR B/W	7	1	1	1	1	1	1	63	3F

B/W = Black and White
RM = Medium Resolution
HR = High Resolution

CRT Controller Registers (Address 3D4) — CRT controller registers (R0 through R15) are 8-bit registers. They are not directly accessible to the software; instead, an address register (AR) is addressed (3D4) and loaded with a selected register number (0-11 Hex). The 16 registers are:

- Horizontal Total (R0) — This register is set to the horizontal synchronization period (character times); it is the number of displayed characters plus the number of non-display characters times (retrace) minus one.

- Horizontal Displayed Register (R1) — This register is set to the number of displayed characters per line; it must be less than the contents of R0.

- Horizontal Sync Position Register (R2) — This register is set to a value that defines the horizontal sync and scan delays. Increasing its value shifts the display to the left and decreasing its value shifts the display to the right.

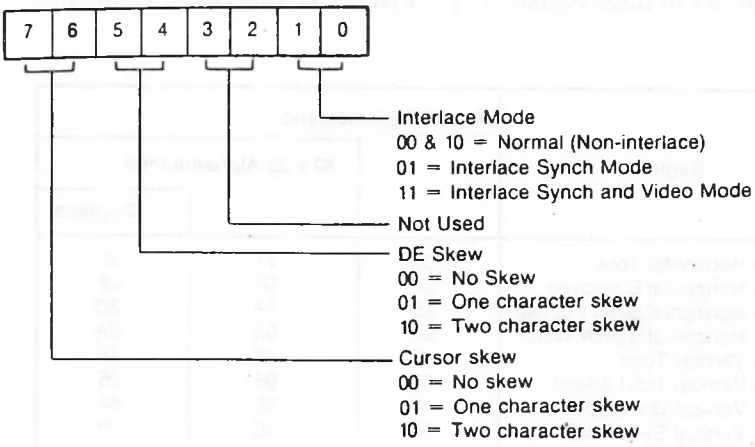
- Sync Width Register (R3) — This register is set to the value of the vertical sync pulse width which is fixed at 16 scan-line times and the horizontal sync pulse width which may range from 1 to 15 character clock periods.

- Vertical Total Register (R4) and Vertical Total (R 5) — These two registers are set to the elapsed time of the vertical scan. R4 is set to the integer number of the character line time minus one. R5 is set to the number of scan lines.

- Vertical Displayed Register (R6) — This register is set to the number of displayed character row times. The value must be less than the value of R4.

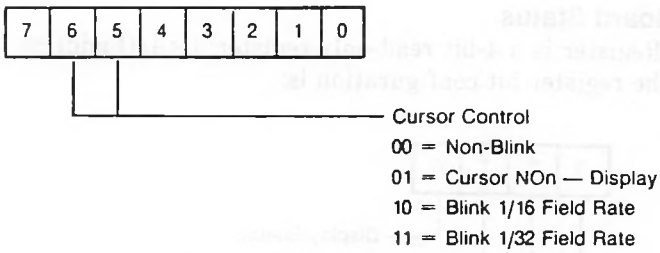
- Vertical Sync Position (R7) — This register is set to a value that controls the position of the vertical sync; the value is one less than the computed character line times. Increasing its value shifts the display up and decreasing its value shifts the display down.

- Interlace Mode and Skew Register (R8) — This register is set to a value that specifies the interlace mode, and the display enable and cursor output delays.



- Maximum Scan Line Address Register (R9) — This register is set to the number of scan lines per character row minus one.

- Cursor Start Register (R10) — This register is set to start the scan line within the character block and the cursor blink rate. Bits 5 and 6 of the register control cursor operation as shown below:



- Cursor End Register (R11) — This register is set to the last scan line of the cursor.

- Start Address Registers (R12 and R13) — This register pair controls the first address output by the CRT controller after vertical blanking. R13 holds the low-order bits.

- Cursor Registers (R14 and R15) — This register pair is set to position the cursor anywhere in the refresh RAM area. R14 holds the high-order bits and R15 holds the low order bits.

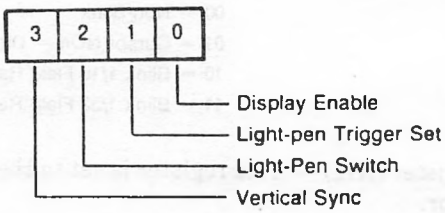
The values set in these registers by the BIOS set video mode command are:

Register	40 x 25 Alphanumeric	80 x 25 Alphanumeric	Graphics
R0 — Horizontal Total	38	71	38
R1 — Horizontal Displayed	28	50	28
R2 — Horizontal Sync Position	2D	5A	2D
R3 — Horizontal Synch Width	0A	0A	0A
R4 — Vertical Total	1F	1F	7F
R5 — Vertical Total Adjust	06	06	06
R6 — Vertical Displayed	19	19	64
R7 — Vertical Sync Position	1C	1C	70
R8 — Interlace Mode	02	02	02
R9 — Max Scan Line Address	07	07	01
R10 — Cursor Start	06	06	06
R11 — Cursor End	07	07	07
R12 — Start Address (H)	0	0	0
R13 — Start Address (L)	0	0	0
R14 — Cursor Address (H)	0	0	0
R15 — Cursor Address (L)	0	0	0

All values are hex

Check of Board Status

The Status Register is a 4-bit read-only register; its I/O address is 3DA Hex. The register bit configuration is:



- Bit 0 is set to 1 if the CRT controller is not accessing the display buffer; the main processor board can access the display buffer without interfacing with the screen (screen flicker).
- Bit 1 is set to 1 if the light pen trigger has been set
- Bit 2 is set to 1 if the light pen switch is OFF and set to 0 if the light pen switch is ON.

- Bit 3 is set to 1 if the CRT controller is in the vertical retrace period; the main processor board can access the display without interference.

Control of the Light Pen

The light pen is controlled by two latches: Clear Light Pen Latch and Reset Light Pen Latch. Any access to address 3DC (Hex) presets the light pen and any access to address 3DB (Hex) resets the light pen. Data is not required with addresses 3DC and 3DB; both are address-activated.

CRT Controller Programming Requirements

The BIOS sets CRT controller registers R0-R7 to preset values depending on the video mode selected. For different video mode requirements, special programs must be developed to set the CRT controller registers.

The following table identifies the parameters used to calculate the CRT controller register values:

Parameters	40 x 25 Alphanumerics	80 x 25 Alphanumerics	Graphics
Displayed Characters Per Row	43	80	43
Displayed Characters Rows Per Screen	25	25	100
Character Blow Rows	8	8	2
Active Scan Lines	200	200	200
Total Scan Lines	261	261	255
Total Rows Per Screen	32.6	32.6	127.6
Horizontal Sync Delay	2	10	2
Horizontal Sync Width	10	10	10
Horizontal Scan Delay	2	14	3
Total Character Times	57	114	57
Vertical Sync Delay	0	0	12

Perform the following procedures to set the CRT controller registers:

1. Send register number (0-11 Hex) of the desired register with an OUT I/0 instruction to address 3D4.

2. Send the desired value of the register with an OUT I/0 instruction to address 3D5.

COLOR/GRAPHICS DISPLAY BOARD PROGRAMMING REQUIREMENTS

The mode control register and the color select register are set to predefined values by the BIOS set video mode command. Additionally, the BIOS sets the color select register for medium-resolution graphics with the set color palette command.

Mode Control Register

For all modes except high-resolution, black-and-white graphics, bit 5 of the register is set to (1). For the graphics displays bit 5 does not have any effect. However, for alphanumeric displays, bit 5 indicates the blinking bit of the display buffer attribute byte is enabled and the character displayed blinks according to the blink bit in the attribute byte. With bit 5 set to 1, the background colors for alphanumerics are limited to 8 colors not requiring the intensity bit.

To define the additional eight background colors specified by the intensity bit, bit 5 of the mode control register must be turned off; value less than 20 Hex.

Color Select Register

The BIOS set video mode command sets the color select register for the following color attributes:

- For 40 x 25 alphanumeric display — border color is black.
- For all alphanumeric displays — background and character colors selected in display buffer.
- For medium-resolution graphic displays — background color is black and foreground color is selected in the buffer display (colors selectable are cyan, magenta, and white)

If the color attributes for the medium-resolution graphic displays are to be changed, the set color palette command of the BIOS can be used. This command resets the background color or the color set for foregrounds. However, a change in the 40 x 25 alphanumeric display border color must be made with special programming. The program must issue an OUT I/O instruction to address 3D9 with the appropriate value for the desired color.

OPERATION

Operation of the color/graphics display board is under system control. If the mode of operation is to be changed after the Set video mode command has been executed, care must be taken to prevent flicker on the screen. To change video mode, perform the following:

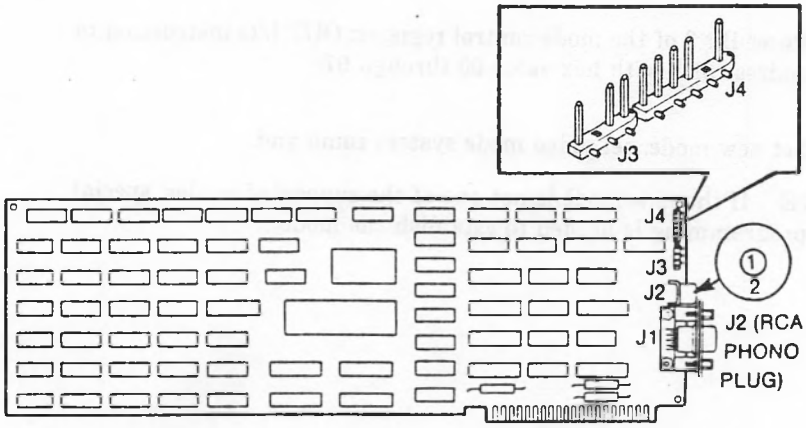
1. Determine the existing mode of operation: read video state system command.

2. Reset Bit 3 of the mode control register: OUT I/O instruction to address 3D8 with hex value 00 through 07.

3. Set new mode: set video mode system command.

NOTE: If the new mode is not one of the supported modes, special programming is needed to establish the mode.

PHYSICAL CONNECTIONS/PIN ASSIGNMENTS (COLOR/GRAPHICS DISPLAY ADAPTER)



J4 — LIGHT PEN INTERFACE

Pin	Signal
1	-Light Pen Input
2	Key
3	-Light Pen Switch
4	Chassis Gnd
5	+5V
6	+12V

J3 — RF MODULATOR INTERFACE

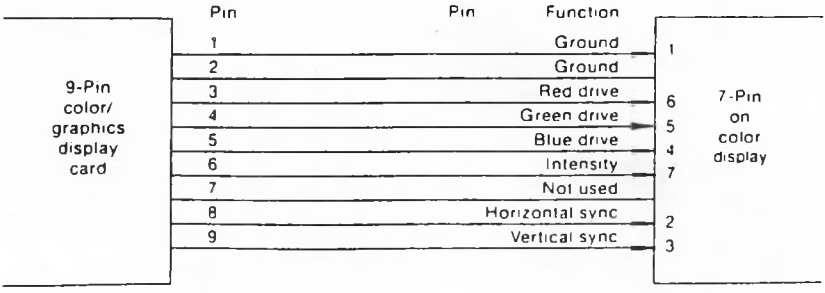
Pin	Signal
1	+12V
2	Key
3	Composite Video Output
4	Logic Gnd

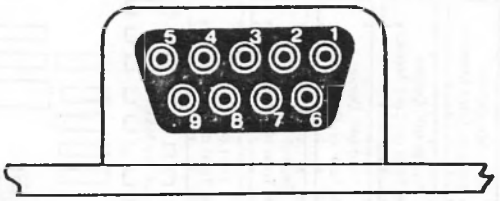
J2 — COMPOSITE VIDEO INTERFACE

Pin	Signal
1	Composite Video Output
2	Chassis Gnd

J1 — RGB COLOR OUTPUT

Pin	Signal
1	Gnd
2	Gnd
3	Red
4	Green
5	Blue
6	Intensity
7	Reserved
8	Hor. Sync.
9	Ver. Sync.





Color/Graphics Adapter Output

Pin	Signal	Pin	Signal	Pin	Signal
A2	+ Data 7	A18	+ A13	B1	Ground
A3	+ Data 6	A19	+ A12	B2	+ Reset
A4	+ Data 5	A20	+ A11	B3	+ 5V
A5	+ Data 4	A21	+ A10	B9	+ 12V
A6	+ Data 3	A22	+ A9	B10	Ground
A7	+ Data 2	A23	+ A8	B11	- MEMW
A8	+ Data 1	A24	+ A7	B12	- MEMR
A9	+ Data 0	A25	+ A6	B13	- IOW
A11	FAEN	A26	+ A5	B14	- IOR
A12	+ A19	A27	+ A4	B20	Clock
A13	+ A18	A28	+ A3	B29	+ 5V
A14	+ A17	A29	+ A2	B30	+ OSC
A15	+ A16	A30	+ A1	B31	Ground
A16	+ A15	A31	+ A0		

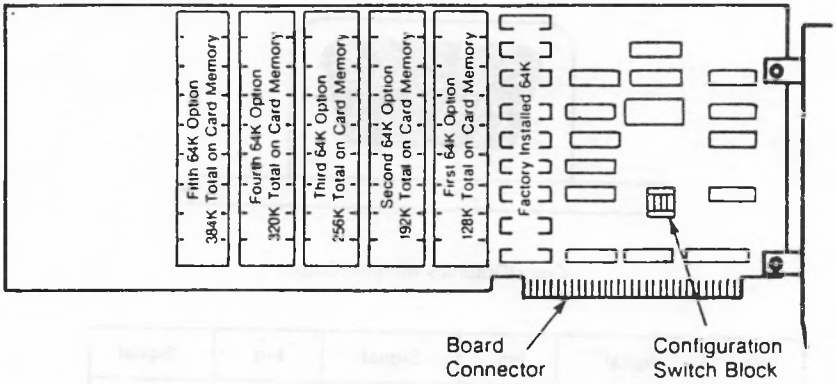
62 — Pin Edge Connector

MEMORY EXPANSION BOARD

The Memory Expansion Board, kit number 3284-K101, provides additional random access memory for the main processor board. The memory expansion on the board is in 64 KB increments up to 384 KB; the first nine chips (64K B) are soldered and the remaining RAM locations are socketed for expansion. Expansion is obtained by populating the board in nine-chip increments.

PHYSICAL DESCRIPTION

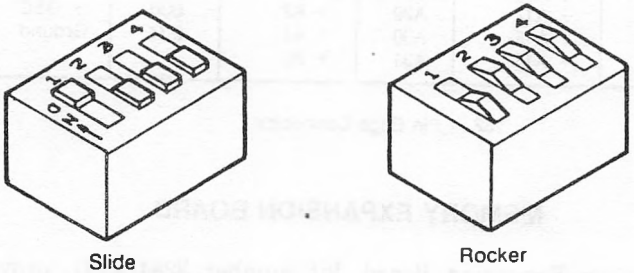
The memory expansion board is 13 inches long and 4.2 inches high: it is populated as shown in the following illustration:



Memory Expansion Card

The main processor board RAM must be populated to 256 KB and no more before the memory expansion board is installed.

The configuration switches are housed in a DIP package. They may be either the slide type of the rocker type.



DIP Switch Types

Each individual switch in the package is identified with a number, and the 'OPEN' or 'ON' position of the switches are also identified on the package. In the illustration above, switch 1 is shown in the CLOSED or ON position, the remaining switches in the OPEN or OFF position.

FUNCTIONAL DESCRIPTION

The memory expansion board contains six banks of nine RAM locations. Bank 0 comes from NCR populated with 64 KB RAM's; banks 1-5 are socketed to provide easy installation of 64 KB RAMs. Memory refresh is provided by the main processor board.

When installing the board, configuration switches on the board must be set to identify the amount of memory installed. The switch settings for this board are shown in the figure on the next page.

Expansion Board Switches				Board Memory Size	Explanation
1	2	3	4		
On	On	On	On	64 KB	Setting as delivered
Off	On	On	On	128 KB	After first 64 KB expansion
On	Off	On	On	192 KB	After second 64 KB expansion
Off	Off	On	On	256 KB	After third 64 KB expansion
On	On	Off	On	320 KB	After fourth 64 KB expansion
Off	On	Off	On	384 KB	After fifth 64 KB expansion

Memory Expansion Card Switch Settings

OPERATING CHARACTERISTICS

- 64 KB to 384 KB expansion range (64 KB increments)
- 200 ns access time
- 320 ns cycle time

PHYSICAL CONNECTIONS/PIN ASSIGNMENTS

Signal	Pin	Signal	Pin
-I/O Check	A1	+ A7	A24
+ Data 7	A2	+ A6	A25
+ Data 6	A3	+ A5	A26
+ Data 5	A4	+ A4	A27
+ Data 4	A5	+ A3	A28
+ Data 3	A6	+ A2	A29
+ Data 2	A7	+ A1	A30
+ Data 1	A8	+ A0	A31
+ Data 2	A9	GROUND	B1
+ AEN	A11	+ RESET	B2
+ A19	A12	+ 5V	B3
+ A18	A13	+ 12V	B9
+ A17	A14	GROUND	B10
+ A16	A15	- MEMW	B11
+ A15	A16	- MEMR	B12
+ A14	A17	- IOW	B13
+ A13	A18	- IOR	B14
+ A12	A19	CLOCK	B20
+ A11	A20	+ 5V	B29
+ A10	A21	+ OSC	B30
+ A9	A22	GROUND	B31
+ A8	A23		

Expansion Bus Connector

SCSI INTERFACE

FUNCTIONAL DESCRIPTION

NCR provides an interface system to allow the Personal Computer to share peripheral devices with other Personal Computers. SCSI, the Small Computer System Interface, uses a high-level command set that masks the on-board structures of the peripheral devices from the interface, making SCSI device independent. This independence allows the substitution of one vendor's device with another's without major modifications of the host hardware or software. The SCSI interface provides the following major features:

- Intelligent Bus
- Device Independence
- Wide Selection of Peripheral Devices
- Direct Copy Between Devices
- Optional Bus Arbitration

Intelligent Bus

SCSI uses an intelligent, eight-port device that permits communications between any two of the eight ports. Any port can be attached to a host computer or a peripheral device controller. A host computer on one of the ports can address any of the other seven ports. Therefore the SCSI can accommodate single- or multiple-host systems with several peripheral device controllers. SCSI can accommodate up to eight devices.

Device Independence

The SCSI command set masks the on-board structures of the peripheral devices from the interface. This eliminates the need for major software modifications when changing peripheral devices.

Wide Selection of Peripheral Devices

The SCSI bus accommodates controllers for low- to medium-performance peripheral devices. SCSI can accommodate hard disk drives, flexible disk drives, magnetic tape drives, and printers.

Direct Copy Between Devices

The SCSI bus configuration allows direct copy between two devices.

Optional Bus Arbitration

The optional SCSI bus arbitration device allows priority assignment of bus capture requests. The highest priority device wins the arbitration and captures the bus.

The SCSI interface also supports 1.5 MB data transfer rates, simplified I/O programming, a device-independent command set, and multiple overlap of peripheral device operations for increased throughput.

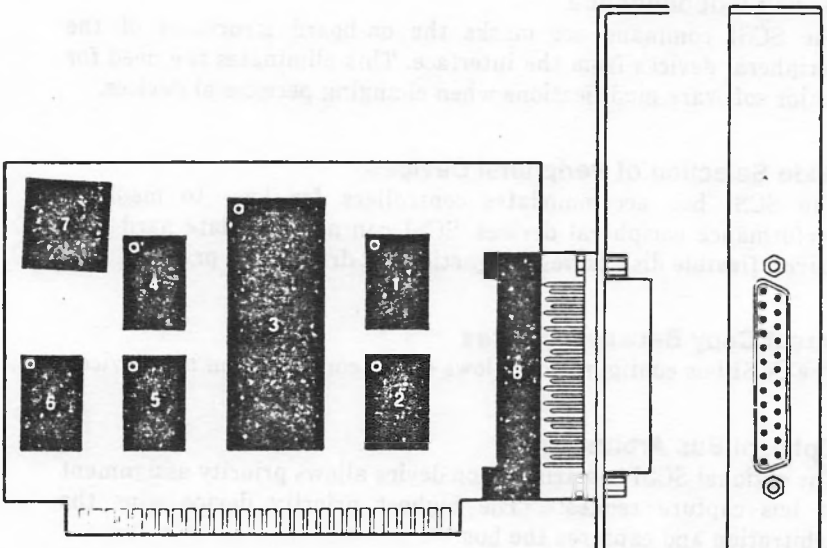
PROPOSED STANDARD

SCSI is a joint effort by NCR, Shugart Associates, and others (as such it has been referred to as SASI). The companies involved with SCSI are presenting it to the American National Standards Institute (ANSI) as a proposed standard interface. SCSI (or SASI) has already been adopted by many companies as a standard interface.

COMMUNICATIONS ADAPTER AND CABLE

ADAPTER

The asynchronous communication adapter is NCR kit 3284-K130. It is an add-on plug-in board that provides the capability of connecting a serial RS 232C device such as a printer, plotter, or modem to the computer. This connection is in addition to any peripheral connected to the internal asynchronous communications port.



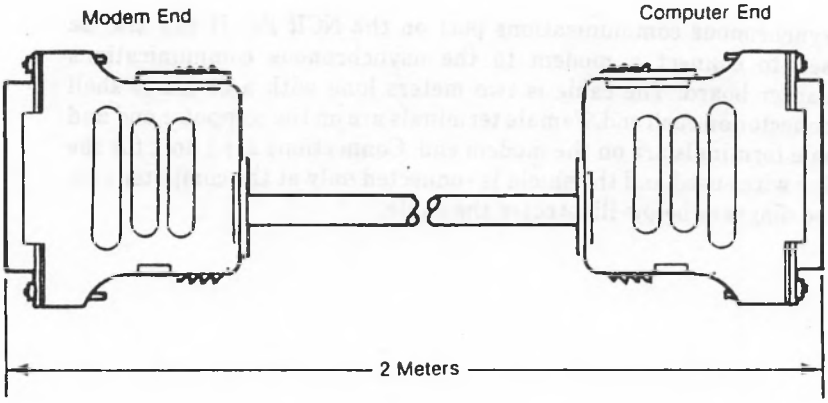
1. Line Driver
2. Line Receiver
3. Async Communications Element
4. Line Receiver
5. Nand Gate
6. Quad Tristate Buffer
7. 1.8432 MHz Crystal
8. DB 25 Connector

Asynchronous Adapter Board

CABLES

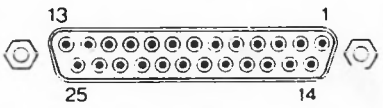
The communications cable is NCR kit 3284-K122. It is an accessory cable which allows connecting a modem to the RS 232C serial

asynchronous communications port on the NCR PC. It can also be used to connect a modem to the asynchronous communications adapter board. The cable is two meters long with a 25-pin D shell connector on each end. Female terminals are on the computer end and male terminals are on the modem end. Connections are 1-to-1 for the nine wires used and the shield is connected only at the computer end. The diagram below illustrates the cable.



Pin assignments at computer end of the cable		Pin assignments at modem end of the cable
1	Frame Ground	None
2	Transmit Data	2
3	Receive Data	3
4	Request to Send	4
5	Clear to Send	5
6	Data Set Ready	6
7	Signal Ground	7
8	Carrier Detect	8
20	Data Terminal Ready	20
22	Ring Indicator	22
	Grounding Strap Connected to Shield	
	All other pins are unused	

Communications cable pin assignments



Female serial connector on the asynchronous device

PRINTER OPTIONS

The following sections present overview and specification information describing the printers and the plotter that are available, as options, with the NCR Personal Computer.

MODEL 6411-8510 DOT MATRIX PRINTER, SMALL CARRIAGE

Physical Description

This printer is a freestanding 120 CPS 80-column dot matrix impact printer that connects directly to a parallel output port of the Personal Computer. State-of-the-art technology provides a compact, lightweight, table-top unit with tractors below the print line. This design allows the printed output to be immediately removed without the wasted paper usually associated with tractor-feed units. Should friction paper feed be preferred, the tractors can be disabled by the operator. The printer can utilize cut sheets or multiple fan-fold forms with up to four parts.

Functional Description

The printer contains a 96-character ASCII generator for upper/lower case print and a graphics character generator for block graphics. In addition, it can move paper bidirectionally, and print bit-image graphics generated by application program. An added feature of the printer is the capability to load (by means of a program) an eight-channel vertical format unit with five tab stops. Tab positions then can be selected or by passed as necessary, to speed printing on applications with variable prints on each line.

Specifications

Specifications for the 6411-8510 are as follows:

Print Method:	Dot matrix, impact
Print Speed:	120 CPS, bidirectional position-seeking 63 lines per minute for full 80-column page
Character Set:	96 character upper/lower case ASCII
Character Format:	7 (horizontal) x 8 (vertical) dot matrix characters 8 (horizontal) x 8 (vertical) dot matrix graphics
Character Pitch:	5, 6, 8.5, 10, 12 characters per inch, or proportional

Paper Feed:	Bidirectional friction tractor
Line Spacing:	6 or 8 lines per inch (characters) N/144 inches (graphics)
Line Feed Speed:	Maximum 100 ms
Form Width:	3.5 to 10 in.
Form Thickness:	.05 - .28 mm
Number of Copies:	Original plus 3
Type of Forms:	Fan-fold sprocket single sheet paper
Form Loading:	Rear
Power:	115VAC + 10%, 60Hz, 180W
Weight:	24 lbs./11 kg
Dimensions:	Width: 22 in. (550 m n); Depth: 21 inches (300 mm), Height: 5.3 inches (133 mm)
Interface:	8-bit parallel (Centronics-compatible)

MODEL 6411-1550 DOT MATRIX PRINTER, LARGE CARRIAGE, FASTER SPEED

Functional Description

The primary difference between this printer and the Model 6411-8510 printer is that this printer has a wider, 136-character carriage. Both 6411 models can utilize cut sheets or multiple fan-fold forms with up to four parts.

Both of the mentioned printers contain a 96-character ASCII generator for upper/lower case print, and a graphics character generator for block graphics. In addition, they can move paper bidirectionally, and print bit-image graphics generated by the application program. An added feature of both 6411's is the capability to load (by means of a program) an eight-channel vertical format unit with five tab channels, with each channel capable of accepting multiple tab stops. Tab positions then can be selected or by-passed to speed printing on applications with variable print lines on each form.

Specifications

Specifications for the 6411-1550 printer are as follows:

Print Method:	Dot matrix, impact
Print Speed:	120 CPS, bidirectional position-seeking, lines per minute for full 136-column page
Character Set:	96 characters upper/lower case ASCII
Character Format:	7 (horizontal) x 9 (vertical) dot matrix characters 8 (horizontal) x 8 (vertical) dot matrix graphics
Character Pitch:	5, 6, 8.5, 10, 12 characters per inch, or proportional
Paper Feed:	Bidirectional friction tractor
Line Spacing:	6 or 8 lines per inch (characters) N/144 inches (graphics)
Line Feed Speed:	Maximum 80 ms
Form Width:	3.5 to 15.0 in.
Form Thickness:	.05 - .28 mm
Number of Copies:	Original plus 3
Type of Forms:	Fan-fold sprocket, single sheet paper
Form Loading:	Rear
Power:	115VAC + 10%, 60Hz, 180W
Weight:	24 lbs./11 kg.
Dimensions:	Width: 22 in. (550 mm); Depth: 12 in. (300 mm); Height: 5.3 inches (133 mm)

Interface: 8-bit parallel (Centronics-compatible)

MODEL 6455-2310 LETTER QUALITY PRINTER

Functional Description

This printer provides the highest quality printer output. A letter-quality original, with up to five copies, can be printed at speeds of up to 33 characters per second. A program mode feature allows complete control of the printer through the application program of such items as thimble pitch, impression control, and character spacing. The latest word processing technology and printer features include:

- 2K buffer
- Auto bidirectional printing
- Two-color ribbon
- End-of-ribbon detect
- Paper-out detect
- Friction feed platen
- Set/reset horizontal tabs
- Set/reset vertical tabs
- Set/reset forms length
- Set/reset left/right margins
- Reverse line feed
- Half-line and reverse half-line feed
- Set format mode (for pre-printed forms)
- Paper out defeat (allows operator to override paper out detect)
- Graphics mode (requires bidirectional tractor option)
- Remote diagnostics

- Word Processing Assist Group, including:
  - Auto proportional spacing
  - Auto underscore
  - Auto bold print
  - Shadow print
  - Auto line centering
  - Line justification
  - Fine back spacing
- Operator Switch-Selectable parameters, including:
  - 110 to 9600 baud
  - ETX/ACK-DC1-DC3 protocol
  - Auto CR or LF
  - 6/8 line per inch
  - Impression control
  - 10, 12, or 15 characters per inch or proportional spacing

Other forms-handling options include:

- Single and dual cut-sheet feeders
- Bidirectional forms tractor
- Bottom-feed adapter
- Cut-sheet guide
- Front insertion
- Envelope adapter

Specifications

Specifications for the 6455-2310 printer are as follows:

Print Speed:	Up to 33 characters per second
Maximum Copies:	Original plus 5
Character Set:	Up to 128 characters
Paper Width:	Up to 16 inches
Printing:	136 columns at 10 characters per inch 163 columns at 12 characters per inch 204 columns at 15 characters per inch
Column spacing:	120 positions per inch
Line Feed:	48 positions per inch
Tabbing:	Horizontal and vertical (any direction)
Copy/Impression Control:	Under control of operator or program
Interface Type:	EIA RS 232C/CCITT V.24
Communications Code:	ASCII

MODEL 5403-0102, 0202 PLOTTERS

Physical Description

The Model 5403-0102 Graphics Plotter is an option available with the NCR Personal Computer. The plotter is a two-pen device, accommodating 8-1/2-x-11 inch and 210-x-297 millimeter hard-printout copy.

Pinch wheels and drive wheels move the paper across the platen for X-axis plotting. Pen movement locates points along the Y-axis. Lines can be plotted at speeds of up to 15 inches per second (38 centimeters per second). Labels can be drawn at speeds of up to six characters per second.

The two-pen feature supports dual-color plotting. For plots requiring more than two colors, the program being plotted can be halted and pen colors can be changed.

Five internal characters sets are available. The symbol plotting capability and the seven dashed line fonts provide additional printout versatility.

Operation of the plotter is controlled through the pushbuttons on the front panel. Pushbuttons permit manual control of the paper and pen movement, including pen selection, and halting the program (for changing pens, viewing the plot, etc.).

A six-pen graphics plotter, 5403-0202, is also available for the NCR Personal Computer; this plotter has essentially the same capabilities and operating characteristics as the two-pen model. For additional information, contact your NCR representative.

Functional Description

Either graphics plotter can be used to produce hard copy computer graphics for technical, scientific, and business applications. Charts and graphs can be output in color for such applications as summarizing data, identifying trends, comparing results, focusing on exceptions, etc.

When the plotter is turned on, default conditions are automatically established for most plotting parameters. In most cases, the only additional user action required to start the plotting is to load the pens and plotting medium.

The five internal character sets eliminate the need to use software-generated characters. Text can be written in any direction, with or without slant, and in various sizes.

A variety of operations can be programmed into the plotter, using the 40 plus built-in instructions.

The plotter has an addressable step size of 0.001 inch (0.025 mm), i.e., the plotter can plot up to 1000 points in a one-inch line. When commanded to return to the same point, this repeatability can be achieved within 0.004 inches (0.1 mm).

The interface for the plotter is an RS 232C. A dual input/output cable is available, which allows connection of the plotter in series with a terminal and computer.

Specifications

Plotting Sizes:	0102: Hard copy media size of 8.5 x 11 in.	
	0202: Hard copy media size of 17 x 11 in.	
	0102	0202
Mechanical Limits:	Y-axis: 7.5 in.	10.5 in.
	X-axis: 10.7 in.	16.7 in.

Addressable Resolution:	0.001 in. (Step Size)
Repeatability:	0.004 in. for any specific dimension
Pen Velocity:	Pen down: maximum 15 in. (each axis) per second; programmable from 0.40 to 15 in. in increments of 0.15 in.; Pen Up, 20 in. per second
Communications Modes:	Half- or full-duplex
Transmission Speed:	110 to 9600 baud
Parity:	Odd, even, or marking bit
Receive Buffer Size:	256 characters or 2 KB (switch-selectable)
Overall Dimensions:	Width: 24 inches; Depth: 15 in.; Height: 9 in.
Weight:	27 lbs.
Power Consumption:	80 Watts (stand-by) 170 Watts (operating)
Power Requirements:	115/230 VAC 0215%, 50/60Hz
Environmental And Safety:	Meets UL478 and CSA C22.2
Temperature:	Operating 40 degrees F to 100 degrees F (5 degrees C to 38 degrees C)
Relative Humidity:	Operating/storage 10-90% (non-condensing)
Acoustic Noise:	60 dba (with covers)

NCR DECISION NET SYSTEM

NCR DECISION NET is an efficient way to tie personal computers together in an information network. Interconnection by Omninet, the

NCR local area network, allows the business professional to take advantage of electronic mail and user-to-user interaction.

The DECISION NET system has two major components; MODUS and Omninet. Network control is provided by Omninet.

The Omninet local area network supports 64 workstations with a maximum separation of 5000 feet. Omninet has a collision avoidance scheme to minimize the probability of data collision.

NCR MODUS allows the network to share files and peripherals. The following optional equipment allows the Personal Computer to be connected to Omninet:

DECISION NET Transporter Board and Cable (NCR Kit #3273-K700)
: The microprocessor-based transporter board performs many high level network tasks that are usually handled by the host computer. The transporter board features error detection and message acknowledgement. These features greatly reduce the software burden on the host computer, MODUS, and the personal computers on the network. One transporter board is required for each Personal Computer connected to the network.

DECISION NET Tap Box (NCR Kit #3273-K702)
: The DECISION-NET Tap Box is the hardware component that provides the connection between the Personal Computer and the network cable. One tap box is required for each Personal Computer connected to the network.

DECISION NET Repeater (NCR Kit #3273-K704)
: The DECISION-NET Repeater extends the maximum separation distance between network equipment. Each DECISION-NET Repeater can extend the network 1000 feet. The maximum network length is 5000 feet with the maximum of four DECISION-NET Repeaters.

NCR-DOS 2.11 Networking Software (NCR Kit #GOBO-0014)
: This software provides the communications capabilities on the network.

ROM

ROM BIOS

The overall purpose of the BIOS (basic input/output system) is to provide control of the system devices at the device level. The BIOS consists of two parts: diagnostics/initialization, and the actual device handling routines. The diagnostics and initialization part executes when power is first turned on, and when a keyreset (control-alternate-delete) is issued. It is responsible for verifying and initializing the hardware, and setting up tables and control information required by the operating system. The device handling routines take care of the actual initialization of the devices and the I/O to/from the devices.

The BIOS frees you from the requirement of device addressing and specifying device operating characteristics. This isolation between user programs and device control provides the advantages of (1) removing this programming burden from programmers, and (2) offering additional flexibility by allowing device changes and additions to the system without impacting the user programs. It is for this reason that you should never attempt to branch directly to the BIOS routines, but should always perform I/O through the function calls and interrupts provided by NCR-DOS.

The display of time of day is done through a routine which takes control of interrupt 1C (Hex). The display should be disabled through software in NCR-DOS if you want to use interrupt 1C or run a program which accesses that interrupt and have a problem doing so.

The interrupt service routine always returns control to the system through the standard return address in the ROM-BIOS. When the display is disabled there is only negligible processing in the interrupt service routine.

DIAGNOSTICS

This chapter describes the interfaces for the PC6 user and service diagnostics. The diagnostics for the computer and its devices are set up in two levels, an overall "shell" and the test modules within the shell for each individual device. This arrangement allows the addition of test modules to the shell when a new device is added to the system without modification to the rest of the modules.

MODULAR DIAGNOSTIC CONCEPT

The PC6 diagnostics system is a modular software system with one shell controlling the execution of a variable number of test modules. The shell, running under NCR-DOS, provides a menu of any number of test modules. The test modules can be executed individually or in groups, once only or repeating automatically until stopped. The test modules interface directly to an error log file on the diagnostics diskette. The figure below shows the structure of the diagnostic system. Each test module is also capable of running independently under NCR-DOS.

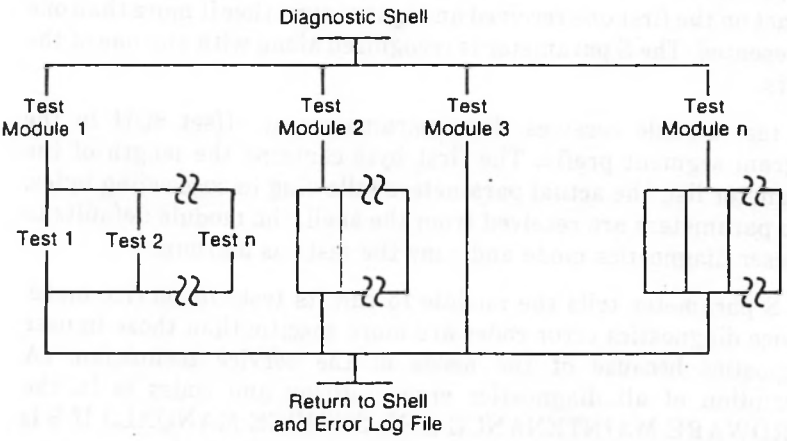


Figure 5-1 Diagnostics Structure Diagram

DIAGNOSTICS

The diagnostics shell, running under DOS, is the core of the diagnostics system. It has features such as utilities and test module installation. The shell prompts you for a choice from a menu of test modules, then sets up the parameters and invol es the selected test module.

The shell permits the user of the diagnostics to add test modules that conform to the module/shell interface and the module/error log interface. This allows you to customize the diagnostics routines to the specific hardware in your system.

MODULE INTERFACE

Test modules are written so that the tests can be run for the user of the system as well as for the service personnel. Because of DOS restrictions, test modules in the PC6 diagnostic system must have unique file names. Test modules do not destroy the operating system or alter its state in any way.

The test module/shell interface requires the shell to pass one of the following parameters to whatever module is invoked:

S	Service Diagnostic Mode
M	Mute User Interaction
G	Group Test Mode
R	Repeat Test Mode
C	Configuration Test Mode

The parameters G, R, and C are mutually exclusive, i.e., the module will act on the first one received and ignore any other if more than one is presented. The S parameter is recognized along with any one of the others.

The test module receives these parameters at offset 80H in the program segment prefix. The first byte contains the length of the parameter list; the actual parameters following in succeeding bytes. If no parameters are received from the shell, the module defaults to the user diagnostics mode and runs the tests as a group.

The S parameter tells the module to run its tests in service mode. Service diagnostics error codes are more specific than those in user diagnostics because of the needs of the service technician. (A description of all diagnostics error returns and codes is in the HARDWARE MAINTENANCE AND SERVICE MANUAL.) If S is passed as the only parameter, the test module displays a menu; otherwise no menu is displayed. A typical service diagnostics menu is shown in Figure 5-2.

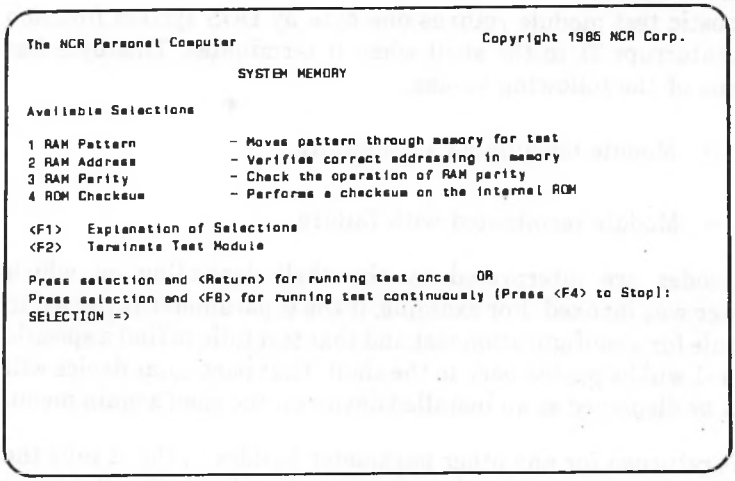


Figure 5-2 Service Menu for System Memory Module

The M parameter tells the module that it should "mute", i.e. suppress, any prompts for operator action whenever the tests are being run in "all" or "continuous" mode. During such a test run the shell continually checks the "stop key", F4, and stops at the end of the current test when F4 is pressed.

The G parameter tells the module that the tests in that module should be run as a group. No menu is displayed. When all of the tests are completed, the module returns to the diagnostics shell. User diagnostics performs tests only in group mode. All keyboard entries are ignored while the tests are running.

The R parameter tells the test module to perform a test by "repeat group". This means that the tests are performed as a group, then repeated again within the module until you press the "stop key", F4. Test banners and passed/error messages are the same as in group parameter tests.

The C parameter tells the test module to perform a configuration test for the module and return a pass/fail byte. The C parameter gives the shell the ability to determine a configuration of test modules and diplay those modules on its main menu. The configuration test checks only whether the devices related to the test module are present. A configuration test is included in each test module.

RETURN CODES

A diagnostic test module returns one byte by DOS system function 4CH in interrupt 21 to the shell when it terminates. This byte has either one of the following values:

0 = Module terminated successfully

-1 = Module terminated with failure

Return codes are interpreted by the shell depending on which parameter was invoked. For example, if the C parameter is passed to the module for a configuration test and that test fails to find a specific device, a -1 will be passed back to the shell. That particular device will then not be displayed as an installed device on the shell's main menu.

If a -1 is returned for any other parameter besides C, the -1 tells the shell that the module detected an error so that the shell will display the message "Failed" on its main menu.

If no errors are detected on the test run, a 0 is returned to the shell to indicate that the test was passed successfully and the message "Passed" will be displayed on the main menu.

ERROR LOG FILE

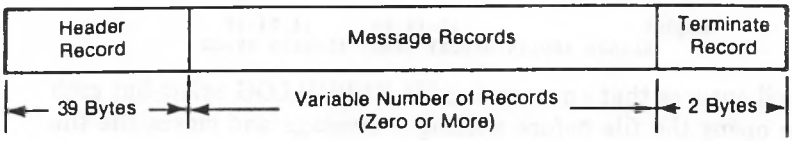
An error logging system is provided with the PC6 diagnostics. Each test module writes error messages in an error log file to be displayed at a later time. All messages written to the file are appended to any messages written there previously.

The name of the error file is ERROR.LOG. The contents of the file are all ASCII characters.

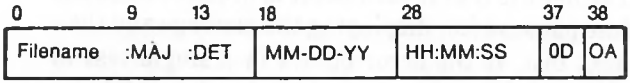
Error messages have the format shown in Figure 5-3. Contained in the messages is a header record, a number of message records, and a terminate record.

The header record consists of the filename of the test module that detected the error, the code of the error in service diagnostics, as well as the date and time of the test.

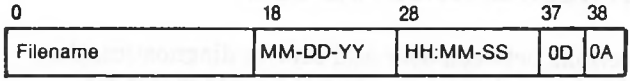
The message record consists of a field of 4 blanks followed by a variable length text field. There can be none or several message records in an error message.



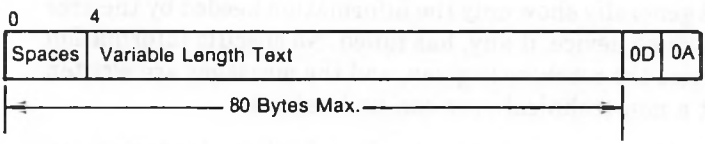
A. Header Record:
1) Service Diagnostics



2) User Diagnostics



B. Message Record:



C. Terminate Record:

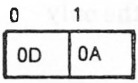


Figure 5-3 Error Message Format

Each header record and message record is followed by a carriage-return line-feed for formatting purposes.

The final record in an error message is the terminate record. It provides an additional carriage-return line-feed so that a blank line is displayed when viewing the error log file.

For example, a typical error message in service diagnostics looks like this:

```
MEMORY :  03: 01        12-12-84      14:34:56
     EXP DATA: 0325    OBS DATA:  0345
```

The same message in user diagnostics looks like this:

```
MEMORY                    18-18-84      14:34:56
     RANDOM ACCESS MEMORY (RAM) ADDRESS ERROR
```

The shell ensures that an error log file ERROR.LOG exists but each module opens the file before writing a message and closes the file before terminating.

The message is displayed on the video display as well as being logged in the error log file. If either the G or R parameter is in effect when the error occurs, the module pauses after displaying the message and then continues with the next test. If the error occurs in a single test in service diagnostics, the module prompts you for a key to continue.

DISTINCTIONS BETWEEN SERVICE AND USER DIAGNOSTICS

There are two distinctions between user and service diagnostics, the flexibility of test selection and the format of the error messages.

User diagnostics are intended for the final user of the PC6 computer and generally show only the information needed by the user to determine which device, if any, has failed. No specific information on how to service the machine is given, and the messages are written in terms that a non-technical user can understand.

Service diagnostics are intended for use by a field service technician to determine as closely as possible the source of an error. Service diagnostics show a menu of test choices if the S parameter is the only one selected from the main menu.

The error messages for service diagnostics contain error codes that are much more specific than the messages in user diagnostics. The messages contain as much information as necessary, e.g., expected data, observed data, and parameter values. A complete description of these messages is included in the HARDWARE MAINTENANCE AND SERVICE MANUAL.

KEYBOARD DEFINITION

The keys which are defined for the PC6 diagnostics and test module operation are:

F1	Explanation of selections (Help)
F2	Terminate test module (Stop)
F3	Return to previous menu
F4	Stop test run. Used to stop a continuous run at any level of test

F5	Not defined
F6	Display utilities menu
F7	Run all tests once (Group Test)
F8	Run this test repeatedly until stopped
F9	Add a test module to the shell
F10	Exit to DOS

ENTER	Terminates any keyboard entry
PgUp	Display previous screen
PgDn	Display next screen
ESC	Cancel selection

SAMPLE SCREENS

Figure 5-4 and Figure 5-5 show two typical diagnostics screens, one from user diagnostics and one from service diagnostics.

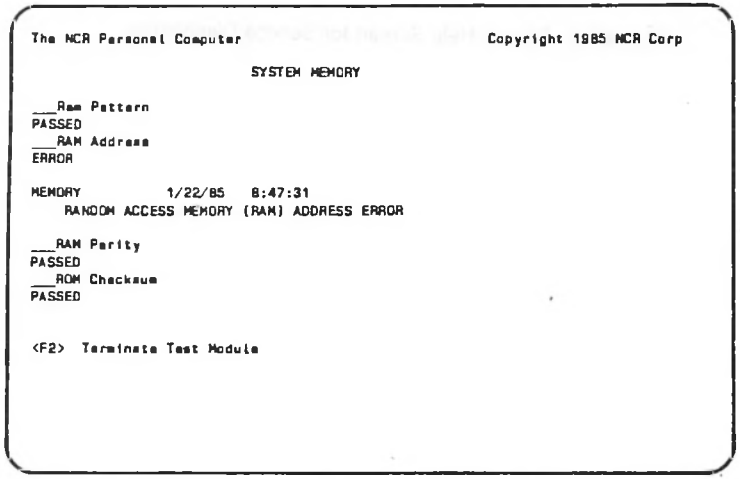


Figure 5-4 Typical Error Message for User Diagnostics

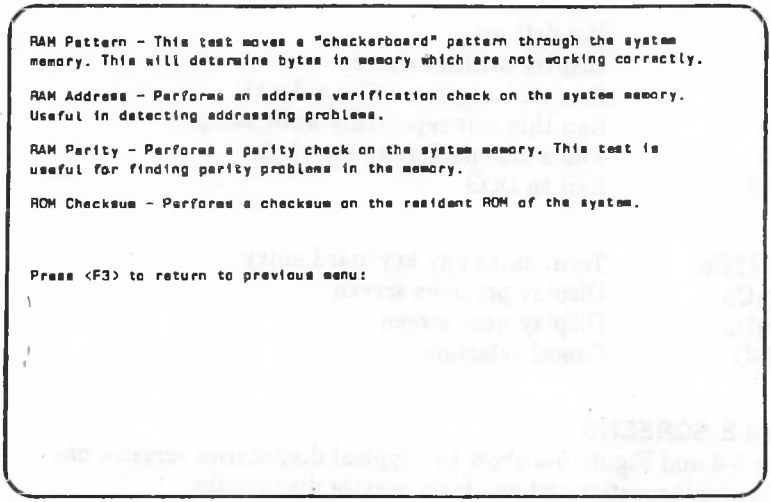


Figure 5-5 Typical Help Screen for Service Diagnostics

Character Set and Color Attributes

This appendix contains a set of two tables presenting the following character set and display attribute information:

- Keystrokes required to display each displayable character.
- Hex values that must be specified in the attribute byte for the various display attribute configurations.

KEYSTROKES

KEYSTROKES

Character Value		Characters/Keystrokes	
Hex	Dec	Symbol	Keystrokes
00	0	Blank (Null)	Ctrl 2
01	1	☺	Ctrl A
02	2	☻	Ctrl B
03	3	♥	Ctrl C
04	4	♦	Ctrl D
05	5	♣	Ctrl E
06	6	♠	Ctrl F
07	7	•	Ctrl G
08	8		Ctrl H Backspace, Shift Backspace
09	9	○	Ctrl
0A	10		Ctrl J Ctrl ↵
0B	11	♂	Ctrl K
0C	12	♀	Ctrl L
0D	13	♪	Ctrl M, ↵, Shift ↵
0E	14	♫	Ctrl N
0F	15	☼	Ctrl O
10	16	►	Ctrl P
11	17	◄	Ctrl Q
12	18	↕	Ctrl R
13	19	‼	Ctrl S
14	20	¶	Ctrl T
15	21	§	Ctrl U
16	22	▬	Ctrl V
17	23	↨	Ctrl W

1 of 10

Character Value		Characters/Keystrokes	
Hex	Dec	Symbol	Keystrokes
18	24	↑	Ctrl X
19	25	↓	Ctrl Y
1A	26	→	Ctrl Z
1B	27	←	Ctrl [, Esc, Shift Esc, Ctrl Esc
1C	28	∟	Ctrl \
1D	29	↔	Ctrl]
1E	30	▲	Ctrl 6
1F	31	▼	Ctrl —
20	32	Blank Space	Space Bar, Shift, Space, Ctrl Space, Alt Space
21	33	!	!
22	34	"	"
23	35	#	#
24	36	$	$
25	37	%	%
26	38	&	&
27	39	'	'
28	40	(	(
29	41	)	)
2A	42	*	*
2B	43	+	+
2C	44	,	,
2D	45	—	—
2E	46		.

2 of 10

Character Value		Characters/Keystrokes	
Hex	Dec	Symbol	Keystrokes
2F	47	/	/
30	48	0	0
31	49	1	1
32	50	2	2
33	51	3	3
34	52	4	4
35	53	5	5
36	54	6	6
37	55	7	7
38	56	8	8
39	57	9	9
3A	58	:	:
3B	59	;	;
3C	60	<	<
3D	61	=	=
3E	62	>	>
3F	63	?	?
40	64	@	@
41	65	A	A
42	66	B	B
43	67	C	C
44	68	D	D
45	69	E	E
46	70	F	F
47	71	G	G
48	72	H	H
49	73	I	I
4A	74	J	J

3 of 10

Character Value		Characters/Keystrokes	
Hex	Dec	Symbol	Keystrokes
4B	75	K	K
4C	76	L	L
4D	77	M	M
4E	78	N	N
4F	79	O	O
50	80	P	P
51	81	Q	Q
52	82	R	R
53	83	S	S
54	84	T	T
55	85	U	U
56	86	V	V
57	87	W	W
58	88	X	X
59	89	Y	Y
5A	90	Z	Z
5B	91	[	[
5C	92	\	\
5D	93	]	]
5E	94	^	^
5F	95	_	_
60	96	`	`
61	97	a	a
62	98	b	b
63	99	c	c
64	100	d	d
65	101	e	e
66	102	f	f

4 of 10

Character Value		Characters/Keystrokes	
Hex	Dec	Symbol	Keystrokes
67	103	g	g
68	104	h	h
69	105	i	i
6A	106	j	j
6B	107	k	k
6C	108	l	l
6D	109	m	m
6E	110	n	n
6F	111	o	o
70	112	p	p
71	113	q	q
72	114	r	r
73	115	s	s
74	116	t	t
75	117	u	u
6	118	v	v
77	119	w	w
78	120	x	x
79	121	y	y
7A	122	z	z
7B	123	{	{
7C	124	|	|
7D	125	}	}
7E	126	~	~
7F	127	△	Ctrl -

5 of 10

Character Value		Characters/Keystrokes	
Hex	Dec	Symbol	Keystrokes
80	128	Ç	Alt 128
81	129	ü	Alt 129
82	130	é	Alt 130
83	131	â	Alt 131
84	132	ä	Alt 132
85	133	à	Alt 133
86	134	a	Alt 134
87	135	ç	Alt 135
88	136	ê	Alt 136
89	137	ë	Alt 137
8A	138	è	Alt 138
8B	139	ï	Alt 139
8C	140	î	Alt 140
8D	141	ì	Alt 141
8E	142	Ä	Alt 142
8F	143	Å	Alt 143
90	144	É	Alt 144
91	145	æ	Alt 145
92	146	Æ	Alt 146
93	147	ô	Alt 147
94	148	ö	Alt 148
95	149	ò	Alt 149
96	150	û	Alt 150
97	151	ù	Alt 151
98	152	ÿ	Alt 152
99	153	ö	Alt 153
9A	154	ü	Alt 154

Note 1: Keystrokes Alt 128 and higher must use the numeric keypad

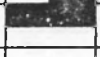
6 of 10

Character Value		Characters/Keystrokes	
Hex	Dec	Symbol	Keystrokes
9B	155	¢	Alt 155
9C	156	£	Alt 156
9D	157	Y	Alt 157
9E	158	Pt	Alt 158
9F	159	ƒ	Alt 159
A0	160	á	Alt 160
A1	161	í	Alt 161
A2	162	ó	Alt 162
A3	163	ú	Alt 163
A4	164	ñ	Alt 164
A5	165	Ñ	Alt 165
A6	166	ª	Alt 166
A7	167	º	Alt 167
A8	168	¿	Alt 168
A9	169	⌐	Alt 169
AA	170	¬	Alt 170
AB	171	1/2	Alt 171
AC	172	1/4	Alt 172
AD	173	¡	Alt 173
AE	174	<<	Alt 174
AF	175	>>	Alt 175
B0	176		Alt 176
B1	177	▒	Alt 177
B2	178	▓	Alt 178
B3	179	│	Alt 179
B4	180	┤	Alt 180
B5	181	╡	Alt 181
B6	182	╢	Alt 182

Note 1: Keystrokes Alt 128 and higher must use the numeric keypad

Character Value		Characters/Keystrokes	
Hex	Dec	Symbol	Keystrokes
B7	183	╖	Alt 183
B8	184	╕	Alt 184
B9	185	╣	Alt 185
BA	186	║	Alt 186
BB	187	╗	Alt 187
BC	188	╝	Alt 188
BD	189	╜	Alt 189
BE	190	╛	Alt 190
BF	191	┐	Alt 191
C0	192	└	Alt 192
C1	193	┴	Alt 193
C2	194	┬	Alt 194
C3	195	├	Alt 195
C4	196	─	Alt 196
C5	197	┼	Alt 197
C6	198	╞	Alt 198
C7	199	╟	Alt 199
C8	200	╚	Alt 200
C9	201	╔	Alt 201
CA	202	╩	Alt 202
CB	203	╦	Alt 203
CC	204	╠	Alt 204
CD	205	═	Alt 205
CE	206	╬	Alt 206
CF	207	╧	Alt 207
D0	208	╨	Alt 208

Note 1: Keystrokes Alt 128 and higher must use the numeric keypad

Character Value		Characters/Keystrokes	
Hex	Dec	Symbol	Keystrokes
D1	209	╤	Alt 209
D2	210	╥	Alt 210
D3	211	╙	Alt 211
D4	212	╘	Alt 212
D5	213	╒	Alt 213
D6	214	╓	Alt 214
D7	215	╫	Alt 215
D8	216	╪	Alt 216
D9	217	┘	Alt 217
DA	218	┌	Alt 218
DB	219		Alt 219
DC	220		Alt 220
DD	221		Alt 221
DE	222		Alt 222
DF	223		Alt 223
E0	224	α	Alt 224
E1	225	ß	Alt 225
E2	226	Γ	Alt 226
E3	227	π	Alt 227
E4	228	Σ	Alt 228
E5	229	σ	Alt 229
E6	230	µ	Alt 230
E7	231	τ	Alt 231
E8	232	Φ	Alt 232
E9	233	Θ	Alt 233
EA	234	Ω	Alt 234
EB	235	δ	Alt 235

Note 1: Keystrokes Alt 128 and higher must use the numeric keypad

9 of 10

Character Value		Characters/Keystrokes	
Hex	Dec	Symbol	Keystrokes
EC	236	∞	Alt 236
ED	237	ø	Alt 237
EE	238	ε	Alt 238
EF	239	∩	Alt 239
F0	240	≡	Alt 240
F1	241	±	Alt 241
F2	242	≥	Alt 242
F3	243	≤	Alt 243
F4	244	⌠	Alt 244
F5	245	⌡	Alt 245
F6	246	÷	Alt 246
F7	247	≈	Alt 247
F8	248	°	Alt 248
F9	249	∙	Alt 249
FA	250	·	Alt 250
FB	251	√	Alt 251
FC	252	n	Alt 252
FD	253	2	Alt 253
FE	254	■	Alt 254
FF	255	BLANK	Alt 255

Note 1: Keystrokes Alt 128 and higher must use the numeric keypad

10 of 10

DISPLAY ATTRIBUTES

Character Value		Display Attributes		
		Color/Graphics		Monochrome
Hex	Dec	Background	Foreground	
00	0	Black	Black	Non-Display
01	1	Black	Blue	Underline
02	2	Black	Green	Normal
03	3	Black	Cyan	Normal
04	4	Black	Red	Normal
05	5	Black	Magenta	Normal
06	6	Black	Brown	Normal
07	7	Black	Light Grey	Normal
08	8	Black	Dark Grey	Non-Display
09	9	Black	Light Blue	High Intensity Underline
0A	10	Black	Light Green	High Intensity
0B	11	Black	Light Green	High Intensity
0C	12	Black	Light Red	High Intensity
0D	13	Black	Light Magenta	High Intensity
0E	14	Black	Yellow	High Intensity
0F	15	Black	White	High Intensity
10	16	Blue	Black	Normal
11	17	Blue	Blue	Underline
12	18	Blue	Green	Normal
13	19	Blue	Cyan	Normal
14	20	Blue	Red	Normal
15	21		Magenta	Normal
16	22	Blue	Brown	Normal
17	23	Blue	Light Grey	Normal

Character Value		Display Attributes		
		Color/Graphics		Monochrome
Hex	Dec	Background	Foreground	
18	24	Blue	Dark Grey	High Intensity
19	25	Blue	Light Blue	High Intensity Underline
1A	26	Blue	Light Green	High Intensity
1B	27	Blue	Light Cyan	High Intensity
1C	28	Blue	Light Red	High Intensity
1D	29	Blue	Light Magenta	High Intensity
1E	30	Blue	Yellow	High Intensity
1F	31	Blue	White	High Intensity
20	32	Green	Black	Normal
21	33	Green	Blue	Underline
22	34	Green	Green	Normal
23	35	Green	Cyan	Normal
24	36	Green	Red	Normal
25	37	Green	Magenta	Normal
26	38	Green	Brown	Normal
27	39	Green	Light Grey	Normal
28	40	Green	Dark Grey	High Intensity
29	41	Green	Light Blue	High Intensity Underline
2A	42	Green	Light Green	High Intensity
2B	43	Green	Light Cyan	High Intensity
2C	44	Green	Light Red	High Intensity
2D	45	Green	Light Magenta	High Intensity
2E	46	Green	Yellow	High Intensity

Character Value		Display Attributes		
		Color/Graphics		Monochrome
Hex	Dec	Background	Foreground	
2F	47	Green	White	High Intensity
30	48	Cyan	Black	Normal
31	49	Cyan	Blue	Underline
32	50	Cyan	Green	Normal
33	51	Cyan	Cyan	Normal
34	52	Cyan	Red	Normal
35	53	Cyan	Magenta	Normal
36	54	Cyan	Brown	Normal
37	55	Cyan	Light Grey	Normal
38	56	Cyan	Dark Grey	High Intensity
39	57	Cyan	Light Blue	High Intensity Underline
3A	58	Cyan	Light Green	High Intensity
3B	59	Cyan	Light Cyan	High Intensity
3C	60	Cyan	Light Red	High Intensity
3D	61	Cyan	Light Magenta	High Intensity
3E	62	Cyan	Yellow	High Intensity
3F	63	Cyan	White	High Intensity
40	64	Red	Black	Normal
41	65	Red	Blue	Underline
42	66	Red	Green	Normal
43	67	Red	Cyan	Normal
44	68	Red	Red	Normal
45	69	Red	Magenta	Normal
46	70	Red	Brown	Normal
47	71	Red	Light Grey	Normal
48	72	Red	Dark Grey	High Intensity
49	73	Red	Light Blue	High Intensity Underline
4A	74	Red	Light Green	High Intensity

Character Value		Display Attributes		
		Color/Graphics		Monochrome
Hex	Dec	Background	Foreground	
4B	75	Red	Light Cyan	High Intensity
4C	76	Red	Light Red	High Intensity
4D	77	Red	Light Magenta	High Intensity
4E	78	Red	Yellow	High Intensity
4F	79	Red	White	High Intensity
50	80	Magenta	Black	Normal
51	81	Magenta	Blue	Underline
52	82	Magenta	Green	Normal
53	83	Magenta	Cyan	Normal
54	84	Magenta	Red	Normal
55	85	Magenta	Magenta	Normal
56	86	Magenta	Brown	Normal
57	87	Magenta	Light Grey	Normal
58	88	Magenta	Dark Grey	High Intensity
59	89	Magenta	Light Blue	High Intensity Underline
5A	90	Magenta	Light Green	High Intensity
5B	91	Magenta	Light Cyan	High Intensity
5C	92	Magenta	Light Red	High Intensity
5D	93	Magenta	Light Magenta	High Intensity
5E	94	Magenta	Yellow	High Intensity
5F	95	Magenta	White	High Intensity
60	96	Yellow	Black	Normal
61	97	Yellow	Blue	Underline
62	98	Yellow	Green	Normal
63	99	Yellow	Cyan	Normal
64	100	Yellow	Red	Normal
65	101	Yellow	Magenta	Normal
66	102	Yellow	Brown	Normal

Character Value		Display Attributes		
		Color/Graphics		Monochrome
Hex	Dec	Background	Foreground	
67	103	Yellow	Light Grey	Normal
68	104	Yellow	Dark Grey	High Intensity
69	105	Yellow	Light Blue	High Intensity Underline
6A	106	Yellow	Light Green	High Intensity
6B	107	Yellow	Light Cyan	High Intensity
6C	108	Yellow	Light Red	High Intensity
6D	109	Yellow	Light Magenta	High Intensity
6E	110	Yellow	Yellow	High Intensity
6F	111	Yellow	White	High Intensity
70	112	White	Black	Reverse Video
71	113	White	Blue	Underline
72	114	White	Green	Normal
73	115	White	Cyan	Normal
74	116	White	Red	Normal
75	117	White	Magenta	Normal
76	118	White	Brown	Normal
77	119	White	Light Grey	Normal
78	120	White	Dark Grey	Reverse Video
79	121	White	Light Blue	High Intensity Underline
7A	122	White	Light Green	High Intensity
7B	123	White	Light Cyan	High Intensity
7C	124	White	Light Red	High Intensity
7D	125	White	Light Magenta	High Intensity
7E	126	White	Yellow	High Intensity
7F	127	White	White	High Intensity

Character Value		Display Attributes		
		Color/Graphics		Monochrome
Hex	Dec	Background	Foreground	
80 to FF Hex are Flashing in both Color & Monochrome				
80	128	Black	Black	Non-Display
81	129	Black	Blue	Underline
82	130	Black	Green	Normal
83	131	Black	Cyan	Normal
84	132	Black	Red	Normal
85	133	Black	Magenta	Normal
86	134	Black	Brown	Normal
87	135	Black	Light Grey	Normal
88	136	Black	Dark Grey	Non-Display
89	137	Black	Light Blue	High Intensity Underline
8A	138	Black	Light Green	High Intensity
8B	139	Black	Light Cyan	High Intensity
8C	140	Black	Light Red	High Intensity
8D	141	Black	Light Magenta	High Intensity
8E	142	Black	Yellow	High Intensity
8F	143	Black	White	High Intensity
90	144	Blue	Black	Normal
91	145	Blue	Blue	Underline
92	146	Blue	Green	Normal
93	147	Blue	Cyan	Normal
94	148	Blue	Red	Normal
95	149	Blue	Magenta	Normal
96	150	Blue	Brown	Normal
97	151	Blue	Light Grey	Normal
98	152	Blue	Dark Grey	High Intensity
99	153	Blue	Light Blue	High Intensity Underline
9A	154	Blue	Light Green	High Intensity

Character Value		Display Attributes		
		Color/Graphics		Monochrome
Hex	Dec	Background	Foreground	
9B	155	Blue	Light Cyan	High Intensity
9C	156	Blue	Light Red	High Intensity
9D	157	Blue	Light Magenta	High Intensity
9E	158	Blue	Yellow	High Intensity
9F	159	Blue	White	High Intensity
A0	160	Green	Black	Normal
A1	161	Green	Blue	Underline
A2	162	Green	Green	Normal
A3	163	Green	Cyan	Normal
A4	164	Green	Red	Normal
A5	165	Green	Magenta	Normal
A6	166	Green	Brown	Normal
A7	167	Green	Light Grey	Normal
A8	168	Green	Dark Grey	High Intensity
A9	169	Green	Light Blue	High Intensity Underline
AA	170	Green	Light Green	High Intensity
AB	171	Green	Light Cyan	High Intensity
AC	172	Green	Light Red	High Intensity
AD	173	Green	Light Magenta	High Intensity
AE	174	Green	Yellow	High Intensity
AF	175	Green	White	High Intensity
B0	176	Cyan	Black	Normal
B1	177	Cyan	Blue	Underline
B2	178	Cyan	Green	Normal
B3	179	Cyan	Cyan	Normal
B4	180	Cyan	Red	Normal
B5	181	Cyan	Magenta	Normal
B6	182	Cyan	Brown	Normal

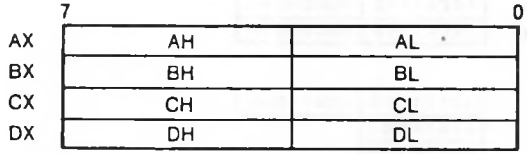
Character Value		Display Attributes		
		Color/Graphics		Monochrome
Hex	Dec	Background	Foreground	
B7	183	Cyan	Light Grey	Normal
B8	184	Cyan	Dark Grey	High Intensity
B9	185	Cyan	Light Blue	High Intensity Underline
BA	186	Cyan	Light Green	High Intensity
BB	187	Cyan	Light Cyan	High Intensity
BC	188	Cyan	Light Red	High Intensity
BD	189	Cyan	Light Magenta	High Intensity
BE	190	Cyan	Yellow	High Intensity
BF	191	Cyan	White	High Intensity
C0	192	Red	Black	Normal
C11	193	Red	Blue	Underline
C2	194	Red	Green	Normal
C3	195	Red	Cyan	Normal
C4	196	Red	Red	Normal
C5	197	Red	Magenta	Normal
C6	198	Red	Brown	Normal
C7	199	Red	Light Grey	Normal
C8	200	Red	Dark Grey	High Intensity
C9	201	Red	Light Blue	High Intensity Underline
CA	202	Red	Light Green	High Intensity
CB	203	Red	Light Cyan	High Intensity
CC	204	Red	Light Red	High Intensity
CD	205	Red	Light Magenta	High Intensity
CE	206	Red	Yellow	High Intensity
CF	207	Red	White	High Intensity
D0	208	Magenta	Black	Normal

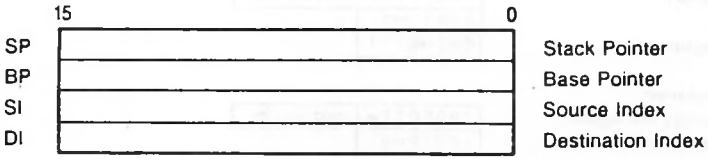
Character Value		Display Attributes		
		Color/Graphics		Monochrome
Hex	Dec	Background	Foreground	
D1	209	Magenta	Blue	Underline
D2	210	Magenta	Green	Normal
D3	211	Magenta	Cyan	Normal
D4	212	Magenta	Red	Normal
D5	213	Magenta	Magenta	Normal
D6	214	Magenta	Brown	Normal
D7	215	Magenta	Light Grey	Normal
D8	216	Magenta	Dark Grey	High Intensity
D9	217	Magenta	Light Blue	High Intensity Underline
DA	218	Magenta	Light Green	High Intensity
DB	219	Magenta	Light Cyan	High Intensity
DC	220	Magenta	Light Red	High Intensity
DD	221	Magenta	Light Magenta	High Intensity
DE	222	Magenta	Yellow	High Intensity
DF	223	Magenta	White	High Intensity
E0	224	Yellow	Black	Normal
E1	225	Yellow	Blue	Underline
E2	226	Yellow	Green	Normal
E3	227	Yellow	Cyan	Normal
E4	228	Yellow	Red	Normal
E5	229	Yellow	Magenta	Normal
E6	230	Yellow	Brown	Normal
E7	231	Yellow	Light Grey	Normal
E8	232	Yellow	Dark Grey	High Intensity
E9	233	Yellow	Light Blue	High Intensity Underline
EA	234	Yellow	Light Green	High Intensity
EB	235	Yellow	Light Cyan	High Intensity

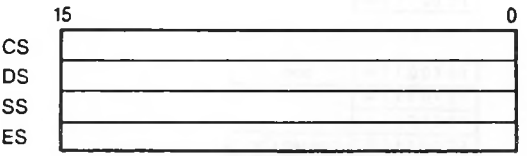
Character Value		Display Attributes		
		Color/Graphics		Monochrome
Hex	Dec	Background	Foreground	
EC	236	Yellow	Light Red	High Intensity
ED	237	Yellow	Light Magenta	High Intensity
EE	238	Yellow	Yellow	High Intensity
EF	239	Yellow	White	High Intensity
F0	240	White	Black	Reverse Video
F1	241	White	Blue	Underline
F2	242	White	Green	Normal
F3	243	White	Cyan	Normal
F4	244	White	Red	Normal
F5	245	White	Magenta	Normal
F6	246	White	Brown	Normal
F7	247	White	Light Grey	Normal
F8	248	White	Dark Grey	Reverse Video
F9	249	White	Light Blue	High Intensity Underline
FA	250	White	Light Green	High Intensity
FB	251	White	Light Cyan	High Intensity
FC	252	White	Light Red	High intensity
FD	253	White	Light Magenta	High Intensity
FE	254	White	Yellow	High Intensity
FF	255	White	White	High Intensity

8088-2 Register Structure

The following tables show the 8088-2 register structure. Additional information in note form is given at the end of this appendix.

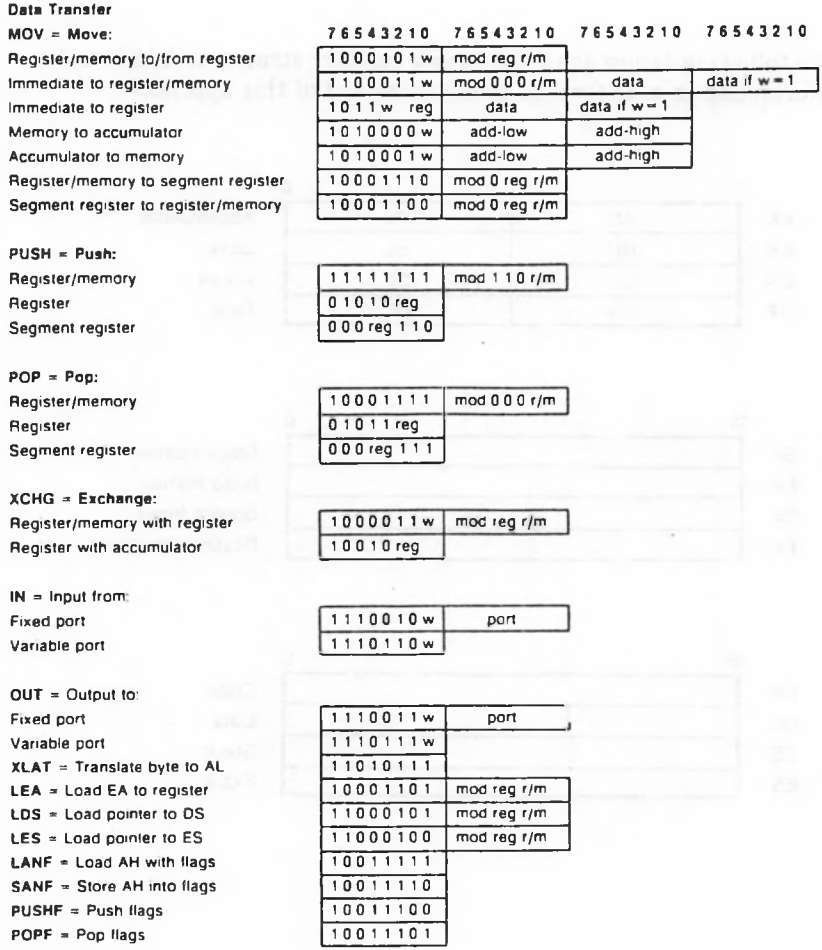






8088-2 INSTRUCTION SET SUMMARY

The following tables summarize the 8088-2 instruction set. Additional information in note form is given after the tables at the end of this appendix.



Data Transfer	76543210	76543210	76543210	76543210
MOV = Move:				
Register/memory to/from register	1000101w	mod reg r/m		
Immediate to register/memory	1100011w	mod 000 r/m	data	data if w = 1
Immediate to register	1011w reg	data	data if w = 1	
Memory to accumulator	1010000w	add-low	add-high	
Accumulator to memory	1010001w	add-low	add-high	
Register/memory to segment register	10001110	mod 0 reg r/m		
Segment register to register/memory	10001100	mod 0 reg r/m		
PUSH = Push:				
Register/memory	11111111	mod 110 r/m		
Register	01010 reg			
Segment register	000 reg 110			
POP = Pop:				
Register/memory	10001111	mod 000 r/m		
Register	01011 reg			
Segment register	000 reg 111			
XCHG = Exchange:				
Register/memory with register	1000011w	mod reg r/m		
Register with accumulator	10010 reg			
IN = Input from:				
Fixed port	1110010w	port		
Variable port	1110110w			
OUT = Output to:				
Fixed port	1110011w	port		
Variable port	1110111w			
XLAT = Translate byte to AL	11010111			
LEA = Load EA to register	10001101	mod reg r/m		
LDS = Load pointer to DS	11000101	mod reg r/m		
LES = Load pointer to ES	11000100	mod reg r/m		
LANF = Load AH with flags	10011111			
SANF = Store AH into flags	10011110			
PUSHF = Push flags	10011100			
POPF = Pop flags	10011101			

Data Transfer

Logic

	76543210	76543210	76543210	76543210
NOT Invert	1111011 w	mod 010 r/m		
SHL/SAL Shift logical arithmetic left	110100 v w	mod 100 r/m		
SHR Shift logical right	110100 v w	mod 101 r/m		
SAR Shift arithmetic right	110100 v w	mod 111 r/m		
ROL Rotate left	110100 v w	mod 000 r/m		
ROR Rotate right	110100 v w	mod 001 r/m		
RCL Rotate through carry flag left	110100 v w	mod 010 r/m		
RCR Rotate through carry right	110100 v w	mod 011 r/m		
AND = And:				
Reg/memory and register to either	001000 d w	mod reg r/m		
Immediate to register/memory	1000000 w	mod 100 r/m	data	data if w 1
Immediate to accumulator	0010010 w	data	data if w 1	
TEST And function to flags no result:				
Register/memory and register	1000010 w	mod reg r/m		
Immediate data and register/memory	1111011 w	mod 000 r/m	data	data if w 1
Immediate data and accumulator	1010100 w	data	data if w 1	
OR = Or:				
Reg/memory and register to either	000010 d w	mod reg r/m		
Immediate to register/memory	1000000 w	mod 001 r/m	data	data if w 1
Immediate to accumulator	0000110 w	data	data if w 1	
XOR = Exclusive or:				
Reg/memory and register to either	001100 d w	mod reg r/m		
Immediate to register/memory	1000000 w	mod 110 r/m	data	data if w 1
Immediate to accumulator	0011010 w	data	data if w 1	

Logic

Arithmetic

	76543210	76543210	76543210	76543210
ADD = Add:				
Reg/memory with register to either	000000dw	mod reg r/m		
Immediate to register/memory	100000sw	mod 000 r/m	data	data if s w 01
Immediate to accumulator	0000010w	data	data if w 1	
ADC = Add with carry:				
Reg/memory with register to either	000100dw	mod reg r/m		
Immediate to register/memory	100000sw	mod 010 r/m	data	data if s w 01
Immediate to accumulator	0001010w	data	data if w 1	
INC = Increment:				
Register/memory	1111111w	mod 000 r/m		
Register	01000 reg			
AAA = ASCII adjust for add	00110111			
DAA = Decimal adjust for add	00100111			
SUB = Subtract:				
Reg/memory and register to either	001010dw	mod reg r/m		
Immediate from register/memory	100000sw	mod 101 r/m	data	data if s w 01
Immediate from accumulator	0010110w	data	data if w 1	
SBB = Subtract with borrow				
Reg/memory and register to either	000110dw	mod reg r/m		
Immediate from register/memory	100000sw	mod 011 r/m	data	data if s w 01
Immediate from accumulator	0001110w	data	data if w 1	
DEC Decrement				
Register/memory	1111111w	mod 001 r/m		
Register	01001 reg			
REG Change sign	1111011w	mod 011 r/m		
CMP = Compare:				
Register/memory and register	001110dw	mod reg r/m		
Immediate with register/memory	100000sw	mod 111 r/m	data	data if s w 01
Immediate with accumulator	0011110w	data	data if w 1	
AAS ASCII adjust for subtract	00111111			
DAS Decimal adjust for subtract	00101111			
MUL Multiply (unsigned)	1111011w	mod 100 r/m		
IMUL Integer multiply (signed)	1111011w	mod 101 r/m		
AAM ASCII adjust for multiply	11010100	00001010		
DIV Divide (unsigned)	1111011w	mod 110 r/m		
IDIV Integer divide (signed)	1111011w	mod 111 r/m		
AAD ASCII adjust for divide	11010101	00001010		
CBW Convert byte to word	10011000			
CWD Convert word to double word	10011001			

Arithmetic

Strng Manipulation	
REP = Repeat	1 1 1 1 0 0 1 2
MOVS = Move byte/word	1 0 1 0 0 1 0 w
CMPS = Compare byte/word	1 0 1 0 0 1 1 w
SCAS = Scan byte/word	1 0 1 0 1 1 1 w
LODS = Load byte/wd to AL/AX	1 0 1 0 1 1 0 w
STOS = Stor byte/wd from AL/A	1 0 1 0 1 0 1 w

String Manipulation

Control Transfer

CALL = Call:	76543210	76543210	76543210
Direct within segment	11101000	disp-low	disp-high
Indirect within segment	11111111	mod 010 r/m	
Direct intersegment	10011010	offset-low	offset-high
		seg-low	seg-high
Indirect intersegment	11111111	mod 011 r/m	

JMP = Unconditional Jump:

Direct within segment	11101001	disp-low	disp-high
Direct with segment-short	11101011	disp	
Indirect within segment	11111111	mod 100 r/m	
Direct intersegment	11101010	offset-low	offset-high
		seg-low	seg-high
Indirect intersegment	11111111	mod 101 r/m	

RET = Return from CALL:

Within segment	11000011		
Within seg adding immed to SP	11000010	data-low	data-high
Intersegment	11001011		
Intersegment adding immediate to SP	11001010	data-low	data-high

JE/JZ = Jump on equal/zero	01110100	disp
JL/JNGE = Jump on less/not greater or equal	01111100	disp
JLE/JNG = Jump on less or equal/not greater	01111110	disp
JB/JNAE = Jump on below/not above or equal	01110010	disp
JBE/JNA = Jump on below or equal/ not above	01110110	disp
JP/JPE = Jump on parity/parity even	01111010	disp
JO = Jump on overflow	01110000	disp
JS = Jump on sign	01111000	disp
JNE/JNZ = Jump on not equal/not zero	01110101	disp
JNL/JGE = Jump on not less/greater or equal	01111101	disp
JNLE/JG = Jump on not less or equal/ greater	01111111	disp
JNB/JAE = Jump on not below/above or equal	01110011	disp
JNBE/JA = Jump on not below or equal/above	01110111	disp
JMP/JPO = Jump on not par/par odd	01111011	disp
JNO = Jump on not overflow	01110001	disp
JNS = Jump on not sign	01111001	disp
LOOP = Loop CX times	11100010	disp
LOOPZ/LOOPE = Loop while zero/equal	11100001	disp
LOOPNZ/LOOPNE = Loop while not zero/equal	11100000	disp
JCXZ = Jump on CX zero	11100011	disp

INT = Interrupt:

Type specified	11001101	type
Type 3	11001100	
INTO Interrupt on overflow	11001110	
IRET Interrupt return	11001111	

Control Transfer

Processor Control	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0
CLC Clear carry	1 1 1 1 1 0 0 0	
CMC Complement carry	1 1 1 1 0 1 0 1	
STC Set carry	1 1 1 1 1 0 0 1	
CLD Clear direction	1 1 1 1 1 1 0 0	
STD Set direction	1 1 1 1 1 1 0 1	
CLI Clear interrupt	1 1 1 1 1 0 1 0	
STI Set interrupt	1 1 1 1 1 0 1 1	
HLT Halt	1 1 1 1 0 1 0 0	
WAIT Wait	1 0 0 1 1 0 1 1	
ESC Escape (to external device)	1 1 0 1 1 x x x	mod x x x r/m
LOCK Bus lock prefix	1 1 1 1 0 0 0 0	
NOP No operation	1 0 0 1 0 0 0 0	

Notes

AL = 8-bit accumulator
AX = 16-bit accumulator
CX = Count register
DS = Data segment
ES = Extra segment
Above/below refers to unsigned value.
Greater = more positive.
Less = less positive (more negative) signed values
if d = 1 then "to" reg; if d = 0 then "from" reg
if w = 1 then word instruction; if w = 0 then byte instruction

if mod = 11 then r/m is treated as a REG field
if mod = 00 then DISP = 0*, disp-low and disp-high are absent
if mod = 01 then DISP = disp-low sign-extended to 16-bits, disp-high is absent
if mod = 10 then DISP = disp-high: disp-low

if r/m = 000 then EA = (BX) + (SI) + DISP
if r/m = 001 then EA = (BX) + (DI) + DISP
if r/m = 010 then EA = (BP) + (SI) + DISP
if r/m = 011 then EA = (BP) + (DI) + DISP
if r/m = 100 then EA = (SI) + DISP
if r/m = 101 then EA = (DI) + DISP
if r/m = 110 then EA = (BP) + DISP*
if r/m = 111 then EA = (BX) + DISP
DISP follows 2nd byte of instruction (before data if required)

*except if mod = 00 and r/m = 110 then EA = disp-high: disp-low.

if s:w = 01 then 16 bits of immediate data form the operand
if s:w = 11 then an immediate data byte is sign extended to
form the 16-bit operand
if v = 0 then "count" = 1, if v = 1 then "count" in (CL)
x = don't care
z is used for string primitives for comparison with ZF FLAG

SEGMENT OVERRIDE PREFIX

0 0 1 reg 1 1 0

Processor Control

REG is assigned according to the following table:

16-Bit (w = 1)		8-Bit (w = 0)		Segment	
000	AX	000	AL	00	ES
001	CX	001	CL	01	CS
010	DX	010	DL	10	SS
011	BX	011	BL	11	DS
100	SP	100	AH		
101	BP	101	CH		
110	SI	110	DH		
111	DI	111	BH		

Instructions which reference the flag register as a 16-bit object use the symbol FLAGS to represent the file:

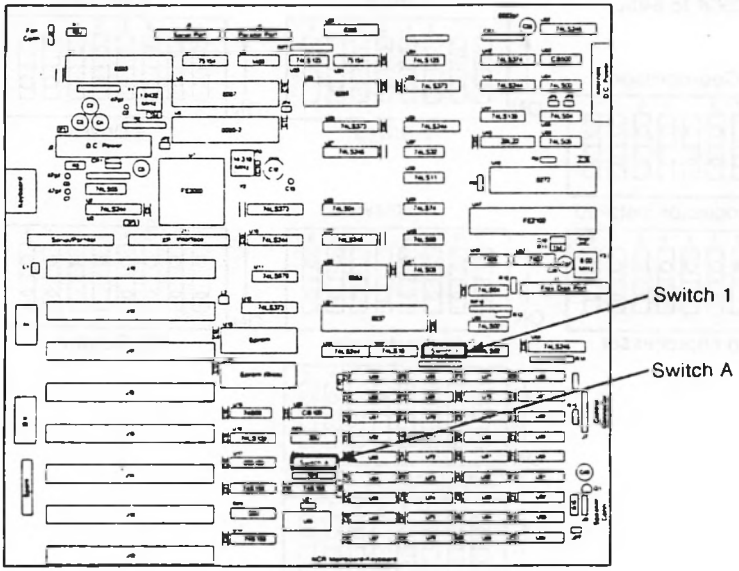
FLAGS = X:X:X:X:(OF):(DF):(IF):(TF):(SF):(ZF):X:(AF):X:(PF):X:(CF)

Switch Configurations

This appendix contains the various settings of the DIP switches on the main processor board and the memory expansion card. Information is also presented describing the system configurations that are defined through the various switch setting combinations.

For the flexible disk drive, the jumper connections for the various drive selection options are documented.

MAIN PROCESSOR BOARD SWITCH SETTINGS



Main Processor Board Configuration Switches

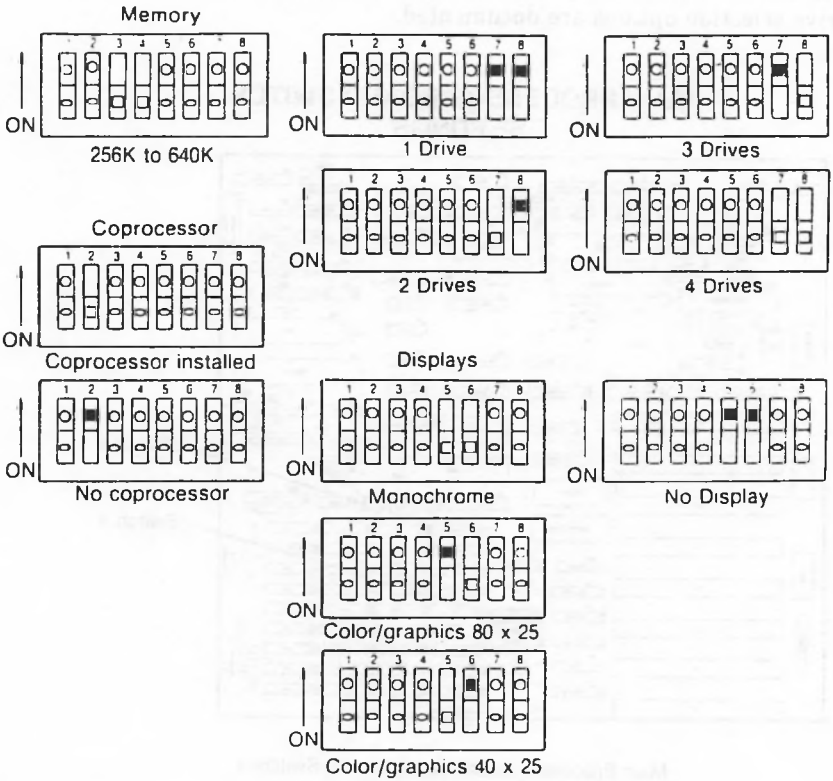
There are two DIP switches located on the main processor board. While these switches do not actually control any circuitry or switch

data lines, they are interpreted by the system software and appropriate action is generated.

Switch one is set to define the amount of memory in the system, the type of CRT used, and whether or not the coprocessor feature is installed.

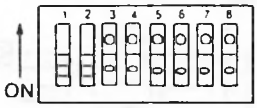
Switch two is set to define the communication and printer channels and informs the main processor board the amount of memory installed and how it is configured.

Switch Number 1 Settings



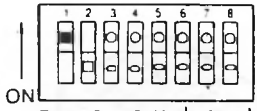
Switch Number A Settings

Memory Bank Options

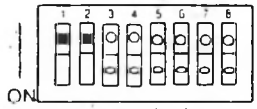


Bank 0 at 64K
Bank 1 at 64K
Bank 2 at 64K
Bank 3 at 64K

Bank 0 at 256K
Bank 1 at 0
Bank 2 at 0
Bank 3 at 0

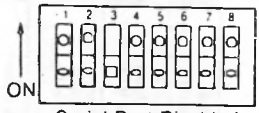


Bank 0 at 64K	64K	
Bank 1 at 64K	64K	
Bank 2 at 256K	256K	
Bank 3 at 256K	64K	

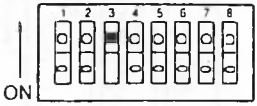


Bank 0 at 256K	256K	256K
Bank 1 at 256K	256K	256K
Bank 2 at 64K	64K	0
Bank 3 at 64K	0	0

Serial Port

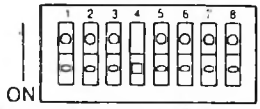


Serial Port Disabled

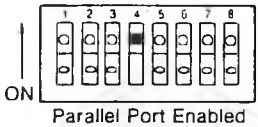


Serial Port Enabled

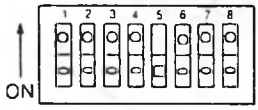
Parallel Port



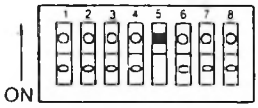
Parallel Port Disabled



Parallel Port Enabled



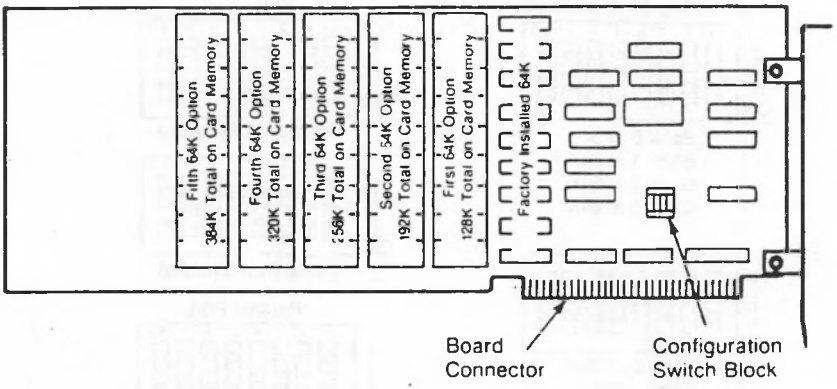
XP Installed



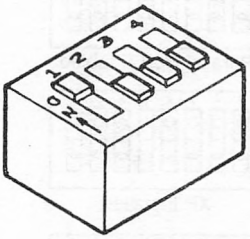
XP Not Installed

* A Memory Expansion Board can be used with these settings.

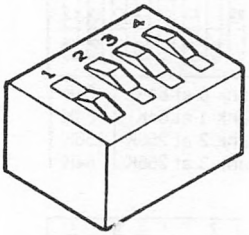
EXPANSION MEMORY BOARD SWITCH SETTINGS



Memory Expansion Card



Slide

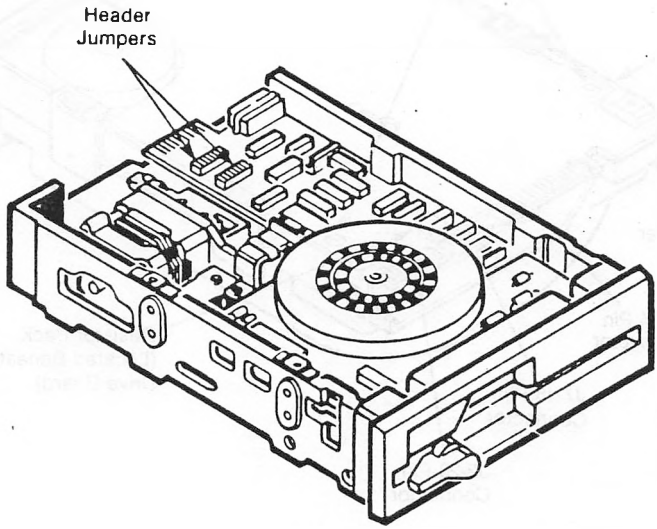


Rocker

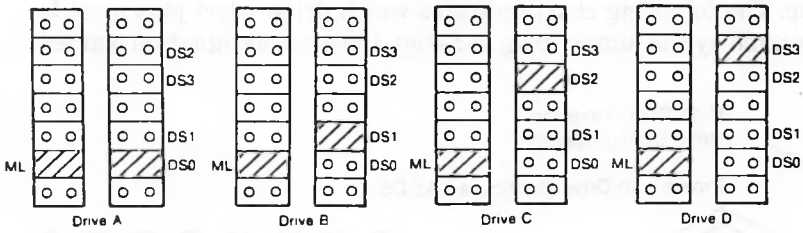
Switch Position Settings				Total Memory on Expansion Card (in KB)	Total Memory in System (256 KB on Main Processor Board)
1	2	3	4		
On	On	On	Off	64	320
Off	On	On	Off	128	384
On	Off	On	Off	192	448
Off	Off	On	Off	256	512
On	On	Off	Off	320	576
Off	On	Off	Off	384	640

FLEXIBLE DISK DRIVE JUMPER HEADERS

The flexible disk drives of the system are selected by connecting a jumper between certain contacts of the header. The following diagrams illustrate the location of the header jumpers on the flexible disk drive unit.

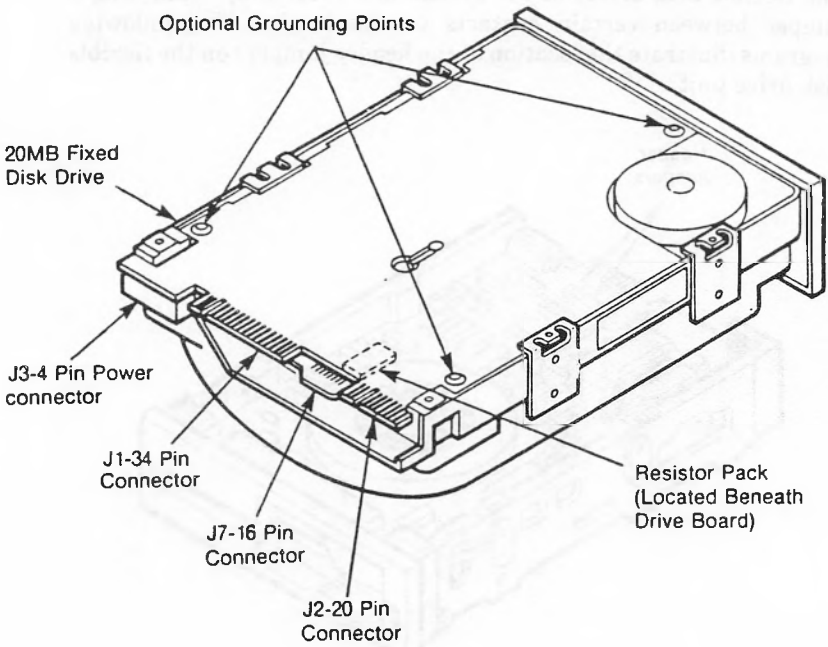


Bottom View



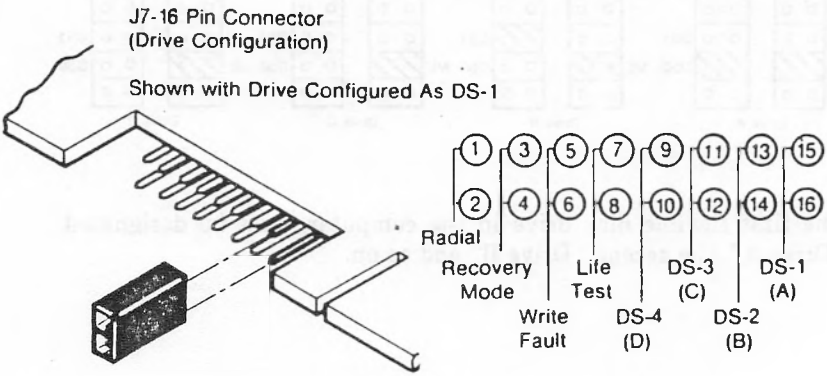
The first flexible disk drive in the computer must be designated "Drive A", the second "Drive B" and so on.

FIXED DISK DRIVE JUMPER HEADERS



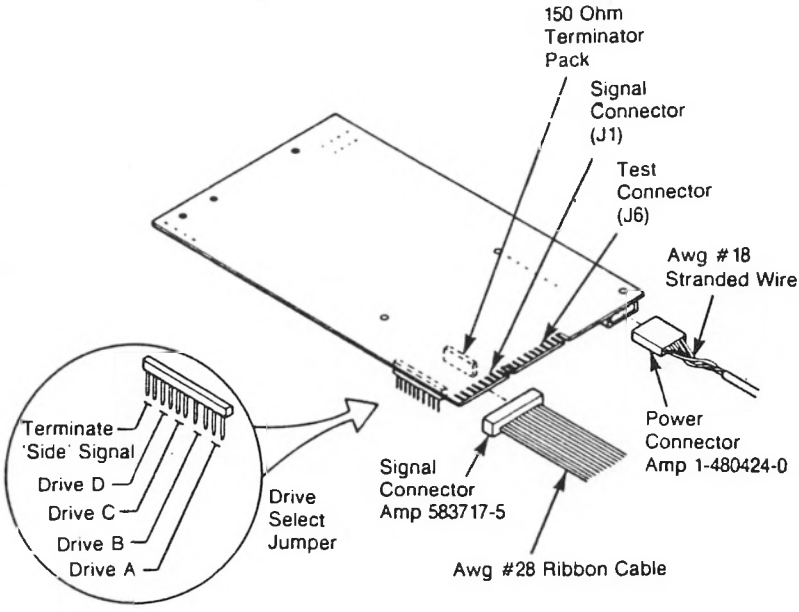
Drive Select Chart

Placing the jumper plug on the appropriate pair of pins on the designator connector, J7, determines which select line activates that drive. The following chart indicates which drive select pins must be connected by the jumper plug to assign the drive designation wanted:



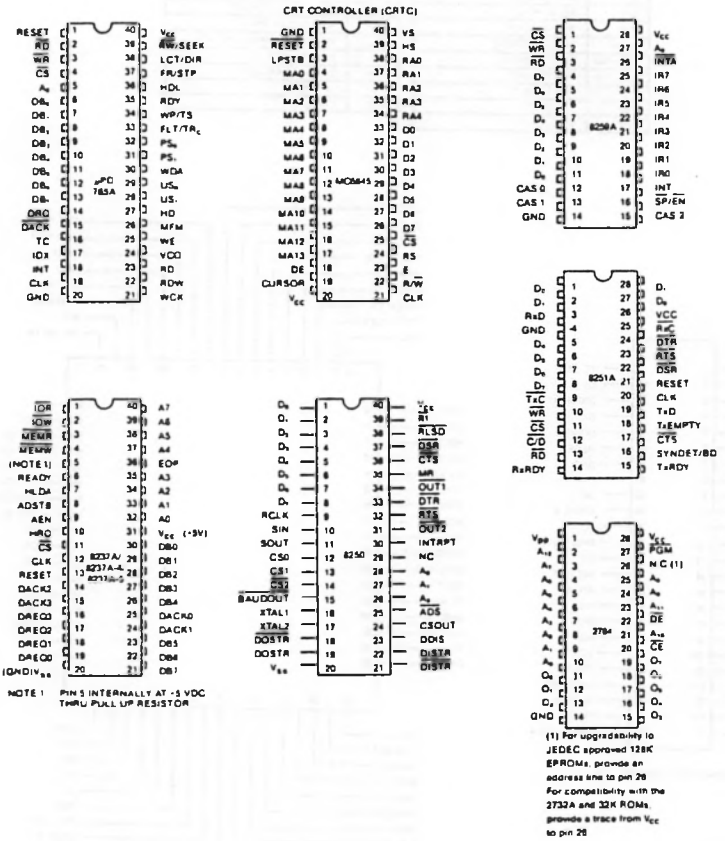
The first fixed disk drive in the computer must be designated "Drive DS-1", the second "Drive DS-2". Drive DS-1 will be automatically assigned one letter value higher than the highest flexible disk drive above "B". Drive DS-2 will be automatically assigned the next higher letter above Drive DS-1.

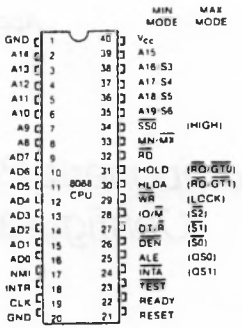
The first tape drive on the cable must be designated to be one number (letter) higher than the highest designation on flexible disk drives. The software will then assign correct designations to all drives in the computer and address them correctly.

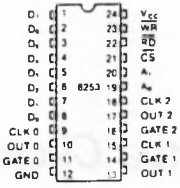


Integrated Circuit Component Pinout Configurations

The following diagram presents the pinout identifications for all of the integrated circuit component types used in the NCR Personal Computer subsystems.

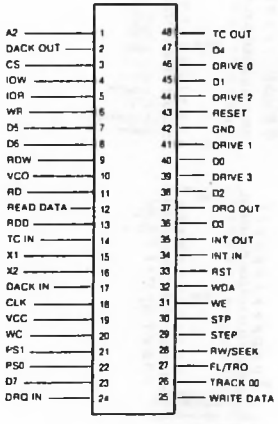




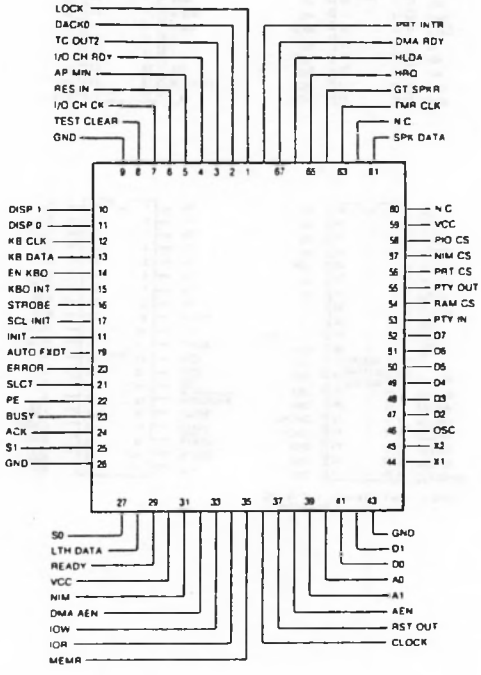


PIN NAMES	
D_7-D_0	DATA BUS (BI-DIRECTIONAL)
RESET	RESET INPUT
CS	CHIP SELECT
RD	READ INPUT
WR	WRITE INPUT
A0-A1	PORT ADDRESS
PA7-PA0	PORT A (8 BIT)
PB7-PB0	PORT B (8 BIT)
PC7-PC0	PORT C (8 BIT)
V_{CC}	+5 VOLTS
GND	5 VOLTS

PIN NAMES	
D_7-D_0	DATA BUS (8 BIT)
CLK N	COUNTER CLOCK INPUTS
GATE N	COUNTER GATE INPUTS
OUT N	COUNTER OUTPUTS
RD	READ COUNTER
WR	WRITE COMMAND OR DATA
CS	CHIP SELECT
A_0-A_1	COUNTER SELECT
V_{CC}	+5 VOLTS
GND	GROUND



FLEXIBLE DISK CONTROLLER



CPU CONTROLLER

Specifications

The sections in this appendix present the specifications for all of the NCR PERSONAL COMPUTER PC6 subsystems.

MAIN PROCESSOR BOARD

INTEL 8088-2 MICROPROCESSOR

- N-channel, silicon gate, NMOS construction
- 16-bit on-board architecture/8-bit data bus interface
- Direct addressing to 1 Megabyte of memory
- 16-bit stacked registers
- Total of 24 operand addressing modes
- 8 and 16 bit arithmetic
  - Binary and decimal
  - Signed and unsigned
  - 4.77MHz clock rate
- Input voltage — 0.5V low; 2.4V high
- Power supply current — 340 mA
- Clock cycle — 200 ns

8259A PROGRAMMABLE INTERRUPT CONTROLLER

- Standard levels of priority — 8
  - Expandable levels of priority — 64

- NMOS construction
- Input voltage — 0.5V low; 2.4V high
- Input current — 85 mA
- Duration of interrupt acknowledge cycle — 160 ns

8288 BUS CONTROLLER

- Bipolar bus driving capability
- 3 status lines
- Input voltage — 0.8V low; 2.4V high
- Supply current — 230mA
- Duration of clock cycle — 100 ns minimum
- Power consumption — 1.5W

8237A PROGRAMMABLE DMA CONTROLLER

- 4 independent channels
- Designed for use with an external 8-bit address register
- 64K address and word capacity on each channel
- Input voltage — .8V low; 2.4V high
- Duration of clock cycle — 210 ns
- Duration of DMA transfer — five 210 ns clock cycles

2764 ERASABLE/PROGRAMMABLE READ-ONLY MEMORY (EPROM) — 16K BYTE CAPACITY BIOS

- Access time — 350 ns maximum
- Power consumption — 525mW maximum
- Total programming time for all 64K bits

- Input voltage — .8V low; 2.4V high

2164 DYNAMIC RANDOM ACCESS MEMORY (DRAM) ON-BOARD MEMORY

- N-channel, HMOS construction
- 64K x 1 bit format
- Input voltage — .8V low; 2.4V high
- Access time — 150 ns maximum
- Duration of read, write cycle — 260 ns
- Duration of read, modify, write cycle — 280 ns
- Power consumption — 1W

EXPANSION SLOTS (8 AVAILABLE)

- 62-pin design
- Lines for:
  - Power
  - Address
  - Data
  - Control
- Compatible with:
  - NCR expansion boards
  - Other industry manufacturers' expansion boards

PARALLEL COMMUNICATIONS (CENTRONICS) CONNECTOR

- DB-25 female connector
- Operates on industry standard signals
- Compatible with IBM peripherals

SERIAL COMMUNICATIONS (RS 232C) CONNECTOR

- DB-25 female connector

- Baud range
  - 50 baud minimum
  - 19.2K baud maximum

MONOCHROME DISPLAY SPECIFICATIONS

The following specifications pertain to NCR kit K150.

MONOCHROME DISPLAY SPECIFICATIONS

Monochrome Functional Area	Measurement	Value	Remarks
Video Input	Amplitude	4.0 ± 1.5 V	Into internal 500 ohms or less contrast control: TTL
	Rise Time	10ns	Maximum leading edge (10-90%)
	Fall Time	10ns	Maximum trailing edge (90-10%)
	Frequency	Up to 20MHz Data Rate	Standard Unit
	Maximum Bandwidth	16.257MHz	
Horizontal Drive Input	Amplitude	4.0 ± 1.5V	Sync Positive
	Rise/Fall Time	40ns Maximum	
	Resolution	18.432KHz/640 PIXEL Resolution	
	Pulse Width		
	Blanking Time	10ns Minimum	
Vertical Drive Input	Amplitude	4.0 ± 1.5V	Sync positive or negative
	Rise/Fall Times	40ns Maximum	
	Resolution	50Hz/200 PIXEL Resolution	
	Refresh Rate	200 lines 50 times per second	
	Pulse Width	.162 ms	
	Blanking Time	1.03 ms	
Input Power	Voltage/ Amperage Requirements	+ 12 Volts @ 1.25 amps nom/ 1.50 amps max.	
	Maximum Ripple	100mv p-p	Refresh Synchronous with power supply
		10mv p-p	Refresh non-synchronous with power supply
		50mv p-p	High Frequency power
Video Input Impedance	Shunt Resistance	4K ohms minimum	Excluding internal contract control
	Shunt Capacitance	30pf maximum	---
Horizontal Drive Input Impedance	Capacitive Coupled Input Impedance	470 ohms minimum	---
Vertical Drive Input Impedance	---	3.3K ohms minimum	
Video Amplifier Response	Small Signal Bandwidth (-3db)	DC — 22MHz DC — 20MHz	Typical Minimum
	Leading Edge (90-10% @ CRT cathode)	20ns	Maximum

Monochrome Functional Area	Measurement	Value	Remarks
Controls	Internal (Factory Preset)		PC Label below:
		Horizontal Hold	"HORIZ HOLD"
		Video Centering	"HORIZ CENT"
		Linearity	"LINEARITY"
		Width	"WIDTH"
		focus	"FOCUS"
		Brightness (Limiting)	RRT
		Contrast	TRS
	External	Brightness	100K ohm potentiometer
CRT Display Characteristics	Diagonal Measurement	12 inches	----
	Deflection Angle	90°	
	CRT Type	20 inch	Spherical Radius
	High Voltage	13.0KV	Nominal
	Usable Screen Area	6.7 x 9.0 inches	
	Horizontal	800 @ 70 cd/m²	Center
	Resolution	650 @ 70 cd/m²	Corners
	Linearity	10% Maximum Height/Width Variance	Adjacent Characters
		20% Maximum Height/Width Variance	All Screen Characters
	Screen Surface	P39 Green Phosphor	
	Characters Per Line:	80	
	Number of Lines:	25	
	Character Boxes:	9 dots x 14 dots	
Mechanical Specification	Weight	10.0 lbs. (4.54 kg)	
	Height	7.49 in.	
	Width	11.1 in.	
	Depth	11.4 in.	
Environment	Ambient Temperature	Operating	
	5° to 50°C (41° to 131°F)	Non-operating	
	-40° to 65°C (-40° to 150°F)		
	Humidity (No-condensing)	5% to 90%	Operating/Non-operating
	Altitude (Maximum)	10,000 ft. (3.048 km)	Operating
		30,000 ft. (9.144 km)	Non-operating

MONOCHROME DISPLAY ADAPTER BOARD SPECIFICATIONS

- Nominal dimensions = 13.00 inches long, 4.2 inches wide
- Cathode ray tube controller IC = Motorola MC6845
- 4K ROM character generator providing 256 resident character patterns
- 62 contact, Main Processor Board Bus expansion connector
- 9-pin 'D-type' video cable connector
- Power Requirements = +5VDC @ 1.0A (maximum)

Video Input:

- Level low = 0 to 0.4V
- Level high = 3V (typical)

Horizontal drive:

- Level low = 0 to 0.4V
- Level high = 3V (typical)

Vertical drive:

- Level low = 0 to 0.4V
- Level high = 3V (typical)

Display Buffer Memory: 4K bytes
Dot Clock Frequency: 16.257MHz
Sweep Rates: 18.432KHz (horizontal); 50Hz (Vertical), while providing a screen-repaint rate of 50Hz Logic Levels are TTL-compatible
Power Requirement: +5VDC +/0.5V at 1.0A (max.)

POWER SUPPLY SPECIFICATIONS

Output	Supplies Power To:
+5.2V at 10A within 4%	Main Processor Board, Flexible Disk Drives, Keyboard, plus all Expansion Adapters

+12.2V at 4.1A within 5%	System dynamic memory, disk drive motors (one at a time) for both flexible and fixed disks
-5.0V at 300MA within 3%	RS 232C port (with -12V) dynamic memory bias
-12.2V at 500MA within 5%	RS 232C port (with +12V)

FIXED DISK DRIVE SPECIFICATIONS

DC Power Requirements:

+12V within 5%, 0.75 amp typical, 2.5 amps (at power on)
*5V within 5%, 0.9 amp typical, 1.2 amps (maximum)

Maximum Ripple: 100MV peak to peak (12V, 5V)

Power Dissipation: 14W, typical
16W, maximum

Performance Specifications Capacity

	Formatted	Unformatted
Per Drive ---	20.0 MB	25.52 MB
Per Surface —	5.0 MB	6.38 MB
Per Track ----	8,192 bytes	10,416 Bytes

Performance Specifications Capacity

Rotational Speed	3600 RPM + 1%
Recording Density	9,784 BPI
Flux Density	9,784 FCI
Track Density	568 TPI
Cylinders	612
Tracks	2,448
R/W Heads	4
Discs	2
Access Time:	
Track to Track	20 ms
Average	85 ms
Maximum	205 ms

Transfer Rate	5.0 Mbits/sec
Average Latency	8.33 ms

FLEXIBLE DISK DRIVE SPECIFICATIONS

- Dimensions: Half-height; approximately 8" by 5-3/4" by 1-3/4"
- 5-1/4" (133 mm) diameter diskette
- 2 read/write heads
- 300 rpm
- Double-sided, double-density*
- 40 Tracks per side*
- 48 Tracks per inch*
- 6 ms track-to-track access time*
- 250K bytes-per-second transfer rate
- Drive timeout in 15 seconds of no use*
- 15 ms head setting time (last track addressed)*
- Error Rate:
  1 per 10A9 (recoverable)
  1 per 10A1A2 (non-recoverable)
  1 per 10A6 (seeks)
- Power: +12VDC 02 0.6V, 900 mA average
  +5.2VDC 02 0.25V, 900 mA average
- Software-controlled by flexible disk drive controller on MPB.

5-1/4" FLEXIBLE MAGNETIC DISK SPECIFICATIONS

- Size 5.25 inches (133.4 mm) square. Distance from edge of disk to edge of jacket: 0.140 inch (3.56 mm)
- Double-sided, double-density, soft-sectored
- Oxide-coated mylar disk
- Spindle access hole
- Read/write access hole
- Index hole
- Write/protect cutout

- 48 tracks per inch (TPI)
- 40 tracks/surface
- 9 sectors to a track
- 512 Bytes per sector
- Disk layout
  Tracks 0-2 operating system
  Track 3 directory
  Tracks 4 — 79 user files

FIXED DRIVE INTERFACES SPECIFICATIONS

- Encoding method MFM
- Tracks per head 306
- Bytes per sector: 512
- Sectors per track: 17
- Total tracks: 1224
- Head selects: 4
- Drive selects: 2
- Data transfer rate: 5 Mbits/sec
- Write precomp time: 12 ns

MAIN PROCESSOR BOARD INTERFACE SPECIFICATIONS

- Type: 62-pin standard I/O channel card edge
- Power: Supplied via 62-pin connector
  +5VDC @ 1.5 amps
  +12VDC @ 100ma

Glossary

A

ABORTED
Ended abnormally before completion, such as a function that is interrupted before completion.

ACOUSTIC COUPLER
A modem that converts the data to be transmitted into a sequence of different tones; sent via a conventional telephone handset to a receiving modem; converts them back to a stream of binary digits.

ACRONYM
A word formed from the first letter or letters of the words in a name, term, or phrase.

ADAPTER
A connector that has a plug for one type of cable or device and a socket for another type. An adapter allows parts of a computer which ordinarily don't fit together to be connected.

ADDRESS
Data is contained in the devices which make up your computer's internal and external memory and the registers in its CPU. Each accessible location within a device is assigned a number, which is known as an "address". In internal memory, the address is a specific byte number. In external memory, the address is a unit number (for example, drive A) and, for disk or diskette drives, the address may include a track number and a sector number. Your computer is able to locate data using these addresses.

APPLICATION PROGRAM
A program that you use on your computer to perform a specific job, such as budgeting or word processing.

ASCII
American National Standard Code for Information Interchange. The standard code, using a coded character set consisting of 7-bit coded characters (8 bits including parity check), used for information interchange among data processing systems, data communication systems, and associated equipment. The ASCII set consists of control characters and graphic characters.

ASSEMBLE
To prepare an object language program from a symbolic language program by substituting machine operation codes for symbolic operation codes and absolute addresses for symbolic addresses.

ASSEMBLER
A computer program that operates on symbolic input data to produce machine instructions. An assembler generally translates input symbolic codes into machine instructions, item for item, and produces, as an output, the same number of instructions or constants that were defined in the input symbolic codes.

ASYNCHRONOUS
Characterizing different time intervals between events or occurrences.

ASYNCHRONOUS DATA TRANSMISSION
A format for data transmitted across telephone lines in which each character is "framed" by a start bit and a stop bit. Thus, when transmitted asynchronously, each character is 10 bits in length: seven information bits, one parity bit, one start bit, and one stop bit.

B

BACK UP, verb
The process of duplicating data from one location to another (i.e., diskette to diskette, or fixed disk to diskette) to prevent total information loss should the original record be lost or damaged.

BACKUP, noun
A copy of a file or disk/diskette.

BACK-UP, adjective
A system that performs the process of backing up data or files.

BASIC

1. Acronym for the programming language Beginner's All-purpose Symbolic Instruction Code. BASIC uses common English words and is relatively easy to use.
2. The computer program which translates statements made in BASIC programming language into instructions to the computer.

BINARY CODE

A system of numbering which uses only two values, zero and one. For example, the ASCII letter D is represented as 01000100.

BINARY DIGIT (bit)

Either of the characters 0 or 1, abbreviated as bit.

BLOCK

A physical unit of data that can be conveniently stored by a computer on an input or output device. The term is synonymous with physical record. The block is normally composed of one or more logical records or a portion of a logical record.

BPI

Abbreviation for bits per inch. The standard measure for the density of data recording on disks/diskettes/tapes.

BPS

An abbreviation for bits per second. In serial transmission, the instantaneous bit speed with which a device or channel transmits a character.

BYTE

A sequence of adjacent bits operated upon as a unit. The smallest addressable memory element; usually represents one character. In your computer, each byte consists of eight bits plus one parity bit.

C

CARTRIDGE

A container with a reel of magnetic tape for the storage of data and a takeup reel for transfer of the tape within the cartridge by means of a capstan drive system.

CATHODE RAY TUBE (CRT)
An electronic vacuum tube with a screen, such as a television picture tube, upon which information may be displayed.

CENTRAL PROCESSING UNIT (CPU)
The central processor or the computer system contains the internal memory unit (memory), the arithmetic logic unit (ALU), and the input/output control unit (I/O Control).

COBOL
An acronym for Common Business Oriented Language — a higher level language developed for business data-processing applications.

CODING
(1) The writing of a list of instructions which will cause a computer to perform specified operations. (2) An ordered list or lists of the successive instructions which will cause a computer to perform a particular process.

COMMAND
An instruction which tells the operating system what you want to do.

COMMUNICATION ADAPTER
A hardware component that is hardwired into the telephone line which prepares data for transmission through a telephone line.

COMPILER
A computer program that operates on symbolic input data to produce machine instructions. A compiler is more powerful than an assembler. It is able to replace certain input items with a series of instructions. The program which results from compiling is a translated and expanded version of the original program.

COMPONENT
A functional part of an operating system, i.e., your keyboard.

COMPRESSION
The elimination of blank spaces on the magnetic tape or disk by placing data files immediately adjacent to each other.

COMPUTER
A device capable of accepting data in the form of facts and figures, applying prescribed processes to the data and supplying the results of these processes as meaningful information. This device usually consists of input and output devices, storage, arithmetic and logic units, and a control unit. Usually, an automatic, stored-program machine is implied.

COMPUTER-ASSISTED INSTRUCTION (CAI)
A data processing application in which a computing system assists in the instruction of students. The application usually involves a dialog between the student and a computer program which informs the student of mistakes as they are made.

COMPUTER SYSTEM
The physical equipment and instructions; i.e., hardware and software, used as a unit to process data. It includes the central processing unit (CPU), its operating system, and peripheral equipment and programs under its control.

CONVERSATIONAL MODE
A mode of operation of a data processing system in which a sequence of alternating entries and responses between a user and the system takes place in a manner similar to a dialog between two persons.

CPS
Abbreviation for characters per second. It is a standard way of measuring the printing speed of a printer.

CPU
See central processing unit.

CRT
See cathode ray tube.

CURSOR
A moving, sliding, or blinking symbol on a CRT which indicates where the next character will appear.

CYLINDER
The tracks of a disk storage device that can be accessed without repositioning the access mechanism.

D

DATA
Any information — letters, numbers, symbols — which is input to, or output from, the computer for storage or manipulation.

DATA BASE
A collection of data fundamental to an enterprise.

DEBUG
To detect, to trace, and to eliminate mistakes in computer programs or in other software.

DEFAULT
An alternative value, attribute, or option that is automatically selected by the computer program when none has been specified.

DESTINATION FILE
A file designated to receive the information which is output from a computer run.

DIAGNOSTICS
Procedures used to identify and isolate problems within the computer or its peripherals.

DIRECTORY
A list of file names kept on each disk or diskette.

DISKETTE
A thin, flat piece of flexible plastic which looks like a phonograph record. It is coated with magnetic material and is encased in a protective paper jacket. Data is recorded and stored on a diskette. Flexible Disk, Floppy Disk, Disk, Flexible Diskette, Floppy Diskette, Floppy, Mini Disk are all common names used to refer to a removable diskette.

DISKETTE ENVELOPE
A heavy paper envelope in which diskettes are stored except when in use.

E

EBCDIC
An acronym for Extended Binary Coded Decimal Interchange Code. A coded character set consisting of 8-bit coded characters.

EDIT

To prepare data for a later operation. Editing may include the rearrangement or the addition of data, the deletion of unwanted data, format control, code conversion, and the application of standard processes such as zero suppression.

ELECTRONICS

Pertaining to the application of that branch of science which deals with the motion, emission and behavior of currents of free electrons, especially in vacuum, gas or phototubes and special conductors or semiconductors. Contrasted with "electric" which pertains to the flow of large currents in wires only.

EPROM

An acronym for Erasable PROM. One of the latest types of monolithic memory. It can be programmed in the field by the user, and it can also be erased and reprogrammed with different information. Once it has been programmed the EPROM memory acts just the same as ROM.

ERASE

To remove data from a data medium, leaving the medium available for recording new data.

EXTENSION

A one-, two-, or three-letter addition to a filename generally used to identify what type of data file it is.

F

FIELD

A unit of data within a record or area. A logical grouping of contiguous characters.

FILE

A set of related records grouped and identified together; the records in a file may be sequenced according to a key contained in each record.

FILENAME

The name applied to a data file to identify it so that the computer can locate it and recall it from a storage device.

FILE-SELECTABLE
The ability of a computer to select data from a storage device by the filename or to transfer data to storage by single filename.

FIXED DISK
A thin, flat, circular piece of rigid plastic or aluminum on which data and information is stored. Hard disks are able to store much more data than flexible diskettes.

FORMATTED DISKETTE
A diskette on which track and sector control information has been written by a particular computer system, i.e., NCR-DOS, but which contains no data.

FORTRAN
An acronym for FORmula TRANslator. A high level programming language used to perform mathematical, scientific, and engineering computations.

FUNCTION
Any activity of the computer directed by the software, such as loading a file into memory, saving a file onto a disk, or performing a series of calculations.

G

GLITCH
A sudden, often unexplained, electronic occurrence which causes problems in an electronic device.

GRAPHICS
Facilities to provide computer output in the form of displays, drawings, and pictures.

H

HARD COPY
A printed copy of machine output in readable form, i.e., reports, listings, documents, summaries.

HARD DISK
See fixed disk.

HARDWARE
Physical equipment used in data processing. Contrast with software.

HEAD
A device that reads, records, or erases data on a storage medium, e.g., a small electromagnet used to read, write, or erase data on a magnetic disk.

HEXADECIMAL DIGIT
A whole number in the hexadecimal numeral system (based on a radix of 16). A hexadecimal digit can be expressed in any one of sixteen different characters: 0,1,2,3,4,5,6,7,8,9,a,b,c,d,e,f.

HOUSEKEEPING
Computer operations that do not directly contribute toward the desired results; in general, initialization, set-up, diagnostics.

I

ILLEGAL CHARACTER
A character or combination of bits which is not accepted as a valid or known representation by the computer.

INDICATOR
A device which registers a condition in the computer.

INITIALIZE
To set counters, switches, and addresses to zero or other starting values at the beginning of, or at prescribed points in, a computer routine.

I/O
Abbreviation for "input and output". Input is the data received by the CPU from devices connected to it. Output is that which is sent from the CPU to those devices.

INPUT
The introduction of data from an external storage medium into a computer's internal storage unit.

INSTRUCTION
A group of characters, bytes, or bits that defines an operation to be performed by the computer.

INTERFACE
A common boundary between two or more electronic devices or software programs which enables them to transfer information.

INTERRUPT
A suspension of a process, such as the execution of a computer program, caused by an event external to that process, and performed in such a way that the process can be resumed.

K

KEY
(1) The field or fields which identify a record. (2) The field which determines the position of a record in a sorted sequence. (3) A lever on a manually operated machine, such as a typewriter.

KILOBYTE
A kilobyte is 1024 bytes. It is commonly abbreviated as K, and used as a suffix when describing memory size in computers. Thus, 24K really means a 24 x 1024 = 24,576 byte memory system.

L

LANGUAGE
A set of characters, conventions, and rules, that is used for conveying information. The three aspects of language are pragmatics, semantics, and syntax.

LED
An acronym for Light Emitting Diode, a commonly used alphanumeric display unit which glows when supplied with a specified voltage.

LOAD
To enter data into storage or working registers of the computer.

LOG
A record of the operations of data processing equipment, listing each job or run, the time it required, operator actions, and other pertinent data.

LOGGING-ON
Giving the computer (particularly if it is a part of a larger system) information such as your name and a password in order to be able to use the system.

LOOP
A sequence of instructions in a program that can be executed repetitively until certain specified conditions are satisfied.

M

MACHINE INSTRUCTION
An instruction that a computer can directly recognize and execute.

MACHINE LANGUAGE
The basic language of a computer.

MACRO INSTRUCTION
(1) A source language instruction that is equivalent to a specified number of machine language instructions. (2) A machine language instruction that is composed of several micro instructions.

MEMORY
The storage facilities of the computer, capable of storing vast amounts of data.

MENU
Options listed in a display image that can be selected by the user of the display device.

MICRO INSTRUCTION
A low level instruction used to obtain a macro, or machine language instruction.

MIRROR-IMAGE
Exact copy of a data storage system such as a hard disk with files arranged in exactly the same sequence, including any blank spaces.

MODEM
Modulator-Demodulator. A device which converts (modulates) serialized digital signals (usually output from a communications

adapter) to acoustic signals for transmission over a telephone line and converts (demodulates) incoming acoustic signals to serialized digital signals.

O

OPERATING SYSTEM
An organized collection of software that controls the overall operations of a computer. The operating system does many basic operations which were performed by hardware in older machines, or which are common to many programs. It is available to the computer at all times either being held in internal storage or on an auxiliary storage device.

OPERATION
A defined action. The action specified by a single computer instruction or high level language statement.

OPERATION CODE
The instruction code used to specify the operations a computer is to perform.

OUTPUT
(1) Data transferred from a computer's internal storage unit to some storage or output device. (2) The final result of data processing; data that has been processed by the computer.

P

PARALLEL TRANSMISSION
In data communications, a method of data transfer in which all bits of a character are sent simultaneously.

PARAMETER
An arbitrary constant. A variable in an algebraic expression that temporarily assumes the properties of a constant.

PARITY
A method used by most of the computer industry to determine if hardware has correctly sent and received data characters. If hardware checks for even parity, it considers valid all characters moved between units, memory registers, or memories whose total number of ON bits is even. If hardware checks for odd parity, it

considers valid all characters moved between units, memory registers, or memories whose total number of ON bits is odd.

PARITY BIT
The extra bit that computer hardware adds to a character or group of characters prior to moving the character between units, memory registers, or memories. Hardware sets the bit either OFF or ON to develop either an odd or even number of ON bits in the character. When this character is received, hardware checks the parity to determine if the data was correctly received or if a parity error exists.

PARITY CHECKING
Automatic error detection by using checking bits along with the numerical bits.

PASCAL, BLAISE
(1623-1662) A French mathematician who built the first desk-calculator type of adding machine in 1642. This device represented the numbers from 0 to 9 with teeth on gears. The machine could perform addition and subtraction.

PASCAL
A high-level, procedure-oriented programming language named for Blaise Pascal.

PASSWORD
A unique string of characters that a program, computer operator, or user must supply to meet security requirements before gaining access to data.

PERIPHERAL
A device which is separate from the computer but which works in conjunction with it, such as a printer, a keyboard, a disk drive, etc.

PHYSICAL RECORD
The unit of data for input or output; e.g., a punched card, a tape block, a record on a disk.

PIXEL
A picture element.

PL/1

A high level programming language designed to process both scientific and business applications. The PL/1 language contains many of the best features of FORTRAN, COBOL, ALGOL and other languages as well as a number of facilities not available in previous languages.

PROCESSOR

A device or system capable of performing operations upon data; e.g., CPU (hardware) or compiler (software). A compiler is sometimes referred to as a language processor.

PROGRAM

(1) A set of sequenced instructions to cause a computer to perform particular operations. (2) A plan to achieve a problem solution. (3) To design, write, and test one or more routines. (4) Loosely, a routine.

PROGRAMMING

The process of translating a problem from its physical environment to a language that a computer can understand and obey. The process of planning the procedure for solving a problem. This may involve among other things the analysis of the problem, preparation of a flowchart, coding of the problem, establishing input/output formats, establishing testing and checkout procedures, allocation of storage, preparation of documentation, and supervision of the running of the program on a computer.

PROM

An acronym for Programmable Read Only Memory. A memory that can be programmed by electrical pulses. Once programmed, it is read only. The PROM chips can be purchased blank and then be programmed by using a special machine. Once programmed, this memory behaves the same as the ROM. That is, it can be read as many times as desired but cannot be written.

R

RAM

Random Access Memory. The type of internal memory of a computer in which data can be written to, read from, erased, or stored in any order. RAM is maintained by electrical current and makes up much of the internal memory.

RESET
(1) To return computer components to a specified static state. (2) To place a binary cell into the zero state.

RESPONSE TIME
The time it takes the computer system to react to a given input. It is the interval between an event and the system's response to the event.

RESTART
To reestablish the execution of a routine.

RESTORE
To recover data from a storage device such as a tape cartridge and transfer it back to the disk from where it was originally copied.

RETENSION
To adjust the tension again on the tape in a cartridge so that it is uniform in tension throughout the reel.

ROM
An acronym for Read Only Memory. Nonerasable, permanently programmed memory usually used to store monitors, I/O drivers, interpreters, or special application functions. It is not possible to write into ROM memory.

ROUTINE
A set of machine instructions for carrying out a specific processing operation. Sometimes used as a synonym for program.

RUN TIME
The time during which the data are fetched by the control unit and the actual processing is performed in the arithmetic unit.

S

SAVE TO TAPE
Transfer data from disk or other memory device to tape.

SCREEN
The display surface of a CRT device.

SCROLL
To roll lines up or down a CRT screen to review text or information. Most screens display only 25 lines at a time, so scrolling is useful in viewing large files of information.

SECTOR
One of the peripheral elements into which each track of a disk surface is divided. Disks are usually formatted into 8 or 9 sectors.

SOFTWARE
The non-physical portion of your system. Any kind of program within the electrical circuits of a computer is software.

SOURCE DOCUMENT
An original document from which basic data are extracted; e.g., invoice, sales slip, inventory tag.

SPECIAL CHARACTER
A graphic character that is not a letter, a digit, nor a blank; e.g., plus sign, equal sign, asterisk, dollar sign, comma, and period.

START/STOP
A mode of operation of a tape drive in which the data are transferred in blocks during which the tape runs and then stops while the computer reads more data for transfer.

STATEMENT
In programming, an expression or generalized instruction in a source language.

STORAGE
Descriptive of a device or medium that can accept data, hold them, and deliver them on demand at a later time. The term is preferred to memory.

STORAGE CAPACITY
The number of items of data which a storage device is capable of containing. Frequently defined in terms of computer words, bytes, or characters.

SYNCHRONOUS DATA TRANSMISSION
A transmission mode in which regularly timed clock pulses are used to provide synchronization between the transmitting and

receiving devices on a communication line. Synchronous transmission reduces overhead, compared with asynchronous transmission, by eliminating the need to send individual start and stop bits for each character transmitted.

SYSTEMS PROGRAMS
Computer programs that provide a particular service to the user; for example, compilers, assemblers, operating systems, soft-merge programs, linkage editor programs, graphic support programs, etc.

T

TERMINAL
(1) An I/O peripheral device which is on-line to the computer, but which is in a remote location: another room, another city, or another country. (2) A point at which information can enter or leave a communication network.

TRACKS
A series of concentric rings on a disk or diskette. Data can be written to or read from the tracks by the read-write head.

U

UPDATE
To incorporate into a master file the changes required to reflect transactions or other events.

USER GROUP
A group of computer users that share knowledge they have gained and programs they have developed on a computer or class of computers of a specific manufacturer.

UTILITY ROUTINES
Software used to perform some frequently required process in the operation of a computer system.

V

VALIDATION
The examination of data for correctness against certain criteria, such as format, ranges, check digits, equivalent entries on a master file.

VARIABLE
A quantity that can assume any of a given set of values.

VERIFY
(1) To determine whether a data processing operation has been accomplished accurately; e.g., to check the results of keypunching. (2) To check data validity.

W

WORD
A group of bits, or bytes considered as an entity and capable of being stored in one storage location.

WORD LENGTH
The number of bits, or bytes in a word.

WRITE
(1) The process of transferring information from the computer to an output medium. (2) To copy data, usually from internal storage to auxiliary storage devices.

WRITE-INHIBIT TAB
Opaque tape used to cover the write-enable notch on diskettes to prevent writing on the disks.

WRITE ENABLE NOTCH
A small notch located on an edge of most diskettes. It permits data to be recorded on that diskette.

Index

SEE REVERSE SIDE OF THIS FORM FOR INSTRUCTIONS

DOCUMENTATION ORDER FORM

NCR Customer No.	Purchase Order No.	Purchase Order Date

SHIP TO:	Ship To No.:
Company Name	
Address	
City/State/Zip	
Attention	
In case we have questions regarding your order Area Code ( ) Number — Ext.	
☐ Change of Address	

BILL TO:	Bill To No.:
Company Name	
Address	
City/State/Zip	
Attention	
In case we have questions regarding your order Area Code ( ) Number — Ext.	
☐ Change of Address	

Ship VIA

International Only — Customs Declaration

Comments:

DOCUMENT NUMBER	QUANTITY	DESCRIPTION	UNIT PRICE	AMOUNT
1			$	$
2			$	$
3			$	$
4			$	$
5			$	$
6			$	$
7			$	$
8			$	$
9			$	$
10			$	$
			Subtotal	$
			State/Local Taxes	$
			Total	$

Tax Exempt? ☐ No ☐ Yes	Tax Exempt No.

For your convenience you can:

1. Mail this order to:
   NCR Corporation
   Order Processing
   Publication Services
   Dayton, Ohio 45479
2. Submit this order to your local NCR office
3. Call our toll-free number:
   1-800-543-2010
   In Ohio:
   1-800-543-6691
   8:00 A.M.-4:30 P.M.
   EST - Weekdays

NCR

Signature _____ Date _____

ORDERING INFORMATION

HOW TO ORDER

For a fast, easy way to order and receive the documents you need, complete this Documentation Order Form as follows.

1. NCR CUSTOMER NO. .

Enter your 8-digit NCR customer number.

> ***CUSTOMER NUMBERS ARE REQUIRED ON ALL ORDERS.***
>
> *If you are unsure of your customer number, please contact your local NCR office.*

2. PURCHASE ORDER NO.

Enter your purchase order number.

3. PURCHASE ORDER DATE

Enter the purchase order date.

4. SHIP TO

a. If you wish to have documents shipped to a location different than the location associated with your NCR customer number, enter the appropriate information in the space provided.

b. If the order is to be shipped to your NCR customer number location, no entry is required in this space.

5. BILL TO

No entry is required unless the BILL TO location is different from the SHIP TO location.

6. SHIP VIA

Enter your preferred method of delivery. All orders for items in stock will be processed and shipped within one week of receipt of order via UPS or mail for domestic shipment and air shipment for international orders. Rush orders will be processed and delivered within 48 hours.

7. CUSTOMS DECLARATION (For International Orders)

If a customs declaration is required, enter the full text of the declaration in the space provided.

8. COMMENTS

Use this space for special comments about your order.

9. DOCUMENT NUMBER

Enter the number of the document you wish to order. NCR document numbers have a 2-character prefix, followed by 4 to 7 characters. (D1-0000-00).

10. QUANTITY

Enter the quantity desired. The following discounts apply when any document is purchased in quantities of 10 or more on one order.

- 10-49 10% discount
- 50-99 15% discount
- 100 or more 20% discount

11. DESCRIPTION

Enter the title of the document.

12. UNIT PRICE

Enter the unit price of the document. (Prices listed are those in effect at the time of printing and are subject to change without notice.) All prices are quoted in U.S. dollars.

13. AMOUNT

To calculate the line item amount, multiply the quantity by the unit price.

14. SUBTOTAL

Add all entries in the amount column and enter the sum in the SUBTOTAL space.

15. STATE/LOCAL TAXES

Calculate applicable state and local taxes by multiplying the SUBTOTAL amount by the percentage of tax. Enter that number in the STATE/LOCAL TAXES space. If tax exempt, your tax exempt number must be entered in the space provided to the left.

16. TOTAL

Enter the total amount of the order.

THREE CONVENIENT WAYS TO ORDER

Enter your order using one of the following convenient methods:

U.S. Customers

- Mail the Documentation Order Form to NCR Corporation, Order Processing—Publication Services, Dayton, Ohio 45479.
- Submit the order to your local NCR office.
- Call our toll-free number: 1-800-543-2010; in Ohio, 1-800-543-6691. Phone orders are taken from 8:00 am to 4:30 pm EST—weekdays.

International Customers

- Customers located outside of the United States should contact their local NCR office for ordering and pricing information.

PAYMENT METHODS

Payments are accepted by check, money order, or purchase order. Please do not send cash.

RETURNS

If you wish to return documents for credit, please contact our Order Processing department (1-800-543-2010; in Ohio, 1-800-543-6691) within 30 days of the shipment date. Full credit will be given if documents are returned because of an NCR error. A credit of up to 75% of the net amount may be issued for the return of unused, shrink-wrapped documents. Returns will NOT be accepted without prior approval from Publication Services.

OUT OF STOCK ITEMS

Every attempt will be made to ensure that your order is filled completely and accurately. If a document is temporarily out of stock, it will be placed on back order. When a partial shipment is made, your packing list will include a notification of this condition. Back orders will be automatically filled when the document is returned to our inventory.

Retain a copy of this order for your records. Thank you.

NCR

READER'S COMMENTS FORM

BOOK TITLE	BOOK NO.	PRINT DATE

To help us plan future editions of this document, please take a few minutes to answer the following questions. Explain in detail using the space provided. Include page numbers where applicable.

Are there any technical errors or misrepresentations in the document?

Is the material presented in a logical and consistent order?

Is it easy to locate specific information in the document?

Is there any information you would like to have added to the document?

Are the examples relevant to the task being described?

Could parts of the document be deleted without affecting the document's usefulness?

Did the document help you to perform your job?

Any general comments?

NAME _____

TITLE _____

COMPANY _____

ADDRESS _____

_____

TELEPHONE NO. ( ) _____

Thank you for your evaluation of this document.
Fold the form as indicated and mail to NCR. No postage is necessary in the U.S.A.

fold

NO POSTAGE
NECESSARY
IF MAILED
IN THE
UNITED STATES

BUSINESS REPLY MAIL

FIRST CLASS PERMIT NO. 3 DAYTON, OHIO

POSTAGE WILL BE PAID BY ADDRESSEE

NCR Corporation

ATTENTION: Publication Services
WHQ-4

Dayton, Ohio 45409

TAPE

NCR

NCR Corporation
Dayton, Ohio 45479

D1-0315-A
150-0002000