SERVICE PC / DOCUMENTATION

Documentation Update

MANUAL : P2000C System Reference and Service Manual

12 NC : 5103 993 30423

AMENDMENT : 3

DATE : 19th April 1985

NOTE : 12 NC becomes 5103 993 30424 after incorporating this amendment.

INSTRUCTIONS

Remove and replace (R&R) or remove and destroy (R&D) or insert (INS) the pages indicated in the 'List of Affected Pages'.

Update the 12 NC number on the Front Page and the Spine Label to reflect the change of 12 NC number.

Significant changes to the text (or illustrations) are marked with a line in the outer margin.

The deletion of text is marked with the symbol '*'.

Note: If your P2000C System Reference and Service Manual does not incorporate Amendments 1 and/or 2 (see Manual Status Form) please order copies from your dealer.

Please file this sheet behind the Front Page to indicate that the amendment has been incorporated.

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Documentation Update

This amendment introduces chapter 3.9, covering all aspects of the 8088 CoPower Board option. At the same time, the Spare Part Catalogue has been revised and some pages amended to reflect the addition of the 16-Bit CoPower Board.

List of Affected Pages

Pages					Reason for Change
	xiii & xiv		(R&R)		:Change of contents
2.1	3-11 &	2.1	3-12	(R&R)	:Correction to information & reflects Term. S/W Rel. 1.3
2.1	4-1 to	2.1	4-4	(R&R)	:Reflects Term. S/W Rel.1.3 only
2.1	4-7 to	2.1	4-12	(R&R)	:Expansion of description & reflects Term. S/W Rel.1.3
2.1	4-15 &	2.1	4-16	(R&R)	:Expansion of description
2.1	4-19 to	2.1	4-22	(R&R)	:Expansion of description & reflects Term. S/W Rel.1.3
3.4	1-1 &	3.4	1-2	(R&R)	:Correction to information
3.9	1-1 to	3.9	3-30	(INS)	:Addition of 8088 CoPower Board
8088 Circuit & Layout Drawings				(INS)	:Addition of 8088 CoPower Board
4.2	1-1 &	4.2	1-2	(R&R)	:Inclusion of Routing Indicator
4.2	2-1 to	4.2	8-4	(R&R)	:Revision of Catalogue
(complete catalogue)					
Manual Status Form				(R&R)	:Standard procedure
Comment Form				(R&R)	:Standard procedure

CHAPTER 6 - DISK DRIVES

CHAPTER 7 - MEMORY EXTENSION P2092

CHAPTER 8 - IEEE EXTENSION P2091

CHAPTER 9 - 8088 COPOWER BOARD - P 2093

Note: Full contents are given on page 3.9 1-1.

PART 4
SERVICING AND SPARE PARTS

CHAPTER 1 - REMOVAL AND REPLACEMENT OF ASSEMBLIES AND UNITS

CHAPTER 2 - SPARE PART CATALOGUE

APPENDIX

3.2.5 BOOT THE SYSTEM TRACK(S) FROM THE SELECTED DRIVE

Bytes 11 - 12H: DEFW BOOTER

On entry: DRIVE contains the selected drive
Action: the track-0 of the selected drive is read to D600H. In case of error the "SYSTEM DISK?" message is displayed and the operator must press any key except ESC to repeat.

If D603 = 80 a return is made
81 track-1 is read from the same side to E600H
82 track-0 is read from the other side to E600H.

On exit: RWBUFF, RWLGT and all simple registers are destroyed.

3.2.6 GET LISTING DEVICE STATUS

Bytes 13 - 14H: DEFW LISTAT

Action: The USART control byte is read. DSR, TxRDY and TXEMPTY must be set for ready. (The printer READY BIT is connected to the USART DSR pin because it can be read directly from control byte.)
On exit: if device ready, A = FFH and zero flag is reset.
If device busy, A = 0 and zero flag is set.
All other registers are unchanged.

3.2.7 PRINT SCREEN

Bytes 21 - 22H: DEFW PRSCR

PRSCR is an auxiliary subroutine to print one or more lines from the screen.

On entry: BC = the screen address (top-left position is 0)
A = the number of lines to print (1 to 24)

On exit: A = FFH and the zero flag is reset if printing successful
A = 0 and the zero flag is set if either,
- the range specified is out of the screen range
- a printer error has occured

WARNING No key may be depressed during the procedure.

Note: Print screen is not possible in 25 line mode.

3.3 System Timer

The system supports a 4 Bytes long 60 Hz system timer. It's value can be accessed in DPB Bytes 29 to 2CH (29H is the lowest Byte). This CLOCK field is cleared on reset unless the user depresses the SPACE bar.

The user can also define a subroutine that will be called-in every 16.7 ms. Its address is stored at DPB Bytes 25 - 26H. The user must save all registers and as no CP/M stack may be used a user defined stack must be set up.

3.4 Summary of the Driver Parameter Block

The pointer to this block is stored at FFD0H.

00 DRIVE	ACTUAL DRIVE NUMBER
01 TRACK	ACTUAL TRACK NUMBER
03 SECTOR	ACTUAL SECTOR NUMBER
04 HEAD	ACTUAL HEAD NUMBER
05 RWBUFF	READ-WRITE BUFFER ADDR
07 RWLGT	READ-WRITE LENGTH - 1
09 RDS	READ SECT SUBROUTINE ADDR
0B WRS	WRITE SECT SUBROUTINE ADDR
0D STEP	SEEK SUBROUTINE ADDR IN PROM
0F RECAL	RECALIBRATE SUBROUTINE ADDR IN PROM
11 BOOTER	BOOTER SUBROUTINE ADDR
13 LISTAT	LIST STATUS SUBROUTINE ADDR
15 PRTAB	PRINT TABLE ADDR
17 PRWAIT	MAX PRINTER WAITING TIME IN 4 SEC UNITS
18 PRSTAT	PRINTER STATUS BYTE IS 0 IF PR ERR OCCURED
19 PR CONT	IF 0, NO MESSAGE IF PRINTER NOT RDY
1A BOOTDR	BOOTING DRIVE (0, FF OR 1)
1B DSKFLG	INTERNAL DISK FLAG
1C DMSTAT	DMA SHADOW BYTE
1D HDERSU	XEBEC ERROR ROUTINE ADDR FOR MAINTENANCE
1F DSKDR	00, C9 FOR STANDARD TRACK NUMBERING 24, C9 FOR OLD PHILIPS TRACK NUMBERING
21 PRSCR	PRINTSCREEN SUBROUTINE ADDR
23 MSWBYT	0 IF ROM, 2 IF RAM PROGR RUNS
24	C3 FOR JUMP
25 TINEX	ADDRESS OF EXTERNAL TIMER INT
27 KSTAT	KEY STATUS IS 0 IF NO KEY DEPRESSED
28 KBYTE	HOLDS THE LAST DEPRESSED KEY
29 CLOCK	4 BYTES LONG 60 HZ CLOCK
2D RESULT	7 BYTES LONG FIELD FOR FLOPPY RESULT BYTES

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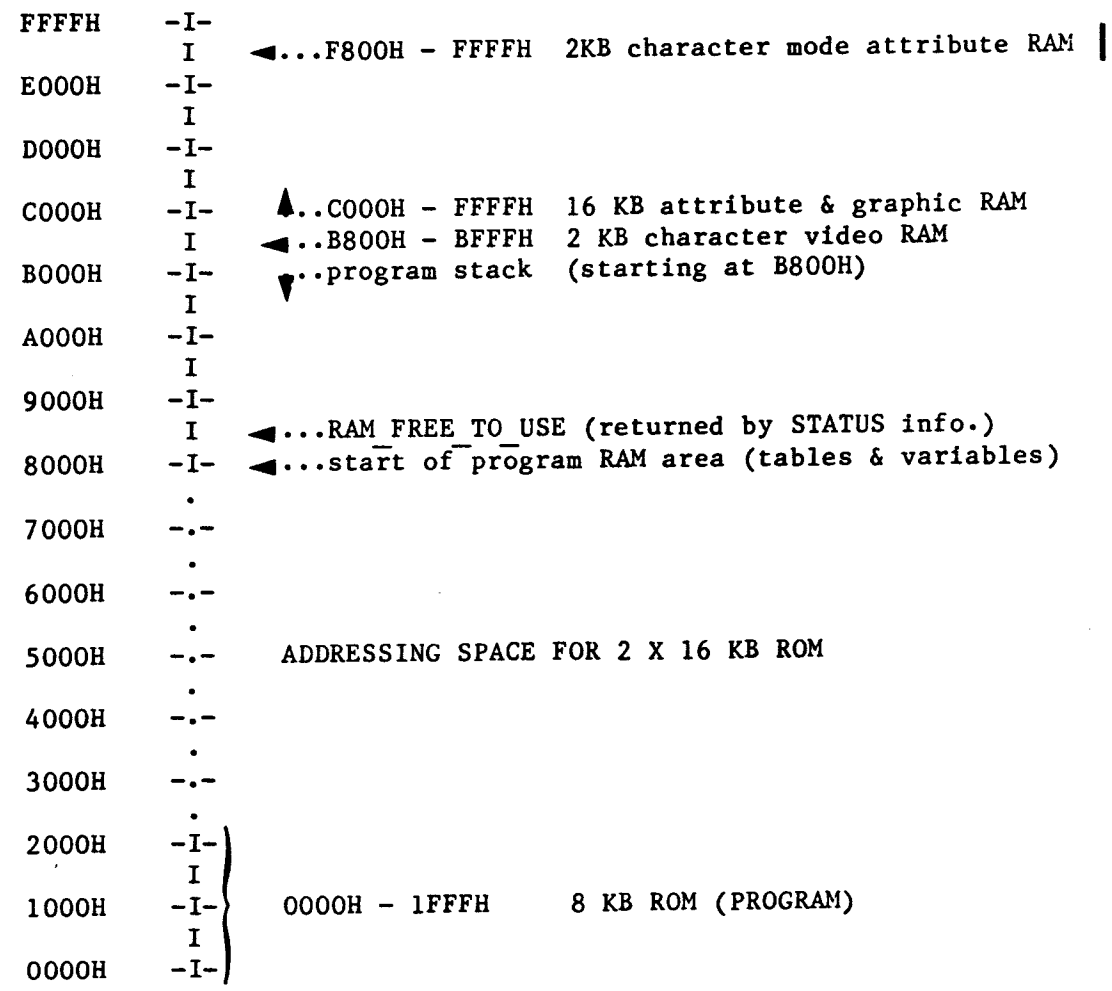
1 GENERAL

1.1 Memory Layout



The RAM area from RAM FREE TO USE to (B800H - STACK) may be used by the user-program (loaded in INTEL-HEX FORMAT). The area from C000H to F800H may also be used if the High resolution Graphic mode is not used. The RAM FREE TO USE is fixed for any particular software release but may change on re-issue.

Note: Amendments marked with a double bar relate to Release 1.3 Terminal Software onwards.

1.2 Features

1.2.1 COMMUNICATION

Asynchronous up to 19200 Bd.
(Queued in both directions in a 255 byte queue.)

1.2.2 KEYBOARD

8-bit code supporting national versions.
Standard ASCII key table in ROM, download of national versions is possible.
Keys queued.

1.2.3 SCREEN

8-bit code (national versions) 24 lines/80 characters.
Switchable to 25 lines.

Character Mode:

- Bidirectional scrolling
- Split-screen capability (partial scroll)
- Three attribute modes:
  - ° Manual: Read and write data from/to attribute page (normal memory access)
  - ° Auto duplicate: The read attribute data will be duplicated
  - ° Block mode: For "block moves" such as scrolling, the attribute page will be scrolled automatically
- Attributes:
  - ° Underline)
  - ° Invert) and all
  - ° Blink) combinations
  - ° 4 Intensity levels)
- Adjustable TABs
- Teletext graphics
- Text and Attribute back-transfer from screen possible

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High Resolution Graphics Mode:

- 2 selectable modes
  512 x 252 dots (no attributes)
  256 x 252 dots (3 intensity levels + background)

Each dot addressable
Simple vector handling:
- In Cartesian and Polar co-ordinates.
- Combination with character mode
  (characters: 21 lines/64 characters)

2 DETAILED DESCRIPTION

2.1 Communication

The communications control between the terminal and the CPU is done by the V24 control lines. Transfer is asynchronous at 19200 Baud.

The following transfers must be initiated by the software running on the mainboard side; i.e., not by the software loaded into the terminalboard.

2.1.1 TRANSFER - CPU TO TERMINAL

Note: RTS of the terminal is connected to CTS of the CPU and CTS of the terminal is connected to DTR of the CPU.

The terminal sets the signal RTS (data terminal ready) if it is ready to receive. (Normal situation).

The CPU can send data, but has to check if CTS is high during sending (this is done by hardware).
The terminal stores the characters in an internal queue and resets RTS when the queue is full or the terminal is no longer ready to receive.

2.1.2 TRANSFER - TERMINAL TO CPU

This is done the same way.

2.2 Keyboard

The pressed keys will be converted into the extended ASCII-code corresponding to the key tables stored in a queue. If there is a character in the queue the terminal will send it to the CPU as described.

2.3 Screen and Screen Codes

The screen is controlled by both single codes and ESC sequences.

2.3.1 SINGLE CODES

The single codes are shown in the following table:

ACTION		CODE	*	ACTION		CODE
Cursor Home	SOH	01H	*	Reset Terminal	CAN	18H
Cursor Forward	ACK	06H	*	CAPS_LOCK	SI	0FH
Cursor Down	LF	0AH	*	Lock Keyboard	EM	19H
Cursor Up	SUB	1AH	*	Unlock Keyboard	STX	02H
Cursor Back	NAK	15H	*	Bell-Beep	BEL	07H
Clear Screen	FF	0CH	*	Backspace	BS	08H
CR	CR	0DH	*	TAB	TAB	09H
End of Page (col 80, row 24/25)	EOT	04H	*			

Note: The Reset Terminal command (18H) causes a software reset (re-initialise) to the terminal software.
It has the following effects:

- Clears receive and transmit queues
- Resets TABs to every 8 columns
- Clears the screen
- Unlocks all locked areas
- 'CAPS_LOCK' becomes inactive
- Resets blink frequency to 320 msec
- Resets the screen to 24 lines

After the RESET command the terminal is unable to receive characters for about 500 msecs.

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2.3.2 ESCAPE SEQUENCE - SET ATTRIBUTE

SET ATTRIBUTE = ESC,0,b

where b = attribute byte
and 0 = numeric zero (ASCII 30H)

CAUTION! Take care that the correct attribute byte will be sent. The byte sent after 'ESC,0' will always be interpreted as the attribute byte.

An attribute can be set at any time and will remain valid until a new attribute is selected.

Attributes:

- Underline: characters underlined if bit 5 (UL) = 1
- Blink: characters blink if bit 1 (BL) = 1
- Invert: characters inverted if bit 4 (INV) = 1
- 4 Intensities: determined by bit 6 (in1) & bit 0 (in2)
- Blink frequency: changed if bit 7 (fr) = 1

Attribute byte:

	fr	in1	UL	INV	0	0	BL	in2
bit:	7	6	5	4	3	2	1	0

NOTE:

Unless the attribute byte is being used to define a new blink frequency (see below) bits 2 and 3 MUST be set to '0'.

Intensity	in1	in2
Quarter bright	0	0
Bold	0	1
Normal	1	0
Half bright	1	1

If bit 7 = 1, then bits 0 - 6 indicate the new blink frequency. The value ((bits 0 - 6) * 40) is the periodic time in millisecs.

EXAMPLES

ESC,0,&H63 gives characters:
- half bright
- underlined
- blinking

ESC,0,&H84 sets the blink time to 160 (4 x 40) msec.

In a BASIC environment the above examples would be entered in the form:

```
1. PRINT CHR$(27)+"0"+CHR$(&H63)

2. PRINT CHR$(27)+"0"+CHR$(&H84)
```

2.3.3 ESCAPE SEQUENCES - SCREEN CONTROL

ACTION		Code	ASCII
Cursor Addressing		ESC,Y,r,c	Y=59H/89
r = row = 0 to 23 (+20H offset)			
c = column = 0 to 79 (+20H offset)			
Erase to End of Line		ESC,K	K=4BH/75
Erase to End of Screen		ESC,k	k=6BH/107
Scroll Up one Line		ESC,S	S=53H/83
Scroll Down one Line		ESC,T	T=54H/84
Set TAB at Cursor Position		ESC,I	I=49H/73
Clear TAB at Cursor Position		ESC,G	G=47H/71
Clear all TABs		ESC,g	g=67H/103
Insert Line		ESC,L	L=4CH/76
Delete Line		ESC,l	l=6CH/108
Insert Character at Cursor Position	ON	ESC,Q	Q=51H/81
	OFF	ESC,R	R=52H/82
Delete Character at Cursor Position		ESC,P	P=50H/80
Insert Character Wrap-around	ON	ESC,N	N=4EH/78
	OFF	ESC,R	R=52H/82
Delete Character Wrap-around		ESC,O	O=4FH/79
Back TAB		ESC,i	i=69H/105
Cursor Visible		ESC,C	C=43H/67
Cursor Invisible		ESC,c	c=63H/99
Start Teletext Graphic		ESC,1	1=31H/49
End Teletext Graphic		ESC,2	2=32H/50
Lock Area for Scrolling		ESC,A,n	A=41H/65
n=number of lines			
Unlock Area from cursor		ESC,a	a=61H/97
Unlock all Areas		ESC,u	u=75H/117
Send Status		ESC,?	?=3FH/63
Send Text from Cursor Position		ESC,$,nn	$=24H/36
nn=number of characters			
Send Attributes of Text from Cursor		ESC,%,nn	%=25H/37
Load User Program (in INTEL HEX format)		ESC,p	p=70H/112
End of INTEL HEX Format (exits loader, normal operation)		ESC,:	:=3AH/58
Execute User Program		ESC,x	x=78H/120
Load New Keyboard Table		ESC,@	@=40H/64
Load New Screen Table		ESC,!	!=21H/33
Define Caps Lock Key		ESC,+,k,nn	+=2BH/43
(k=key,nn=upper limit (HEX))			
After terminal reset: ESC,+,80H,'Z' reactivates normal caps lock!			
Switch to 25 Video lines		ESC,^Y	^Y=19H/25
(^Y = CTRL Y)			

Note:All two-byte values are in Z80 format; low byte first!

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2.3.4 DESCRIPTION OF CONTROL CODES

Cursor home:	New cursor position is column 1/row 1.
Cursor forward:	Column + 1 (to next line if at end of line)
Cursor down:	New line. Scroll if last line or beginning of a locked area.
Cursor up:	One line up. If 1st line then new position is the bottom line.
Cursor back:	Column - 1 (to previous line if at start of line)
Backspace:	Same as cursor back.
TAB:	Cursor to next TAB position, default every eighth column.
Clear screen:	Erase the whole screen, cursor at home position.
CR:	Cursor at column 1 in current line.
End of page:	New cursor position is column 80 and row 24/25.
Reset terminal:	Initialise hardware and software. After RESET allow 500ms before sending data to terminal.
Lock keyboard:	Keyboard entries are re-enabled.
Set attribute:	A new attribute is used until the next "set attribute" command.
Cursor address:	Absolute cursor address with an offset of 20H (ESC,Y,20H,20H is the "home position").
Erase to end of line:	Clear all characters including cursor position to column 80.
Erase to end of screen:	Same as "Erase to end of line" to column 80 row 24/25.
Scroll up 1 line:	Scroll up the whole screen or area and clear last line.
Scroll down 1 line:	Same as above, but scroll down.
Set TAB:	Sets a new TAB position at cursor position.
Clear TAB:	A TAB position is removed at cursor position.
Clear all TABs:	Removes all TABS.
Insert line:	Scroll down the lines from cursor line + 1, and clear cursor line.
Delete line:	Scroll up the lines from cursor line +1 to cursor line.
Insert ON:	The next character will be inserted at cursor position, the last character in the line will be lost.
Insert wrap-around:	Same as "Insert" but the last character of the screen will be lost.
Insert OFF:	Exit insert mode, normal overwrite.
Delete character:	Delete character at cursor position, the last character in the line will be a blank.
Delete character wrap around:	Same as "Delete character" but last character of screen will be blank.

Back TAB: New cursor position is previous TAB position.

Start Teletext graphic: All characters between 20H & 3FH and 60H & 7FH are interpreted as teletext characters.

End Teletext: Revert to normal character mode.

Lock area: From cursor line, n lines (1 - 23/24) will be locked. (This area will not be scrolled by Cursor up and down, only by explicit "Scroll up (down)" command.
See Scroll Lock on following pages.

Unlock area: The cursor position area is unlocked.

Unlock all: Normal screen status.

Send status: 12 bytes terminal staus information will be sent (see STATUS INFORMATION).

Send text: nn characters from cursor position will be sent back.

Send attribute: Sends nn attribute bytes from cursor position. (Alphanumeric mode only).
Video attribute bytes differ from the 'SET ATTRIBUTE' byte and are arranged as follows:

bit
7 not used
6 not used
5 not used
4 in1 (see table)
3 in2 (see table)
2 INV (0 = INVERT ON)
1 BL (0 = BLINK OFF)
0 UL (0 = UNDERLINE ON)

Intensity	in1	in2
Quarter bright	0	0
Bold	1	1
Normal	0	1
Half bright	1	0

Load user PGM: **) This function enters a built-in INTEL_HEX_FORMAT loader. The load address may be anywhere in the free RAM areas (see memory layout). To find the RAM_FREE_TO_USE use the STATUS command (ESC,'?'). The terminal remains in the LOADER until it recognises an ESC,':' after a valid INTEL_HEX_FORMAT record. If loading is finished, normal terminal operation is possible.

End Loader: Exits the loader, enables normal operation.

Execute PGM: **) This function CALLs a previously loaded user program. The user program entry address is defined by an INTEL_HEX_FORMAT record with a record-type '01'. Ensure that the loaded program has such a record, otherwise a CALL to the location '0' will be performed (RESET). Only the last '01' record is valid. The user program should exit via a 'RET' instruction, making a normal return to the terminal program.

**) Additional information is given at the end of this section.

Load new keyboard table: Loads the following 360 bytes into the internal keyboard table. It consists of four 90 byte sub-tables; (NORMAL, SHIFT, SUPER-SHIFT, SHIFT-SUPER-SHIFT).
Note: If CONTROL pressed, all key codes are logically ANDed with '1FH'.

Load new screen table: Loads the following 256 bytes into the internal screen table.

Define Caps Lock key: The key 'k' is new Caps Lock key. There is no default key. 'nn' is upper limit for Caps Lock. Normal CAPS LOCK range is 41H - 5AH (A - Z) with 5AH as upper limit.

Switch to 25 video lines: Changes screen layout to 25 lines and 80 characters (must be initiated from normal alphanumeric mode only).

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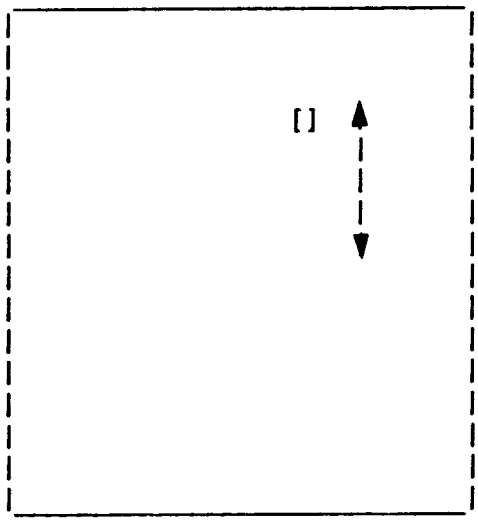
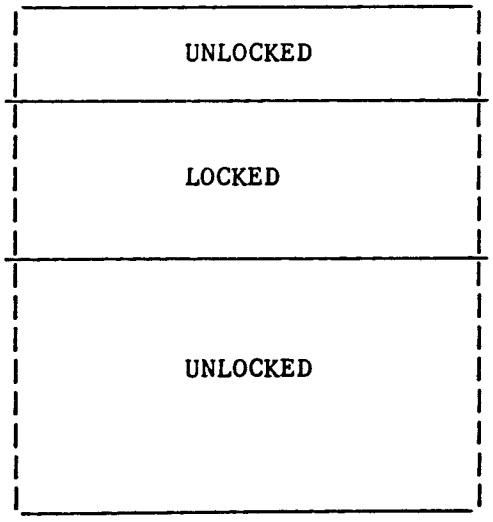
LOCKED AREAS AND SCROLLING POSSIBILITIES

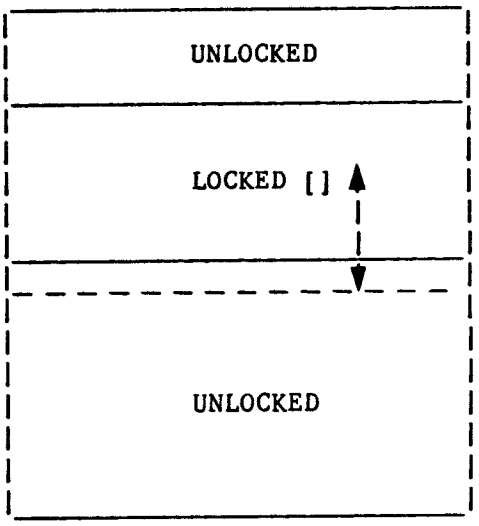
Normally, all 24/25 lines of the screen will be scrolled by a LINEFEED on the last line, a printable character on the last screen position or by an explicit SCROLL UP - SCROLL DOWN command. For some applications it is useful not to scroll the whole screen e.g., in word porcessing (tab - format line).
On the P2000C it is possible to lock certain areas of the screen, or the whole screen, from automatic scrolling. This is done with the command ESC,'A',n. It locks n lines, starting with the cursor line. Normal scrolling is still possible with the explicit SCROLL UP - SCROLL DOWN commands in the unlocked areas. (Cursor must be in the unlocked area).
If cursor is in a locked area any scroll command has no effect.

EXAMPLES

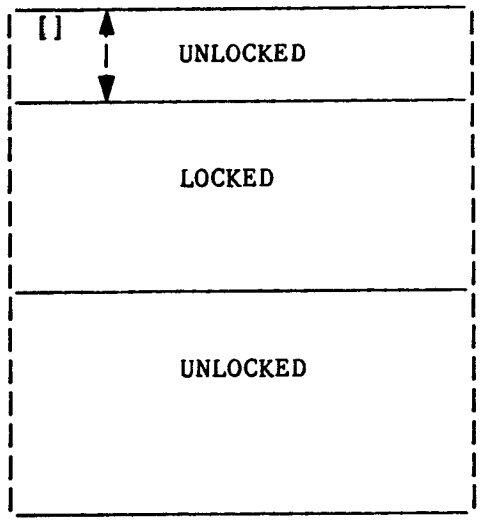




ALLOCATING MORE SCROLL LOCKED LINES



With sequence 1BH,41H,5H with cursor in line 10, the lines 10 - 14 will be locked. As lines 10, 11 & 12 are already locked, the locked area will simply be increased.



Locking an additional lines from line 0 with command 1BH,41H,6H will lock all lines to 14. Only lines 15 - 23 are now unlocked.

Angle ALPHA "A" is in steps of one degree (0 to 360).

Defining angle "A"; 2 bytes (low order byte FIRST in command)
low order byte: = A MOD 256
high order byte: = INT(A/256)

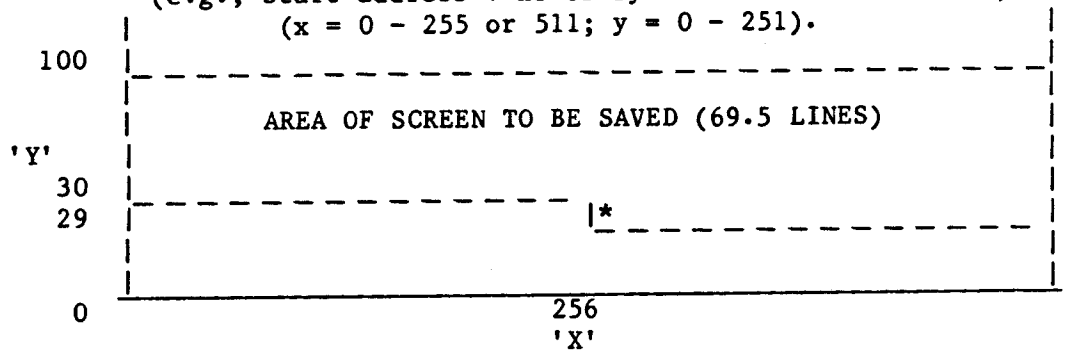
Defining value "abs"; 2 bytes (low order byte FIRST in command)
low order byte: = abs MOD 256
high order byte: = INT(abs/256)

DESCRIPTION OF SEND/RECEIVE PICTURE

In either high resolution graphics mode, an area of the screen can be stored for fast retrieval with the ESC 'r' & 't' sequences.

The sequence ESC,t,xy,nn (Receive Picture - the main processor 'receives' the information) defines the first co-ordinate of the screen image to be stored (nn). In the 512 x 252 mode the 'x' co-ordinate requires 2 bytes. The number of bytes must be calculated at 64 bytes for each complete line. The first byte to be stored is calculated from the xy co-ordinates. The screen is filled upwards.

CAUTION: Ensure that screen addresses are within limits.
(e.g., start address + no of bytes within screen area)
(x = 0 - 255 or 511; y = 0 - 251).



ESC, 't',	0 , 1	, 29,	(69.5 x 64)	
	x1, x2	, y ,	n1	, n2
1BH, 74H,	0 , 1	, 29,	96	, 17

The sequence ESC,r,xy,nn (Send Picture - the main processor 'sends' the information to the terminal) defines the start position of the picture on the receiving screen (xy) and the number of bytes to be transferred (nn).

ESC, 'r',	0 , 1	, 29,	(69.5 x 64)	
	x1, x2	, y ,	n1	, n2
1BH, 72H,	0 , 1	, 29,	96	, 17

It is important that the value x1 is divisible by 8 as the absolute start address of the picture must always be defined from the beginning of a character block.

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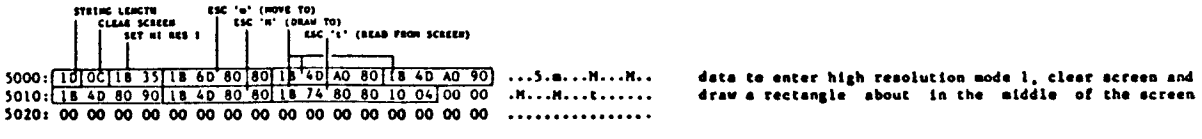
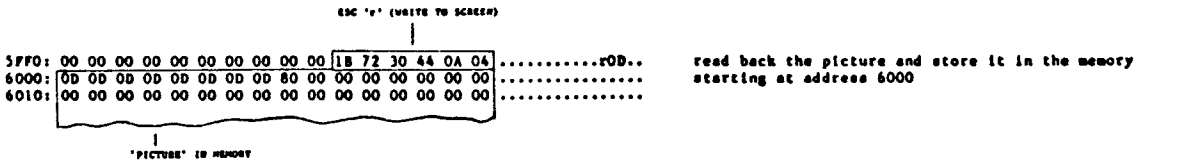
EXAMPLE PROGRAM SHOWING SEND/RECEIVE PICTURE USING ZSID

```
4000  LD   HL,5000   nr. of bytes to be printed (stored at 5000H)
4003  LD   B,(HL)
4004  INC  HL
4005  LD   C,(HL)    get next data byte
4006  PUSH BC        save register
4007  PUSH HL        save register
4008  CALL F60C      print (on console)
400B  POP  HL        restore register
400C  POP  BC        restore register
400D  DJNZ F5  (4004)loop for all bytes to be printed
400F  NOP
4010  NOP
4011  LD   C,04      number of bytes to read back from screen (410hex)
4013  LD   B,10
4015  LD   HL,6000   write bytes from screen to memory starting at address 6000
4018  PUSH BC        save register
4019  PUSH HL        save register
401A  CALL F609      get one byte from screen
401D  POP  HL        restore register
401E  POP  BC        restore register
401F  LD   (HL),A    save byte from screen to next free location
4020  INC  HL        move to next location
4021  DNJZ F5  (4018)loop for all bytes requested
4023  LD,  B,FF      next 256 bytes
4025  DEC  C         until register C contains 0
4026  LD   A,C
4027  CP   FF
4029  JR   NZ,ED (4018)
402B  NOP
402C  NOP
402D  NOP
402E  NOP
402F  NOP
4030  NOP
4031  LD   C,04      nr. of bytes to be printed (416hex)
4033  LD   B,16
4035  LD   HL,5FFA   start printing bytes at address 5FFA
4038  PUSH HL        save register
4039  PUSH BC        save register
403A  LD   C,(HL)    print byte, addressed by register HL
403B  CALL F60C
403E  POP  BC        restore register
403F  POP  HL        restore register
4040  INC  HL        move to next location until all characters are printed
4041  DJNZ F5  (4038)
4043  LD   B,FF
4045  DEC  C
4046  LD   A,C
4047  CP   FF
4049  JR   NZ,ED
404B  .              stop program here (set a breakpoint, or execute a return)
```

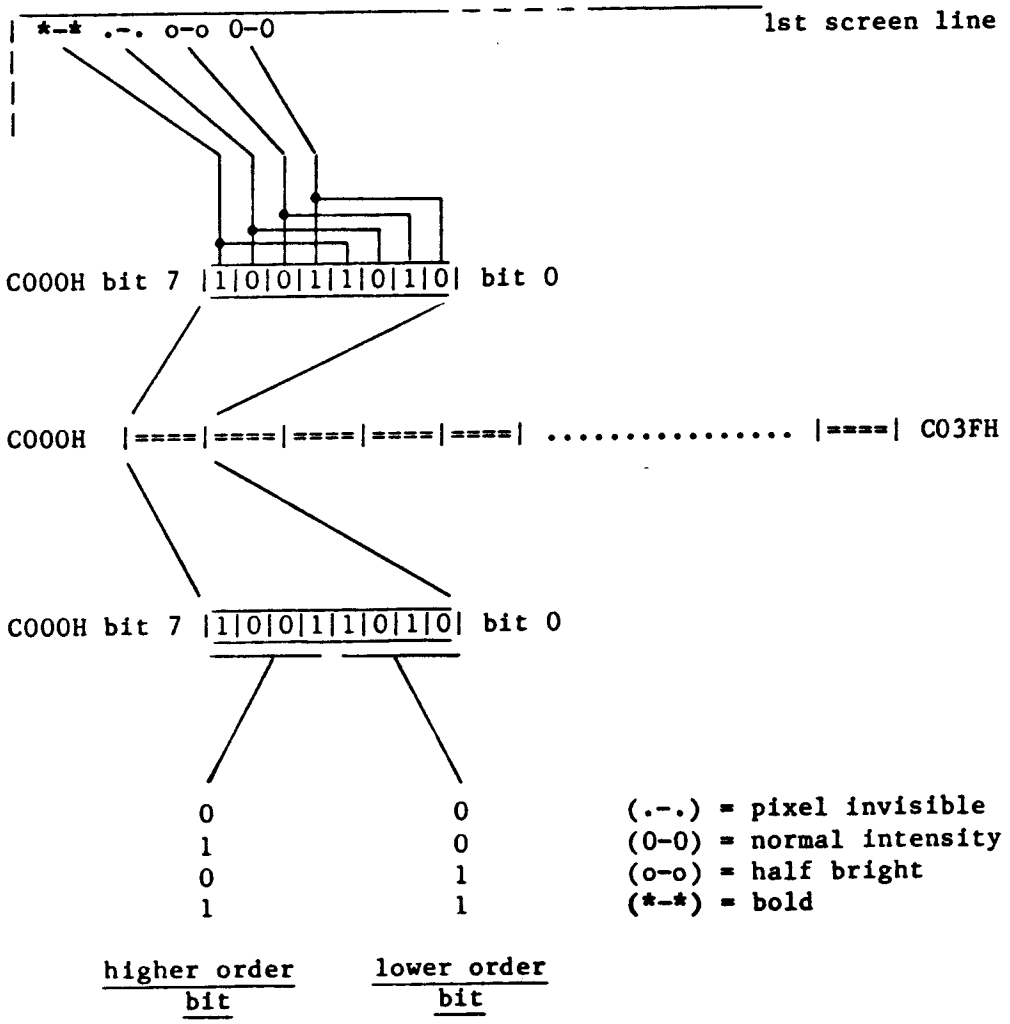




Operating Systems
Terminal Board Firmware

256 X 252 MODE

In this mode, 1 byte represents 4 pixels, each pixel consisting of TWO adjacent screen dots. The first 64 bytes of graphic RAM (C000H to C03FH) represents the first (top) line of the screen, 64 x 4 giving the 256 pixels in each line. Each pixel is defined by 2 bits, with the msb (most significant bit) and msb minus 4 relating to the leftmost screen pixel. The values of these two bits determine the pixel intensity, i.e.,



2.4 Status Information

The terminal status information is given in the form of a 12 byte string, as shown below:

Byte Number		Contents
1		cursor position - column
2		cursor position - row
3		character at cursor position
4		status flag
	bit:	
	0	1 = graphics on (see note below)
	1	0 = graphics mode 1 1 = graphics mode 2
	2	1 = teletext on
	3	1 = insert mode on
	4	1 = insert wrap-around on
	5	1 = keyboard is locked
	6	reserved
	7	reserved
		internal graphic cursor field
5,6		x co-ordinate
7		y co-ordinate
8,9		free space pointer (beginning of RAM area for user program in Z80 notation; low byte first)
10,11,12		reserved for future use

Note: If status flag bit 0 = 0, then bit 1 has no meaning.

Operating Systems
Terminal Board Firmware

Note: User Programs in the Terminal Board:

The following notes are suggestions for writing programs for running in the Terminal Board.

1. Define the address to which you wish to write the program in the Terminal Board e.g., 8E00H, which will be used in this note to represent the actual address used.

   The lowest possible address that you can use can be seen in the status bytes (ESC,?). See program example on following page.

2. Write the program. If you use the Microsoft M80 macro assembler use the ".PHASE 8E00H" command at the beginning (or your actual address value)

3. Assemble the program

4. Link the program. If you use the Microsoft L80 linker type the following:

   L80 PROG-NAME/N,PROG-NAME/P:8E00/X/E.

   This links a file in INTEL_HEX format at the chosen address.

5. Load the program to the Terminal Board with:

   ESC,p

   Send the PROG-NAME.HEX file to the Terminal Board.

   EXIT INTEL_HEX loader with:

   ESC,:

6. Initialise the user program address

   This must be done even if the address is the same as the address given in the status byte.
   Initialisation is carried out with the following sequence:

   ESC, p
   :008E000100 [do not forget the colon!]
   ESC,:

7. Run user program with:

   ESC,x

To repeat user program calls, repeat step 7 only. Several programs can be loaded on various places in the user program area and then selected (as in steps 6 and 7) via their start address.

ASSEMBLER PROGRAM - STATUS BYTES

```
0100  NOP
0101  NOP
0102  NOP
0103  LD   C,1B      ;LD C, ESC
0105  CALL F60C      ;CALL CONOUT
0108  LD   C,3F      ;LD C, '?'
010A  CALL F60C      ;CALL CONOUT
010D  LD   B,0C      ;LOOP X 12
010F  LD   DE,0103   ;ADDRESS FOR BUFFER
0112  CALL F609      ;CALL CONIN
0115  LD   (DE),A    ;ONE BYTE TO BUFFER
0116  INC  DE        ;INCREMENT POINTER TO BUFFER
0117  DJNZ F9        ;DJNZ TO 0112
0119  NOP
011A  NOP

D130
0130: 00  17  00  02  00  00  00  6D  8D  00  00  00  .....
```

Detailed Description and Servicing
Keyboard

1 GENERAL

The keyboard has been specially designed for the P2000C microcomputer, with particular attention having been paid to the ergonomic requirements of the professional user. It is a low profile unit with sculptured keys on the typewriter section and has separate function and numeric pads. An LED is incorporated in the 'shift-lock' key to indicate that the keyboard is in the shift-lock mode.
The keyboard is separate from the main unit and connected by a spiral cable. It contains only the keyswitch matrix and a few TTL packages, which reduces the number of wires required in the connecting cable.
For transportation the keyboard fits inside the facia of the main unit and is secured by the carrying strap. The keyboard connecting cable is stowed, with the mains cable, in a compartment at the back of the unit.

1.1 National Versions

Although the keyboard is obtainable in various national versions, the electronics of each is identical and only the keytops differ. The adaptation of the basic keyboard to meet national requirements is carried out by the use of the Keyboard and Video tables via the Configuration program. (See CP/M Reference Manual).

This chapter contains illustrations of two national keyboards: Austrian/German and United Kingdom.

Detailed Description and Servicing
Keyboard

2 CIRCUIT DESCRIPTION

The keyboard is scanned in synchronisation with video refresh operation of the CRTC. At each key depression the light pen input is activated and the key is identified by means of the light pen register in the CRTC. (This restricts the use of the keyboard to functioning with the video circuits).

Key rollover and key lockout depends on the position of the key in the scanning row. If the 'key 2' is depressed while 'key 1' remains depressed; two situations are possible:
- If 'key 2' stands later in the scanning row than 'key 1', it will be encoded when 'key 1' is released.
- If 'key 2' stands earlier in the scanning row it will be encoded immediately.

Special keys (shift, supershift, control and shift-lock) are encoded whenever they are depressed.

The circuit action is described further under Terminalboard - Keyboard Logic.

2.1 Pinning

The keyboard cable 5103 107 81270 with 2 plugs 6-pole DIN 45 322 (240°) has the following pin designation:

PIN	SIGNAL	I/O
1	count	O
2	vertical sync	O
3	ground	O
4	light pen	I
5	+12V	O
6	led	O
screening to ground		

Detailed Description and Servicing
P2000C Options - 8088 Copower Board P2093 - Introduction

1 GENERAL

This chapter (3.9) will cover the following topics:

- 3.9 1-x Introduction
  - 1 General
  - 2 Product Overview
  - 3 Copower Board Signals
- 3.9 2-x Software Description
  - 1 General
  - 2 Interprocessor Communication
- 3.9 3-x Hardware Description
  - 1 General Description
  - 2 Block Diagram
  - 3 Electrical Interfaces
  - 4 Detailed Circuit Descriptions
    - 1 Timing Circuit
    - 2 Bus Controller
    - 3 8088 CPU
    - 4 Z80A Interface
    - 5 RAM Banks (including Memory Access & Refresh)
    - 6 8087 Math processor (optional)

2 PRODUCT OVERVIEW

With the addition of the P2093 Copower Board, the P2000C can be upgraded to a 16 bit system.

The subsystem contains:

- 8088 CPU operating at 5 MHz
- two banks of 8 bit wide RAM which can be equipped with 64 KByte or 256 KByte dynamic RAM chips
- the control logic for interfacing to the P2000C extension bus

By using different RAM chips and appropriate jumper settings the following extension RAM sizes are available:

128 KByte : 2 banks of 64 KBit RAM chips
256 KByte : 1 bank of 256 KBit RAM chips
512 KByte : 2 banks of 256 KBit RAM chips

In addition to the extension RAM, the Mainboard RAM Bank (64 KByte) is also accessible to the 8088 CPU. This is configured as shared memory. It provides the possibility of 8088 CPU startup after a system reset.

2.1 Two Mode Operation

Either the 8088 or the Z80A can control operation of the system (8088 Master Mode/ Z80A Master Mode).
In case of 8088 Master Mode, the 8088 CPU becomes the main processor in the multiprocessor system. In this case the Mainboard acts as an I/O processor for the 16 bit system.

In the Z80A Master Mode, the 8088 CPU acts as a memory disk controller for the 8 bit CP/M or p-System.

Detailed Description and Servicing
P2000C Options - 8088 Copower Board P2093 - Introduction

3 COPOWER BOARD SIGNALS

Signal	Description
AD0 - AD7	Address Data Bus lines
A8 - A15	Address Bus lines
A16 - A19	Address/Status lines
AB0 - AB15	Address lines at Mainboard interface
A16L - A19L	Latched Status lines
AIOWC-N	Advanced I/O Write Command
ALE	Address Latch Enable
AMWC-N	Advanced Memory Write Command
BAO/BAO-N	Bus Acknowledge Out
BUSAK-N	Bus Acknowledge
BUSEN-N	Bus Enable
BUSRQ-N	Bus Request
CAS0-N	Column Address Strobe 0
CAS1-N	Column Address Strobe 1
CASEN-N	CAS Enable
CLK	Clock (5 MHz)
D0L - D7L	Latched Data lines
DT/R-N	Data Transmit/Receive (Hi = Transmit; Lo = Receive)
EINT-N	External Interrupt
EMA-N	External Memory Access
ENIHI-N	Enable High Address
ENILO-N	Enable Low Address
ID0 - ID7	Internal Data lines at Mainboard interface
IMA-N	Internal Memory Access
INACC	Internal Access
INTA-N	Interrupt Acknowledge
INTR	Interrupt 8088
IORC-N	I/O Read Command
IORQB-N	I/O Request Buffered
IVSET-N	Interrupt Vector Set
LOCK	Locks 8088 access to Z80A memory
M1B-N	Z80A CPU Memory cycle
MA0 - MA8	Multiplexed Address lines
MEMACC	Memory Access
MRDC-N	Memory Read Command
MREQ-N	Memory Request
MRQB-N	Memory Request Buffered
OSC	Oscillator - buffered quartz output (15 MHz)
PORTSET-N	I/O decoder output; sets LOCK and RES88
RA-N	Refresh Access
RAS-N	Row Address Strobe
RDB-N	Read at Mainboard interface
REFREQ	Refresh Request
RES/RES-N	Reset
RES88-N	Reset 8088; derived from D1L, RES-N, PORTSET-N
RESI&E	Reset Internal/External Memory Access
RESRC	Reset Refresh Counter
RESRC-N	Reset Refresh Counter
S0-N - S2-N	Status 0 to Status 2
WRB-N	Write Buffered at Mainboard interface

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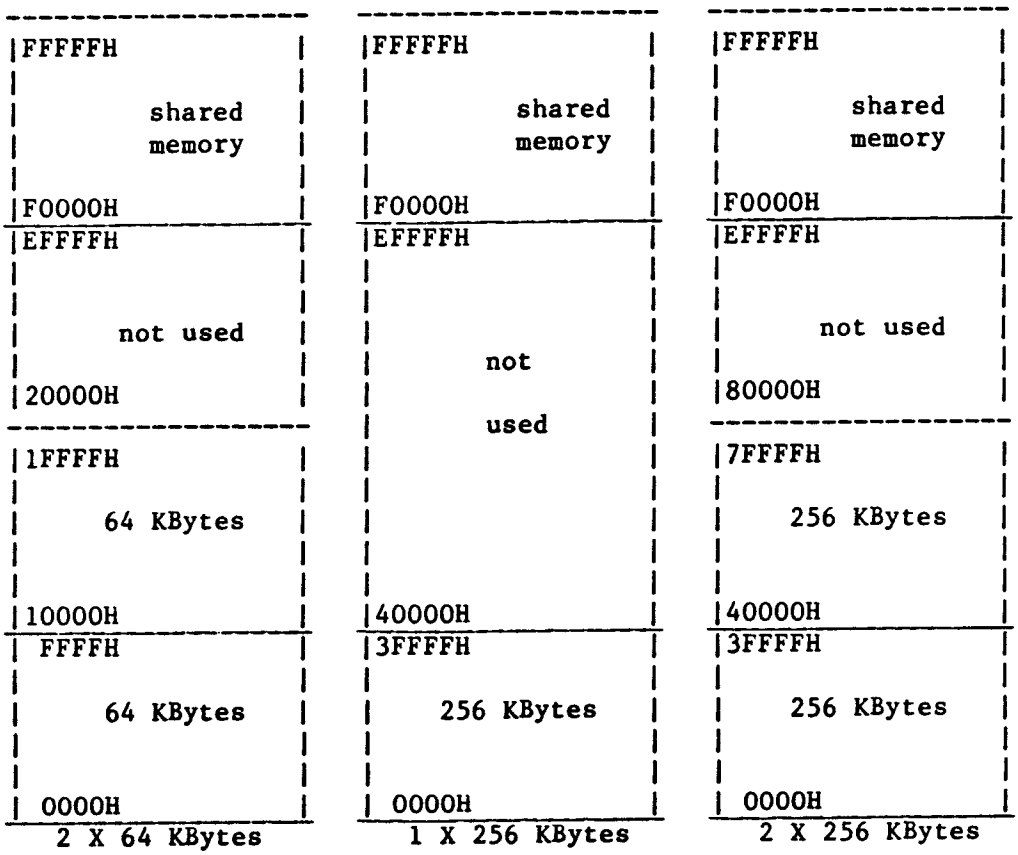
1 GENERAL

1.1 Memory Configurations

The memory layouts described below give the address range of the 8088 16 bit CPU. RAM is allocated in 8 bit words but the 8088 works internally with 16 bit words. Word access in the 8088 software uses a CPU internal sequencer which splits up the memory access into two memory cycles. Two bytes on consecutive locations are then accessed.



2 INTERPROCESSOR COMMUNICATION

There are three means of communication between the mainboard Z80A processor and the 8088 16 bit CPU and two methods by which the Z80A can take control of the 8088.

2.1 Shared Memory Concept

Data can be transferred via the 64 KByte shared memory area between the two processors. In the 8088 address map the shared memory is allocated from address F0000H to FFFFFH. In the Z80A address map the whole accessible 64 KByte memory area from address 0000H to FFFFH is shared with the 16 bit CPU.

For optimum system performance the shared memory area should only be used as bootstrap memory for the 8088 processor and as data communication area for both processors. Any 8088 access to the shared memory, via a DMA operation as seen from the Z80A CPU, decreases the performance of both the Z80A system and the 8088 subsystem. Accesses to the "internal" memory of the 8088 (address 0 to 7FFFFH) have no effect on the performance of the Z80A processor.

2.2 8088 Interrupt

The Z80A CPU can signal the end of an I/O operation to the 8088 CPU in 8088 master mode or trigger a memory disk action in Z80A master mode via a Z80A I/O write operation to an even address in the I/O address space (30H to 3EH). This I/O write operation triggers an 8088 interrupt with the interrupt vector set to the value written to the I/O port.

2.3 Z80A Interrupt

The 8088 CPU can signal the end of a memory disk action in Z80A master mode or trigger the start of a Z80A I/O operation in the 8088 master mode via any port write command. This I/O write command triggers an interrupt on the external interrupt input of the P2000C extension bus. The software and hardware on the Z80A side of the system must be set up to recognise this interrupt. (P2000C mainboard, 5103 108 0271.: Jumper J 15 set for external interrupt, CTC2 channel2 (I/O address 26H) must be programmed to counter mode with a time constant of 1).

2.4 8088 Reset

The Z80A processor on the P2000C mainboard can force the 16 bit 8088 processor into a reset condition by writing a logical "0" to data bit 1 of any odd address in the I/O address space from 31H to 3FH. This is the default condition after reset or after power-up.
Before the reset signal is removed from the 8088 subsystem a boot-strap loader program has to be written to memory locations FFF0H in the Z80A address space (FFFF0H in the 8088 address space, the program start address for the 8088 after reset!).
Because of this, no IPL ROM is needed on the 8088 subsystem.

2.5 8088 Lock

The Z80A processor on the P2000C mainboard can prevent the 8088 CPU from accessing the shared memory area if it has to perform time critical tasks such as disk read operations. The access is prevented by writing a logical "1" to data bit 0 of any odd address in the I/O address range from 31H to 3FH.

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Detailed Description and Servicing
P2000C Options - 8088 Copower Board P2093 - Hardware Description

1 GENERAL DESCRIPTION

The heart of the 16-Bit extension subsystem is the iAPX 88/10, an 8-Bit HMOS Microprocessor with 16-Bit internal architecture. The 8088 version is used, which works at 5 MHz. It operates in maximum mode, controlled by an 8288 Bus Controller.

An 8087 Numeric Data Coprocessor may be fitted as an option.

When the system is operating in the 8088 mode the Z80A operates as an I/O processor. Only the 8088 CPU can access the 8088 RAM.
RAM refresh, timing control (RAS and CAS) and the multiplexer signals are generated in a memory and refresh controller circuit.

In Z80A mode, the 8088 CPU works as a memory controller.

The shared memory can be accessed by both CPUs. This is the system memory located on the P2000C Mainboard. Refresh of this memory is done by the Z80A CPU.
To ensure proper refresh of the mainboard memory, only single byte accesses are possible for the 8088 CPU, after which the Z80A has the opportunity to access at least one byte.

If the 8088 wants to access the shared memory, the 8088 'memory and refresh controller' generates a BUSRQ-N signal to the Z80A processor at an early stage of the 8088 bus cycle. (see timing diagram). The Z80A CPU tri-states its ADDR, DATA and control bus and then activates BUSACK-N (BAO derived from BUSACK by mainboard priority resolver). BAO-N and ALE then latch the control, address and data signals onto the Z80A busses. The memory access is then carried out.

If the Z80A is performing a time critical operation, the LOCK signal is produced via an I/O-write to inhibit the BUSRQ-N. If the 8088 tries to access the shared memory at this time the 8088 is forced into a wait condition (Tw clock cycles) until the BUSRQ-N is granted with the BUSAK-N signal.

The 5 MHz System Clock (CLK) is derived from the 15 MHz quartz oscillator.

The only I/O command that the 8088 CPU can perform is an I/O Write to any address which results in the generation of an interrupt to the Z80A system.

The Z80A interface circuitry includes an I/O decoder for addresses in the range 30H to 3FH. Z80A access to even I/O addresses in this range sets an interrupt flip flop and latches an interrupt vector into an 8 bit latch. When the 8088 acknowledges the interrupt, the flip flop is reset and the interrupt vector is enabled onto the 8088 multiplexed address data bus.
Z80A access to odd addresses sets a write only I/O port. LOCK and RESET.

2 BLOCK DIAGRAM

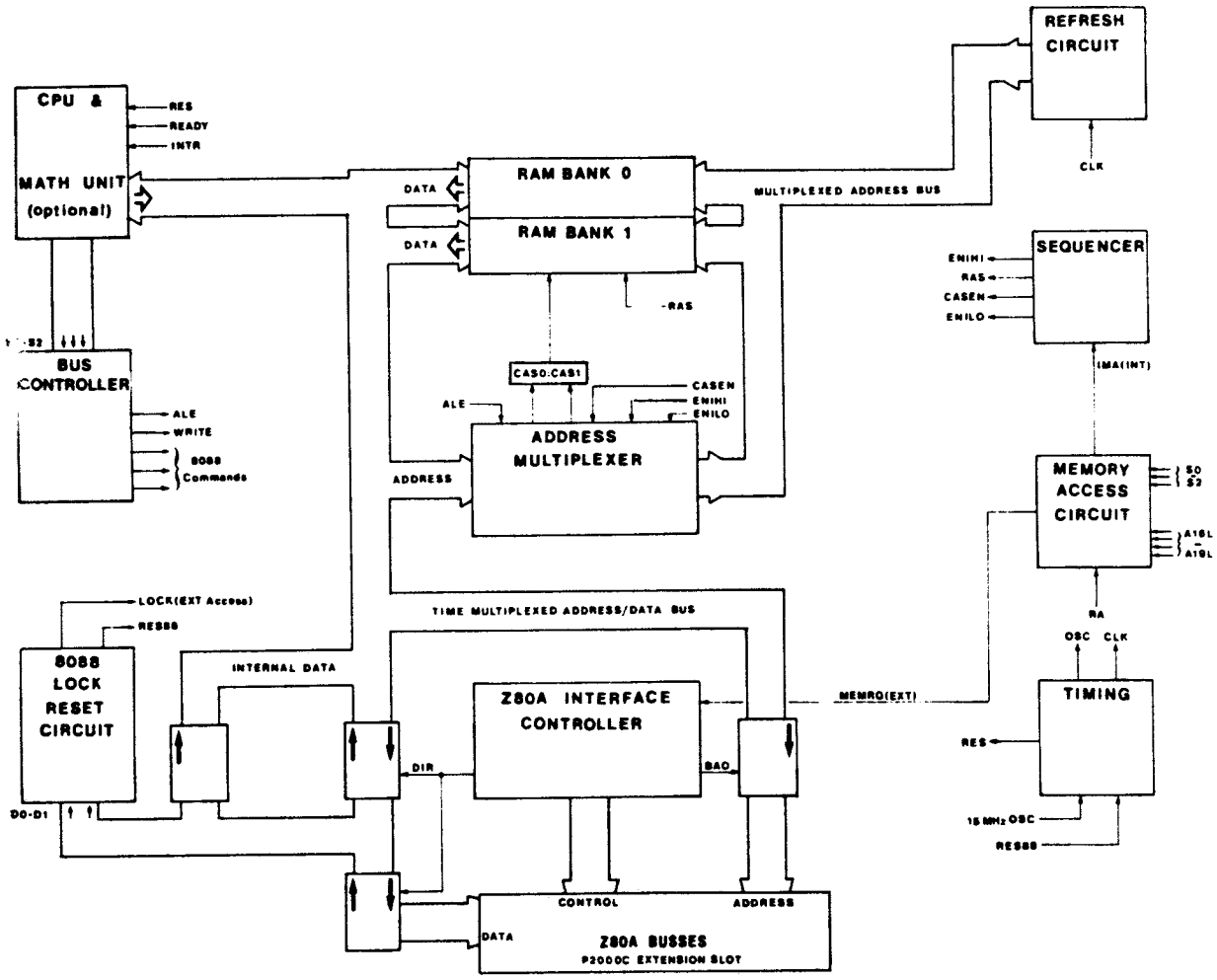

Figure 3.1 8088 Copower Board - Block Diagram

3 ELECTRICAL INTERFACES

The only electrical interface between the P2000C mainboard and the 16-Bit Extension Subsystem is via the 120 way extension slot. The lines used are shown in table 9.1; directions with respect to the Mainboard.

Table 9.1 Interconnections - 16-Bit Extension Subsystem

PIN	SIGNAL	DIRECTION	PIN	SIGNAL	DIRECTION
01	NC		53	IORQB-N	OUT
03	phi	OUT	55	AB15	IN
05	NC		57	AB14	IN
07	NC		59	AB13	IN
09	NC		61	AB12	IN
11	NC		63	AB11	IN
13	EINT-N	IN	65	AB10	IN
15	NC		67	AB9	IN
17	NC		69	AB8	IN
19	NC		71	AB7	IN
21	NC		73	AB6	IN
23	RES-N	OUT	75	AB5	IN
25	NC		77	AB4	IN
27	NC		79	AB3	IN
29	NC		81	AB2	IN
31	NC		83	AB1	IN
33	NC		85	AB0	IN
35	BAO-N	OUT	87	ID7	IN/OUT
37	NC		89	ID6	IN/OUT
39	BUSAK-N	OUT	91	ID5	IN/OUT
41	BUSRQ-N	IN	93	ID4	IN/OUT
43	WRB-N	OUT	95	ID3	IN/OUT
45	RDB-N	IN	97	ID2	IN/OUT
47	NC		99	ID1	IN/OUT
49	M1B-N	IN	101	ID0	IN/OUT
51	MRQB-N	IN			

Pins 117 - 120 +5 V
Pins 2, 4, 6 ... 106, 103, 105, 111 & 112 - GND

4 DETAILED CIRCUIT DESCRIPTIONS

4.1 Timing Circuit

4.1.1 GENERAL

The timing circuit comprises the following items:

7040 - Clock Generator Driver (8284A)
7043 - 74 S 10 - 3 input NAND
7036 - 74 LS 00 - 2 input NAND
7055 - 15 MHz Quartz
4004 - Resistor network
3016) 2 X 560 Ohm resistors for xtal stabilisation
3017)

Inputs:

15 MHz (X1,X2), RDY1, RDY2, RES-N (= RES88-N).

Outputs:

READY, CLK (5 MHz), OSC (15 MHz), RES.

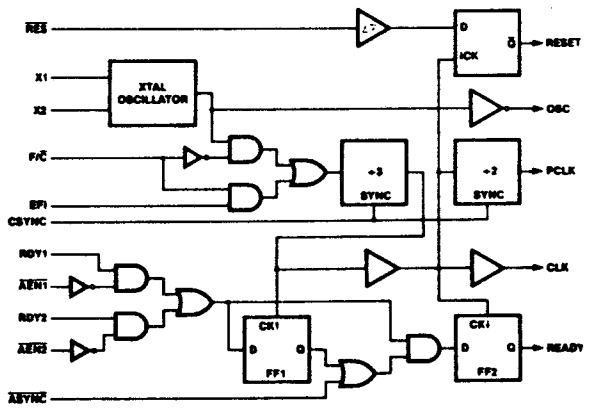

Figure 3.2 8284A Clock Generator - Block Diagram

4.1.2 FUNCTIONAL DESCRIPTION

The 15 MHz quartz (item 7055) and the 8284A Clock Generator (item 7040) form the 'timing circuit' of the Copower Board. The buffered oscillator output OSC is provided on pin 12 (TTL level). A divide by three circuit gives the buffered 5 MHz CLK output which is available on pin 8. The two resistors, items 3016/3017, ensure quartz stability.

In addition to the timing signals, the system signals READY and RES are also produced.

RDY1 is derived from INTA-N and AIOWC-N and IORC-N (item 7043)
RDY2 is derived from IMA-N and MREQ-N (item 7036)

When RDY1 or RDY2 goes active, READY will be produced on the falling edge of the next complete CLK pulse, thus introducing a slight delay into the production of the READY signal. READY is switched inactive by a CLK falling edge when both RDY1 and RDY2 have gone inactive.

The 8088/8087 RESET signal, RES, is the RES88-N signal, synchronised to the falling edge of CLK.

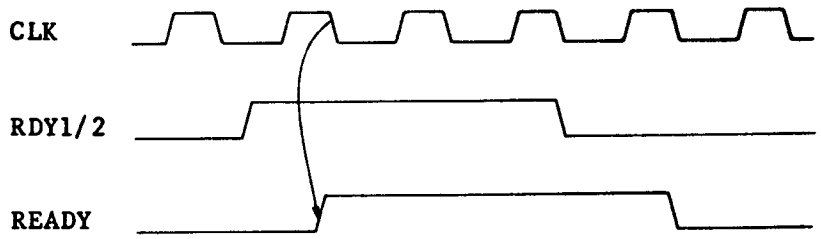

Figure 3.3 Timing Diagram: RDY1, RDY2, CLK and READY

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4.2 Bus Controller

4.2.1 GENERAL

The bus controller provides command and control timing generation as well as bi-polar bus drive capability while optimising system performance. It comprises the following items:

7041 - Bus Controller 8288
4004 - sets AEN-N to LOW (enables I/O Bus mode)
4005 - sets IOB (I/O Bus mode) and CEN (Command Enable) to HIGH

Inputs:

S0-N, S1-N, S2-N, CLK

Outputs:

MRDC-N, AMWC-N, INTA-N, ALE, DT/R-N, AIOWC-N, IORC-N

When using the 8088 in maximum mode, the use of 8288 (bus controller) is mandatory. Maximum mode has also to be selected in order to be able to use the 8087 (math coprocessor).

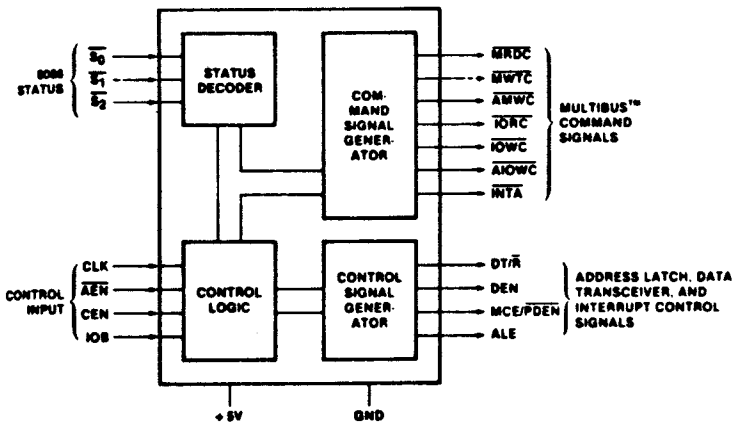

Figure 3.4 8288 Bus Controller - Block Diagram

4.2.2 FUNCTIONAL DESCRIPTION

As signal IOB (Input/Output Bus Mode) is strapped HIGH (pin 1), the 8288 operates in the I/O Bus Mode. The signal CEN (Command Enable) is strapped HIGH (pin 15) to enable the command outputs. The signal AEN-N (Address Enable) is strapped LOW (pin 6), it has no effect in the I/O Bus Mode.

The 8288 decodes the 8088 status logic (S0-N to S2-N) and determines which of the following command signals is to be active:

$\overline{S0}$	$\overline{S1}$	$\overline{S2}$	Processor State	8288 Command
0	0	0	Interrupt Acknowledge	INTA-N
1	0	0	Read I/O Port	IORC-N
0	1	0	Write I/O Port	AIOWC-N
1	1	0	Halt	none
0	0	1	Code Access	MRDC-N
1	0	1	Read Memory	MRDC-N
0	1	1	Write Memory	AMWC-N
1	1	1	Passive	none

In addition to the command signals, the 8288 also produces two control signals. These are:
Address Latch Enable (ALE) and Data Transmit/Receive (DT/R-N)

The following paragraphs give the uses of the 8288 command and control signals:

4.2.2.1 Interrupt Acknowledge - INTA-N

This signal is used:

° In the timing circuit, for production of the RDY input

° As output control input to 8-bit register (item 7023)

° To reset the INTR flip-flop (2 X NAND 7048)

4.2.2.2 Read I/O Port - IORC-N

This signal is used:

° Exclusively for production of the RDY input in the timing circuit. As no input ports are available, 'Read I/O Port' has no significance.

4.2.2.3 Write I/O Port - AIOWC-N

This signal is used:

° In the timing circuit, for production of the RDY input

° As EINT-N to Mainboard

4.2.2.4 Code Access/Read Memory - MRDC-N

This signal is used:

° As RDB-N to Mainboard

4.2.2.5 Write Memory - AMWC-N

This signal is used:

° As WRB-N to Mainboard

° As WE-N input to 8088 RAM Banks

4.2.2.6 Address Latch Enable - ALE

This signal is used to:

° Clock the D-Flip Flop (item 7052) for production of the signal RESI&E (Reset Internal and External Memory Access)

° Gate the 8-bit D-latches (items 7018/7031) and enable the two 2-bit D-latches (item 7034)

4.2.2.7 Data Transmit/Receive - DT/R-N

This signal is used to:

° Provide direction information for the 8-bit bus transceivers (items 7024/7025)

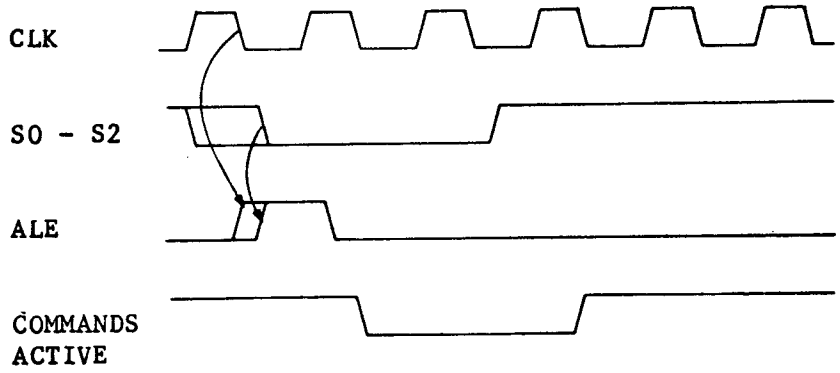

Figure 3.5 Timing Diagram - Bus Controller

4.3 Central Processor Unit - 8088

4.3.1 GENERAL

The CPU is an Intel iAPX 88/10 working in maximum mode. It has an 8-Bit data bus interface and 16-Bit internal architecture. The 8088 operates with a clockrate of 5 MHz.

The 8088 provides a 20-Bit address to memory, capable of accessing up to 1 million bytes. The usable addresses for the Copower Board, with each RAM layout, are shown in paragraph 1.1.

16-Bit operands can be located on even or odd address boundaries and occupy two adjacent locations in memory. For address and data operands, the least significant byte of the word is stored in the lower value address location and the most significant byte is stored in the next higher address location. Two fetch or write cycles will be automatically executed for 16-Bit operands.

Maximum mode is achieved by strapping pin 33 (MN/MX-N) to ground. In maximum mode the signals required for operating the 8087 math coprocessor are produced. The status signals SO-N to S2-N are used by the bus controller 8288 to produce command and bus control signals.

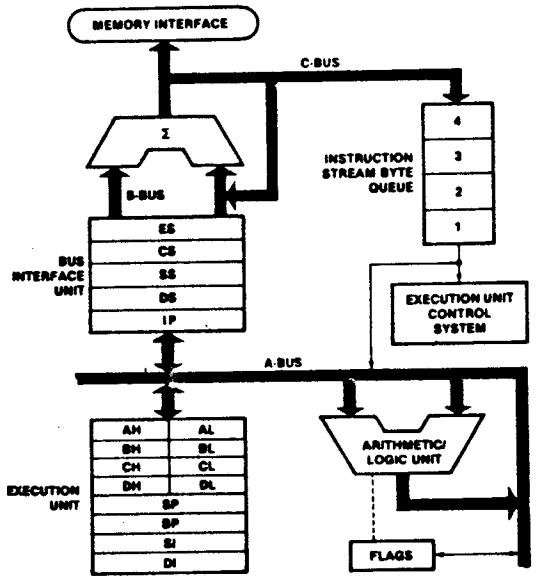

Figure 3.6 iAPX 88/10 (8088) - Block Diagram.

4.3.2 FUNCTIONAL DESCRIPTION

Address/Data Bus Signals:

AD0 to AD7 - Address data bus; these lines constitute the time multiplexed memory/IO address (T1) and data (T2, T3, Tw and T4) bus. These lines are active HIGH and float to 3-state OFF during interrupt acknowledge and local bus hold acknowledge.

A8 to A15 - Address bus; these lines provide address bits 8 to 15 for the entire bus cycle (T1 to T4). These lines do not have to be latched by ALE to remain valid. A15 to A8 are active HIGH and float to 3-state OFF during interrupt acknowledge and local bus hold acknowledge.

A16 to A19 - Address/Status (S3 to S6); during T1, these are the four most significant address lines for memory operations. During I/O operations, these lines are LOW. During memory and I/O operations, status information is available on these lines during T2, T3 Tw and T4. S6 is always LOW. The status of the interrupt enable flag bit (S5) is updated at the beginning of each clock cycle.

S4 and S3 signify the following:

S4	S3	Characteristics
0	0	Alternate data
0	1	Stack
1	0	Code or none
1	1	Data

This information indicates which segment register is being used for data accessing. These lines float to 3-state OFF during local bus hold acknowledge.

Control Bus Signals:

SO-N to S2-N - Status; is active during clock high of T4, T1 and T2 and is returned to the passive state (1,1,1) during T3 or during Tw when READY is HIGH. This status is used by the 8288 Bus Controller to generate all memory and I/O access control signals. Any change of S2-N, S1-N or SO-N during T4 is used to indicate the end of a bus cycle.

SO-N, S1-N and S2-N signify the following:

SO-N	S1-N	S2-N	Characteristics
0	0	0	Interrupt acknowledge
1	0	0	Read I/O Port
0	1	0	Write I/O Port
1	1	0	Halt
0	0	1	Code access
1	0	1	Read memory
0	1	1	Write memory
1	1	1	Passive

These signals float to 3-state OFF during hold acknowledge.

READY - READY; is acknowledgement from an addressed memory or I/O device that data transfer will be completed.

CLK - CLOCK; provides basic timing for the processor and the bus controller. It is asymmetric with a 33% duty cycle.

RES - RESET; causes the processor to terminate current activity. The signal must be active (HIGH) for at least 4 clock cycles.

INTR - Interrupt Request; is sampled during the last clock cycle of each instruction to determine if interrupt acknowledgement is required.

Additional Signals:

TEST-N - TEST; "wait for test" instruction not used. Strapped HIGH.

NMI - NON MASKABLE INTERRUPT; strapped to ground.

MX-N - MAXIMUM/MINIMUM MODE; strapped to ground giving maximum mode

Bus Operation:

The three parts of the 8088 address/data bus are the lower eight address/data bits (AD0-AD7), the middle eight address bits (A8-A15), and the upper four address bits (A16-A19). The address/data bits and the highest four address bits are time multiplexed.
The middle eight address bits are not multiplexed, they remain valid throughout each bus cycle.

Each processor bus cycle consists of at least four CLK cycles. These are referred to as T1, T2, T3 and T4. The address is emitted from the processor during T1 and data transfer occurs on the bus during T3 and T4. T2 is used primarily for changing the direction of the bus during read operations. In the event that a 'NOT READY' indication is given by the device, "wait" states (Tw) are inserted between T3 and T4. Each inserted "wait" state is of the same duration as a CLK cycle.
Idle periods can occur between 8088 driven bus cycles. These periods, which are inactive CLK cycles, are used by the processor for internal housekeeping.

During T1 of any bus cycle, the ALE (address latch enable) signal is emitted by the 8288 bus controller. At the trailing edge of this pulse a valid address and certain status information may be latched.

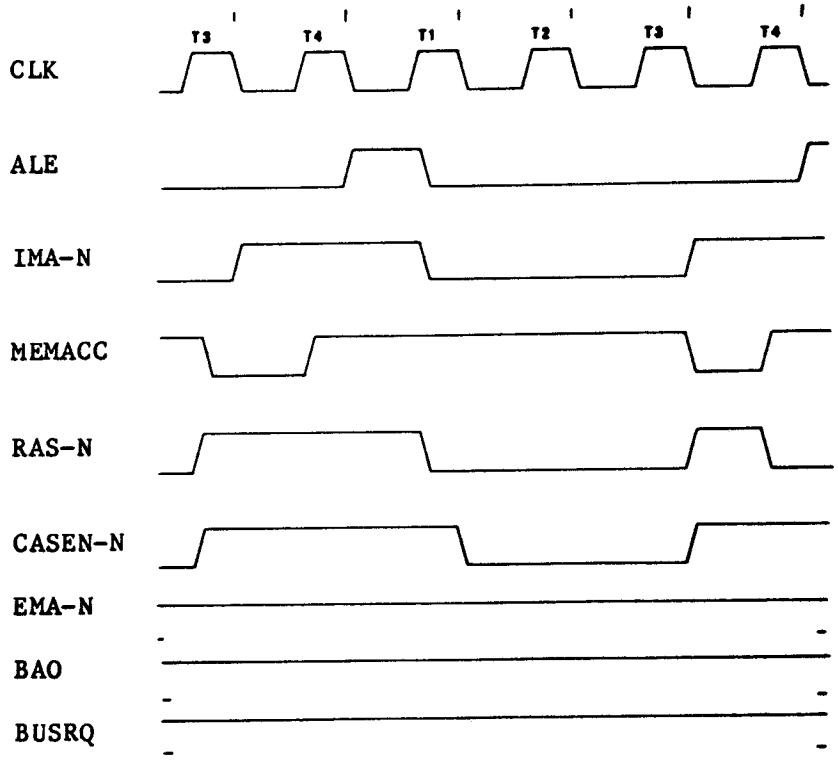

Figure 3.7 iAPX 88/10 Timing Diagram - Internal Memory Access

4.4 Z80A Interface

4.4.1 GENERAL

The interface between the Copower Board and the Mainboard allows an interchange of data in common (Mainboard) memory between the two processors. In addition to the address and data lines, the following control signals are available at the extension interface:

RES-N; BUSRQ-N; BUSAK-N; phi; EINT-N; BAO-N;

MRQB-N; RDB-N; WRB-N; IORQB-N; M1B-N

4.4.2 FUNCTIONAL DESCRIPTION

RES-N

Active (LOW) at 'power on' or RESET, this signal on the Clear input of the RESET flip-flop (item 7022/2) causes RES88-N to become active (LOW), resetting the 8088 CPU. The RES-N will also cancel a LOCK condition by clearing the LOCK flip-flop (item 7022/1).

Resetting the 8088 CPU does not affect the refresh cycle, ensuring that the contents of Copower Board RAM are not disturbed.

With RES-N inactive (HIGH), LOCK can be set-up by writing 1 to data bit 0. PORTSET-N is then required to initiate the LOCK signal.
In a similar way, an 8088 reset can be initiated by writing 0 to data bit 1; followed by PORTSET-N. PORTSET-N becomes active during an I/O WR operation of the Z80A to the appropiate address. The contents of the Z80A databus must contain appropriate data.

The LOCK is activated, by the Z80A CPU, to prevent the 8088 CPU accessing the common memory during time critical Z80A operations. LOCK disables the BUSRQ-N from the 8088.

BUSRQ-N

Active (LOW) when the 8088 requires access to the mainboard address bus. BUSRQ-N is disabled by the LOCK signal.

BUSAK-N

Active (LOW) when the Z80A CPU grants bus access.

phi

Z80A system clock (4 MHz). Synchronises the 8088 bus access signals to the Z80A.

If the 8088 attempts to access the shared, or external, memory the address lines A16L to A19L will be HIGH (shared memory is at locations F0000 to FFFFF as seen from the 8088). These four address lines, gated with RA-N (refresh access) and MEMACC (active HIGH if either S0-N and/or S1-N are LOW and S2-N is HIGH); produce the J input to JK flip-flop item 7051 - pin 8.
If external memory access is allowed Q-N will be LOW and fed to the D input of item 7052. This will set the Q output LOW (BUSRQ-N active).

BUSRQ-N can be suppressed by:

- RA-N active [refresh active] or
- LOCK active [Z80A accessing shared memory]
- MEMACC - ALE

The resultant BUSRQ-N active will be sent to Z80A and, if access granted, will result in BUSAK-N going active. This will shut-off the phi input to item 7052.

EINT-N — External interrupt (8088 to Z80A). Uses the AIOWC-N from the bus controller with status lines S0 to S2. set to 0; 1; 0.

BAO-N — Used as control signal for latching data and address information between the 8088 and Z80A. Also used to control (3-state) the MREQ-N, MRDC-N and AMWC-N signals.

MREQ-N — Derived from 8088 generated EMA-N (external memory access). This signal is seen as MRQB-N by the Z80A.

Any memory access will drive either EMA-N or IMA-N active. Pin 9 of item 7049 will be "1" if any of the 4 higher address bits are "0". Pin 5 (BAO) will be "1" if BAO-N is active. This feeds MREQ-N, via item 7053/3, to become MRQB-N.

MRDC-N — Memory Read Command. Output from the bus controller. This signal depends on 8088 CPU status bits (S0 - S2) and is seen as RDB-N by the Z80A. controlled by BAO-N as above.

AMWC-N — Memory Write Command. Output from the bus controller. This signal depends on 8088 CPU status bits (S0 - S2) and is seen as WRB-N by the Z80A. Controlled by BAO-N as above.

IORQB-N
M1B-N — From Z80A, active LOW. When WRB-N is active (LOW) the 3-bit binary decoder (item 7030) will decode addresses between 30H and 3FH to give IVSET-N (even addresses) or PORTSET-N (odd addresses). Synchronised by Z80A M1B-N.

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4.5 RAM Banks

4.5.1 GENERAL

The 8088 Copower Board RAM can be fitted with:

- two banks of 64KBit RAMs; HM4864 random access memories
- one bank of 256KBit RAMs; HM41256 random access memories
- two banks of 256KBit RAMs; HM41256 random access memories

RAM Bank0 consists of items 7001 to 7008,
RAM Bank1 consists of items 7009 to 7016.

RAM interface is via:

- Address lines MA0 - MA8
- RAS-N
- AMWC-N (used as WE-N), and
- CAS0-N or CAS1-N
- Data IN/Data OUT lines AD0 - AD7

CAS0-N and CAS1-N, the bank select signals, are derived from the address bits A16L to A19L when CASEN-N is active.
Data lines AD0 - AD7 are in parallel for the two banks.

Pin 1 (MA8) of the 64KByte RAM is not connected internally.

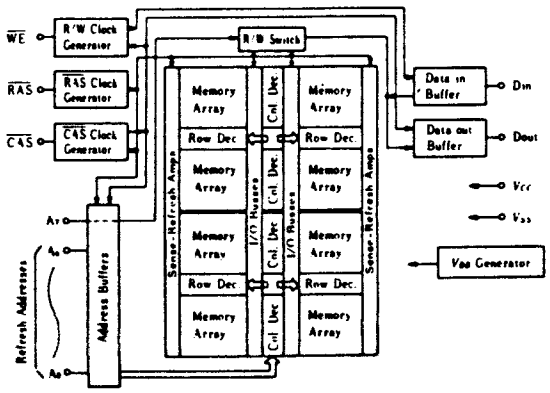

Figure 3.8 Dynamic RAM HM4864 - Block Diagram

4.5.2 FUNCTIONAL DESCRIPTION

4.5.2.1 RAM Addressing

The RAM address to be accessed is set-up by the 8088 CPU on address lines AD0 to A16 (2 x 64KBytes) or address lines AD0 to A18 (2 x 256KBytes). Jumper positions for the two sizes of RAM that may be fitted are given below:

	2 x 64KBytes	2 x 256KBytes
J1, J3, J5	closed	open
J2, J4, J6	open	closed

ADDRESS SELECTION:

The low order part of an address designates the ROW, and the high order part the COLUMN, of a location within a RAM chip. A location is accessed by setting up the ROW ADDRESS and sending a row address strobe (RAS) and then setting up the COLUMN ADDRESS and sending a column address strobe (CAS). The content of the addressed location will be made available at the output of the RAM. If the Write Enable signal is active (WE-N), the level at the input of the RAM will be written to the addressed location. As all 8 RAMs in a bank are addressed and strobed simultaneously, all 8 bits will be read or written at the same time.

The low order part of the address, on the combined address/data bus, is first 'latched' into item 7018 with the ALE (address latch enable). With ENILO-N active (LOW) the RAS-N signal going LOW strobes the row address on BOTH RAM Banks.

The high order part of the address does not need latching as it is available during the complete cycle.
After strobing the row, the column address is placed on the MA bus when the signal ENIHI-N becomes active, and a column address strobe sent to ONE of the RAM Banks. (See next page).

Depending on the size of RAM, the address lines are:
- 2 x 64KBytes: low part = AD0 to AD7; high part = A8 to A15
- 2 x 256KBytes: low part = AD0 to A8; high part = A9 to A17

Three elements of item 7021, tri-state bus drivers, are used to pass the higher bits of each part of the address in the 256KByte configuration.
When the 64KByte configuration is used, address bit A8 is fed onto the MA bus as the most significant bit of the higher part of the address, instead of as the least significant bit. This means that logically adjacent locations will not be physically adjacent, but it allows the address decoders to operate with both sizes of RAM.

BANK SELECTION WITH 2 x 64KByte RAM:

The physical location of an address, bank0 or bank1, is determined by the magnitude of the address; locations up to 0FFFFH being in bank0 and locations 10000H to 1FFFFH in bank1.
Reading or writing to memory is initiated by sending a Column Address Strobe (CAS) to the RAM with the column address set up on the MA bus. The address line (A16L) is used to decide whether the CAS should be sent to bank0 (CAS0-N) or to bank1 (CAS1-N).

The higher address bits, A16 to A19, are first latched with ALE in item 7034. The lines are decoded by item 7027 and, with A17L to A19L LOW a location in internal (8088) memory is indicated. The output of item 7027, when gated by the CASEN-N signal, will be controlled by the level of A16L and will be CAS0-N or CAS1-N.

BANK SELECTION WITH 2 x 256KByte RAM:

The situation is exactly the same as described above with the following exceptions:

° bank0 contains locations up to 3FFFFH
° bank1 contains locations 40000H to 7FFFFH
° address line A19L LOW indicates internal memory
° With A19L LOW, item 7027 output will be controlled by A18L.

	Internal memory if LOW	Bank0 if LOW	Bank1 if HIGH
2 x 64K ..	A19, A18, A17	A16	A16
2 x 256K ..	A19	A18	A18

4.5.2.2 Memory Refresh and Access

REFRESH:

In order to 'refresh' the dynamic RAM the 'RAS-N only' method is used, where each row is addressed at the same time as 'RAS-N' is active. It is not necessary, but allowed, to address the highest address line. As the Copower board refresh circuitry addresses lines MA0 to MA7 it will work with both 64KB and 256KB RAM's.
The complete 64KB memory must be refreshed within 2 milliseconds and the 256 KB memory within 4 milliseconds.

Circuit items 7019 and 7020 are used to set up the row to be refreshed; the output of the counter (item 7020) is placed on the MA bus by the signal RA-N; followed by the RAS-N signal which 'strobes' one row of memory. RESRC-N is then produced, which terminates RAS-N and RA-N. The derived signal, RESRC, is used to increment the counter (item 7020) ready for the next refresh cycle.
Circuit items 7038 - 7037 and associated logic act as a 'sequencer', producing the following signals as required:

MREQ-N; RESRC-N; CASEN-N; RAS-N; ENIHI-N/ENILO-N;

If the three inputs to item 7043 (at pins 3, 4 & 5) are HIGH, indicating NO refresh or memory access, item 7038 will be in a reset state with pin 11 HIGH and pins 12, 13 & 15 LOW. The logic holds all outputs of item 7037 inactive (HIGH).

REFREQ (refresh request) is produced at item 7028 by the 64th CLK pulse and fed to the D input of item 7035 with pin 13 HIGH.
This will produce a pulse (high) at item 7046 pin 5. The Q-N output of item 7035 will be synchronised to give a HIGH on item 7046 pin 4 (via JK flip-flop item 7044), to drive RA HIGH and RA-N LOW (active), providing no memory access is in progress. This has the following effects:

° 'Count' on item 7020 placed on MA bus by RA-N

pin 11 of item 7038 is HIGH; this is gated with RA HIGH which drives item 7046 pin 8 LOW, thus activating RAS-N and refreshing one row of RAM.

- Pin 3 of item 7043 LOW causes shift register (7038) to start, clocked by the OSC signal; the next four OSC pulses cause the following outputs:

pulse 1:- pin 15 HIGH (no effect with IMA-N HIGH)
pulse 2:- no effect
pulse 3:- pin 13 HIGH (no effect with IMA-N HIGH)
pulse 4:- pin 11 LOW, terminates the RAS-N pulse
pin 12 HIGH, activating RESRC-N. This signal resets the refresh timer (item 7028) and (inverted by item 7045, pin 6) increments the refresh counter (item 7020). RESRC-N is also used to CLR item 7035, driving pin 9 LOW and de-activating the RA-N. This resets the shift register (item 7038).

The cycle repeats, with RAM address row incremented each cycle.

As the 8 bit counter (item 7020) is incremented from 0 to 255 it will address a complete 64KB RAM (from 0 to 127) twice or a complete 256KB RAM (from 0 to 255) once. This causes a full refresh cycle of 1.6 milliseconds (3.2 milliseconds for 256 KB).

MEMORY ACCESS:

CPU cycle consists of at least four CLK cycles (T1 to T4).

If memory access is required with the same CLK pulse as a refresh access the refresh will take priority (item 7046 pin 3 LOW). Refresh request during any memory access cycle will be delayed until the 8088 cycle is complete.

The CPU indicates an access requirement with status bits S0 to S2 and the address to be accessed will be set up on AD0 to A19 at T1. At T2 the lines AD0 to AD7 will contain data to be written to memory or must be free to accept data to be read from memory.

The lines S0-N to S2-N (valid T4 - T2) are decoded by item 7048. A LOW (output pin 8) is produced if memory access is indicated, which will drive MEMACC HIGH via JK flip-flop item 7051.

This in turn is used as a CLR input to item 7052.
The ALE (CLK low of each 8088 T1 cycle) is used to clock the RESI&E signal to the 'memory access gates' item 7049.
In addition to the status lines indicating that memory access is required, the highest address lines A16 to A19 are decoded.
If all lines are '1', external memory is indicated (address FXXXXH); otherwise internal memory is indicated (address below F0000H)

Internal Memory Access:

Internal memory access is granted, IMA-N goes active (LOW), if:

° memory access required - status bits checked
° A16 - A19 not all HIGH (7049 pin 9)
° no Refresh cycle - HIGH from item 7046 pin 3
° T1 of 8088 cycle - ALE goes HIGH

IMA-N going active (LOW) has the following effects:

° Low to item 7046 pin 9 drives RAS-N active

as ENILO-N is active, LOW, this strobes the row address that was latched by ALE via item 7018

° Pin 4 of item 7043 LOW causes sequencer (7038) to start:

Pin 11 remains HIGH: no effect as RA remains LOW.

Next four OSC pulses cause the following outputs:

pulse 1:- pin 15 HIGH, gated with IMA HIGH to drive ENIHI-N LOW; ENILO-N HIGH
pulse 2:- no effect
pulse 3:- pin 13 HIGH, gated with IMA HIGH to drive CASEN-N LOW

CASEN-N produces CAS0-N or CAS1-N (depending on address ≙ RAMbank). With ENIHI-N active (LOW) this strobes the column address.
Depending on the chip write enable signal (AMWC-N from Bus Controller) the contents of RAM will be copied to or from the databus (AD0 to AD7).

pulse 4:- pin 12 HIGH, no effect as RA remains LOW
pin 11 LOW, no effect

At T3, status bits S0-N to S2-N go inactive. MEMACC then goes LOW, causing RESI&E to go LOW and terminating the IMA-N. This resets the sequencer, 7038, and the next 8088 cycle is started.

External Memory Access:

External memory access is granted, EMA-N goes active (LOW), if:

° memory access required - status bits checked
° A16 - A19 all HIGH (7049 pin 9)
° no Refresh cycle - HIGH from item 7046 pin 3
° T1 of 8088 cycle - ALE goes HIGH

° BAO (Bus Acknowledge Out) signal given by Z80 CPU

Before BAO can become active the following circuit actions must occur:-

Pin 6, item 7042 becomes HIGH - A16 - A19 HIGH/RA-N HIGH/MEMACC HIGH

This produces a LOW at pin 6 of item 7051. Providing the LOCK signal is also LOW the BUSRQ-N signal will be driven active (LOW). This will result in a BUSAK-N signal from the mainboard, which will hold the BUSRQ-N signal until the end of the 8088 cycle. The Z80A will then activate the BAO signal to initiate the EMA-N signal.
This, in turn, will initiate the MREQ-N signal to the Z80A CPU.

BAO-N will also enable the external memory address onto the Z80A bus and move the data to or from the Z80A data bus as appropriate.

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4.6 Maths Co-Processor (8087)

4.6.1 GENERAL

It is possible to fit an Intel 8087, which will upgrade the iAPX 88/10 CPU to an iAPX 88/20 Numeric Data Processor. With this upgrade the 88/20 provides 100 times the performance of the 88/10 alone for numeric processing. It must be stressed that this enhanced performance is only available in the case of application programs written with the 8087 Maths Co-Processor in mind and will have no effect on standard programs.

It is not feasible to present details of the device in this manual, but full details can be found in the Intel Microprocessor and Peripheral Handbook.

Fitting instructions for the 8087 will be available from your dealer.